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The Hybrid Integrated Circuit of the ALICE Inner Tracking System upgrade

G. Fiorenza, V. Manzari, C. Pastore and V. Valentino

INFN, Sezione di Bari - Bari, Italy

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Summary. — The upgrade of the Inner Tracking System scheduled during the second long shutdown is an important milestone of the ALICE upgrade and it will provide a high improvement of its performances. In this contribution the smallest operator unit of the detector, the Hybrid Integrated Circuits, is presented.

1. – Introduction

ALICE [1] (A Large Ion Collider Experiment) is an experiment at the Large Hadron Collider (LHC) aimed to the study of heavy-ion collisions. ALICE is preparing a major upgrade of its experimental apparatus and in particular of the Inner Tracking System, planned for the installation during the second long shutdown in the 2019–2020. A key element of the upgrade is the construction of a new, high-resolution, low-mass 7-layers silicon tracker based on monolithic pixel detectors. The ITS upgrade [2] includes different advantages: reduction of the distance of the first detection layer from the interaction point to improve the measurement of the impact parameter resolution and reduction of the material budget to improve the tracking performances and momentum resolution.

2. – New ITS layout

The geometry of the new ITS provides a grouping of seven layers in two separate barrels (Inner and Outer). The Inner Barrel consists of three innermost layers while the Outer Barrel contains two middle layers and two outermost layers. The ITS layers are azimuthally segmented in units named Staves which are split into two Half-Staves glued on a lightweight carbon fiber structure, for the Outer Barrel. Each Half-Stave consists of 4 or 7 Hybrid Integrated Circuits (HIC), for the middle and outer layers, respectively. The HIC is the smallest operable unit of the detector and consists of an array of 2×7 pixel chips (15 mm wide, 30 mm long and 0.05 mm thick) connected to a Flexible Printed Circuit (FPC) (33 mm wide, 210.6 mm long and 0.15 mm thick) by

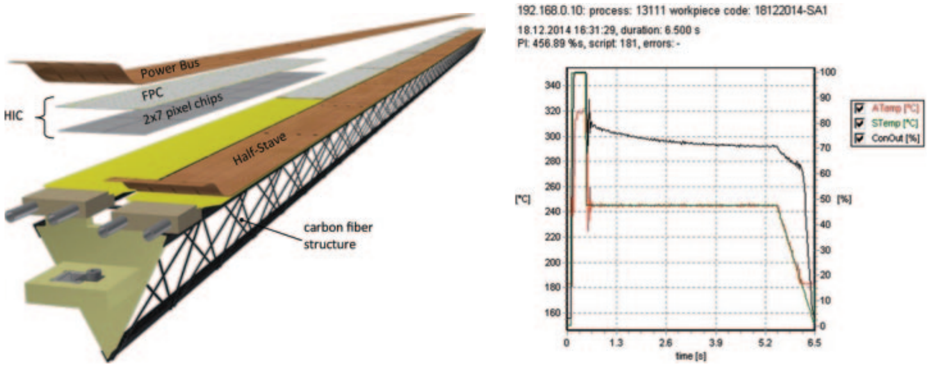

Fig. 1. – Schematic exploded view of the Outer Barrel Stave (left). Temperature profiles and Power Integral recorded during a soldering process (right).

means of a laser soldering technique. All chips in a HIC are directly connected to the analog and digital power planes of the FPC, which are fed by the Power Bus serving each Half-Stave.

3. – HIC assembly procedure

The design of the jigs and the movement procedures developed, guarantee a geometrical placement accuracy of the individual chip in the horizontal plane of $\pm 5\,\mu$m. The first step in the HIC assembly procedure is the alignment of 14 chips on a vacuum assembly table in nominal position with respect to the reference markers. Then the FPC is cleaned in an ultrasound bath and aligned above the chips array referring to three dowel pins on the jig. A macor soldering grid, 1 mm thick with an array of conical holes matching the FPC holes and the chips pads, is placed on the FPC. The grid presses the FPC against the chips to minimize the gap in between and guides the soldering balls on the chips pads through the FPC holes. A dedicated vacuum tool is sequentially used to pick and place sets of soldering balls above the chip pads one after the other. The HIC assembly procedure is completed with the laser welding sequence of each ball/hole connection. In particular, a laser beam of $200\,\mu$m diameter melts locally each ball, avoiding thermal stress on the full HIC sandwich structure. Moreover, programmable temperature profile and laser power modulated by pyrometer, ensure a limitation of extra-heating. A first quality assurance of the soldered joint is given by the temperature profiles and by the value of the Power Integral shown in fig. 1. Furthermore HICs electrical and functional test will be carried out by means of a testing station. Next year six production centers will start the production of more than 2000 HICs by means of an automatic assembly system which will ensure a homogenous quality over the whole production.

REFERENCES

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