A Highly Digital Microbolometer ROIC employing a novel Event-based Readout and Two-Step Time to Digital Converters

by

SHAHBAZ ABBASI

Submitted to the Graduate School of Engineering and Natural Sciences
in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy

Sabancı University

March, 2019

A Highly Digital Microbolometer ROIC employing a Novel Event-based Readout and Two-Step Time to Digital Converters

APPROVED BY

Prof. Dr. Yaşar GÜRBÜZ
(Thesis Advisor) .....

Assist. Prof. Dr. Ömer CEYLAN .....

Assist. Prof. Dr. Erdinç ÖZTÜRK .....

Prof. Dr. Uğur ÇİLİNGİROĞLU .....

Prof. Dr. Arda Deniz YALCİNKAYA .....

DATE OF APPROVAL: 25th March 2019

To My Parents
Who always have sacrificed
their needs for my needs...

The more you know, the more you realize how much you don't know...
(David T.Freeman)

Acknowledgements

First of all, all the glory and praise be to Allah, The Almighty. He has been my strength when I was weak, my endurance when I was tired and my hope when I was lost.

My time at Sabanci University has been one of the best and most enjoyable journeys of my life. I have grown both professionally and socially, thanks to the experience that I had.

First and foremost, it is my pleasure to express my deepest gratitude for my advisor, Professor Yaşar Gürbüz, for everything that he has taught me and done for me over the years. His patience and knowledge have not only helped me grow professionally, but also expanded my horizon and understanding of what it means to be a great researcher. I cannot begin to imagine how the invaluable skills that I have learnt from you will help me find my future paths and grow beyond the man that I am today.

I also would like to thank Professor Meriç Özcan, Professor Erdinç Öztürk and Professor Murat Kaya for being on my dissertation committee. Though briefly, it has been an honor to have interacted and worked with you in the past and to have had you during my PhD qualification examination.

I would really like to express my gratitude to Mehmet and Canan, for all the technical help, and IHP for chip fabrication.

Next, I would like to thank my colleagues from the SUMER group for all the social interaction and technical discussions that have helped me go this far. This includes Atia Shafique, Ömer Ceylan, Cern Ninan, Melik Yazici, Arman Galioğlu, Can Çalışkan, İlker Kalyoncu, Aburrahman Burak, Alper, Eşref Türkmen and Elif Gül. Many of you have helped me through some of the toughest times at Sabanci, and these memories would undoubtedly stay with me wherever I go.

My journey at Sabanci would not have been so fulfilling and complete without the support of my family. For that, I would like to thank my wife, parents and siblings. I am eternally grateful for your never ending love and support. I am sorry to have been living away from you (parents and siblings) for quite a few years now; but I hope that this small accomplishment could partly express my gratitude for the countless sacrifices that you made for me. This work and my humble accomplishment today are entirely dedicated to you.

A Highly Digital Microbolometer ROIC employing a novel Event-based Readout and Two-Step Time to Digital Converters

Shahbaz Abbasi
EE, Ph.D. Thesis, March 2019
Thesis Advisor: Prof. Dr. Yaşar Gürbüz

Keywords: Long-wave infrared, uncooled microbolometer, readout integrated circuit, time-mode processing, low power, NETD, self-heating.

Abstract

Uncooled infrared imaging systems are a light weight and low cost alternative to their cooled counterparts. Uncooled microbolometer IR focal plane arrays (IRFPAs) for applications such as medical imaging, thermography, night vision, surveillance and industrial process control have recently been under focus. These systems have small pixel pitches ($< 25\mu$m) and require power efficiency, low noise equivalent temperature difference (NETD) (< 50 mK) and adequate scene dynamic range (> 250 K). Low NETD demands excellent microbolometer and readout noise performance. If sensitive analog circuits, driving long metal interconnects, are part of the pre-digitization readout channel, this necessitates the use of power consuming buffers, potentially in conjunction with noise cancellation circuits that result in power and area overhead. Thus re-thinking at the architectural level is crucial to meet these demands.

Accordingly, in this thesis a column-parallel readout architecture for frame synchronous microbolometer imagers is proposed that enables low power operation by employing a time mode digitizer. The proposed readout circuit is based on a bridge type detector network with active and reference microbolometers and employs a capacitive transimpedance amplifier (CTIA) incorporating a novel two-step integration mechanism. By using a modified reset scheme in the CTIA, a forward ramp is initiated at the input side followed by the conventional backward integrated ramp at the output. This extends the measurement interval and improves signal-to-noise ratio (SNR). A synchronous counter based TDC measures this interval providing robust digitization. This technique also provides a way of compensating for self-heating effects.

Being highly digital, the proposed architecture offers robust frontend processing and achieves a per channel power consumption of 66 μW, which is considerably lower than the most recently reported designs, while maintaining better than 10-mK readout NETD.

Mikrobolometreler İçin İki Aşamalı Zamandan Sayısala Dönüştürücü İçeren ve Asenkron Çalışan Yeni Bir Sayısal Tümleşik Okuma Devresi

Shahbaz Abbasi
EE, doktora Tezi, 2019
Tez Danışmanı: Prof. Dr. Yaşar GÜRBÜZ

Anahtar Kelimeler: Uzun-dalga kızılötesi, soğutmasız bolometre, öngörücü model, TCAD, Si/SiGe çoklu-kuantum kuyusu, yüksek Ge içeren SiGe bolometre, yüksek TCR (sıcaklığa bağlı direnç değişim katsayısı), düşük gürültülü bolometre

Özet

Soğutmasız kızılötesi görüntüleme sistemleri, soğutmalı emsallerine göre hafif ve düşük maliyetli bir alternatiftir. Soğutmasız kızılötesi görüntüleme sistemlerinin en bilinenlerinden biri olan mikrobolometreler tıbbi görüntüleme, termografi, gece görüşü, gözetleme ve endüstriyel proses kontrolü gibi uygulamalar için son yıllarda artarak devam eden araştırmalara konu olmuştur. Bu sistemlerin küçük piksel aralıklarına ($< 25\ \mu$m) sahip olması, enerji verimliliklerinin yüksek olması, gürültü performansının yüksek olması (NETD) (< 50 mK) ve yüksek dinamik aralığa ($>$ 250 K) sahip olması gerekmektedir. Düşük NETD mükemmel mikrobolometre ve okuma gürültüsü performansı gerektirir. Eğer hassas analog sinyaller uzun metal bağlantılarla bağlanmışsa, bu durum genellikle gürültü performansını iyileştirmek için yüksek güç tüketen ve fazla alan kaplayan tampon devreler gerektirir. Bu nedenle hem yüksek gürültü performansına ulaşan hem de düşük güç tüketip az alan kaplayan okuma devrelerinin geliştirilmesi için mimari düzeyde yenilikler gerekmektedir.

Buna bağlı olarak, bu tezde zaman uyumlu bir sayısallaştırıcı kullanarak düşük gürültülü çalışmayı mümkün kılan mikrobolometre okuma devreleri için sütun-paralel bir okuma mimarisi önerilmiştir. Önerilen okuma devresi, aktif ve referans mikrobolometrelere sahip olan köprü tipi bir dedektör ağına dayanmaktadır ve yeni bir iki aşamalı entegrasyon mekanizmasını içeren kapasitif bir transpedans yükseltecini (CTIA) kullanmaktadır. CTIA'da modifiye edilmiş bir sıfırlama şeması kullanılarak, giriş tarafında ileri bir rampa ve ardından çıkışta geleneksel geriye entegre eden rampa kullanılır. Bu metod, ölçüm aralığını uzatır ve sinyal-gürültü oranını (SNR) iyileştirir. Senkron bir sayaç tabanlı zamandan sayısala çevirici (TDC), bu aralığı ölçerek sağlam dijitalleştirme sağlar. Dahası, bu teknik aynı zamanda kendi kendine ısınma etkilerini telafi etmenin bir yolunu sağlar.

Yüksek dijitalliğe sahip olan önerilen mimari, güçlü ön uç işleme sunuyor ve en son bildirilen tasarımlardan oldukça düşük olan, kanal başına 66 μW güç tüketiyor. Bununla beraber 10 mK NETD değeri ile oldukça iyi bir gürültü performansı sunuyor.

Contents

List of Figures

List of Tables

List of Abbreviations

AC	Alternating Current
a-Si	Amorphous Silicon
BCDI	Bolometer current direct injection
BW	Bandwidth
CCBDI	Constant Current Buffered Direct Injection
CTIA	Capacitive Transimpedance Amplifier
CDS	Correlated Double Sampling
DC	Direct Current
DR	Dynamic Range
FOM	Figure-of-Merit
FPA	Focal Plane Array
Ge	Germanium
IR	Infrared
LDO	Low Dropout
LWIR	Long Wavelength Infrared
MCT	Mercury Cadmium Telluride
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MWIR	Mid-Wavelength Infrared
NEP	Noise Equivalent Power
NETD	Noise Equivalent Temperature Difference
NMOS	Ntype MOSFET
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PIN	Ptype-Intrinsic-Ntype
PMOS	Ptype MOSFET
PSD	Power Spectral Density
R	Resistance
RMS	Root Mean Square
ROIC	Readout Integrated Circuit
Si	Silicon
SNR	Signal-to-Noise Ratio
SOI	Silicon on Insulator
SWAP	Size Weight and Power
SWIR	Short Wavelength Infrared
TCR	Temperature Coefficient of Resistance
TDC	Time-to-Digital Converter
TSI	Two-Step Integration
VCCS	Voltage Controlled Current Source
VGA	Variable Gain Amplifier
WBDA	Wheatstone Bridge Differential Amplifier
ZnSe	Zinc Selenide

1 Chapter 1
Introduction

1.1 Motivation

Much research in recent years has focused on uncooled infrared (IR) imaging systems [1–3]. These systems have small pixel pitches ($< 25\mu$m) and require power efficiency, low noise equivalent temperature difference (NETD) (< 50mK) and adequate scene dynamic range (> 200K).

Application requirements of microbolometer based imaging systems are pointed out in Fig. 1.2. While recent developments in microbolometer detector technology have allowed the reduction of cost and size, improvements are still required on the readout front to lower the overall power consumption and to enable FPAs with small pixel size (pitch). The figures of merit, related to microbolometer imagers, that are directly affected by these requirements include NETD and readout dynamic range (digital resolution). A low NETD demands excellent readout noise performance which becomes a challenge if noisy analog circuits are to be implemented off-pixel. This is because long metal interconnects commuting sensitive analog signals necessitate the use of power consuming buffers, potentially in conjunction with noise cancellation circuits that can be an additional power and area overhead. Moreover, high readout dynamic range also requires adequate performance on multiple fronts. In addition to circuit imperfections such as offset and noise, self-heating of the microbolometer detector also makes the required dynamic range unnecessarily large, resulting in a higher power consumption and potential complexities in the readout circuit chain. In short, achieving a low NETD and a large readout dynamic range becomes a challenge with power and size constraints.

Low noise performance could be achieved with a pixel-parallel readout architecture in which the digitization takes place inside the pixel. However, with a small pixel pitch, this approach severely limits the achievable resolution. This leaves us with architectures that use off-pixel circuitry to perform the digitization and possibly part of the signal conditioning as well. One of the limiting elements in achieving high precision with low power consumption in such architectures is the pre-digitization

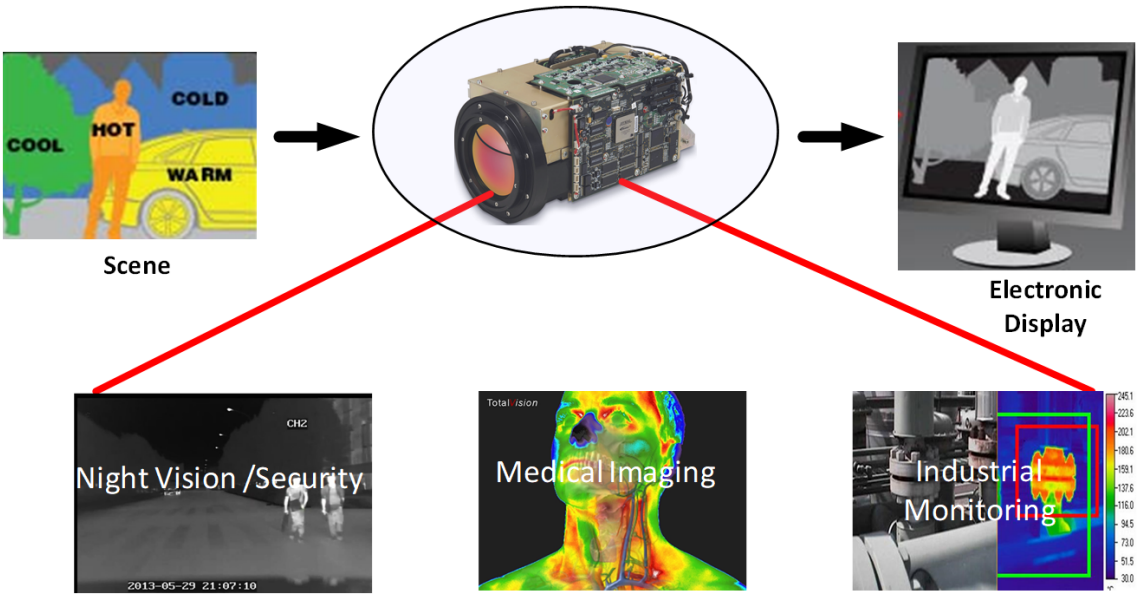


Figure 1.1: Applications of thermal IR cameras

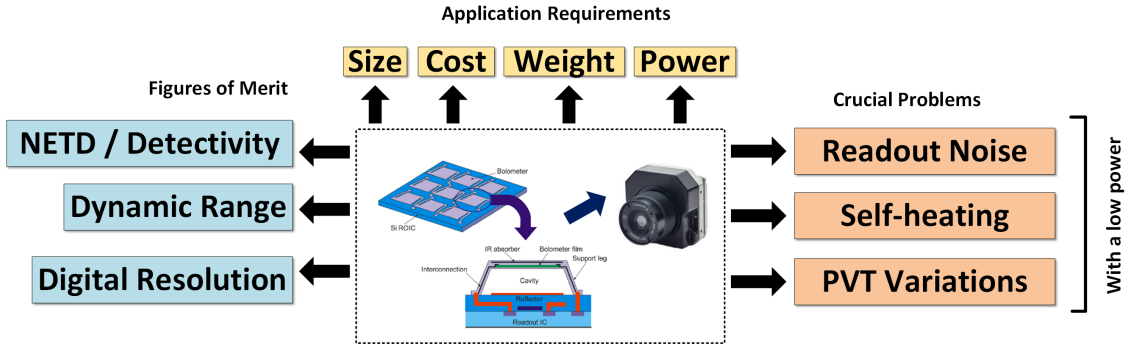


Figure 1.2: Application Requirements and Figures of Merit of Microbolometer Imagers

analog signal path that is typically and primarily comprised of a current to voltage pre-amplifier, an offset/noise canceling circuit and a sample and hold circuit. These are power hungry circuits made to drive large loads in such architectures. Therefore, there is a clear need to re-invent the readout chain in a non-pixel-parallel architecture to improve noise performance while keeping the power consumption on the lower side. Time mode circuits are a potential candidate since such circuits are predominantly comprised of digital circuits (gates, flip-flops etc.) and can, in principle, offer a robust alternative to analog chains [4]. Moreover, the time-based outputs of such circuits can be readily converted to digital using time-to-digital converters (TDCs) without having to be intermediately converted to a voltage.

On top of the low noise requirement, achieving a good image quality and high digital resolution requires controlled low offsets and the compensation/cancellation

of the very specific effect of self-heating found in microbolometers. Effects of offsets are typically mitigated by the use of calibration circuitry or special offset subtracting amplifiers such as the widely used correlated double sampling (CDS) circuit [5, 6]. Calibration usually requires foreground operation in which the camera shutter is closed and the circuits are calibrated for offset variations [7,8]. Whereas, CDS circuit requires an operational amplifier (opamp) and additional sampling capacitors costing power and area. Thus, low-power and calibration-free approaches are desirable to circumvent these problems.

1.2 Research Contribution and Thesis Organization

In this thesis, we present the design and analysis of a highly digital readout architecture for microbolometer imagers implemented in a 130-nm Bulk CMOS technology. The presented architecture advances the state-of-the-art by simultaneously implementing digital offset correction, and achieving a low NETD ($<$ 10 mK) and low power consumption ($<$ 100 μW per readout channel). This combination of performance is accomplished via the use of a time-mode readout channel that employs a novel current-to-time conversion circuit followed by a two stage time to digital converter. Two-step time to digital conversion is realized using a counter as the first stage and an inverter-based delay line as the second stage. The counter is 12-bit wide and the delay line provides 4 least significant bits. The TDC resides in the column and serves a single column of the imager.

Furthermore, an innovative reset scheme is used in the frontend amplifier that aids in cancellation of the self-heating effect. The proposed architecture improves the NETD and dynamic range (DR) of the microbolometer FPA and makes its performance less dependent on circuit imperfections. Though the solution comes at the cost of some added complexity in array control, the circuit simplicity and robustness of the time-based signal path compensates for it.

This thesis is organized as follows: Chapter 2 briefly reviews the fundamentals of microbolometer imaging and introduces the various readout architectures typically employed in IR imagers. Chapter 3 then delves into the design details and requirements of a conventional CTIA based readout architecture and provides a detailed analytical treatment of aspects like noise and linearity. Next, Chapter 4

introduces the proposed time-mode readout architecture and examines the noise and power trade-off of the architecture. This is followed by the implementation details and measurement results of our prototype ROIC in Chapter 5. Finally, Chapter 6 suggests future work directions and closes the thesis with a conclusion.

2 Chapter 2

An Overview of Microbolometer Imaging

In this chapter, a review of the operating principles, fundamental figures of merit and performance parameters of resistive microbolometers are presented. Furthermore, an analytical model is discussed that allows crucial insights into the dynamic electro-thermal behavior of microbolometers.

2.1 Infrared Imaging

Infrared (IR) radiation is found on the electromagnetic spectrum between wavelengths of 1 μm and several tens of μm [9]. IR Imaging technology has seen major research interest in recent times owing to its special imaging capabilities. Industrial, commercial and military systems have been making use of these capabilities for applications such as surveillance, night vision, process monitoring and medical imaging. Selection criteria of the infrared detector type for these applications is determined by the temperature range of the targets and the atmospheric transmission characteristics as shown in Figure 2.1. 3 μm - 5 μm band in medium-wave infrared (MWIR) and 8 μm - 12 μm band in long-wave infrared (LWIR) are the most commonly used spectral windows. The atmospheric absorption is at considerably low levels in these bands.

IR imaging systems have become mainstream components in various military and commercial applications. Two main categories of IR imaging technologies can be found: cooled and uncooled. A component wise breakdown of these technologies is shown in Figure 2.3. The cooled technology incorporates IR detectors with required operating temperatures far below room temperature achieved by combined cryo cooler. Cooled cameras offer superior sensitivity to IR radiation owing to the considerably reduced thermal noise. This advantage comes at the expense of bulky size and increased cost. Moreover, the imaging speed and magnification capabilities of cooled cameras are also much higher compared to their uncooled counterparts.

An excellent low cost alternative to the expensive cooled IR systems is the uncooled IR technology. Uncooled IR detectors operate at room temperature 298 K $\sim$ 300 K.

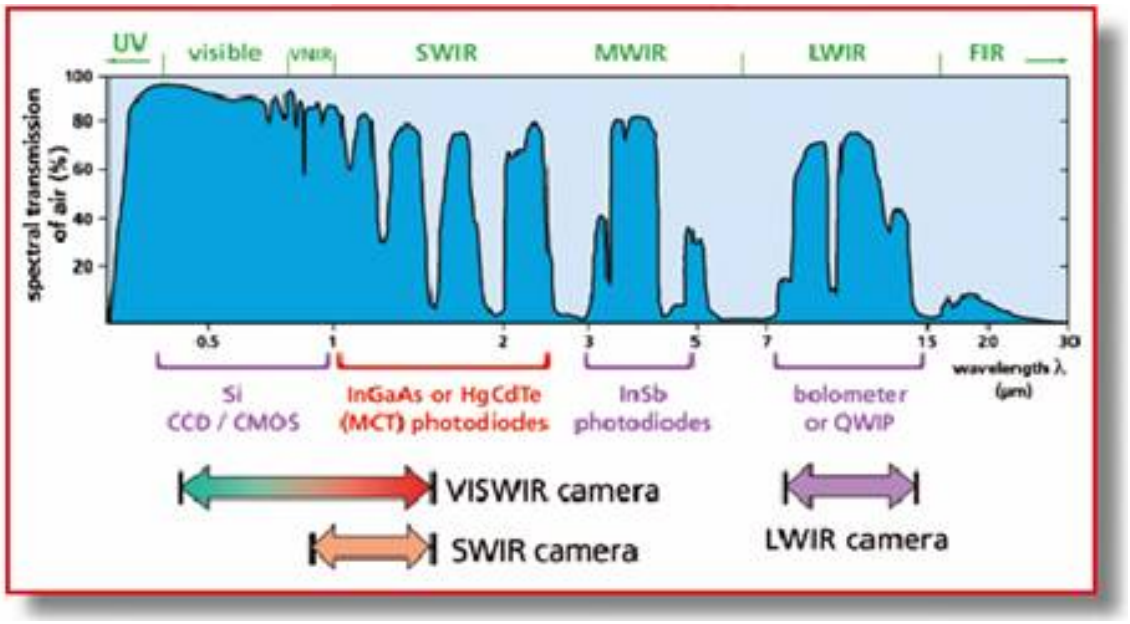


Figure 2.1: Infrared Spectrum (http://www.adept.net.au)

Due to the absence of cooling systems, such imaging systems are highly maintainable and offer unprecedented benefits in terms of cost and size. Such cameras are typically employed in LWIR imaging applications. A typical unit pixel architecture of photon and thermal FPAs is shown in Figure 2.4.

2.1.1 Uncooled Resistive Microbolometer Detectors

There are three types of uncooled thermal detectors namely (1) pyroelectric (2) thermoelectric and (3) resistive microbolometer detectors. Pyro-electric detectors operate on the principle of electrical polarization which is caused under thermal drive due to absorbed IR radiations. Thermoelectric detectors, on the other hand, use the Seebeck effect between dissimilar metal to produce voltage change across its terminals in response to the temperature change. There has been little effort towards the development of such detectors due to their responsivity being on the lower side. The detection principle of resistive microbolometer relies on a change in the electrical resistance caused by the change in temperature due to absorbed IR illumination. Thermal isolation in these detectors is achieved by the mechanical suspension of the active part of the detector over a readout substrate. Typically, the IR camera comprises of the components illustrated in Figure 2.2.

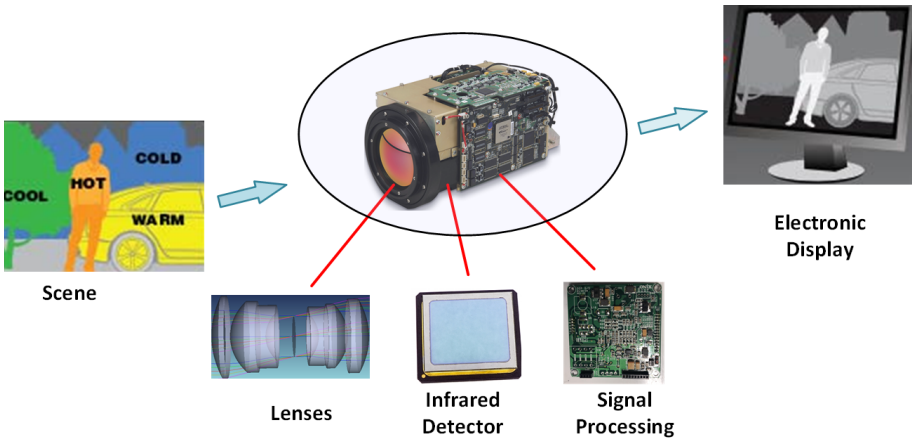


Figure 2.2: Components of an IR Camera [10].

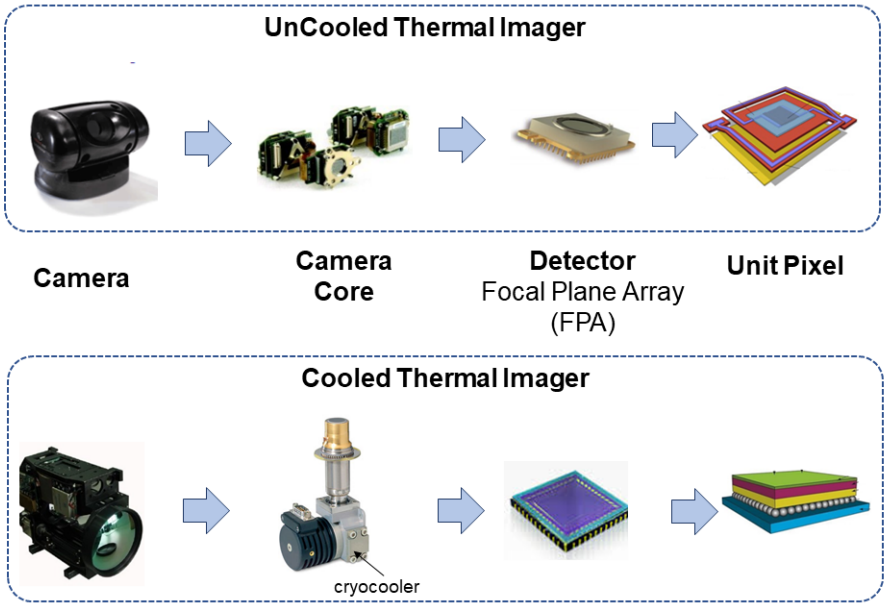


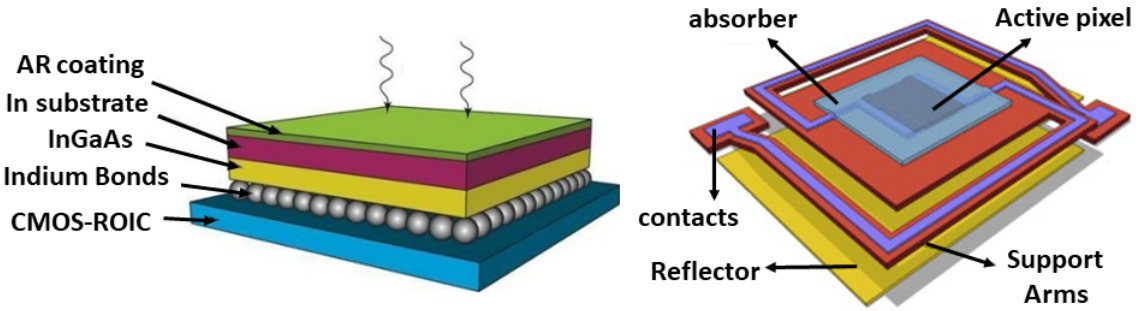
Figure 2.3: Technology perspective of cooled and uncooled IR cameras [11, 12].

2.2 Microbolometer Device Aspects

In this section, we define three important microbolometer design parameters: (1) Temperature dependent resistance, (2) Temperture coefficcient of Resistance and (3) Thermal Conductance.

2.2.1 Temperature-Dependent Resistance

The resistivity of the active part of the microbolometer, shown in Figure 2.6, is strongly temperature-dependent. The temperature change due to incident IR



(a) (b)

Figure 2.4: Unit pixel in a) photon detector using flip-chip technology for hybridization [13], b) thermal detector monolithically integrated and suspended over the ROIC [14].

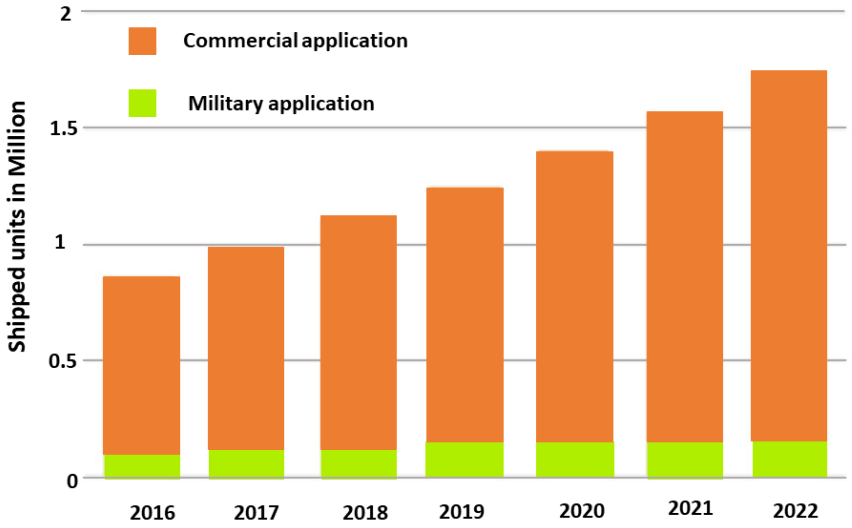


Figure 2.5: Uncooled thermal cameras in military and commercial applications [15].

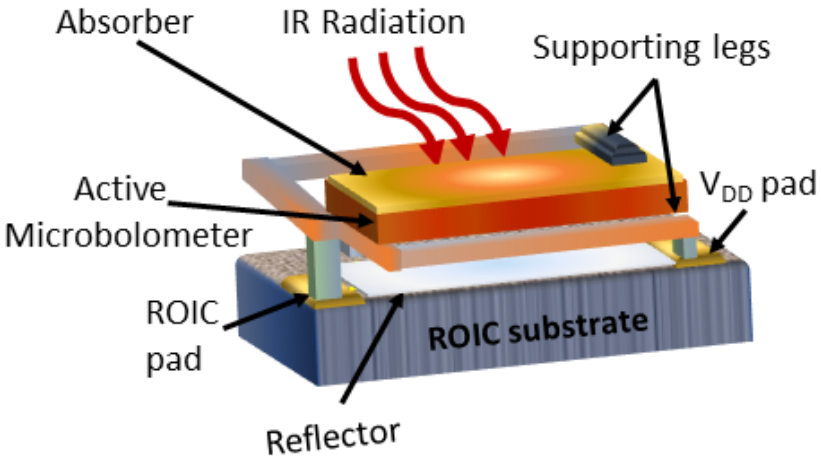


Figure 2.6: A suspended microbolometer structure over readout substrate.

radiation varies the electrical resistance of the microbolometer. For a metal detector, temperature-dependent resistance $R(T)$ can be expressed as the linear function of temperature change ΔT, given below:

$$R(T) = R_0(1 + \alpha\Delta T) \tag{2.1}$$

R_0 is detector resistance at ambient temperature T_{sub}. ΔT is the difference of microbolometer temperature (T) due to absorbed radiation and the substrate temperature (T_{sub}) as:

$$\Delta T = T - T_{sub} \tag{2.2}$$

For a semiconductor based microbolometer, $R(T)$ is modeled as a function of thermal activation energy (E_a) [16]

$$R(T) = R_0 \exp\left(\frac{E_a}{k_B T}\right) \tag{2.3}$$

where k_B is the Boltzmann's constant. Equation (2.3) shows that $R(T)$ depends exponentially on the temperature.

2.2.2 Temperature Coefficient of Resistance

The temperature coefficient of resistance TCR is defined as the percentage change in the resistance per kelvin change in the temperature. TCR is denoted by α, measured in %/K and expressed as follows:

$$\alpha = \frac{1}{R}\frac{dR}{dT} \tag{2.4}$$

2.2.3 Thermal Conductance

Thermal Conductance (G_{th}) is defined as the thermal loss through the microbolometer under various heat transfer mechanisms. There are three fundamental thermal loss mechanisms via heat transfer processes namely, convection, radiation and conduction. Since microbolometers are encapsulated in vacuum package, the major thermal loss happens via thermally conducting legs of microbolometer, whereas radiation loss also contributes to the thermal loss [17], as illustrated in

Figure 2.7. The total thermal conductance can be expressed as:

$$G_{th} = G_{leg} + G_{rad} \tag{2.5}$$

It should be pointed out that G_{leg} is typically order of magnitudes higher as compared to G_{rad} and dominates the thermal loss through the microbolometer.

2.3 Electrical-Thermal Behavior

To analyze the thermal behavior, we consider a detector representation in Figure 2.8 which consists of an absorber layer with the heat sensing material of thermal heat capacitance C_{th} coupled via a low thermal conductance path G_{th} to a substrate acting as a heat sink at absolute temperature T_{sub}. Under no incident radiation, the temperature of the detector is same as that of substrate temperature. When exposed to the IR radiation, the thermal detector converts the incident radiant flux into the thermal energy and hence the detector temperature rises. The absorption efficiency is determined by an absorption coefficient of the detector material. The conversion of the resulting temperature variation into the resistance change is determined by the TCR of the detector.

Figure 2.9 represents an equivalent circuit representation of a microbolometer. The microbolometer resistance R varies with the ΔT due to absorbed IR radiation ηP_{in} and due to the bias heating effect. As a consequence of self-heating, R decreases which causes the microbolometer temperature to rise. The higher bias current acts as a negative thermal feedback due to the negative TCR in a semiconductor-based mi-

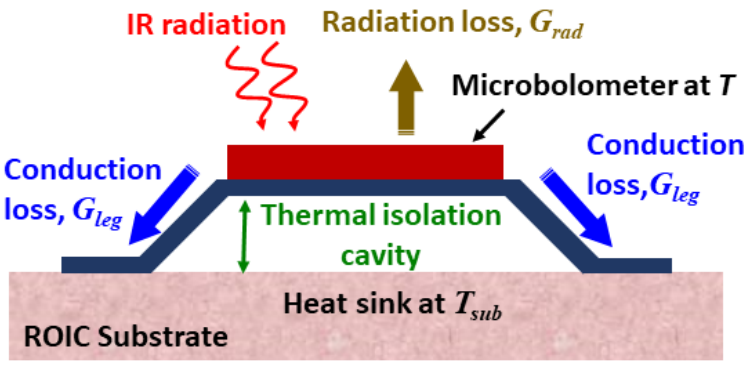


Figure 2.7: Thermal loss mechanisms in microbolometers.

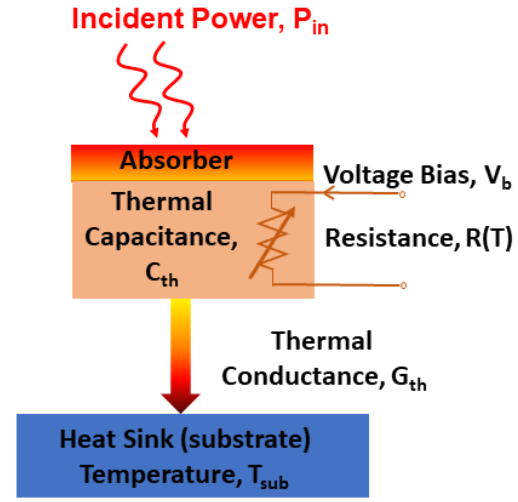


Figure 2.8: Thermal model of a microbolometer.

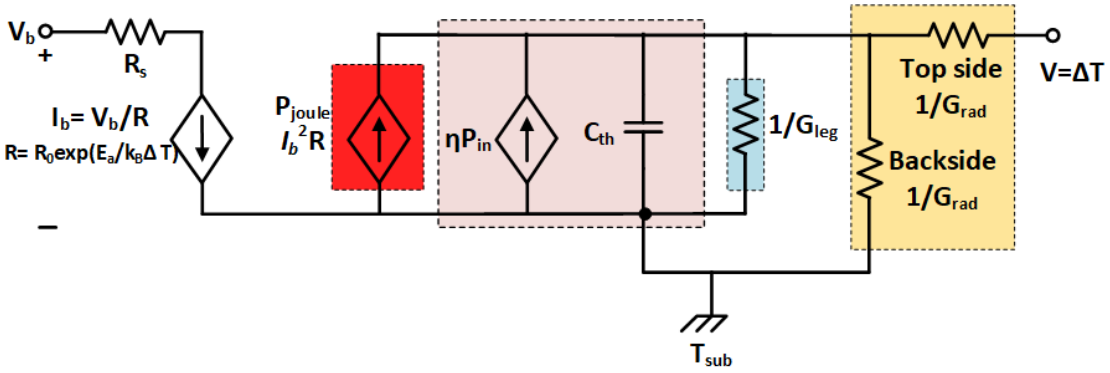


Figure 2.9: Equivalent electrical-thermal circuit model of a microbolometer ([18]).

crobolometer and deteriorates the detector operation. Nevertheless, this fact unfolds the closely inter-dependent thermal and electrical behavior of a microbolometer. The variable non-linear R of a microbolometer is represented by voltage-controlled current source (VCCS) under constant voltage bias V_b, where the current flowing through the microbolometer is proportional to V_b/R and R varies in proportion to ΔT and TCR. The series resistance R_s is included to account the contact resistance. The radiative and conductive thermal losses are included using their thermal equivalent values connected in parallel to the current source P_{in}.

2.3.1 Dynamic and Static Analysis

The heat balance equation can be used to assess the thermal behavior of a microbolometer. The equation can be expressed as.

$$C_{th}\frac{d\Delta T}{dt} + G_{th}(\Delta T) = \eta P_{in} \tag{2.6}$$

P_{in} is the incident power in W.m^{-2}, η is the absorption coefficient of detector representing the amount of power absorbed in active area ($P_{absorbed}/P_{incident}$), and T_{bolo} is the temperature of the microbolometer. The incident power is modulated such that P_{in}= $P_{in}\exp(j\omega t)$, where ω is the modulation frequency of incident IR power ($\omega = 2\pi f$) [19]. Equation (4.24) assumes no Joule bias heating, the solution of the equation is:

$$\Delta T = \frac{\eta P_{in}\exp(j\omega t)}{G_{th} + j\omega C_{th}} = \frac{\eta P_{in}}{G_{th}\sqrt{1+\omega^2\tau_{th}^2}} \tag{2.7}$$

τ_{th} is thermal time response time, expressed as

$$\tau_{th} = \frac{C_{th}}{G_{th}} \tag{2.8}$$

Equation (2.7) indicates that the temperature sensitivity (ΔT) of thermal detectors is proportional to the incident power, whereas, it varies in inverse proportion to the G_{th}. Therefore, it is desired to have ΔT as large as possible to enhance the detector response which implies that G_{th} must be very low. On the other hand, larger τ_{th} is manifested by the lower value of G_{th}, hence to reduce τ_{th} for faster response G_{th} should be larger. Both equations (2.7) and (2.8) illustrates one of the key design trade-off in terms of G_{th} for a resistive microbolometer.

Considering the simple circuit represented in Figure 2.10 with a battery of voltage V, a microbolometer of resistance R and a load resistor R_L, then the change is resistance ΔR due to ΔT can be expressed as:

$$\Delta R(T) = \alpha R_0 \Delta T = \frac{\eta\alpha f_F A_{bolo} R_0 P_{in}}{G_{th}\sqrt{1+\omega^2\tau_{th}^2}} \tag{2.9}$$

Ultimately, the change in voltage output ΔV (the signal voltage across R_L) caused by ΔT, under the bias current I_b is as follows:

$$\Delta V(T) = I_b \Delta R = \frac{\eta \alpha f_F A_{bolo} R_0 I_b P_{in}}{G_{th}\sqrt{1+\omega^2\tau_{th}^2}} \tag{2.10}$$

where, A_{bolo} is the active microbolometer area and f_F is the fill factor which defines the percentage of the actual pixel area used for the IR collection.
When taking Joule heating into account, the heat balance equation (4.24) becomes:

$$C_{th}\frac{d\Delta T}{dt} + G_{th}(\Delta T) = P_{joule} + \eta P_{in} = \frac{d(I_b^2 R)}{dT}\Delta T + \eta P_{in} \tag{2.11}$$

where the first term on the right hand side can be expressed as

$$\frac{d(I_b^2 R)}{dT}\Delta T = \frac{d}{dT}\left(\frac{V^2 R}{(R+R_L)^2}\right)\Delta T = \left(\frac{V^2(R_L - R)}{(R+R_L)^3}\right)\frac{dR}{dT}\Delta T \tag{2.12}$$

V is the supply voltage, and R_L is the load resistance in series with the microbolometer. When (2.12) substituted into (2.11), then the equation is written as follows:

$$C_{th}\frac{d\Delta T}{dt} + G_{th,e}(\Delta T) = \eta P_{in} \tag{2.13}$$

$G_{th,e}$ is referred as effective thermal conductance and is defined as [19]:

$$G_{th,e} = G_{th} - G_{th,sub}(T_{JH} - T_{sub})\alpha\left(\frac{(R_L - R}{R_L + R}\right) \tag{2.14}$$

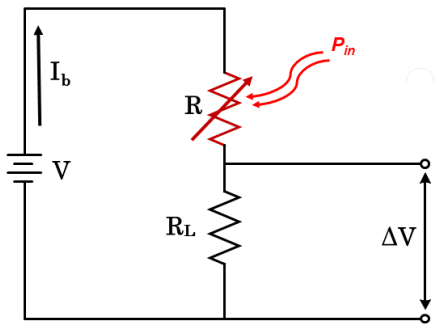


Figure 2.10: The electrical circuit representation of a microbolometer.

T_{JH} is the temperature increase in the microbolometer caused by the Joule heating. The steady-state solution of (2.13) becomes [19]:

$$\Delta T = \frac{\eta P_{in}}{G_{th,e}\sqrt{1+\omega^2\tau_{th,e}^2}} \tag{2.15}$$

where, the effective thermal time constant $\tau_{th,e}$ is

$$\tau_{th,e} = \frac{C_{th}}{G_{th,e}} \tag{2.16}$$

Similarly, (2.10) becomes

$$\Delta V(T) = \frac{\eta\alpha f_F A_{bolo} R_0 I_b P_{in}}{G_{th,e}\sqrt{1+\omega^2\tau_{th,e}^2}} \tag{2.17}$$

Equation (2.14) shows that the effective thermal conductance $G_{th,e}$ represents the difference in two terms. For the nominal device operation, $G_{th,e}$ must be positive i.e the second term must be less than the first term. If $G_{th,e}$ becomes negative (very low G_{th}), the microbolometer reaches burnout because of an exponential increase in the microbolometer temperature. As long as $G_{th,e}$ remains positive, the second term in (2.14) can be minimized by increasing the bias value (since the first term will remain same) to decrease $G_{th,e}$ which eventually enhances the voltage change as given in (2.17). On the other hand, $\tau_{th,e}$ will become large as $G_{th,e}$ decreases, which is undesirable in some applications.

For unmodulated radiation i.e ($\omega = 0$), equation (2.7) can be written as

$$\Delta T = \frac{\eta f_F A_{bolo} P_{in}}{G_{th}} \tag{2.18}$$

f_F is the fill factor, η is the absorption efficiency and A_{bolo} is the active detector area. Thereby, when the microbolometer temperature increases by amount ΔT due to IR absorption, the corresponding change in resistance $\Delta R(T)$ can be expressed in terms of TCR, as follows:

$$\Delta R(T) = \alpha R_0 \Delta T = \frac{\eta\alpha f_F A_{bolo} R_0 P_{in}}{G_{th}} \tag{2.19}$$

where α is the temperature coefficient of resistance. Finally, the change in the electrical resistance $\Delta R(T)$ caused by ΔT is measured by the voltage change (ΔV) across the detector. The voltage signal measured when biasing the microbolometer with a current I_b is

$$\Delta V(T) = \alpha R_0 I_b \Delta T = \frac{\eta \alpha f_F A_{bolo} R_0 I_b P_{in}}{G_{th}} \tag{2.20}$$

2.3.2 Responsivity

Responsivity ($\Re_v$) of a microbolometer measured in V/W, is defined as the ratio of output voltage change ΔV to the incident radiation power

$$\Re_v = \frac{\Delta V}{P_{in} A_{bolo}} = \frac{\eta \alpha f_F R_0 I_b}{G_{th}} \tag{2.21}$$

$\Re_v$ can be transformed into current responsivity ($\Re_i$) when microbolometer is operated in voltage bias mode [20] as given below:

$$\Re_i = \frac{\eta \alpha f_F V_b}{R_0 G_{th}} \tag{2.22}$$

2.4 Microbolometer Noise Sources

There are four fundamental noise sources in a microbolometer, namely, Johnson noise (thermal noise), flicker noise ($1/f$ noisse), thermal fluctuation noise, and background fluctuation noise. Readout noise will be considered in the subsequent chapters. The total root mean square (RMS) noise voltage is the sum of the RMS noise voltages of all four sources [16]. The total noise measured as power spectral density (PSD, S_v) in V^2/Hz, depends upon the noise bandwidth, given as:

$$S_v = \frac{V_n^2}{BW} \tag{2.23}$$

where V_n is the root mean-square (RMS) noise voltage and BW is the bandwidth. The noise bandwidth is the reciprocal to the integration time (τ_{int}) for the duration a bias pulse is applied.

2.4.1 Johnson or Thermal Noise

Johnson noise is caused by the random fluctuation of charge carriers in passive materials. Since resistive bolometers are passive, Johnson noise is present in this type of detector. The Johnson noise power spectral density (PSD) in any resistor with resistance R_0, at temperatıre T_0, can be expressed as [21]

$$S_J = 4k_B T_0 R_0 \tag{2.24}$$

The RMS voltage noise contribution by the Johnson noise (V_J) is expressed as

$$V_J^2 = 4k_B T_0 R_0 BW = \frac{2k_B T R_0}{\tau_{int}} \tag{2.25}$$

To reduce johnson noise, photon detector based imagers employ cooling systems to operate the detector at low temperatures. This helps significantly reduce johnson noise. Uncooled detectors, on the other hand, need to resort to low detector resistance and small reduced readout bandwidth to circumvent this noise.

2.4.2 1/f Noise

$1/f$ noise or flicker noise is dominant in the lower part of the frequency spectrum. It is referred to as $1/f$ noise since its PSD varies with $1/f$. Moreover, it also varies with the applied bias across the detector. This implies that the bias offers a degree of freedom in adjusting the $1/f$ noise. The corresponding noise power spectral density (S_f) is approximated by [22]:

$$S_f = \frac{V_b^{\beta} k_f}{f^{\gamma}} \tag{2.26}$$

f is the frequency, γ is approximately equal to 1 whereas β is close to 2, and k_f is the flicker noise constant. k_f is related to the Hooge's parameter α_H [23] and depends on the volume of the material. It is expressed as $k_f = \alpha_H / nV$, where n is the mobile charge carrier density and V is the volume of the resistor material. k_f is considered as material-related noise parameter, strongly depending upon the resistor material type, the growth and deposition techniques, structural dimensions and electrical contacts. There is no straightforward analytical expression for RMS flicker noise, but experiments has indicated that its value is approximately expressed

as [16] over the BW:

$$V_{1/f}^2 = \frac{V_b^2 k_f}{f} \tag{2.27}$$

Despite the fact $1/f$ noise dominates at lower frequencies, but at higher frequencies it falls below Johnson noise and this cross-over point is termed as the "knee frequency or the corner frequency". The knee frequency is determined by observing the overall noise, the frequency at which the Johnson noise becomes equal to $1/f$ noise in a 1-Hz interval [16]

$$4k_B T R_0 = \frac{V_b^2 k_f}{f_{knee}} \implies f_{knee} = \frac{V_b^2 k_f}{4k_B T R_0} \tag{2.28}$$

2.4.3 Temperature Fluctuation Noise

This noise is due to the random fluctuations in temperature caused by the heat transfer among various microbolometer objects by conduction and radiation. From [24], the expression for mean square temperature fluctuation noise can be written as

$$V_{TF}^2 = \frac{k_B (2\alpha R_0 I_B T)^2}{G_{th}(1+\omega^2 \tau_{th}^2)} = \frac{4k_B G_{th} T^2 \Re_v^2 BW}{\eta^2} \tag{2.29}$$

where C_{th} is thermal capacity. It can be seen from (2.29) that the only way to reduce this noise is by increasing thermal isolation of the microbolometer detector.

2.4.4 Background Fluctuation Noise

Background fluctuation noise is due to heat exchange between the detector and surrounding due to the radiative heat loss. Assuming ($\eta = \varepsilon$), background fluctuation noise can be written as:

$$V_{BF}^2 = \frac{16 k_B \sigma_B A_{bolo} T^5 \Re_v^2 BW}{\eta} \tag{2.30}$$

2.5 Imager Figures of Merit

2.5.1 Noise-Equivalent Power

For a microbolometr, the noise equivalent power (NEP) can be defined as the amount absorbed IR radiation in microbolometer that leads to an output voltage or

current equivalent to the noise power:

$$NEP = \frac{\sqrt{V_J^2 + V_{1/f}^2 + V_{TF}^2 + V_{BF}^2}}{\Re_v} \tag{2.31}$$

2.5.2 Detectivity

Detectivity can be defined as the NEP normalized to the detector area. It offers a more generalized way of classifying detectors. It can be expressed as

$$D^* = \frac{\sqrt{A_{bolo}BW}}{NEP} = \frac{\Re_v\sqrt{A_{bolo}BW}}{V_N} \tag{2.32}$$

It is worth mentioning that for the purpose of measurements, bandwidth BW of the readout must be taken into account.

2.5.3 Noise Equivalent Temperature Difference

Noise Equivalent Temperature Difference (NETD) is a measure of the smallest temperature difference the thermal detector is sensitive to. It is expressed in mK and can be calculated by estimating the spectral differential exitance (dM/dT) by unit area of a blackbody at certain temperature within the spectral band from λ_1 to λ_2. It can be expressed as [24]:

$$NETD = \frac{4F_\#^2 V_N}{\tau_0 A_{bolo}\Re_v (dM/dT)_{T,\lambda_1-\lambda_2}} = NEP\frac{4F_\#^2}{\tau_0 A_{bolo}(dM/dT)_{T,\lambda_1-\lambda_2}} \tag{2.33}$$

τ_0 is the transmittance coefficient of optics, $F_\#$ is the F-number of the optics. NETD can be written as function of D^*

$$NETD = \frac{\sqrt{BW}4F_\#^2}{D^*\tau_0\sqrt{A_{bolo}}(dM/dT)_{T,\lambda_1-\lambda_2}} \tag{2.34}$$

2.6 Design Constraints and Trades-off

2.6.1 Pixel Pitch

To ensure the necessary alignment with the SWAP trend, smaller pixel pitches are desirable. There are two main factors that drive the trend towards smaller pixel

size: (1) lower cost of lens optics and (2) high spatial resolution to enhance the capabilities of the camera. Reducing the pixel pitch decreases the lens diameter and thus cuts down the cost. Furthermore, pixel pitch plays an essential part in setting performance parameters such as noise, frame rate and power consumption. Though smaller pixels enable superior spatial resolution, they impose an upper limit on the complexity of the in-pixel readout frontend. Moreover, the charge handling capacity is compromised, resulting in the degradation of imager dynamic range. In addition, small pixel pitch makes it difficult to achieve a high fill factor. State of the art FPAs include detectors with pixel pitch of 17 µm and 15 µm.

2.6.2 Noise and Integration Time

Both $1/f$ noise and the Johnson noise components eminently contribute to the total noise of detector. As it is illustrated in (2.25), the Johnson noise depends on the integration time but $1/f$ noise is not by the integration time. Therefore, if the noise is dominated by the Johnson noise, the total noise can be reduced significantly by the larger integration time or by increasing the bias voltage. On the contrary, if $1/f$ is the dominant noise component then the larger integration time does not improve the overall noise performance. Further, it is worth pointing out that that the primary constraint on integration time comes from the frame rate specification.

2.6.3 Self-Heating

Self-heating was introduced above in the electrical-thermal model. In this subsection we delve şnto the related design constraints. The resistance of a microbolometer is measured by biasing it with a current (voltage) and measuring the voltage (current) drop over it. The applied bias causes the microbolometer temperature to rise resulting in a drop in the resistance. To achieve a sensitive imaging sensor, a low bolometer resistance is desired for a low thermal noise while a high bias voltage is desired for high responsivity. This causes high power dissipation on the detector and thus large self-heating upon bias application. The change in temperature due to self-heating also depends on the thermal capacity of the microbolometer membrane.

For small variations, this change in temperature can be approximately written as:

$$\Delta T \approx \frac{V_{bias}^2 \times T_{bias}}{R_{bol} \times C_{th}} \tag{2.35}$$

where V_{bias} is the applied bias voltage, T_{bias} is the biasing time, R_{bol} is the average bolometer resistance during biasing and C_{th} is the thermal capacity of the bolometer. A specification of handling self-heating up to 10 K is usual and ensures good performance. Assuming a reasonable bolometer TCR of $-2.6\%/K$, the resulting resistance change is then as much as $\Delta R = \Delta T \times |TCR| = 26\%$.

2.7 Readout Architectures for Resistive Microbolometer based Imagers

The readout circuits employed in resistive microbolometer based imagers perform pixel addressing, biasing and pre-amplification/signal conditioning of the detected signal before any digitization. While standard multiplexer based circuits are employed for pixel addressing, the pre-amplifier and bias circuit structure depends on the electrical properties of the detector and also on the magnitude of the signal coming in from the detector. This section discusses the various bias configurations and pre-amplifier topologies used in microbolometer imaging systems. Additionally, typical approaches to reduce self-heating induced artifacts are also reviewed. The section ends with a survey of state of the art microbolometer ROICs.

2.7.1 Biasing Schemes

Either voltage or current biasing circuitry is required for resistive type microbolometers in order to sense the change in resistance as a result of incident infrared radiation. This sub-section introduces the biasing circuits used for resistive type microbolometers.

Figure 2.11(a) and 2.11(b) show constant current and constant voltage biasing methods, respectively, to measure the resistance of microbolometers. While the latter can be implemented in CMOS with adequate performance accuracy, implementation of a low-noise current source is non-trivial. These biasing methods have some drawbacks. Firstly, the resistance measurements taken with these circuits are

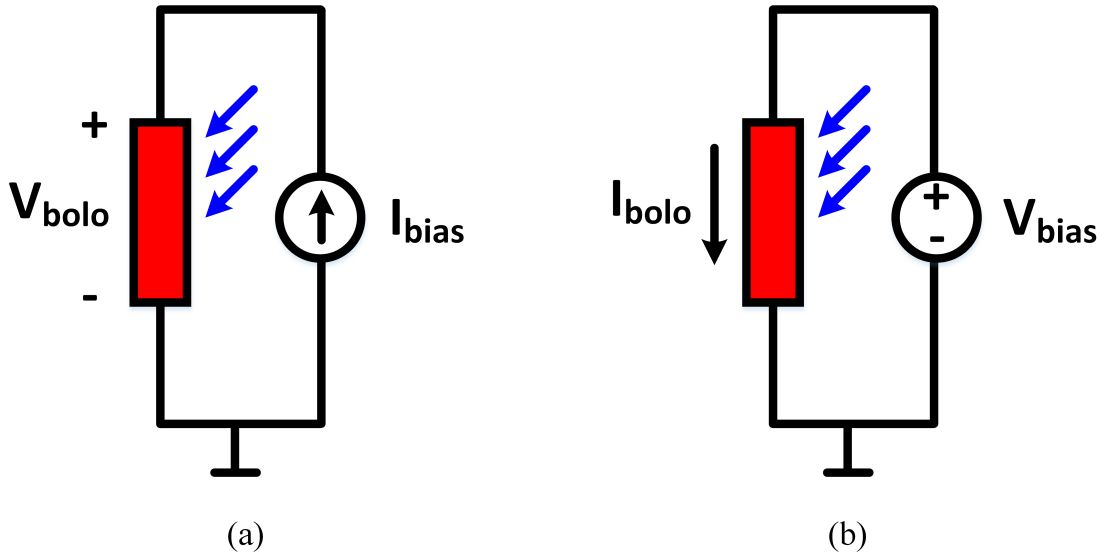


Figure 2.11: Simplified circuit of (a) microbolometer biased with a constant current and (b) with a constant voltage.

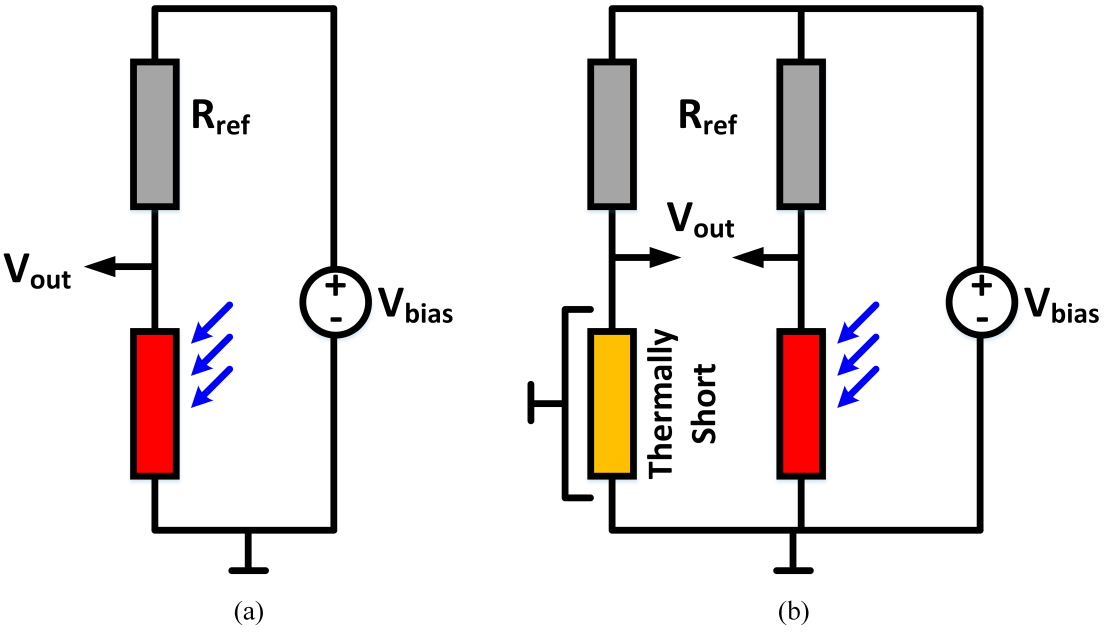


Figure 2.12: Microbolometer biasing with a (a) half bridge circuit and (b) full bridge circuit.

absolute and are sensitive to temperature and process variations. Secondly, the rise in detector temperature caused by self-heating results in excessive variation in microbolometer resistance. Usually this additional rise in temperature (resistance) is much larger than caused by incident IR illumination.

To reduce the effects of PVT variations, ratio based measurements, which can be carried out using resistive divider circuits, can be employed. Half and full bridge circuits used with resistive microbolometers are shown in Figure 2.12, where R_{ref}

are reference resistors. While the reference resistors are made insensitive to IR radiation, the thermally shorted microbolometer is essentially shorted to the substrate. Both R_{ref} and the thermally shorted microbolometer are otherwise identical to the bolometer pixel. Moreover, they are designed to have a thermal conductance much higher than that of the active microbolometer. The purpose of the thermally shorted microbolometer is to compensate for self-heating effects. A subsequent section provides further the details on self-heating compensation. Moreover, a variation of the half bridge circuit has been employed in the proposed readout as outlined in Chapter 4.

2.7.2 Pre-amplifiers

The pre-amplifiers used for resistive microbolometers usually employ a simple biasing circuit followed by an integrator. The pre-amplifier senses and amplifies the detector current or voltage with minimum noise contribution. In this sub-section, we discuss four types of pre-amplifiers typically employed in microbolometer imagers: 1) Bolometer current direct injection (BCDI) [25], 2) capacitive transimpedance amplifier (CTIA) [26, 27], 3) Wheatstone bridge differential amplifier (WBDA) [28], and 4) constant current buffered direct injection (CCBDI) [29] circuits. The first two pre-amplifiers convert the detector current to voltage through an integration process, whereas the last two convert the detector voltage to current with a low noise differential preamplifier.

(i) BCDI: Figure 2.13(a) shows the circuit of BCDI pre-amplifier. Note that this circuit is based on constant voltage biasing. R_b is the active microbolometer, whereas R_r is the reference microbolomter. R_r is thermally shorted to substrate and is, therefore, not sensitive to incident IR radiation. This arrangement helps cancel out any DC offsets and also reduces self-heating induced change in resistance. Before integration starts, rst is asserted to discharge the capacitor. Next, int is asserted and the difference current of the two microbolometers is integrated on the load capacitor. A major drawback of the BCDI amplifier is the lack of buffering at the output.

(ii) CTIA: Figure 2.13(b) shows a simplified schematic of the CTIA. As seen, constant voltage biasing is employed, and the detector current is integrated using

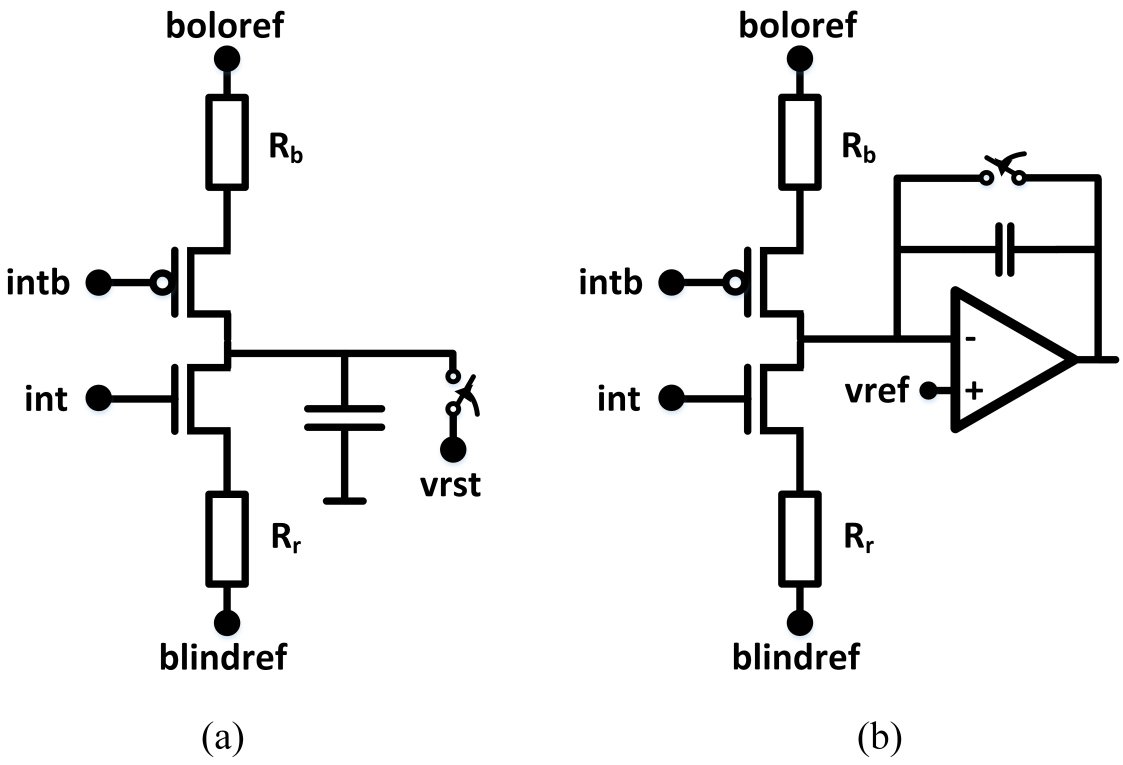


Figure 2.13: (a) BCDI pre-amplifier circuit (b) CTIA pre-amplifier circuit.

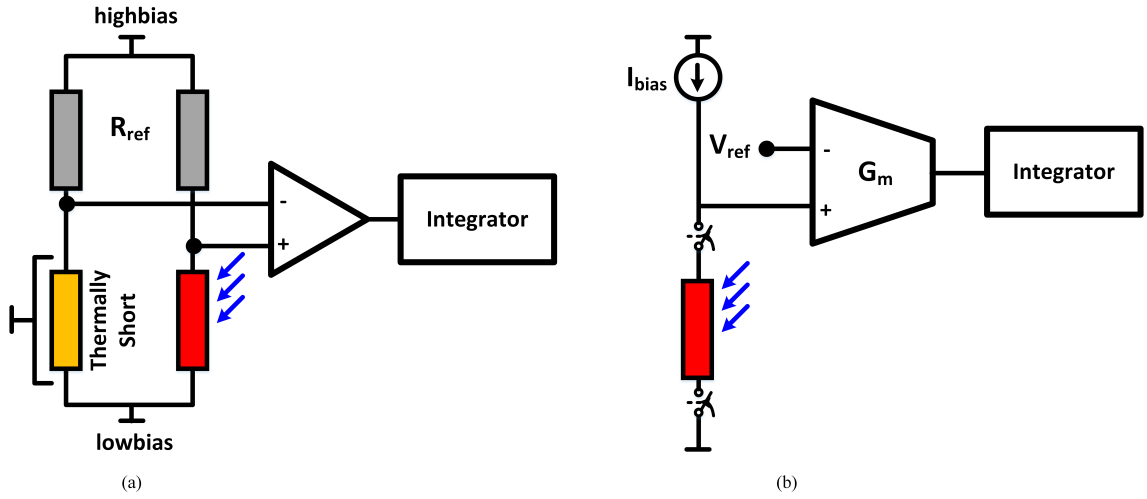


Figure 2.14: (a) WBDA pre-amplifier circuit and (b) CCBDI pre-amplifier circuit.

a switched capacitor integrator. This arrangement is similar to BCDI, however, the use of operational amplifier (opamp) based reset integrator provides adequate output buffering.

(iii) WBDA: WBDA preamplifier structure employs a wheatstone bridge type differential detector biasing circuit followed by a low noise differential preamplifier and an integrator circuit. Figure 2.14(a) shows the schematic of the WBDA

readout circuit [28]. The detector voltage is sensed by a differential amplifier. In this configuration, most of the errors coming from PVT variations and self-heating are cancelled out. Next, the output is filtered and amplified through integration. The requirement of both optically isolated and thermally shorted detectors makes this approach complex to implement and thus finds limited applications.

(iv) CCBDI: Figure 2.14(b) shows the simplified schematic of a CCBDI pre-amplifier. Unlike previously outlined approaches, CCBDI uses constant current biasing. Constant current biasing has the advantage of increased responsivity and improved linearity. Given the constant current biasing nature, it is necessary to use a transconductance amplifier to convert the detector output voltage to current prior to an integrator circuit. A major limiting factor of the CCBDI pre-amplifier is that the design of low noise and stable current sources is difficult to accomplish.

Among the approaches outlined above, the CTIA pre-amplifier is typically favored due to its simple and robust design. For this reason, it has been opted in the readout design proposed in this work. More on this is described in Chapter 4. Moreover, a detailed analysis of the signal and noise aspects of CTIA based readout front-end is provided in Chapter 3.

2.7.3 Self-Heating Compensation

Various approaches have been reported for the compensation of self-heating effects in microbolometer imagers. One method uses an external circuitry which emulates the change in the detector voltage for compensation purposes [30]. This method is simple but causes excessive noise coupling, reducing the overall performance.

A more commonly used method is based on the use of an identical reference microbolometer that undergoes a similar rise in resistance caused by self-heating and can therefore be used to cancel it out [31]. Perfect cancellation of self-heating induced temperaturre change is not possible using this method owing to imperfect detetor matching. A further cause of the ineffectiveness of this method is the fact

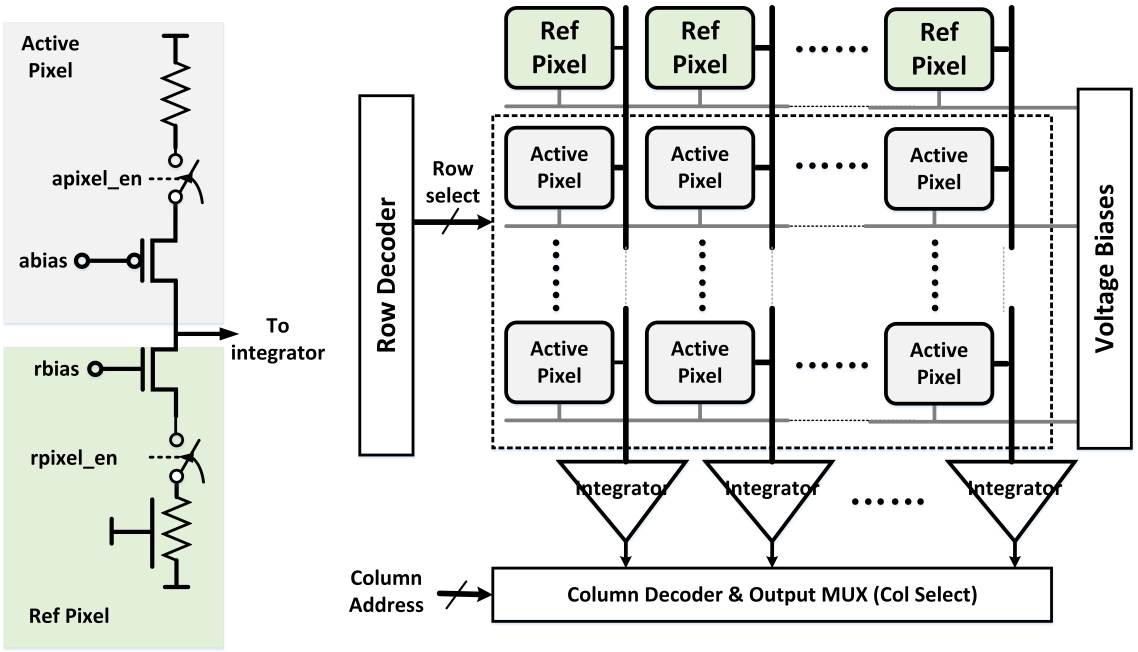


Figure 2.15: A conventional microbolometer ROIC architecture

that the reference detectors have higher thermal conductance compared to the active detectors. Reference detectors are designed this way so that they can have faster cooling cycle and can, therefore, be addressed more frequently serving a whole column turn-by-turn within a frame. This additional mismatch makes it difficult to achieve complete cancellation.

Another method corrects self-heating induced artifacs by applying an equivalent correction signal to the detector output before the signal is amplified or integrated [32].

2.7.4 State of the Art

Figure 2.15 shows an example of a conventional microbolometer ROIC architecture. Every pixel in a column shares an optically isolated reference blind bolometer (Ref Pixel) and an integrator to facilitate column parallel readout. The blind reference pixel is thermally shorted to the substrate and is, therefore, not affected by infrared radiation. The voltage bias signals required for active and reference pixel are shared in a row. Blind bolometer is used as a reference bolometer in bridge type readout pixel as shown on the left side in Figure 2.15. As pointed out previously, this kind of a detector network provides a robust means to cancel self-heating artifacts, since the two currents from the active pixel and reference pixel are subtracted. In

addition, it provides a high output resistance to the integrator circuit which helps reduce the noise through this path. When integration starts, *apixelen* and *rpixelen* signals, that control the switches of active and reference bolometers, respectively, are asserted. *apixelen* is essentially the row select signal of the corresponding row in the array. In this way, the rows are subsequently scanned using the row select signals. The frame ends when the last row is integrated and data is read out. In such an architecture, the offset caused by the integrator needs to be reduced otherwise it results in column fixed pattern noise (FPN), degrading image quality. Moreover, as mentioned before, the analog output from the pixel being commuted through column long lines also causes severe mismatch primarily due to the fact that this is a sensitive signal.

While the architecture depicted in Figure 2.15 has made to the list of workhorse approaches for microbolometer FPAs, its analog readout path demands additional noise/offset cancellation circuits that are power hungry. For instance, the column-parallel readout circuit reported in [6] employs a differential delta sampling stage that samples the incoming voltage, from the frontend amplifier, twice at two different instances and thereby cancels offset and low-frequency noise. However, it requires additional amplifier circuit and potentially large capacitors to suppress the kTC switching noise. Moreover, a variable gain amplifier (VGA) has also been included in the readout path so that the full-scale range of the signal going into the ADC (not shown) can be matched to ADC's full-scale. Given that it is a column-parallel ROIC, a separate VGA is needed for each column imposing strict requirements on power consumption and matching (among columns). Other such architectures have been reported in [5, 33–36] where different analog frontends have been proposed to reduce noise and power consumption. However, the readout signal path remains to be dominantly analog.

The circuit demonstrated in [7] is another example of a microbolometer ROIC employing an analog readout path. However, its emphasis is on a scheme to cancel offset effects by the use of a network of chip-wise and column-wise reference bolometers. It utilizes a thermally shorted microbolometers that follow the substrate temperature, an optically isolated pixel, and active microbolometers which are sensitive to IR radiation. During integration, the output currents from the thermally shorted

microbolometers are used to compensate for the substrate temperature variation, whereas the output current from optically isolated microbolometers helps suppress the effect of self-heating. A double sampling sample and hold circuit lowers the FPN resulting from offsets. At least two operational amplifiers can be seen in this circuit along with a comparator circuit. Though the ensemble of reference pixels improves the performance in terms of fixed pattern noise, the cost is a complex signal chain requiring compensation circuits. The power consumption is not reported, but it is anticipated to be dominated by the operational amplifier and comparator circuits.

The reported work in [37] aims to address the concern of self-heating in microbolometer imagers. It proposes a multiple digital correlated double sampling (MD-CDS) scheme for a better compensation of self-heating. However, it depends on a differently fabricated reference pixel. In fact, it is a set of reference pixels connected either in a series or parallel fashion. By having a series of reference pixels, the heating/cooling cycles of the active and reference pixels match, providing a better compensation. However, the change required in the process can cost in terms of fabrication time.

2.8 Chapter Summary

The chapter started with a review of the fundamentals of infrared imaging subsequently narrowing down to thermal microbolometer type imagers. Device aspects of microbolometers were then discussed followed by their dynamic/transient behavior. Following the device aspects is a discussion that highlighted the imager figures of merit and design constraints. The chapter then delves into the microbolometer readout architectures discussing the various front end detector networks, pre-amplifiers and state of the art readout designs.

3 Chapter 3

Theoretical Analysis of Conventional CTIA-based Readout

The previous chapter introduced crucial aspects of microbolometer imagers followed by a qualitative discussion of the various readout architectures found in such imagers. The superiority of CTIA-based readouts was established owing to the wide dynamic range they offer. This chapter provides a quantitative analysis of the CTIA amplifier's performance and tradeoffs. Moreover, noise performance of the entire readout chain is examined analytically. Important issues like offset and self-heating are also discussed. Generally, our approach consists of establishing an intuitive view of the presented tradeoffs using the CTIA amplifier to facilitate analysis of the proposed time mode readout presented in the subsequent chapter.

In terms of organization, the chapter begins with a detailed block and circuit level description of the CTIA-based readout chain in Section 3.1. This section also includes a closer examination of the non-idealities that influence the amplifier's achievable gain, bandwidth and dynamic range. In Section 3.2 noise contribution from both the microbolometer detector and readout circuit is derived analytically. Section 3.3 then analyze the implications of the readout architecture on detector self-heating. Following this discussion, Section 3.5 points out the limitations of the CTIA-based readout that lead to the need to re-think the readout architecture. Finally, the chapter concludes with a brief summary.

3.1 Signal Characteristics of CTIA-based Readout

A generic CTIA-based microbolometer sensor and ROIC is illustrated in Figure 3.1. The unit cell consists of a microbolometer bias circuit, a CTIA, and a CDS sample-and-hold circuit. The bias circuit consists of a thermal shorted blind microbolometer R_b, and an active bolometer R_a. R_b and R_a have identical resistance values.

A multiplexer traverses through the sampled analog outputs from the various columns. Its output is typically fed to a unit gain output buffer and then to an

ADC. The following sub-sections describe and analyze the various stages of this readout chain in detail.

3.1.1 Detector Biasing and CTIA Pre-amplifier

The bridge type voltage bias detector network depicted in Figure 3.1 is typically preferred over its current bias counterpart owing to its ability to cancel background effects. Transistors M_1 and M_2 facilitate the application of appropriate voltage bias across the active (R_a) and blind (R_a) bolometers. To accommodate this background suppression mechanism in a 2D microbolometer array, employing column-wise readout, one thermally shorted blind microbolometer R_b is typically used for each column of the array.

The CTIA amplifier, shown in Figure 3.1, is composed of a high gain opamp having an integration capacitor C_{int} and switch S_1 in the feedback network. In a typical imager, several integration capacitors might be employed to deal with different illumination conditions. The timing operation of the readout is depicted in Figure 3.2. In the beginning, the switch S_1 is turned on to reset C_{int} such that V_{ctia} sets to the reference voltage V_{ref}. Subsequently, S_1 is turned off followed by the assertion of S_2 switches. At this point, the useful current from R_a starts to integrate on C_{int} causing V_{ctia} to decrease at a rate proportional to the ratio of the incoming current I_d and C_{int}. The virtual ground at the inverting opamp input ensures that charge is accumulated on C_{int}. At the end of integration, V_{ctia} can be written as

$$V_{ctia} = V_{ref} - \Delta V_{ctia} \tag{3.1}$$

$$\Delta V_{ctia} = \frac{1}{C_{int}} \int_0^{T_{int}} I_d(t)dt \tag{3.2}$$

where T_{int} is the integration time (the time between the opening and closing of S_2). To analyze (3.2), we define the flipped gate function $\psi_{T_{int}}(t)$ as follows

$$\psi_{T_{int}}(t) = \begin{cases} 1 & -T_{int} \leq t \leq 0 \\ 0 & elsewhere \end{cases} \tag{3.3}$$

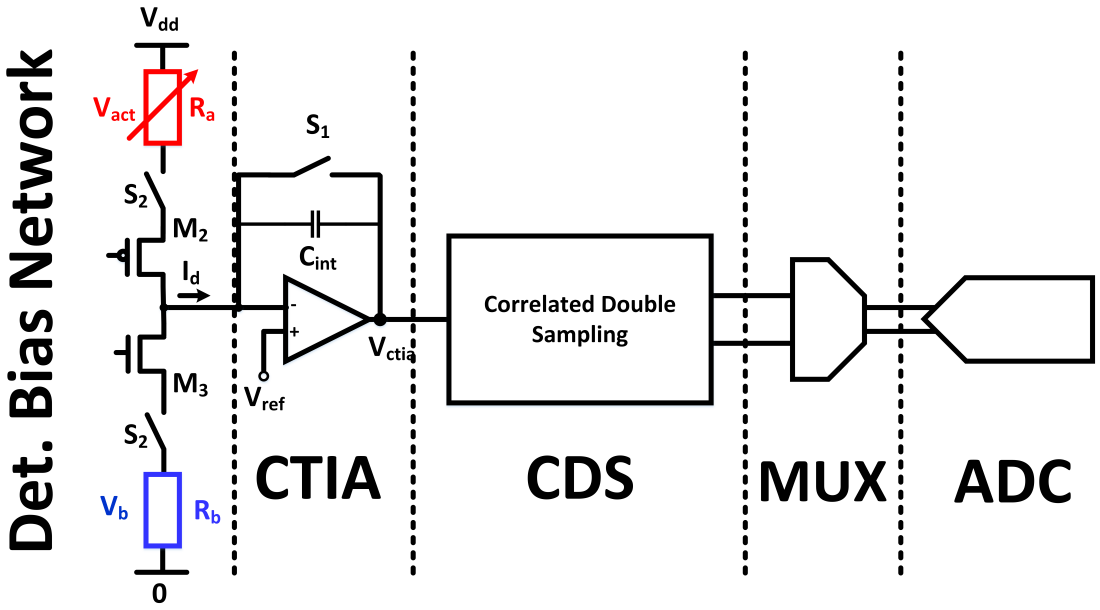


Figure 3.1: CTIA-based readout architecture

By using the gate function, (3.2) can be rewritten as

$$\Delta V_{ctia} = \frac{1}{C_{int}} \int_{-\infty}^{\infty} \psi_{T_{int}}(-t) I_d(t) dt \tag{3.4}$$

Assuming a frame time of T_{frame}, 3.4 can be modified as

$$\Delta V_{ctia}(kT_{frame}) = \frac{1}{C_{int}} \int_{-\infty}^{\infty} \psi_{T_{int}}(kT_{frame} - t) I_d(t) dt \tag{3.5}$$

where k is the frame number. The integration in (3.5) corresponds to the convolution product of the signal $I_d(t)$ and the gate function at time kT_{frame}. The ROIC takes samples periodically with the frame period T_{frame}, resulting in a discrete spectrum transfer function with the envelope $\Psi(f)$. However, it can be taken as a continuous spectrum transfer function, which is reasonable for $T_{frame} \gg T_{int}$. As a result, the transfer function in the frequency domain $\Psi(f)$ is given by

$$\Psi(f) = \frac{T_{int}}{C_{int}} \frac{sin(\pi f T_{int})}{\pi f T_{int}} \tag{3.6}$$

This transfer function is important for noise analysis and will therefore be utilized in Section 3.2.

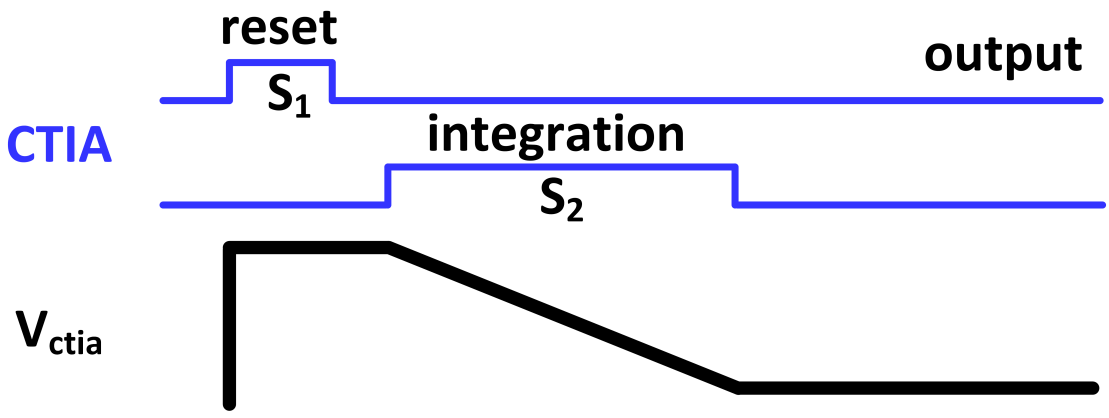


Figure 3.2: CTIA-based readout timing waveform

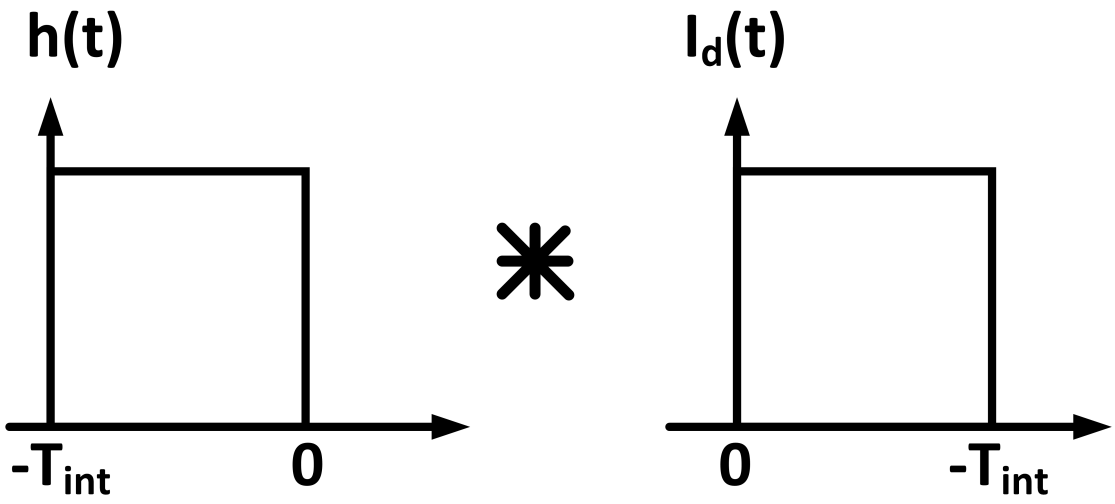


Figure 3.3: CTIA operation as convolution.

3.1.2 Correlated Double Sampling

The CDS circuit is usually employed to cancel the offset and 1/f noise of the CTIA pre-amplifier. Moreover, it also suppresses the kTC noise resulting from the reset mechanism in the CTIA. It is implemented as a switched capacitor network and operates on a double sampling principle in which the reset voltage is first sampled followed by the sampling of the desired CTIA output signal. Difference of the two samples provides a clean sample that is theoretically free of offset, 1/f noise and kTC noise.

Figure 3.4 depicts a popular switched capacitor implementation of the CDS circuit. Its timing operation is depicted in Figure 3.5. Three phases of operation can be seen, namely, reset, integration and output. The corresponding state of the CDS

circuit in each phase is shown in Figure 3.6. When the CTIA amplifier is being reset, switch S_{3a} is asserted to sample the reset voltage. If V_n encapsulates the noise and offsets, the charge across C_1 in the reset phase can be written as

$$Q_{C_1} = (V_{ref} + V_n) \times C_1 \tag{3.7}$$

This is followed by the assertion of S_{3b} to sample the signal output of the CTIA (at the end of integration). The charge sampled on C_2 during this phase can be written as

$$Q_{C_2} = (V_{ref} - \Delta V_{ctia} + V_n) \times C_2 \tag{3.8}$$

This concludes the sampling and is followed by switches S_4 being asserted. In this phase, the CDS circuit becomes a differential amplifier as shown in Figure 3.6. The negative feedback forces the inverting and non-inverting terminals to be equal (node V_x) and thus the series combination of C_1 and C_2 carries no charge. Charge conservation causes the transfer of the charge on C_1 and C_2 on to C_F, and thus the output voltage V_{cds} can be derived to be

$$V_{cds} = \frac{C}{C_F} \times (V_{ref} + V_n - (V_{ref} - \Delta V_{ctia} + V_n)) \tag{3.9}$$

$$V_{cds} = \frac{C}{C_F} \times \Delta V_{ctia} \tag{3.10}$$

where $C = C_1 = C_2$. Thus, it has been assumed that C_1 and C_2 are equal. Noise contributions, comprising offset and gain errors, reside on the lower-frequency side and their impact is therefore filtered out by the discrete high-pass signal transfer function.

To ensure that CDS own offset and flicker noise do not contribute to its output, usually an auto-zero function is embedded within the CDS amplifier. This auto-zero functionality samples CDS's own offset and low-frequency noises on CF during the reset phase and subtracts it from the output during the output phase.

3.1.3 Integration Time and Bandwidth

Integration time, which was introduced in Section 3.1.1, is usually constrained by the imaging frame rate. If T_{fr} denotes the frame time and N_{rows} denotes the

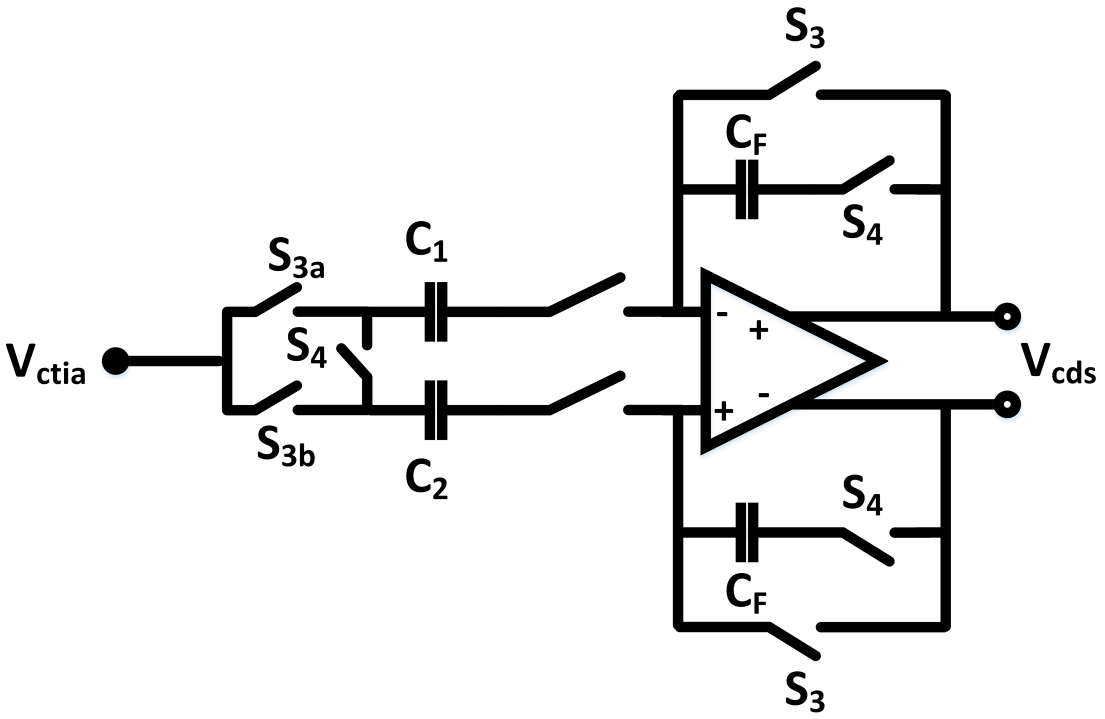


Figure 3.4: CDS Schematic

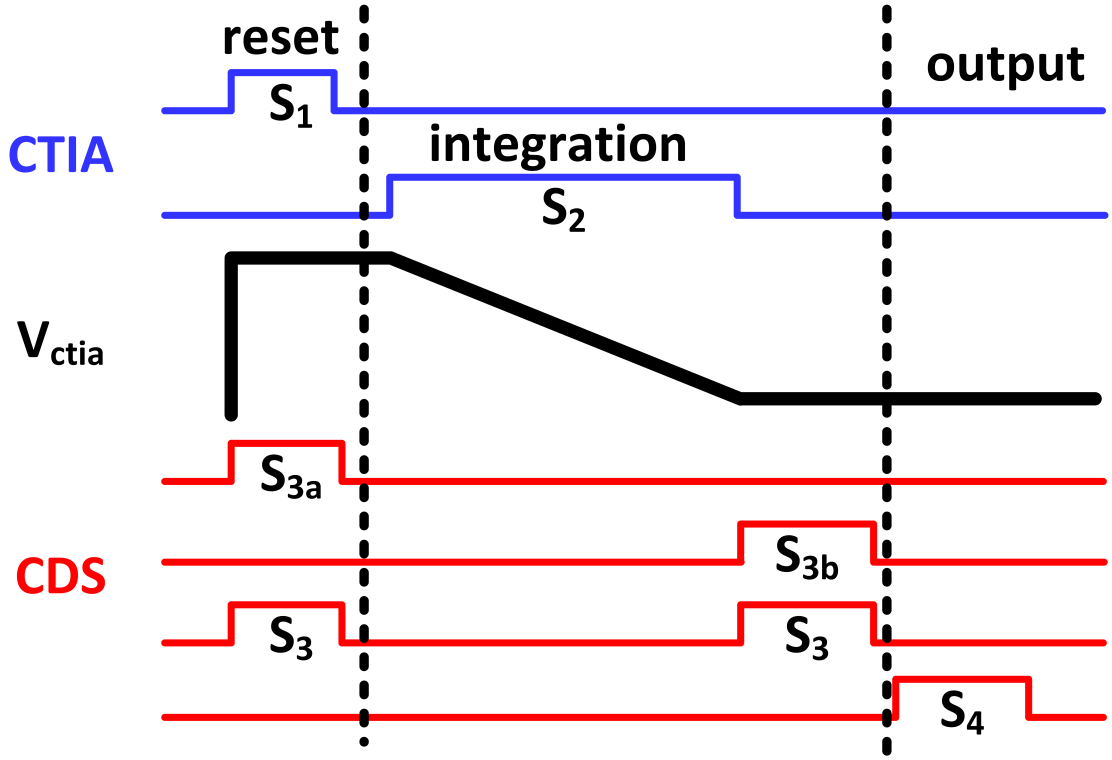


Figure 3.5: CDS Timing Waveform

number of rows in the imager, the maximum integration time can be written as

$$T_{int-max} = \frac{T_{fr}}{N_{rows}} - T_{adc} \tag{3.11}$$

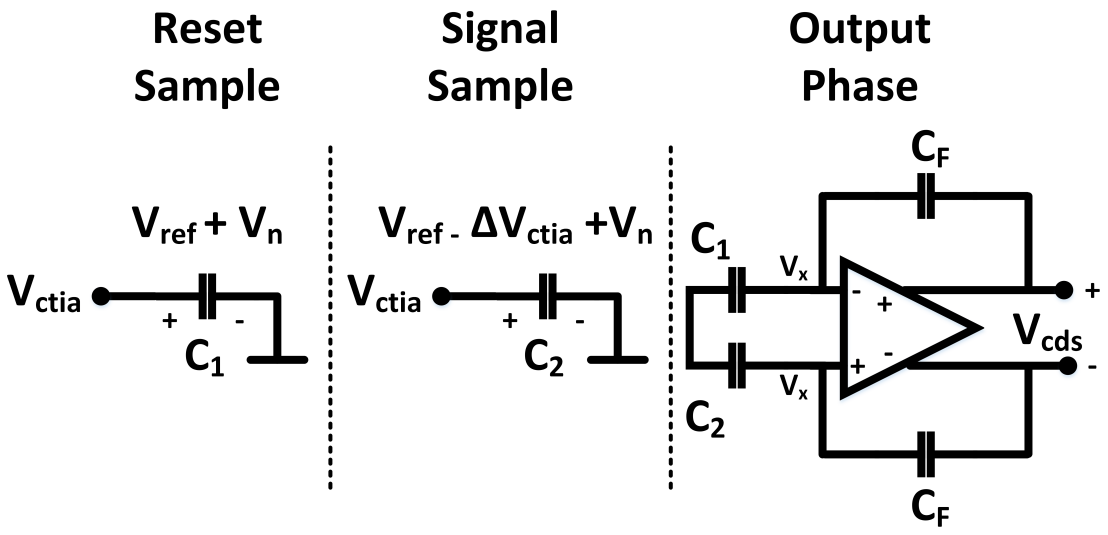


Figure 3.6: CDS Phases

where T_{adc} encapsulates the ADC sampling and conversion time. Thus for higher frame rates, the integration time can not take large values.

Furthermore, integration time has implications on the noise bandwidth of the readout. To appreciate this, we derive an expression for the noise bandwidth of the readout circuit. One way is to perform this derivation is by integrating (3.3), however, it is easier to use the Parseval's relation:

$$\begin{aligned} B &= \int_0^{+\infty} \left(\frac{sin(\pi f T_{int})}{\pi f T_{int}} \right)^2 df \\ &= \frac{1}{2} \int_0^{+\infty} |\psi_{T_{int}}|^2 df \\ &= \frac{1}{2} \int_0^{+\infty} h(t)^2 dt \\ &= \frac{1}{2} \int_0^{T_{int}} \frac{1}{T_{int}^2} dt \\ B &= \frac{1}{2T_{int}} \end{aligned} \tag{3.12}$$

We see that the noise bandwidth is inversely proportional to twice the integration time. Thus, longer integration time helps in reducing the overall noise of not just the readout but also the detector, since detector noise encounters the same noise bandwidth in the overall system.

3.1.4 Signal Readout due to Microbolometer Temperature Change

For circuit shown in Figure 3.1, the output voltage of the CTIA at the end of output phase is given by

$$V_o = V_{ref} - \left(\frac{V_{act}}{R_a} - \frac{V_b}{R_b}\right) \times \frac{T_{int}}{C_{int}} \tag{3.13}$$

where V_{act} is the active microbolometer bias voltage, V_b is the blind/reference microbolometer bias voltage, R_b is the blind microbolometer resistance, and R_a is the active microbolometer resistance. Lets $R_s = R_b = R_0$ at room temperature T_0, we can change Vsk and V_{det} to make $V_o = V_{ref}$, and that means $V_{sk} - V_{ref} = V_{ref} - V_{det} = V_{fid}$. When the microbolometer's temperature is changed due to irradiation by T, the relationship between R_b and Rs is $R_s = R_b(1 + \alpha T)$ and the change of output voltage V_o can be expressed as

$$\begin{aligned} |V_j|^2 &= \frac{V_{fid} \times T_{int}}{R_b \times C_{int}} - \frac{V_{fid} \times T_{int}}{R_b \times (1 + \alpha \Delta T_0) C_{int}} \\ &= \frac{\alpha \Delta T_0 V_{fid} T_{int}}{R_b \times (1 + \alpha \Delta T_0) C_{int}} \\ &= \frac{\alpha \Delta T_0 V_{fid} T_{int}}{R_0 C_{int}} \end{aligned} \tag{3.14}$$

3.2 Noise Analysis

There are several noise sources that affect the performance of the microbolometers imagers, most of which have been discussed by Mather in 1982 [38]. These include the Johnson noise of the microbolometer, the Johnson noise of the blind bolometer used in the detector network, and the noise of the readout electronics. A simplified schematic of microbolometer's electrical noise current integrated on the CTIA is illustrated in Figure 2, where $R_o = R_s || R_b$, I_{dn} is the noise current of the microbolometer, and V_{an} is the input-referred noise voltage of the opamp used in the CTIA.

The output of a circuit having transfer function $\psi_{T_{int}}(f)$ and input current power spectral density $S_i(f)$ is given by

$$|V_n|^2 = \int_0^{+\infty} S_i(f) |\psi_{T_{int}}(f)|^2 df. \tag{3.15}$$

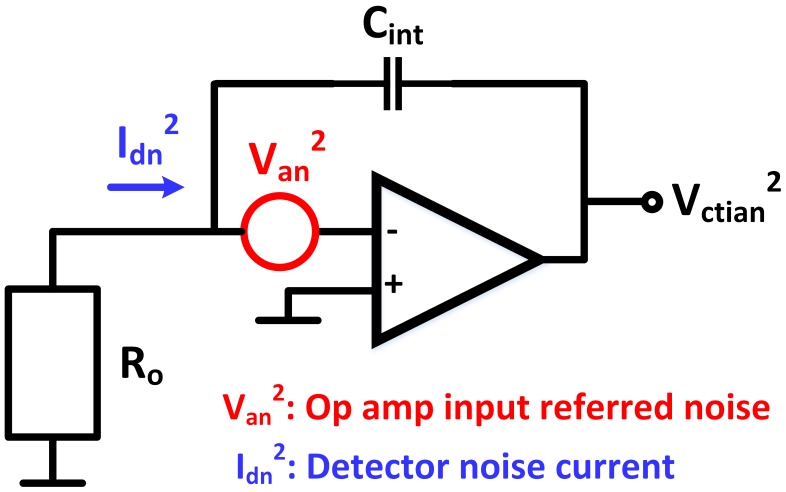


Figure 3.7: Simplified CTIA schematic with noise sources indicated.

3.2.1 Detector Noise Contribution

The Johnson noise power due to the microbolometer at the output of the CTIA is found by

$$\begin{aligned} |V_j|^2 &= \int_0^{+\infty} (\frac{V_{nR}}{R_o})^2 |\psi_{T_{int}}(f)|^2 df \\ &= \int_0^{+\infty} (\frac{4kT}{R_o}) |\psi_{T_{int}}(f)|^2 df \\ &= \frac{2kT_0T_{int}}{R_0C_{int}^2} \end{aligned} \tag{3.16}$$

By substituting the flicker noise power spectral density of the microbolometer into (3.16), the mean square output noise voltage of the CTIA is found to be

$$\begin{aligned} |V_{1/f}|^2 &= \int_{f1}^{+\infty} \frac{K_f V_{fid}}{R_o^2 f} |\psi_{T_{int}}(f)|^2 df \\ &= \frac{K_f V_{fid}^2 T_{int}^2}{R_0^2 C_{int}^2} \int_0^{+\infty} (\frac{4kT}{R_o}) |\psi_{T_{int}}(f)|^2 df \end{aligned} \tag{3.17}$$

where K_f is a constant that depends on the material used as well as on the geometry of the microbolometer, and f_1 is an arbitrary frequency chosen to avoid divergence. In this case, f_1 is determined by the on time of the system. In addition to Johnson noise and flicker noise, the other forms of noise are temperature fluctuation noise and the background noise. The mean-square fluctuations in energy of a system with

thermal capacity C and temperature T is

$$|\Delta E|^2 = kT^2C = C\Delta T_{tf}^2 \tag{3.18}$$

This random fluctuation of the energy in the bolometer will cause a fluctuation in bolometer temperature, which in turn will lead to a random fluctuation of the bolometer voltage, i.e., a temperature fluctuation noise voltage. Therefore, the temperature fluctuation is

$$\Delta T_{tf}^2 = \frac{kT^2}{C} \tag{3.19}$$

Thus, the mean square temperature fluctuation noise voltage of the microbolometer is

$$|V_{tf}|^2 = \frac{\alpha^2 V_{fid}^2 kT^2}{R_0^2 C} \int_0^{+\infty} \frac{1}{1+(2\pi f\tau)^2} |\psi_{T_{int}}|^2 df \tag{3.20}$$

As noted in the [24], if most of the heat loss from bolometer is due to radiation, the thermal conductance reduces to the radiation thermal conductivity $G_{rad} = 8A_d\sigma T^3$ (σ is the Stefan-Boltzmann constant), and the temperature fluctuation noise identifies with the background fluctuation noise V_{bf}.

The total mean square noise voltage V_{dn}^2 due to the microbolometer is can be written as

$$|V_{dn}|^2 = |V_j|^2 + |V_{1/f}|^2 + |V_{tf}|^2 + |V_{bf}|^2 \tag{3.21}$$

Since $G_{rad} \leq\leq G$, the bolometer noise due to radiation can usually be ignored in the total noise calculation.

3.2.2 CTIA Pre-amplifier Noise

The readout noise caused by the amplifier can be calculated by considering the input-referred noise of the opamp circuit. Figure 3.8 shows the schematic of a typical NOS input folded cascode opamp For such an opamp circuit, the noise power density

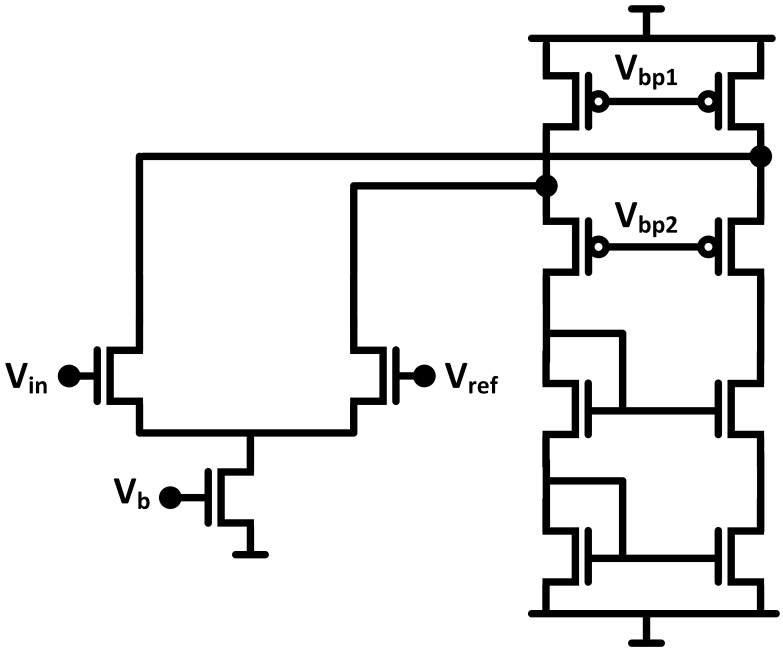


Figure 3.8: Schematic of Folded Cascode opamp employed in CTIA.

including white and 1/f noise is given by [8]

$$V_{an}^2 = 8kT\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{g_{m1}^2}\right) + \frac{2K_N}{C_{ox}(WL)_1 f} + \frac{2K_p g_{m3}^2}{C_{ox}(WL)_3 f g_{m1}^2} \tag{3.22}$$

where W is the width of the transistor, L is the length of the transistor, Cox is the capacitance per unit of the transistor, g_{m1} is the transconductance of the input transistor, g_{m3} is the transconductance of the load transistor, KN and KP are the constants that depend on the NMOS and PMOS transistors process, respectively.

The white noise power and 1/f noise power at the CTIA output caused by the amplifier can be described as

$$|V_n|^2 = \left(\frac{T_{int}}{C_{int}R_o}\right)^2 \frac{8kT}{2T_{int}}\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{g_{m1}^2}\right) \tag{3.23}$$

By taking the noise contribution caused by both the microbolometer and the amplifier into account, the total mean square noise voltage can be expressed by

$$|V_{nt}|^2 = |V_{na}|^2 + |V_{nd}|^2 \tag{3.24}$$

3.3 Implications on Self-Heating

One of the major concerns of designing a ROIC for microbolometer FPAs is the large change in temperature caused by bias heating during the application of bias on the microbolometer detector. Studies have shown that the temperature change due to bias-heating can be many times higher than the incident infrared signal. The well-known heat balance equation is expressed as

$$C_{th}\frac{\delta\Delta T}{\delta t} = \frac{\Delta T}{R_{th}} + \Delta P_{ir} + \frac{V_{bias}^2}{R_0 e^{EA/k(T_{FPA}+\Delta T)}} \tag{3.25}$$

where C_{th} is the thermal capacity, ΔT is the change in microbolometer temperature, R_{th} is the thermal resistance of the bolometer legs (in a suspended structure), P_{ir} is the incident infrared power, V_{bias} is the applied bias on the bolometer detector, R_0 is an absolute resistance technology coefficient, EA is the activation energy and T_{FPA} is the FPA substrate temperature. The third term on the right hand side represents the power dissipated in the microbolometer due to the applied bias current or voltage. Although a large bias is preferable as it would help improve the responsivity of the readout, it is quite apparent from the equation that it can cause severe bias heating due to excessive power dissipation. The result is a considerable increase in the required readout dynamic range. Thus, it is very much desirable to compensate for the effect of self-heating. Two architectures were described in the state of the art chapter that address this issue, however, at the cost of increased complexity.

3.4 Limitations of Conventional CTIA-based Readout

As seen in this chapter, conventional CTIA-based readout operates in voltage mode to amplify/condition the incoming current from the detector network. The process of digitization is typically either pixel-parallel, column-parallel or using a single chip-wide analog-to-digital converter (ADC). The pixel-parallel architecture promises superior noise performance, owing to its ability to carry out direct in-pixel analog to digital conversion. However, the area constraint limits its use to FPAs with large pixel pitches. The latter two approaches are thus preferred for small pitch

FPAs. In these approaches, pixel values (either current or voltage) are commuted through column-long lines to either column-parallel or single ADCs. Proper buffering/amplification becomes crucial resulting in additional noise. CDS is a commonly used technique in which the output of the pixel frontend is sampled twice to effectively cancel out offset and reset noise. However, the additional operational amplifier becomes a potential noise contributor and increases the overall power consumption. Furthermore, as far as PVT variations are concerned, sensitive analog blocks in the readout chain make these variations worse and impose the need to perform either background or foreground calibration. The result is an increase in area and power consumption. Thus, there is a need to develop innovative readout techniques that ensure low noise and low power.

3.5 Chapter Summary

This chapter analyzed the practical design tradeoffs of important parameters of the amplifier such as gain, linearity, common mode and supply rejection, and noise. The discussion combined the use of a hydraulic model and analytical results to offer both an intuitive and quantitative view of these tradeoffs. In particular, the discussion emphasized the importance of minimizing the signal dependence of the moscap and reducing key parasitic capacitances to achieve the highest linearity and gain while ensuring adequate common mode rejection. It was also concluded from the discussion that a thin-film SOI process with a grounded body offered the best performance combination of gain, linearity, and common mode rejection. In the next two chapters, the settling performance and implementation details of the amplifier will be discussed, demonstrating how the discussed advantages of the SOI process also help increase the amplifier's speed.

4 Chapter 4

Proposed Time Mode Readout Architecture

In this chapter, we describe how the understanding of the design tradeoffs developed in Chapter 2 and 3 led to a readout architecture suitable for low-power and low-noise operation of microbolometer imagers. In addition, we explain the concept and circuit design of the proposed architecture, supported by simulation results.

The chapter is organized as follows. We start by developing the motivation behind choosing a time-mode readout architecture in Section 4.1, followed by a summary of the specifications of the target imager in Section 4.2. Next, a discussion of the novel aspects and crucial concepts, that enable time-mode processing, is provided in Section 4.3. Subsequently, we delve into the the circuit design considerations of the various blocks of the readout in Section 4.4. Analysis of noise, self-heating and offsets are then presented in Sections 4.5-4.7, followed by the array design and chapter summary in Sections 4.8 and 4.9, respectively.

4.1 Motivation to opt for Time-Mode Processing

As established so far, the major challenge on the readout front of current microbolometer imaging systems is to reduce readout noise in a power efficient manner. The ROICs found in the literature are implemented as column-parallel arrays and can be classified into two major categories: (1) analog frame-synchronous readouts and (2) dynamic vision based readouts. The designs reported in [7, 37, 39, 40] fall within the category of analog ROICs. The ROIC in [39] uses a chain of programmable gain/chopper analog amplifiers to cancel offset and noise and, as a result, consumes large power (420 mW for a 320×240 array in a 500-nm CMOS process). A readout channel proposed in [40] and using the same technology node demonstrates 81 mK NETD but consumes 175 mW. The design in [7] employs multiple reference microbolometers to reduce substrate temperature variation and self heating but the readout channel remains analog. Finally, the most recent work in [37] uses digital CDS along with custom designed reference microbolometers to counter offset and gain errors. It reports a power consumption of 45 mW in 350-nm for an 80×60 array

with an NETD of 100 mK. Thus with a conventional analog readout architecture, large power consumption seems inevitable if noise performance is to be improved.

Dynamic vision based readouts, on the other hand, are asynchronous and offer lower power consumption since individual pixels respond to changes in illumination by generating digital events in the form of pulses. Although the on-demand nature of operation provides enhanced temporal resolution, the temperature resolution is limited as reported in [41–43]. Thus, applications of such systems are quite limited. However, introducing the concept of dynamic event generation into frame synchronous readouts provides an opportunity to get the best of both worlds.

By converting the microbolometer temperature to a time-mode signal, using digital events, it is possible to design a robust and power efficient readout channel promising improved noise performance. Time mode circuits are pre-dominantly comprised of digital circuits and can offer a robust alternative to sensitive analog chains. Moreover, the time-based outputs of such circuits lend themselves well to the digitization process using time-to-digital converters (TDCs) making them a desirable alternative. Time-mode circuits prove appealing in this scenario since they minimize the amount of analog circuitry and use noise-robust asynchronous time events as inputs and outputs. They provide a seamless interface to the growing number of time-based sensors which already output compatible timing events. Time-mode circuits have simple architecture, provide high signal-to-noise ratio, dynamic range, consume low power, and hence, prove advantageous in architecturally complex applications like imaging systems.

Accordingly, in this work a column-parallel readout architecture for frame synchronous microbolometer imagers is proposed that enables low noise operation by employing a time mode digitizer. The proposed readout circuit is based on a bridge type detector network with active and reference microbolometers and employs a capacitive transimpedance amplifier (CTIA) [11] incorporating a novel two-step integration mechanism. By using a modified reset scheme in the CTIA, a forward ramp is initiated at the input side followed by the conventional backward integrated ramp at the output. This extends the measurement interval and improves signal-to-noise ratio (SNR). A synchronous counter based TDC measures this interval providing robust digitization.

Table 1: System Specifications of the proposed ROIC

Specification	Value
Target Array Size	320×240^a
Frame Rate	30 Hz
Max Integration Time	60 μs
Min Integration Time	10 μs
Max Clock Frequency	70 MHz
Power Consumption	$<$ 60 mW
Scene Temperature	up to 150^oC
Desired Readout NETD	$<$ 10 mK
TDC Resolution	16

[a]Array size of prototype imager: 32×32

4.2 Target Imager Specifications

As pointed out above, the aim in this thesis is to develop both circuit-level and architecture-level solutions to circumvent the deficiencies of the approaches outlined in the previous chapters. Specifically, efforts are to be directed towards the design and implementation of a low-noise readout circuit for microbolometer FPAs that employs minimum number of analog blocks in the readout chain. Additionally, robust approaches that compensate for offsets and self-heating are proposed that cost very little power and area overhead.

Table I provides a list of the desired specifications for the proposed system. An array format of 320×240 is chosen considering the current trends and application requirements. However, the developed prototype has a size of 32×32. This array size is deemed to be adequate for a comprehensive demonstration of the proposed idea [44]. Being slow detectors, microbolometers are typically used in slow frame rate imagers, which is why a frame rate of 30 Hz is chosen. Given the array size and frame rate specifications, a maximum of around 100 μs of time per row is allowed. A maximum of 60 μs is chosen for integration and the rest of the margin is for digitization and readout. The proposed event based readout requires a clock to go in-pixel. To avoid large amount of buffering, a maximum of 10 MHz of clock frequency has been opted. As will be explained in the later subsections, the maximum residue time corresponds to one clock period, which amounts to be 100 ns. A power specification of less than 200 mW, scene temperature of 150C and NETD od less than 50 mK is chosen to meet current application requirements. Finally, 16 bit of digital resolution

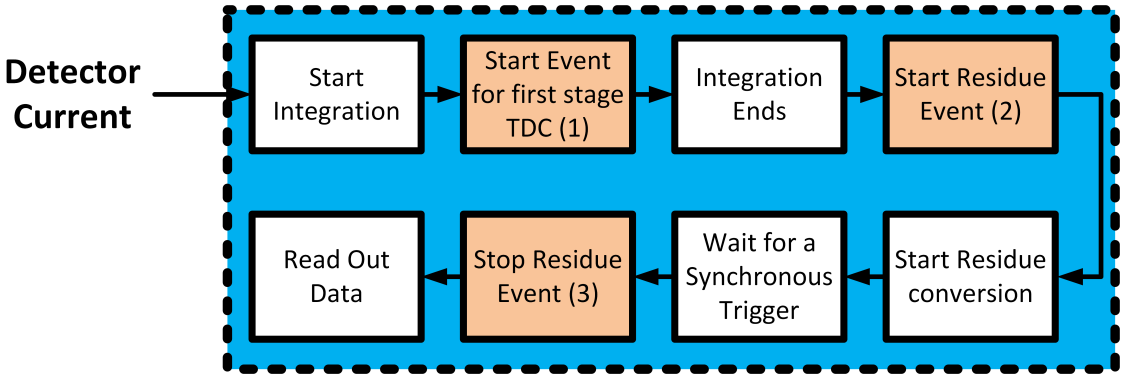


Figure 4.1: Flow chart representation of the proposed readout scheme.

is chosen as it is known to be more than sufficient for microbolometers.

4.3 Proposed Features to Enhance the Performance of Time-Mode Readout

This section introduces three main concepts either explicitly proposed in this thesis or carrying implicit significance on the proposed readout scheme:

(i) Event-Based Readout: A time-mode readout chain operating on timing events generated using comparators, latches and logic gates. The dynamic nature of the readout chain offers reduced power consumption and a robust digitization procedure.

(ii) Two-Step Integration: By using a modified reset scheme in the CTIA, a forward ramp is initiated at the input side followed by the conventional backward integrated ramp at the output. This extends the measurement interval by time amplification and improves SNR.

(iii) Dynamic Integration Time: In a time-mode readout approach, in which the integration time span is being measured, we expect radiation dependent integration time. Thus the time for which the detector is biased (or exposed to IR radiation) depends on the intensity of incident radiation. Moreover, the readout bandwidth is also radiation dependent. Consequently, a feedback mechanism is involved.

In the subsequent sub-sections, it is explained how these proposed approaches help achieve the target attributes in a low power microbolometer imager.

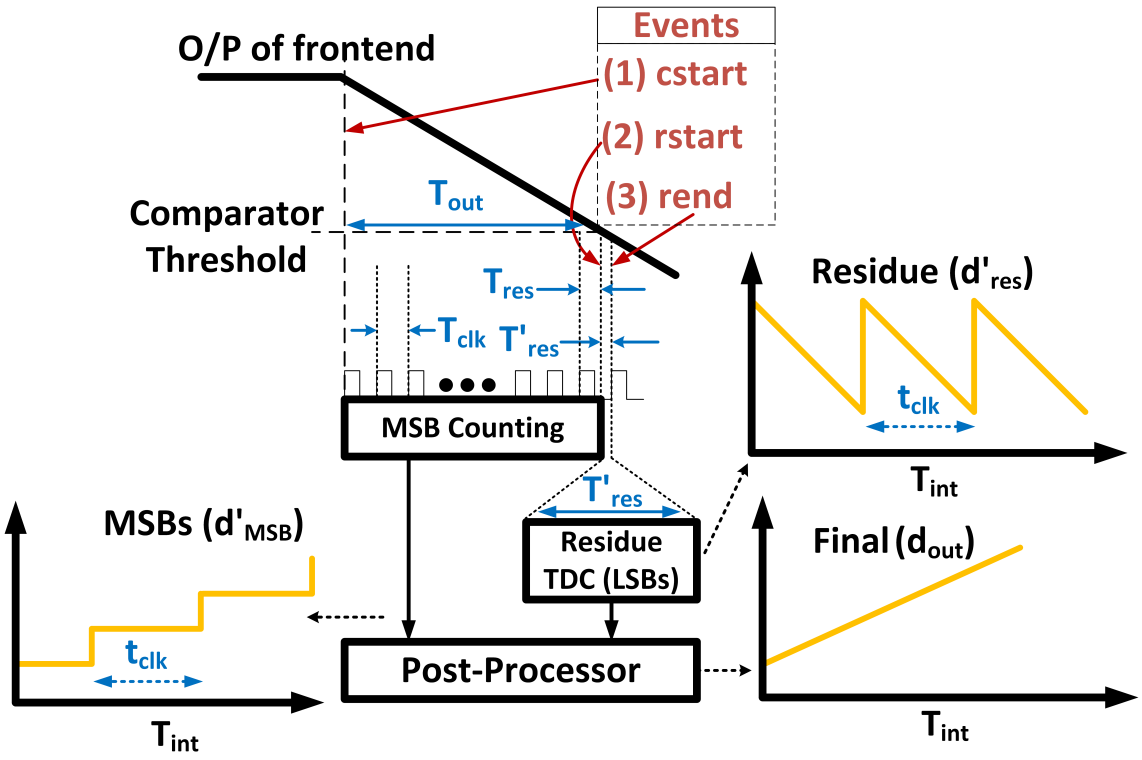


Figure 4.2: Proposed two-step TDC concept.

4.3.1 Event-Based Architecture

The proposed time-mode readout circuit generates asynchronous events and operates in tandem with a two-step TDC. Figure 4.1 shows the flowchart of readout operation. Note that this is still an integration based readout with a CTIA frontend amplifer. As the integration starts, a start event is generated through a comparator for the first stage TDC. Based on this event, the first stage TDC starts to measure and quantize the time interval. After the CTIA output reaches a fixed threshold, a start residue event is initiated. This event indicates that the first stage TDC needs to stop converting and the remaining residue time interval should be digitized. Thus, this event also serves as the start signal for the second stage TDC. Next, a stop event for the residue TDC is generated. At this point, the second stage TDC is either done converting the residue time to digital or it will take some more time and indicate to a controller circuit that the data is ready to be read out.

A detailed view of the two-step conversion concept and a block digram representation of the event-based readout are depicted in Figure 4.2 and Figure 4.3, respectively. A counter is chosen as the first stage TDC given that it will be a low

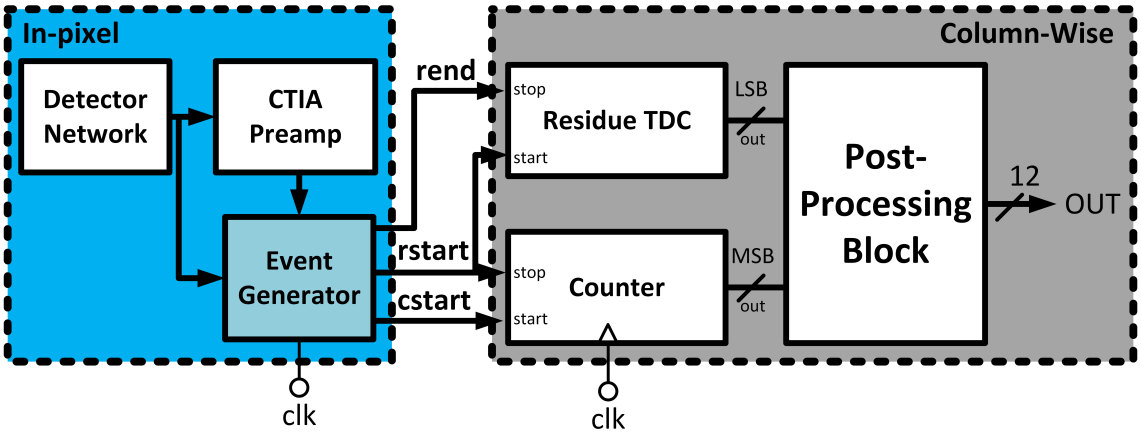


Figure 4.3: Block diagram of the proposed readout.

resolution TDC and as long as a fast clock is not required, decent performance can be obtained from the counter. The *cstart* event triggers the counter that continues counting until the threshold is reached. At this point, the *rstart* event is generated starting the residue TDC. The stop time of the residue (denoted with *rend*) is reached when the next positive edge of the clock arrives. It should be noted that this time interval T_{res} doesn't represent the actual residue. The true residue (T'_{res}) can be calculated as

$$T'_{res} = T_{clk} - T_{res} \tag{4.1}$$

The actual residue T_{res} will have to be extracted from this by the post-processing unit.

To understand conceptually how the events are generated, please refer to Figure 4.4. We see that this is a CTIA frontend with a modified reset scheme. In typical CTIA-based pixel frontends the reset switch is connected across the integration capacitor C_{int} as described in the previous chapter. As we will see in the subsequent sections, this change allows for a larger output dynamic range. When rst is asserted, the reset phase begins and the *ctiain* node discharges first to $vref$. At this point, *ctiaout* charges up to vdd followed by *ctiain* being pulled down to ground. As soon as rst is de-asserted, *ctiain* starts to charge back to $vref$. When it reaches $vref$, negative feedback becomes effective and the circuit starts to behave as an integrator causing *ctiaout* to discharge at a rate proportional to the incoming current I_{diff}. Generation of the events *cstart* and *rstart* is depicted in Figure 4.4 as well. Two possibilities for *cstart* event are shown. First, the start of the reset phase could

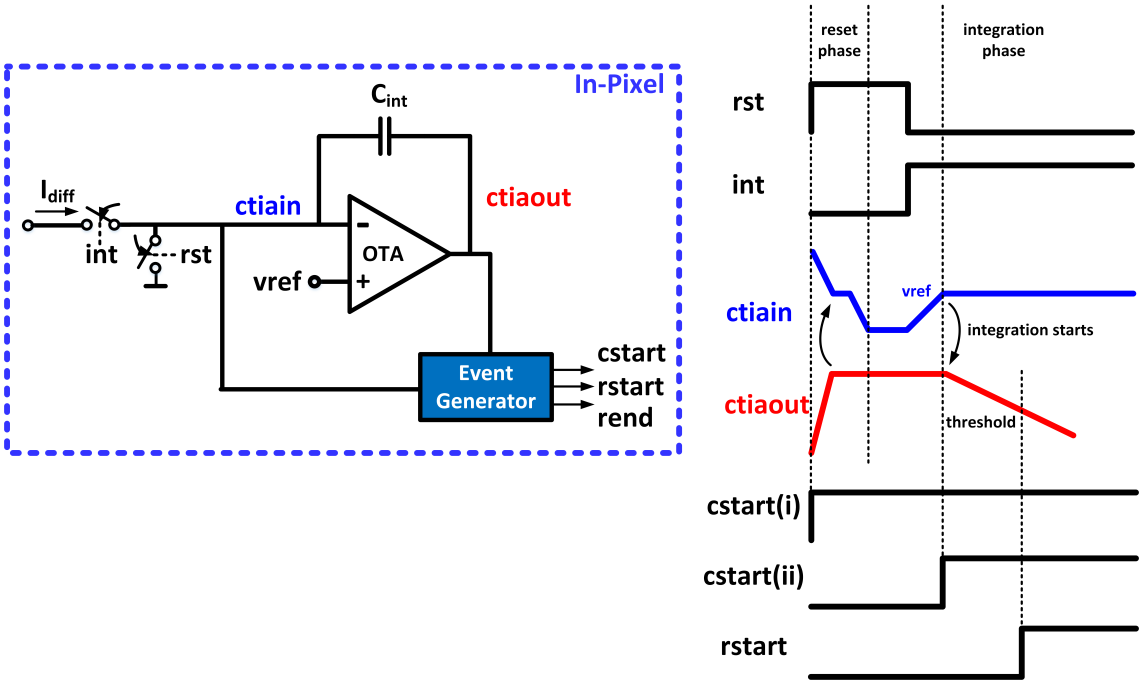


Figure 4.4: Generation of the events

mark the start of the *cstart* event. Second, the *cstart* event could be fired when integration begins on the *ctiaout* node. While the former approach is simpler and offers reduced jitter, the later method offers cancellation of offsets. This will be re-visited and explained further in a subsequent chapter.

Furthermore, we note that because of the fact that *ctiain* node is reset to ground, this node also integrates the incoming current until the voltage on this node reaches $vref$. This is followed by the integration on *ctiaout*. Thus we observe two back-to-back integration operations on the same current using only one opamp. This is not typically found in CTIA frontends and has been exploited in this work to attain time amplification and improved signal-to-noise ratio. The next subsection reflects on this further.

4.3.2 Two-step Integration

In this sub-section we look at the proposed time-mode CTIA frontend from the perspective of two-step integration based operation. Figure 4.5 depicts comparative block diagrams of conventional and time-mode CTIA frontends. Note that I_{diff} represents the difference current from the detector network.

In a conventional integration based readout, the incoming current is integrated

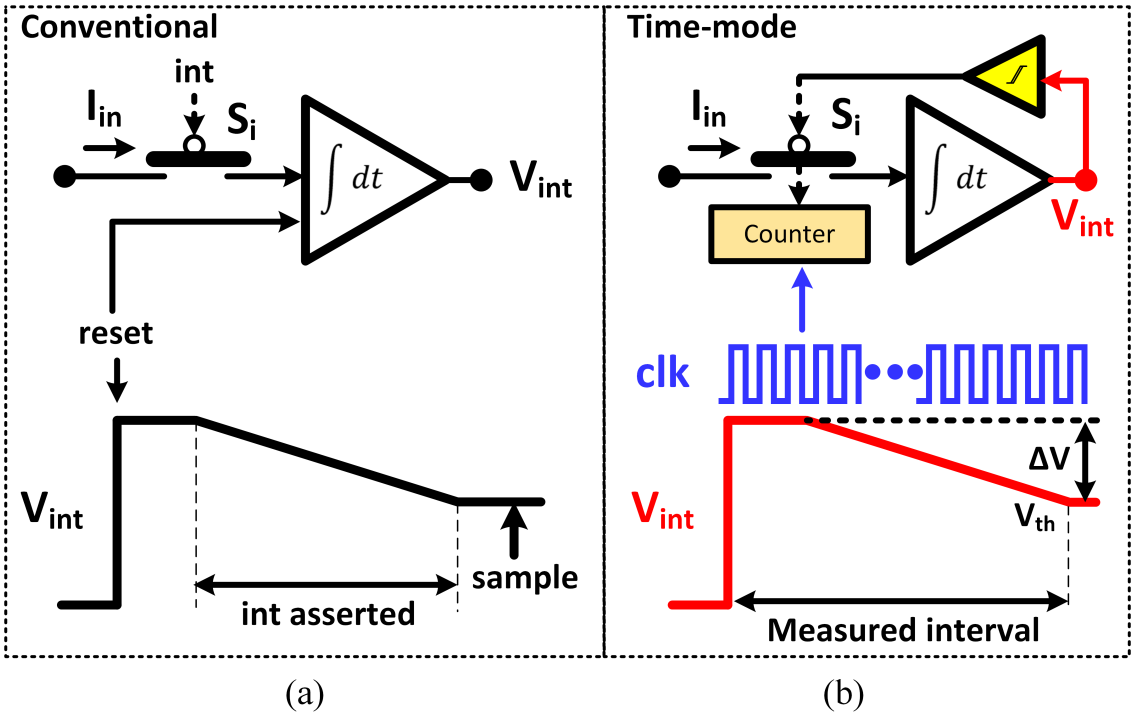


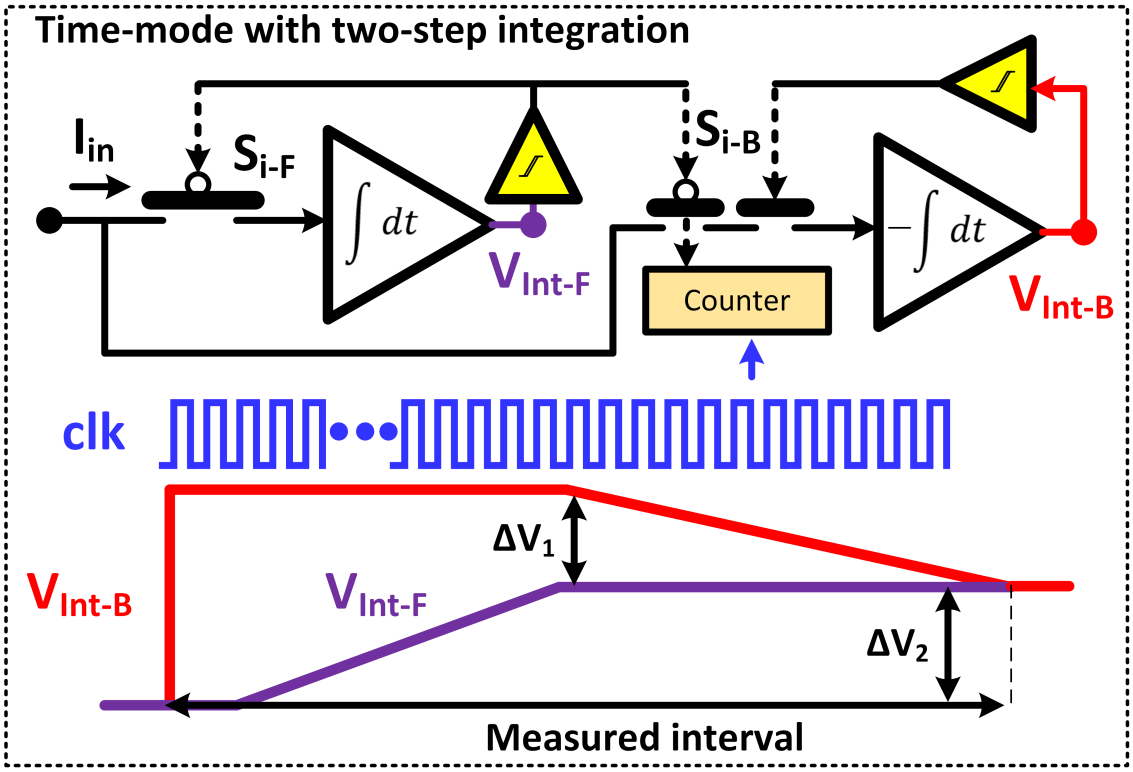
Figure 4.5: Conceptual block diagram of (a) conventional integration based readout (b) single slope time mode readout

for a pre-determined fixed period. The output voltage at the end of integration is processed/conditioned before being sampled by an ADC. This operation is represented with a switch S_i and an integrator block in Figure 4.5(a). After resetting the integrator, the *int* control input is asserted for the desired duration of integration.

As mentioned earlier, to avoid the use of power hungry signal conditioning blocks, a time mode read out approach is proposed in this work. Figure 4.5(b) shows an abstract block diagram of a single slope time mode readout. It can be seen that instead of sampling the voltage at the end of integration, I_{in} is integrated until V_{int} reaches a fixed comparator threshold V_{th}. At this point, the comparator trips and turns off the Switch S_i to stop integration. This interval is measured using a synchronous counter thereby readily digitizing the interval. The counter contents (D_{cntr}) at the end of integration represent the quantized magnitude of the incoming current I_{in} and can be expressed as

$$D_{cntr-single} = f_{clk} M \frac{\Delta V}{I_{in}} + T_{E-single} \tag{4.2}$$

where f_{clk} is the clock frequency, M is a circuit dependent scaling factor and $T_{E-single}$



(c)

Figure 4.6: Proposed two-step integration readout concept

is the quantization error.

Since digital resolution depends on f_{clk}, a higher frequency is required to ensure sufficient resolution. Thus, to relax the requirement on f_{clk} for a given input current, a two-step integration based time mode readout method is proposed as shown in Figure 4.6. Extending the concept of the single slope readout, two integrators are employed, performing forward and backward integration. After the output of forward integrator (V_{int-F}) reaches V_{th} the S_{i-F} switch is opened to stop integration and the S_{i-B} switch is closed. Similarly once V_{int} reaches V_{th}, S_{i-B} is opened as well. The entire interval spanning the two integration cycles is measured by the counter. The counter contents for this case can be expressed as

$$D_{cntr-twostep} = f_{clk} M \frac{\Delta V_1 + \Delta V_2}{I_{in}} + T_{E-twostep} \tag{4.3}$$

where $T_{E-twostep}$ denotes the quantization error in case of two-step integration. Thus, the measurement interval is doubled for a given I_{in} thereby improving SNR. Furthermore, in thesis a variation of this two step integration technique is also introduced.

Table 2: Microbolometer specifications from [45]

Specification	Symbol	Device I
Resistance	R_b	300 KΩ
Thermal Conductance	G_{th}	$2 \times 10^{-8} W/K$
Thermal Capacity	C_{th}	$0.9 \times 10^{-9} J/K$
Dimensions	A	$17\mu m \times 17\mu m$
Temperature Coefficient	α	-4%

In this technique, a fixed current is integration as the first step and then the normal integration operation on the signal current continues in the second step. This allows cancellation of offsets resulting from the CTIA and comparators.

4.3.3 Dynamic Integration Time

In typical microbolometer imagers, the incoming current is integrated for a fixed integration time. This integration time is usually adjusted (programmed) as per the scene conditions and the desired dynamic range. In this case, the detector exposure time is fixed. Moreover, the readout noise bandwidth is also fixed and well-defined. However, in a time-mode readout approach, in which the integration time span is being measured, we expect radiation dependent integration time. Thus the time for which the detector is biased (or exposed to IR radiation) depends on the intensity of incident radiation. Moreover, the readout bandwidth is also radiation dependent. We note that a feedback mechanism is involved here. In this section, we analyze the impact of this dynamic integration time on both the microbolometer's operation and on the readout front.

Variation in the microbolometer's resistance comes from two major sources: (1) the self-heating effect, and (2) the incident IR radiation. The temperature change due to self heating is usually much larger than that due to the absorbed IR power and causes severe drifts and saturation. The result is a large dynamic range requirement. Therefore, this unwanted rise in microbolometer's temperature must be suppressed or compensated. To this end, this work proposes the application of short bias pulses to reduce the effect of self-heating. This section presents simulated impact of these short bias pulses on microbolometer's temperature. For this purpose, a SiGe based microbolometers, fabricated by IHP Microelectronics [45], has been chosen as an example. Table 2 lists the relevant parameters. The presented model is applicable

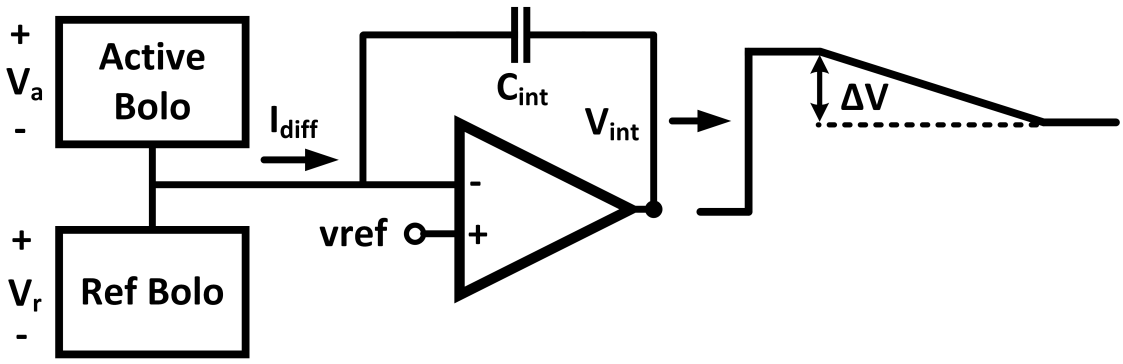


Figure 4.7: Conventional CTIA front-end with active and reference detectors.

to any resistive microbolometer device.

Typically, either voltage or current bias pulses are applied across the microbolometer detectors periodically, at the imager frame rate. At the end of each pulse, the microbolometer resistance, which is dependent on the incident IR radiation, is readout using appropriate frontend and quantification circuits. Figure 4.7 shows a conventional CTIA based voltage biased readout channel in which the difference current (I_{diff}) resulting from the temperature change of active microbolometer is integrated and read out in voltage form. Microbolometer's temperature change ($\Delta T(t)$) is usually described by the well known heat balance equation [46]

$$C_{th}\frac{d\Delta T(t)}{dt} = -\Delta T(t)G_{th} + P_r(t) + I_a^2(t)R_0(1+\alpha\Delta T(t)) \tag{4.4}$$

where C_{th} denotes thermal capacitance, R_{th} is thermal resistance, $P_r(t)$ is the incident IR power, $I_a(t)$ is the applied bias pulse, R_0 is bolometer resistance and α is temperature coefficient of resistance at FPA temperature (T_0). Note that to keep the equation linear, a current bias has been assumed. This linearity allows us to analyze ΔT by evaluating (4.4) separately for the two inputs $I_a(t)$ and $P_r(t)$. $I_a(t)$ is applied as a periodic train of current pulses and can be expressed as

$$I_a(t) = I_a \times \Pi(NT_{fr}, T_{bias}) \tag{4.5}$$

$$\Pi(t_1, t_2) = u(t-t_1) - u(t-t_1-t_2) \tag{4.6}$$

where $u(.)$ is unit step function, N is the frame number, and T_{fr} and T_{bias} are frame length and bias pulse width in seconds, respectively. Numerical simulations of (4.4)

reveal that ΔT increases linearly with time during T_{bias}, consequently, we assume a first degree polynomial based solution to determine the change in microbolometer temperature due to $I_a(t)$ (ΔT_{I_a}). It can be expressed as

$$\Delta T_{I_a} = A(t - NT_{fr}) \times \Pi(NT_{fr}, T_{bias}). \tag{4.7}$$

Substituting (4.7) in (4.4), setting $P_r(t) = 0$ and noting that $(t - N\Delta T_{fr}) << G_{th} - I_b^2 R_0 \alpha$, ΔT_{I_a} is found to be

$$\Delta T_{I_a} = \frac{I_a^2 R_0}{C_{th}}(t - N\Delta t_{fr}) \times \Pi(NT_{fr}, T_{bias}). \tag{4.8}$$

The proposed readout circuit employs voltage bias configuration, thus we modify (4.8) as

$$\Delta T_{V_a} = \frac{V_a^2}{R_0 C_{th}}(t - N\Delta t_{fr}) \times \Pi(NT_{fr}, T_{bias}). \tag{4.9}$$

In a like manner, to determine the change in temperature due to incident IR radiation $P_r(t)$, we assume a sinusoidal incident IR power with amplitude P_0 and frequency ω. The resulting change in microbolometer temperature ($\Delta T_{P_r}(t)$) is found to be

$$\Delta T_{P_r}(t) = \frac{P_0}{G_{th}(1 + \omega^2 \tau_{th}^2)}(sin(\omega t) - \tau_{th} cos(\omega t)) \tag{4.10}$$

$$\Delta T_{P_r}(t) \approx \frac{P_0}{G_{th}(1 + \omega^2 \tau_{th}^2)} sin(\omega t). \tag{4.11}$$

where $\tau_{th} = C_{th}/G_{th}$ is the thermal time constant. Hence, the total change in microbolometer temperature, including an initial transient response, can be written as

$$\begin{aligned} \Delta T(t) = e^{-t/R_{th}C_{th}} \Delta T_0 + \frac{P_0}{G_{th}(1 + \omega^2 \tau^2)} sin(\omega t) \\ + \frac{V_a^2}{R_0 C_{th}}(t - NT_{fr}) \times \Pi(NT_{fr}, T_{bias}). \end{aligned} \tag{4.12}$$

The proposed readout approach involves measurement of pixel values using time mode processing and, as a consequence, employs variable length bias pulse width. The specific pulse width depends on the intensity of the incident IR radiation (or change in microbolometer temperature) and the frontend readout topology. Fur-

thermore, since short bias times are targeted in this work, higher I_{diff} is required. With the CTIA based topology depicted in Figure 4.7, I_{diff} can be increased by applying a slightly lower bias on the reference bolometer (V_r). In this case, I_{diff} will be composed of an IR dependent component (I_{P_r}) and a residue (I_{res}). Thus, if the CTIA output (V_{int}) integrates across a voltage range of ΔV, the bias pulse duration (T_{bias}) can be expressed as

$$T'_{bias} = \frac{C_{int}\Delta V}{I_{P_r} + I_{res}} \tag{4.13}$$

$$I_{P_r} + I_{res} = \frac{V_a}{R_0(1 + \alpha\Delta T_{Pr})} - \frac{V_r}{R_0} \tag{4.14}$$

where the underlying assumption in (4.14) is that the temperature difference due to disparate biases on the active and reference microbolometers is negligible given the short bias time. Hence the corresponding change in microbolometer temperature due to bias pulse in is re-written as

$$\Delta T'_{V_a} = \frac{V_a^2}{R_0 C_{th}}(t - N\Delta t_{fr}) \times \Pi(N\Delta t_{fr}, T'_{bias}). \tag{4.15}$$

Figure 4.8 shows the effect of IR radiation on T'_{bias} for Device I. To generate this plot, a scene dynamic range of 250 K has been assumed and then ΔT_{Pr} has been determined using [24]

$$\Delta T_{Sc} = \frac{\Delta T_{Pr} G_{th}(4F^2 + 1)}{AI}. \tag{4.16}$$

To find $I_{P_r} + I_{res}$ through (4.14), we assume $V_a = 0.4V$ and $V_r = 0.394$. These values have been adjusted to attain maximum and minimum bias spans of of 8 μs and 1.5 μs, respectively. Integration in this range ensures sufficiently low power as will be reported in the subsequent sections. Then using (4.13) we determine T'_{bias}. We can see that when ΔT_{Sc} is close to 0, a large bias time is observed and vice versa. This variable bias time has two fold implications on imager performance: at large temperature changes (1) it provides superior self-heating suppression and (2) lower noise is integrated at the output. The reduction in noise is at the cost of increased power which is needed to attain adequate bandwidth in order to support the small bias time. However, the dynamic nature of the overall readout circuit helps mitigate this requirement. It should be noted that the range of bias times, for a given scene dynamic range, can be adjusted by setting the appropriate current range (through

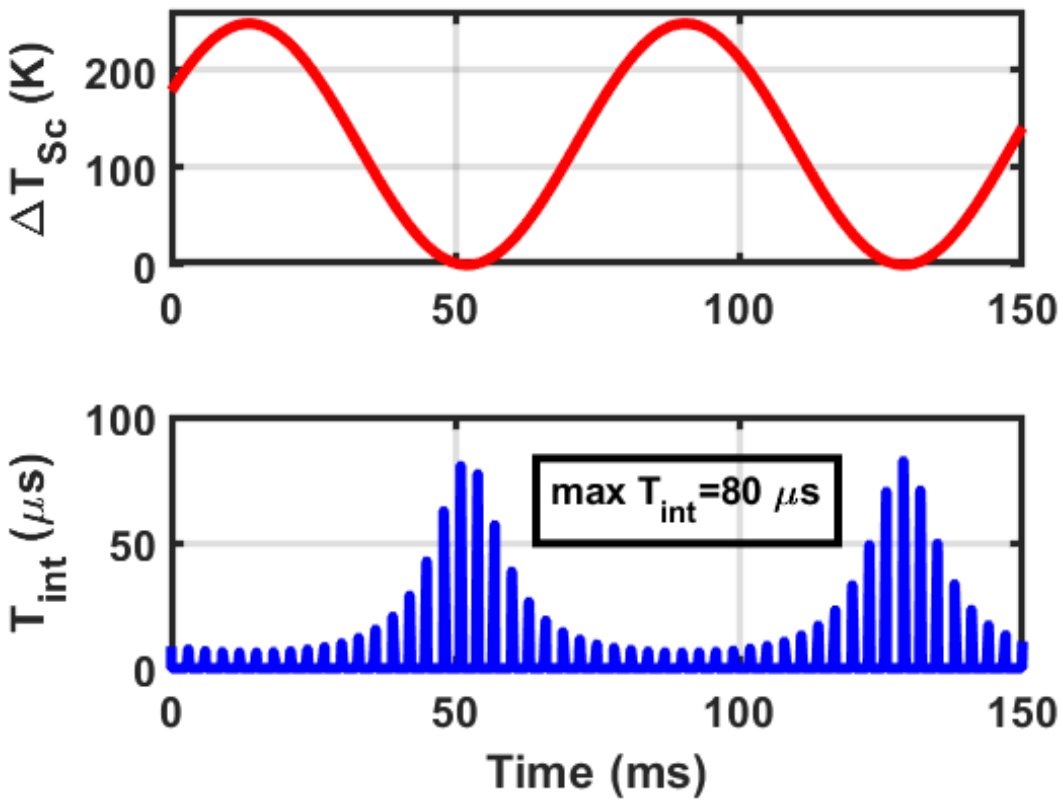


Figure 4.8: Scene dependent bias time (T'_{bias}) for Device I.

V_r).

As mentioned previously, the dynamic integration time has implications on the noise bandwidth of the readout. To appreciate this, we derive an expression for the noise bandwidth of the readout circuit. The integration operation depicted in Figure 4.7 corresponds to the convolution product of the signal $I_{diff}(t)$ and a rectangular window with length equal to T_{int}. The ROIC takes samples periodically with the frame period T_{frame}, resulting in a discrete spectrum transfer function with the envelope $H(f)$. However, it can be taken as a continuous spectrum transfer function, which is reasonable for $T_{frame} \gg T_{int}$. As a result, $H(f)$ is given by

$$H(f) = \frac{T_{int}}{C_{int}} \frac{sin(\pi f T_{int})}{\pi f T_{int}} \tag{4.17}$$

To derive the bandwidth, we use the Parseval's relation as follows:

$$\begin{aligned} B &= \frac{1}{2}\int_0^{+\infty} |H(f)|^2 df \\ &= \frac{1}{2}\int_0^{+\infty} h(t)^2 dt \\ &= \frac{1}{2}\int_0^{T_{int}} \frac{1}{T_{int}^2} dt \\ B &= \frac{1}{2T_{int}} \end{aligned} \tag{4.18}$$

We see that the noise bandwidth is inversely proportional to twice the integration time. Thus, longer integration time helps in reducing the overall noise of not just the readout but also the detector, since detector noise encounters the same noise bandwidth in the overall system. For an imager with dynamic integration time, this implies that when IR radiation is large, causing large I_{diff}, and short integration time and hence larger noise bandwidth.

4.4 Circuit Design Considerations of the Proposed Time-Mode Readout

In this section we delve into the circuit design aspects of the proposed time-mode readout circuit. We start by describing the pixel circuit for two cases:

(i) Employing two-step integration (TSI): In this case the *cstart* event is fired at the start of reset. The time amplification aspect of TSI is exploited in this pixel to enhance readout SNR.

(ii) Employing two-step integration with a fixed input current in first step (TSI-F): In this case *cstart* is fired when integration starts on *ctiaout*.

Moreover, we also discuss the circuit considerations for the TDC, that forms the column circuit of the readout This involves the counter, ring oscillator and delay line depicted in Figure 4.3.

4.4.1 TSI Pixel Circuit

Schematic of the proposed pixel readout circuit is shown in Figure 4.9. To aid in performance verification, PMOS and NMOS devices have been used to mimic

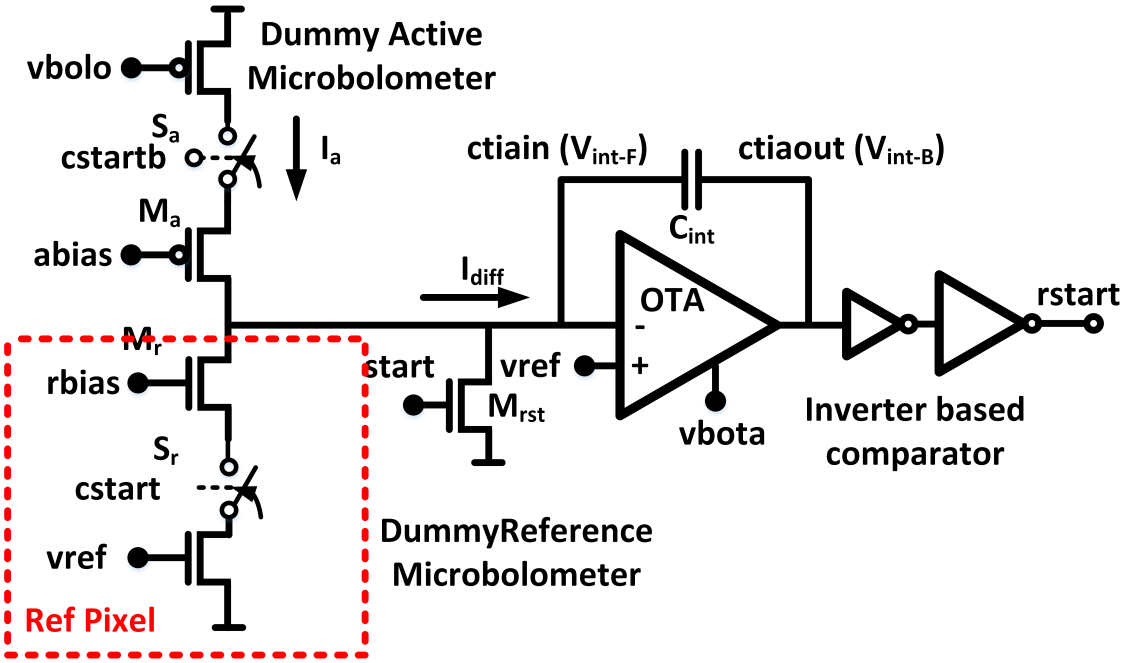


Figure 4.9: Schematic of proposed readout circuit.

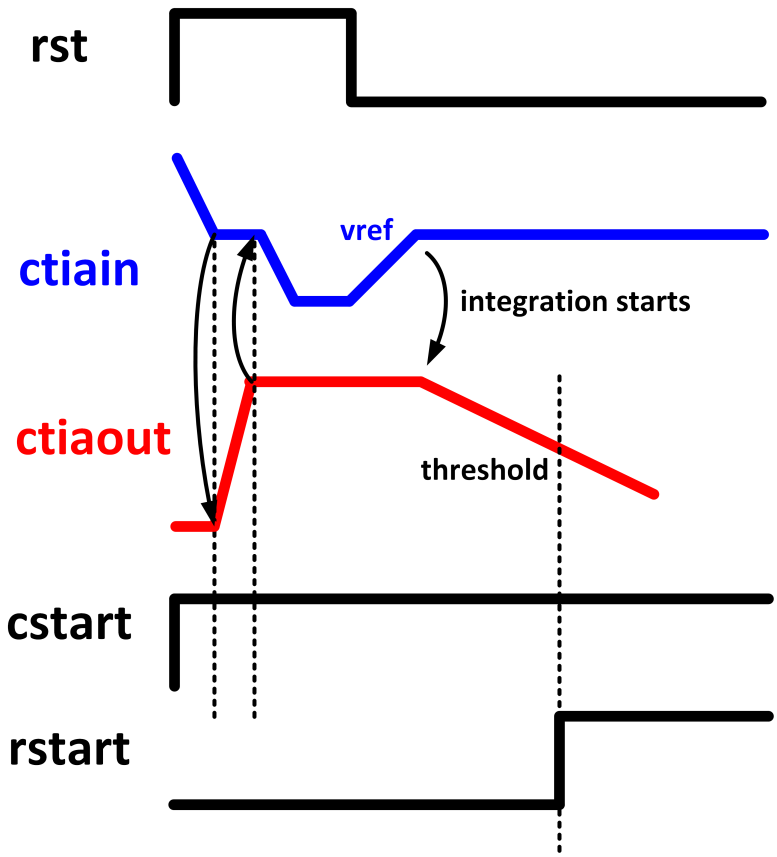


Figure 4.10: Simulated timing waveform of proposed readout circuit.

active and reference bolometers, respectively. M_a and M_r provide fixed voltage bias across the dummy detectors. As reported in [47], such an arrangement offers

accurate characterization capability if the dummy detectors are biased in the triode region. In addition to the dummy detector network, the pixel comprises a CTIA pre-amplifier and a comparator.

We note that the nodes *ctiain* and *ctiaout* correspond to V_{int-F} and V_{int-B} in Figure 4.6, respectively. In a typical CTIA topology, a reset switch, in parallel with the feedback integration capacitor (C_{int}), discharges the capacitor before the start of integration [40]. This resets the CTIA output (*ctiaout*) to the reference voltage ($vref$) connected to the positive terminal of operational transconductance amplifier (OTA). While such a configuration provides the desired functionality in voltage mode operation, the limited integration span would restrict the dynamic range in case of time mode processing. Moreover, it is important to extend this measurement interval without reducing the input current to keep an adequate SNR. Thus, in this work a modified reset scheme is presented in which the reset transistor M_{rst} is connected to the *ctiain* node as shown in Figure 4.9. Resetting through M_{rst} pulls *ctiaout* to *vdd* which forces the *ctiain* node to integrate, followed by a second integration on *ctiaout*. The measured time span (T_{meas}) can be expressed as

$$T_{meas} = f_{clk} C_{int} \frac{vref + vdd - V_{th}}{I_{in}} + T_{E-twostep} \tag{4.19}$$

This way of processing in the time mode provides a two-fold benefit: (1) firstly, *ctiaout* resets to *vdd* expanding the voltage dynamic range of the CTIA and (2) given the time-mode nature of the proposed technique, back-to-back integrations enhance the measurable time span for a given input current, thereby, improving the readout SNR.

To understand the operation of the modified CTIA, we look at Figure 4.10. When rst is asserted, *ctiain* is pulled to $vref$ resulting in the negative feedback getting activated causing *ctiaout* to charge up to *vdd*. This is essentially followed by the *ctiain* node being finally pulled down to *gnd*. Once rst is de-asserted, *ctiain* integrates up to $vref$. At this point, the negative feedback becomes active again and keeps *ctiain* at $vref$ causing *ctiaout* to integrate down until it reaches the comparator threshold (V_{th}). Note that although for conceptual illustration, Figure 4.6 depicts two integrators, we see that two-step integration can be implemented using a single CTIA by a simple modification of the reset mechanism. Moreover,

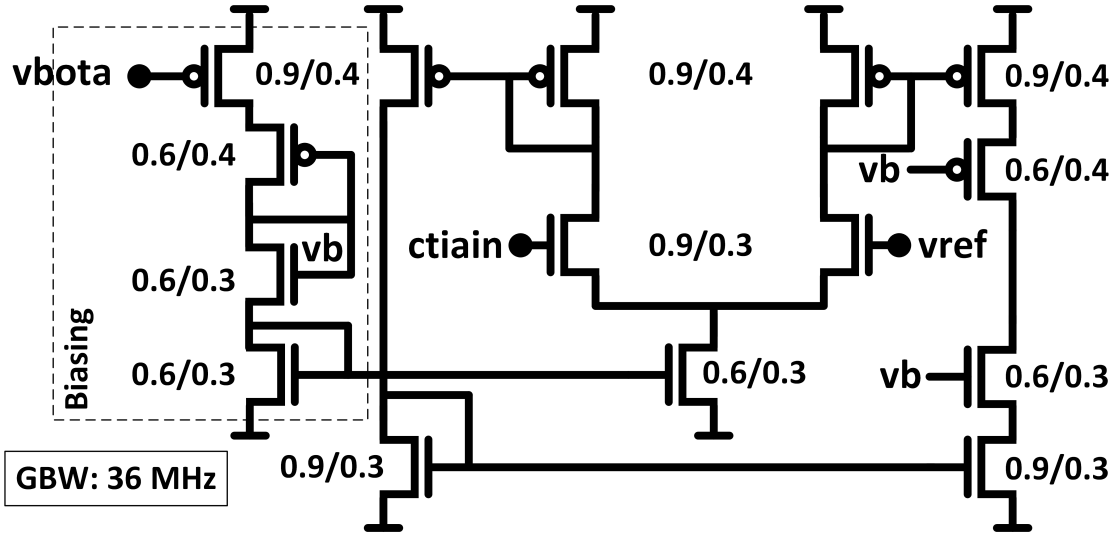


Figure 4.11: Schematic of the OTA (Dimensions W/L in μm).

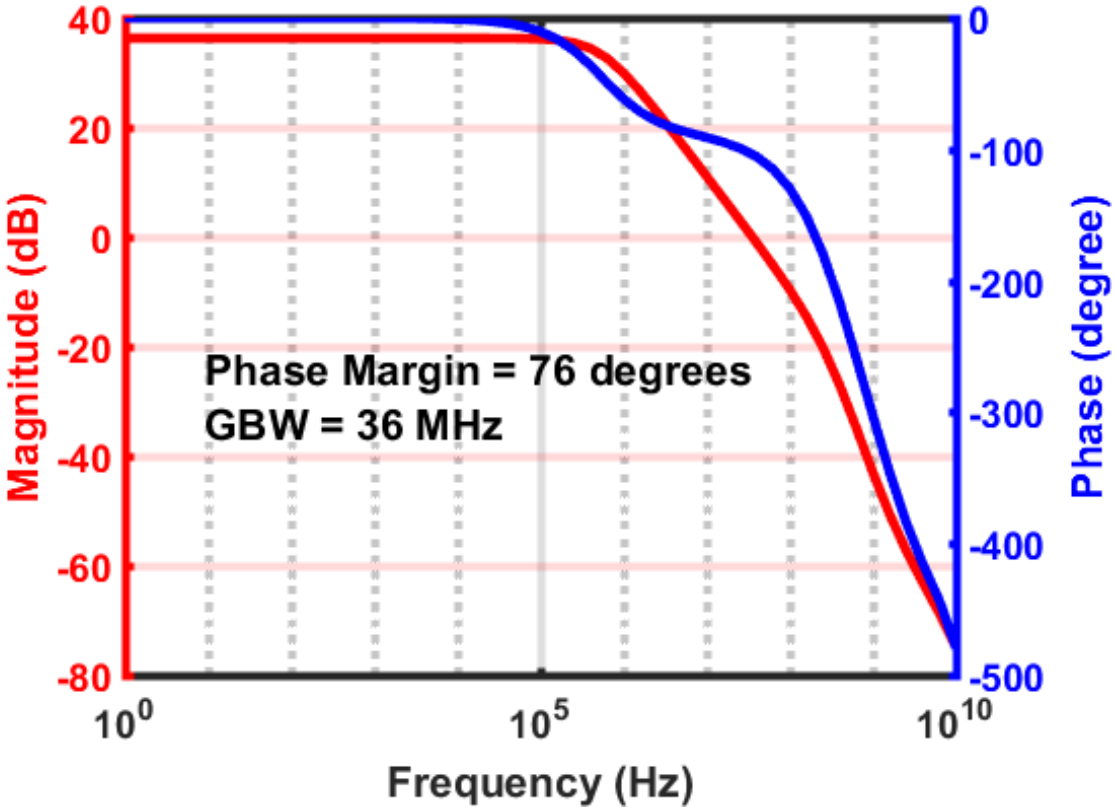


Figure 4.12: Frequency Response of the OTA employed in CTIA amplifier.

we see that while switches S_a and S_r correspond to S_{i-B} of Figure 4.6, S_{i-B} is not explicitly needed since the negative feedback implicitly stops the integration on *ctiain* and initiates discharge of C_{int} by forcing backward integration on *ctiaout*.

Given that the integration time can be small, crucial bandwidth requirement is imposed on the OTA. A gain-bandwidth (GBW) product much higher than

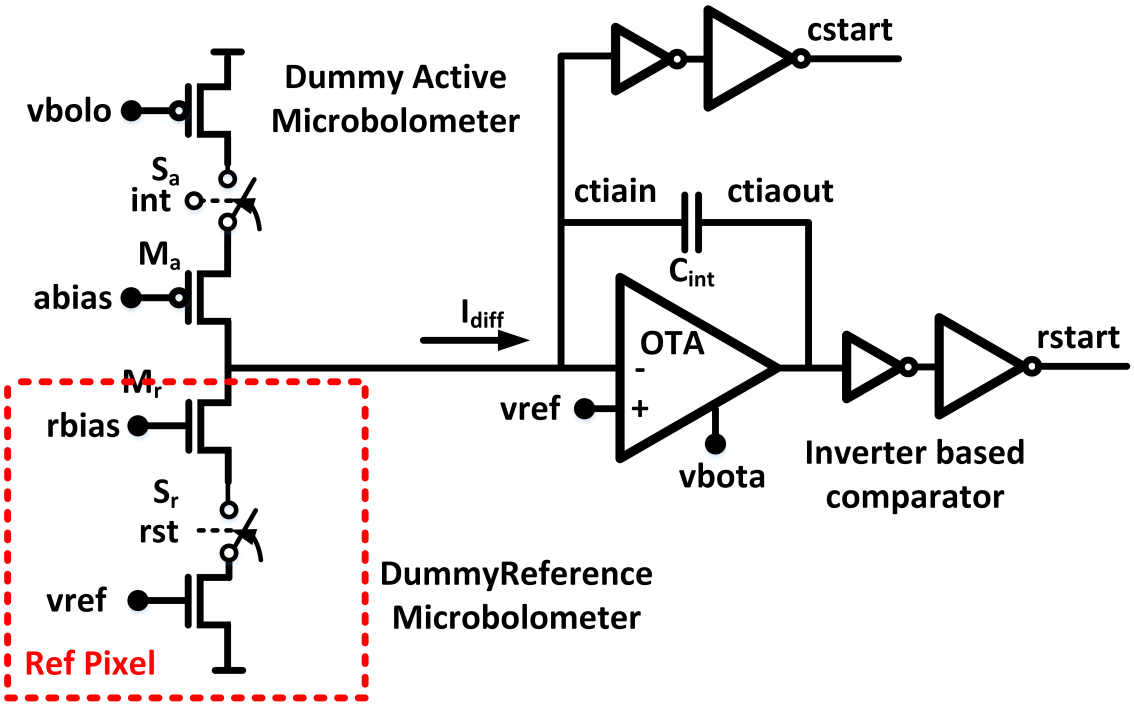


Figure 4.13: Circuit schematic of the proposed TSI-F pixel.

$1/(2T_{bias})$ is needed for accurate and linear translation from current to time. To ensure sufficient accuracy, the OTA has been designed for a 36 MHz GBW. A 3-current mirror based topology for the OTA achieved the desired GBW with a compact area and static power consumption of of 5 μW. Figure 4.11 depicts the schematic of OTA and 4.12 shows the corresponding frequency response. The cascoded output stage helps provide adequate gain. Moreover, the biasing network allows single input biasing which is desirable in an array implementation. The transistors have been sized large for matching concerns.

4.4.2 TSI-F Pixel Circuit

The schematic of the pixel employing two-step integration with fixed current in the first step is shown in Figure 4.13. We note that this pixel has two main differences when compared with the pixel depicted in Figure 4.9. First, there is an additional comparator based on a set of inverters, that generates the *cstart* event. The input to this comparator is the *ctiain* node. Generating *cstart* this way provides an opportunity to exploit the integration of reset current occurring during the reset phase. This can be seen in Figure 4.14 where the time interval spanning from the rising edge of *rstart* to the falling edge of *cstart*, during the reset phase, can also be

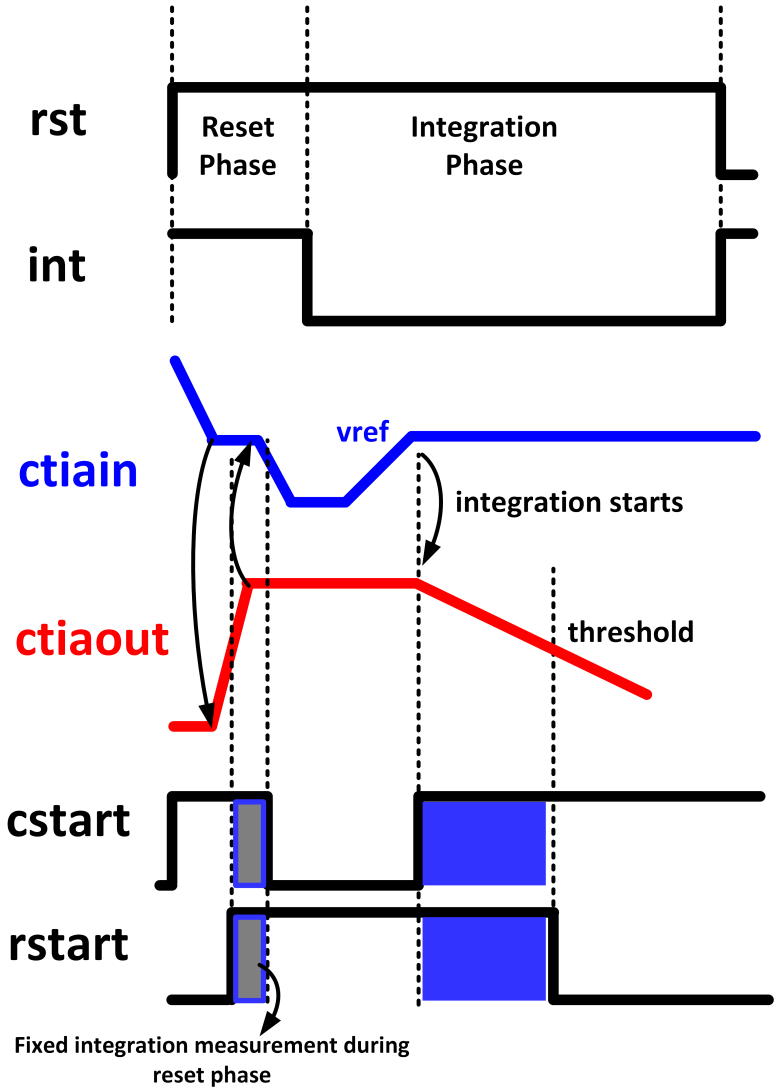


Figure 4.14: Timing waveform of the TSI-F pixel.

measured in addition to the interval representing the main integration ramp. And since the reset current is fixed and independent of the incident IR radiation, there is a potential to use this time interval to extract gain and offset errors stemming from the CTIA and reference bolometer.

The second difference is that there is no separate reset switch. The S_r switch, which is used to apply bias on the reference bolometer, serves as the reset switch as well. Thus the reset current essentially flows through the reference bolometer. Resetting this way provides a two-fold benefit: (1) it eliminates the need to use an additional transistor for resetting and (2) it offers a way to reduce self-heating artifacts. The latter will be elaborated further in Section 4.6.

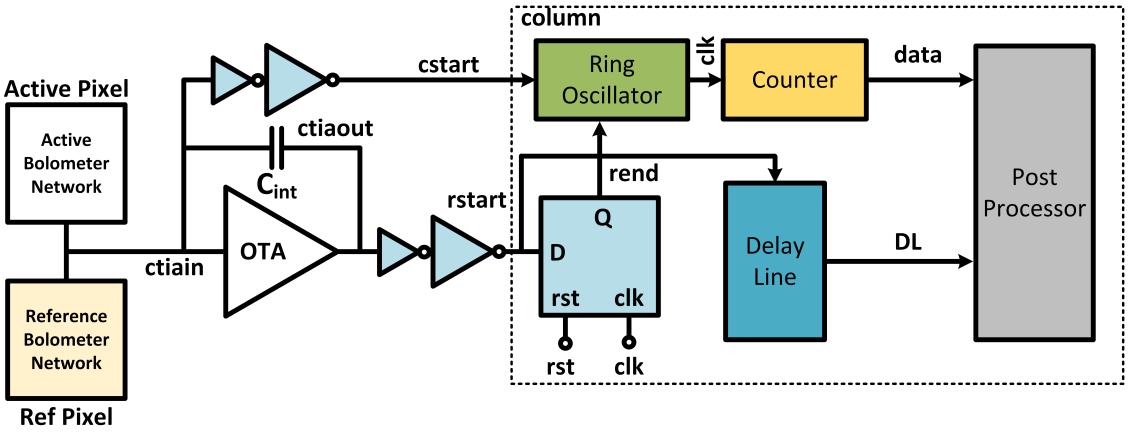


Figure 4.15: Block diagram depicting the Two-step TDC.

4.4.3 Time-to-Digital Conversion

A block diagram of the readout chain including the pixel and column circuits is shown in Figure 4.15. The counter forms the first stage TDC, whereas the delay line is the second stage TDC. Note that in this block diagram a TSI-F pixel is shown, however, the TDC is equally applicable to the TSI pixel. As pointed out previously, the events *cstart* and *rstart* are generated in-pixel. To generate the *rend* event, we see that a flip-flop has been employed. When *rstart* asserts, *rend* is fired at the next positive edge of *clk*. At this point, the delay line output, which is essentially a thermometer representation of the 4-bit residue, is sampled by the post processor. This timing operation is shown in Figure 4.16.

The detailed circuit schematic of the TDC is depicted in Figure 4.17. We see that both the ring oscillator and delay line are based on current starved inverter based stages. These inverters are required to be sized large enough to reduce non-uniformity concerns. Given that the TDC resides within a $17\mu m$ column, proper sizing and placement is done to ensure satisfactory performance. Enabling/disabling of the counter is accomplished by starting/stopping the ring oscillator. The NAND gate provides a convenient control to enable the ring oscillator when *cstart* is asserted. This ensures reduced power consumption since the clock is not running at idle times. Moreover, coupling noise effects are also minimized.

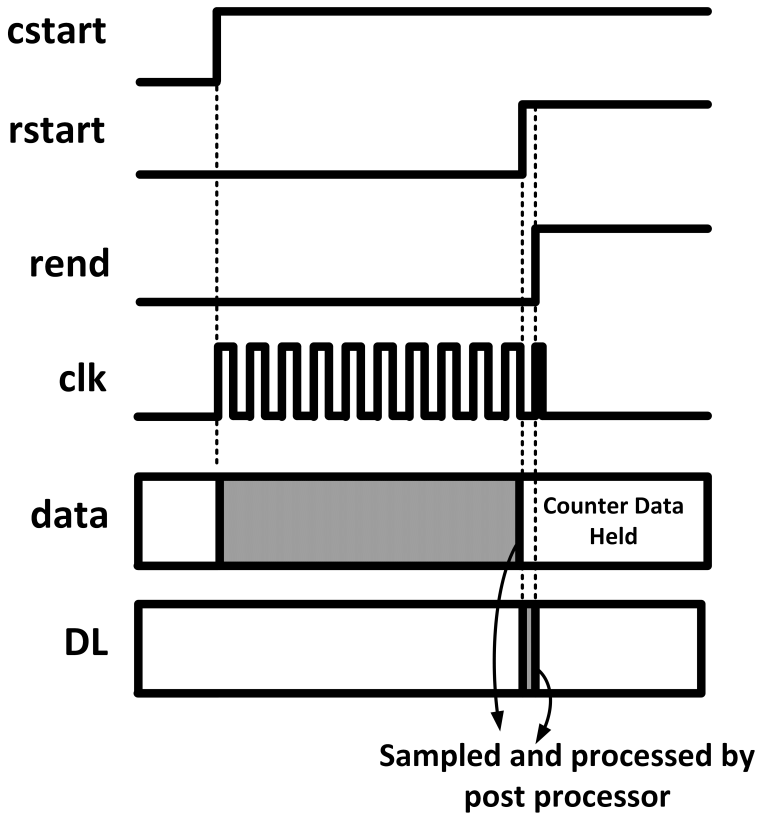


Figure 4.16: TDC Timing waveform.

4.4.4 Ring Oscillator Clock Period Variations

Since digitization accuracy of the measured time interval depends heavily on the clock generated by the ring oscillator, we have performed Monte Carlo simulations at various process corners to observe the distribution of the clock period. As shown in Figure 4.18, 4.19 and 4.20, the worst-case standard deviation comes out to be 8 ns when the fast-fast process corner is set.

4.5 Front-End Jitter Noise Analysis

Time mode nature of the proposed frontend circuit calls for the evaluation of jitter noise in the timing events. To analyze noise , we chose the TSI-F pixel architecture since it has a more involved timing operation as compared to the TSI architecture. In the TSI-F architecture, the start and stop events of the interval to be measured are defined by the positive edges of *cstart* and *rstart* signals, respectively (Figure 4.16).

To this end, we identify five major noise sources as shown in Figure 4.21. I_{dn}^2

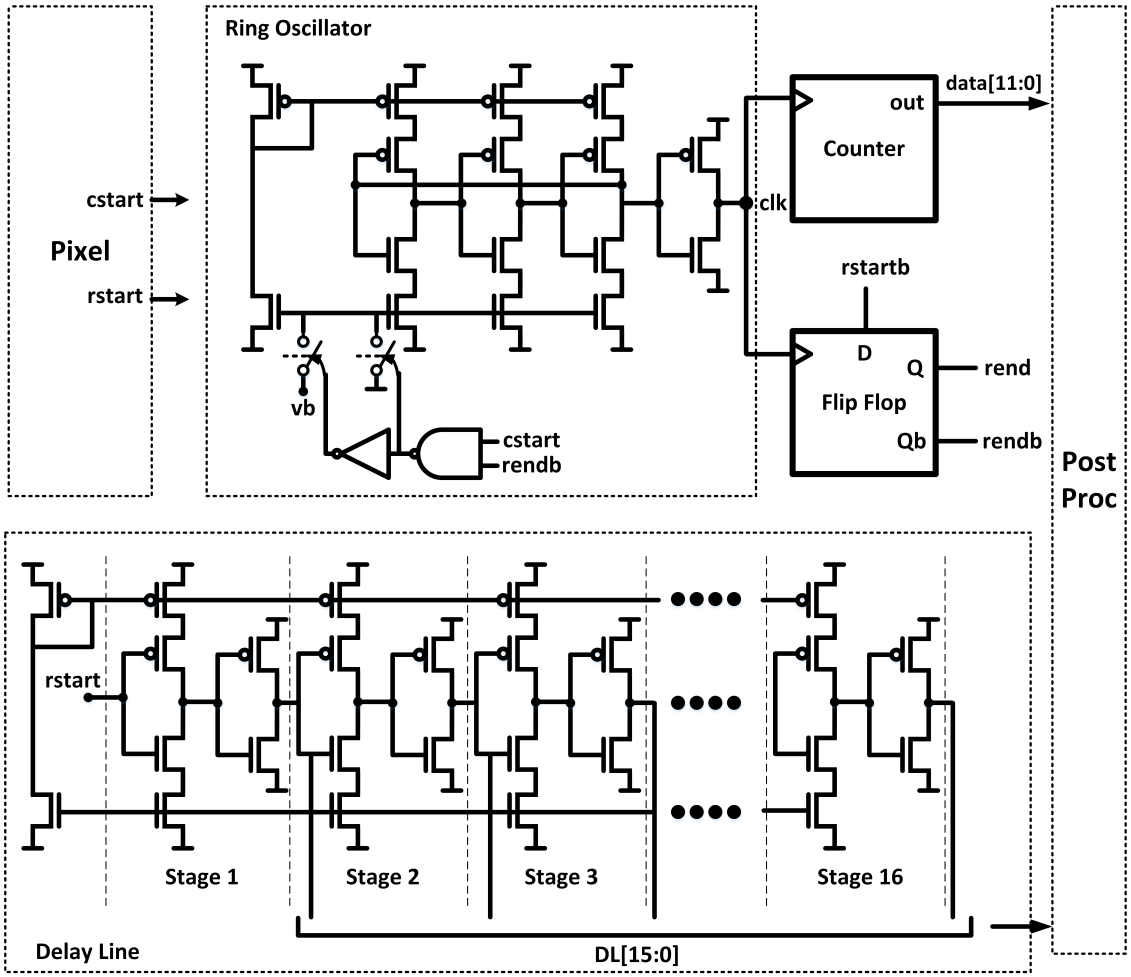


Figure 4.17: Detailed schematic of the proposed two-step TDC.

denotes the current noise of the detector side and V_{an}^2 is the input referred noise of the OTA. I_{cp1}^2 and I_{cn1}^2 represent the noise currents of the PMOS and NMOS devices of the first and second inverters of the *cstart* comparator, respectively, whereas I_{cp2}^2 and I_{cn2}^2 represent the noise currents of the PMOS and NMOS devices of the first and second inverters of the *rstart* comparator, respectively. These specific noise contributions from the comparator are considered dominant since the crucial transition at the input of the *cstart* comparator is low-to-high and that at the input of the *rstart* comparator is high-to-low.

To obtain the jitter noise in the *trig* signal, we follow the methodology reported in [48]. According to this methodology, the measured time interval is assumed to be a random variable with a mean and variance. If the input signal current is known, the Wiener–Khinchine theorem [49] can be used to find the jitter noise variance by applying a windowed convolution on the input current. The length of this window

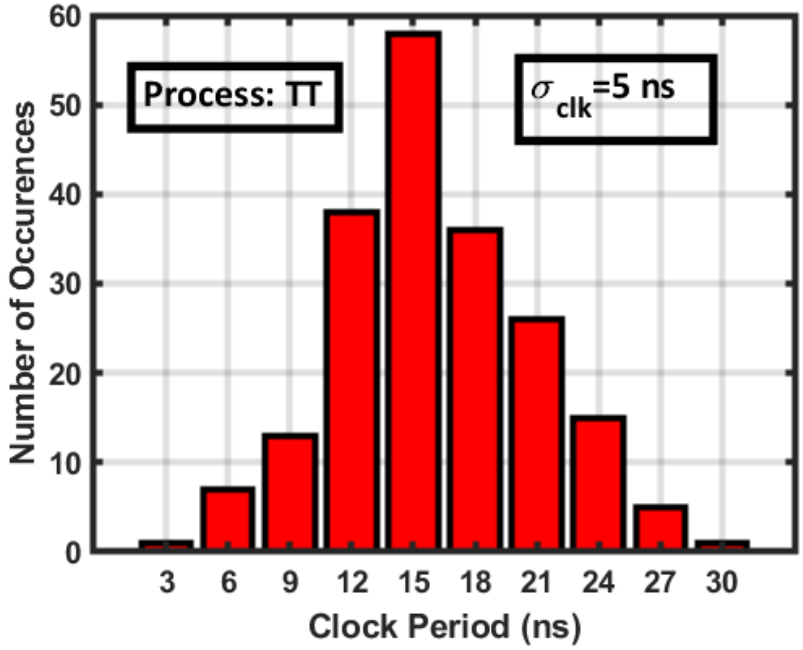


Figure 4.18: Simulated distribution of RO clock period for TT process corner.

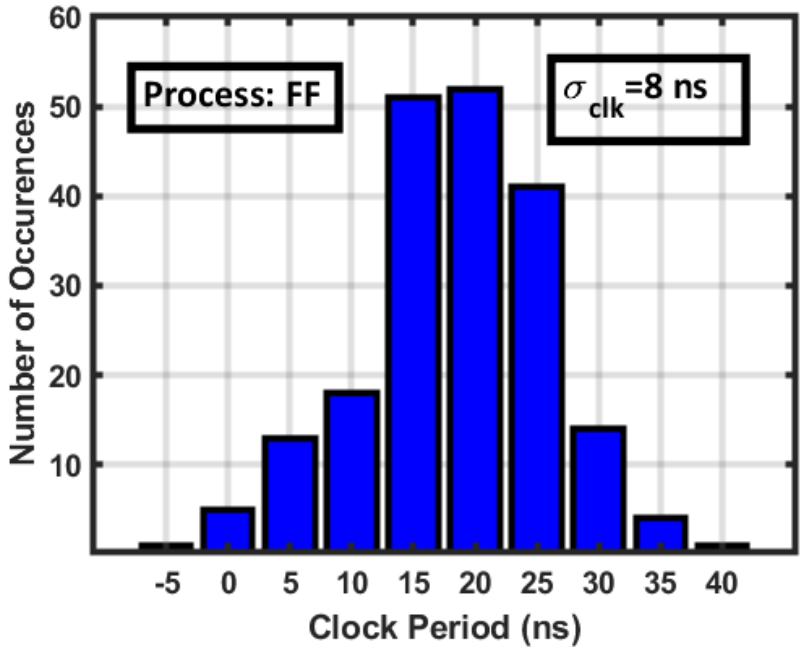


Figure 4.19: Simulated distribution of RO clock period for FF process corner.

is equal to the mean of the measured interval.

First, we apply this method on I_{dn}^2 and V_{an}^2. The jitter variance due to I_{dn}^2 can

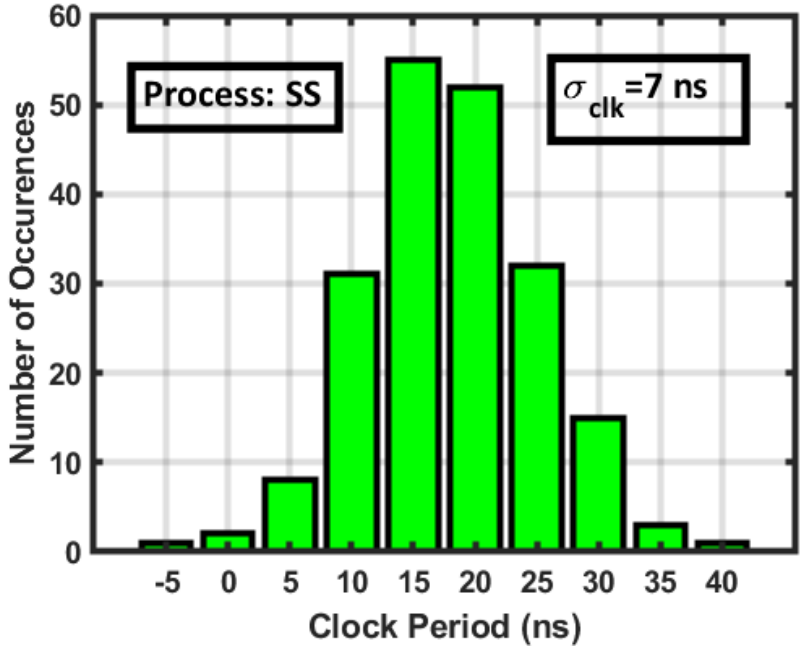


Figure 4.20: Simulated distribution of RO clock period for SS process corner.

be expressed as

$$\begin{aligned}\sigma_{tidn}^2 &= \int_0^\infty \left(\frac{T_{int}^2}{I_{diff}^2} sinc^2(fT_{int}) \times I_{dn}^2\right) df \\ &= \frac{T_{int}^2}{I_{diff}^2} I_{dn}^2 \int_0^\infty \frac{sin^2(\pi f T_{int})}{(\pi f T_{int})^2} df \\ &= \frac{T_{int}^2}{I_{diff}^2} I_{dn}^2 \int_0^\infty \frac{sin^2(x)}{x^2} \frac{dx}{\pi T_{int}} \\ &= \frac{T_{int}}{2I_{diff}^2} I_{dn}^2\end{aligned} \tag{4.20}$$

Similarly, the jitter variance due to V_{an}^2 is

$$\begin{aligned}\sigma_{tvan}^2 &= \int_0^\infty \left(\frac{T_{int}^2}{I_{diff}^2} sinc^2(fT_{int}) \times \frac{V_{an}^2}{R_0^2}\right) df \\ &= \frac{T_{int}}{2I_{diff}^2} \frac{V_{an}^2}{R_0^2}\end{aligned} \tag{4.21}$$

For the comparator, we assume propagation delays of t_p and t_n for the PMOS and NMOS transistors respectively. Thus, jitter variance due to I_{cp} and I_{cn} can be

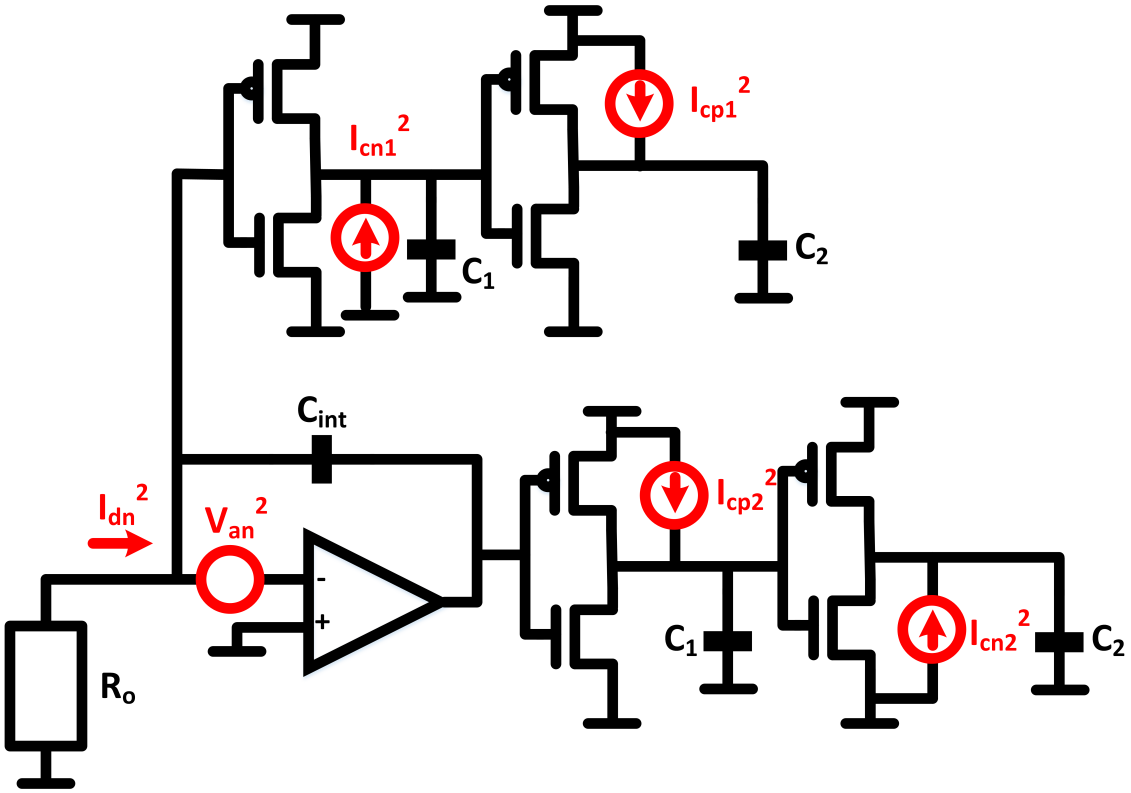


Figure 4.21: Schematic of CTIA frontend with noise sources indicated

written as

$$\begin{aligned}\sigma_{ticp}^2 &= \int_0^\infty \left(\frac{T_{int}^2}{I_{sat}^2} sinc^2(fT_{int}) \times I_{cp}^2\right) df \\ &= \frac{T_{int}}{2I_{sat}^2} I_{cp}^2\end{aligned} \tag{4.22}$$

$$\begin{aligned}\sigma_{ticn}^2 &= \int_0^\infty \left(\frac{T_{int}^2}{I_{sat}^2} sinc^2(fT_{int}) \times I_{cn}^2\right) df \\ &= \frac{T_{int}}{2I_{sat}^2} I_{cn}^2\end{aligned} \tag{4.23}$$

These are integral expressions for the uncertainty in propagation delay caused by current noise integrating on to the load capacitor. A more compact expression can be derived from this to arrive at the exact relation. However, just by looking at these integrals, it can be seen from these that as the integration period (T_{int}) increases, the rate of change of the dominant noise wander slows down, indicating that progressively lower frequencies are being accentuated, while the standard deviation widens, indicating a diffusion process.

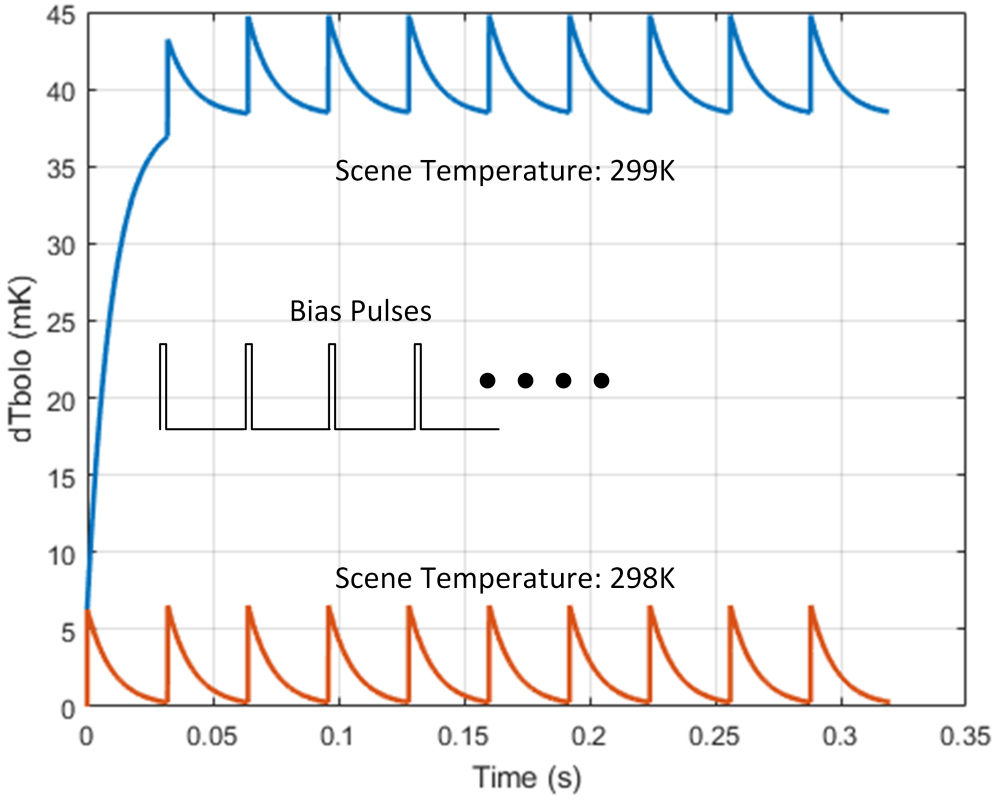


Figure 4.22: Change in bolometer temperature on the application of bias pulses

4.6 Self-Heating Compensation

One of the major concerns of designing a ROIC for microbolometer FPAs is the large change in temperature caused by bias heating during the application of bias on the microbolometer detector. Studies have shown that the temperature change due to bias-heating can be many times higher than the incident infrared signal [50]. The well-known heat balance equation [46] is expressed as

$$C_{th}\frac{\delta\Delta T}{\delta t} = \frac{\Delta T}{R_{th}} + \Delta P_{ir} + \frac{V_{bias}^2}{R_0 e^{(EA/k(T_{FPA}+\Delta T))}} \tag{4.24}$$

where C_{th} is the thermal capacity, ΔT is the change in bolometer temperature, R_{th} is the thermal resistance of the bolometer legs (in a suspended structure), ΔP_{ir} is the incident infrared power, V_{bias} is the applied bias on the bolometer detector, R_0 is an absolute resistance technology coefficient, EA is the activation energy and T_{FPA} is the FPA substrate temperature. The third term on the right hand side represents the power dissipated in the microbolometer due to the applied bias current or voltage.

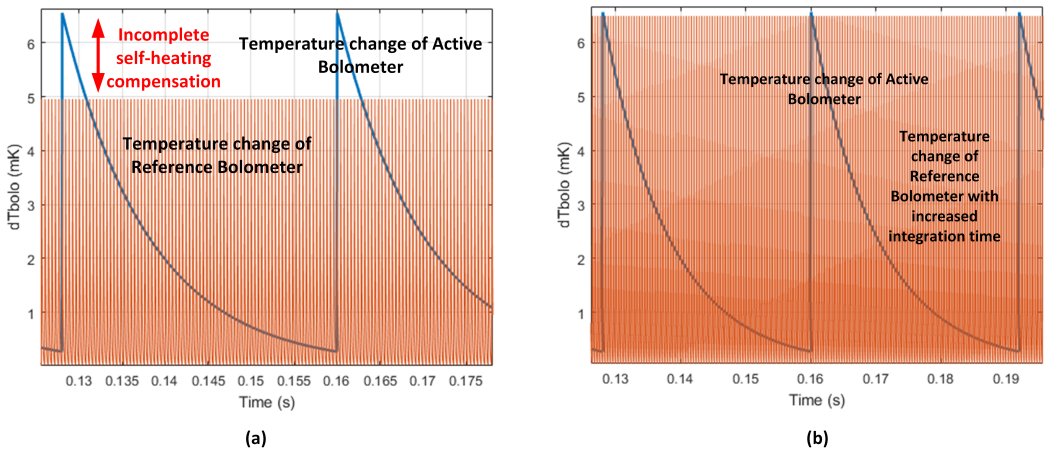


Figure 4.23: Comparison of temperature change in active and reference bolometers. (a) Small reset time (b) Slightly larger reset time

Although a large bias is preferable as it would help improve the responsivity of the readout, it is quite apparent from the equation that it can cause severe bias heating due to excessive power dissipation. The result is a considerable increase in the required readout dynamic range. Thus, it is very much desirable to compensate for the effect of self-heating. Two architectures were described in the state of the art chapter that address this issue, however, at the cost of increased complexity.

In this work, a reference blind microbolometer is employed to prevent self-heating from affecting the performance of the readout. This approach is widely used to tackle this problem. However, it has its limitations. Since, the reference bolometer has to be biased for each row inside the frame time, it needs to have a sufficiently low thermal conductance to be able to discharge heat faster. To illustrate this, behavioral simulations have been performed. In Figure 4.22, the change in bolometer temperature has been plotted when bias pulses are applied at two scene temperatures (a black body with adjustable temperature has been assumed). This plot has been generated by solving (4.24) in a numerical simulator. As seen in the plot, when the bias pulse is applied, the bolometer temperature shoots up and when the pulse is removed, it discharges to a temperature. It is clear that the heat discharge time of the reference bolometer needs to be much faster than this otherwise it will heat up excessively. This also helps to keep the reference bolometer unresponsive to infrared radiation. However, the downside is that the reference bolometer ends up having different heating/cooling cycles and creates a mismatch between the active

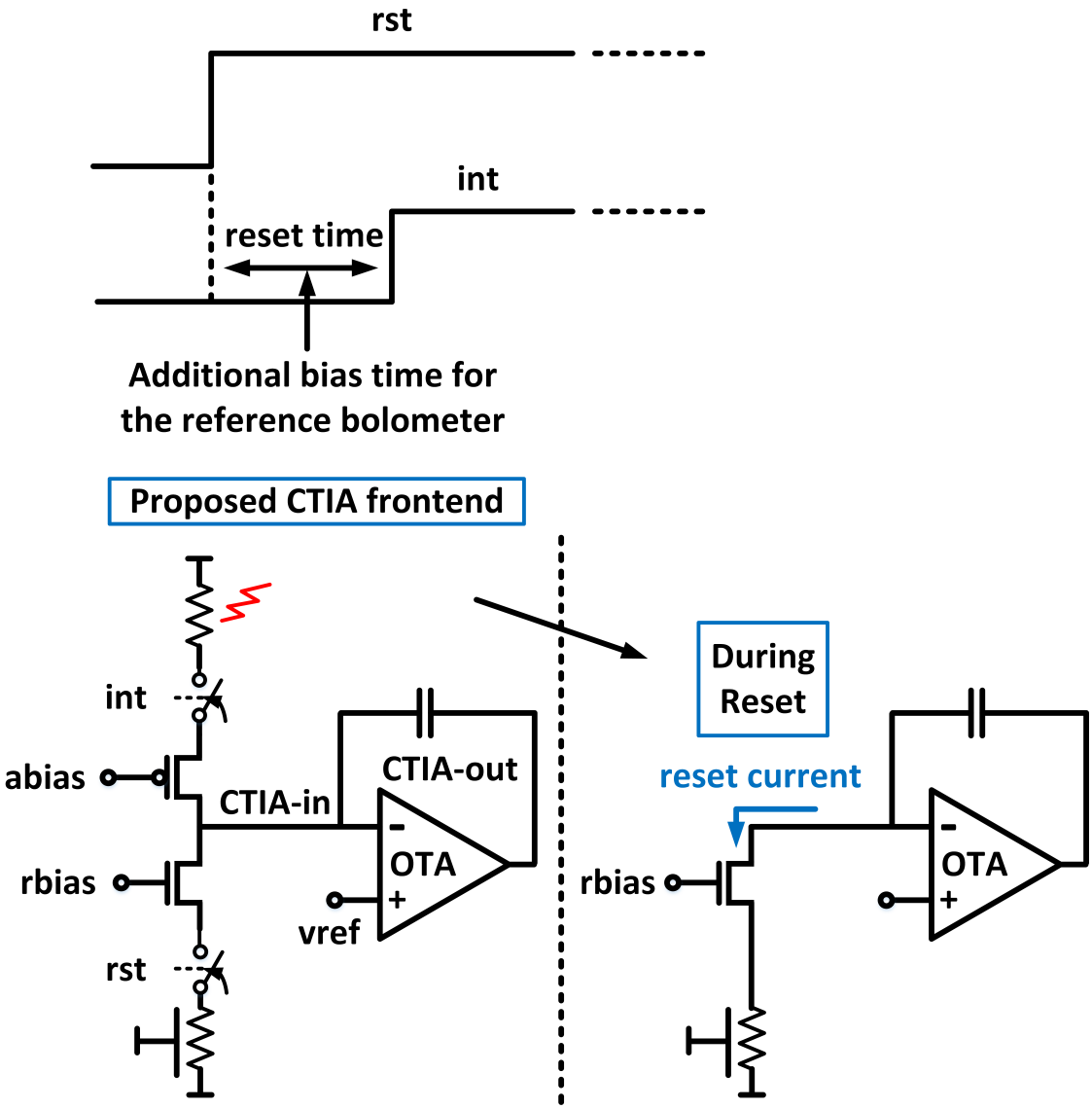


Figure 4.24: Proposed concept of self heating compensation

and reference bolometers as illustrated in Figure 4.23(a), where the difference in temperature is quite apparent.

To this end, a subtle opportunity in the proposed frontend pixel circuit has been exploited. The frontend circuit and its reset mechanism lend themselves well to a robust self-heating compensation technique. As illustrated in Figure 4.24, in a conventional CTIA based frontend circuit, during reset the output goes to vref while both *apixelen* and *rpixelen* are off. However, in the proposed frontend circuit, during reset the bias network reduces to the circuit shown on the right side of the figure. This is when *rpixelen* is high and , *apixelen* is low. During this time a bias is applied only on the reference bolometer and not on the active bolometer.

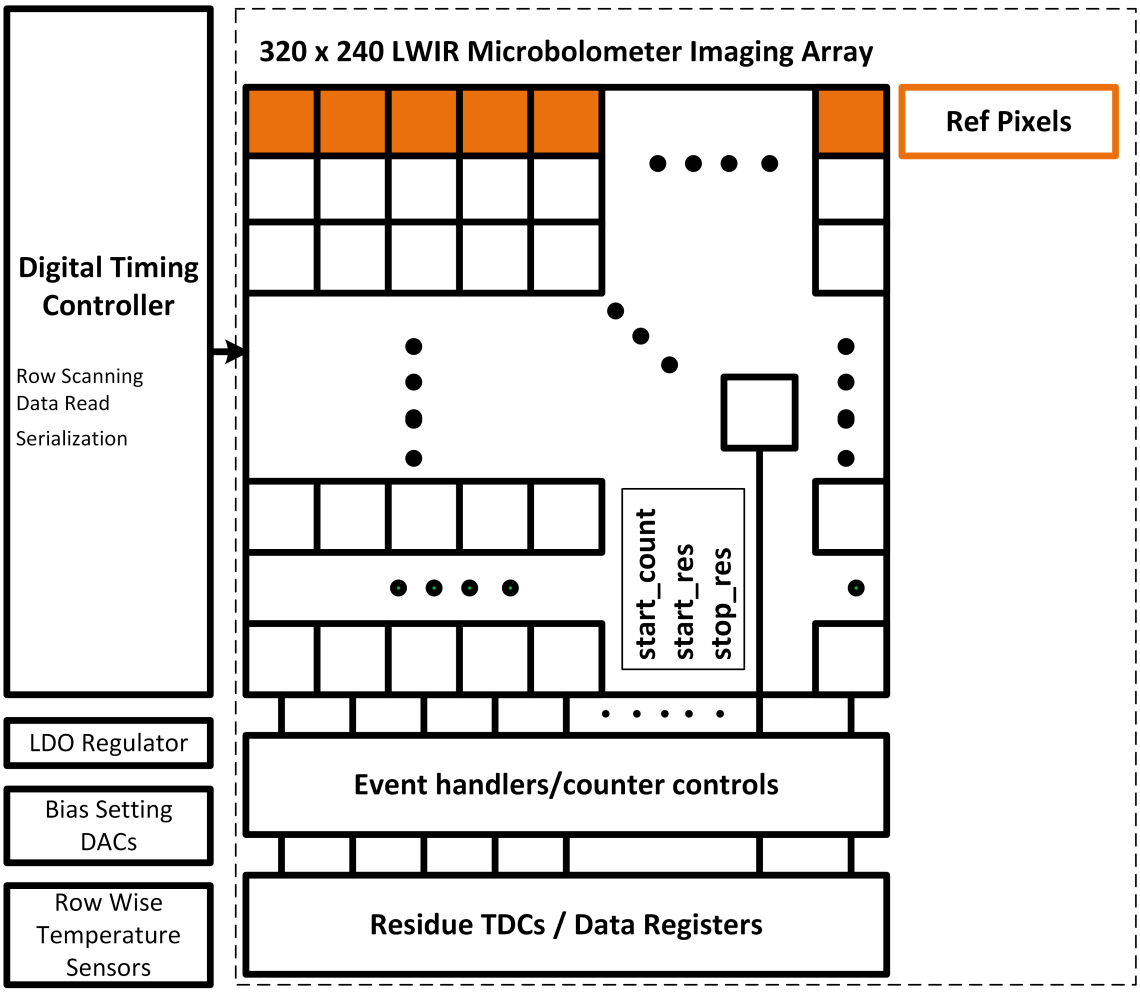


Figure 4.25: Proposed Microbolometer ROIC

The capacitor charges through the reference bolometer path to reset the CTIA amplifier. This is essentially an additional bias time for the reference bolometer. So it has an added amount of time to heat itself up further and, ideally, end up having the same temperature change as the active bolometer. This was simulated in the same numerical simulator but this time with 1.3 times higher bias time compared to the active bolometer. The result was the plot in Figure 4.23(b). As seen, the temperature change now matches with the active bolometer in a better way. This, however, will require a careful calibration of the reset time on the system (array) level such that the highest possible self-heating cancellation is achieved.

4.7 Array Design

Figure 4.25 depicts the proposed array. Each row of active pixels in the array is integrated sequentially. The top row has reference blind pixels for the purpose of

the cancellation of DC offsets and for self-heating compensation.

The digital control circuit will provide timing waveforms for the proper operation of the pixel and column circuits. It generates the *rst* and *int* signals required to reset and integrate the pixel circuit. The delay between these signals is adjustable so that the duration of reset is flexible. Additionally, the controller performs column-wise data read by serializing the 16-bit output. The controller also performs any programmability or reconfigurability related duties.

For the purpose of obtaining a low noise voltage supply and bias voltages, linear dropout (LDO) voltage regulators have been used outside the chip. This helps improve power supply rejection. A board with simple layout, less complexity and minimum number of components has a better EM/noise performance.

4.8 Chapter Summary

This chapter discussed the conceptual aspects and design considerations of the proposed time mode readout architecture and showed how the architecture has important implications on noise, power consumption and self-heating. The two-step integration enabled by the modified reset scheme of the CTIA led the way to incomplete settling technique described in Chapter 4 can be combined with a comparator look-ahead scheme to achieve a conversion rate of 500 MS/s. A layout strategy to reduce parasitic capacitances was also discussed. The next chapter will present the measurement results of our prototype ADC.

5 Chapter 5

Measurement Results

To demonstrate the effectiveness of the proposed readout approach, two prototype ROICs have been developed and characterized:

(i) Single Pixel Prototype IC (SPP-IC): A prototype in the form of a single-pixel, counter and data serializer is developed as a proof of concept. The pixel in this prototype is based on the TSI architecture. The idea is to find optimal bias conditions and to examine the implications of the dynamic readout time on the readout front-end.

(ii) 32×32 Array Prototype IC (32P-IC): A full blown 32×32 array prototype implementing the proposed time-mode readout. In this prototype, the pixels are based on the TSI-F architecture. Though the array size is 32×32, the ROIC has been over-designed for a 320×240 array format. This has implications on the overall consumption.

5.1 SPP-IC Implementation Details

Figure 5.1 shows the circuit schematic of the SPP-IC chip. To implement the two-step integration, a latch and counter are employed as off-pixel circuits. These circuits, in conjunction with the comparator, capture and process the integration start and stop events to facilitate time-mode processing. Once the comparator trips, its output is latched and integration is either started or stopped (by asserting/de-asserting *cstart*). Moreover, the 12-bit counter is enabled during the time that *cstart* is asserted. The data serializer performs data shift-out.

The measured timing waveform for SPP-IC can be seen in Figure 5.2. The timing waveform is similar to the operational timing of TSI pixel, however, the *cstart* signal is generated using a latch instead of using a manual input. When *start* is asserted, *ctiain* is pulled to *gnd* and, because of the high open-loop gain of the OTA, *ctiaout* is forced to *vdd*. Once start is de-asserted, *ctiain* integrates up to $vref$. At this point, the negative feedback becomes active and keeps *ctiain* at $vref$ causing *ctiaout* to integrate down until it reaches the comparator threshold (V_{th}).

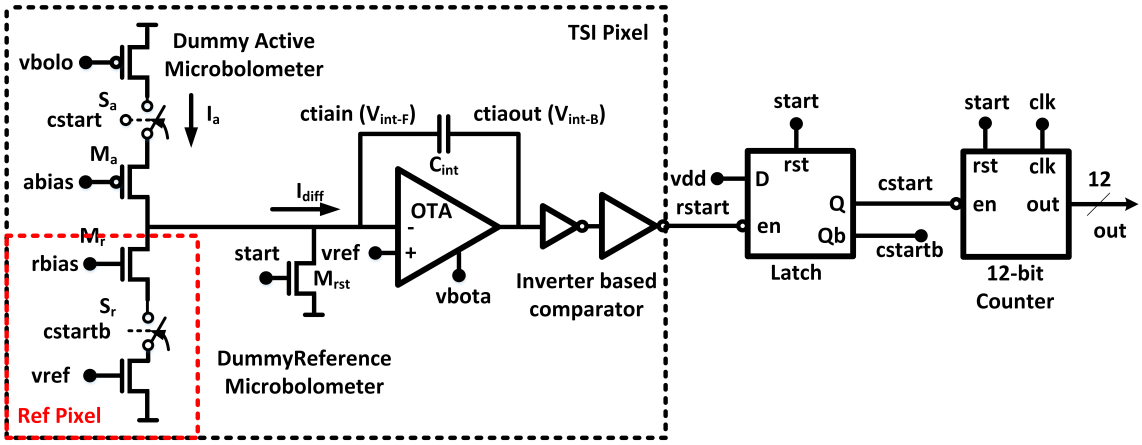


Figure 5.1: (a) SPP-IC die micrograph and (b) zoomed-in view of the chip core.

When the output of the CTIA reaches the threshold of the inverter, the latch gets enabled and a high value is written into the latch. Therefore, the output Q of the latch generates a stop event for the counter. This counter stop signal is also fed to a D flip-flop, which goes high at the next clock edge, generating a stop residue event. The inverters have been sized to drive a large load offered by the off-pixel long metal interconnects. Moreover, large inverters also provide a better pixel-to-pixel match.

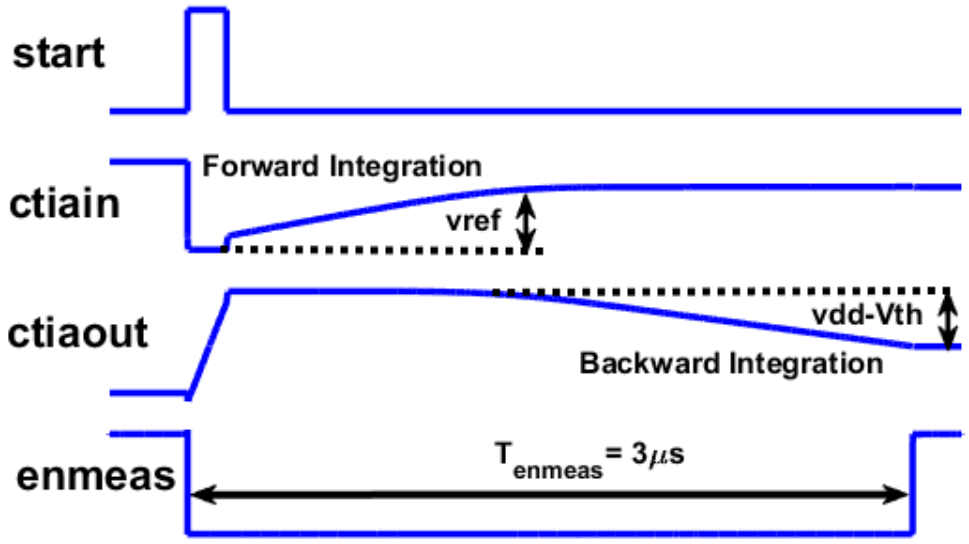


Figure 5.2: (a) SPPI Die Micrograph and (b) zoomed-in view of the chip core.

The challenge in the pixel design was to fit the active bolometer network, CTIA

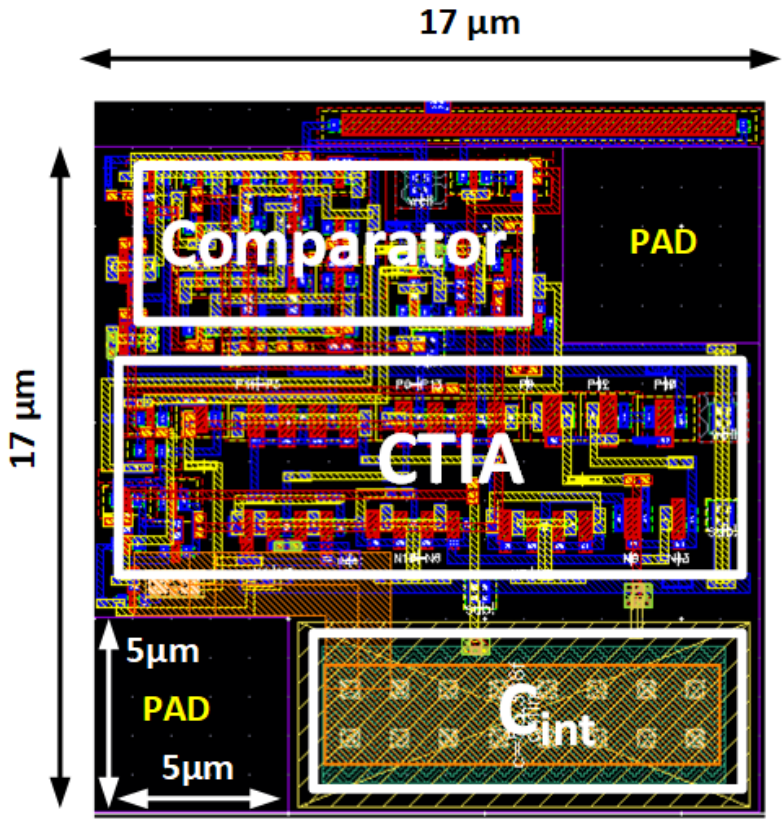


Figure 5.3: SPP-IC Pixel Layout.

and event generation circuitry within a $17\mu m \times 17\mu m$ area, while also leaving space for the detector pads. An operational transconductance amplifier (OTA) based on the 3 current mirror topology is chosen to have a compact design. Dimensions of the transistors are made as large as possible to reduce noise and mismatch. Moreover, the transistors in OTA operate in moderate inversion to save power.

Figure 5.3 shows the layout of the pixel. It can be seen that sufficient space for two microbolometer pads (5μm$\times 5\mu$m each) has been reserved inside the pixel. The remaining area is occupied by the in-pixel circuitry. Issues like matching and drive capability of the in-pixel circuits require adequately large device sizes, therefore, the transistors have been appropriately sized and inserted in the available area.

5.2 SPP-IC Measurements

The SPPI prototype is designed and fabricated using a 130-nm 5-metal bulk CMOS process. Die photo of the chip and zoomed-in view of the active part are shown in Figure 5.4(a) and Figure 5.4(b), respectively. For comprehensive testing,

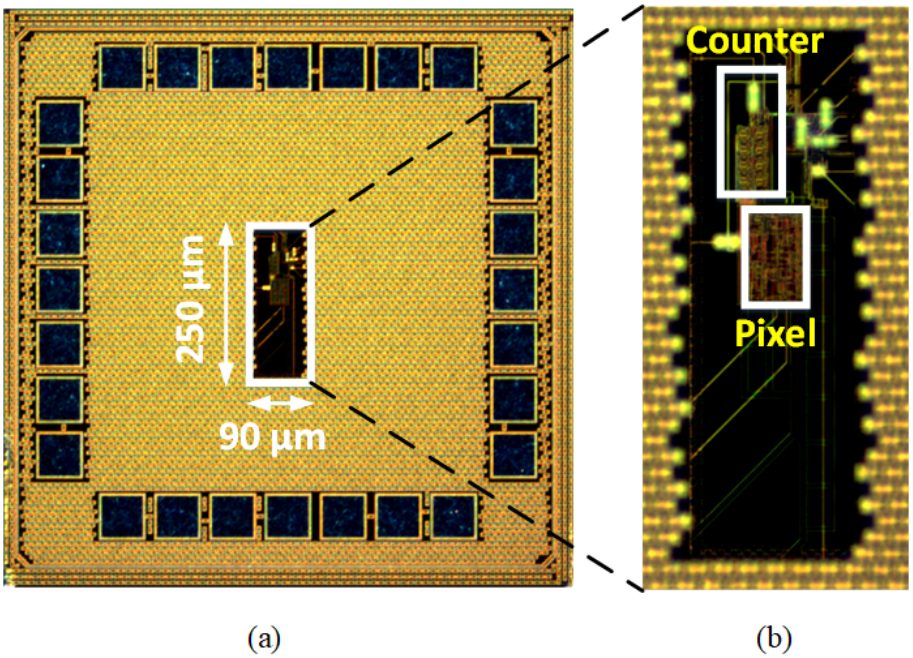


Figure 5.4: (a) SPPI Die Micrograph and (b) zoomed-in view of the chip core.

separate bias and supply voltages were used. For this reason, we see that the chip is pad-limited. Furthermore, on the most part, top metal fillers occupy the chip area to meet the minimum density requirements. This section proceeds by introducing the test setup. Subsequently, measurements, that have been carried out to characterize noise, dynamic range and power consumption, have been reported.

5.2.1 Test Setup

Figure 5.5 depicts the measurement setup of the SPP-IC prototype. The supply voltages are provided using LDO voltage regulators, whereas bias voltages are provided using high precision power supplies. Male SMA connectors, assembled on the PCB, provide a robust interface interface to supply pads on the IC package. Two kinds of decoupling capacitors are also employed. First, 10 nF capacitors are placed very close to the supply pins. These capacitors provide high frequency noise filtering. Secondly, 100 μF capacitors are placed within a distance of 2 in. from the chip. The purpose of these capacitor is to be a reservoir of charge to supply the instantaneous charge requirements of the circuits locally so the charge need not come through the inductance of the power trace. Figure 5.6 shows a screen shot of the layout of the two-layer PCB. Decoupling capacitors, labeled as $C\#$, can be seen along with the various connectors. Furthermore, a digital pattern generator is used

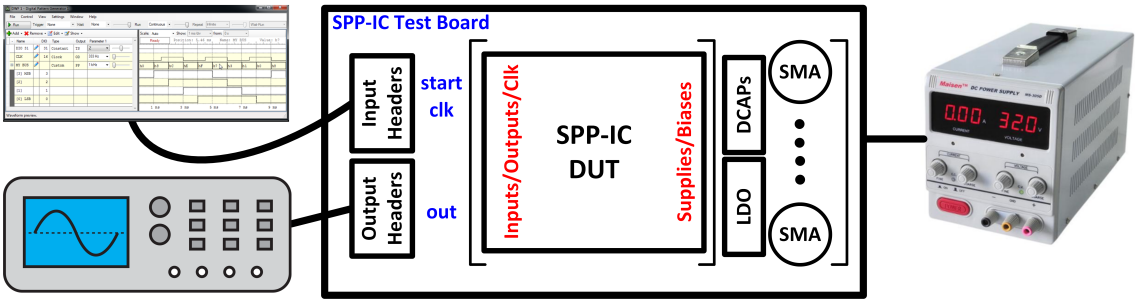


Figure 5.5: SPP-IC Test Setup.

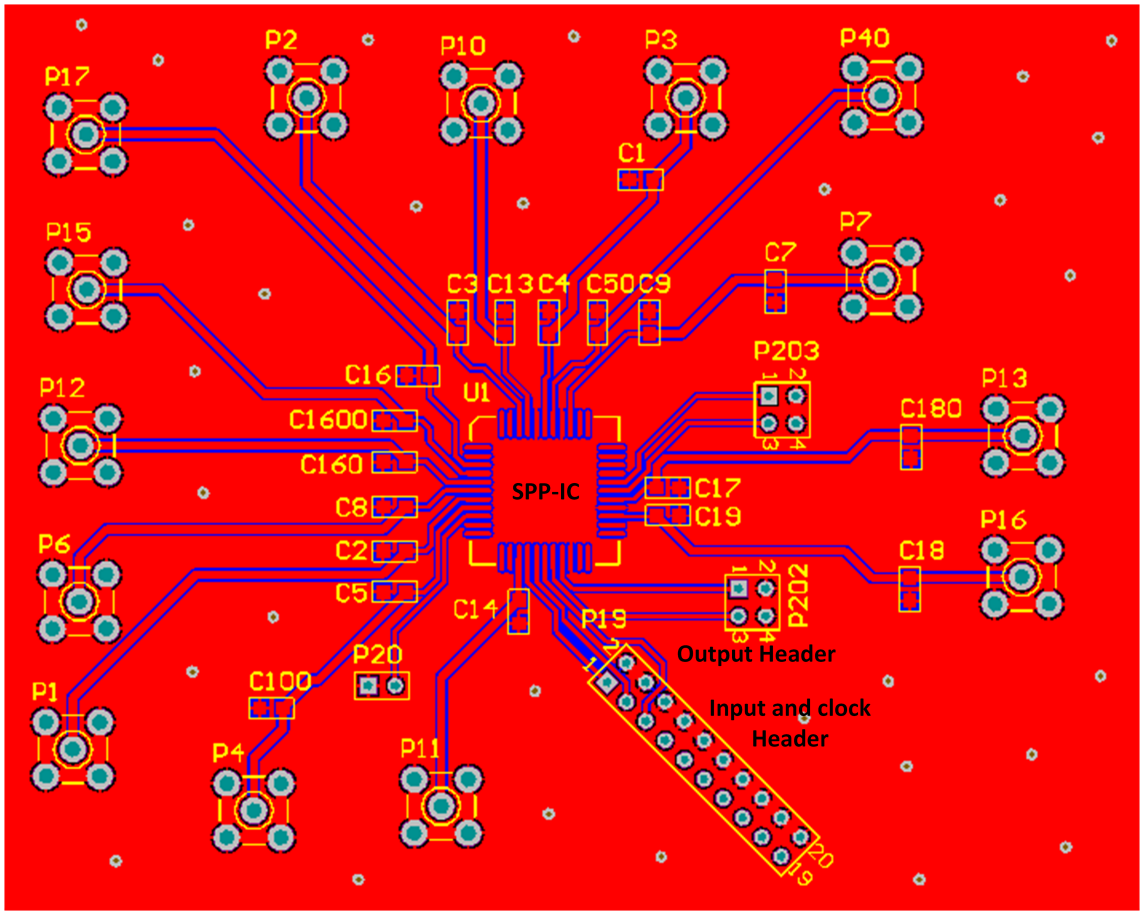


Figure 5.6: SPP-IC Test Board Layout.

to generate the *start* and *clk* signals. The resulting counter output is observed on a digital oscilloscope. This output is then manually read and placed on a network server for further processing on MATLAB.

5.2.2 Measurement Methodology

To characterize the chip, data is taken by reading contents of the 12-bit counter (*out* in Figure 5.1). By measuring 1000 integration periods and taking the mean, we obtain a quantized version of the integration time (T_{Qint}) which can be written

as

$$T_{Qint} = D_{cntr} \times T_{clk} - T_{start} \tag{5.1}$$

where T_{clk} is the clock period and T_{start} is the duration of start pulse. Similarly, standard deviation of these 1000 samples returns the noise. Measurements have been carried out for various input currents I_{diff} (through *vbolo*) and clock frequencies. Two clock frequencies of 60 MHz and 70 MHz have been used. The choice of frequency determines the amount of quantization noise and coupling induced noise.

For computational convenience, all the signal and noise measurements have been referred to the I_{diff} branch (Figure 5.1). From the measured values of T_{Qint}, I_{diff} can be calculated as

$$I_{diff} = \frac{C_{int} \times vref}{T_{Qbias}} + \frac{C_{int} \times (vdd - Vth)}{T_{Qbias}} \tag{5.2}$$

where V_{th} is the comparator threshold. Measured I_{diff} vs *vbolo* is plotted in Figure 5.7. We can see that *vbolo* provides a linear control of I_{diff}. Thus, all the subsequent measured quantities have been plotted against I_{diff}. However, we see that due to a large quantization error difference between 60 and 70 MHZ, there is a certain level shift. It will be shown in the measurements of 32p-IC that this error reduces because of the reduced quantization error.

5.2.3 Noise

To measure readout noise, we calculate the standard deviation of measured samples. Fig. 5.8 shows a plot of the noise (in pico-seconds) for the TSI pixel in SPP-IC.

5.2.4 Power Consumption

Finally, to measure power consumption, the *start* input was asserted periodically at a rate of 30 Hz and average current was extracted using a precision DC source. The proposed circuit consumes 27 μA. With a 1.2 V supply this is equivalent to a power consumption of 32 μW.

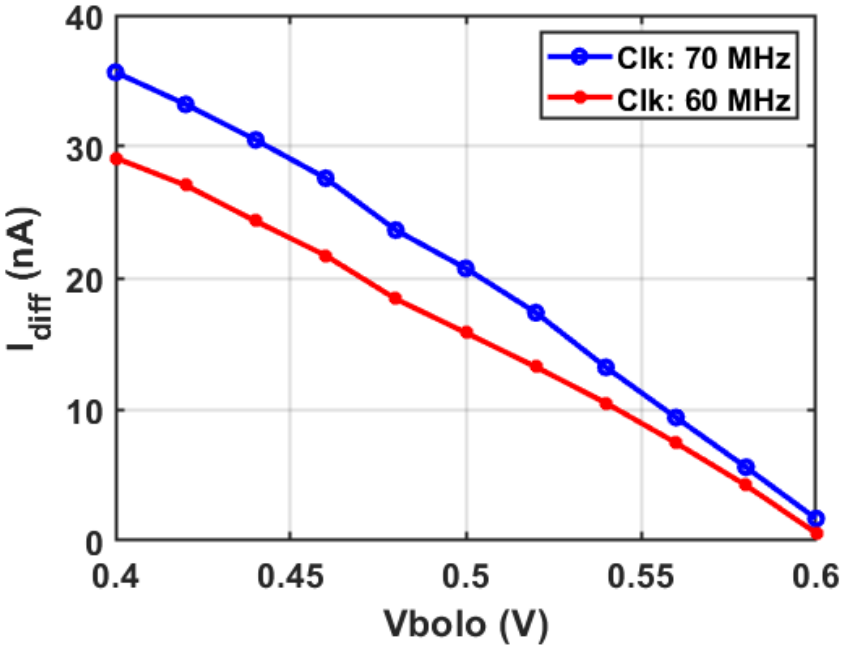


Figure 5.7: Measured I_{diff} vs *vbolo*.

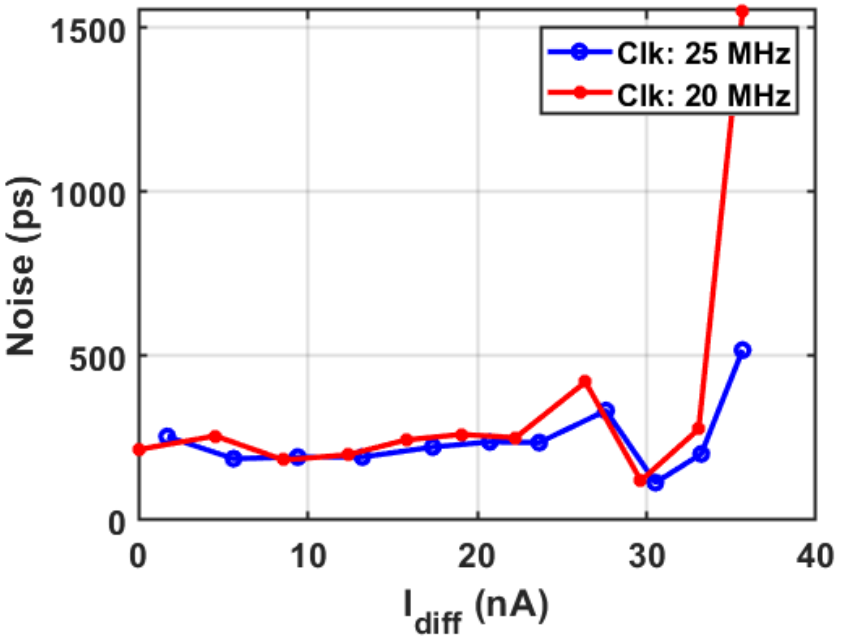


Figure 5.8: Measured $NETD$ vs I_{diff}.

5.3 32P-IC Implementation Details

Figure 5.9 shows a block diagram of the 32P-IC chip core. Each active pixel of the 32×32 array consists of a dummy detector network, a CTIA pre-amplifier and two inverter based comparators to generates the *cstart* and *rstart* events. We

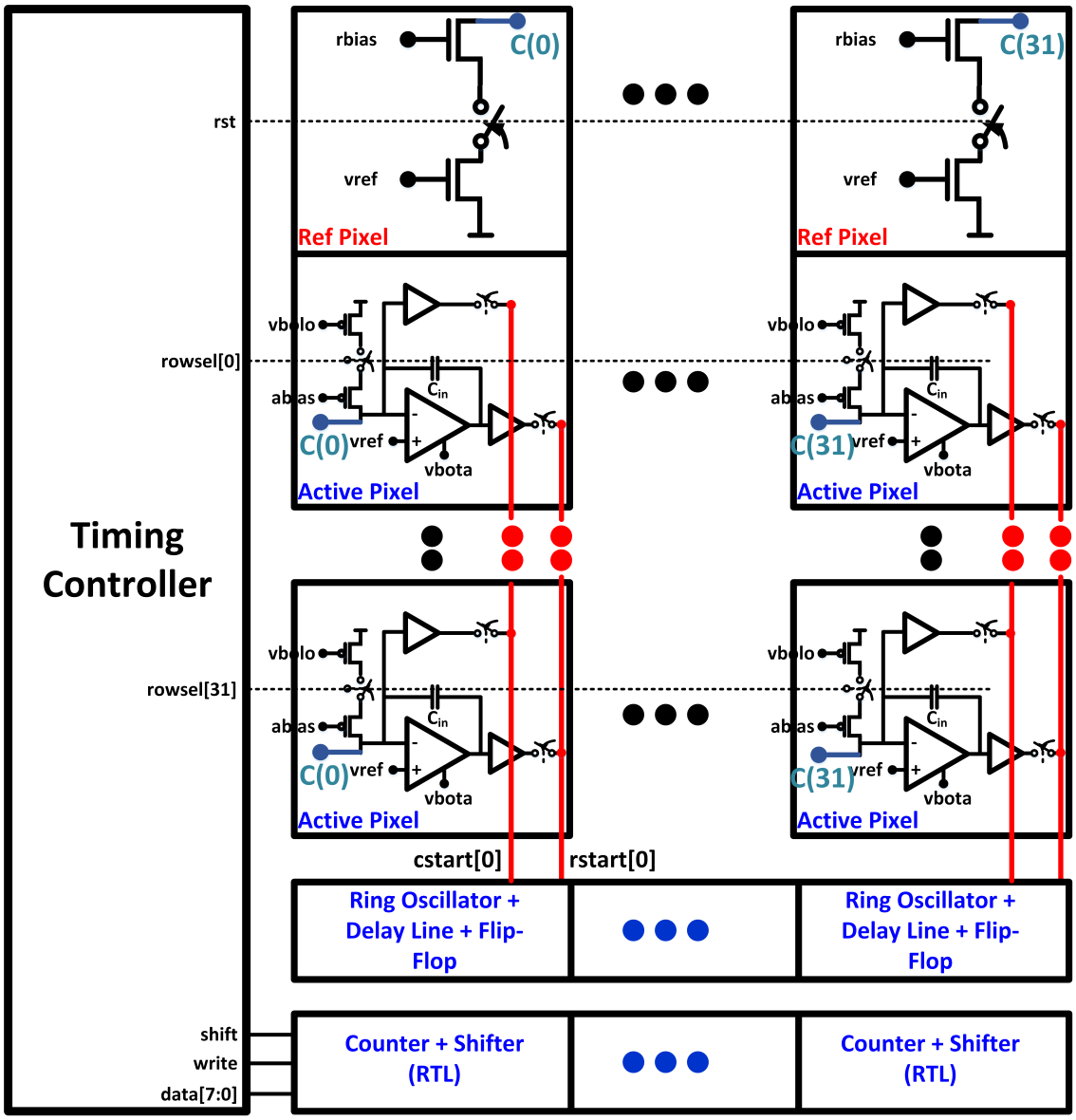


Figure 5.9: Measured ΔT_{Sc} vs I_{diff}.

note that the bias voltages $rbias$, $vref$, $vbolo$, $abias$ and $vbota$ are array wide. Furthermore, the rst signal, that turns the reference pixel on, and row select signals $rowsel[31:0]$ are buffered before being routed to the in-pixel switches. The buffers are over-designed and have been sized for 320 columns.

Figure 5.10 shows the layout of 32P-IC chip. It can be seen that the controller has been placed on the left side with the column circuits being at the bottom. Moreover, reference pixels (not labeled) are in the top row of the array. Bias routing is from the right side of the array, whereas supply/ground routing, using wide metal interconnects, has been drawn separately for the column circuits, array and controller.

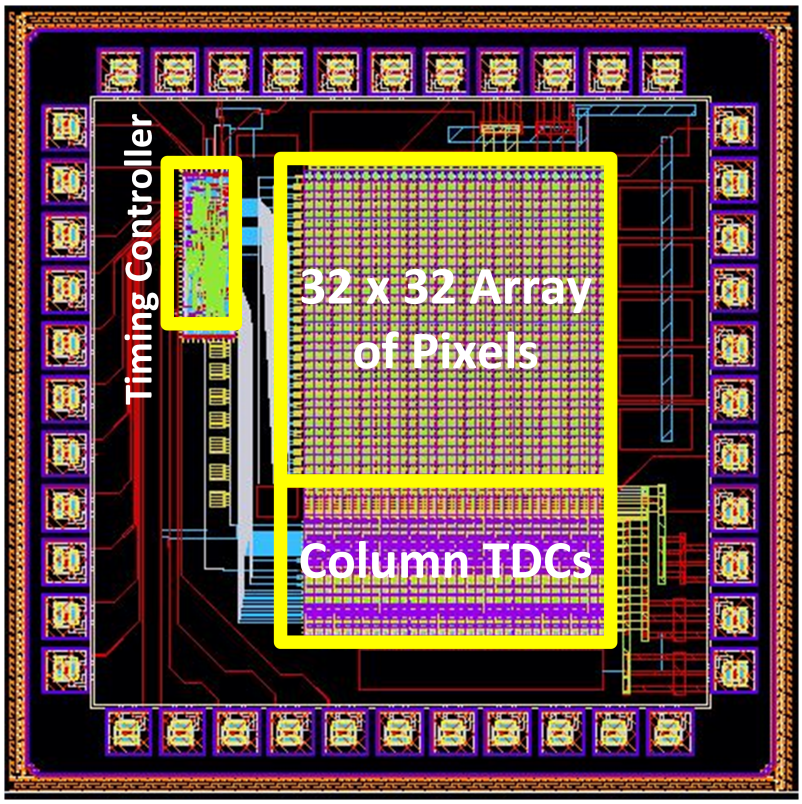


Figure 5.10: SPP-IC Pixel Layout.

5.4 32P-IC Measurements

The 32P-IC prototype is designed and fabricated using a 130-nm 5-metal bulk CMOS process. This section describes the test setup, subsequently reporting the various measurement results. Finally, a performance summary is provided along with a comparison with state of the art designs.

5.4.1 Test Setup

Figure 5.5 depicts the measurement setup of the 32P-IC prototype. It is pretty much the same as the test setup of SPP-IC. Figure 5.12 shows a screen shot of the layout of the two-layer PCB. Once again, we see decoupling capacitors both very close to and at a little distance from the package pins. The data extracting method is similar to what was described above in the SPP-IC test setup.

5.4.2 Measurement Methodology

To characterize the 32P-IC chip, data is taken by integrating each row and reading out (or shifting out) the corresponding 16 bit digital word. By measuring

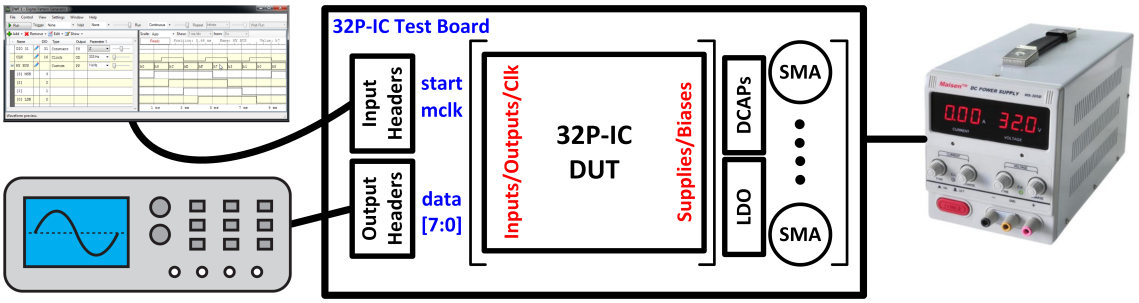


Figure 5.11: 32P-IC Test Setup.

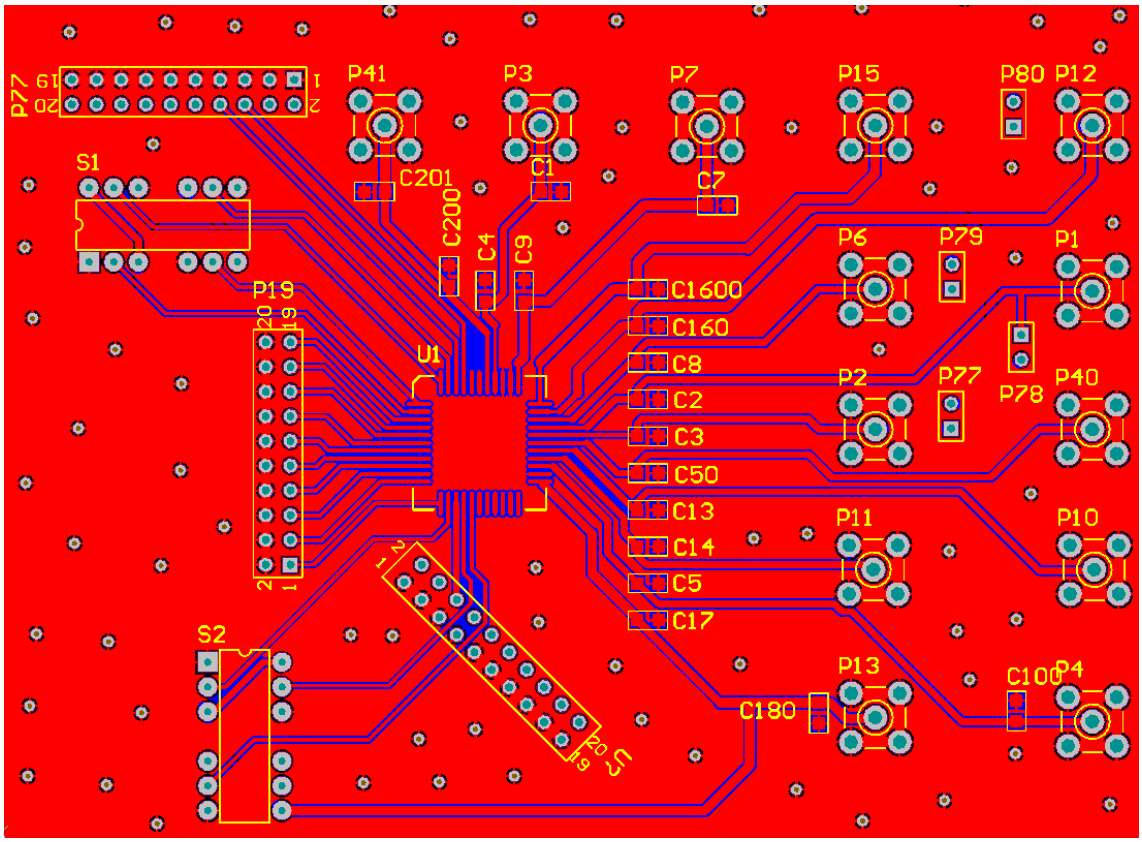


Figure 5.12: 32P-IC Test Setup.

1024 frames and taking the mean of each pixel, we obtain a quantized version of the integration time for the ith pixel ($T_{Qint,i}$), and can be written as

$$T_{Qint,i} = D_{cntr} \times \frac{T_{clkro}}{16} \tag{5.3}$$

where T_{clkro} is the clock period of the ring oscillator and the 16 in the denominator comes due to the fact that the delay line digitizes the residue (equivalent to one RO clock period) to 4 bits.

Next, the standard deviation of these 1024 samples for each pixel returns the

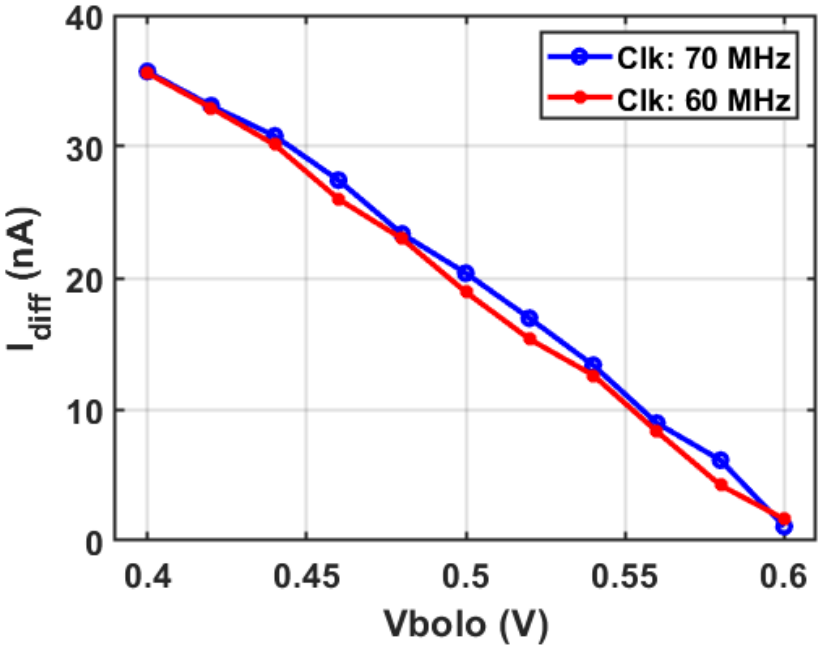


Figure 5.13: Measured I_{diff} vs *vbolo*.

temporal noise of each pixel. The noise across the array is then averaged to come up with a single noise measurement for given input current. These measurements have been carried out for various input currents I_{diff} (through *vbolo*) and clock frequencies. Once again, clock frequencies of 60 MHz and 70 MHz have been used.

Once again, referring these noise measurements to the I_{diff} branch leads to the plot in Figure 5.13. We can see that *vbolo* provides a linear control of I_{diff}. Thus, all the subsequent measured quantities have been plotted against I_{diff}.

5.4.3 Linearity

The plot of measured T_{qint} vs I_{diff} is shown in Figure 5.14. As indicated earlier, V_a and V_r need to be adjusted such that the desired integration time is achieved. Expectedly, the plot is nonlinear due to the inverse relationship between input current and integration time. To circumvent this nonlinearity, it is proposed that the inverse of the measured T_{Qbias} be taken to transform it to a frequency quantity. The result is plotted in Figure 5.15. F_{qint} essentially represents the frequency of a periodic signal in which every period is a replica of the integrated output. This would essentially require a digital inverse hardware or this operation could be carried out in a software platform.

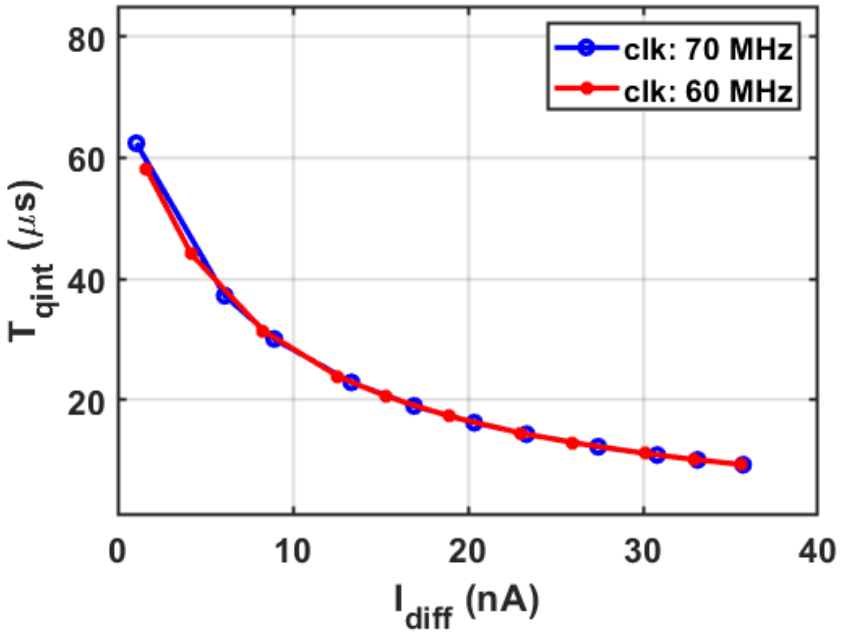


Figure 5.14: Measured T_{qint} vs I_{diff}.

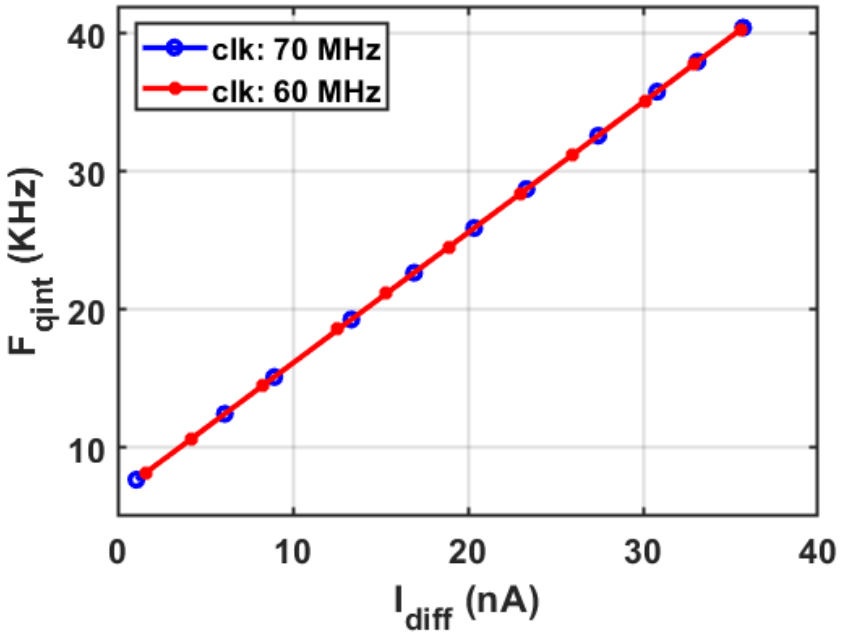


Figure 5.15: Measured F_{qint} vs I_{diff}.

5.4.4 NETD

To measure readout NETD, the following expression is used [51, 52]

$$NETD = \frac{(4F^2 + 1)\sigma_N}{AR_I I} \tag{5.4}$$

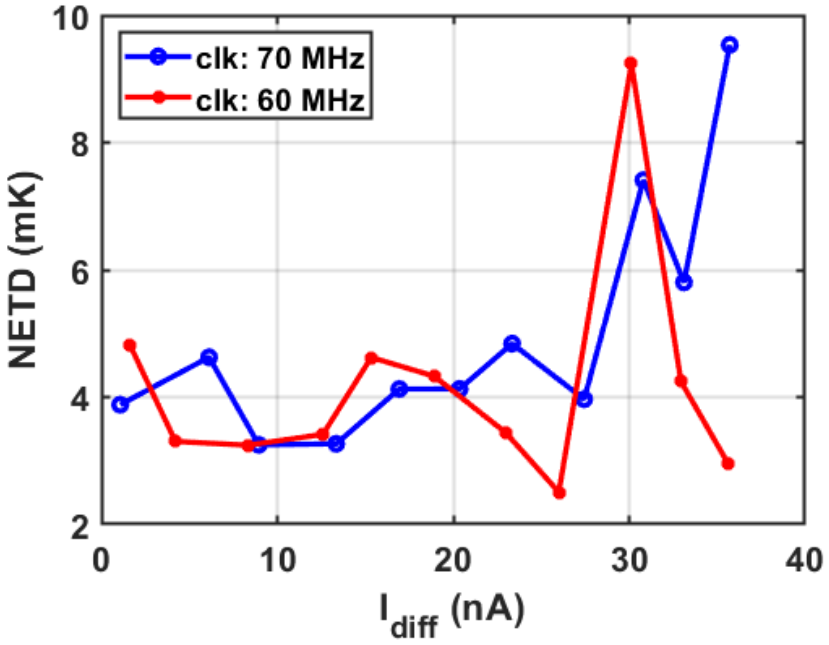


Figure 5.16: Measured $NETD$ vs I_{diff}.

where F is f-number of the detector optics, σ_N is readout noise referred to I_{diff} branch, A is pixel area, R_I is the current responsivity and I is black body integral. To determine the values of F, A and I, microbolometer characteristics need to be assumed. The target specifications are listed in Table 2. As far as σ_N is concerned, its value comes from the standard deviation of measured samples. R_I can be calculated using the following expression

$$R_I = \frac{\alpha V_r}{R_b G_{th}} = 0.75 A/W. \tag{5.5}$$

The NETD computed for f/1-optics is shown in Figure 5.16. Note that the NETD remains below 10 mK for the entire range of I_{diff}. A slight tendency towards higher noise at higher I_{diff} could be attributed to the larger noise bandwidth at larger values of I_{diff} (smaller bias time).

5.4.5 Dynamic Range

Furthermore, to measure the dynamic range, change in microbolometer temperature and, consequently, the corresponding scene temperature change has been computed from the measured data. The first step is to determine the current through the active microbolometer (I_a). With a voltage V_r across the reference microbolometer,

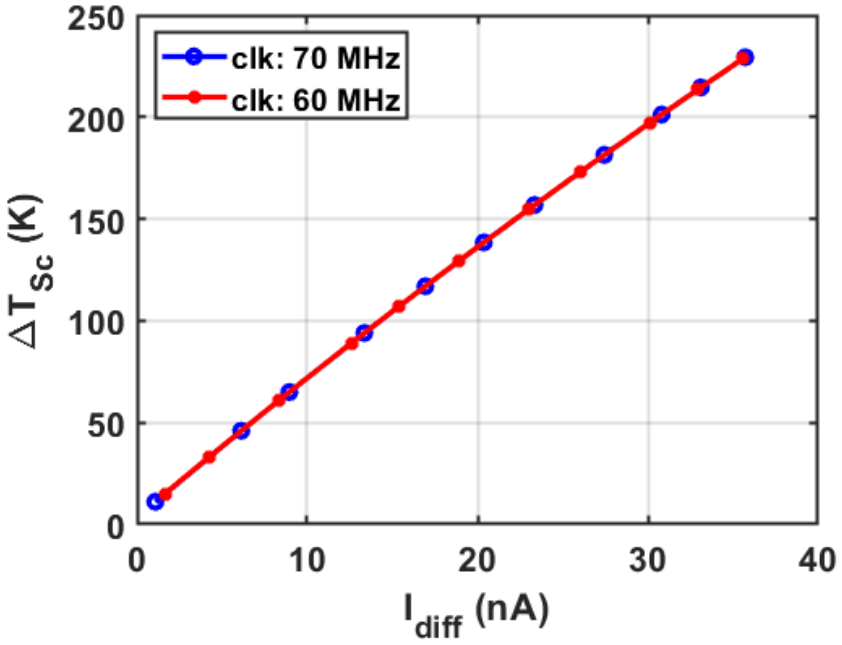


Figure 5.17: Measured ΔT_{Sc} vs I_{diff}.

I_a can be calculated as

$$I_a = \frac{V_r}{R_b} + I_{diff}. \tag{5.6}$$

This subsequently allows computing the change in microbolometer temperature (ΔT_{IR}) as follows

$$\Delta T_{IR} = \frac{1}{\alpha}\left(\frac{V_a}{I_a \times R_b} - 1\right). \tag{5.7}$$

where V_a is the bias voltage across the active microbolometer. The change in scene temperature has been determined using (4.16). Figure 5.17 plots the calculated scene dynamic range. Note that dynamic range on the lower side will be improved with more digital resolution.

5.4.6 Power Consumption

To measure power consumption, the readout operation is triggered by applying a single *start* pulse. The average current was then extracted using a precision DC source. Power consumption of the pixels and column TDCs is measured independently. Total power of a single pixel is a function of input current. Worst-case power of 20 μW is measured at the lowest I_{diff}. Moreover, each column ADC consumes 30 μW. This amounts to a total channel power consumption of 50 μW per read-

Table 3: Comparison with state of the art

	This work	**[37] 2017**	**[7] 2014**	**[40] 2013**
Process	0.13 μm	0.35 μm	0.5 μm	0.5 μm
Frame Rt.	60 Hz	60 Hz	60 Hz	60 Hz
ROIC	TDC based	Analog w/ Dig. CDS	Analog w/ multi bolos	Analog with conv. CDS
Supply	1.2 V	2.6 - 3.6 V	5 V	5 V
Pwr/Ch[a]	66 μW	562 μW	N/A	457 μW
Pitch	17 μm	35 μm	25 μm	35 μm
Dynamic Range	240 K	N/A	250 K	N/A

[a]Total power normalized to the number of column wise readout channels

out channel. For a fair comparison, we add 5 mW of estimated power contribution from I/O circuits/buffers and digital controller. Thus, for a targeted array size of 320×240, the total power comes out to be about 21 mW. Normalizing this total power to the number of column-wise readout channels results in 66 μW per readout channel.

5.4.7 Comparison with State of the Art

Table 3 provides a comparison of this work with other ROIC designs. As mentioned above, about 10 mW of additional power has been considered in the calculations for the proposed ROIC to compensate for power consumed by the chip level digital timing controller and by the IO pads/buffers. The improvement in power consumption is apparent from the table. Since the designs in [37, 40] use comparatively older processes and higher supplies, one could argue that in smaller technology nodes these designs could demonstrate reduced power. However, since these designs are essentially analog, with smaller dimensions, matching of analog circuits becomes more difficult and the lower supply voltages result in less voltage headroom and a lower SNR, requiring additional power for compensation. Thus, the presented design offers an innovative approach, in the form of a digital time-mode readout path, to achieve adequate noise performance at low power consumption. Furthermore, as indicated previously, the scene dynamic range is expected to improve when a TDC for residue digitization is included.

5.5 Chapter Summary

This chapter discussed the performance of two readout chips developed based on the proposed time mode concept. Competitive noise performance at low power consumption is demonstrated. The proposed readout concept thus has the potential to enable thermal imagers for portable low power applications such as Internet of Things (IoT).

6 Chapter 6

Conclusions and Future Directions

6.1 Conclusion

A highly digital readout technique for microbolometer based imagers has been proposed and demonstrated with a 32×32 aray prototype fabricated in a standard 130-nm bulk CMOS process. By employing a two-step integration based time-mode architecture, a low-noise low-power readout channel has been demonstrated. The resulting readout path circumvents the inevitably large power consumption, found in its analog counterparts, with the aid of a counter based time-to-digital converter. Moreover, short and variable bias times are proposed to suppress the impact of self heating on readout dynamic range. At a frame rate of 60 Hz, the proposed readout channel consumes 63 μW serving as a potential enabler of very low power microbolometer imagers. Additionally, the digital nature of the proposed architecture promises power and area scaling at advanced CMOS nodes.

6.2 Future Directions

6.2.1 Non-Uniformity and Substrate Temperature Variation

The features proposed in this work help satisfy the application requirements of low-cost, low-power, and low-size on the most part. However, one of the limiting elements is the requirement for a thermal-electric cooler to provide substrate temperature stabilization for the microbolometer imager. Such a cooler requires up to 2000 mW of power. Moreover, the settling time of such coolers is larger than 100ms and therefore doesn't favor the requirement of instant-on start in current systems. Consequently, adaptive substrate temperature compensation without a cooler is highly desirable.

To this end, it is suggested that the TSI-F pixel architecture has the potential to offer compensation of offset and non-linear (temperature dependent) gain. The initial phase of the TSI-F pixel operation integrates a fixed reset current (throught the reference microbolometer) and, therefore, the integrated time span carries in-

formation about the offset and gain errors resulting from the reference bolometer. This in conjunction with an arrangement of temperature sensors could potentially provide a means to compensate for temperature variations and could bar the need for a cooler.

6.2.2 Other TDC Architectures

The counter based TDC employed in the proposed ROIC proves to serve the purpose of low power and high resolution operation. However, if we are to learn from the voltage mode ADCs, when high resolution is desired in such ADCs, the noise shaping sigma delta modulators are the first choice. The equivalent of sigma delta in time domain is the gated ring oscillator based TDC reported in [53]. The input time signal is used to enable/disable a ring oscillator. One single measurement is done by counting all the phase transitions in the oscillator during the enabling phase. The quantization error, which refers to the intermediate state of the oscillator, is preserved between measurements. This results in a first-order noise shaping on the quantization noise. After digital low-pass filtering, the signal can be reconstructed with strongly reduced quantization error. This technique has the potential to be employed in imager applications since it can achieve high resolution with reasonable area consumption.

6.2.3 Towards Camera Development

Future possible directions also include the development of a thermal camera that utilizes the low-power capability of the proposed ROIC.

One aspect of this is the hybridized integration of the developed ROIC prototype with a microbolometer detector array. Since the proposed array has been designed for slow resistive microbolometer detectors, it is compatible with such thermal imaging systems. Moreover, sufficient space has been left for pad locations inside the pixels. The pad locations have the possibility to be relocated within the pixel as well, if needed.

Furthermore, for improved performance, the inclusion of low-dropout volatge regulators and digit-to-analog converters (DACs) is also suggested. The DACs will be used to allow easy adjustment of bias voltages. Moreover, on-chip bias generation

is also highly desirable to reduce supply pins.

References

[1] M. Moreno, R. Jimenez, A. Torres, and R. Ambrosio, "Microbolometers based on amorphous silicon–germanium films with embedded nanocrystals," *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2120–2127, jul 2015.

[2] P. Wang, S. Chen, X. Gan, R. Sun, W. Chen, S. Yang, and H. Wang, "High sensitivity 17μ pixel pitch 640×512 uncooled infrared focal plane arrays based on amorphous vanadium oxide thin films," *IEEE Electron Device Letters*, vol. 36, no. 9, pp. 923–925, sep 2015, doi: 10.1109/led.2015.2451995.

[3] D. Tezcan, S. Eminoglu, and T. Akin, "A low-cost uncooled infrared microbolometer detector in standard CMOS technology," *IEEE Transactions on Electron Devices*, vol. 50, no. 2, pp. 494–502, feb 2003, doi: 10.1109/ted.2002.807453.

[4] V. Ravinuthula, V. Garg, J. G. Harris, and J. A. B. Fortes, "Time-mode circuits for analog computation," *International Journal of Circuit Theory and Applications*, vol. 37, no. 5, pp. 631–659, jun 2009.

[5] S. Kavadias, P. D. Moor, and C. V. Hoof, "CMOS circuit for readout of microbolometer arrays," *Electronics Letters*, vol. 37, no. 8, p. 481, 2001.

[6] J. Seo, G. Kim, K. Lim, C. Seok, H. Kim, S. Im, J.-H. Kim, C.-Y. Kim, and H. Ko, "An analog front-end IC with regulated r-i amplifier and CDS CTIA for microbolometer," in *2013 13th International Conference on Control, Automation and Systems (ICCAS 2013)*. IEEE, oct 2013.

[7] J. Lv, L. Que, L. Wei, Y. Zhou, B. Liao, and Y. Jiang, "Uncooled microbolometer infrared focal plane array without substrate temperature stabilization," *IEEE Sensors Journal*, vol. 14, no. 5, pp. 1533–1544, may 2014.

[8] D. Svard, C. Jansson, and A. Alvandpour, "A readout circuit for an uncooled IR camera with mismatch and self-heating compensation," in *NORCHIP 2012*. IEEE, nov 2012.

[9] H. Baltes and A. Schaufelbühl, "Thermal imagers in cmos technology," pp. –, 2002.

[10] [Accessed:19-July-2018]. [Online]. Available: http://www.globalsources.com/si/AS/FLIR-Systems/6008830560341/pdtl/Thermal-Imaging-Camera/1053358970.htm

[11] www.scd.co.il. [Accessed:18-July-2018].

[12] [Accessed:18-July-2018]. [Online]. Available: https://www.slideshare.net/Yole_Developpement/yole-uncooled-thermalimaging2014sample

[13] [Accessed:19-July-2018]. [Online]. Available: http://www.raptorphotonics.com/wp-content/uploads/2015/10/Ninox-White-Paper-Final.pdf

[14] Y. E. Kesim, E. Battal, M. Y. Tanrikulu, and A. K. Okyay, "An all-ZnO microbolometer for infrared imaging," *Infrared Physics & Technology*, vol. 67, pp. 245–249, nov 2014.

[15] E. Mounier, "Uncooled infrared imagers market and technology trends," Yole Development, Tech. Rep., 2017.

[16] P. W. Kruse and D. D. Skaturd, *Uncooled Infrared Imaging Arrays and Systems*. Academic Press, 1997.

[17] K.-P. M. Michael Vollmer, *Infrared Thermal Imaging: Fundamentals, Research and Applications*. WILEY-VCH Verlag GmbH & Co., 2010.

[18] R. S. Saxena, A. Panwar, S. S. Lamba, and R. Bhan, "A sub-circuit model of a microbolometer IR detector and its experimental validation," *Sensors and Actuators A: Physical*, vol. 171, no. 2, pp. 138–145, nov 2011.

[19] D. J. Paul, "Si/SiGe heterostructures: from material and physics to devices and circuits," *Semiconductor Science and Technology*, vol. 19, no. 10, pp. R75–R108, sep 2004.

[20] M. Moreno, A. Torres, R. Ambrosio, and A. Kosarev, *Un-Cooled Microbolometers with Amorphous Germanium-Silicon a-GexSiy:HThermo-Sensing Films*. nTech, 2012.

[21] H. Nyquist, "Thermal agitation of electric charge in conductors," *Physical Review*, vol. 32, no. 1, pp. 110–113, jul 1928.

[22] F. Hooge, "1/f noise sources," *IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 1926–1935, 1994.

[23] F. Hooge and L. Vandamme, "Lattice scattering causes 1/f noise," *Physics Letters A*, vol. 66, no. 4, pp. 315–316, may 1978.

[24] P. W. Kruse, *Uncooled Thermal Imaging Arrays, Systems, and Applications*. SPIE, jul 2001.

[25] A. Tanaka, K. Chiba, T. Endoh, K. Okuyama, A. Kawahara, K. Iida, and N. Tsukamoto, "Low-noise readout circuit for uncooled infrared FPA," in *Infrared Technology and Applications XXVI*, B. F. Andresen, G. F. Fulop, and M. Strojnik, Eds. SPIE, dec 2000.

[26] W. J. Parrish, J. T. W. II, G. T. Kincaid, J. L. Heath, and J. D. Frank, "Low-cost 160 x 128 uncooled infrared sensor array," in *Infrared Readout Electronics IV*, B. Pain and T. S. Lomheim, Eds. SPIE, sep 1998.

[27] E. Mottin, A. Bain, J.-L. Martin, J.-L. Ouvrier-Buffet, S. Bisotto, J.-J. Yon, and J.-L. Tissot, "Uncooled amorphous silicon technology enhancement for 25-μm pixel pitch achievement," in *Infrared Technology and Applications XXVIII*, B. Andresen, G. F. Fulop, and M. Strojnik, Eds. SPIE, jan 2003.

[28] P. E. Howard, J. E. Clarke, A. C. Ionescu, C. C. Li, and J. C. Stevens, "DRS u6000 640x480 VO x uncooled IR focal plane," in *Infrared Detectors and Focal Plane Arrays VII*, E. L. Dereniak and R. E. Sampson, Eds. SPIE, aug 2002.

[29] T.-H. Yu, C.-Y. Wu, P.-Y. Chen, F.-W. Chi, J.-J. Luo, C. D. Chiang, and Y.-T. Cherng, "A new CMOS readout circuit for uncooled bolometric infrared focal plane arrays," in *2000 IEEE International Symposium on Circuits and Systems. Emerging Technologies for the 21st Century. Proceedings (IEEE Cat No.00CH36353)*. Presses Polytech. Univ. Romandes.

[30] C. Jansson, U. Ringh, and K. C. Liddiard, "Theoretical analysis of pulse bias heating of resistance bolometer infrared detectors and effectiveness of bias compensation," in *Infrared Technology XXI*, B. F. Andresen and M. Strojnik, Eds. SPIE, sep 1995.

[31] X. Gu, G. Karunasiri, J. Yu, G. Chen, U. Sridhar, and W. Zeng, "On-chip compensation of self-heating effects in microbolometer infrared detector arrays," *Sensors and Actuators A: Physical*, vol. 69, no. 1, pp. 92–96, jun 1998.

[32] A. Tanaka, S. Matsumoto, N. Tsukamoto, S. Itoh, K. Chiba, T. Endoh, A. Nakazato, K. Okuyama, Y. Kumazawa, M. Hijikawa, H. Gotoh, T. Tanaka, and N. Teranishi, "Infrared focal plane array incorporating silicon IC process compatible bolometer," *IEEE Transactions on Electron Devices*, vol. 43, no. 11, pp. 1844–1850, 1996.

[33] S. I. Haider, S. Majzoub, M. Alturaigi, and M. Abdel-Rahman, "Column-wise ROIC design for uncooled microbolometer array," in *2015 International Conference on Information and Communication Technology Research (ICTRC)*. IEEE, may 2015.

[34] C. Hwang, C. Kim, Y. Lee, and H. Lee, "Pixelwise readout circuit with current mirroring injection for microbolometer FPAs," *Electronics Letters*, vol. 44, no. 12, p. 732, 2008.

[35] D. Liu, Z. Chen, W. Lu, and S. Lei, "Low-noise readout circuit for thermoelectrical cooler-less uncooled microbolometer infrared imager," *Electronics Letters*, vol. 52, no. 9, pp. 705–706, apr 2016.

[36] J. Lv, Y. Jiang, D. Zhang, and Y. Zhou, "Ultra-low-noise readout integrated circuit for uncooled microbolometers," *Electronics Letters*, vol. 44, no. 12, p. 733, 2008.

[37] S. Park, T. Cho, M. Kim, H. Park, and K. Lee, "A shutter-less micro-bolometer thermal imaging system using multiple digital correlated double sampling for mobile applications," in *2017 Symposium on VLSI Technology*. IEEE, jun 2017.

[38] J. C. Mather, "Bolometer noise: nonequilibrium theory," *Applied Optics*, vol. 21, no. 6, p. 1125, mar 1982.

[39] D. Svärd, C. Jansson, and A. Alvandpour, "A readout IC for an uncooled microbolometer infrared FPA with on-chip self-heating compensation in 0.35 μm CMOS," *Analog Integrated Circuits and Signal Processing*, vol. 77, no. 1, pp. 29–44, aug 2013, doi: 10.1007/s10470-013-0116-9.

[40] J. Lv, H. Zhong, Y. Zhou, B. Liao, J. Wang, and Y. Jiang, "Model-based low-noise readout integrated circuit design for uncooled microbolometers," *IEEE Sensors Journal*, vol. 13, no. 4, pp. 1207–1215, apr 2013.

[41] M. Yang, S.-C. Liu, and T. Delbruck, "A dynamic vision sensor with 1% temporal contrast sensitivity and in-pixel asynchronous delta modulator for event encoding," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 2149–2160, sep 2015.

[42] C. Brandli, R. Berner, M. Yang, S.-C. Liu, and T. Delbruck, "A 240 × 180 130 dB 3 μs latency global shutter spatiotemporal vision sensor," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 10, pp. 2333–2341, oct 2014.

[43] C. Posch, D. Matolin, R. Wohlgenannt, T. Maier, and M. Litzenberger, "A microbolometer asynchronous dynamic vision sensor for lwir," *IEEE Sensors Journal*, vol. 9, no. 6, pp. 654–664, jun 2009, doi: 10.1109/jsen.2009.2020658.

[44] S. Eminoglu, M. A. Gulden, N. Bayhan, O. S. Incedere, M. Isikhan, S. T. Soyer, C. Yalcin, C. M. B. Ustundag, S. Kocak, O. Turan, U. Eksi, and T. Akin, "A 640x480-17um ROIC for uncooled microbolometer FPAs," in *Infrared Technology and Applications XLI*, B. F. Andresen, G. F. Fulop, C. M. Hanson, and P. R. Norton, Eds. SPIE, jun 2015.

[45] A. Shafique, S. Abbasi, O. Ceylan, Y. Yamamoto, C. B. Kaynak, M. Kaynak, and Y. Gurbuz, "Comprehensive predictive device modeling and analysis of a $Si/Si_{1-x}Ge_x$ multiquantum-well detector," *IEEE Transactions on Electron Devices*, pp. 1–9, 2018.

[46] B. Dupont, A. Dupret, E. Belhaire, and P. Villard, "FPN sources in bolometric infrared detectors," *IEEE Sensors Journal*, vol. 9, no. 8, pp. 944–952, aug 2009.

[47] S. Abbasi, A. Shafique, O. Ceylan, C. B. Kaynak, M. Kaynak, and Y. Gurbuz, "A test platform for the noise characterization of SiGe microbolometer ROICs," *IEEE Sensors Journal*, vol. 18, no. 15, pp. 6217–6223, aug 2018.

[48] A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, aug 2006.

[49] S. U. P. A. Papoulis, *Probability, Random Variables, and Stochastic Processes*. New York: McGraw Hill, 2002.

[50] A. Tanaka, S. Matsumoto, N. Tsukamoto, S. Itoh, K. Chiba, T. Endoh, A. Nakazato, K. Okuyama, Y. Kumazawa, M. Hijikawa, H. Gotoh, T. Tanaka, and N. Teranishi, "Influence of bias heating on a titanium bolometer infrared sensor," in *Infrared Technology and Applications XXIII*. SPIE, aug 1997.

[51] A. Ahmed and R. Tait, "Characterization of an amorphous $Ge_xSi_{1-x}O_y$ microbolometer for thermal imaging applications," *IEEE Transactions on Electron Devices*, vol. 52, no. 8, pp. 1900–1906, aug 2005, doi: 10.1109/ted.2005.852545.

[52] H. M. Oloomi, M. S. Alam, and M. M. Rana, "Noise performance evaluation of uncooled infrared detectors (june 2009)," *IEEE Sensors Journal*, vol. 11, no. 4, pp. 971–987, apr 2011.

[53] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, apr 2009.