Consideration of Electromagnetic Noise During Design of Inverter for Transportation Applications

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Consideration of Electromagnetic Noise During Design of Inverter for Transportation Applications

Berücksichtigung elektromagnetischer Störungen bei der Auslegung von Wechselrichtern für Transportanwendungen

Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)
genehmigte Dissertation von Danil Drozhzhin aus Tscherepowetz, Russische Föderation
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List of Symbols and Abbreviations

List of symbols

C_{dc}	$20\,\mu$F	DC link capacitance
C_{ds}	nF	drain-source capacitance
C_{gs}	nF	gate-source capacitance
C_{dg}	nF	drain-gate capacitance
C_{ac}	nF	anode-cathode capacitance
C_{mh}	12.2 pF	capacitance between MOSFET and heatsink
C_{dh}	6.8 pF	capacitance between diode and heatsink
C_{gd}	7 pF	capacitance of gate driver
C_{ms}	0.5 pF	stray capacitance of delta-sigma converter
C_{y_i}	33 pF	Y-capacitance of i input cell
d	m	gap distance
E_{tot}	mJ	total energy loss per one commutation
ε_0	$8.854 \times 10^{-12}\,\mathrm{F\,m^{-1}}$	permittivity of vacuum
ε		electrical permittivity
f_s	μs	sampling frequency
f_{clk}	50 MHz	clocking frequency of FPGA
I_{in}	A	input current of inverter
I_{out}	A	output phase current of inverter
I_d	A	drain current
I_{dm}	A	differential mode current source
I_{cm}	A	common mode current
I_{dm1}	A	differential mode current 1
I_{dm2}	A	differential mode current 2
$I_{cm.o}$	A	output common mode current of inverter
$I_{dm1.o}$	A	output differential mode current 1 of inverter
$I_{dm2.o}$	A	output differential mode current 2 of inverter
$I_{cm.i}$	A	input common mode current of inverter
$I_{dm.i}$	A	differential mode current of inverter
I_{sat}	mA	saturation current
i_g	A	gate current
L_{lead}	7 nH	lead inductance of power switch
L_Σ	nH	total stray inductance
$L_{w.fm}$	36 nH	inductance between filter and measurement circuit

$L_{\text{w.mi}}$	86 nH	inductance between measurement circuit and inverter
$L_{\text{w.t}}$	43 nH	inductance of PCB
$L_{\text{w.t}}$	141 nH	inductance between inverter and measurement circuit
m		modulation index
P	kW	Motor load
Q_{ds}	nC	drain-source charge
Q_{ac}	nC	anode-cathode charge
R_{g}	Ω	gate resistor
R_{d_i}	Ω	damping resistance of i input cell
T_{s}	μs	sampling time
t_{DT}	500 ns	dead time
t_{f}	ns	fall time of MOSFET
U_{ref}	V	reference voltage
U_{Δ}	V	triangle signal
U_{cm}	V	common mode voltage
U_{dm1}	V	differential mode voltage 1
U_{dm2}	V	differential mode voltage 2
U_{dc}	540 V	DC link voltage
U_{ds}	V	drain-source voltage
V_{d}	V	forward voltage of diode
Z_{s}	Ω	source impedance
Z_{motor}	Ω	motor phase impedance
Z_{l}	Ω	receiver impedance
$Z_{\text{cm.i}}$	Ω	input CM impedance of inverter
$Z_{\text{cm.o}}$	Ω	output CM impedance of inverter

List of abbreviations

AC	alternating current
ACPI	auxiliary commutated pole inverter
ADC	analog to digital converter
AEA	all electric aircraft
AZPWM	active zero PWM
CM	common mode
DC	direct current
DM	differential mode
DSP	digital signal processor
EM	electromagnetic
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ESL	equivalent series inductance

ESR	equivalent series resistance
EUT	equipment under test
FB	full-bridge
FEM	finite element model
FPGA	field-programmable gate array
GaN	gallium nitride
GPS	global positioning system
IC	integral circuit
IGBT	insulated gate bipolar transistor
LF	low-frequency
MCU	micro controller unit
MEA	more electric aircraft
MM	mixed mode
MOSFET	metal-oxide-semiconductor field effect transistor
NPC	neutral point clamped
NSPWM	near state PWM
PCB	printed circuit board
PFC	power factor correction
PV	photovoltaic
PWM	pulse width modulation
RBW	resolution bandwidth
RCMV-PWM	reduced common mode voltage PWM
RF	radio frequency
RMS	root mean square
RSPWM	remote state PWM
RTCA	radio technical commission for aeronautics
Si	silicon
SiC	silicon carbide
SPWM	sinusoidal PWM
SVPWM	space vector PWM
SWDFT	short-window Fourier transform
USB	universal serial bus
VNA	vector network analyser
VSC	voltage source converter
WBG	wide bandgap//

Abstract

One of the main goals in modern power electronics lies in the increase of power density. This trend is mostly provoked by the electrification in the transportation (electric/hybrid vehicles and aircraft). The increase of power density should be resolved keeping the other parameters of power converters such as cost and degree of complexity on the adequate level. Moreover, all environmental conditions should be also fulfilled regarding the application. The power converters were improved from the topology and control point of view since the invention of silicon (Si) insulated gate bipolar transistors (IGBT) at the beginning of the '80s. However, the development and appearance on the market of the new power switches took the most attention of engineers in the last decade. Such semiconductor materials as silicon carbide (SiC) and gallium nitride (GaN) introduce a new class of power switches with reduced switching and conduction losses. At the first view, it seems that it is possible to improve the existing power converters only by the replacement of the conventional Si power switches. It is often assumed that such a simple approach reduces the size of the cooling system and/or the size of the passive components due to the increased switching frequency. However, low switching losses are also associated with short commutation times (rise/fall times of voltages and currents) and with high voltage slew rate ($\frac{du}{dt}$). The increased switching frequency and high values of $\frac{du}{dt}$ introduces new limitations in the design of power converters, which were underestimated or neglected in the power electronics based on the semiconductors with low commutation speed.

Several problems of high-speed commutation can be indicated in the literature: high overvoltages and oscillations during the commutation due to the presence of stray inductance, influence on the isolation, the increased bearing currents in the electrical drives and additional problems of electromagnetic interference (EMI). The last problem can be crucial for the application of the new power switches because it can require the installation of additional filters. The additional EMI filters can lead to the decrease of the power density of the whole system including power converter itself and all passive components. This thesis discusses the problem of EMI generated by the inverter of an electrical drive in the transportation systems. The work considers the aerospace application, where power density plays the most important role, but the requirements for the EMI are very strict. The nature of the conducted noise in the AC drives is considered in the details. The thesis presents also the various methods applied for the reduction of emissions generated by the power converter. The research work considers the application of conventional EMI filters and different inverter design techniques (topology, modulation techniques and hardware).

This research was carried out to build an approach for including the high-frequency EMI effects in the design stage of the inverter utilizing the appropriate simulation. Whereas the most existing research works are concentrated on the EMI filter design and its optimization, this work presents a new frequency domain model, which is capable to consider different noise reduction techniques in the AC drive including the EMI filters and the inverter design methods. Moreover, the most existing models do not take coupling between common mode and differential mode into account. However, it is shown theoreti-

cally and experimentally, that the mixed-mode (MM) noise can be observed in the system where EMI is measured according to the aerospace standards. The proposed frequency domain models can be used to analyse the MM noise. The model keeps the simple frequency domain behaviour with low computational effort that makes it suitable for the application in the optimization procedure.

The prototype of an inverter based on SiC metal-oxide-semiconductor field-effect transistors (MOSFET) was built within the research work to implement the AC drive system for the EMI measurements. It is used to conduct the experimental investigation of different noise reduction techniques as well as to validate the developed model. The results show that the EMI in the AC drives has a very complex nature. The particular noise reduction techniques are efficient only under the certain conditions. The proposed model can be used to analyse these conditions.

Kurzfassung

Eines der Hauptziele der modernen Leistungselektronik ist die Erhöhung der Leistungsdichte. Dieser Trend wird vor allem durch die Elektrifizierung im Verkehr (Elektro- / Hybridfahrzeuge und Flugzeuge) ausgelöst. Die Erhöhung der Leistungsdichte sollte die anderen Parameter der Leistungswandler sowie Kosten und Komplexitätsgrad auf einem angemessenen Niveau anhalten. Darüber hinaus sollten alle Umgebungsbedingungen hinsichtlich der Anwendung erfüllt sein. Die Wandler wurden seit der Erfindung der IGBTs bezüglich der Topologie und Steuerung verbessert. Die Entwicklung und die Lieferung der neuen Leistungsschalter an den Markt haben jedoch in den letzten zehn Jahren die größte Aufmerksamkeit der Ingenieure auf sich gezogen. Solche Halbleitermaterialien sowie SiC und GaN haben eine neue Klasse von Leistungsschaltern mit reduzierten Schalt- und Durchlassverlusten gegründet. Auf den ersten Blick scheint es möglich zu sein, die vorhandenen Stromrichter durch die Ersetzung der konventionellen Si-Leistungsschalter zu verbessern. Es wird oft angenommen, dass solcher Ansatz die Maße des Kühlsystems und/oder die Maße der passiven Komponenten verringert. Geringe Schaltverluste sind jedoch auch mit kurzen Kommutierungszeiten (Anstiegs- und Abfallzeiten von Spannungen und Strömen) und mit einer hohen Spannungsanstiegsrate ($\frac{du}{dt}$) verknüpft. Die erhöhte Schaltfrequenz und die hohen Werte von $\frac{du}{dt}$ führen zu neuen Einschränkungen bei der Konstruktion von Stromrichtern, die in der Leistungselektronik auf der Basis von Halbleitern mit niedriger Kommutierungsgeschwindigkeit unterschätzt oder vernachlässigt wurden.

In der Literatur wurden mehrere Probleme der Hochgeschwindigkeitskommutierung aufgezeigt: hohe Überspannungen und Schwingungen während der Kommutierung wegen der Streuinduktivität, Einfluss auf die Isolation, Lagerströme und Probleme der elektromagnetischen Verträglichkeit (EMV). Das letzte Problem kann für die Anwendung der neuen Leistungshalbleiter die entscheidende Bedeutung sein, weil die zusätzlichen Filter installiert werden sollen. Die EMV-Filter können dazu führen, dass die Leistungsdichte des gesamten Systems sich einschließlich des Stromrichters und aller passiven Komponenten verringert. Diese Arbeit beschäftigt sich mit dem Problem der elektromagnetischen Störungen, die durch den Wechselrichterbetrieb eines elektrischen Antriebs in Transportsystemen erzeugt werden. Die Arbeit berücksichtigt die Luftfahrtanwendung. Bei dieser Anwendung spielt die Leistungsdichte die wichtigste Rolle. Aber die EMV-Anforderungen sind sehr streng. Die Art des Rauschens ist detailliert berücksichtigt. In der Arbeit werden auch die verschiedenen Methoden zur Reduzierung der Emissionen vorgestellt. Die Forschungsarbeit befasst sich sowohl mit der Anwendung konventioneller EMV-Filter als auch mit verschiedenen Techniken, die auf das Design des Inverters bezogen (Topologien, Modulationsarten und Hardware).

Das Ziel der Forschungsarbeit ist die Entwicklung der Methoden für die Berücksichtigung der hochfrequenten EMV-Effekte während der Entwurfsphase des Wechselrichters. Dafür sollte die entsprechende Simulation erstellt werden. Die aktuellen Forschungsarbeiten konzentrieren sich auf die Modelle für das EMV-Filterdesign und dessen Optimierung. Im Gegensatz stellt diese Arbeit ein neues Frequenzbereichsmodell, das die verschiedenen Entstörungsmethoden einschließlich der EMV-Filter und der Wech-

selrichterdesignmethoden berücksichtigt. Darüber hinaus betrachten die meisten vorhandenen Modelle keine Umwandlung zwischen Gleichtakt und Gegentakt. Es wird jedoch theoretisch und experimentell festgestellt, dass die Umwandlung in dem System beobachtet werden kann. Das entwickelte Frequenzbereichsmodell kann verwendet werden, um diese Umwandlung zu analysieren. Das Modell behält das einfache Frequenzbereichsverhalten mit geringem Rechenaufwand bei, sodass es für die Anwendung im Optimierungsverfahren geeignet ist.

Der Prototyp eines Wechselrichters auf Basis von SiC-MOSFET wurde im Rahmen der Forschungsarbeiten entwickelt, um den elektrischen Antrieb für die EMV-Messungen zu implementieren. Es dient zur experimentellen Untersuchung verschiedener Entstörungsmethoden sowie zur Validierung des entwickelten Modells. Die Ergebnisse zeigen, dass die EMV in den Frequenzumrichtern sehr komplex ist. Die speziellen Entstörungsmethoden sind nur unter bestimmten Bedingungen wirksam. Das vorgeschlagene Modell kann verwendet werden, um die Bedingungen zu analysieren.

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Motivation

Stanislav Lem, one of the greatest science fiction writer and philosopher, made a parallel in his book "*Summa Technologiae*" between biological and technological evolutions. Similar as huge creatures such as dinosaurs were pushed out by the small mammals and particular by the humans, the huge steam machines invented at the beginning of the 18^{th} century were replaced by the combustion engines putting the steam technology on the shelves of museums. This process goes further and we can see how electric motors are making the same steps. It is well known that during thousands of years different kinds of mammals were obtaining various characteristics occupying larger areas. And nowadays, it can be also observed how the electrical drives are finding more and more applications in the last 100 years. The most recent example is transportation such as electric vehicles and aircraft. The last one is mirrored in the concepts of More Electric Aircraft (MEA) and All Electric Aircraft (AEA). These concepts are assuming that all classical hydraulic and pneumatic drives will be replaced by the electrical alternatives in the modern aircraft [1, 2].

The power electronics become a key technology in the further development of electrified transport. The modern electrical drives cannot be imagined without a power converter [3]. It is interesting that the power electronics itself is also developing further with more efficient and compact converters. A good example here is a "*Google Little Box Challenge*" which was held during conduction of this research. Its goal was to push the power density of a solar converter to the limit [4]. The results of this competition are very impressive for the actual state of technology. The values of efficiency and power density equal to 98% and $1000\,\mathrm{W\,cm^{-3}}$ respectively were achieved during the competition [5]. Looking on the results, it can be seen that all best competitors were using the wide bandgap devices (WBG) with increased switching frequency. This shows us the future trend in the power electronics: the compact and efficient converters based on SiC and GaN power semiconductors will replace converters based on the Si power switches, especially in transportation applications where power density plays the biggest role [6].

However, application of power converters based on WBG semiconductors has some challenges regarding its integration [7, 8]. One problem is electromagnetic compatibility (EMC) of power converters because they produce the electromagnetic (EM) noise due to the switched operation. The problem of EMI increases with the increased switching frequency and decreased commutation times of WBG devices. The EMC is very critical parameter for transportation systems. This can slow down the development of new power converters in this field. The classical approach to reduce the EM noise is to use the EMI filters [9]. But it leads to the power density decrease of a converter reducing the profit given by the WBG power switches. A lot of research work was conducted in recent years to overcome the problem of increased EMI and decreased power density of power converters. Most of the works are dedicated to the optimization of EMI filters [10, 11, 12, 13].

At the same time, EMC of the electrical drive can be also improved by the appropriative design of the power converter. However, it is hard to find the works where all design techniques for EM noise reduction are summarized and investigated. The impact of converter design on its EMI behaviour is considered

in many publications but only for the particular techniques: topologies [14, 15], modulation techniques [16, 17], switching behaviour with layout parasitics [18, 19, 20] and gate drivers design [21]. A volume optimization of a converter with power factor correction (PFC) including EMI was considered in [22]. However, EMI of the converter was considered only for the lower frequency range.

This work is aimed to structure all methods of EM noise reduction generated by the power converter. The work is concentrated on the inverter of an electrical drive applied in the aircraft. The goal of this research is also to provide the model which is capable to predict the EMI of a power converter under different conditions and to take various EM noise reduction techniques into account. The work should also provide a link between EMI behaviour and efficiency of a power converter in order to use it further for power density optimization. Assuming that converter design and optimization is a very time critical procedure, the model should provide low computational effort.

1 EMI in Aircraft AC Drives

The EM noise can be divided according to the way of its transmission [23]. The 1st group of EM noise is defined with electrical quantities, voltage and current, and described the propagation of electromagnetic fields guided by the conducting structures. This type of emission is called conducted EMI. This type of noise can propagate through the power supply to the other loads causing EMC issues. The 2nd group called radiated EMI is associated with EM fields which are propagating away from the electric device. These two groups are closely related as EM fields are produced by the flowing currents and applied voltages. The radiated EMI is associated with the radio-frequency (RF) currents, which can circulate in the loops formed by the conducting structures such as cables and traces of printed circuit board (PCB). This research work is dedicated to the 1st group, namely to the conducted EMI.

Interpretation of EMI measurements depends greatly on the applied standard [23]. As the aerospace industry is considered in this work as an example of a transportation system, this chapter presents the corresponding standard for the civil aviation industry in details. Then, the nature of conducted EMI noise generated by the inverter in the AC drive is also explained. The 2nd part of this chapter provides an overview of existing conducted EMI reduction and mitigation techniques. The work considers the conventional approach (passive EMI filters) as well as methods which are related to the design of the power converter itself.

1.1 EMI Standard Description

An applied standard should describe all aspects of EMI evaluation: settings of measurement devices, installation rules, frequency ranges, amount of tests, maximum levels and etc [23]. For the civil aviation industry, the main environmental standard is DO-160 which is published by the Radio Technical Commission for Aeronautics (RTCA). Section 21 of DO-160 describes the test procedure for the measurements of emissions (conducted and radiated) generated by the airborne equipment [24]. The measurements and simulation in the current research work are conducted in accordance with this standard.

Before the conducted emissions can be measured, the equipment under test (EUT) should be assembled appropriately. This procedure is obligatory in order to ensure the repeatability of the tests. An assembly for the measurement of conducted emission is shown in Figure 1.1. It is recommended to place the whole setup in a shielded enclosure, but this statement is not mandatory. Firstly, it is necessary to put all relevant parts of the system above a metallic (conducting) plate of a defined thickness (>0.5 mm for copper).

The cable between the power supply and the EUT is called the power line. In order to decouple the power supply from the measurement setup, it is required to install Y-capacitors of $10\,\mu$F together with the line impedance stabilization network (LISN) at the beginning of the power line. LISN provides the defined value of impedance of the power line for test repeatability [23]. According to DO-160, the feed-through technology should be applied for the input Y-capacitors. The impedance of LISN according to

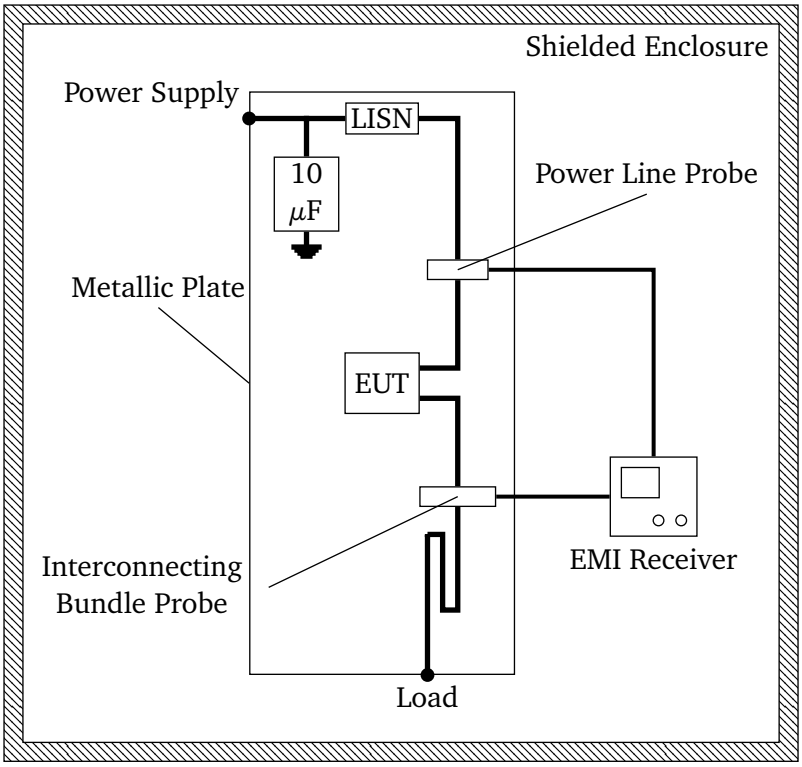


Figure 1.1.: The top view of an assembly for conducted emission measurements according to DO-160.

DO-160 is shown in Figure 1.2. As can be seen, the LISN sets the value of impedance equal to 50 Ω with a certain accuracy after the frequency of 1 MHz. A resonance can be also observed in the LISN impedance at the frequency equal to 20 kHz .

The circuit realisation of the considered LISN is shown in Figure 1.3. It contains already the decoupling input Y-capacitor of 10 μF. It can be also observed that the 50 Ω resistor provides a matched termination for the measurement equipment. However, this terminal is normally used only for evaluation purposes. The conducted noise observed at the LISN is not required for the compliance of EUT according to DO-160.

At the output, the EUT is connected with a specified load in Figure 1.1. The connection between the load and EUT is the interconnecting cable bundle. All parameters (length, type, amount of phase, etc.) of power line cables as well as of interconnecting bundles are defined by the equipment specification.

For the certification according to DO-160, the conducted noise is measured using RF current probes. According to Figure 1.1, the probes are placed at the input and output bundles. The harmonics above 150 kHz of these currents are defined as conducted emissions according to DO-160 [24]. However, it is very important to mention, that at the interconnecting bundle, the noise is measured on the whole bundle, whereas for the power lines the currents should be measured on each line. This statement defines the type of noise, which will be observed during the measurements (see Section 1.3).

The measured currents are sent to the EMI receiver or spectrum analyser (see Figure 1.1). These devices represent the measured signal directly in the frequency domain. They are based on the principles of the superheterodyne receiver [23]. The levels of signal (noise) observed on the screen of the measurement device depenend also on parameters of the receiver [25, 26]. Therefore, it is necessary to consider these parameters during the EMI analysis. The parameters of the EMI receiver (spectrum analyser) are

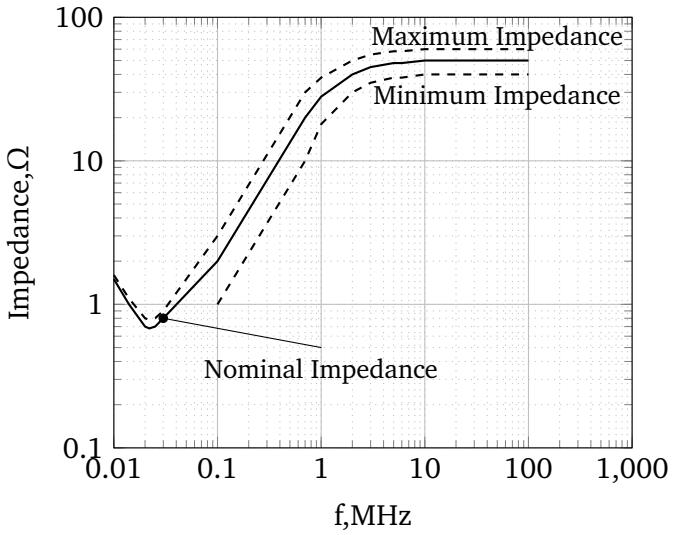


Figure 1.2.: The requirements for LISN impedance according to DO-160.

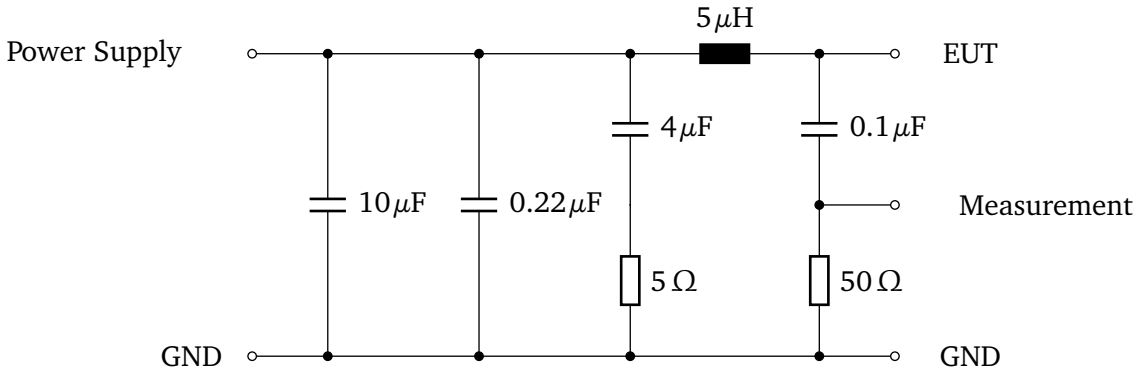


Figure 1.3.: The schematic of circuit corresponding to the applied LISN.

also given in DO-160 section 21 [24]. The most relevant parameters of the EMI receiver given in DO-160 are analysed and given below as:

Frequency range: The limits for conducted noise is defined for frequencies from 150 kHz up to 152 MHz in DO-160. The impact of the frequency range is obvious. It requires, that all measurement devices (EMI receiver and probe) should operate at least in this range. According to section 21 of DO-160, the whole frequency range for conducted and radiated emissions is divided into several subranges with slightly different parameters of EMI receiver. The frequency range of conducted emissions is presented by 2 subranges: from 150 kHz up to 30 MHz and from 30 MHz up to 152 MHz [24]. The main difference between two subranges is the value of resolution bandwidth (RBW). The value of RBW impacts the noise level as it is mentioned below. This work is concentrated on the 1st frequency subrange to avoid the inconvenience in the interpretation of the simulation and measurement results.

Resolution bandwidth: The value of RBW corresponds to the width of the filter applied in a heterodyne receiver [25]. Its value defines the amount of energy which is acquired for each frequency step.

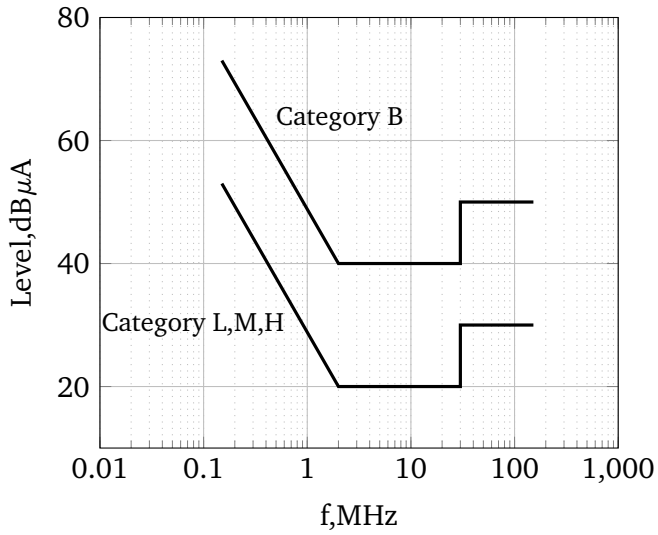


Figure 1.4.: Limits for conducted emission according to DO-160.

Higher values of RBW are leading to an increased noise floor and increased levels of wideband signals [26]. Typically, RBW in EMC applications is defined according to the level of −6 dB [23]. In DO-160 for the frequencies from 150 kHz to 30 MHz, the value of RBW is equal to 1 kHz, whereas the value of RBW is equal to 10 kHz for RF range (up to 400 MHz) [24].

Dwell time: This value corresponds to the time duration during which the spectrum analyser accumulate energy for the single frequency step. In DO-160 the minimum dwell time is 1.5 ms. However, the dwell time is not limited and should be even increased if higher emissions are expected with longer times [24].

Detector type: The amplitude of measured signals is usually changing (fluctuating) within the dwell time. The detector defines which value is taken and visualized on the screen of the spectrum analyser. There are three types of detectors which are normally integrated into the EMI receivers: average, peak and quasi-peak [23]. The average detector takes the average value of the signal during the dwell time. The peak detector takes the maximum value. The quasi-peak detector consider also the duration between the maximum and minimum values using different charging and discharging constants [23]. The DO-160 recommends the application of the peak type detectors.

The resulting values observed on the screen of an EMI receiver should be compared with an appropriate limit. There are several categories (L, M, H and B) which define the limit according to section 21 of DO-160 [24]. The category of the measured signal is chosen according location of measurement point towards life important equipment. The limits for the corresponding categories of DO-160 are shown in Figure 1.4. The category B assumes that the noise is measured far away from any antenna in the aircraft. In order to pass the EMI tests, the measured noise level should be lower than the corresponding limit on the whole frequency range.

The DO-160 contains more particular information about the assembly, measurement procedure and documentation. For example, all cables and EUT should maintain a distance of 10 cm above the metallic

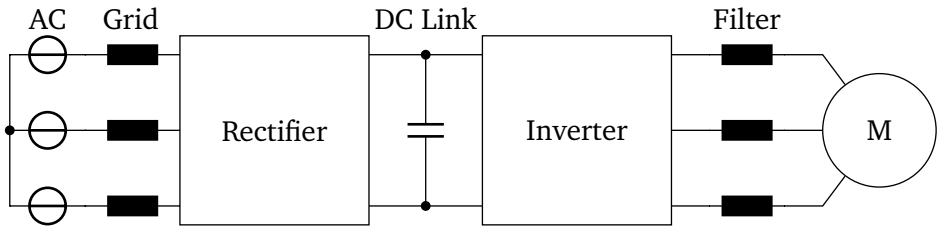


Figure 1.5.: The simplified structure of a typical AC drive.

plate. The same distance should be kept between edges of the metallic plate and all components. However, the most relevant information about DO-160 section 21 is discussed in this section. The presented information is essential for the analysis of noise generated by the AC drives as well as for the further measurements and simulation.

1.2 Generation of Conducted Noise in AC drives

In order to understand the nature of conducted noise in modern AC drives, it is required to discuss their basic operation principles. The simplified structure of the typical variable frequency drive or AC drive is shown in Figure 1.5. The rectifier supplies the DC link voltage from the AC grid. Using the pulse width modulation (PWM) operation of inverter, it is possible to provide AC voltage/current with adjustable amplitude, phase and frequency at the input of a motor. Therefore, simple, cheap and robust AC induction machines can be used in the AC drives [3]. The structure of an AC drive presented in Figure 1.5 is based on the voltage source converter (VSC). Such type of AC drive is the most widely used in the middle power range [27].

With invention of IGBT in '80s, a new era began in the history of electrical drives. Due to their properties, IGBTs can be used to design the high-efficiency PWM inverters for medium and high power applications. Since then, the AC drives were developing very fast. Nowadays, electrical drives based on PWM converters are the most common type of drives applied in the industry [27]. However, the AC drives based on Si IGBT are reaching its limitation regarding the efficiency and power density [6]. In the last decade, the new WBG materials were developed and appeared on the market. Due to the properties of such materials, it becomes possible to build unipolar power switches (Schottky diodes and MOSFETs) with higher blocking voltage [8]. The unipolar power semiconductors have certain advantages in comparison to bipolar devices [7]. One of the most important is improved switching characteristics that allows the design of PWM converters with a high switching frequency. At the current state of technology, the SiC devices are the most promising technology for the aerospace industry. Many researchers and companies are proposing the converters based on these power switches [28, 29]. Therefore, this work considers the AC drive with a VSC based on SiC MOSFETs and Schottky diodes.

For industry applications, it is necessary to obtain the DC voltage out of AC supplied from the grid (see Figure 1.5). However, due to widespread of modern AC drives and other loads based on power electronics together with an increase of renewable power sources, it is proposed to make DC electrical power systems for the local distribution grids [30]. Due to the increasing amount of power electronics by the AEA and MEA concepts, the same idea of common DC supply is also proposed for the future electrical

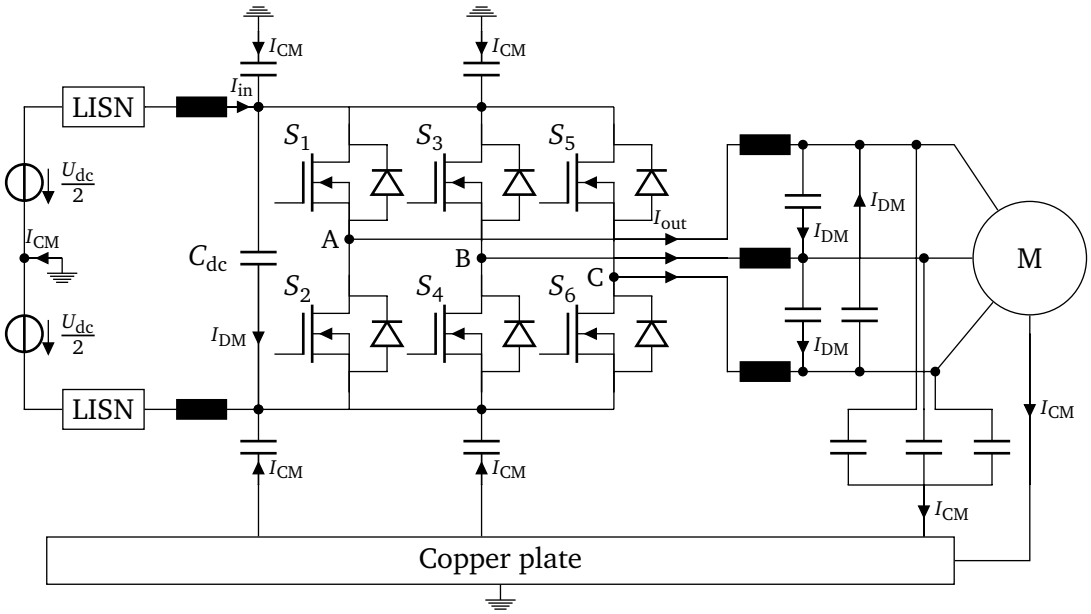


Figure 1.6.: Structure of the AC drive in accordance to DO-160 conducted EMI measurements.

power systems of an aircraft [31]. In that case, there is no need for a rectifier. The inverter is supplied directly from the DC source. For the high power loads in the future aircraft, it is assumed to use bipolar DC supply with voltage $U_{dc} = 540\,V$ [32, 2]. This kind of electrical power system is considered in the research work. The noise generated by the rectifier is therefore ignored.

Section 21 of DO-160, which defines the conducted emissions for the airborne equipment, is described in the previous section. In order to understand how the conducted noise is generated by the VSC, the AC drive system must be represented in accordance with the DO-160 assembly for the conducted EMI measurements (see Figure 1.1). The respective arrangement of the studied system is shown in Figure 1.6. The whole AC drive is supplied from the bipolar DC power supply. The input DC voltage is converted to AC by means of the PWM inverter. For simplicity, a full-bridge (FB) 2-level VSC is considered in Figure 1.6. The power line is a two-phase DC cable which connects the converter to the power supply through the LISN. The VSC corresponds to the EUT in this sense. The LISN includes already the $10\,\mu F$ decoupling Y-capacitors. The motor is assumed to be the specified load. Therefore, the three-phase cable in between is an interconnecting bundle. According to DO-160 section 21, the conducted noise is measured on all bundles with RF current probes [24]. The respective currents are also shown in Figure 1.6: input current I_{in} and output current I_{out}.

All components (cables, LISN and VSC) of the system are located above the copper plate which serves as a common ground path. Due to wide frequency range of consideration (up to 30 MHz), huge amount of stray parameters should be taken into account. As can be seen in Figure 1.6, all conductive parts of the system have stray inductances. The stray capacitance between phases can be observed in Figure 1.6. Due to safety reasons, all conductive non-electrical parts of the system should be grounded [33]. These parts are heatsinks, cable shields and motor housing. Therefore, additional stray capacitances between phases and ground can be also observed in Figure 1.6. The presented stray capacitances provide a low impedance path for the high-frequency currents.

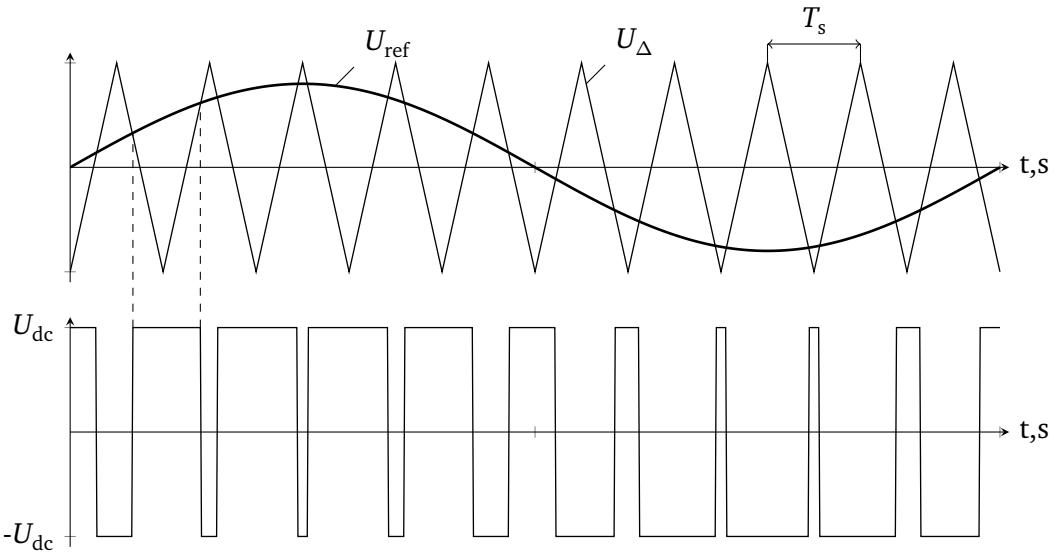


Figure 1.7.: The principle of SPWM.

The RF currents are observed during the operation of the AC drive due to the switching nature of the PWM voltage at the output of the inverter. In order to understand the principles of PWM, the simple sinusoidal PWM (SPWM) can be considered [34]. The idea of SPWM is explained in Figure 1.7 on example for the voltage modulation in one phase of VSC. The reference output voltage U_{ref} calculated by the control system of an AC drive is compared with a carrier signal U_Δ which has a triangle shape. Then the reference voltage is higher than a triangle signal, the high side switch S_1 is turned on. In order to avoid a short circuit, the low side S_2 switch is turned off (phase A in Figure 1.6). In that case, the output phase voltage will be connected to the positive rail of DC supply with a voltage $\frac{U_{dc}}{2} = 270\,\text{V}$. Otherwise, then the carrier signal is higher than the reference, the output voltage will be connected to the negative rail $-\frac{U_{dc}}{2} = -270\,\text{V}$ by turning S_1 off and S_2 on.

The sampling time is equal to the period of the carrier signal (T_s). The relationship (1.2) between amplitudes of reference and carrier signals is called modulation index m. As far as $U_{ref} \leq U_\Delta$ the fundamental component of the output pulsed voltage is linearly proportional to the reference signal [27].

$$m = \frac{\hat{U}_{ref}}{\hat{U}_\Delta} \tag{1.1}$$

Despite the fundamental components, the harmonics are also presented in the output voltage [27]. It is comfortable to consider two types of harmonics for the further analysis: low-frequency (LF) harmonics with frequencies lower than the sampling frequency (f_s) of VSC and high-frequency harmonics with frequencies above the sampling frequency. The amplitude of LF harmonics is mostly defined by the type of PWM [27]. With high values of f_s, the LF harmonics are very low in the input and output currents

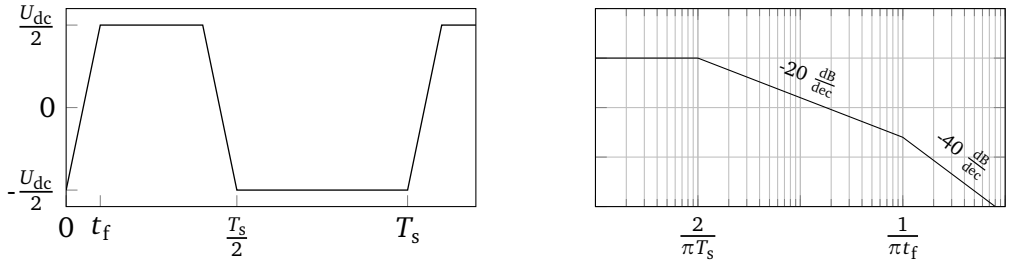


Figure 1.8.: Trapezoidal signal in time and frequency domains.

of VSC because the motor inductance acts as a simple low pass filter. For such frequencies, the parasitic capacitances are very low and can be neglected as well. However, the amplitude of the signal is very high at the frequency equal to the sampling frequency of PWM. Therefore, some currents can be observed at f_s in the output current. These currents are often called current ripples. The current ripples are associated with the corresponding DC link voltage ripples and with losses in the motor and VSC [35, 36].

The VSC output voltage on one sampling period can be replaced by the trapezoidal signal for the simplified RF representation. The period of this signal is defined by the sampling time of PWM (T_s). According to the principles of PWM (see Figure 1.7), the duty cycle of such a signal is varied during the fundamental period. The fall and rise edges of the pulses are defined by the switching characteristics of the power semiconductor. For simplicity, it can be assumed that the rise and fall times (t_f) are equal and much smaller than the period of the signal ($T_s >> t_s$). The duty cycle is also assumed to be fixed. The trapezoidal signal with its spectrum envelope is shown in Figure 1.8. As it can be observed, the magnitude of the signal falls with -20 dB per decade starting from the frequency $\omega_s = \frac{2}{\pi T_s}$. From the point where the frequency is equal to $\frac{1}{\pi t_f}$, the magnitude of the trapezoidal signal starts to decrease with -40 dB per decade.

As can be seen in Figure 1.8, the magnitudes of RF harmonics decreases. However, the stray capacitances, which can be observed in Figure 1.6, provide a low impedance path for these harmonics of VSC output voltage. The currents, which are defined as a conducted emissions according to DO-160 (see Figure 1.4), are in the range of μA. Therefore, the relatively low values of RF currents can be higher than the applied limit for the conducted EMI.

From the other side, the sampling frequency of modern PWM converters is also increasing due to the development of new WBG power semiconductors. The SiC MOSFETs are capable to switch with rise/fall times in the range of couple ns with a very low switching losses allowing the increase of the switching frequency up to the hundreds of kHz. Increased switching frequency provides the possibility to reduce the size of passive components [37]. But according to the spectrum envelope of trapezoidal signal in Figure 1.8, more energy is shifted towards RF range with the increased sampling frequency of PWM and decreased commutation times of the power switches.

The nature of conducted emission generated by the AC drive is explained in this section. Using simple trapezoidal representation of inverter PWM output voltage, it is shown that relatively high currents in RF range can occur due to the presence of stray parameters in the components of the typical electrical drive. More detailed information about conducted noise in the AC drives is given in the next section.

1.3 Common Mode and Differential Mode Noise

The RF currents are flowing through the parasitic elements during operation of an AC drive. As it is shown in Figure 1.6, some currents circulate between the phases, whereas the other currents flow through the parasitic elements to the ground. It makes sense to consider these currents separately as differential mode (DM) and common mode (CM) noise respectively [23]. However, from the EMI point of view, the AC drive system has some special features in comparison to the other electrical devices. The amount of phases at the input and output is different in the conventional AC drive. The VSC is a non-linear device, that introduces some problems in the analysis as well. In [38], the CM and DM conducted emissions in a variable frequency drive (AC drive) are analysed in details. In this section, the information about CM and DM noise in AC drives is summarized and structured according to its further application in the research work. This section introduces also the MM noise which occurs due to the coupling between DM and CM.

1.3.1 DC Side

The DC side with bipolar power supply can be treated as a simple differential line. The phase currents in such a line can be represented using CM and DM as it is shown in Figure 1.9. The CM current flows in one direction through the line wires and back through the common ground. Whereas DM currents circulate between two lines. The operating (useful) signal is normally observed only in DM. However, the frequency of the operating signal (fundamental frequency) is much lower than the frequency of emissions (above the sampling frequency of PWM). In case of an AC drive, the operating signal at the input of VSC is just a DC.

The CM and DM currents can be generated only by the respective voltages in the symmetrical systems. The mode currents and voltages can be found using (1.2) and (1.3) respectively using the single-ended quantities. These equations can be applied to the currents and voltages at the DC side of a considered AC drive system (see Figure 1.6).

$$\begin{aligned} I_{\mathrm{CM}} &= I_1 + I_2 \\ I_{\mathrm{DM}} &= \frac{I_1 - I_2}{2} \end{aligned} \tag{1.2}$$

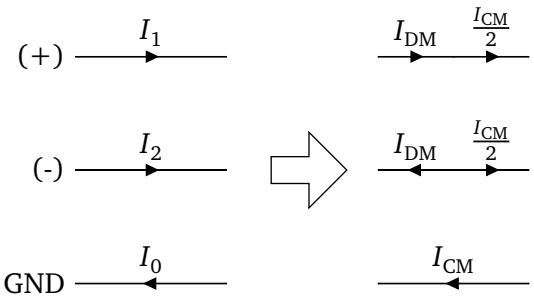


Figure 1.9.: CM and DM representation of the differential line.

$$U_{\mathrm{CM}} = \frac{U_1 + U_2}{2}$$
$$U_{\mathrm{DM}} = U_1 - U_2 \tag{1.3}$$

However, the conducted noise at the DC input cannot be considered separately from the output noise of VSC. This is due to the fact that PWM voltage is observed at the output of VSC. The components of both sides (AC and DC) of the considered electrical drive contribute to the propagation path for high-frequency current. The currents flow to the load (motor) and back to the inverter through the DC side [38]. It is not possible to decompose the AC side currents in a similar way as for the DC side because the three-phase output of VSC cannot be treated as a simple differential line.

1.3.2 AC Side

The DM and CM representation of a three-phase side of an AC drive was proposed in [39, 40]. Similar as for the DC side, the AC side CM current is a part of the phase current which flows in the same direction in all phases. Therefore, the CM current can be found using (1.4):

$$I_{\mathrm{CM}} = I_{\mathrm{a}} + I_{\mathrm{b}} + I_{\mathrm{c}} \tag{1.4}$$

Following the logic of the mode representation applied to the DC side, the current in one phase consists of CM and DM. The DM part for phase A can be found by subtracting the CM part from the phase current leading to:

$$I_{\mathrm{DM}} = I_{\mathrm{a}} - \frac{I_{\mathrm{CM}}}{3} \tag{1.5}$$

Replacing the CM current in (1.5) by (1.4), it is possible to obtain the equation for the 1$^{\mathrm{st}}$ differential mode (DM_1) at the AC side (1.6). In order to find the 2$^{\mathrm{nd}}$ part of DM current (DM_2) at the AC side, it is required to make an assumption, that two DM currents are flowing through one phase. The corresponding transformation is shown in Figure 1.10, where DM_1 and DM_2 flow through phase B in different directions. The current I_{DM_2} can be then found by subtracting I_{CM} and adding I_{DM1} current to phase A that leads to (1.7).

$$I_{\mathrm{DM}_1} = \frac{2I_{\mathrm{a}} - I_{\mathrm{b}} - I_{\mathrm{c}}}{3} \tag{1.6}$$
$$I_{\mathrm{DM}_2} = \frac{I_{\mathrm{a}} + I_{\mathrm{b}} - 2I_{\mathrm{c}}}{3} \tag{1.7}$$

The corresponding CM and DM voltages for the three-phase side of an AC drive can be found using (1.8)..(1.10). As can be seen, the DM_1 and DM_2 voltages are simple line-to-line voltages.

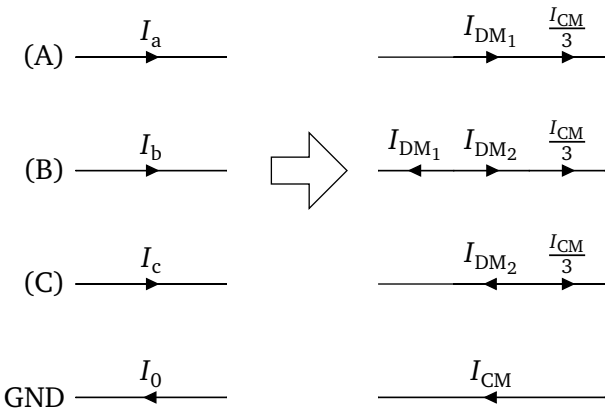


Figure 1.10.: CM and DM representation of currents for the three-phase line.

$$U_{CM} = \frac{U_a + U_b + U_c}{3} \tag{1.8}$$

$$U_{DM1} = U_a - U_b \tag{1.9}$$

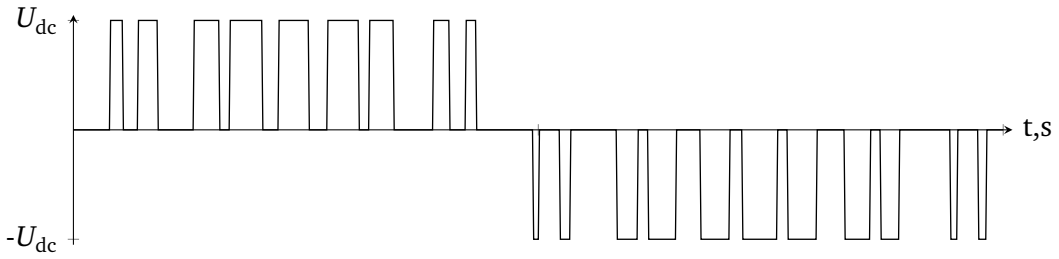
$$U_{DM2} = U_b - U_c \tag{1.10}$$

The proposed decomposition of DM voltages and currents of the three-phase system is not unique. In Figure 1.10, it is assumed that phase B is a reference phase for the DM currents. Similar assumption can be applied to any other phase leading to slightly different decompositions of the three-phase currents. Moreover, the proposed decomposition of the three-phase currents/voltages can cause some inconvenience to the readers who are more familiar either with classical $\alpha\beta\gamma$-transformation [34] or with symmetric components [41]. The 1st transformation is often applied for the control of VSC in AC drives and grid applications. The symmetric components are often used for the analysis of asymmetric three-phase systems. However, the benefits of proposed CM and DM transformation for the EMI analysis of three-phase AC drives are explained in Appendix A. It is shown, that decomposition with CM, DM_1 and DM_2 provides the direct connection between output and input mode currents of VSC.

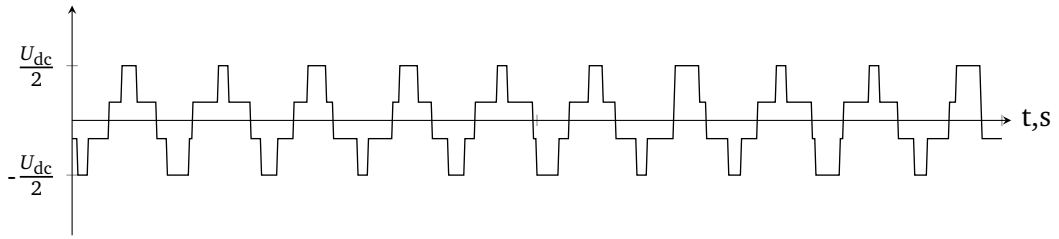
1.3.3 DM and CM Voltage at the Output of VSC

As it is shown in Section 1.2, the RF currents are generated in the AC drives due to the switching nature of VSC. Using PWM, the required voltages are generated at the output phases: A, B and C. The PWM voltage at phase A is also presented in Figure 1.7 in case of SPWM. The voltages at phases B and C can be found in a similar way. During normal operation of PWM inverter, the reference signals for the output voltages B and C have a phase shift of $-120°$ and $120°$ respectively. Using (1.8)..(1.10), the output DM and CM voltages can be found for SPWM operation of VSC. The resulting mode voltages at the output of VSC under SPWM operation are shown in Figure 1.11.

The DM_1 voltage in Figure 1.11a is an output line-to-line voltage between phase A and B (U_{ab}). This voltage contains the useful fundamental part which is proportional to the reference signal. The DM_2



(a) DM voltage (U_{ab})



(b) CM voltage

Figure 1.11.: DM and CM voltages at the output of VSC under SPWM.

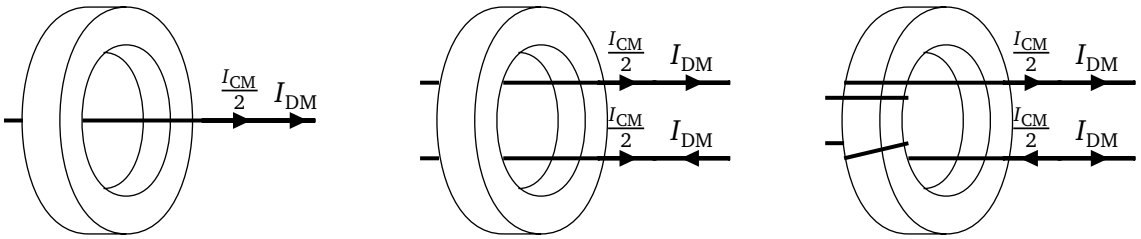
voltage has the same shape as in Figure 1.11a but with $-120°$ phase shift. The DM voltages at the output of VSC are switched between 3 levels: 0, U_{dc} and $-U_{dc}$. The spectrum envelope of output DM voltage can be represented by the trapezoidal signal as in Figure 1.8.

The corresponding CM voltage is shown in Figure 1.11b. In comparison to DM the output CM voltage is switched between 4 levels:$\pm\frac{U_{dc}}{2}$ and $\pm\frac{U_{dc}}{6}$. The trapezoidal signal can be also used to describe the spectrum envelope of the output CM voltage for the initial analysis [42]. A more detailed analysis of the voltage spectrum for VSC is given in Section 2.4.

The spectrum envelope of the trapezoidal signal (see Figure 1.8) shows that the harmonics of DM and CM voltages can be observed in the wide frequency range above the sampling frequency. The parasitics in the AC drive are also presented in both modes (DM - between phase, CM - between phase and ground, see Figure 1.6). Therefore, both types of conducted emissions can be observed during operation of the AC drive. The trapezoidal representation explains the impact of PWM sampling time and commutation times of power switches on the resulting amount of emissions. Increase of the sampling frequency and decrease of the commutation times lead to increased levels of conducted EMI.

1.3.4 Conducted Noise Separation

As it was mentioned before, the CM noise is associated with currents which flow in the forward direction through the line wires and back through the common wire (ground). Whereas, the DM currents circulate only in the line wires. Despite that, sum of both currents is indicated as a conducted noise according to DO-160, it is very important to recognize which type of noise dominate during measurements, because propagation paths for each mode are different [38]. Different conducted noise reduction and elimination techniques influence mostly the particular mode (see Section 1.4) as well. Therefore, it is preferable to separate the measured conducted noise.



(a) Measurement of phase current **(b)** Measurement of CM current **(c)** Measurement of DM current

Figure 1.12.: Different configurations of current measurement probe.

The easiest way to separate the CM and DM mode noise is to use a current probe with different wire configurations. The different DC side wires configurations with the same current measurement probe are shown in Figure 1.12. If the probe is placed only on one phase as in Figure 1.12a, the sum of DM and CM currents will be observed as it equals to the phase current. In order to measure only the CM current, the probe should be placed on both line wires simultaneously like in Figure 1.12b. In that case, the DM current is compensated in the probe. The pure DM current can be obtained by wounding phases of a differential line in the opposite directions as it is shown in Figure 1.12c. Similar approach can be applied to the three-phase AC side of VSC [43].

This type of mode separation is preferred for the current work because the noise is also measured using RF current probes according to DO-160 [24]. For the voltage based EMI measurements, the so-called mode separators are usually applied to distinguish CM and DM [44]. As it is also mentioned in Section 1.1, the conducted emissions are measured on each phase of the power line as in Figure 1.12a and on the whole bundle similar as in Figure 1.12b for interconnecting cables. It means, that for AC drive shown in Figure 1.6, the sum of both modes is measured at the DC input of VSC. The DM current at the input is normally much lower than the CM because the DC link capacitors introduce the filtering effect for the DM currents [39]. The value of C_{dc} is much higher than the value of stray capacitors of the input cable. This assumption is also used during simulation of conducted EMI in AC drives (see Chapter 2). At the same time, the stray Y-capacitances of inverter and other components of the system have values almost in the same order. Therefore, part of CM current flows back through the LISN and input cable. This current is mostly observed during conducted EMI measurements at the input of EUT (VSC) according to DO-160.

The three-phase cable between the motor (load) and VSC (EUT) is treated as an interconnecting bundle according to DO-160. Therefore, only CM is measured at the AC side of the studied system. Summarizing all mentioned above, it can be concluded that the CM has a dominant influence on conducted EMI in AC drives. This corresponds to the conclusions made in [39].

1.3.5 Crosstalk Between CM and DM

It is possible to decompose the measured currents and voltages into CM and DM. Under ideal conditions, the CM and DM currents/voltages can be considered separately using the superposition principle. However, such an assumption cannot be used in real systems in all cases. Sometimes, the presence of CM currents/voltages can cause the DM noise and vice versa. Such type of noise is called further the MM noise in this work.

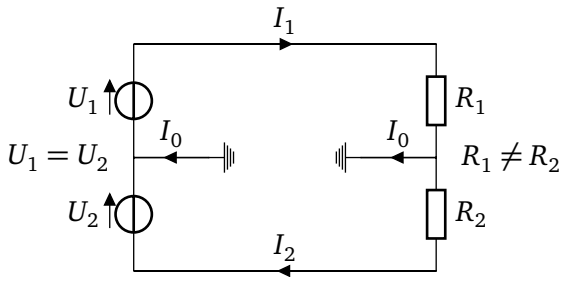


Figure 1.13.: Crosstalk between CM and DM due to unbalanced impedances.

The crosstalk between CM and DM can be easily caused by the presence of unbalanced impedances in the system as in the differential line shown in Figure 1.13. The CM voltage is equal to 0 according to (1.3) in case of balanced voltages U_1 and U_2 in Figure 1.13. However, some ground current I_0 can be observed in the differential line because load resistances R_1 and R_2 are not balanced. A similar effect can be observed in the three-phase AC side as well, where the unbalanced impedances are leading to the shift of neutral point [38].

This kind of coupling between CM and DM is well known. It is often observed in the differential lines, for example in the twisted pairs [45]. Normally, the impedances in AC drive system are designed to be balanced. However, in the RF range the slight differences can play a huge role and cause some noise transformation between DM and CM. For example, badly designed connectors with so-called "pig-tail" can be a reason for the MM noise [23].

The coupling between modes due to the small asymmetries is not the only kind of the MM noise in the AC drives. One type of coupling at the DC side is also observed due to the non-linear operation of an inverter. Such a type of MM noise was studied for DC-DC converters of switched mode power supplies in [46] and DC-fed motor drives in [47]. According to the analysis provided in Appendix A, some part of the CM current flows always through the DC link capacitors causing this natural coupling to the DM in the AC drives. However, the DC link capacitor should also act as a filter in this case.

1.4 Conducted Noise Reduction Techniques

The problem of conducted noise in the AC drives is discussed in the previous section. The respective EMI standard for civil aviation and the nature of the conducted noise in the AC drives are explained in details. The provided analysis based on the trapezoidal representation of PWM voltage shows that the problem of the conducted EMI increases in modern power electronics due to the increased switching frequency and application of WBG power switches. In order to comply with DO-160 requirements regarding the conducted emission, the respective high-frequency currents should be reduced both at the input and output of VSC. This section gives an overview of the existing approaches for the reduction of conducted noise generated in the AC drives. Firstly, the passive EMI filters are considered as a classical way to reduce the level of conducted emissions in any electrical device. Then, a group of EMI reduction techniques is presented which are related to the design of VSC. The benefits and drawbacks of all approaches are indicated as well as their limitations and relations to the performance (efficiency and power density) of the VSC.

1.4.1 EMI Filters

The most straightforward way to reduce the level of conducted noise in an electronic device is an application of EMI filters. The conventional EMI filters are constructed using basic passive components. This is a very simple but effective approach to reduce the conducted emission. In most cases, the operating signal and emissions are allocated far from each other in the frequency domain: the operating signal is in the low-frequency and noise is in the RF. Therefore, simple passive components can be used to implement the required low pass filter [9, 23]. These components should have an appropriate configuration which defines the resulting passband of the filter.

Any electrical system can be represented by the source of emissions and its receiver for the initial EMI analysis [9]. Both source and receiver have the corresponding impedances Z_s and Z_l respectively as it is shown in Figure 1.14. The EMI filter, which is placed between source and receiver, should reduce the voltage U_2 at the receiver side. It is common to use the insertion loss (IL) for the evaluation of EMI filter efficiency. The insertion loss of EMI filter can be found using (1.11) where the voltage U_2' is a voltage at the receiver without any EMI filter.

The insertion loss of the EMI filter depends on the values of the passive components, which are used to build the filter, and on the structure of the filter itself. However, impedances of the source and receiver play also a huge role. In [9], it was shown how to define the insertion loss of EMI filter using 2-port network parameters of EMI filter as well as the values of Z_s and Z_l. Based on these calculations, the basic recommendations upon the structure of a filter were given for the different impedances of source and receiver. These recommendations are summarized in Table 1.1.

$$IL = 20 \log \frac{U_2'}{U_2} \tag{1.11}$$

Using the superposition principle, similar initial analysis as in Figure 1.14 can be applied for DM and CM noise separately. Due to the different noise propagation paths, the values of Z_s and Z_l can differ for each mode. As it is mentioned in Section 1.3, the measured according to DO-160 noise in AC drives is mostly defined by the CM currents. The EMI filters can be built to damp the particular conducted noise (DM or CM) by the application of the corresponding components.

Such characteristics of EMI filters as insertion loss allows the comparison of different filters. However, it is not so easy to obtain real values of IL on the whole frequency range. The components applied in the EMI filters are also influenced by the parasitics. The impedances of the source and receiver change with the frequency increase influencing the value of insertion loss. Therefore, the real efficiency of the EMI

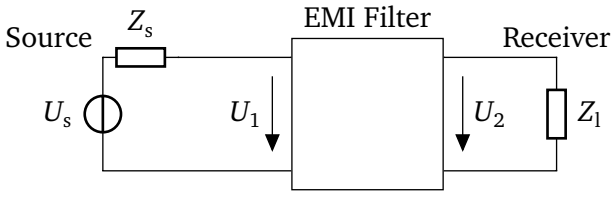
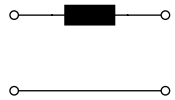
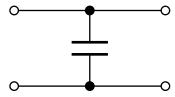
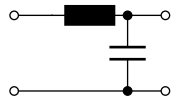
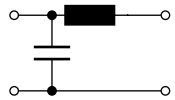
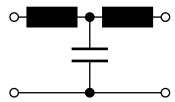
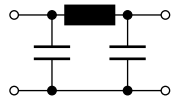


Figure 1.14.: Circuit for the simplified EMI analysis.

Table 1.1.: Recommendations for the selection of EMI filter structure.

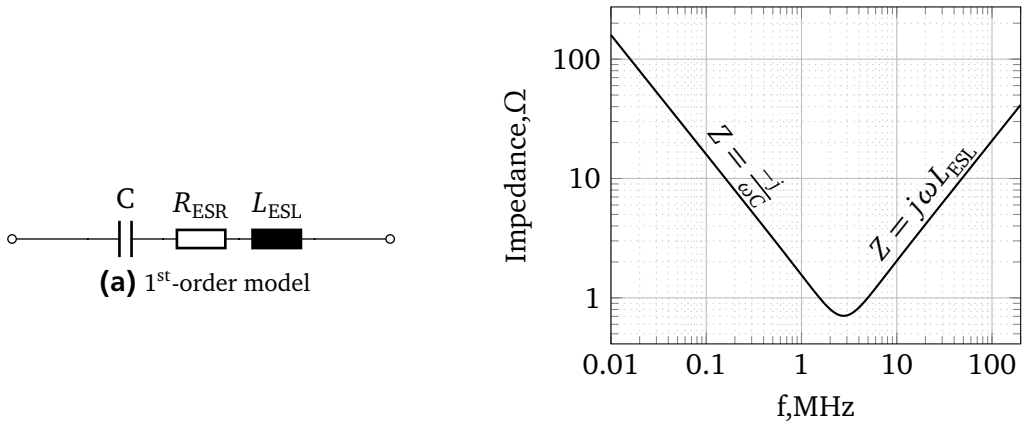
Source Impedance	Filter Structure	Receiver Impedance
Low		Low
High		High
Low		High
High		Low
Low, unknown		Low, unknown
High, unknown		High, unknown

filters is mostly evaluated experimentally using the "cut and try" method. Despite the stray parameters, there are also some other limitations applied to the EMI filter components such as current and voltage ratings. These limitations are also necessary to take into account during the design of the EMI filter. The components applied in the EMI filters are considered further in details.

Capacitors

The capacitors for EMI filters are firstly divided into 2 groups according to its connection. The capacitors, which are installed between power lines (phases), are called X-capacitors. The 2nd type is the Y-capacitors which are installed between the phase and common ground. The X-capacitors have an influence only on the DM noise, whereas Y-capacitors influence both CM and DM noise. The difference between these two types lies also in the safety requirements as the failure of Y-capacitors can cause safety problems including hazards to human beings [23].

Because EMI filters should not have any influence on the functionality of the system even in the case of failure, EMI capacitors fulfil the special requirements. Most of the capacitors considered for the EMI filter design are the metallised film capacitor with self-healing properties [48]. For the grid applications according to EN 123400, X- and Y-capacitors are divided into subclasses regarding the maximum breakdown voltage [44]. For the aircraft application, the capacitors should also have appropriate certification. The considered restrictions for capacitors have an influence on the dimension, price and maximum in-



(a) 1st-order model

(b) Impedance (C=33 nF, ESR=0.5 Ω, ESL=30 nH)

Figure 1.15.: Consideration of non-ideal parameters of a capacitor.

sertion loss of EMI filters. The following requirements for EMI filter capacitors are considered in this work:

- Only film capacitors can be applied for the design of EMI filters [48].
- From the practical experience in order to pass the DO-160 requirements for the lightning transients (DO-160 section 22.0 [49]), Y-capacitors should be avoided at the output of VSC.
- The sum of all Y-capacitors at the input of VSC should be less than 150 nF. Otherwise, the AC drive would not be able to pass the tests against lightning transients according to DO-160 [49],

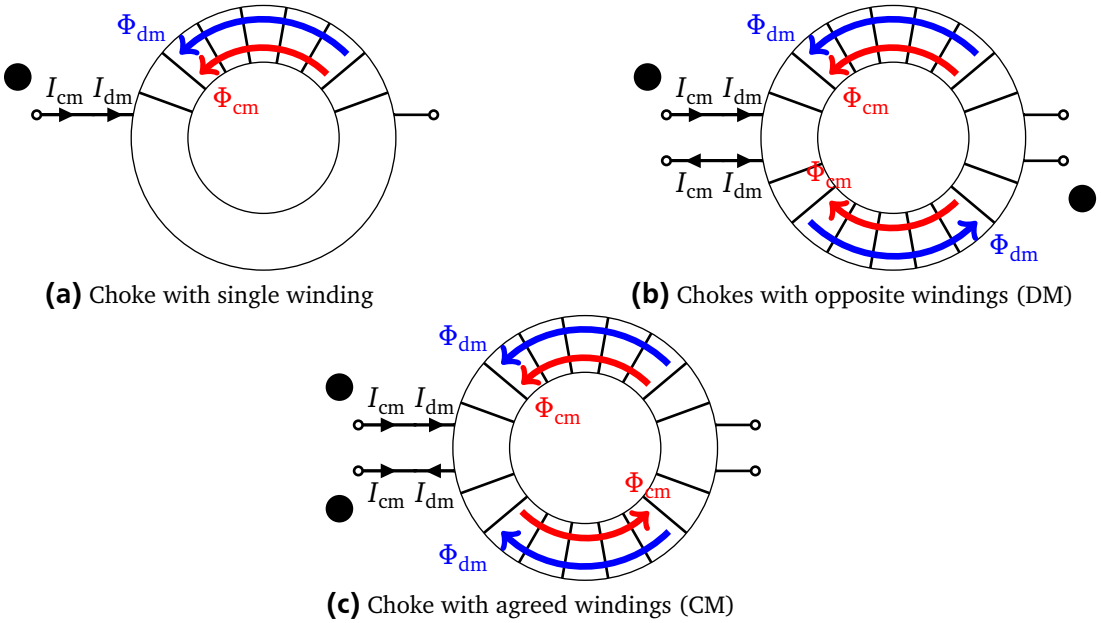
The impedance of an ideal capacitor is decreasing with the frequency increase with $\frac{-j}{\omega C}$. However, the real capacitors, which behaviour is explained in Figure 1.15, include some stray parameters. The 1st-order model of a capacitor shows that the impedance of the real capacitors is defined by the equivalent series resistance (ESR) and inductance (ESL in Figure 1.15a). The resulting impedance for a typical capacitor of 33 nF is shown in Figure 1.15b. As can be seen, the resonance is observed at the frequency of 3 MHz. After this frequency, the capacitor behaves like an inductor. For the considered frequency range (up to 30 MHz) such a capacitor applied in the EMI filter changes the behaviour of insertion loss and reduces the filtering efficiency.

In order to reduce the value of ESL, the lead-through capacitors were introduced for the EMI filters [23, 27]. The parasitic inductance can be also reduced in a bank of capacitors which can be chosen with smaller values of capacitance and maximum breakdown voltage. Because EMI filters are considered for the noise reduction in a wide frequency range, even small magnetic couplings define the value of ESL in the high-frequency range. A lot of attention should be paid to the layout of an EMI filter. As it was shown in [50, 51], even the placement of capacitors in the bank of capacitors influences the insertion loss of EMI filters in the RF range.

Another component, which is also widely used in passive EMI filtering, is an inductor or a choke. Chokes are built with wires, which are wound on the ferromagnetic core. The value of inductance is defined by the permeability and geometry of the core as well as by the number of turns of windings. However, it is all possible to make different configurations of windings in order to influence the particular mode (DM or CM). Different types of winding configurations for the 2-phase choke are shown in Figure 1.16.

The magnetic core can be wound with a single wire and applied to each phase as it is shown in Figure 1.16a. In that case, the phase current with DM and CM components causes the magnetic flux which is also built by two components. Such an inductance is observed in both modes. If the 2nd phase of the line is wound on the same core in opposite direction to the 1st phase (see Figure 1.16b), the resulting flux in the core is formed mostly by the DM part of the current. In this case, the CM flux is considered to be cancelled if the leakage is ignored. Another situation is observed with the agreed windings which are shown in Figure 1.16c. In this case, the DM flux is compensated in the core. Therefore, the value of inductance for the CM current is very high. Such an inductor is called the CM choke.

Despite, that some chokes can produce only CM or DM inductance, they should be able to handle the phase current which flows through the windings. This applies the limitation on the cross-section area of the wire. Moreover, the magnetic core should not be saturated during the operation. The saturation of the core is defined by the core properties including its geometry. The number of turns influences saturation as well. This results in the trade-off between the inductance of the choke and its dimension. Increase of inductance in the EMI filter leads to the increase of the filter dimension. This reduces the power density of a power converter if EMI filters are taken into account.



(a) Choke with single winding

(b) Chokes with opposite windings (DM)

(c) Choke with agreed windings (CM)

Figure 1.16.: Types of windings for a 2-phase choke.

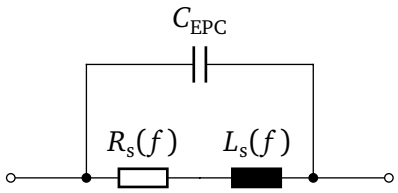


Figure 1.17.: The 1st-order representation of the choke.

The chokes include the parasitics which define their RF behaviour similar to the capacitors. But the RF characterization of the chokes for EMI filters is more complex in comparison to the capacitors [52]. The reasons for this are summarized as follows:

- Due to the skin and proximity effects in the wires, additional conduction losses should be considered in inductors. These losses are frequency dependent [53].
- In contrast to the ESL of a capacitor, the main stray element of a choke is the equivalent parallel capacitance (EPC). The EPC is formed by the stray capacitances between the turns of windings, between the winding itself and the core. The value of EPC is therefore strongly dependent on the type of winding. Slight variations (multi-layer or single layer implementation, the distance between turns) will lead to the huge differences in the value of EPC. Due to the EPC, a self-resonance is observed in the chokes [54].
- For the CM chokes, it is impossible to achieve full cancellation of the DM flux. Due to the leakage, some amount of DM inductance is also observed in the CM choke. This effect should be considered during the design of an EMI filter [55].
- The choke characterization is complicated by the properties of the applied ferromagnetic materials for the core. Due to the hysteresis of the magnetic material, the core introduces additional losses in the choke. The most significant parameters of the core material such as magnetic losses and permeability are also frequency-dependent [53, 52].

The simplest characterization of the choke is the 1st-order model shown in Figure 1.17. The stray series resistance $R_{\mathrm{s}}(f)$ reflects the magnetic losses of the core and conduction losses of the coils. The EPC is summarized as a single capacitance in parallel to the series inductance and resistance. The series elements $R_{\mathrm{s}}(f)$ and $L_{\mathrm{s}}(f)$ are frequency dependent. For the DM characterization of the CM chokes, the frequency dependence of $L_{\mathrm{s}}(f)$ for stray DM inductance can be neglected as DM flux do not circulate in the core [53]. The parameters of the 1st-order model can be extracted using impedance measurements [56, 57]. However, it is hard to fit these parameters with the measured impedance due to their frequency dependence. For the wider frequency ranges, it is necessary to extend the circuit representation of the choke using a higher number of components [52].

The discussed above model of the choke is valid only for the linear range of operation (small-signal analysis). Therefore, it is required to pay attention to the saturation of inductors during the design of EMI filters. Some models proposed in the literature are extended in order to include the behaviour of the choke under saturation [58]. For the CM chokes, the partial saturation can be also caused by the

DM currents due to small asymmetries between coils [59]. This effect can degrade the CM inductance as well [60].

New materials, such as nanocrystalline and amorphous alloys [61, 62], have appeared on the market in the last decade. These materials show superior properties in comparison to the classical materials such as iron and ferrit. Laminated iron cores show high permeability which decreases rapidly with a frequency increase. Therefore, this material is used for the grid filters to suppress the harmonics up to 40^{th}. In turns, ferrite cores show low permeability which is stable with frequency increase. It makes ferrite a standard material for the EMI filters in consumer electronics. The new materials demonstrate a better trade-off between its permeability with saturation flux density and broadband performance. Therefore, such materials are preferable in power electronics where high power disturbances should be suppressed in the wide frequency range. However, price of the new materials is still higher in comparison to the standard ferromagnetic materials. Consideration of the different core materials and types of windings complicates the design of the chokes for EMI filters. Some details on the design of the applied CM choke are given in Appendix C where nanocrystalline was chosen for the designed EMI filters.

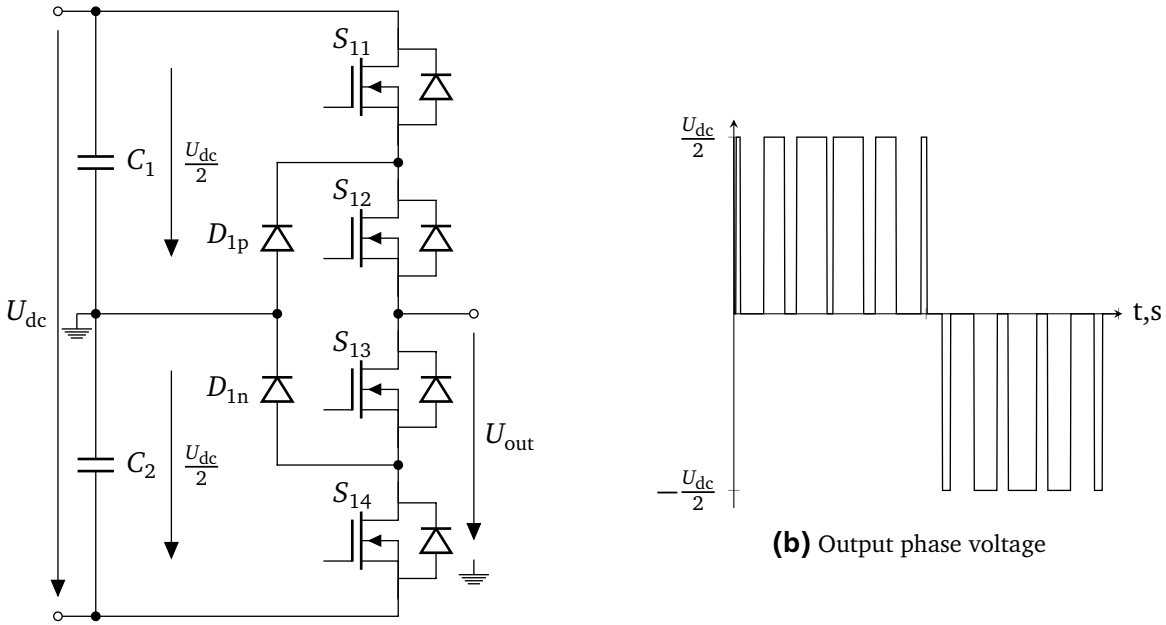
As it is shown in this section, the final value of insertion loss and the dimensions of the filter depend on the number of parameters: filter topology, values of capacitance and inductance, placement and design of the applied components. The selection and design of the components can be also a complicated task. Therefore, a lot of research works are devoted to the optimal design of the EMI filters [44, 10, 13, 64]. However, the EMI filter is not the only method which can be used to reduce the conducted noise in the AC drives. Looking on the simplified structure for the EMI analysis in Figure 1.14, it can be concluded that voltage on the noise receiver can be also reduced by changing the source side U_s and Z_s (The receiver side is fixed during the standard tests). Because the VSC is the main source of noise in the AC drive, it can be designed in the appropriate way to improve the EMI behaviour of the whole AC drive. According to Figure 1.14, it is possible to influence the source of noise U_s and/or its internal impedance Z_s. The next section discusses the EMI reduction techniques which can be applied during the design of VSC.

1.4.2 Converter Topologies

The first step in the design of any power converter is a topology selection. A large number of topologies was proposed in the last decades for the inverters applied in the AC drives. They are mostly proposed for the achievement of higher efficiency and power density of a converter itself [27]. In recent years, lots of inverter topologies are also studied in the sense of the generated conducted EMI. Some of them show superior behaviour. A brief overview is given on some of the existing inverter topologies with the reduced EMI in this section.

In Figure 1.6, the AC drive system is considered with the conventional full-bridge (FB) inverter. The FB inverter consists of 6 switches S_1 to S_6. This topology was proposed long ago and supposed to be the simplest one for the DC to AC conversion [27]. It requires lower effort for the gate driver and control design. The FB topology of an inverter is very robust and efficient for low and medium voltages/powers. Therefore, this kind of topology is still the most widely used one in the industrial AC drives.

A reduced level of conducted noise can be achieved utilizing multi-level inverter topologies [14]. Such inverters begun to appear in the research works in the middle of '80s. The first multi-level converters were proposed for high power applications. The main idea is to divide the DC voltage source into several



(a) Phase leg of a NPC converter

(b) Output phase voltage

Figure 1.18.: Neutral point clamped converter.

series-connected sources (voltage levels). Each source can be then connected to the output of a converter using the corresponding configuration of the power switches [27]. The resulting voltage at the output of inverter has a staircase shape. Such waveform corresponds more to an ideal sinusoid in comparison to the PWM voltage of 2-level FB inverter (see Figure 1.7). The apparent PWM sampling frequency is increased by the number of levels. Therefore, the multi-level converters can be switched with lower frequency reducing the losses. Moreover, power switches with a lower blocking voltage can be applied in a multi-level converter. It reduces also the conduction losses due to the lower on-state resistance of such switches. The 3-level neutral point clamped (NPC) converter was proposed as the first alternative to the FB inverter for the traction drives [65]. The operation principle of NPC inverter is explained in Figure 1.18.

One phase of NPC inverter is shown in Figure 1.18a. The converter consists of 4 series connected switches from S_{11} to S_{14} and two additional clamping diodes D_{1p} and D_{1n}. The output voltage U_{out} can be connected either to the positive or to the negative rail by turning on all high side or low side switches respectively. If only inner switches S_{12} and S_{13} are turned on, the output voltage is connected to the mid-point of the input DC source through the clamping diodes. The mid-point can be organised using series-connected capacitors. Therefore, the output voltage has three levels instead of two in comparison to FB inverter (see Figure 1.7). The output voltage for NPC under simple SPWM operation is shown in Figure 1.18b.

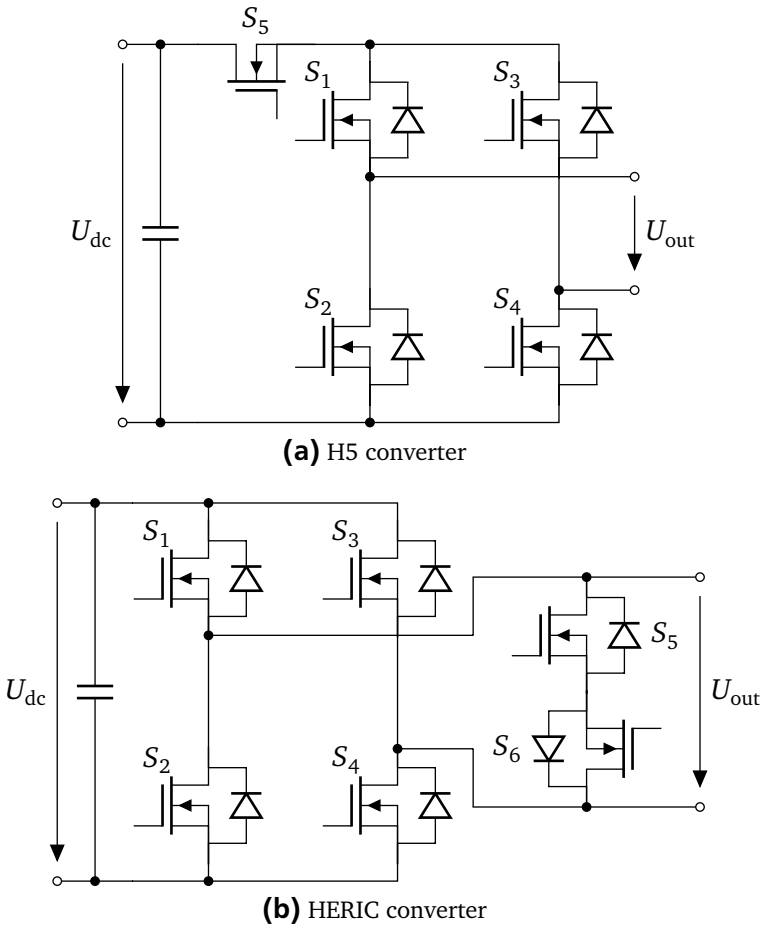
The resulting DM and CM output voltages of the three-phase converter are switched between 5 and 6 levels of U_{dc} respectively. The staircase waveform allows the same THD of output current as in FB converters but under lower sampling frequency of PWM [27]. The resulting RF spectrum of the output voltages is lower in NPC converters that results in the improved EMI behaviour [14]. Moreover, a lot of PWM techniques were developed for the three-phase NPC converters with reduced or even ideally

eliminated CM voltage [66, 67, 68]. However, these PWM techniques for NPC converters degrade in the quality (LF harmonics) of the output voltage [69]. The number of levels can be easily increased using additional switches and splitting the input voltage with more capacitors. In this case, the improvement of output THD and EMI behaviour will be increased as well [15]. The drawback of multi-level converters lies in their complexity. It is necessary to operate more power switches and to keep the voltage balance between the split capacitors. The control of the multi-level converter is more complex in comparison to the simple FB inverter. Additionally, the usage of extra semiconductors increases the price and decreases the reliability of the multi-level converters.

In order to keep the reliability achieved with the FB converter, other topologies were proposed which have lower complexity than the multi-level converters but allow the improvement of the EMI behaviour. In Figure 1.19 the 2-phase inverters are shown which were proposed for photovoltaic (PV) application [70]. One of the biggest problem in transformerless grid-connected PV converters is the leakage current which flows through the capacitance of a PV panel [71]. This leakage current is the CM current which is also recognized as conducted noise during the EMI measurements. The main idea in such converters is to decouple the input DC and output AC sides during the free-wheeling states of a converter. As it is shown in Subsection 1.4.3, the maximum levels of CM voltage are observed during the free-wheeling states (zero vectors $\vec{V}_0$ and $\vec{V}_7$ in Table 1.2). Decoupling of AC from DC side during the free-wheeling states decreases the amplitude of the CM voltage. Therefore, the generated conducted noise should be decreased as it consists mostly of the CM current.

In H5 topology shown in Figure 1.19a, the DC side is disconnected from the converter during the free-wheeling states by means of the one additional switch S_5 [72]. This switch is turned off during the zero states of FB inverter. The problem of such a topology is additional losses which occur in this switch. The S_5 has to handle the whole current at the input (DC). The AC side of the inverter can be also decoupled during free-wheeling states by means of two additional anti-series switches S_5 and S_6 as it is done in HERIC inverters shown in Figure 1.19b. The anti-series switches are turned on during the free-wheeling state. Additional losses in HERIC converter are lower because the S_5 and S_6 conduct only during the zero states of the inverter. However, the complexity of HERIC converter is higher as two additional switches are required. Both inverters show the reduction of leakage currents in transformerless PV converters. Therefore, they are also proposed for the reduction of conducted CM noise [73, 74]. The considered topologies can be easily extended to three-phase systems [75]. The control of such converters has only a minor difference in the complexity from the FB inverters. However, some extra switches are still required increasing the costs.

The considered topologies can be applied to reduce the conducted noise. However, they are mostly influencing the LF part of the converter output CM voltage. The reduction of RF conducted noise can be achieved by the soft-switching converters [76]. The topology of such a converter assumes to provide zero voltage or zero current during the switching event. It reduces the switching losses and gives the possibility to increase the switching frequency. Commutation under zero current or voltage avoids the RF oscillations which occur during the switching process. Different topologies can be used to operate with zero switching [27]. An example of the inverter with a soft switching is the auxiliary commutated pole inverter (ACPI). This converter provides a zero voltage commutation by means of an auxiliary branch in each phase leg which consists of two switches, inductor and snubber capacitors [77]. Under zero



(a) H5 converter

(b) HERIC converter

Figure 1.19.: Topologies proposed for the transformerless photovoltaic stations.

voltage switching, the spectrum of the output voltage is lower in the RF range in comparison to the hard switched FB inverter. As it was reported in [78], the conducted noise can be significantly improved in the RF range, if the ACPI is applied in the AC drive. However, the level of conducted noise in the low-frequency range remains the same in comparison to the conventional FB converter. The complexity of control for soft-switching is also very high, as soft switching conditions must be guaranteed during the operation. The ACPI requires also installation of additional switches and passive components which can reduce the power density of a converter.

This section considers various topologies which can be applied in the AC drive instead of the classical FB inverter. The multi-level topologies offer improved EMI behaviour in the whole frequency range and the increased efficiency. However, they also introduce an additional degree of complexity. The topologies with decoupled free-wheeling states (H5 and HERIC) show almost the same complexity and efficiency as FB inverter. But, they are only efficient for the reduction of the low-frequency CM current. The soft switching topologies can be used to increase the efficiency and to decrease the RF noise but at the price of complex structure with additional active and passive components.

1.4.3 PWM Techniques

As it is shown in the previous section, the conducted noise in the AC drive system can be reduced by means of different topologies of VSC. However, in comparison to the 2-level FB inverter, all other topologies require the implementation of additional power switches and/or passive components increasing the price and reducing the reliability of a converter. Reliability is a crucial factor for the aerospace and civil aviation industry. Moreover, the conventional FB VSC is already implemented in the most AC drives which are in the operation nowadays. Therefore, some methodologies to reduce the conducted noise were also developed for the implementation in the conventional 2-level FB inverters. As it is shown in Section 1.2, the spectrum envelope depends on the applied modulation technique. It is not possible to change the total amount of energy of harmonics. But implementation of different modulations techniques can be used to spread the spectrum among the harmonics that can result in the improvement of EMI behaviour. Such an approach requires only minor changes of the VSC control system. Different modulation techniques with improved EMI behaviour were discussed and compared in [79, 80, 81, 17, 82]. Some of the techniques will be considered below in details to understand the basic principles behind them.

According to Figure 1.8, the level of the output voltage on the whole frequency range depends on the sampling frequency of PWM. The decrease of the energy transmitted by the harmonics can be achieved by the reduction of the sampling frequency f_s. However, if only motor inductance is used as a low pass filter, the sampling frequency is limited by its minimum value. Additionally, the reduced sampling frequency can cause an acoustical noise in the motor of a drive[83].

The first PWM technique with a reduced level of conducted noise is a so-called random PWM. This technique was proposed for SPWM for the reduction of acoustical noise in electrical drives [84]. Later, this technique was also applied for the reduction of conducted EMI [79]. In random PWM, the sampling frequency is variated during the fundamental period of the output voltage. In that case, the spectrum is spread among the frequencies which are applied during the randomization reducing the level of output voltage on the whole frequency range. Such a technique can be easily applied to any type of VSC with any type of PWM. However, as discussed in [85], the random PWM reduces only the level of noise measured by the EMI receiver if the value of RBW defined in the applied standard is lower than the sampling frequency. Because the noise is measured under RBW equal to 1 kHz according to DO-160 [24], this condition is always fulfilled in the modern AC drives. However, random PWM can even worsen EMI behaviour under special operation points [85].

As it is discussed in Section 1.3, the CM current has the most significant impact on the conducted noise in AC drives measured according to DO-160. Another set of PWM techniques are aimed to reduce the level of output CM voltage. Before such PWM techniques will be considered, it is necessary to explain the principle of space vector PWM (SVPWM). This type of PWM is a standard technique for the most three-phase VSCs [34].

The SVPWM belongs to the class of the digital PWM techniques which requires algorithmic units for its calculation. As the computational power of microcontroller units (MCU) and digital signal processors (DSP) were increasing, the digital PWM techniques were taking more attention by the engineers. Implementation of SVPWM provides such benefits as the increased maximum output voltage of inverter

Table 1.2.: The possible switches states of FB converter and the resulting output voltages.

State	High side			Low side			U_a	U_b	U_c	U_α	U_β
	S_1	S_3	S_5	S_2	S_4	S_6					
$\vec{V}_0$	0	0	0	1	1	1	$-\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	0	0
$\vec{V}_1$	1	0	0	0	1	1	$+\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$\frac{2U_{dc}}{3}$	0
$\vec{V}_2$	1	1	0	0	0	1	$+\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$\frac{U_{dc}}{3}$	$\frac{U_{dc}}{\sqrt{3}}$
$\vec{V}_3$	0	1	0	1	0	1	$-\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$\frac{-U_{dc}}{3}$	$\frac{U_{dc}}{\sqrt{3}}$
$\vec{V}_4$	0	1	1	1	0	0	$-\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$\frac{-2U_{dc}}{3}$	0
$\vec{V}_5$	0	0	1	1	1	0	$-\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$\frac{-U_{dc}}{3}$	$-\frac{U_{dc}}{\sqrt{3}}$
$\vec{V}_6$	1	0	1	0	1	0	$+\frac{U_{dc}}{2}$	$-\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$\frac{2U_{dc}}{3}$	$-\frac{2U_{dc}}{\sqrt{3}}$
$\vec{V}_7$	1	1	1	0	0	0	$+\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	$+\frac{U_{dc}}{2}$	0	0

and decreased THD. The SVPWM operates in the two-phase $\alpha\beta$ coordinates instead of the three-phase abc system. The required coordinates in $\alpha\beta$-plane can be obtained by means of a Clarke transform. This type of three-phase transformation is also explained in Appendix A.

In order to understand the principles of SVPWM, it is required to consider all possibles states of the power switches S_1 to S_6 for the conventional FB inverter (see Figure 1.6). Each switching state produces the respective output voltages. The corresponding switching states and output voltages are presented in Table 1.2. The output voltages referenced to the value of U_{dc} are presented in abc- and $\alpha\beta$-frames respectively. There are 8 possible switching states for the 2-level FB converter. Each switching state corresponds to a vector from $\vec{V}_0$ to $\vec{V}_7$ on the axes of $\alpha\beta$-plane [34]. There are 2 zero vectors $\vec{V}_0$ and $\vec{V}_7$ with zero values of output $\alpha\beta$ voltages. The rest ($\vec{V}_1$ to $\vec{V}_6$) are the so-called active vectors. All vectors are allocated on the $\alpha\beta$-plane in Figure 1.20 that allows the explanation of SVPWM working principles.

The active vectors divide the whole plain into 6 sectors in Figure 1.20. The reference voltage, which is generated by the control system of AC drive, can be also presented in $\alpha\beta$-frame. For normal sinusoidal three-phase voltage the reference vector $\vec{V}_{ref}$ rotates on the plane crossing all sectors. According to SVPWM, it is possible to synthesis the desired reference vector using border vectors of the current sector and zero vectors for each sampling period [34].

For the 1st sector, which is highlighted in Figure 1.20, vectors $\vec{V}_1$ and $\vec{V}_2$ are assumed to be used to modulate the reference vector in the conventional SVPWM. The modulation of $\vec{V}_{ref}$ can be achieved by fulfilling the equation (1.12), where T_s is the sampling period of PWM, T_1 and T_2 are the durations of the corresponding active vectors, whereas T_0 is a duration of zero vectors.

$$\vec{V}_{ref} T_s = \vec{V}_1 T_1 + \vec{V}_2 T_2 + \vec{V}_0 T_0 \tag{1.12}$$

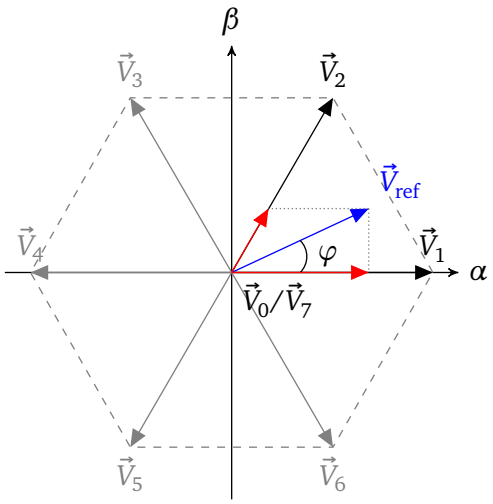


Figure 1.20.: The vector diagram for SVPWM.

Decomposing the (1.12) on the real and imaginary parts, it becomes possible to obtain equations for the calculation of vectors duration (1.13).

$$\begin{aligned} T_1 &= \sqrt{3}\hat{V}_{\text{ref}} T_s \sin(\frac{\pi}{3} - \varphi) \\ T_2 &= \sqrt{3}\hat{V}_{\text{ref}} T_s \sin(\varphi) \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{1.13}$$

The required active and zero vectors can be applied in any sequence. This is another benefit of SVPWM. Depending on the sequence, different properties can be obtained for the output PWM voltage [34]. The symmetric sequence shown in (1.14) provides lower THD and switching losses in comparison to the conventional SPWM [27]. With a slight THD increase, it is also possible to reduce the switching losses even more (up to 30%). This type of sequence is called discontinuous pulse width modulation (DPWM) [34]. Only one zero vector should be used during the sampling period to implement DPWM. An example of possible vector sequence of DPWM is shown in (1.15) for the 1st sector.

$$\vec{V}_0 \rightarrow \vec{V}_1 \rightarrow \vec{V}_2 \rightarrow \vec{V}_7 \rightarrow \vec{V}_7 \rightarrow \vec{V}_2 \rightarrow \vec{V}_1 \rightarrow \vec{V}_0 \tag{1.14}$$

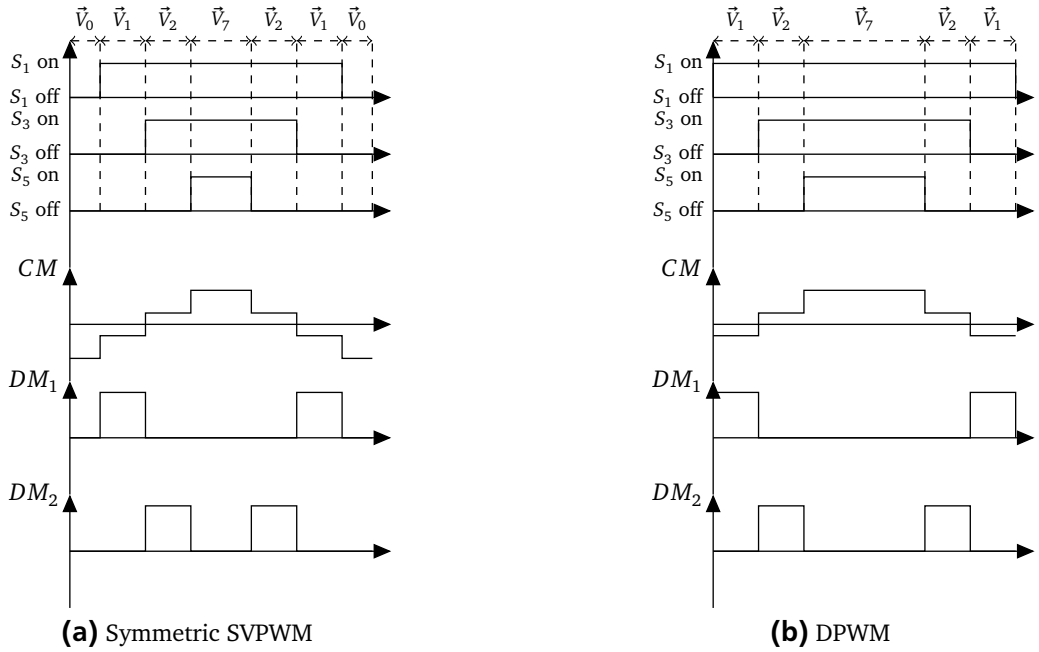
$$\vec{V}_1 \rightarrow \vec{V}_2 \rightarrow \vec{V}_7 \rightarrow \vec{V}_2 \rightarrow \vec{V}_1 \tag{1.15}$$

The space vector approach simplifies the analysis of the converter output voltage [34]. Using values of output phase voltages from Table 1.2 and equations (1.8)..(1.10), it is possible to find the corresponding output CM and DM voltages for each switching state of FB inverter (see Table 1.3). Further, the output mode voltages can be analysed for the different types of SVPWM. The DM and CM output voltages of symmetrical SVPWM and DPWM techniques are compared in Figure 1.21.

The corresponding CM and DM voltages can be observed for the symmetric SVPWM in Figure 1.21a. The phase-to-phase voltages (DM) correspond to the normal PWM signals of a certain duration. The

Table 1.3.: DM and CM output voltage for FB VSC.

State	CM	DM_1	DM_2
$\vec{V}_0$	$-\frac{U_{dc}}{2}$	0	0
$\vec{V}_1$	$-\frac{U_{dc}}{6}$	U_{dc}	0
$\vec{V}_2$	$\frac{U_{dc}}{6}$	0	U_{dc}
$\vec{V}_3$	$-\frac{U_{dc}}{6}$	$-U_{dc}$	U_{dc}
$\vec{V}_4$	$\frac{U_{dc}}{6}$	$-U_{dc}$	0
$\vec{V}_5$	$-\frac{U_{dc}}{6}$	0	$-U_{dc}$
$\vec{V}_6$	$\frac{U_{dc}}{6}$	U_{dc}	$-U_{dc}$
$\vec{V}_7$	$\frac{U_{dc}}{2}$	0	0

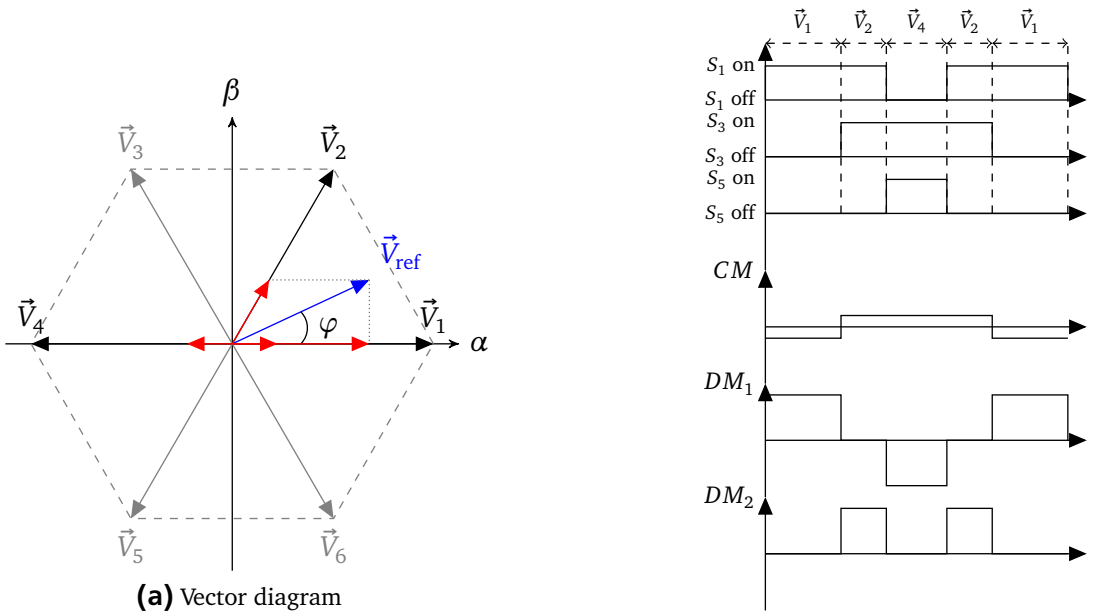


(a) Symmetric SVPWM **(b)** DPWM

Figure 1.21.: Gate signals and corresponding output voltages for different SVPWM sequences.

shape of this signal depends on the current position of the reference vector on the $\alpha\beta$-plane. At the same time, CM voltage has a staircase shape which switches between several possible levels $\pm\frac{U_{dc}}{2}$ and $\pm\frac{U_{dc}}{6}$ during the sampling period. It should be mentioned, that the highest absolute value of the CM voltage is achieved during the zero vectors. The duration of zero vectors depends mostly on the modulation index m. Therefore, the higher CM voltage stress on the motor will be observed for the operation points with low modulation indexes of VSC. It has a considerable impact on the generated conducted noise and saturation of CM chokes of EMI filters [16]. If AC drive is operated in different operation points with low and high modulation indexes, its EMI behaviour should be analysed for all operation points.

The pattern of DPWM has a reduced number of switching events per modulation period that is shown in Figure 1.21b. The waveforms of DM voltages are almost the same as for symmetric SVPWM observing



(a) Vector diagram

(b) Timing diagram and output mode voltages

Figure 1.22.: Vector diagram and corresponding outputs of AZPWM.

only a small phase shift in comparison to the DM voltage in Figure 1.21a. However, the valuable changes can be observed in the CM voltage of DPWM. Due to the lack of vector $\vec{V}_0$, the CM voltage changes its value from $-\frac{U_{dc}}{6}$ to $+\frac{U_{dc}}{2}$ adding the DC bias in the CM voltage under DPWM. The DC bias does not have any impact on the typical AC drive, as there is no connection between the neutral point of the motor and protective earth. But, due to this bias, the AC part of CM voltage is lower under DPWM in comparison to the symmetric SVPWM. As it was discussed in [81, 82], implementation of DPWM reduces the amplitude of CM voltage and current.

Looking at the output voltages of symmetric SVPWM and DPWM (see Figure 1.21), it can be concluded that the zero vectors $\vec{V}_0$ and $\vec{V}_7$ have the highest impact on the CM voltage. But, the decomposition method of reference vector shown in Figure 1.20 requires the application of zero switching states. However, such a decomposition is not the only possible one. A set of PWM techniques were developed based on the space vector modulation without the application of zero vectors [86]. These techniques are also called reduced common mode voltage PWM (RCMV-PWM). In [87], the new RCMV-PWM technique was proposed where the zero vectors were replaced by the two neighbouring active vectors. Such type of SVPWM was called an active zero PWM (AZPWM). The principle of AZPWM is explained in Figure 1.22.

The decomposition of $\vec{V}_{ref}$ under AZPWM is shown in Figure 1.22a. As can be seen, it is similar to the standard SVPWM scheme (see Figure 1.20). But, interval T_0 is spread among neighbouring vectors ($\vec{V}_1$ and $\vec{V}_4$ for the 1st sector). The calculation of interval timings T_0, T_1, T_2 is the same as in SVPWM (see (1.12) and (1.13)). The switching sequence could be also selected freely. The best THD of the output

current will be achieved with a symmetric sequence [87]. The possible sequence for the reference vector in the 1st sector for AZPWM is presented in (1.16).

$$\vec{V}_1 \rightarrow \vec{V}_2 \rightarrow \vec{V}_4 \rightarrow \vec{V}_4 \rightarrow \vec{V}_2 \rightarrow \vec{V}_1 \tag{1.16}$$

Using Table 1.3, it is also possible to represent the timing diagrams for the chosen sequence of AZPWM. The corresponding CM and DM voltages are shown in Figure 1.22b. The amplitude of CM voltage is limited by the value of $\pm\frac{U_{\mathrm{dc}}}{6}$ under AZPWM. The DM_2 voltage has the same shape as under SVPWM and DPWM (see Figure 1.21). However, some waveform changes are observed for the voltage DM_1. In comparison to the conventional SVPWM, the DM_1 is switched between zero value and $\pm U_{\mathrm{dc}}$ on the one sampling period. The average value of DM voltages on the one sampling period is the same under SVPWM and AZPWM. But, due to the bipolar nature, more energy is shifted in the harmonics of DM voltages under AZPWM. It means that the reduction of CM voltage/current lead to an increase of the DM noise. However, assuming that conducted noise is mostly defined by the CM current in AC drives (see Section 1.3), the AZPWM should lead to the decrease of the overall conducted EMI measured according to DO-160.

Other neighbouring active vectors ($\vec{V}_3$ and $\vec{V}_6$ for the 1st sector) can be used to replicate the zero vectors [86]. This type of PWM is called AZPWM2. Following the idea of DPWM to reduce the amount of switching actions during the sampling period, the near state PWM (NSPWM) was presented in [88]. In this type of PWM, the active vectors, which are replacing the zero vectors, are selected according to the allocation of reference vector in each sector. The drawback of NSPWM lies in the limited value of modulation index (from $m_{\mathrm{min}} = \frac{4}{3\sqrt{3}}$ to $m_{\mathrm{max}} = \frac{2}{\sqrt{3}}$) [88]. In the other type of PWM, which is called 3 active vectors PWM in [86] and remote state PWM (RSPWM) in [80], the modulation index is limited by the maximum value of $m_{\mathrm{max}} = \frac{4}{3\sqrt{3}}$. The RSPWM was proposed firstly in [89] where it was stated to use only odd or even active vectors during the modulation. In that case, the CMV voltage remains on the constant level of $\frac{U_{\mathrm{dc}}}{6}$ during one modulation period. The NSPWM and RSPWM were combined as a single PWM technique in [81] showing the significant reduction of CM voltage and current.

All RCMV-PWM techniques were compared in [80, 81] for the AC drive application and in [17, 82] for PV grid-connected converters. The modulation schemes were compared according to the resulting THD of phase current, losses in the VSC and amplitude of CM leakage current. In [90], the comprehensive analysis was provided on the impact of various PWM techniques on the conducted noise and the saturation of CM chokes of EMI filter. The noise level was considered in the dedicated frequency range and saturation of chokes was analysed using volt-second characteristic. It was shown, that it is possible to reduce the noise level and peak value of CM current to avoid the saturation of CM chokes. However, it was also shown that CM current can be increased under RCMV-PWM techniques at particular frequencies. Therefore, the resonance frequencies should be analysed in the propagation path of CM current of an AC drive before such a PWM technique can be applied.

The number of PWM techniques for conventional FB VSC is quite high. In general, two groups of PWM techniques can be highlighted. The 1st is based on the random frequency modulation reducing the measured noise rather than the energy of the noise. Another set of PWM techniques has a decreased value of output CM voltage making the noise lower as it mostly consists of the CM current. All of PWM

techniques are reducing the effort for EMI filter design. However, they can also have the drawback such as increased losses and/or THD of the output phase current. It should be also mentioned, that different RCMV-PWM techniques were also developed for 3-level converters [91]. Due to the higher amount of possible switching vectors, the CM noise reduction is supposed to be much higher in multi-level converters with RCMV-PWM.

1.4.4 Converter Hardware Design

Before this section will continue a discussion about the other techniques of conducted EMI reduction in AC drives by means of VSC design, it is necessary to clarify which kind of activities are defined under the term "hardware design" in this research work. Different aspects of VSC design can be understood under this term. For example, the topology selection procedure, which is considered in Subsection 1.4.2, can be also related to the hardware design. In the conducted research, the activities, which are made usually at the last design stages, are understood as "hardware design". These activities are closer to product development rather than to the prototyping. These are:

- The selection of components for a power converter. This design stage is quite typical for any electronic system. After the control and electrical circuits are simulated with ideal components, it is necessary to choose the real physical parts of the converter. For the power converters, it can be power switches, passive components (e.g. DC link capacitors and chokes), gate driver circuits, additional power supplies and sensors [92]. Another important part of the power converter design is a cooling system, which should be able to dissipate the losses generated by the power switches. Despite, that thermal design can require high effort [93], the development of the cooling system is also considered as a component selection in this work (heatsink selection).

- After the components are chosen, they should be connected with each other both mechanically and electrically defining the layout of the converter. For the low power applications, the printed circuit board (PCB) technology is usually applied. The middle and high power converters are connected with copper or aluminium bus bars. For simplicity, only the PCB technology is considered in this work.

- One special subsystem required for any power electronics device is a gate driver [27]. The gate drivers can be designed in different ways, that results in the different switching behaviour of power switches [94]. Switching behaviour has a huge impact on EMI of the power converter as well as on the losses. Therefore, the design of this subsystem of the VSC will be considered separately despite, that it could be also related to the components selection.

The generation of conducted noise by an AC drive can be also reduced with an appropriate hardware design of VSC. However, it is hard to put together all mentioned above activities of conducted noise reduction because they are mostly based on the experience of engineers rather than on the theory. In this section, an attempt will be made to structure this topic.

Presented in the literature activities for the EMI reduction by means of the power converter design are addressed to the particular aspects of the converter hardware design. These activities are not structured

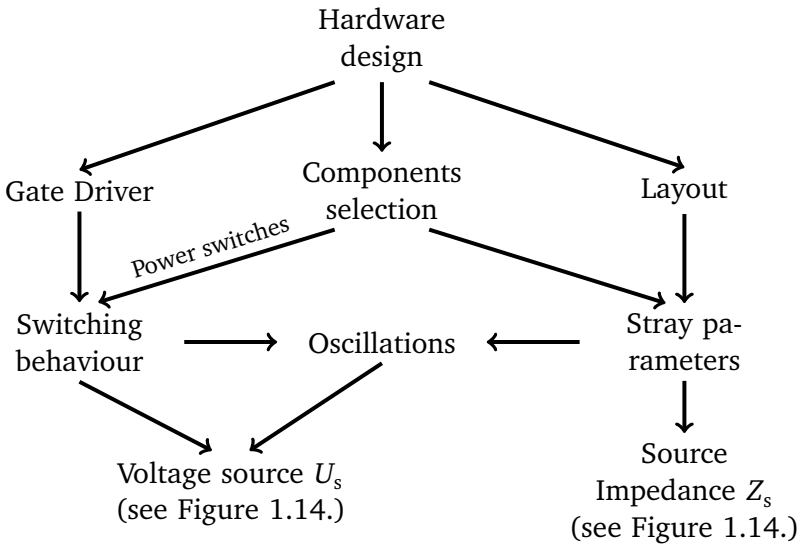


Figure 1.23.: Summarized hardware design activities to reduce the conducted noise generated by a power converter.

considering the whole system. After the research, the mentioned above aspects of the converter hardware design were structured as in Figure 1.23. It is better to start from the bottom of the diagram presented in Figure 1.23. According to the simplified structure of an electronic system for the EMI analysis (see Figure 1.14), the converter can be represented by a voltage source (noise) and internal impedance. At the first step, all hardware design approaches can be divided into two groups according to the way of generated noise mitigation: improvement of the voltage source U_s or matching of the source impedance Z_s.

The adjustment of the internal impedance of noise source Z_s is also a quite typical approach to minimize the EMI noise for an electronic device. The internal impedance of the source (converter) is defined mostly by the parasitics which are observed in the converter. These are the stray inductances of interconnections and capacitances between phases and ground (some of them are already considered in Figure 1.6). In turns, the parasitics of a converter are defined by the PCB layout and by the components which were applied (selected) for the design. The PCB layout of a power converter can be evaluated using finite element models (FEM). Such works were conducted in [95, 96] for the DC/DC converters. The layout of VSC was considered during detailed EMI simulation in [97]. The research provided in [98] serves as an example of how components selection can influence the impedance Z_s. In this work, the stray capacitance between the power switch and the heatsink was reduced using electrically non-conductive heatsink leading to the decrease of generated EM noise.

The 2nd group of activities is aimed to reduce the energy which is transmitted as noise. The amount of this energy is defined significantly by the voltage source U_s (see Figure 1.14). The application of different converter topologies and PWM techniques can be also related to this group. However, the methods considered in the previous sections are influencing mostly the LF part of the PWM signal. The switching behaviour, which is defined by the gate drivers and selected power switches (see Figure 1.23), defines how fast the current and voltages are commutated during operation of the inverter. For the simplified representation of the PWM signal in Figure 1.8, the switching behaviour is reflected by the

rise/fall times (t_f). It means that the assumed hardware design activities influence the RF part of the spectrum envelope through the switching behaviour of power switches.

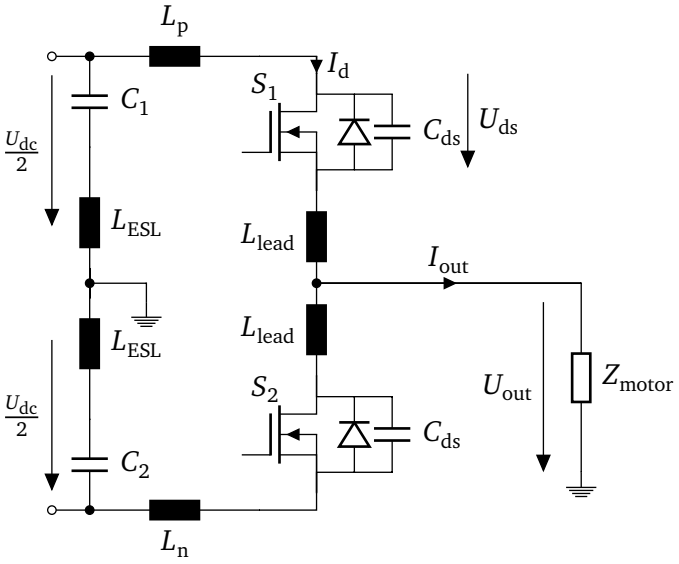
The switching behaviour of the power switches in VSC is a complicated process, which is also accompanied by the oscillations of voltages and currents in the commutation path. These oscillations are special phenomena in power electronics due to the commutation of relatively high currents [27]. They are associated with the switching losses in a converter during the design. However, they influence the level of the generated noise as well. At the same time, oscillations are also defined by the stray parameters of the converter. It means that the parasitics (impedance of converter) have an indirect impact on the voltage source (U_s). In order to understand the switching behaviour of the modern power semiconductors and how it is possible to improve it from the EMI point of view, it is necessary to consider the commutation process of the power MOSFETs in VSCs in details.

Switching Behaviour

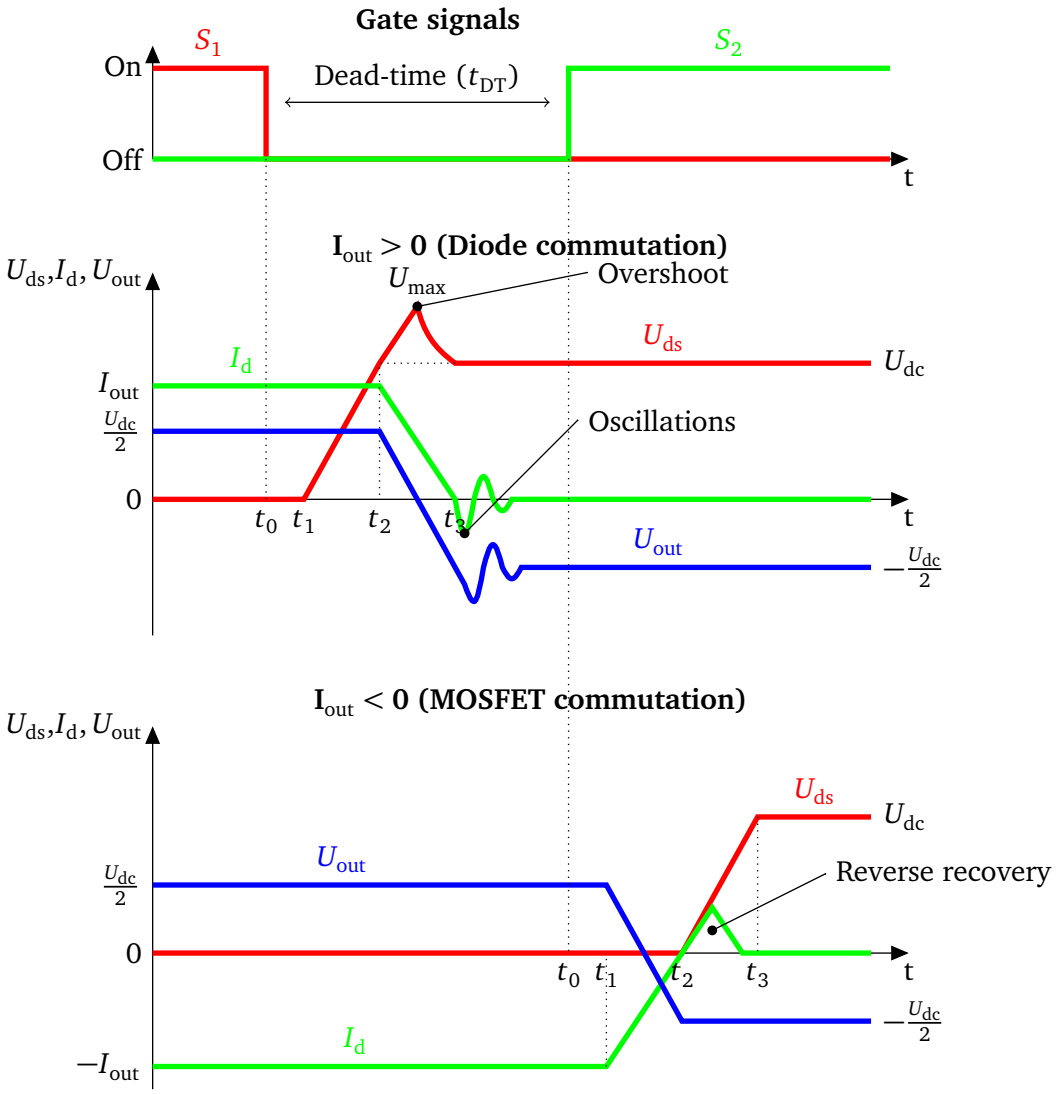
In most research works, the switching process is analysed only from the switch point of view. A lot of recent studies are devoted to WBG devices due to their high switching speed [99, 100]. The main goal of these works is to estimate and to reduce the losses and/or the maximum voltage overshoot of the power switch. Hence, only the current of a switch and the voltage between its terminals is considered. These parameters are essential for the normal operation of VSC. However, in the case of EMI analysis, it is also necessary to understand, how does the output phase voltage behave during the switching event. Comprehensive analysis of the switching process for Si- and SiC-based AC drive inverter including output phase voltage was provided in [101]. The relationship between switching behaviour and conducted EMI in the variable speed drives is also presented in [38]. Some conclusions of these works are summarised below which are important for the analysis of PWM voltage spectra in Section 2.3 and further investigation in Chapter 4.

The commutation process, which is observed in the power switches of a VSC, is explained in Figure 1.24. It is not enough just to consider the switching event of only one switch because the switching action on the high side switch is always combined with the switching of the low side switch and vice versa. However, assuming the symmetrical operation, it is enough to consider only one phase leg of the three-phase VSC which is shown in Figure 1.24a. In Figure 1.24a, the MOSFET based half-bridge is supplied by the bipolar DC power supply. The output phase voltage is applied to the motor which is represented by a single-phase impedance Z_{motor}. For simplicity, it can be considered that input voltage U_{dc} and output phase current I_{out} are constant during one switching event. For the one switching period, this assumption is normally fulfilled because time constants of motor and DC link are normally much higher than the sampling period of PWM. The switches can be commutated either with the positive or negative value of the output current. All components are also shown with the corresponding stray parameters in Figure 1.24a. The respective parasitics of MOSFETs are the inductance of the leads (L_{lead}) and stray drain-source capacitance (C_{ds}).

The switching behaviour for the positive and negative value of I_{out} is shown in Figure 1.24b. The typical gate signals can be observed on the upper plot. It can be seen, that there is a certain time slot right after the turn off of the high side switch (S_1), then both switches are in the off state. This period is called dead-time (t_{DT}). Dead-time is applied to ensure the off state of the power switch in a half-bridge



(a) Schematics of a half-bridge with parasitics



(b) Voltages and currents during turn off process

Figure 1.24.: Analysis of the turn-off process of high-side switch in a half-bridge.

before the opposite switch will start to conduct. Otherwise, the short circuit can occur in the DC link if both high (S_1) and low side (S_2) switches will be switched simultaneously [27].

For the positive direction of the output current ($I_{out} > 0$ in Figure 1.24b), the commutation starts after a small delay between t_0 to t_1. This delay is caused by the gate-to-source capacitance of a power switch which should be charged up to the threshold value of the gate voltage [27]. The drain-source voltage U_{ds} of the switch S_1 starts to increase at t_1. At the same time, the drain current I_d of MOSFET remains almost constant. It means, that the output is still connected to the positive rail of the DC supply and $U_{out} = \frac{U_{dc}}{2}$. After U_{ds} reaches the value, which is equal to the input DC link voltage $U_{ds} = U_{dc}$, the body diode of S_2 starts to conduct. Then I_d of the high side switch S_1 starts to decrease slowly commutating to the body diode of the opposite switch. At the same time output voltage is commutated to the negative rail of the DC supply. The voltage overshoot can be observed during the period of drain current fall from t_2 to t_3. This effect appears due to the stray inductances in the commutation path of I_d. The voltage between MOSFET terminals continues to grow reaching its maximum value U_{max} which is defined by (1.17):

$$U_{max} = 2U_{dc} + L_{\Sigma}\frac{dI_d(t)}{dt} \simeq 2U_{dc} + L_{\Sigma}\frac{I_{out}}{t_3 - t_2} \tag{1.17}$$

, where L_{Σ} (1.18) is a sum of all stray inductances in the commutation path according to Figure 1.24a.

$$L_{\Sigma} = 2ESL + L_p + L_n + 2L_{lead} \tag{1.18}$$

Because current is commutated to the body diode of a low side switch, the duration of voltage fall $t_f = t_3 - t_2$ is defined by the output capacitance of a MOSFET S_1 and by the value of I_{out} [101]. The output current is charging the drain-source capacitance. The further turn-on of the switch S_2 after the dead-time does not have a huge impact on the switching behaviour. The current will move into the switch from its body diode. After current I_d reaches its zero value, some oscillations can be observed in the current and output voltage. This is due to the resonant circuit which is formed by the drain-source stray capacitance of a MOSFET (C_{ds}) and by the stray inductance. The impact of these parasitic parameters on the oscillations during switching of a MOSFET was studied in [102].

The opposite situation is observed in the case of the negative output current ($I_{out} < 0$) which is shown on the lower plot in Figure 1.24b. After turn-off of the high side switch S_1, the current continues to flow through the body diode and no commutation is observed for the output voltage. The switching process starts after the dead-time when the low side MOSFET is turned on. Similar, after the short delay the commutation starts with a current rise at t_1. The current I_d moves firstly from the body diode of S_1 into the MOSFET S_2. The output voltage is also commutated from the positive to the negative rail of the DC supply. The duration of the time from t_1 to t_2 is defined by the MOSFET itself and by its gate driver [27]. After the current reaches the zero value, the voltage across the high side switch starts to rise. A small additional current rise of I_d is also observed after t_3. This is due to the reverse recovery of charge carriers of the body diode in S_1. The commutation of output voltage from negative to positive rail can be considered in a similar way. However, in that case, the low side switch S_2 is turned off first.

Looking at the switching behaviour of a half-bridge several ideas, which are essential for the further analysis, can be conducted:

- The voltage overshoot and oscillations are observed due to the steep changes of relatively high currents and due to the presence of stray parameters in the commutation path.
- The switching behaviour is affected by the output current. The value of I_{out} defines when the commutation will take place (right at the beginning or after the dead-time).
- The duration of dead-time (t_{DT}) has also a certain impact on the spectrum of the output PWM voltage.
- The duration of fall/rise time (t_{f}) for the output phase voltage can be defined either by the diode or MOSFET commutation.
- In the case, then the output voltage is commutated by the body diode, the duration of voltage rise/fall depends on the values of I_{out} and C_{ds}.

The commutation times of power switches in VSC are defined by the MOSFET, output current and drain-source capacitance as well as by the gate driver. Through the gate driver design, it is possible to influence the switching behaviour.

Improvement of Switching Behaviour

The switching of a power semiconductor is a very complicated process, which is accompanied by several aspects. In most research works dedicated to the impact of switching behaviour on EMI, only part of a problem is considered. An attempt below is made to summarize all these approaches in order to give the common view on the problem.

The impact of dead-time on EMI behaviour was studied in [103]. It was shown that the amplitude of CM current increases with a dead-time that can also lead to the saturation of CM chokes in the EMI filters. A significant impact of dead-time was reported for VSC based on 3-level converters operated with RCMV-PWM [104]. The compensation method was proposed as well.

Despite that the reverse recovery of a diode contributes to the switching losses of a converter, no impact was reported on the generation of conducted noise in the AC drives. In [105], the conducted noise of the power factor correction circuit was not affected by the diode reverse recovery as well. Moreover, modern SiC power devices have almost zero reverse recovery [7]. Therefore, this phenomenon of the switching behaviour is ignored further in the research.

The increased drain-source voltage overshoot and voltage oscillations are well-known problems of the modern power WBG power switches. The value of $\frac{\text{d}i}{\text{d}t}$ of modern WBG devices is very high. Hence, even the relatively small value of stray inductance in the commutation path can lead to a huge overshoot. This overshoot can be much higher than the breakdown voltage of a switch. As it was also shown in [102], an increase of stray inductance leads to the higher switching losses in a converter. Therefore, a lot of effort in the power electronics community is applied to the reduction of stray inductances [106, 107, 20]. All these works are aimed to reduce the stray inductance by means of a power converter layout. In [20],

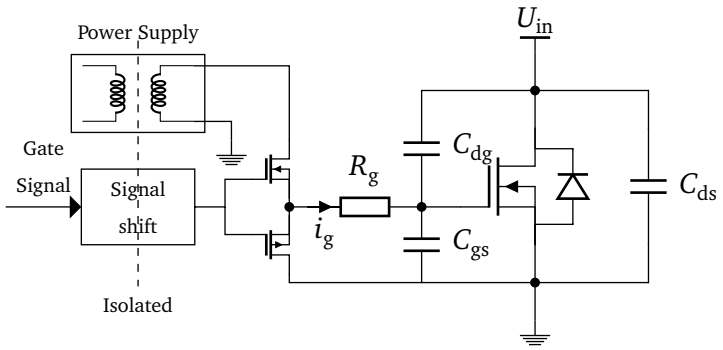


Figure 1.25.: Typical structure of MOSFET gate driver.

the impact of stray inductance on the EMI behaviour of a converter was studied as well. The reduction of conducted noise was shown under the optimised layout of a half bridge module with a reduced stray inductance. Due to the low value of stray inductance, the frequency of oscillations was increased (see Figure 1.24). However, the resulting frequency of oscillations was always (in case of normal and decreased value of L_Σ) outside of the range for conducted noise measurements. Therefore, the decrease of the noise was not observed for the considered standard.

According to the trapezoidal representation of PWM signal (see Figure 1.8), the low values of t_f are leading to the higher levels of conducted noise in RF. It is possible to regulate the duration of voltage rise/fall time by means of a gate driver [27, 94]. The operation principles of the MOSFET gate driver and its impact on the switching behaviour can be understood by means of Figure 1.25 where the simplified structure of a typical gate driver is shown. All drivers in a typical VSC have a signal shifter and power supply. Both components of the gate driver provide galvanic isolation. This isolation is necessary because the source of a high side MOSFET in inverter has a floating potential. The gate signal is transmitted to the MOSFET side through the signal shifter. The gate of a MOSFET is connected either to a positive potential or to the source using a small switching circuit base on P- and N-channel MOSFETs . Instead of the source, the MOSFET can be connected to the negative rail of the gate driver power supply (negative bias). This is done in order to ensure the off state of a switch [27].

The main parameters, which define the switching behaviour of a MOSFET, are also shown in Figure 1.25. These are gate resistance R_g, gate-source capacitance C_{gs} and drain-gate (Miller) capacitance C_{dg} [94]. R_g together with C_{gs} is responsible for the switching delay (the interval from t_0 to t_1, see Figure 1.24b) and for the drain current rise/fall time. Increase of these parameters will lead to an increase of the corresponding times. Gate resistance and Miller capacitance are responsible for the commutation time of drain-source voltage [27].

Despite that the voltage edges can be easily regulated with the value of R_g, such an approach is not preferable for the EMI behaviour improvement due to the increase of the switching losses. The total switching losses of VSC are defined by the PWM sampling frequency and by the energy which is absorbed by the MOSFET during the switching event. For the commutation shown in Figure 1.24b, the turn off losses can be defined using (1.19).

$$E_{off} = \int_{t_0}^{t_3} I_d U_{ds} dt \tag{1.19}$$

As can be seen, the increase of commutation times leads to an increase of the switching losses. The dependence of total switching energy loss and voltage fall time from the value of R_g were estimated experimentally for the designed VSC (see Chapter 3) and are given in Figure 3.7. Some intelligent structures for gate drivers were proposed in [108, 109, 21] for MOSFETs and IGBTs. The main idea of such drivers is to control actively the gate current i_g (see Figure 1.25) during the switching process. It allows to control separately the $\frac{dI_d}{dt}$ and $\frac{dU_{ds}}{dt}$ for turn on and off processes of a power switch. The gate driver with active control of i_g can be used to reduce the ringing effect (oscillations) or to decrease the losses even with increased voltage commutations times. However, the complexity of such drivers is very high.

This section is concentrated on the design activities which are applied at the last stage of VSC development. All these activities have an influence either on the shape of PWM voltage through the switching behaviour or on the impedance of a converter. It means that these techniques can be applied only to reduce the RF noise generated by the inverter in the AC drive. The switching behaviour, which defines the duration of commutation times, has an influence on the RF part of the PWM signal. The parasitics of a converter, which are defined by the layout and components selection, are relatively low. They start to influence the impedance on VSC only in the high-frequency range. Due to this reason, these hardware design activities were summarized and considered separately from such a design step as topology selection. The complexity of the problem is also discussed. Looking in the literature, it is hard to summarize all hardware design activities aimed at the EMI reduction. Most of the works are concentrated only on one single phenomenon. The first attempt is made in this section to structure all VSC design activities for the reduction of conducted EMI.

The switching behaviour of a SiC MOSFET is analysed in details regarding the output phase voltage. It is shown that commutation time can be defined either by the MOSFET itself or by its free-wheeling diode. At the same time, stray parameters show also a huge influence on the commutation process for the modern high-speed power switches based on WBG semiconductors. The switching behaviour can be also improved by means of the gate driver design. However, any increase of the commutation time leads to an increase of the switching losses in VSC.

1.5 Conclusion

This chapter describes firstly the standard which defines the conducted noise in the electrical equipment of an aircraft. According to it, the currents in the range from 150 kHz up to 152 MHz should be limited at all input and output cables of EUT. Then, the nature of conducted noise in the AC drives is presented according to the applied standard. It is indicated that the CM current provides the most significant influence on the noise level measured according to DO-160. However, some additional noise levels can be also observed due to the coupling between CM and DM. It is also shown that the problem of EMI generated by the inverter in the AC drive is increasing in modern power electronics. More energy of the PWM signal is shifted in the RF range with increased switching frequency and reduced commutation times in converters based on the WBG power switches.

The second part of this chapter presents different methods which allow the reduction or mitigation of the conducted EMI in the AC drives. The conventional EMI filters are very efficient but they can decrease the power density of the whole system including converter and filter itself. From the other side, it is

also possible to reduce the EMI by means of the inverter design. All these methods were structured and summarized in this chapter. It is shown that such techniques are only efficient in the particular frequency range. The drawbacks of such techniques are discussed e.g. increased complexity and/or losses of the power converter. However, all considered noise reduction techniques can be combined. Implementation of sophisticated topologies or PWM techniques can reduce the effort for the passive filtering of EM noise. Improved hardware design can be used to decrease the RF noise compensating the parasitics of EMI filters. The number of all possible design solutions for the EMI filters and for the inverter is very high. Therefore, the design methodology based on the experiments ("cut and try" method) is not efficient if all noise reduction techniques are taken into account.

2 Simulation of Conducted Noise in AC drives

The previous chapter explains the problem of conducted noise in the AC drives and shows the methods of its mitigation. For conventional power converters with low switching frequency, application of the EMI filters can give appropriate results with comparably low design effort. The effect of converter design on the conducted noise generation is normally neglected as it requires high effort to consider it. Improvement of EMI behaviour of a VSC can also lead to an increase of the losses and/or THD of the output current. For the power converters with low PWM frequencies, the EMI filters can be obtained in the lower dimension in comparison to the other parts of the converter. Hence, it is usually preferred to design the VSC with optimal performance (losses, THD and power density). Then, the EMI filters are implemented to reduce the measured generated noise to the required level.

The situation is different for the modern power converters. The size of power converters was significantly reduced in recent years due to new technologies. The most demonstrative example is the "Google Little Box Challenge" [4]. This competition gave a task to develop the smallest single-phase power converter for the solar application with power density higher than $3\,\mathrm{kW\,dm^{-3}}$. The competition attracted a lot of attention in the research community. Some promising results were achieved at the end of the challenge. The converter design solutions of the top competitors are described in [5]. The size of the DC link capacitors was reduced using active ripple control. Advanced topologies and control techniques were used to reduce the losses. At the same time, the size of the heatsink was also decreased with special thermal design methodologies. But the most significant improvement of the converter power density was achieved due to the application of new power semiconductors. All top competitors were using WBG materials (SiC or GaN) to design their converters [5]. The switching frequencies applied in the proposed converters varies from dozens of kHz up to 1 MHz. As it was explained in the previous chapter, the increase of commutation speed of WBG devices and the switching frequency of VSC leads to the higher levels of the conducted noise generated by the converter. The size of EMI filters becomes comparable with the other parts of the power converter. Therefore, consideration of EMI behaviour during the design of power converter is also taking more attention in recent years.

Using different structures and components for the EMI filter design, it is possible to optimize the power density of the filter itself. Such an approach was proposed in many research works [10, 13]. At the same time, some works propose to consider EMI during the optimization of a converter. In [22], the power density of an active front end was optimised taking into account the generation of EMI and different modulation schemes of 2- and 3-level converters. However, as topology and modulation techniques have an impact only on the LF part of the generated noise (see Section 1.4), the conducted noise was considered only up to 30 kHz.

In most optimization schemes of a power converter or an EMI filter, it is necessary to obtain a model which can estimate the level of conducted noise. This model is applied to check the EMI level in the system according to the chosen standard. However, a systematized approach for the simulation of conducted EMI is still missing in the area of power electronics. In order to take into account all noise

reduction techniques considered in Section 1.4 during the optimal design of a power converter, it is necessary to obtain the model which satisfies several criteria:

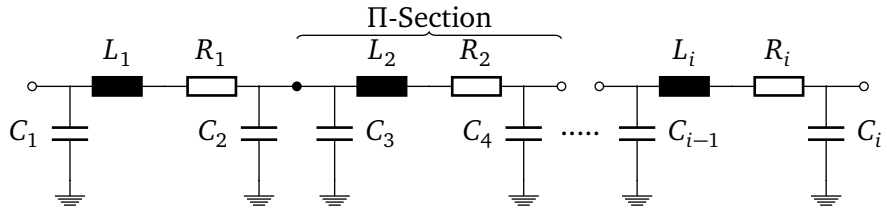
- The model for conducted noise prediction should be able to take into account the EMI filter as well as the converter itself. It should be possible to include all converter related noise reduction techniques.
- The model should be able to predict the noise in the whole frequency range because some noise reduction techniques have an impact on the LF, whereas the other techniques influence only the RF part of the conducted EMI.
- Both CM and DM noise should be included in the model. As it was explained in Section 1.4, some reduction techniques decrease the power of CM but at the price of DM. Moreover, coupling between modes can occur in the real system (see Section 1.3).
- The final and one of the most important criterion requires the low computational effort of the model in order to have the possibility to apply it later in the optimization procedure. Amount of different noise reduction techniques and its combinations is very high. Therefore, a small increase in the computation time will increase dramatically the duration of the design procedure.

This work is devoted to the development of the model, which meets the criteria stated above. The first part of this chapter gives an overview of the existing simulation techniques of conducted EMI in power electronics and particular in AC drives. Then, the basic mathematical tools applied for the simulation are described. More details are given on the converter representation. Finally, the whole model is described together with the calculation procedure.

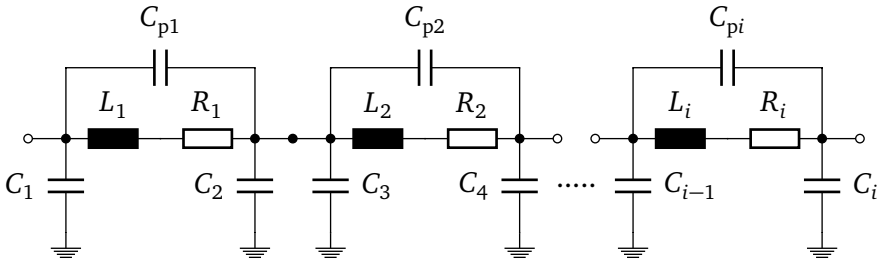
2.1 Existing Approaches

2.1.1 Time Domain

For control design purposes, time domain models are preferred by power electronics engineers. A lot of simulation tools such as PSpice, SimPowerSystem (toolbox for Matlab/Simulink), Saber, Plexim, etc. were developed and successfully applied in power electronics. The time domain models were also applied for conducted noise simulation in [18, 110, 111, 112]. Such models can be easily integrated into existing simulation tools. Moreover, they can be used to include the precise model of a power switch with its non-linear behaviour. These models of power switches are often provided by the manufacturers. Due to the wide frequency range of analysis (up to 30 MHz), it becomes necessary to consider the stray parameters in the system (see Figure 1.6) which are ignored in the analysis for lower frequency ranges e.g. in the control system design. Moreover, it is required to consider the wave reflections in the transmission lines (cables). It can be done by means of distributed element models. Such models for cables and motors were used in [110] for the prediction of EMI behaviour in AC drives. A detailed description of RF models is given in [44]. In Figure 2.1, the single-phase models of the motor and cable are presented for the high-frequency characterization.



(a) Single phase of a cable



(b) Single phase of a motor

Figure 2.1.: RF time domain characterization of different components in the AC drive.

The effect of the wave reflections was observed and studied away back for the 1st transmission lines i.e. for the telegraph [113]. Due to the wave reflection, voltage overshoot can be observed on the motor terminals in AC drives with long cable connection between the motor and inverter. Therefore, the first RF models were obtained for power cables in AC drives to evaluate the voltage overshoot on motor terminals [114]. Such a model is presented in Figure 2.1a. In [110], a similar model is used to simulate the power cable in time domain model for EMI prediction. It consists of the simple Π-sections. The required number of Π-sections are connected in a chain. The number of sections n depends on the cable length and the frequency range of consideration. The model in Figure 2.1a can be fitted to describe the behaviour of the AC motor in RF as well [110]. However, in [44], the RF description of the motor was improved considering the capacitance between the turns of the stator winding (C_{pi} in Figure 2.1b). The difference between two models (for cable and motor RF description) lies also in the value of series inductance L_i. The inductance of the motor is much higher. In order to consider the DM, the capacitances between phases and mutual inductances should be added in each section. Such models can be obtained from the measurements using conventional impedance analyser. However, it is required to conduct the fitting procedure of the model parameters in order to obtain the same impedances on the whole frequency range [44]. The fitting procedure can be a difficult task for the complex multiphase components. The fitting procedure can also introduce an error in the simulation if the circuit does not correspond to the physical structure of the motor.

As can be seen from Figure 2.1, the number of parameters, which should be considered in the simulation, increases with frequency. The simulation time step should be decreased with frequency increase as well. All this lead to a very high computational effort of the time domain models [115]. Moreover, it becomes hard to provide convergence of such models. This complicates the simulation process and violates one of the criterion stated above (low computational effort). Therefore, time domain models are not considered further in this work.

2.1.2 Frequency Domain

Due to the reduced computational effort, a lot of attention is attracted by the frequency domain approach for the simulation of conducted EMI. The 1st frequency domain models for AC drives were presented in [116]. It was proposed to replace the power switches by the corresponding voltage sources. The converter, which consists of voltage sources, can be then split into CM and DM circuits. Several assumptions are made at this step: all components of the AC drive are symmetric meaning that there is no crosstalk between CM and DM, the DC link capacitance (C_{dc} in Figure 1.6) is high enough to provide a short-circuit for the DM currents. All other components of the drive (motor, cable and filter) are also divided into 2 separate models for CM and DM noise respectively. It becomes possible to use the corresponding impedances (DM and CM) of the components which can be measured directly. An example of the frequency domain circuits for DM and CM current calculation is given in Figure 2.2.

In both models for CM (see Figure 2.2a) and DM (see Figure 2.2b), all components besides the VSC are characterised similarly. The LISN and motor are represented by the respective impedances. These impedances can be measured directly using impedance analyser. The DM impedance is just an impedance measured between phases. For the CM impedance, it is necessary to short-circuit all phases and to measure the impedance between phase and ground [44]. The cables can be simulated in various ways. In [116], transmission line equations were used for the output cable in the CM model. The simple Π-section was used in the DM model. It is also possible to use the 2-port networks as it is shown in Figure 2.2. The VSC in the model for CM model is represented by a voltage source and stray capacitance in Figure 2.2a. The voltage source is just an output CM voltage which can be found using (1.8). In the model for DM, the VSC is characterised using stray inductance of the DC link capacitance (ESL) and voltage source. The voltage source (U_{dm}) is calculated according to the states of VSC. The definition of U_{dm} was described in [116].

The voltage sources are defined in the frequency domain by their spectrum. The Fourier transform can be applied to the measured or to the simulated VSC output voltages in the time domain in order to find the required spectrum. The currents in RF, which are defined as noise according to DO-160 (see Section 1.1), are calculated for each frequency using simple numerical equations in a step-by-step manner. The proposed models have a relatively low computational effort. Moreover, the numerical values of measured impedances can be used without the fitting procedure. However, the accuracy and the frequency range of the 1st frequency domain models is also low because the representation of the most components was oversimplified during the analysis. For example, the motor was represented by a simple capacitor. The spectrum envelope of a trapezoidal signal was used to calculate the voltage sources in [116]. Therefore, more accurate but similar frequency domain models were proposed in the different research works. In [42], the measured 2-port networks were used to describe all components of an AC drive beside the VSC. Only CM model was considered as it is the most significant contributor to the conducted noise in the AC drives. However, the VSC was still represented only by its stray capacitance and the trapezoidal voltage source. The frequency range of simulations was extended up to 5 MHz [42].

The computational time of the frequency domain models is much lower than of the time domain models. Moreover, additional steps such as circuit fitting can be avoided because the measured impedances can be used in the frequency domain models directly [116]. However, the problem of such models lies

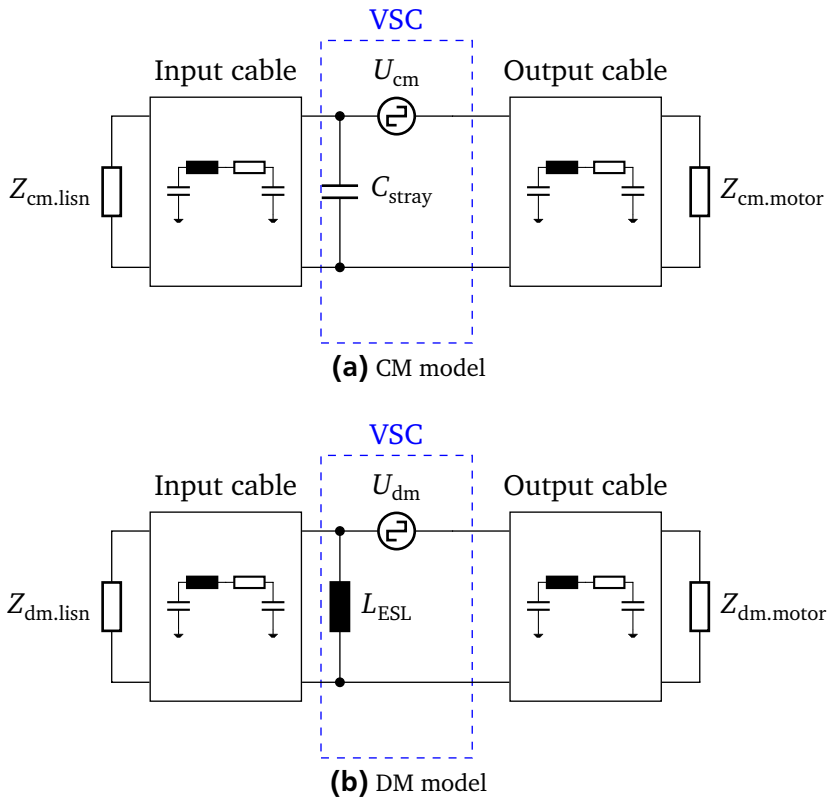


Figure 2.2.: The simplified CM and DM circuits of AC drive for conducted EMI simulation.

in the characterization of VSC, as it is a non-linear part of the system. A simple characterization of VSC with a single stray capacitance and voltage source gives low accuracy for the higher frequencies [117]. Therefore, another representation of converter was developed for the frequency domain models.

Behavioural Characterization of VSC

Because power converter is a switching device which changes its structure during the operation (in time), the VSC of AC drive is non-linear part of the system. Therefore, it is difficult to characterize the VSC in the frequency domain. Moreover, it is not always possible to measure the real parasitics of a VSC because they depend on the value of applied voltage (e.g. drain-source capacitance of MOSFET [27]). One solution was proposed in [118] for the EMI simulation of DC/DC converters. In [119, 120], this idea was adopted for the characterization of VSC for the switched-mode power supplies. In these works, an equivalent Norton circuit was proposed to represent the half-bridge of a power converter. This circuit is shown in Figure 2.3. It consists of two current sources I_{S_i} and internal impedance Z_{S_i} where i is a number of a power switch. The values of Z_{S_i} and I_{S_i} are not given. However, they can be found using the results of the supplement conducted noise measurements. Because all other components (LISN, cables, etc) are given and can be measured in the frequency domain, it becomes possible to obtain the values of Z_{S_i} and I_{S_i} using fitting procedure [118]. Such a model of VSC does not consider the physics and structure of a converter. Therefore, it was called the behavioural model. In other research works, such an approach was also called the black-box model [121, 122].

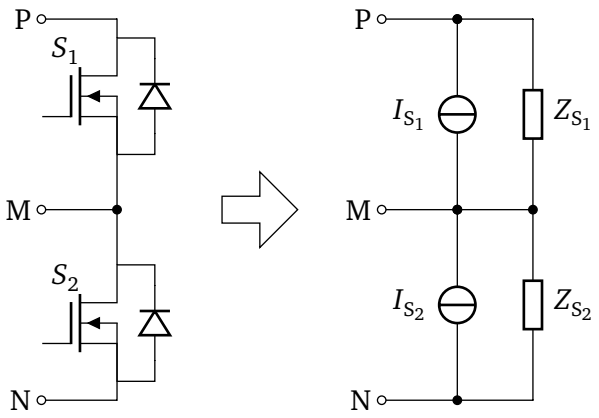


Figure 2.3.: Norton equivalent circuit of a half-bridge.

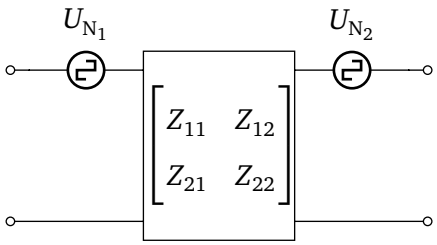


Figure 2.4.: Behavioural converter characterization for estimation of input and output CM noise.

The presented converter description can be also applied to predict the conducted noise generated by AC drives [122]. In that case, the impedances Z_{S_i} includes also the whole noise propagation path with the output cable and motor. However, the proposed behavioural approach can be applied to predict the conducted noise only at the input of VSC or on the LISN. It is enough for the most CISPR standards [123]. But according to DO-160 [24], which is observed in Section 1.1, the conducted noise should be measured on all input/output cables. New behavioural models, which can be used to predict the level of conducted EMI both at the input and output according to DO-160, were proposed in [124, 125]. In [124], separate behavioural models for DM and CM were obtained for the calculation of input and output conducted EMI. In [125], the VSC converter was characterised by a 2-port network and two voltage sources for input and output respectively as it is shown in Figure 2.4. The 2-port network was measured using the vector network analyser (VNA), whereas the voltage sources were obtained using results of conducted noise measurements according to DO-160.

The accuracy of the models proposed in [125] is high and covers the frequency range up to 30 MHz. The proposed model was used further for the optimization of EMI filters [11]. Despite all benefits of the behavioural converter characterization, such a model does not take the physics of VSC into account. The obtained behavioural model is fixed to the particular converter, PWM technique and operation point of an AC drive. Therefore, the behavioural models cannot be used to compare different designs of the converter (topology, PWM, gate drivers and layout). The behavioural characterisation of inverter violates another requirement stated at the beginning of this chapter - the ability to consider all possible methods of noise reduction in AC drive.

The VSC characterization proposed in the 1st research works dedicated to the frequency domain models is oversimplified [116, 42]. An improved VSC representation for the frequency domain models was proposed in [126, 127, 96]. In all these works, the noise propagation paths and/or voltage sources are considered more carefully. More attention is paid to the different stray parameters of a converter in [126]. The authors in [127] consider the whole AC drive system using matrix equations. In [96], the layout of a converter is taken into account using FEM. The spectrum of the voltage source is also improved including ringing effects and overshoot (see Section 1.4). All models are showing that it is possible to improve the accuracy and to extend the frequency range of the frequency domain models.

However, the frequency domain models proposed in [126, 127, 96] do not fulfil all requirements stated at the beginning of this chapter. The CM and DM were divided into separated circuits in [126]. Such a model cannot predict the noise if the coupling exists between CM and DM. In [42, 124], the coupling between modes was evaluated. It was shown that up to frequencies of several MHz the mode coupling can be ignored but it increases for the higher frequencies. Assuming the application of WBG power semiconductors, which are introducing more noise in the RF range, this problem can influence the simulation results. In [127], the trapezoidal representation of voltages source was improved, but some effects of the real switching behaviour were still neglected. The spectrum for voltage sources was obtained using the measured database with the real switching behaviour in [96]. However, this approach requires a lot of effort to consider different power switches and gate drivers.

It can be concluded that a new model is required for the conducted noise prediction in AC drives for the optimization of converter design. In order to ensure the low computational effort, this model should be based on the frequency domain approach. But this approach should be improved further to fulfil the criteria regarding the accuracy and coupling between DM and CM. A new model is proposed in this chapter with improved characterization of passive (motor, cable) and active (inverter) components of the AC drive. The theoretical background of applied improvements is explained in the next sections.

2.2 N-port Networks and Mixed Mode Parameters

The coupling between DM and CM (MM noise), which occurs due to the asymmetry of the real components, can be included into the frequency domain simulation by the improvement of the characterization of the passive components. In the originally proposed frequency domain models, the components were defined using simple unterminated impedances (see Figure 2.2). In [42], the components like cables and motor were represented by the 2-port networks. Utilization of 2-port networks provides the improvement of accuracy in comparison to the simple impedances. The graphical representation of the 2-port network of Z-parameters is shown in Figure 2.5.

The 2-port networks of Z-parameters are described by the matrices which correspond to (2.1). This network can be easily utilized with the existing frequency domain circuits ensuring the low computational effort. Depending on the circuit, it can be more comfortable to use Y-parameters in (2.2) or ABCD-parameters in (2.3). These parameters are used with the same graphical representation as in

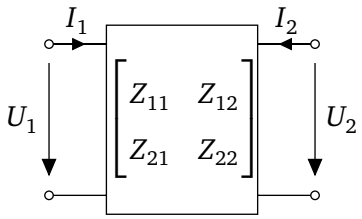


Figure 2.5.: 2-port network of Z-parameters.

Figure 2.5. Z- and Y-parameters are used with series and parallel connections of networks respectively, whereas ABCD-parameters are applied in the case of chain connection of networks.

$$\begin{bmatrix} U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2.1}$$

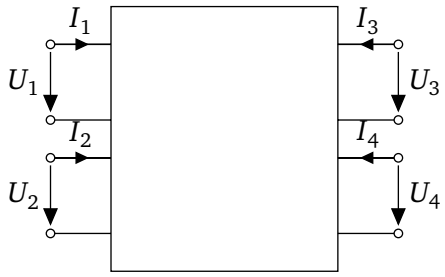
$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \end{bmatrix} \tag{2.2}$$

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} U_2 \\ -I_2 \end{bmatrix} \tag{2.3}$$

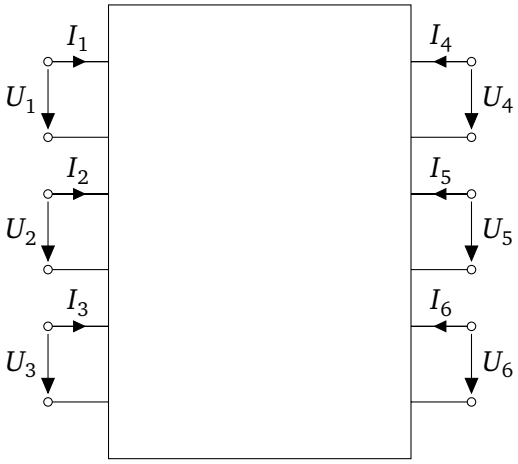
It is a well-known approach for the evaluation of current and voltages of RF systems. Such description can be also related to the black-box model as the inner structure of a component can be unknown. But the required parameters can be also obtained for the components with a known structure just solving equations (2.1)..(2.3). In [42], 2-port networks for CM voltage and current were proposed for the cable and motor description. The parameters were measured directly by means of the impedance analyser and injection probe. However, this approach does not allow to consider the noise coupling between DM and CM.

2.2.1 n-Port Networks

The theory of n-port parameters is widely applied in RF and communication engineering for the description of multi-line transmission lines [128]. These networks are an extension of 2-port networks with n ports and the corresponding number of voltages and currents. Considering systems with an equal amount of input and outputs, the n-port network is always described by n-by-n matrix (see (2.4) for Z-



(a) 4-port network for DC side characterization



(b) 6-port network for AC side characterization

Figure 2.6.: N-port networks of Z-parameters for characterization of AC drive components.

parameters). Similar as for the 2-port networks, it is also possible to obtain Z-, Y- and ABCD-parameters for the n-port networks.

$$\begin{bmatrix} U_1 \\ U_2 \\ . \\ . \\ U_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & . & . & Z_{1n} \\ Z_{21} & Z_{22} & . & . & Z_{2n} \\ . & . & . & . & . \\ . & . & . & . & . \\ Z_{n1} & Z_{n2} & . & . & Z_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ . \\ . \\ I_n \end{bmatrix} \tag{2.4}$$

The n-port networks can be applied to characterize the components of an AC drive for the simulation of conducted EMI. As can be seen in Figure 1.6, the VSC converter is supplied at the input with a bipolar power supply. Therefore, the 4-port network shown in Figure 2.6a can be used for the input DC side (input cable, EMI filter and LISN). The three-phase output of VSC consists of three individual lines. Considering 3 voltages between each phase and ground, the AC side can be described using 6-port networks (see Figure 2.6b).

The resulting 4- and 6-port networks are described with 4-by-4 and 6-by-6 matrices respectively according to (2.4). Similar as for 2-port representation, the Z-parameters of n-port networks can be easily converted to Y- and ABCD-parameters (see Appendix B). Therefore, the model can be built using these networks similar as in [42]. At the same time, the matrices of n-port networks describe the relationship between voltages and currents at all ports and between them. If the asymmetry between ports exists in the real system, it will be then taken into account.

The considered parameters can be also measured by means of a current injection probe as in [42]. Sinusoidal current with a particular frequency is injected at each port. Then, the amplitude and phase shift of voltage are measured on the corresponding ports. The ports are left open during the measurements. Each element of Z-parameters matrix can be then calculated using (2.4). However, some difficulties can

be observed during measurements in RF range with such an approach. Due to the wave reflections at the higher frequencies, the voltage cannot be measured appropriately because of the oscillations. Moreover, the condition of short- or open-circuit during the measurements of conventional parameters cannot be always ensured for the RF range. Therefore, the new parameters, which are called S-parameters, were developed by the engineers for the description of microwave systems [129, 130]. The principle of S-parameters is based on the transmission line theory and consider high-frequency effects. Moreover, the special devices called network analysers or VNA were developed to measure S-parameters.

Power waves and S-parameters

The scattering parameters (S-parameters) were introduced by Vitold Belevitch in his thesis [131]. The theory was further popularized among engineers in [129]. Instead of current and voltages, S-parameters are described using the power waves at each port i. These waves are defined by the equations (2.5) and (2.6):

$$a_i = \frac{U_i + Z_i I_i}{2\sqrt{|\mathrm{Re}\, Z_i|}} \tag{2.5}$$

$$b_i = \frac{U_i - Z_i I_i}{2\sqrt{|\mathrm{Re}\, Z_i|}} \tag{2.6}$$

where U_i and I_i are voltages and currents of i-port, Z_i is a reference impedance connected to each port. The power waves a_i and b_i are the incident and reflected waves respectively. The power waves are applied to build a new set of parameters, namely S-parameters. These parameters for the n-port network are described by (2.7):

$$\begin{bmatrix} b_1 \\ b_2 \\ . \\ . \\ b_\mathrm{n} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & . & . & S_{1\mathrm{n}} \\ S_{21} & S_{22} & . & . & S_{2\mathrm{n}} \\ . & . & . & . & . \\ . & . & . & . & . \\ S_{\mathrm{n}1} & S_{\mathrm{n}2} & . & . & S_{\mathrm{nn}} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ . \\ . \\ a_\mathrm{n} \end{bmatrix} \tag{2.7}$$

The S-parameters is a very powerful tool for systems which are operated with RF. They provide the possibility to calculate directly such essential parameters in microwave engineering as reflection coefficient, insertion loss, voltage standing wave ratio, etc. The S-parameters can be measured directly making characterization of microwave components easier. It is more comfortable at RF to provide the connection of each port to the reference impedance rather than to ensure the short- and open-circuit conditions. The reference impedance is always made equal to the wave impedance of the source and receiver of the measurement device in order to avoid reflections in the measurement device itself.

The first devices for measurements of S-parameters appeared at the beginning of the '60s. In such a device, the incident wave is generated by a sinusoidal source, whereas the reflected wave is normally measured using the directional coupler and heterodyne receiver directly in the frequency domain. The 1st devices capable to measure the amplitude and phase of S-parameters appeared at the beginning of the '80s. These devices are called vector network analysers [132]. As S-parameters can be measured in the RF range, they are widely applied for the characterization and design of EMI filters [133, 134]. S-parameters are also used to determine the insertion loss on the whole frequency range of the designed EMI filter [135].

Because the conducted EMI in AC drives is related to the currents and voltages, it is hard to apply the S-parameters directly in the frequency domain simulation. The relationship between conventional and S-parameters is also given in [129]. The Z-parameters can be found from S-parameters using (2.8):

$$\mathbf{Z} = \mathbf{F}^{-1}(\mathbf{I}-\mathbf{S})^{-1}(\mathbf{SG}+\mathbf{G}^{*})\mathbf{F} \tag{2.8}$$

where $\mathbf{I}$ is a unity matrix, $\mathbf{F}$ and $\mathbf{G}$ are the diagonal matrices which elements are equal to $\frac{1}{2\sqrt{|\mathrm{Re}\, Z_i|}}$ and Z_i respectively. Symbol $*$ indicates the complex conjugate transpose matrix. Using the equations from Appendix B, it becomes possible to obtain all types of conventional parameters as well. Using the required networks, the frequency domain model can be built for the prediction of EMI behaviour. This model includes the asymmetry between the lines (phases) due to the application of n-port networks. Because S-parameters are used for the measurements in RF, such a model is more accurate in the high-frequency range.

Measurement of S-parameters

Due to the application of high-frequency signals during measurements of S-parameters, some care should be taken in order to obtain clean results. In the current research work, all elements of the system were measured by means of the VNA E5061B from the Keysight technologies. A detailed description of the device can be found in Appendix D. The applied VNA is only a 2-port device. But for the description of an AC side, at least 6 ports are required according to Figure 2.6. Using the superposition principle, it is possible to obtain n-port S-parameters only with a 2 port VNA. An example of 4-port measurements is shown in Figure 2.7. All ports should be connected with a reference impedance during the measurements. The value of reference impedance in the applied VNA is 50 Ω as it is designed for standard RF components. The ports, which are connected to VNA, are shunted with a reference impedance directly in the analyser.

For the connection of VNA ports shown in Figure 2.7, 4 components of S-parameters are measured with indexes 2 and 3. In total, there are n^2 components for a single n-port network. It is necessary to connect VNA with the other ports to measure the rest of them. Assuming the reciprocity of the measured network, it is possible to measure only diagonal and upper or lower components of the matrix. Another issue of the RF measurements lies in the appropriate connection between VNA and the measured equipment. The photos in Figure 2.8 are showing how the motor was measured for the studied AC drive.

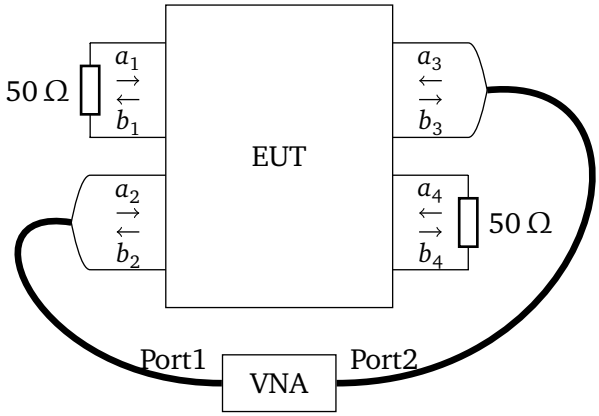


Figure 2.7.: Measurement of 4-port S-parameters

Figure 2.8.: The RF S-parameters measurements of the induction motor.

In order to keep the shielded structure of the motor, the cover was replaced with a copper plate. The copper plate was equipped with 6 SMA connectors which allows the connection between ports of the applied VNA and terminals of the motor. The measurement device was configured using the in-built calibration of the applied VNA. This calibration procedure includes only 2-port calibration. For the more accurate measurements, a special calibration should be provided assuming the error due to the coupling between ports [136]. Similar measurements were provided for the input and output cables. The measured S-parameters were converted into Z-parameters in order to use them in the frequency domain simulation.

2.2.2 Mixed Mode Parameters

The multiport networks can be used to analyse a system with asymmetry between phases. The conventional n-port networks operate with the phase currents and voltages. This type of currents and voltages is also called single-ended. However, the frequency domain models, which were considered in Subsec-

tion 2.1.2, operate with DM and CM voltages. As it was shown in [116], such a representation has computational benefits. The DM currents of DC and AC sides are assumed to be decoupled that provides simple linearisation of inverter for the analysis of AC drive. As it is also explained in Section 1.3, the decomposition on CM and DM is also helpful for the noise evaluation. Moreover, different conducted noise reduction techniques (see Section 1.4) influence in most cases only the dedicated mode. For example, the improvement of CM voltage in VSC can be achieved by means of the RCMV-PWM techniques. However, it can also lead to an increase of DM output voltage (see Subsection 1.4.3). Therefore, it is preferable to keep the representation of VSC with separated CM and DM similar as in Figure 2.2. In order to do it, a new approach for the characterization of AC drive components was developed within the conducted research.

The coupling between DM and CM is a well-known problem in the microwave differential transmission lines. Therefore, a so-called mixed mode S-parameters were presented in [137] to evaluate the crosstalk between modes in differential pairs. Firstly, it is necessary to define the differential and common mode power waves. For this, the current and voltages in (2.5) and (2.6) are substituted by those from (1.2) and (1.3). The resulting equations are:

$$\begin{aligned} a_{\mathrm{cm}} &= \frac{U_{\mathrm{cm}} + Z_{\mathrm{cm}} I_{\mathrm{cm}}}{2\sqrt{|\mathrm{Re}\, Z_{\mathrm{cm}}|}} \\ b_{\mathrm{cm}} &= \frac{U_{\mathrm{cm}} - Z_{\mathrm{cm}} I_{\mathrm{cm}}}{2\sqrt{|\mathrm{Re}\, Z_{\mathrm{cm}}|}} \end{aligned} \tag{2.9}$$

$$\begin{aligned} a_{\mathrm{dm}} &= \frac{U_{\mathrm{dm}} + Z_{\mathrm{dm}} I_{\mathrm{dm}}}{2\sqrt{|\mathrm{Re}\, Z_{\mathrm{dm}}|}} \\ b_{\mathrm{dm}} &= \frac{U_{\mathrm{dm}} - Z_{\mathrm{dm}} I_{\mathrm{dm}}}{2\sqrt{|\mathrm{Re}\, Z_{\mathrm{dm}}|}} \end{aligned} \tag{2.10}$$

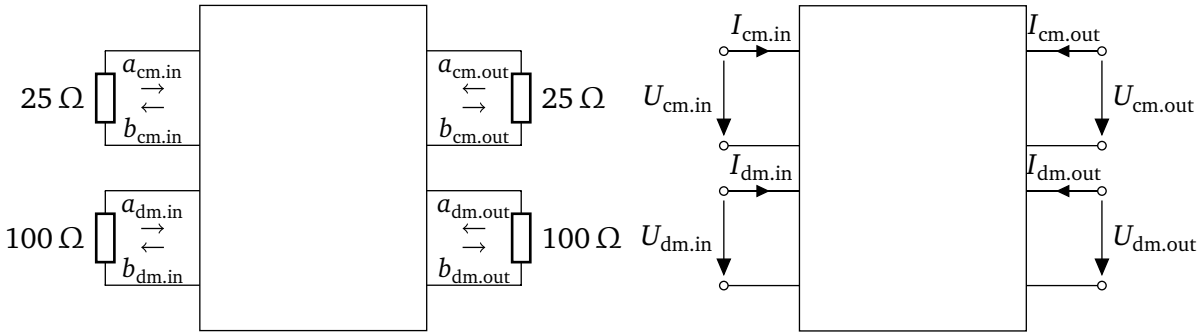
The corresponding reference impedances for CM and DM are equal to $\frac{Z_0}{2}$ and $2Z_0$ respectively. In this case all impedances Z_i from (2.5) and (2.6) should be equal to Z_0. Assuming a 4-port network from Figure 2.7, it is possible to define the similar network where incident and reflected power waves are associated with CM and DM. The relationship between single-ended and CM/DM power waves for the input of the 4-port network is defined by (2.11).

$$\begin{aligned} a_{\mathrm{cm}} &= \frac{1}{\sqrt{2}}(a_1 + a_2) \quad a_{\mathrm{dm}} = \frac{1}{\sqrt{2}}(a_1 - a_2) \\ b_{\mathrm{cm}} &= \frac{1}{\sqrt{2}}(b_1 + b_2) \quad b_{\mathrm{dm}} = \frac{1}{\sqrt{2}}(b_1 - b_2) \end{aligned} \tag{2.11}$$

Now, it is possible to convert vectors of the single-ended power waves a_{se} and b_{se} from (2.7) into the vectors of DM and CM waves. This results in (2.12).

$$[b_{\mathrm{se}}] = \mathbf{S}[a_{\mathrm{se}}] \rightarrow \mathbf{A}[b_{\mathrm{se}}] = \mathbf{ASA}^{-1}\mathbf{A}[a_{\mathrm{se}}] \rightarrow [b_{\mathrm{mm}}] = \mathbf{ASA}^{-1}[a_{\mathrm{mm}}] \tag{2.12}$$

In the case of a single differential line (4-port network), the transformation matrix $\mathbf{A}$ is equal to:



(a) 4-port network of MM S-parameters **(b)** 4-port network of MM Z-parameters

Figure 2.9.: 4-port networks of mixed mode parameters.

$$\mathbf{A} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 \end{bmatrix}$$

A similar transformation matrix can be also obtained for the n-port network where the number of individual differential lines is equal to $\frac{n}{2}$. Looking at (2.12), it becomes possible to define a set of new S-parameters which are called MM ($\mathbf{S}_{mm}$) parameters. These parameters can be easily calculated from the single-ended S-parameters ($\mathbf{S}_{se}$) from (2.7) by means of (2.13).

$$\mathbf{S}_{mm} = \mathbf{A}\mathbf{S}_{se}\mathbf{A}^{-1} \tag{2.13}$$

The matrix $\mathbf{S}_{mm}$ describes the MM S-parameters. The corresponding MM 4-port networks are presented in Figure 2.9. The 4-port network of MM S-parameters is shown in Figure 2.9a. As can be seen, the resulting network describes the relationship between input/output DM and CM power waves which are defined by (2.9) and (2.10). The corresponding reference impedances are also shown in Figure 2.9a.

The MM S-parameters can be easily converted into MM Z-parameters by means of (2.8). The resulted 4-port network is shown in Figure 2.9b. The corresponding 4-by-4 matrix describes the relationship between DM/CM currents and voltages at the input and output of a network. The respective components of the MM network can be also used to evaluate the coupling between modes. Using the superposition principle, it is possible to divide the 4-port network of MM parameters into several 2-port networks for different modes. For the proposed conversion, it is required to combine matrix components with indexes 1 and 3 in order to obtain the 2-port network for the CM. The components with indexes 2 and 4 can be used to build 2-port network for DM. The crosstalk between modes can be studied considering the components of the matrix with the mixed ports related to DM and CM e.g. 1 and 4.

The presented MM parameters are more comfortable for EMI analysis of systems with mode coupling in comparison to the single-ended parameters (see Figure 2.6). The MM parameters were proposed for

the characterization of EMI filters in [138, 139]. In [139], the MM parameters were used to obtain the mode transfer impedance Z_{TM} to predicted the conducted noise in the PFC circuit. In [124], these parameters are used to evaluate the coupling between modes where they were applied to the DC side of the AC drive. It was shown, that coupling is low and therefore can be neglected at lower frequencies. However, the coupling factor increases for the frequencies above several MHz. Hence, the MM noise cannot be ignored, if the conducted noise is evaluated in the whole frequency range. It also corresponds to the results obtained in [42] where the coupling between CM and DM was evaluated using current probe and noise separator.

The 4-port network of conventional parameters represented in MM can be used to combine the frequency domain circuits for CM and DM which are shown in Figure 2.2a and Figure 2.2b respectively. The idea is to replace the 2-port networks and terminated impedances with the corresponding ports of the 4-port network of MM parameters. In that case, it is possible to evaluate the CM, DM and MM noises simultaneously. Such an approach remains the simple representation of VSC (see Figure 2.2) with divided CM and DM reducing the computational effort of the EMI simulation. At the same time, the coupling or MM noise can be predicted in all other components of an AC drive (EMI filters, cables and motor).

2.2.3 MM Parameters for Three-Phase Systems

The original MM parameters, which were obtained for S-parameters, can be easily scaled to n independent differential lines [137]. The bipolar DC power supply of the studied system (see Figure 1.6) can be considered as a single differential line. Therefore, it is possible to apply the 4-port network of MM parameters from Figure 2.9b to components on the DC side such as input EMI filters, cable and LISN. However, the output (AC side) of the considered system is a conventional three-phase power line. This line cannot be treated as 3 independent differential lines because the 3^{rd} line is always in the dependence from others. Therefore, the conventional MM parameters should be extended for the three-phase systems in order to apply them for the characterization of components for conducted noise simulation. This extension was conducted during the research.

Some extensions of MM parameters for the three-phase components were proposed already in [41, 140]. In [41], the MM S-parameters are extended to the three-phase systems using the conversion to the symmetric components. The resulting S-parameters are applied for the analysis of the EMI filters. The authors in [140] proposed a new modal decomposition of the three-phase currents assuming that current DM_2 flows in one direction through phase A and back through the phase B. The MM parameters can be based on any linear transformation of the three-phase coordinates. Different well-known transformation of three-phase systems are considered and compared in Appendix A. It is shown that the simple transformation of three-phase voltages and currents into CM, DM_1 and DM_2 (see equations (1.5)..(1.10)) gives the possibility to couple directly the input and output mode currents. All other types of transformation require additional scaling or shifting of AC side currents in order to connect them with the input DC side mode currents. It means that the extensions of MM parameters based on other types of three-phase modal transform require the extension of the VSC model as well. Whereas, modal transformation considered in Subsection 1.3.2 gives the possibility to use VSC representation shown in Figure 2.2.

The transformation from phase currents/voltages into the three-phase CM/DM values is derived by means of equations (1.4)..(1.10). These equations can be written in the form of matrices (see (2.14) for currents and (2.15) for voltages). In order to transform vectors of single-ended voltages and currents into the vectors of MM values, it is required to multiply them with matrices **K** and **M** respectively.

$$\begin{bmatrix} U_{\mathrm{cm}} \\ U_{\mathrm{dm}_1} \\ U_{\mathrm{dm}_2} \end{bmatrix} = \mathbf{Ku}_{\mathrm{abc}} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} U_{\mathrm{a}} \\ U_{\mathrm{b}} \\ U_{\mathrm{c}} \end{bmatrix} \tag{2.14}$$

$$\begin{bmatrix} I_{\mathrm{cm}} \\ I_{\mathrm{dm}_1} \\ I_{\mathrm{dm}_2} \end{bmatrix} = \mathbf{Mi}_{\mathrm{abc}} = \begin{bmatrix} 1 & 1 & 1 \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix} \begin{bmatrix} I_{\mathrm{a}} \\ I_{\mathrm{b}} \\ I_{\mathrm{c}} \end{bmatrix} \tag{2.15}$$

Assuming (2.4) for 6-port Z-parameters, it is possible to obtain the transformation from single-ended to MM parameters using the same logic as in (2.12). The only difference is that this transformation is obtained for the conventional single-ended Z-parameters ($\mathbf{Z}_{\mathrm{se}}$). The matrix $\mathbf{Z}_{\mathrm{se}}$ can be obtained from the measured single-ended S-parameters using (2.8). The resulting equation for three-phase MM Z-parameters is (2.16):

$$\mathbf{Z}_{\mathrm{mm}} = \mathbf{T}_{\mathrm{u}} \mathbf{Z}_{\mathrm{se}} \mathbf{T}_{\mathrm{i}}^{-1} \tag{2.16}$$

where transformation matrices $\mathbf{T}_{\mathrm{u}}$ and $\mathbf{T}_{\mathrm{i}}$ were obtained in (2.17) and (2.18) using matrices **K** and **M**:

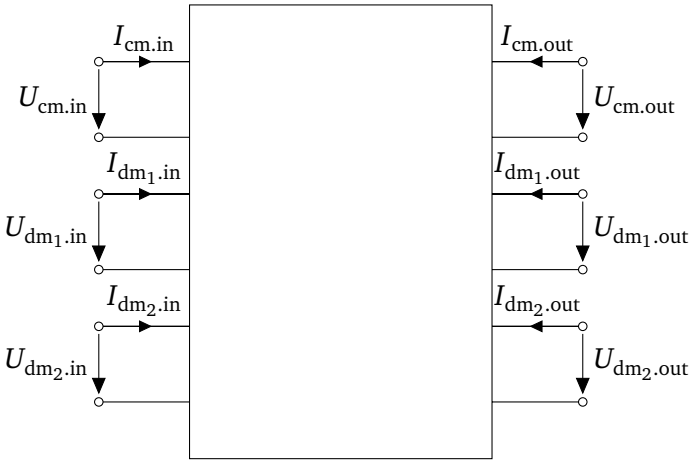


Figure 2.10.: 6-port network of three-phase MM parameters.

$$\mathbf{T}_{\mathrm{u}} = \begin{bmatrix} \mathbf{K} & 0 \\ 0 & \mathbf{K} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \end{bmatrix} \tag{2.17}$$

$$\mathbf{T}_{\mathrm{i}} = \begin{bmatrix} \mathbf{M} & 0 \\ 0 & \mathbf{M} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} & 0 & 0 & 0 \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix} \tag{2.18}$$

The resulting Z-parameters are operating with input/output currents and voltages of CM, DM_1 and DM_2. The corresponding network is shown in Figure 2.10. This network describes the input/output voltages and currents for each mode. It means that it is possible to replace the 2-port networks and unterminated impedances in Figure 2.2 with a proposed network at the AC side of the considered system. The description of VSC in the frequency domain remains the same keeping the computational effort of the model on the same level.

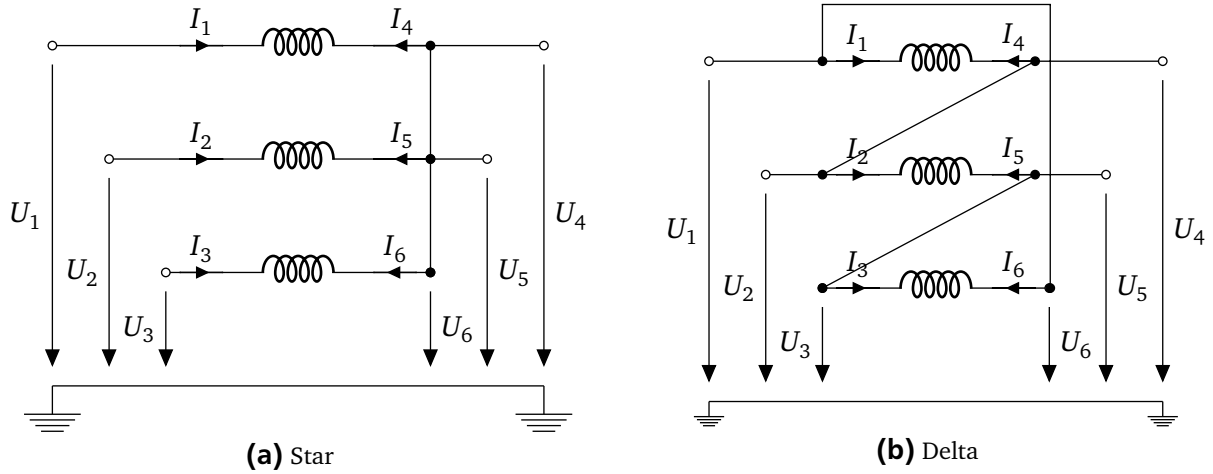
Delta and Star Connection of Motor:

The windings of a three-phase induction machine can be connected in star or delta. The selection of motor windings connection depends on motor design and nominal output voltage of VSC. Both cases can be found in the industrial AC drives. The connections of motor windings are shown in Figure 2.11. Both types of connections are shown in the relationship to the currents and voltages of a single-ended 6-port network (see Figure 2.6b).

In Figure 2.11a, the motor windings are connected in a star by short-circuiting the phases at the output. The midpoint (neutral) is not grounded. In that case, the phase voltage is applied to the motor windings. In the delta connection (see Figure 2.11b), the output phases are connected with the input neighbouring phases. It makes windings to be operated under phase-to-phase voltages. In both cases, the pins are floating to the ground. It means, that it would be difficult to apply single-ended 6-port networks for the motor description directly because classical networks operate with short and open circuits between terminals of the component and its ground. The short-circuit between pins of the different ports cannot be taken into account.

The proposed MM 6-port networks can be easily applied to the star connection of a motor. The DM_1 and DM_2 voltages are equal to the potential difference of neighbouring phases (phase-to-phase). It means that the corresponding 6-port MM network will have a short-circuit on the output ports for DM_1 and DM_2 for star connected motor (see Figure 2.10). Because the neutral point on the motor output is not grounded, the CM output of the respective network is assumed to be open-circuit during the calculation of the model.

However, the MM 6-port network from Figure 2.10 cannot be applied directly in case of motor windings connected in delta. It is possible to apply transformation from the delta into the star, but it requires knowledge about the exact circuit which mirrors the physical structure of the motor. In the considered case, the motor is characterized directly from the measurements. Its exact structure is supposed to be unknown (black-box). Therefore, it is necessary to find another way to describe the delta-connected motors. Using the same idea, which was previously discussed for the single-ended parameters and star-



(a) Star **(b)** Delta

Figure 2.11.: Possible connections of motor windings.

connected motor, it is necessary to define another set of MM parameters. These parameters should be suitable for the delta connection. It means that voltages should be redefined according to the short-circuited terminals in Figure 2.11b. In that case, the DM voltages are defined between the output phase and the input neighbouring phase. The resulting equation for output DM voltages is (2.19):

$$\begin{bmatrix} U_{\mathrm{dm}_1} \\ U_{\mathrm{dm}_2} \\ U_{\mathrm{dm}_3} \end{bmatrix} = \mathbf{K}_{\Delta}\mathbf{u} = \begin{bmatrix} 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 1 & 0 \\ -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ U_4 \\ U_5 \\ U_6 \end{bmatrix} = \tag{2.19}$$

The voltage DM_3 is introduced in order to take into account all pins, which are short-circuited in delta connected motor (Figure 2.11b). From the other side, input side of the MM 6-port network should remain the same in order to have the possibility to couple with other MM networks (the output cable is connected in the chain with the motor). Using the same idea as in (2.14)..(2.18), the voltage transformation matrix for delta connected motors is obtained in (2.20).

$$\mathbf{T}_{\mathrm{u}.\Delta} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 1 & 0 \\ -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.20}$$

Unfortunately, the delta MM transformation matrix for the currents is not so obvious as for the voltages. However, it is possible to apply one condition which can be used to find the transformation matrix for the currents in the delta connected motors. Any transformation should keep the same value of power. It means, that the dot product of vectors for currents $\mathbf{i}$ and voltages $\mathbf{u}$ should be the same for single-ended and for MM values.

$$\mathbf{i}_{\mathrm{se}} \cdot \mathbf{u}_{\mathrm{se}} = \mathbf{i}_{\mathrm{mm}} \cdot \mathbf{u}_{\mathrm{mm}} \tag{2.21}$$

Applying transformation from the single-ended to MM vectors in (2.21) and replacing voltage vector using (2.4), it is possible to obtain another equation for MM Z-parameters:

$$\mathbf{i}_{se} \cdot \mathbf{u}_{se} \rightarrow \mathbf{i}_{se} \cdot \mathbf{Z}\mathbf{i}_{se} \rightarrow \mathbf{T}_i^{-1}\mathbf{i}_{mm} \cdot \mathbf{Z}\mathbf{T}_i^{-1}\mathbf{i}_{se} \rightarrow \mathbf{i}_{mm} \cdot (\mathbf{T}_i^{-1})^T\mathbf{Z}\mathbf{T}_i^{-1}\mathbf{i}_{mm} \tag{2.22}$$

Comparing transformations in (2.22) with (2.16), which is obtained for the star-connected components, the relationship between matrices of voltage $\mathbf{T}_u$ and current transformation $\mathbf{T}_i$ can be conducted:

$$\mathbf{T}_i^T = \mathbf{T}_u^{-1} \tag{2.23}$$

The previously obtained transformation matrices (2.17)..(2.18) are also fulfilling the condition in (2.23). Now, it becomes possible to find the transformation matrix for the conversion from single-ended to MM currents in delta connected motors:

$$\mathbf{T}_{i.\Delta} = (\mathbf{T}_{u.\Delta}^{-1})^T \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} & -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{2.24}$$

The resulting matrix for the current transformation from single-ended to MM for the delta connection of motor windings shows that the CM current is equal to the sum of all input and output phase currents. It means, that CM current is always short-circuited and independent from the impedances which are connected between the output ports of the MM network. Such effect of delta connections is used in the presence of 3rd order harmonics in the load (the 3rd order harmonics are also CM currents in the symmetrical three-phase systems). For example, the static reactive compensators with thyristor controlled reactors [27] are always connected in the delta.

The final 6-port network is similar to the already presented three-phase MM network (see Figure 2.10), except for the output CM port which is replaced by DM_3. This port corresponds to the phase-to-phase voltage between phases A and C. The delta MM 6-port network of motor should be short-circuited at all output ports during the simulation.

2.2.4 Conclusion on n-Port Networks and MM Parameters

This section presents the MM n-port networks for the characterization of the components of an AC drive beside the VSC for frequency domain EMI simulation. The passive components such as cables and motors are usually specified and cannot be improved in the AC drive regarding the EMI behaviour. It

means that there is no need to define electrical equivalent circuit of these components in order to have a link between their design and impedance. Therefore, it is possible to use a so-called black-box model. The black boxes can be then defined using the measurements results.

The 2-port networks were already applied in some models with separately considered DM and CM circuits of AC drive. They were used to replace the unterminated impedances. However, such an approach does not consider the crosstalk between CM and DM (MM noise). Therefore, it is proposed to use n-port networks instead. These parameters describe the relationship between current and voltage at all ports. The 4- and 6-port networks are proposed to be used for DC and AC side respectively of the considered AC drive system. Besides the classical Z, Y and ABCD-parameters, the S-parameters are presented in this section. They are based on the transmission line theory and describe the relationship between the incident and reflected waves on each port. This characteristic of S-parameters provides the possibility to measure the circuit in the RF range by means of VNA. The S-parameters can be easily converted to the other representations (Z-parameters or unterminated impedances).

The single-ended n-port networks cannot be directly applied to the classical frequency domain EMI simulation of an AC drive. Firstly, it is necessary to obtain an appropriate model for the VSC converter. In order to keep the simplicity and low computation effort which were obtained in the conventional frequency domain models of AC drives, it is proposed to use the MM parameters. These parameters were originally obtained for S-parameters for the characterization of microwave differential pairs. Such parameters describe the relationship between the DM and CM current/voltages of a network. The respective ports of the MM network can be used to replace the 2-port networks in the widely applied frequency domain models for AC drives.

In summary, application of MM parameters have the following benefits:

- Reduced computational effort due to the frequency domain nature of n-port networks. The fitting procedure is not required because n-port networks can be measured and applied directly in the frequency domain models.
- Good accuracy of EMI simulation in the RF range. The n-port networks can be measured in the form of S-parameters which are suitable for the RF measurements.
- The coupling between CM and DM can be taken into account.
- Model of VSC can remain the same as in conventional frequency domain models of AC drives.

Finally, the MM parameters are extended to the three-phase systems for the characterization of AC side components. Both types of motor windings connection (delta and star) can be considered with the proposed extension. Using the proposed approach, the MM parameters can be easily applied to any multiphase system considering any possible connection between phases.

2.3 Improvement of Converter Representation

The method for characterization of passive components in the AC drive is discussed in the previous section. However, the proposed MM parameters cannot be easily applied for the characterization of VSC. As it was mentioned before in Section 1.4, the noise transmitter (VSC in the AC drive) is an

active component which is represented by the voltage source (U_s) and impedance (Z_s) during the EMI simulation. Such representation is also reflected in the simplified frequency domain models. However, the converter representation was oversimplified in the 1st frequency domain models of AC drives [116, 117, 42]. Some improvements of converter representation, which were proposed already in [126, 127, 12], do not cover all requirements listed at the beginning of this chapter. Therefore, it is necessary to improve the converter characterization. This section presents the improvements of VSC model in the frequency domain. The 1st part of the section provides the analysis of the output voltage of the inverter based on SiC MOSFETs. It presents also a new algorithm which allows the generation of time domain data for estimation of PWM voltage spectra. The 2nd part presents the most significant stray parameters of the designed inverter. Consideration of these parameters improves the impedance of VSC in frequency domain simulation.

2.3.1 Voltage Source

It is required to estimate the spectrum envelope of the respective voltages (CM and DM) for the calculation of frequency domain models. In some models [116, 42, 126], the actual voltage is replaced by the trapezoidal signal with the respective amplitude, period, duty cycle and rise/fall times. The corresponding spectrum envelope is also considered in Figure 1.8 in order to explain the relationship between VSC parameters and generated conducted EMI. However, this approach does not take into account various conducted noise reduction techniques which were considered in Section 1.4.

As it was proposed in [116], the spectrum envelope of the respective voltage can be obtained by means of the Fourier transform applied to the measured voltage in the time domain. The required data can be also generated using time domain simulation such as SPICE. In the case of the measured values, the model is fixed to the particular design of VSC. An intermediate approach is presented in [12]. This approach assumes the generation of PWM voltage in the time domain using simulated PWM signal convoluted with a database of the switching characteristics of an IGBT. The database contains only the commutation events during on and off. It can be acquired using simulation or measurements results. The resulting spectrum envelope takes into account lots of parameters: control strategy and PWM techniques, sampling frequency, dead-time, switching behaviour of IGBT. The results can be easily adapted for the various PWM techniques. However, the proposed methodology requires the accumulation of specific databases. The measured values are still applied in the provided work. Moreover, only the switching behaviour of IGBTs is taken into account. Such an approach does not provide a link between the switching behaviour of IGBT and the spectrum envelope of PWM voltage. Therefore, it is difficult to evaluate the influence of gate drivers and VSC design on the generated EMI. In order to see how switching behaviour influences the output voltage fall and rise times, a comprehensive analysis of PWM voltage is required for the inverter based on SiC MOSFETs.

Analysis of PWM Voltage in VSC Based on SiC MOSFETs

As it was discussed in Subsection 1.4.4, the switching of the output voltage can be provided either by the body-diode (external free-wheeling diode if it is applied) or by the MOSFET itself depending on the sign of the phase current at the beginning of the commutation process. In the case of MOSFET

commutation, voltage rise and fall times are defined by the MOSFET itself and by its gate driver. Duration of edges during diode commutation is defined by the value of phase current and by the drain-source capacitance. The logic from Figure 1.24b can be applied to the timing diagrams of the respective PWM technique. The timing diagram of the symmetric SVPWM can be observed in Figure 1.21a as an example. The first edge of voltage DM_1 is caused by the transition from the switching vector $\vec{V}_0$ to $\vec{V}_1$. According to the timing diagram, the switch S_2 should be turned off first. Then S_1 should be turned on after the dead-time. In that case, the current in phase A (I_a) defines which type of commutation takes place. The current I_b defines the type of the output voltage commutation for the next falling edge of DM_1 because commutation occurs in phase-leg B (transition from vector $\vec{V}_1$ to $\vec{V}_2$ according to Figure 1.21a).

This behaviour can be observed during the whole fundamental period of the VSC output voltage. As it was also explained in Subsection 1.4.4, the duration of the particular fall or rise time depends on the instantaneous value of the output current during the switching process. The fall/rise times (t_f and t_r) were evaluated for the output phase-to-phase voltage (DM_1) for the experimental VSC which is described in Section 3.1. The PWM voltage corresponds to the operation under symmetric SVPWM with a switching frequency of $f_s = 24\,\text{kHz}$. The motor was operated in the idle mode with relatively low output currents. The shape of PWM voltage DM_1 was measured at the output of VSC by means of the high-resolution oscilloscope (see Appendix D). The voltage waveform with a time span equal to the fundamental period is presented in Figure 3.8. The shape of PWM voltage during the whole period does not present any useful information. However, all edges (rising and falling) of PWM voltage were calculated using the obtained data. The commutation times with respective phase currents are shown in Figure 2.12. As can be seen, the output currents correspond to an ideal sine waveform with some ripples and low order harmonics. The amplitude of the fundamental part of output current is equal to 7.7 A. Due to the idle mode operation, the fundamental part of the output current (I_a) is almost pure reactive with phase shift equal to 90°.

The respective fall and rise times (t_r and t_f) of voltage DM_1 are shown on the graphs below the phase currents in Figure 2.12. For each switching event, the values of the respective commutation times are scattered on the graph. Some points are coloured in red. These are the switching events which occur during zero-crossing of the output current (see Figure 2.16). These special points will be discussed later in this section. As can be observed in Figure 2.12, rise and fall times are equal to 45 ns during the most switching events. This value corresponds to the applied gate resistance $R_g = 15\,\Omega$ for the current experiment (see Figure 3.7). However, some edges are taking different values in the range between 45 ns and 100 ns. This behaviour occurs due to diode commutation. As it was discussed in Subsection 1.4.4, voltage rise/fall time ($t_3 - t_2$ in Figure 1.24) is defined by drain-source capacitance and by the value of phase current during the diode commutation. This time is required to charge or to discharge the capacitance C_{ds} by the respective current. The simplified equation for fall/rise time during diode commutation is:

$$\Delta t = \frac{C_{ds} U_{dc}}{I_{t_0}} \tag{2.25}$$

where I_{t_0} is the value of phase current at the beginning of the switching process. It can be observed that the duration of fall/rise time is inverse proportional to the phase current.

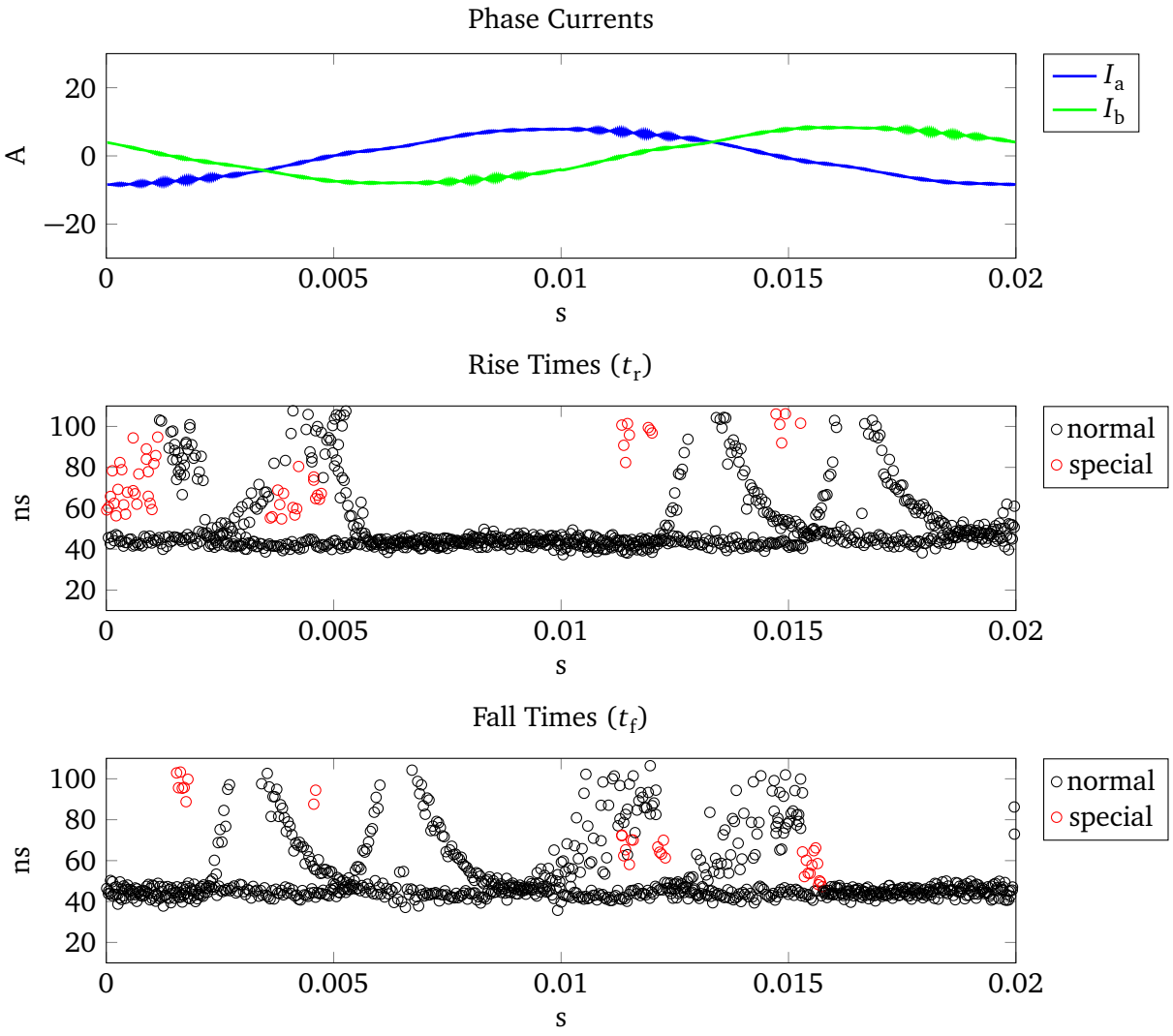


Figure 2.12.: Rise and fall times of PWM voltage U_{ab} (DM_1) with motor in idle mode during one fundamental period.

The falling and rising edges of the phase-to-phase PWM voltage were also evaluated for the operation of the motor under the load of 7.5 kW. The shape of the PWM voltage on the fundamental period was the same as in Figure 3.8. The durations of falling and rising edges were also evaluated for the operation under load. The respective results are shown in Figure 2.13. As can be seen, the amplitude of the phase current is equal to 20 A. Due to the presence of active power in the load, the resulting phase shift between PWM phase-to-phase voltage and I_a was reduced to 45° in comparison to the idle mode operation (see Figure 2.12). Similar to the PWM signal under operation of the motor in the idle mode, some edges have almost the same duration equal to 45 ns. The respective switching events are associated with the MOSFET commutation as the value of R_g is the same as in Figure 2.12. But commutation times with variable duration are taking values between 25 ns and 110 ns in Figure 2.13. The minimum value of voltage fall and rise times is reduced to the value which is lower than the commutation time of MOSFET. This is due to the increased values of phase currents according to (2.25).

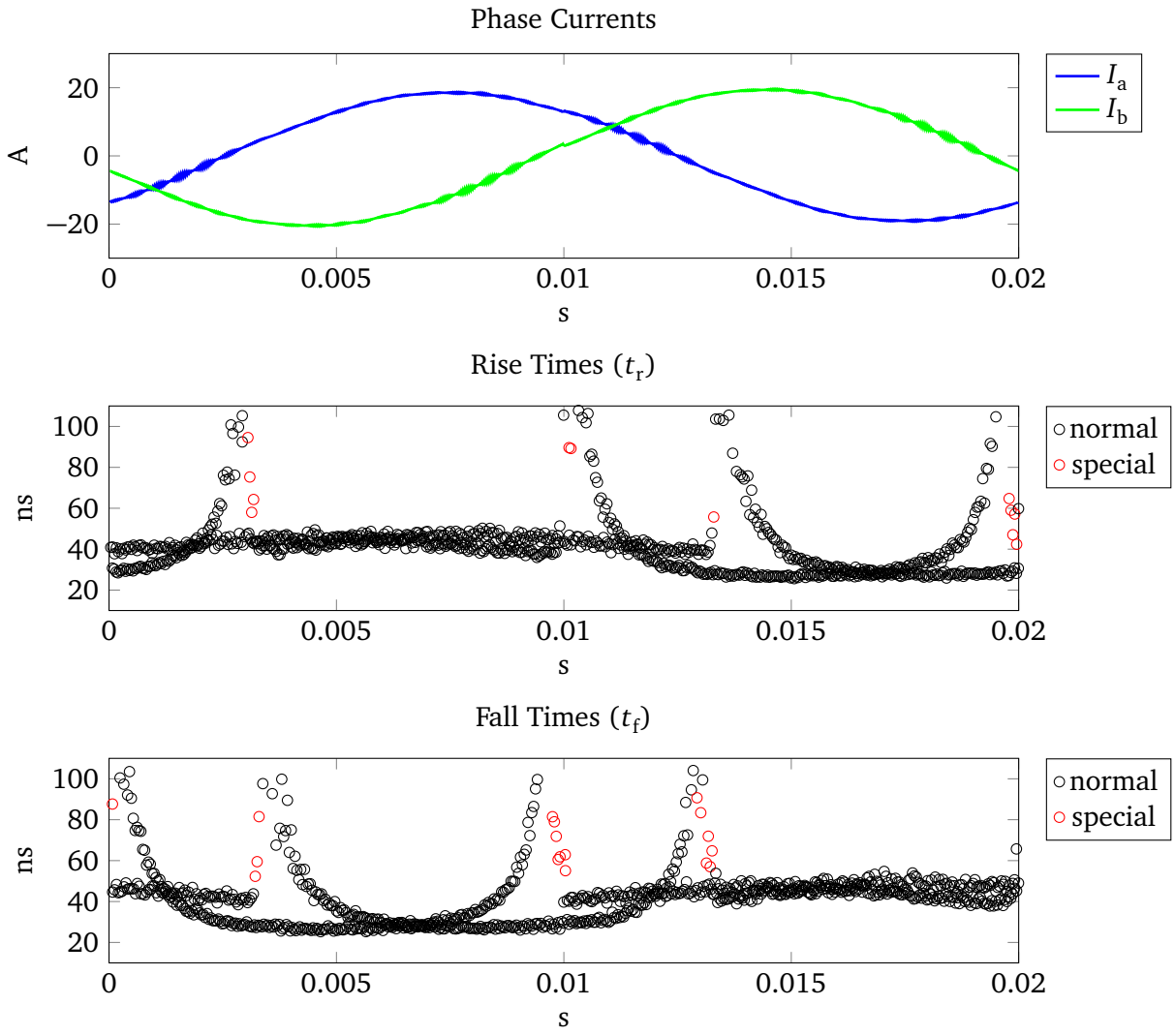


Figure 2.13.: Rise and fall times of PWM voltage U_{ab} (DM_1) with motor load of 7.5 kW during one fundamental period.

In both cases of motor operation, the highest values of t_f and t_r in the VSC output line voltage are observed near zero-crossing of the phase current. Moreover, diode commutations can be recognized as commutation times with variable durations repeating the shape of cosecant ($\frac{1}{\sin(x)}$) function. Such behaviour corresponds to (2.25). Influence of the switching behaviour on the spectrum of PWM voltage is considered further in Subsection 2.4.2. The considered behaviour of edges in the PWM signal can be simulated using precise models of the power switches. But it would be a time-consuming process. In order to reduce the computational effort, a simplified algorithm is proposed to generate time domain PWM signal considering the effect of diode commutations.

Generation of PWM Voltage in Time Domain

The impact of diode commutations on the fall and rise time of the output voltage was observed during the measurements. In the case of MOSFET commutation, the switching time is relatively stable and is only defined by the gate resistance R_g (see Figure 2.12 and Figure 2.13). In the case of diode commu-

ation, the value of rise/fall time can be estimated using (2.25). All parameters in (2.25) can be easily obtained except the value of drain-source capacitance. The value of C_{ds} is influenced by the MOSFET itself, by the parasitic capacitance of PCB and by the external free-wheeling diode, if the later one is applied (the capacitance between anode and cathode C_{ac} of the free-wheeling diode). The capacitance of semiconductor devices such as power MOSFET and diode shows a non-linear behaviour. This capacitance depends on the value of applied voltage $C(u)$ [27]. Therefore, it is more comfortable to replace the capacitor C_{ds} in (2.25) with a drain-source charge Q_{ds} that leads to equation:

$$\Delta t = \frac{Q_{ds} + Q_{ac}}{I_{t_0}} \tag{2.26}$$

where Q_{ds} and Q_{ac} are the charges which are formed by the MOSFET and by the free-wheeling diode respectively. The stray capacitance of PCB is ignored in (2.26). Q_{ac} should be considered only in the case then external diodes are applied in the design of VSC. Both charges can be calculated using (2.27):

$$Q_{ds} = \int_{V_f}^{U_{dc}} C(u)du \tag{2.27}$$

where V_f is a forward voltage drop of the applied free-wheeling diode (body diode). The resulting integral can be calculated numerically using the graphs of the respective capacitances for MOSFET and diode. This data can be found in the datasheet [141, 142]. Taken into account the effect of diode and MOSFET commutation, it is possible to generate numerically the PWM signal in the time domain. This signal would be an approximation of the real output PWM voltage.

The algorithm for the numerical PWM signal generation is shown in Figure 2.14. The algorithm considers different operation points of an AC drive through the reference voltage (U_{ref}) and type of load which is observed by the VSC (active P and reactive Q components of the load). These parameters are also used to obtain the phase current (I_{out}). The phase current can be calculated using only the simple fundamental model assuming that the amplitude of I_{out} is defined only by the fundamental frequency (see also Figure 2.13). The reference voltage is also applied to generate the gate signals (switching events as in [12]). The PWM algorithm can be adopted from the simulation or directly from the software of VSC control system. The gate signals are also influenced by the other parameters of the control system such as PWM sampling time T_s (switching frequency), dead time t_{dt} and even by the system clocks of control system (f_{clk}). The value of clocking frequency defines the resolution of PWM.

As the phase current and gate signals are obtained, it becomes possible to define which type of commutation takes part during each switching event. If the output voltage is commutated by the MOSFET, the corresponding edge for the particular switching event can be taken from it turn-on switching characteristics. These characteristics are normally given in the datasheet [141, 142]. In the case of the diode commutation, the corresponding duration of rising or falling edges can be calculated by means of (2.26). The corresponding edges are added to the gate signals. The final signal should be scaled by the value of DC voltage obtaining the final waveform of the output phase voltage.

The presented algorithm should be calculated for each phase-leg of VSC. Using equations (1.8)..(1.10), the corresponding DM and CM voltage can be calculated as well. In order to apply them in the frequency

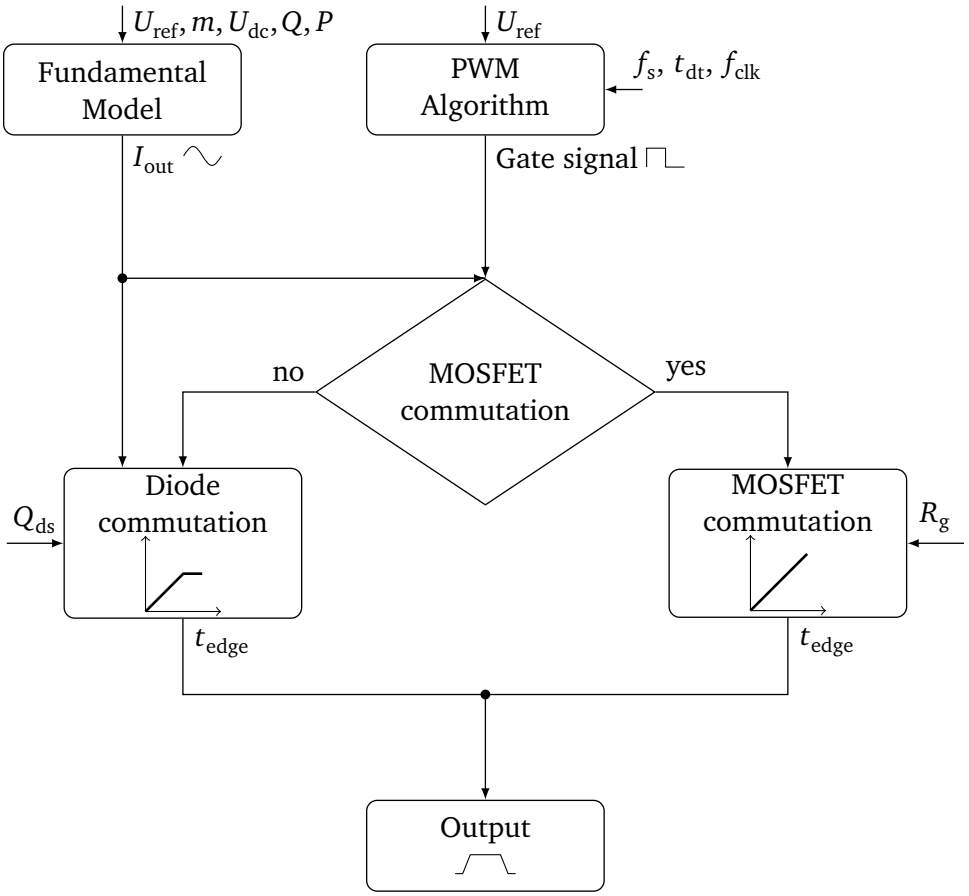


Figure 2.14.: Algorithm for the generation of output phase voltage with corresponding rise and fall times.

domain models (similar as in Figure 2.2), it is required to apply the Fourier transform to the generated signal in the time domain as it was proposed in [116]. This part is described in Subsection 2.4.2.

The proposed algorithm was used to obtain the DM_1 voltage. The generated waveform has the same shape as the real PWM voltage shown in Figure 3.8. The PWM voltage waveform was simulated assuming the operation of the motor under a load of $P = 7.5\,\text{kW}$ that corresponds to the experiment considered in Figure 2.13. The reactive power Q=4.5 kvar was calculated using motor parameters (see Table 3.2). The reference voltage was assumed to be a pure sinusoidal signal. The other parameters required for the generation of time domain data (m, U_{dc}) were taken the same as in the conducted experiments provided for the analysis above. The rising and falling edges of the generated PWM signal was analysed in the same manner as it was made before. The results are presented in Figure 2.15. The phase currents in Figure 2.15 have the same amplitude and phase shift as in Figure 2.13. But there is no ripples because only the fundamental parameters are used to obtain the phase currents in the simplified algorithm (see Figure 2.14).

Comparing the results of the analysis between the measured and simulated (Figure 2.15) PWM phase-to-phase voltages, it can be concluded that the proposed algorithm can be applied to replicate the behaviour of the PWM voltage. The behaviour of edges in the generated signal corresponds to the real output voltage of inverter based on SiC MOSFETs. The generated PWM voltage obtains the fixed rising/falling times during the MOSFET commutation. The edges with variable duration in Figure 2.15

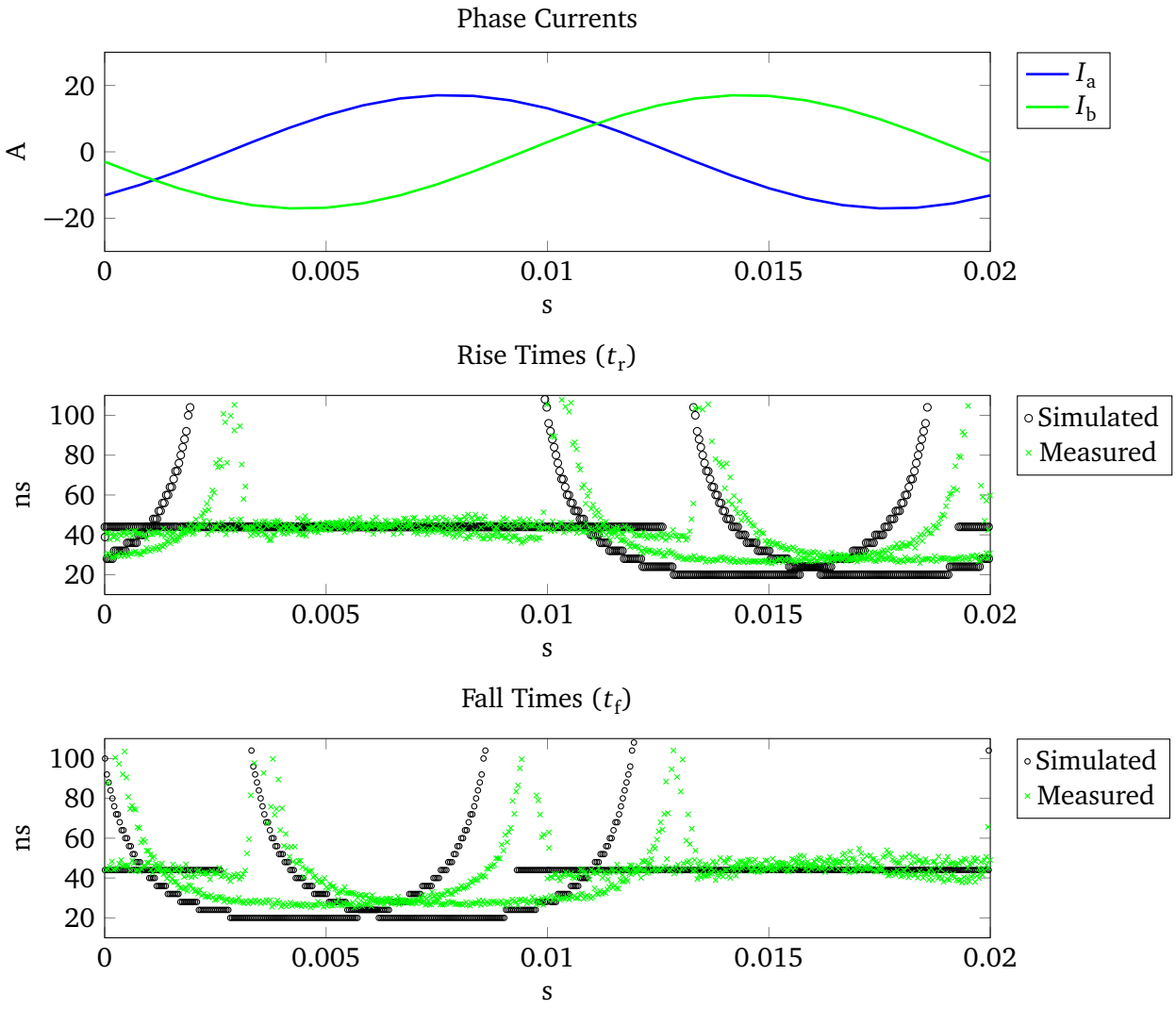


Figure 2.15.: Rise and fall times of simulated PWM voltage U_{ab} (DM_1) with motor load of 7.5 kW during one fundamental period.

(diode commutation) are also repeating the diode commutations observed in the measured PWM signal. Some deviations are presented due to the synchronization between the measured and simulated data. The drain-source charge was also obtained using the datasheet of applied power switches [141, 142]. The real value of Q_{ds} can be also different introducing an error in the proposed algorithm in Figure 2.14. The dependence between MOSFET commutation time and R_g was obtained from the measured values shown in Figure 3.7. However, a similar graph is also given in the datasheet [142].

The algorithm in Figure 2.14 can be easily applied with any type of PWM. It considers also the different operation points of an AC drive. The measured databases are not required even for the estimation of rise/fall time during MOSFET commutation. The proposed algorithm is very simple and requires low computational effort. Due to the linear relationship between gate resistance and commutation time of MOSFET, the value of R_g can be easily corrected. Therefore, it can be concluded that the developed algorithm can be easily applied to different converter designs. The proposed algorithm was implemented only for the conventional hard-switched FB inverter. However, it can be easily extended to the multi-level

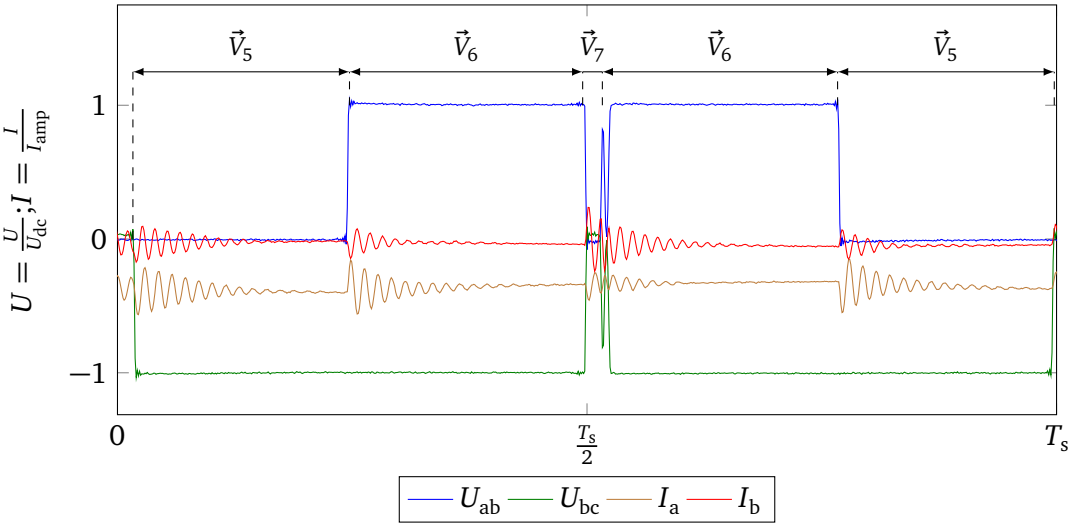


Figure 2.16.: Switching behaviour near current zero crossing.

topologies. For the soft-switching inverters, such an algorithm is not required because the shape of edges is defined by the topology of an inverter.

Diode Commutation Near Current Zero-Crossing

Some rising and falling edges of measured PWM voltage are not observed in the simulated PWM signal in Figure 2.13. These edges are highlighted with red colour in Figure 2.13 and Figure 2.12. It was mentioned before, that such commutations occur near or during the zero-crossing of the corresponding phase current. A closer look on this commutation is given in Figure 2.16 where the phase-to-phase voltages (U_{ab} and U_{bc}) and phase currents (I_a and I_b) are shown during one sampling period of symmetrical SVPWM $T_s = 41.7\,\mu s$. All voltages and currents are scaled to the reference values. The voltages are scaled to U_{dc}, whereas currents are scaled to the amplitude of the current of the fundamental frequency. Comparing the timing diagram of the symmetrical SVPWM (Figure 1.21a) with Figure 2.16, it can be concluded, that the reference voltage vector is allocated in the 5^{th} sector. The switching sequence starts from the zero vector $\vec{V}_0$. Then, it goes to active vectors $\vec{V}_5$ and $\vec{V}_6$. After the 2^{nd} zero vector $\vec{V}_7$, the sequence is repeated in the reverse order according to the principles of the symmetrical SVPWM.

The switching behaviour, which was not described in Subsection 1.4.4, is observed during the transition from $\vec{V}_7$ to $\vec{V}_6$. In that case, the second phase leg (phase B) of VSC is switched from positive to negative output voltage according to Table 1.2. The sign of current in phase B defines the type of commutation (diode or MOSFET). It can be observed in Figure 2.16 that the average value of I_b is almost equal to zero during the considered sampling period. As can be seen in Figure 2.16, the phase-to-phase voltage U_{ab} starts to rise and then it suddenly goes down and up once again. Such behaviour is observed due to several reasons. The current ripples in phase B were caused by the commutation during the transition from $\vec{V}_6$ to $\vec{V}_7$. Because the duration of $\vec{V}_7$ is very short, the ripples are presented in the current I_b until the next commutation. The commutation from $\vec{V}_7$ to $\vec{V}_6$ starts from the turn-off of high side MOSFET in phase B. Due to the ripples, current I_b is higher than the zero at the beginning of the commutation process ($\vec{V}_7$ to $\vec{V}_6$). Therefore, the diode of low side switch in phase B starts to commutate the output

voltage U_b to the negative rail according to Figure 1.24. Together with the commutation of U_b to the negative rail of DC supply, line voltage U_{ab} begins to rise and U_{bc} begins to fall. Due to the ripples, the current I_b crosses the zero value once during the rise of U_{ab} (fall of U_{bc}). During dead-time $t_{dt} = 500\,\text{ns}$ (see Table 3.3) both switches are in off state. The output voltage in phase B starts to commutate back to the positive rail through the high side diode after the current zero-crossing which was caused by the ripples. It makes voltage U_{ab} to fall back to zero value. The line voltage U_{bc} rises to zero value as well. After the dead-time, phase B is finally commutated to the negative rail through the MOSFET. The line voltages rise and fall back to the corresponding values: $U_{ab} = U_{dc}$ and $U_{bc} = -U_{dc}$. As can be seen in Figure 2.16, the switching of power MOSFETs near the zero-crossing can cause multiple commutations during the dead-time. The duration of the resulting edges is hard to predict because it depends on the ripples. The ripples are defined in turns by the parameters of motor and PWM.

If the instantaneous value of output current at the beginning of the switching process is higher than the amplitude of the ripples, there would not be any multiple zero-crossings during the dead time. If the duration between two switching instances is longer than the duration of current oscillations (ripples), such behaviour would not be observed as well. The frequency of ripples influences this phenomenon as well. A frequency increase of the ripples prevents the multiple rises and falls too. Comparing edges of phase-to-phase PWM voltage with the motor in the idle mode (Figure 2.12) and with the loaded motor (Figure 2.13), it can be observed that amount of such commutations is higher in the experiment under idle mode operation of the motor. This is due to the lower amplitude of phase current and the phase shift between PWM voltage and the phase current.

The presented above effect produces the falling and rising edges in the PWM voltage with a hardly predictable duration. However, the amount of these commutations is low in comparison to the commutations considered in Subsection 1.4.4. Moreover, the presented switching behaviour cannot introduce the rise/fall times with very short duration. All red points in Figure 2.12 and Figure 2.13 are above the commutation time of MOSFET (45 ns). It means that these commutations do not introduce the additional noise level. As can be also seen in Figure 2.16, the commutation near zero-crossing in the presence of the current ripples produces the voltages pulses with a duration equal to the half of the ripples period. These pulses can introduce an additional noise level at the frequency equal to the doubled value of the ripples frequency (approx. 3.6 MHz). However, no impact was observed during the measurements of conducted EMI (see Chapter 4).

Further Improvements

The proposed algorithm for the generation of time domain data of VSC output voltage (see Figure 2.14) does not take into account all the effects of the real switching behaviour (see Section 1.4). These effects are listed below:

- The voltage overshoot is ignored because no significant values were observed during the measurements of drain-source voltage. Moreover, the stray inductance, which influences the maximum value of voltage overshoot according to (1.17), can be reduced with an appropriate hardware design [106, 107, 20]. With a relatively low output phase currents, the overshoot would not con-

tribute to the level of conducted EMI. However, with a power increase of an AC drive, the impact of overshoot should be evaluated as well.

- The effect of drain-source voltage oscillations is also ignored in the conducted research. The frequency of oscillations is defined by the value of stray inductance and drain-source capacitance C_{ds} (see Figure 1.24). This frequency can be shifted out of the frequency range where conducted noise is defined. This can be done by means of the appropriate design with the reduced value of stray inductance [20].

- As it was mentioned already, the commutations which occur near zero-crossing of phase current are also neglected. In order to include such switching behaviour, it would be necessary to obtain phase currents in Figure 2.14 including high-frequency ripples. However, the amount of such commutations is very low (see Figure 2.12), especially in the operation mode with a motor under the load (normal operation of an AC drive). Therefore, such behaviour of the real PWM signal was also neglected.

All switching events define the shape of the spectrum envelope of the VSC output voltage in the RF range. The phenomena mentioned above are necessary to consider in order to extend the frequency range and accuracy of the frequency domain simulation. The generated time domain data should be then transformed into the frequency domain. However, the simple Fourier transform applied to the time domain data can not be used to predict the level of noise under a different type of detection. The proper spectral analysis of the VSC output voltage is presented in Subsection 2.4.2. It explains how to consider the effect of the spectrum analyser during the frequency domain simulation.

2.3.2 Converter Impedance

The characterization of VSC impedance for the frequency domain EMI simulation was improved in [12, 97, 96] by means of FEM simulation. Such an approach can be used to obtain a very precise model of VSC. However, it also requires huge computational effort. If all components of the VSC are considered during the FEM simulation, the computational time increases dramatically. In order to reduce the computational time of the model for EMI prediction, the analytical way can be used to describe the VSC, similar as it was originally presented in [116]. But the number of stray parameters should be increased in order to extend the frequency range of EMI simulation. In [116], the impedance of inverter Z_s is represented by two lumped parameters (capacitor and/or inductor) considering only the most significant parasitics. Amount of stray parameters for VSC characterization was increased in [42, 126]. However, some components were still missing in the proposed approaches. Moreover, the stray parameters, which define the impedance of a converter, are not concentrated at a certain point. Instead of this, they are spread on the whole PCB. An extension of the analytical approach for VSC converter characterization is provided in this section. For these purposes, the components of VSC are analysed indicating the main parasitics. The analysis is provided only for the CM because the DC link has the most significant influence on DM. Therefore, analysis of stray parameter for DM is not required. At the end of this section, a description of possible FEM characterization of VSC is considered as well and compared with the analytical approach.

As it was mentioned in Subsection 2.1.2, it is assumed that DM of VSC is short-circuited through the DC link capacitance. It gives the possibility to consider the simple model for the VSC in the frequency domain [116]. This assumption means that the output and input DM currents are decoupled. Such an assumption is usually fulfilled in the real VSC. Normally, the amount of DM capacitors at the DC side of VSC is not limited. Therefore, if such an assumption is violated, additional small capacitors with low ESL can be added in parallel to the DC link to keep the low impedance path for the RF DM currents. The stray capacitance C_{ds} of the power switches contributes to the DM capacitance of VSC as well. Moreover, as it was shown in Appendix A, the output DM current is partially short-circuited through the power switches as well. It means that the DM characterization of VSC can be the same as in the simplified frequency domain model in Figure 2.2b. The only relevant parameters here are the DC link capacitance and its stray inductance. The stray inductance is defined by the ESL of the DC link capacitor and by the interconnections (layout of PCB, lead of components, etc.). Additionally, the ESL of the DC link capacitors contributes to the drain-source voltage overshoot (see (1.17)..(1.18)). This inductance should be reduced from the EMI perspective as well as from the semiconductor point of view (losses and breakdown voltage). For the modern power converters based on WBG semiconductors, the stray inductance in the DC link is made as low as possible.

The situation is more difficult for CM characterization of VSC. According to the analysis provided in Appendix A, the CM output and input side are always coupled during all switching states of the 2-level FB converter. The total value of Y-capacitors is normally limited in order to avoid the huge leakage currents (see Section 1.4). Therefore, it is not possible to decouple DC and AC side CM currents in the AC drive. The stray capacitances between each phase (both at the input and output of VSC) play a huge role and should be taken into account. These capacitances can be formed by several components which are applied in the typical VSC. The most significant stray capacitors were summarized and presented hereunder:

The capacitance between MOSFET and heatsink (C_{mh}): This capacitance is supposed to have the largest value among other parasitic Y-capacitors in the power converters. In [116, 42], it is the only capacitance which was considered during the simulation of CM current. C_{mh} is observed almost in any power converter. Its value is defined by the shape of the cooling pad which can be found in the datasheet [142]. It is also defined by the thermal interface material which is used as an insulator between the power switch and the heatsink. For the FB inverter, there are 6 of such capacitances: 3 of them are connected to the positive rail of DC supply (drain pins of high side MOSFETs) and another 3 are connected to each phase at the output (drain pins of low side MOSFETs). Assuming, that heatsink is ideally grounded, this capacitance has very low ESL. The value of capacitance can be estimated using (2.28), where A is across-section area of the thermal pad of the MOSFET, d and ϵ are thickness and electrical constant of thermal interface material respectively.

The capacitance between diode and heatsink (C_{dh}): This capacitance has the same nature as C_{mh} but it is formed between the external free-wheeling diode and the heatsink. It means that these parasitics can be avoided if only body-diodes of MOSFETs are used. The external SiC Schottky diodes were

applied in the designed converter in order to reduce the losses (see Section 3.1). The applied diodes introduce a capacitance between its cathode and ground [141]. Therefore, they are connected in parallel with C_{mh}. The value of C_{dh} can be estimated using (2.28) as well.

The capacitance of gate driver circuit C_{gd}: The typical gate driver circuit, which is shown in Figure 1.25, provides galvanic isolation between the source of a switch and the control system. The power domain of the control system is normally grounded. Therefore, the parasitic capacitances, which are observed in the isolated power supply and the signal shifter, should be considered too. Values of these capacitances can be given by the manufacturer, for example for an isolated DC/DC converter which was applied during the design [143]. Some amount of ESL is presented in C_{gd} which is defined by the structure and by the corresponding layout of the gate driver (see Figure 1.25). The gate driver introduces parasitic capacitance between the source of a MOSFET and the ground. Therefore, there are 3 additional capacitors connected to the negative rail of DC power supply (gate drivers of low side MOSFETs), whereas another 3 are connected to each phase at the output (gate drivers of high side MOSFETs).

The capacitance of the measurement circuit C_{ms}: For the protection and control purposes some measurements circuits are always applied in VSC. In the experimental converter (see Section 3.1), there are two current measurements and one voltage measurement which were realised with delta-sigma analog to digital converters (ADC) [144]. These circuits introduce some value of Y-capacitance with some portion of ESL at the input and output of the converter.

$$C = \frac{\epsilon_0 \epsilon A}{d} \tag{2.28}$$

All these capacitances are allocated at different points of VSC according to the layout of PCB. Therefore, some amount of inductance is observed between each capacitor. In order to build the analytical model for the CM characterization of the designed inverter, it is necessary to calculate these inductances. According to the hardware description given in Chapter 3, two types of interconnections are presented in the designed VSC (power core): wires and traces of PCB. Simple formulas can be used to obtain inductances of these interconnections. The simplified formulas for the calculation of self- and mutual inductances can be found in [145]. For the simplicity mutual inductance of wires is ignored. The inductance of a single wire can be found:

$$L_{\mathrm{w}} = 2l\Big(\ln\big(\frac{2l}{r}\big) - \frac{3}{4}\Big) \tag{2.29}$$

where l and r are the length and radius of a single wire in cm respectively. The resulting value obtained (2.29) returns the value of self-inductance of a single wire in nH [145]. Thus, the resulting CM inductance should be L_{w} divided by the number of parallel wires (2 for input bipolar DC supply and 3 for output three-phase AC).

The traces in the PCB are made with copper polygons for the power lines. The polygons have a complex geometry including cutouts. The slots and cutouts of the copper polygons are ignored for the simplified calculation. Because the thickness of traces and the distance between them are very low, all power lines

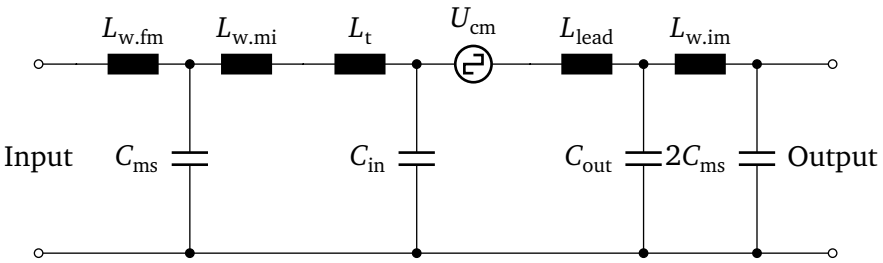


Figure 2.17.: Analytical CM representation of the designed VSC.

are assumed to be electrically connected for the CM representation of VSC. Such an assumption gives the possibility to avoid the calculation of the mutual inductance. The value of self-inductance in nH of thin tapes according to [145] is:

$$L_t = 2l\Big(\ln\big(\frac{2l}{b}\big) + 0.5\Big) \tag{2.30}$$

where l and b are the length and width of the traces in cm respectively. As far as all stray Y-capacitances and inductances are defined, the circuit can be built for the CM model of VSC in the frequency domain. This circuit is shown in Figure 2.17. It is built in accordance to the structure of the designed inverter (see Chapter 3). The input of the converter (DC side) is connected through the relatively short cable to the measurement circuit. This part of the VSC is represented by the inductance $L_{w.fm}$ of the cable and the capacitance C_{ms}. The measurement circuit is then connected to the PCB with the other wires, which are also represented by the inductance $L_{w.mi}$ in Figure 2.17. The inductance L_t of PCB is also presented before the parasitic capacitance C_{in}. This capacitance is equal to the sum of all stray Y-capacitors which are introduced by the power switches and gate drivers at the DC side. For the designed FB converter it is:

$$C_{in} = 3(C_{mh} + C_{dh} + C_{gd}) \tag{2.31}$$

The power switches are replaced with the source of CM voltage similar to the concept of the 1st frequency domain models [116, 42]. Some portion of the lead inductance L_{lead} of a switch in TO-247 package is also taken into account. Its value was evaluated in [146] where it was also obtained using (2.30). The value of capacitance C_{out}, which is observed at the AC side of the inverter, is equal to C_{in} for the designed converter. The output of designed VSC is connected to the current measurement circuits with wires. The output current measurements are also mirrored in Figure 2.17 with $L_{w.im}$ (wire) and doubled value of C_{ms} (2 measurements circuits are applied for the current at the AC side of the inverter).

Some parameters of the circuit in Figure 2.17 are taken from the datasheets. The other components are calculated using equations (2.28)..(2.30). All these parameters are summarized in Table 2.1. The main problem comes with the evaluation of L_t. For the current PCB design (see Figure 2.18), all half-bridges are allocated on the different distances from the input connector. For the analytical model, it is decided to calculate the PCB inductance L_t between the connector and the middle half-bridge (phase B).

Table 2.1.: Stray parameters of VSC for analytical model.

Parameter	Value	Calculation
C_{mh}	12.2 pF	Equation 2.28: $\epsilon = 9.8$, $A = 281\,\mathrm{mm}^2$, $d = 2\,\mathrm{mm}$
C_{dh}	6.8 pF	Equation 2.28: $\epsilon = 9.8$, $A = 141\,\mathrm{mm}^2$, $d = 1.8\,\mathrm{mm}$
C_{gd}	7 pF	Datasheet[143]
C_{ms}	0.5 pF	Datasheet[144]
$L_{\mathrm{w.fm}}$	36 nH	Equation 2.29: n=2, $l = 10\,\mathrm{cm}$, $r = 2.5\,\mathrm{mm}$
$L_{\mathrm{w.mi}}$	86 nH	Equation 2.29: n=2 $l = 20\,\mathrm{cm}$, $r = 2.5\,\mathrm{mm}$
L_{t}	43 nH	Equation 2.30: $l = 14\,\mathrm{cm}$, $b = 10\,\mathrm{cm}$
L_{lead}	7 nH	According to [146]
$L_{\mathrm{w.im}}$	141 nH	Equation 2.29: n=3 $l = 30\,\mathrm{cm}$, $r = 2.5\,\mathrm{mm}$

The proposed analytical representation of the CM circuit for the frequency domain model takes more stray parameters into account in comparison to the simplified circuits [116, 42]. The parameters of such circuits can be easily obtained without complex calculations. However, some effects of the real PCB are ignored such as: complex geometry of the traces, different location of parasitic capacitances and stray capacitance between the PCB itself and the heatsink. These parameters can be considered more precisely using FEM.

VSC Characterization Using FEM

A lot of FEM tools have appeared on the market in the last decade. All of them give the possibility to calculate the electric and magnetic fields of the complex structures such as PCB. Rise of such FEM tools was initiated by the communication and computer technologies where the estimation of the RF stray parameters of PCB is required for the signal integrity analysis. The most FEM software packages allow the upload of the PCB design files directly from the development software. It reduces the effort to build the FEM model. The FEM software, which was used in the conducted research, is called "CST PCB Studio". The software is optimised for the signal and power integrity analysis of PCBs. The photo of the user interface of "CST PCB Studio" with the uploaded design of the studied inverter is shown in Figure 2.18 where the PCB can be observed from the top.

Before the PCB was uploaded, its structure was simplified in order to reduce the computational time. Only the main components, which are involved in power transfer, were considered: power switches, gate drivers, DC link capacitors with resistors and power connectors. All other components were excluded such as test points, level shifters, logic circuits, etc. Because the applied tool is optimised to be used only with PCBs, it is not possible to add the real model of a heatsink in this model. The heatsink was added as an additional conduction layer below the bottom copper layer of PCB. The layer stack information can be seen in Figure 2.18 on the right (the additional layer has a grey colour). The distance between

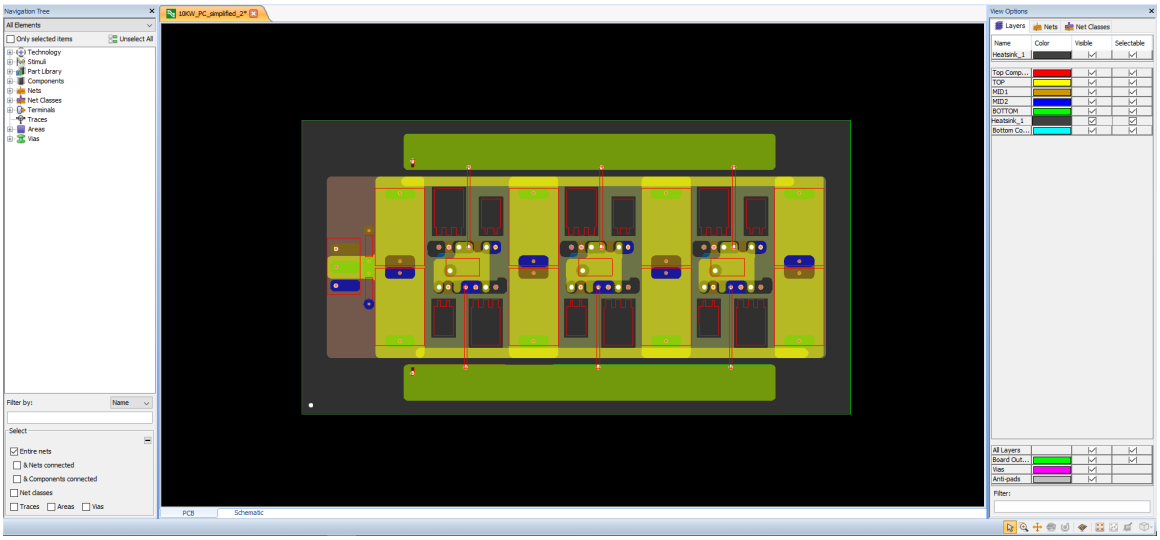


Figure 2.18.: The user interface of "CST PCB Studio" with uploaded PCB.

the bottom layer and the "heatsink layer" corresponds to the designed inverter and equal to 8 mm. The thickness of the additional layer is 100 μm.

The software provides the possibility to model the S-parameters of a PCB with defined ports [147]. Amount of ports depends on the components which are assumed during the simulation. Despite that components are shown in red in Figure 2.18, they are not considered directly during the FEM calculation. Each component just gives at least 1 port for the output S-parameters. The results of FEM simulation can be proceeded further in the schematic tool "CST Studio Suite". Its working environment is shown in Figure 2.19. The simulated PCB is a huge block in the middle of Figure 2.19 with a required number of terminals. These terminals are representing the input/output of the corresponding components of the PCB circuit. Depending on the required accuracy, the terminals of PCB should be connected with an appropriate model of a switch. It is also possible to use SPICE models of switches in the time domain, as it was done in [97]. However, the power switches are simplified in order to reduce the computational effort of the FEM simulation as much as possible. The ports are connected only with the respective stray capacitances which are listed in Table 2.1. It means that the model is used to consider only parasitics of PCB, whereas components are replaced by the simple concentrated parameters (capacitors).

The results of FEM simulation can be also used to analyse the DM impedance. Therefore, some components were added to the schematic in Figure 2.19 in order to obtain the DM impedance of the VSC. These are the DC link capacitors with the balancing resistors and the capacitances between terminals of the power switches (the drain-source capacitance of a MOSFET C_{ds} and anode-cathode capacitance of the Schottky diode C_{ac}). The values for these components were taken from the corresponding datasheets [141, 142]. The values of C_{ds} and C_{ac} are voltage depended, but the zero bias values were considered for the initial evaluation.

The presented FEM model provides simulation only of the main part of the power core. The measurement circuits (DC link voltage and output currents) were also considered only by the stray capacitances to the ground similar as in Figure 2.17. The wire interconnections between the measurement circuits and power switches are also represented by the lumped inductances from Table 2.1.

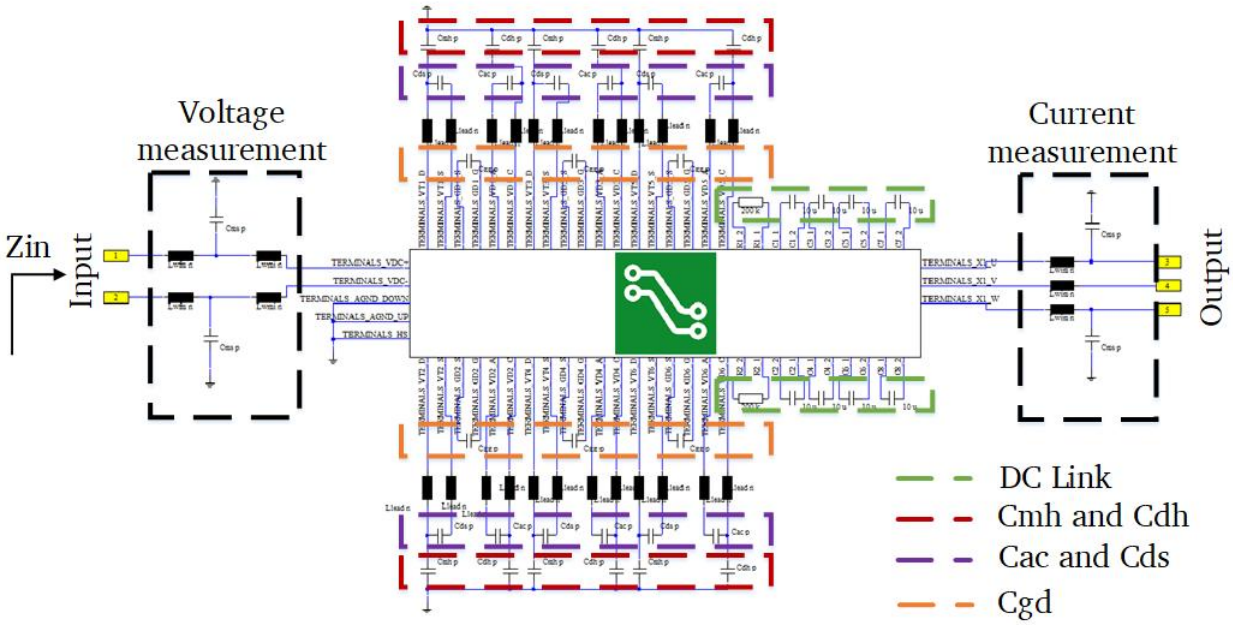


Figure 2.19.: Schematic post processing of FEM simulation results in CST.

The circuit representation of VSC with FEM simulated PCB in Figure 2.19 can be further used to obtain a CM 2-port network. It is necessary to short circuit single-ended input and output pins. Then, the 2-port network of CM parameters can be calculated using current and voltage source at the input and output. The same procedure can be applied to the real VSC. In this case, the 2-port network of S-parameters can be measured using VNA similar as it was made for the behavioural models in [125]. The "CST Design Studio" allows the extraction of such network directly from the simulation. The resulting S-parameters can be easily converted to Z-parameters by means of (2.8). In order to compare the FEM and analytical approach of VSC characterization, the 2-port network is also evaluated for the circuit shown in Figure 2.17. The value of input impedance (impedance measured between short-circuited inputs of VSC and ground or $\mathbf{Z}_{11}$ of 2-port CM network) is presented in Figure 2.20 for both cases of the simulation and measurements results. The simulation results can be also compared with the measurements in Figure 2.20.

As can be seen in Figure 2.20, all impedances show the same capacitive behaviour. The impedances are falling reaching its lowest value around 20 MHz. Up to this frequency, the VSC can be represented only by the stray capacitance as it was done in [116]. A further increase of impedance can be observed after the frequency of 20 MHz. Such behaviour corresponds to the 1^{st}-order model of a capacitor (see Figure 1.15). From this point, it can be stated, that both FEM and analytical approaches replicate the behaviour of the real VSC. However, the accuracy of the analytical model is lower as it was expected. Despite, that the same parasitics of components were used in the analytical model and in the FEM, the later one shows the better accuracy. There is about 3.5 dB difference between the analytical and measured results. At the same time, the FEM approach provides a very good accuracy on the whole frequency range. The results in Figure 2.20 show the influence of PCB on the CM impedance of the designed inverter. It can

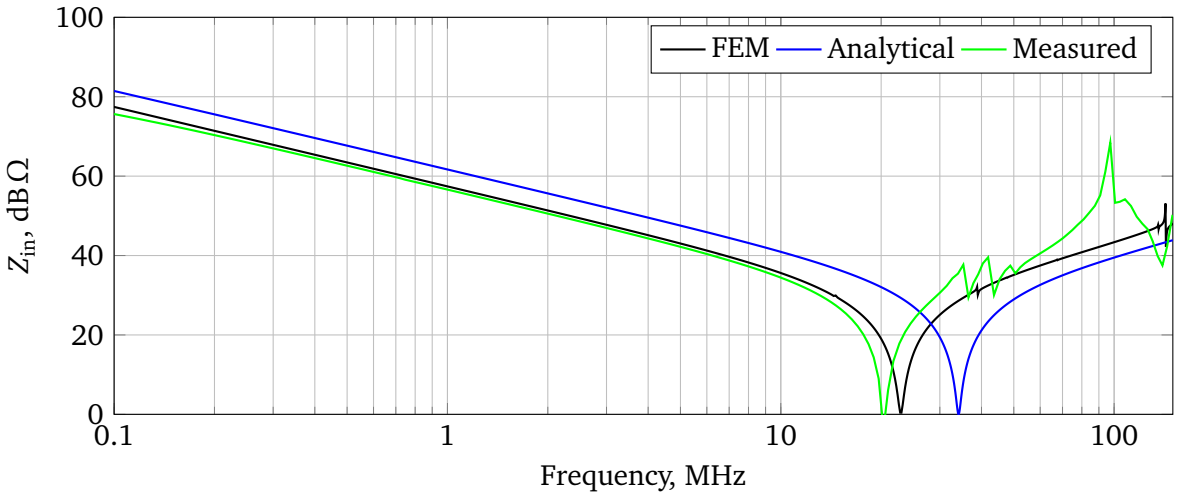


Figure 2.20.: The simulated and measured input CM impedance of VSC.

be concluded that PCB introduces the additional stray capacitance. This capacitance is formed between the PCB itself and the heatsink. It is not considered in the analytical model (see Figure 2.17).

After the frequency of 10 MHz, the difference increases between the simulated and measured impedances even for the FEM simulation in Figure 2.20. It can be observed, that the resonance of the simulated CM impedance is slightly shifted towards higher frequency range (22 MHz for FEM upon 20 MHz for measurements). This is due to the stray parameters which were ignored during the simulation. In order to improve the accuracy of the FEM simulation of PCB, it is necessary to consider more effects: losses in the conductive and insulating materials, detailed model of the components (switches, gate drivers, heatsink, wires and measurements circuits). Some increase of accuracy can be also provided in the software by making the finer mesh for the finite elements for example. All improvements can be realised with modern software packages. However, the computational time increases with the accuracy of the FEM model as well.

Looking on the measured values in Figure 2.20, it can be concluded that the input impedance on inverter can be simulated using 1st-order model of a capacitor (see Figure 1.15) in the considered frequency range. This corresponds to the ideas which were made for the 1st frequency domain models [116]. However, the accurate estimation of exact model parameters (capacitance and ESL) prior measurements is mostly possible by means of FEM tools.

As it was explained before, the accuracy of the FEM simulation was also reduced to achieve the lowest computational time of the model in order to fulfil the criteria stated at the beginning of Chapter 2. The computational time of the proposed FEM model for the considered PCB took about 2 min and 47 s. This time is required to obtain the S-parameter model of the PCB. The model of PCB can be then used in the circuit simulator with different components. The time, which is required for the circuit simulator in Figure 2.19 is very low taking about 3 s. This value is comparable with the amount of time which is required for the analytical model about 1 s (the same computer was used to obtain all results). This is a benefit of the proposed approach. In the case of FEM simulation with full component consideration, it would be necessary to run the FEM simulation each time for different components. In the proposed model, it is possible to run the FEM model of the PCB only once. Then, the various components can be considered using their lumped stray parameters. Therefore, the model can be calculated quickly for

different components. It gives the possibility to evaluate the influence of their stray parameters on the conducted EMI. At the same time, the evaluation of new layout only from the EMI point of view is not possible because the other limitations should be also considered during the PCB design (thermal and mechanical stress, vibrations, etc). Moreover, any type of layout should be implemented before the simulation requiring some time as well. Therefore, the proposed FEM approach provides better accuracy with a relatively low computational effort and can be used for the simulation of EMI behaviour in AC drives.

2.4 Description of the Final Model

The previous sections describe the improved characterization of VSC and other components of the AC drive in order to increase the accuracy of the frequency domain model. This section presents the final model which was developed during the conducted research. It explains also the calculation of such a model.

Any model (in the time or frequency domains) for conducted EMI prediction obtains the high-frequency currents which are recognized as a conducted EMI. However, the noise is measured with an EMI receiver or spectrum analyser. These devices are based on the superheterodyne principle as it is explained in Section 1.1. The level of noise depends on the parameters of measurement device such as RBW and detection method (average, peak or quasi-peak) [44]. Therefore, it is required to take parameters of the spectrum analyser into account. The second part of this section discusses an implementation of spectral analysis for the interpretation of the simulation results and its influence on the modelling procedure.

2.4.1 Simulation of High-Frequency Currents

The structure of the model based on MM parameters is shown in Figure 2.21. The following components are considered on the AC side of the VSC according to the structure of EUT for the EMI measurements: output filter, cable and motor. It can be observed that 6-port networks are used to describe these components on the right-hand side from the VSC in Figure 2.21. The networks are the MM parameters which were presented in Section 2.2. The MM parameters are obtained from the measured single-ended S-parameters which were also converted into Z-parameters by means of (2.8). The resulting single-ended Z-parameters of the output filter and cable are converted then into the MM parameters by means of (2.16). The MM parameters of delta connected motor, which is applied in measurement setup (see Section 3.2), is calculated using the corresponding transformation presented in Subsection 2.2.3. The outputs of the 6-port MM network of delta connected motors are short-circuited in Figure 2.21.

On the left-hand side from VSC, the DC side components can be observed as well. The MM 4-port networks are used to describe the bipolar DC side of the considered AC drive system. These networks are obtained directly for the measured S-parameters by means of (2.12). The LISN, input filter and cable are considered on the DC side of the setup. The input cable is then terminated by the CM and DM impedances of the LISN ($Z_{\mathrm{L.cm}}$ and $Z_{\mathrm{L.dm}}$ respectively). The LISN impedances can be easily calculated from the given circuit (see Figure 1.3). Assuming that each power line of DC supply is connected to the LISN, $Z_{\mathrm{L.dm}}$ will be the doubled value of the LISN impedance (see Figure 1.2), whereas $Z_{\mathrm{L.cm}}$ will be

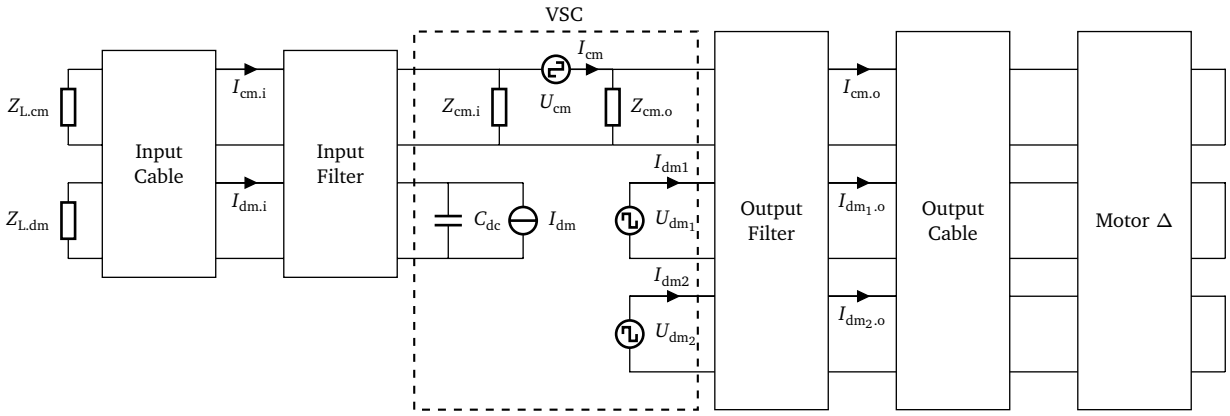


Figure 2.21.: The structure of the model for conducted noise prediction generated by the AC drive.

two times lower than the impedance of the single LISN. As can be seen in Figure 2.4.1, all components are connected in chain. Therefore, it is comfortable to convert the resulting MM Z-parameters into ABCD-parameters (see Appendix B) for further calculation.

The VSC converter is described by the lumped parameters, separately for CM and DM. The CM circuit of VSC in Figure 2.21 is similar to one which was applied in the 1st frequency domain models (see Figure 2.2a) [116]. However, the input $Z_{cm.i}$ and output $Z_{cm.o}$ CM impedances were improved in the previous section considering more parasitics (see Section 2.3). The resulting values of $Z_{cm.i}$ and $Z_{cm.o}$ were obtained using the FEM model of the VSC because it shows better accuracy in comparison to the analytical model of the inverter. The spectrum envelope for the CM voltage source U_{cm} is obtained using Fourier analysis of the generated time domain waveform of CM voltage (see Section 2.3.1).

The DM description of the VSC slightly differs from the one which was proposed in [116] (see Figure 2.2b). This is due to the implementation of 6-port MM parameters for three-phase components where two DM circuits are considered (DM_1 and DM_2). Therefore, two voltage sources U_{dm_1} and U_{dm_2} can be observed on the AC side of VSC. The voltage sources decouple the output and input side of the VSC. The DM noise at the output is defined only by the corresponding voltage sources and the impedance on the AC side of the VSC. The spectrum envelope for DM voltage source is also obtained from the respective phase-to-phase voltage which was generated in time domain.

Ideally, no DM current should be observed at the input side of the VSC due to the presence of DC link capacitors. The value of ESL in the DC link capacitors is normally reduced in order to obtain a lower value of switching losses (see Section 1.4). However, some amount of stray inductance cannot be avoided. It means, that a small portion of RF DM current can be transmitted to the input from the output. As it was shown in Appendix A, it is hard to model the real DM behaviour in the frequency domain due to the high non-linearity. The coupling between input and output DM current depends on the switching state of inverter.

The circuit in Figure 2.21 can be solved manually or using the circuit simulator such as "CST Design Studio". In order to solve the circuit of the proposed model, it is necessary to simplify it. The calculation procedure is explained in Figure 2.22. Assuming the ideal VSC with a decoupled output and input DM currents, the current source I_{dm} in Figure 2.4.1 is assumed to be zero at the first simulation stage (see

Figure 2.22a). Using the ABCD-parameters, it is possible to combine several components to a single 6-port and 4-port networks on the AC and DC side respectively.

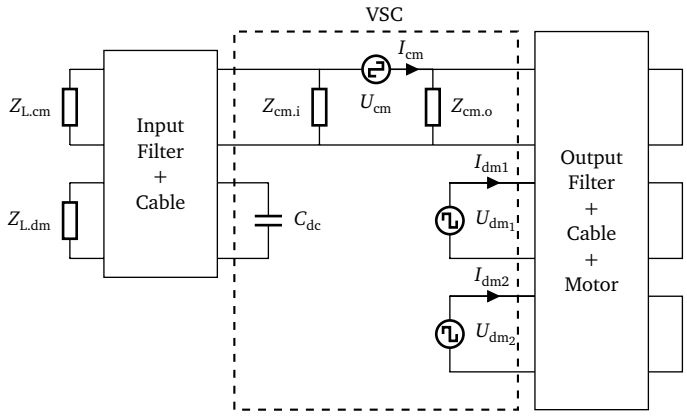
The whole DC side of the AC drive including $Z_{\text{cm.i}}$ can be summarized to the unterminated impedance Z_{in}, as it is shown in Figure 2.22b. It becomes then possible to calculate the current in the VSC: I_{cm}, I_{dm1} and I_{dm2}. The output CM/DM currents ($I_{\text{cm.o}}$, $I_{\text{dm1.o}}$ and $I_{\text{dm2.o}}$ in Figure 2.21) can be estimated using the 6-port network of the output filter. As far as currents in VSC are defined, the input mode currents can be calculated as well. The circuit shown in Figure 2.22c can be then used to estimate the input currents where the output AC of VSC is brought in the form of the unterminated impedance Z_{out}. The current source I_{dm} can be assumed to have a zero value considering decoupled DM currents at the input and output of the VSC. However, it is also possible to validate this assumption by adding the mentioned above current source. The value of I_{dm} can be estimated using the equations from Appendix A applied to the particular switching state of the VSC . These equations contain also the natural coupling from CM to DM at the input of the VSC (see Section 1.3).

Ideally, the DC link capacitor C_{dc} provides a short-circuit of the current I_{dm} in Figure 2.22c. However, some amount of current can penetrate the input DC side. The impedance of the DC link including the ESL can be obtained from the FEM simulation shown in Figure 2.19. Such an approach for the estimation of DM currents at the input of VSC does not provide the exact values. It represents the worst case of the coupling between DM currents at the input and output of VSC. The power switches and their stray capacitances contribute to the decoupling of these currents in the real inverter. If a high level of DM current $I_{\text{dm.i}}$ will be observed during the simulation, the DC link of VSC should be improved. This can be done utilizing the additional bypass capacitors for example.

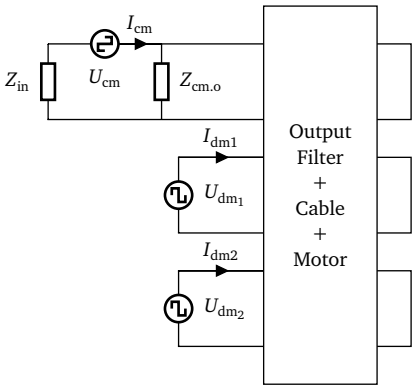
The developed approach can be used to obtain any currents and voltages at the input/output ports of all components in the AC drive. Using the circuit in Figure 2.22c, the voltage on LISN can be estimated for the CISPR standards. According to the DO-160 (see Section 1.1), it is required to measure the noise at input power lines (input cable) and on the whole bundle of interconnection lines (output cable). For the considered AC drive, it is necessary to estimate the values of output CM current $I_{\text{cm.o}}$ and the input phase current. The latter one consists of input CM $I_{\text{cm.i}}$ and DM $I_{\text{dm.i}}$ according to (1.2).

The proposed model has the following benefits:

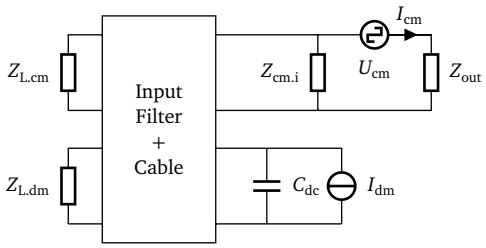
- It uses the frequency domain calculation in order to reduce the computational time.
- The improved replacement circuit of VSC in the frequency domain (see Section 2.3) allows an extension of the maximum frequency range. However, the model is fully compatible with any frequency domain model. Therefore, it is also possible to use the simplified representation of the VSC at the 1$^{\text{st}}$ design steps.
- The model provides a link between converter design (topologies, PWM techniques, hardware design) and the conducted EMI behaviour. Therefore, it can be applied simultaneously for the EMI filter and converter design. It is also possible to obtain the conducted noise for the different operation modes of an AC drive.
- The proposed model can be easily coupled with simple frequency domain models (see Figure 2.2) and with behavioural models. If 4- and 6-port networks are not available for the particu-



(a) Model simplification



(b) Calculation of currents in VSC and at the output



(c) Input current calculation

Figure 2.22.: Simplification and calculation of the proposed model.

lar components, they can be easily replaced by the simple 2-port networks (CM or DM) and by the unterminated impedances.

- It is also possible to consider the CM and DM separately just by setting the respective voltage sources to zero. It is essential for the EMI filter and VSC design because different conducted noise reduction techniques have an influence on the different modes (see Section 1.4).
- The proposed model considers the crosstalk between CM and DM as well. It is also possible to evaluate the natural MM noise at the input of VSC.

The proposed model fulfils all criteria which are stated at the beginning of this chapter. However, some effects are not taken into account. The effects of voltage overshoot and ringing were ignored during the

spectrum envelope calculation of the VSC output voltages (see Section 1.4). These effects can be also included in the spectrum calculation. But this requires an additional computational effort. It is also not possible to consider completely the DM behaviour of the system in the frequency domain because it is assumed that the input DM current is decoupled from the output current in the VSC. However, all these effects can be ignored in the modern VSC based on WBG semiconductors. The parasitics in the DC link of SiC converters are normally reduced, as it is essential for clean switching with the low switching losses and decreased voltage overshoot. In that case, the overshoot of drain-source voltage should not have a huge impact on the EMI. The frequency of oscillations should be also out of the frequency range of conducted noise measurements. The value of ESL is also reduced in the converter based on WBG devices. It makes the assumption about the decoupled input and output in DM of the VSC to be a good approximation.

2.4.2 Spectrum Analysis and Simulation

In most contributions dedicated to the simulation of conducted noise in the frequency domain [116, 42], the spectrum envelope of the voltage source is taken from the trapezoidal representation of PWM signal (see Figure 1.8). In this case, the fixed value of the duty cycle and fall/rise time is considered on the whole fundamental period. Such an approach neglects the varying duty cycle of PWM signal in VSC and variation of rise/fall times of the output voltage. The latter one can be observed in Subsection 2.3.1. The generation of time domain data and its further recalculation in the frequency domain was also proposed and discussed in [116]. This approach was implemented in [12] as well. However, the impact of varying duty cycles and switching times of PWM voltage on the conducted noise calculation was not analysed fully. This section gives a detailed description of the spectrum analysis applied for the frequency domain models.

The principles of the spectrum analysis were investigated during the conducted research [25, 26]. The key parameters of the spectrum analyser (EMI receiver) are summarized in Section 1.1. These parameters influence the level of the measured conducted EMI. During the generation of spectrum envelope, it is required to consider: frequency range, value of RBW, dwell time and the detector type. The frequency range or the maximum frequency defines the time step which should be applied during generation of the VSC output voltage in the time domain (see Section 2.3). The step of the time data should be at least twice time lower than the value of one divided by the maximum frequency. The value of dwell time defines the size of generated time domain data. The generated PWM signal must be obtained at least for the dwell time. However, assuming that noise in the considered AC drive system is measured for each operation mode at steady-state, the fluctuations of noise level are awaited during the fundamental period of PWM. Therefore, it is better to generate the time domain PWM signal for the whole fundamental period, even it is longer than the dwell time.

If the time domain data is generated using the algorithm shown in Figure 2.14, the Fourier transform can be applied to obtain the spectrum of the VSC output CM and DM voltages. However, the simple discrete Fourier transform does not consider the RBW and detector type of an EMI receiver. In order to consider these parameters, it is required to apply the short-window discrete Fourier transform (SWDFT). The windowed Fourier transform was already used for the analysis of EMI generated by the three-phase rectifier with buck stage in the DC link [148]. In SWDFT, the signal is divided into several sectors with a

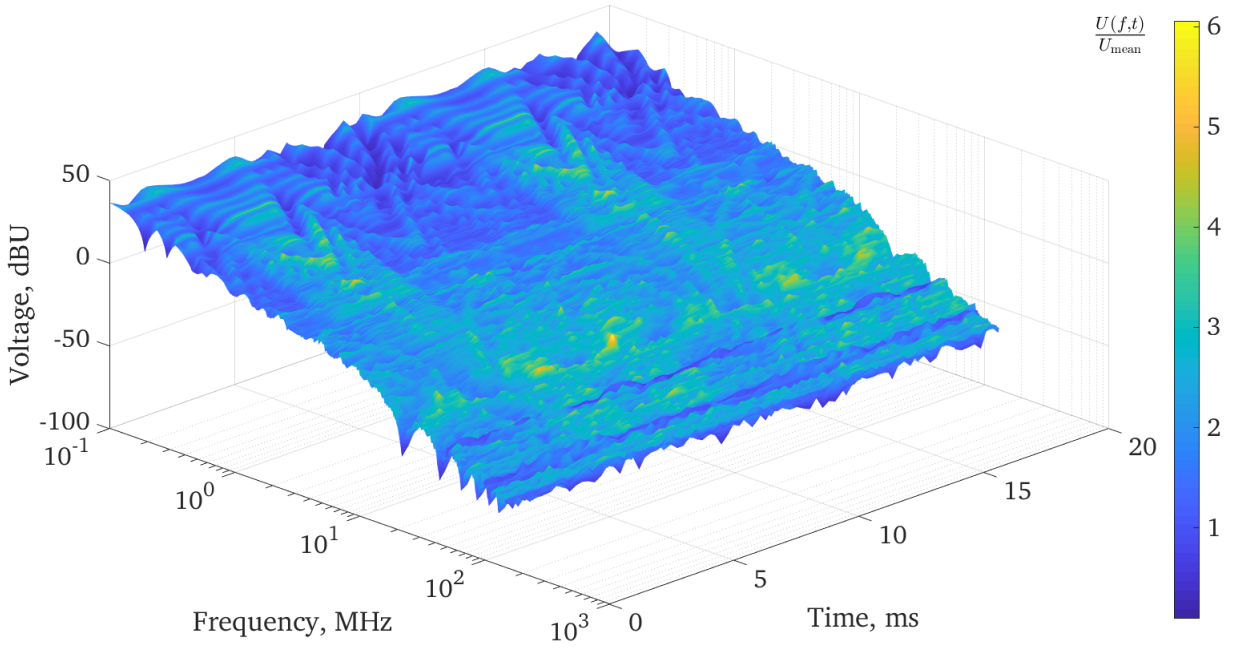


Figure 2.23.: The time-frequency analysis of generated PWM voltage (DM_1).

certain period. These sectors are multiplied with a function of the special shape which implements the window. The shape and size of the window correspond to the RBW filter of the superheterodyne receiver of the spectrum analyser [25]. The discrete Fourier transform is then applied to each window [149]. The output of SWDFT is a time-frequency data which shows how the spectrum of signal changes in time. SWDFT applied to the VSC output voltage considers the variation of amplitudes during the fundamental period of the PWM signal.

The SWDFT was applied to the generated time domain voltage of DM_1 PWM voltage (generated signal from Figure 2.15). The parameters of SWDFT were taken according to DO-160: window length is equal to 0.5 ms (RBW=1 kHz), length of the signal is equal to 20 ms (dwell time is equal to the fundamental period). The resulting time-frequency data of DM_1 voltage can be observed in Figure 2.23. The y- and x-axes show the frequency and time respectively for each point of the presented data. The z-axes show the amplitude of the signal in dBV for each time and frequency step. The colour indicates the difference between the actual amplitude ($U(f,t)$) at the particular frequency and the mean value of amplitudes on the whole period U_{mean}. The value U_{mean} corresponds to the magnitude in case then the Fourier transform is applied to the whole period of the PWM signal. In other words, the mean value corresponds to the amplitude obtained with the value of RBW equal to the fundamental frequency (dwell time) of the output voltage.

It can be seen in Figure 2.23 that the resulting spectrum envelope corresponds to the trapezoidal signal with −20 dB and −40 dB fall of amplitude and the certain minima for the 1$^{\text{st}}$ window (t=0) (see Figure 1.8). However, it can be also observed that the amplitude changes with time during the fundamental period for each frequency step. The dark blue points in Figure 2.23 indicate the amplitudes which are equal to U_{mean} on the whole fundamental period. At the same time, the yellow spots indicate the

time where the particular harmonic reaches its maximum magnitude. The actual value can be 6 times higher than the mean value with the applied RBW. For the lower frequencies (before −40 dB cut-off), the highest magnitudes are observed at 5 and 15 ms. At these points, the fundamental part of phase-to-phase voltage (DM_1) reaches the maximum value. The PWM signal at this point has the longest duty cycle (long duration of an active vector according to SVPWM). The value of duty cycle influences the level in the lower frequency range. The yellow spots are also observed at 5, 8, 15 and 18 ms in the RF range. These times correspond to the peak values of phase currents I_a and I_b (see Figure 2.15). The lowest rise/fall times can be observed at these points due to the diode commutations. Therefore, magnitudes of RF part of PWM signal increase leading to the higher noise levels.

The peak detectors should be applied during conducted EMI measurements according to section 21 of DO-160 [24]. In this case, the maximum amplitude is observed on the EMI receiver for each frequency point [148]. According to Figure 2.23, the difference between the spectrum obtained with SWDFT and with the conventional discrete Fourier transform can reach the value of 15 dB ($20 \log 6$). In order to consider the type of detection, the frequency domain model should be calculated in the following order. First, the SWDFT should be applied to the generated VSC output voltage. The spectrum of each window is then used to define the respective voltage sources in the frequency domain model. The required currents and voltage, which are defined as conducted EMI, can be estimated for each window using the frequency domain model (for example model shown in Figure 2.21). This procedure is repeated for each window. The resulting values of currents are also presented in the time-frequency domain. In order to implement the required peak detection, it is necessary to take the maximum value for each frequency. This approach increases the computation time as the frequency domain model is calculated for each window. However, it is still much faster than the time domain model. Moreover, it also possible to apply the conventional discrete Fourier transform to the proposed model for the 1^{st} analysis, because the increase of the PWM voltage level is observed only at the particular frequencies. These points are indicated in this section.

The proposed approach of spectral analysis allows consideration of EMI receiver parameters such as RBW and peak detection. The provided analysis shows also the effect of variable duty cycles (PWM) and variable rise/fall times. Implementation of SWFDT increases the accuracy of the frequency domain approach of EMI simulation but only in the case then the PWM voltage is generated properly in time domain.

2.5 Conclusion

The power electronics engineers have to consider the behaviour of a VSC in AC drive from different points of view. It is common to consider thermal behaviour and control system design besides the typical circuit simulation during the development of a power converter. One of the goals of the research work is to find a model for the power electronics engineer which can be used to consider the EMI behaviour during the design of converter. This chapter discusses such kind of a model. Several requirements are stated at the beginning of the chapter. These criteria should be fulfilled in order to consider EMI during the design of the converter. Then, the existing approaches are discussed. It is shown that the most promising approach from the computational point of view is the simulation of an AC drive in the

frequency domain. However, the available frequency domain models should be improved regarding the accuracy, especially in the RF range.

The second part of this chapter presents the improvements which were applied to the frequency domain models. In order to include the MM noise, which is associated with crosstalk between CM and DM, all components of the system besides the VSC are described using n-port networks. In order to keep the simplicity of the VSC model, the n-port parameters are converted to the MM. The classical MM parameters, which are normally applied to the differential lines, are extended to the three-phase systems. The VSC characterization is improved keeping in mind that different PWM patterns and switching behaviour should be also considered during the simulation. For this reason, comprehensive analysis of VSC output voltage is provided in this chapter. The new algorithm with the reduced computational effort is proposed. It is used to generate the time domain waveform which replicates the real PWM output voltage of inverter in the AC drive. The impedance of converter in the model is also improved considering the most significant stray components in the designed VSC. The impedance of converter is obtained using the analytical and FEM models. Both models are compared with the measured impedance of the experimental converter. The results are showing good accordance, especially of the FEM model.

Finally, this chapter explains how to combine the MM parameters with the model of VSC. The resulting model can be used to estimate the current and voltage at any point of the AC drive. The model includes the various propagation paths of CM, DM and MM noises. It is also shown how to consider the worst case of DM current transfer between input and output of VSC. The last improvement of the frequency domain simulation is achieved due to the application of SWDFT. It gives the possibility to consider the parameters of EMI receiver such as RBW and peak detector during the simulation.

The resulting model satisfies all criteria stated at the beginning of the chapter. It considers the different noise reduction techniques as well as the MM noise. The computational time of the final model is increased in comparison to the simplified frequency domain models. This is mostly due to the FEM simulation and application of SWDFT. However, the resulting calculation time of the whole model does not exceed 5 min with calculation on the simple laptop. The computational time of the proposed model can be also improved optimizing such parameters as frequency step. Moreover, the FEM simulation and SWDFT can be avoided at the very first design stages reducing the computational time to 1 min. The proposed model is fully compatible with the classical frequency domain models of the AC drives. The model validation is provided in Chapter 4 showing good accordance of the simulation on the whole frequency range.

3 Experimental Setup and Hardware Description

In order to validate the model which is described in Chapter 2, an experimental setup was designed during the research work. This setup was also used to investigate the impact of the conducted noise reduction techniques which are explained in Section 1.4. The research work takes into account a huge number of parameters of the system: parasitics, VSC design and control, operation mode, etc. Therefore it is required to indicate the relationship between the model inputs and the measurement setup. Moreover, the measurement system should fulfil the requirements according to the chosen standards (see Section 1.1). This chapter gives a description of the experimental setup which was built during the research work.

The first part of this chapter discusses the design of the key component of the studied system - the power core. The power core includes the inverter (VSC) in a 2-level FB topology, gate drivers, EMI filters and additional components such as measurement and control circuits. The additional components cannot be avoided because they are also required for the functionality of an AC drive. All components of the VSC influence the resulting conducted noise generated in the AC drive. Therefore, they are designed in a special manner in order to simplify the investigation. The second part of this chapter describes the components of the experimental setup such as motor, cables and measurement devices. Finally, a conclusion is given at the end of this chapter. It provides the link between the structure of the setup and the different test scenarios for the investigation. It also discusses the impact of system components on the measurements results and their accuracy because there was no access to the certified EMI laboratory during the research .

3.1 Power Core

As it is explained in Section 1.2, the VSC is a source of conducted noise in the AC drive. The VSC produces the DM and CM voltages at the output with a broadband spectrum due to the PWM operation. The stray parameters of the VSC provide also the propagation path for the high-frequency currents which are indicated as conducted EMI. However, the VSC cannot be operated without the additional components such as gate drivers and control circuits. All these components of VSC are combined because they have a certain impact on EMI in the AC drive. Some components influence the impedance of the converter. Whereas the other components such as gate drivers have an impact on the spectrum through the switching behaviour. They can be used to reduce the noise as a part of converter design according to Subsection 1.4.4. Combined together with the FB inverter, all these components of the studied AC drive system are called the power core. Additionally, the power core includes EMI filters.

In order to investigate the impact of different conducted noise reduction techniques (see Section 1.4), the power core has a module structure which allows the implementation of different designs of VSC and

EMI filters. From the other side, such an approach worsens some parameters of the system. This should be also taken into account during the measurements. This section explains the design steps which were made to build the power core of the studied system.

3.1.1 Inverter and Gate Drivers

The main part of the power core in the current research is an inverter. Generally, the inverter consists of the DC link capacitors and power semiconductors. Because the power switches cannot be operated without the gate drivers they are also considered in this section. Design of the gate drives is also closely related to the inverter design [27]. The starting point of any power converter development is the input parameters such as operating voltage and power. According to the electrical distribution system of the future aircraft, the input DC voltage of VSC is equal to 540 V [32]. The maximum load of VSC was selected to be 10 kW covering the typical components in the civil aircraft. There are lots of different solutions to build an inverter. Therefore, it is necessary to justify the selected ones.

Firstly, it was decided to implement SiC MOSFETs and Schottky diodes as switching devices in the designed VSC. Such devices are the most promising power switches for the next-generation power converters. Moreover, the application of SiC MOSFETs is already visible for the implementation in the concepts of MEA and AEA despite the higher prices in comparison to the conventional Si power devices [7, 6]. Additionally, the high-speed switching, which is one of the main concerns of SiC MOSFETs application, gives the possibility to observe some EMI effects more clearly in comparison to Si IGBTs.

The topology of the converter influence the generated conducted noise (see Section 1.4). But the full investigation on the different topologies of the VSC will require a lot of effort to design and to compare all of them. Therefore, only a simple 2-level FB converter was designed during the conducted research. The multi-level topologies are not visible in the near future for the WBG devices due to the increased price. It is also difficult to provide clean switching because of the long commutation paths in the multi-level converters [150]. Moreover, multi-level topologies are not preferable for the aerospace application due to the increased complexity and decreased reliability.

The SCT2080KE SiC MOSFETs and SCS220KG Schottky diodes were chosen for the design of VSC. Their parameters can be found in the datasheet [141, 142]. They fulfil the specified voltage and load requirements. The power semiconductors are combined in a phase-leg and should be connected to the DC link. This connection defines the commutation path. According to Subsection 1.4.4, it is required to decrease the stray inductance in the commutation path in order to reduce the losses and the value of drain-source voltage overshoot. The total value of stray inductance in the commutation path is defined by the interconnection and ESL of the applied DC link capacitors (see Figure 1.24). The power converter based on the high-speed WBG devices should be designed carefully in order to reduce the parasitic inductance in the commutation path for clean switching. Special techniques are always applied for the design of SiC-based power modules [106]. As stray inductance of the commutation path is defined partially by the ESL of the DC link capacitors, the required value of DC link capacitance (20 μF) is provided by a bank of capacitors, which are connected in parallel and series. In this case, it is possible to use capacitors with a lower nominal voltage, which introduce a lower value of ESL as well. The capacitor bank in the designed VSC consists of 4 parallel branches. Each branch consists of 2 capacitors connected

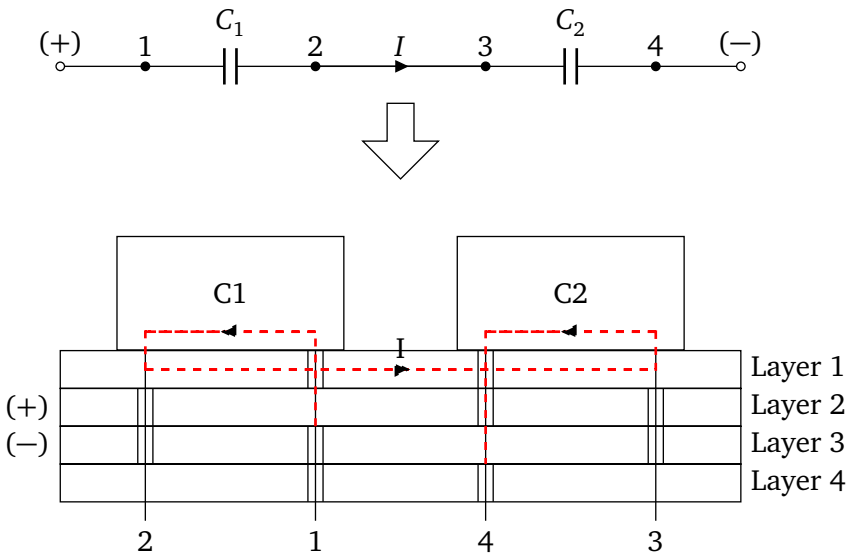


Figure 3.1.: Magnetic field cancellation in the bank of DC link capacitors.

in series. The connection of these capacitors was implemented assuming the magnetic field cancellation which is explained in Figure 3.1.

As can be seen in Figure 3.1, the PCB with 4 layers was used to connect the capacitors in one branch. The outer layers (1 and 4) are connected to the midpoint of the DC link whereas the inner layers (2 and 3) are connected to the positive and negative rail of the DC supply respectively. The plus and minus of the DC supply are also connected to each phase-leg of the inverter as it is shown in Figure 1.24. Close allocation of the inner layers (2 and 3) provides the magnetic field cancellation for the commutation current which flows always in the different directions in the positive and negative rails. The terminals of the DC link capacitors are connected in such manner that the current has the smallest loop (see Figure 3.1). The width of the copper layer, which connects the DC link and the power switches, defines the value of stray inductance as well. Therefore, it is made as wide as possible.

According to Figure 1.6, the FB inverter consists of 3 phase-legs. In order to have a symmetrical value of stray inductance between DC link capacitors and each half-bridge, the whole DC link capacitance is divided into four parallel branches of series-connected capacitors. Each half-bridge is placed between two of such branches. The top view of the designed PCB can be seen in Figure 2.18.

The designed converter is shown in Figure 3.2. The black boxes on the top of the converter are the DC link capacitors, which represent the whole capacitor bank. Each phase-leg, which consists of gate drivers and switches, is placed between 2 branches of the DC link capacitors. The input connector can be observed on the right in Figure 3.2. Output connectors of each phase are allocated in the middle of the half-bridges (three green connectors between the gate drivers in Figure 3.2). The whole PCB is allocated above the aluminium heatsink. The heatsink is used to dissipate the losses generated by the power switches. SiC MOSFETs and Schottky diodes are allocated under the gate drivers and cannot be observed in Figure 3.2. However, as can be seen in Figure 2.18, each half-bridge consist of two MOSFETs in the TO-247 package [142] and two diodes in TO-220 [141]. The power switches and the heatsink are connected mechanically through the thermal interface pads (aluminium oxide). It should be mentioned, that the stray capacitance is observed between the thermal pins of the power switches and the heatsink

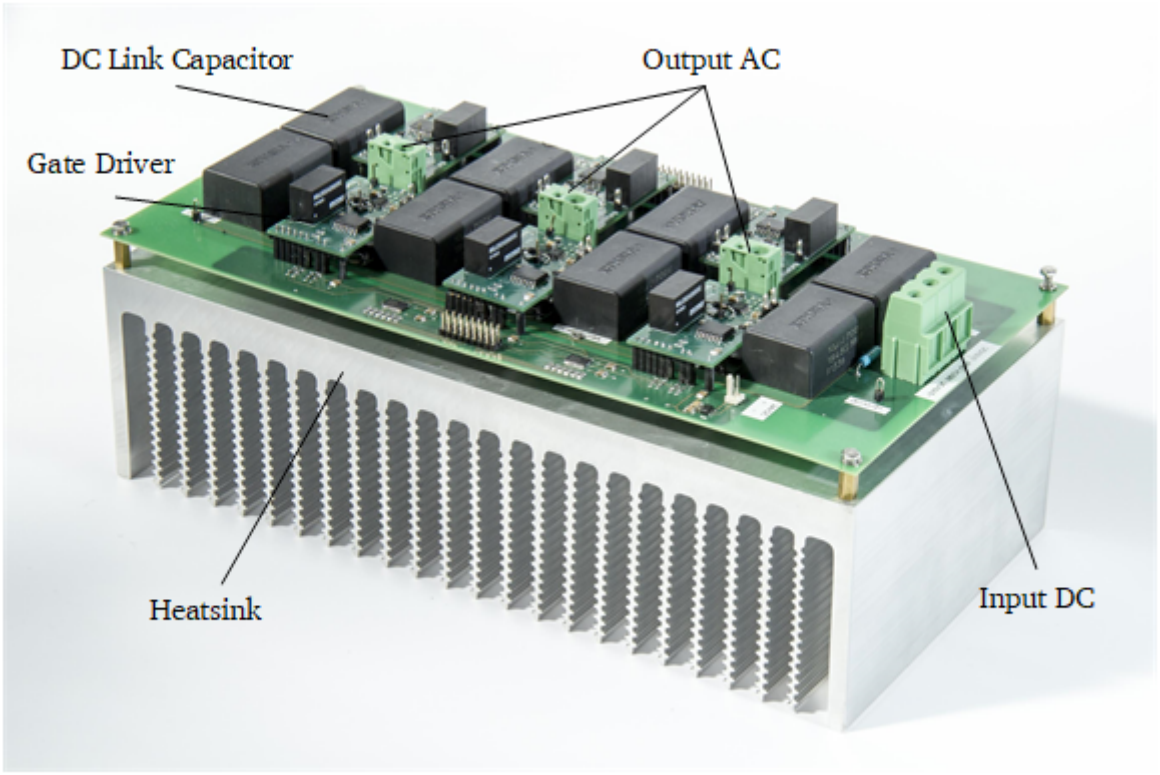


Figure 3.2.: Photo of the designed inverter with gate drivers.

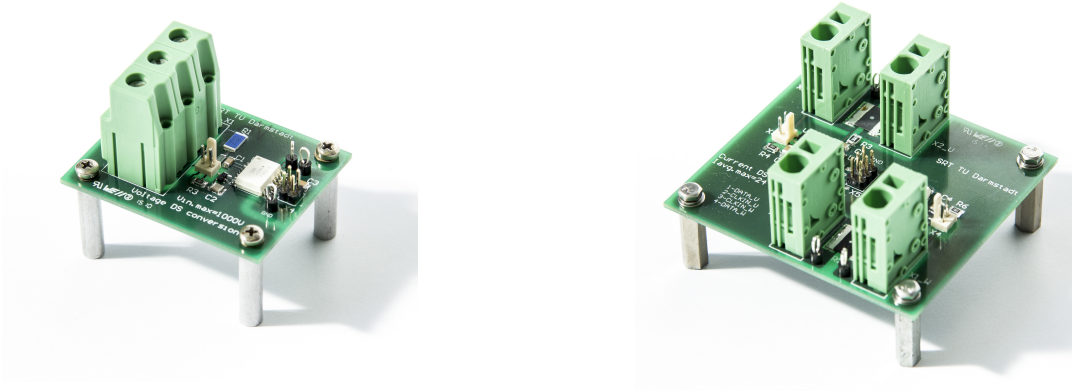
which is normally grounded. These capacitances are considered to have the most significant impact on the CM impedance of the VSC.

The gate drivers can be also observed in Figure 3.2. Each gate driver is allocated above the power switch to have the closest connection to the gate and source pins. All gate drivers (low and high side) have a similar structure and can be detached from the converter in order to replace them or to change the value of the gate resistance. Such a solution is required for further investigation.

The gate drivers have the same structure as in Figure 1.25. The power for the gate side is provided by means of isolated DC/DC converters. They convert the input 28 V DC of the auxiliary power supply into the bipolar DC voltages of 20 V and −5 V for turn-on and turn-off of the SiC MOSFET respectively [143]. The standard integral circuit (IC) is used as a signal shifter. This IC provides the galvanic isolation by means of the planar transformers [151]. Both, the power supply and signal shifting IC contribute also to the high-frequency impedance of VSC due to the parasitic capacitances. The converter presented in Figure 3.2 cannot be operated without control and measurements circuits. The design of these components is considered in the next section.

3.1.2 Additional Components

The control of the VSC requires some information about the state of the system in order to calculate the required output voltage. The information about input/output currents and voltages is also necessary for the protection proposes. Therefore, some sensors are required to provide the functionality of the VSC. Depending on the application of the AC drive number of sensors can be different [27]. For the



(a) DC voltage measurements

(b) AC current measurements

Figure 3.3.: The measurements circuits of the designed power core.

current study, it was decided to implement measurements of the output AC currents and the input DC voltage. Both types of measurements are based on the same IC which provides the delta-sigma conversion of analogue signals [144]. This type of ADC transforms the input voltage into the high-frequency bit-stream using the oversampling technique [152]. The output bit-stream is then converted to the high-resolution digital signal using the digital filters directly in the control system. The analogue signals are obtained using shunt resistors and voltage dividers for the output current and input voltage measurements respectively. The galvanic isolation between the input analogue signal and the output bit-stream is realised by means of the optocoupler in the applied IC [144].

The designed measurements circuits are shown in Figure 3.3. Both circuits for the input voltage in Figure 3.3a and output current measurements in Figure 3.3b are implemented on the separate PCBs. These circuits are connected then to the VSC shown in Figure 3.2 using the power cables. The applied IC with delta-sigma ADCs should be supplied from the high potential and low potential side [144]. All delta-sigma ADCs are supplied from the respective gate drivers. The DC/DC converter of low side gate drivers is used to supply the IC for the voltage measurements. The high side gate drivers provide power for the current measurements in the respective phases. The output currents of VSC are measured only in two phases as can be seen in Figure 3.3b. The current of the 3rd phase is calculated in the control system. The applied ICs introduce also some parasitic capacitance between the high potential and low potential (ground). Therefore, they contribute to the RF impedance of the power core as well.

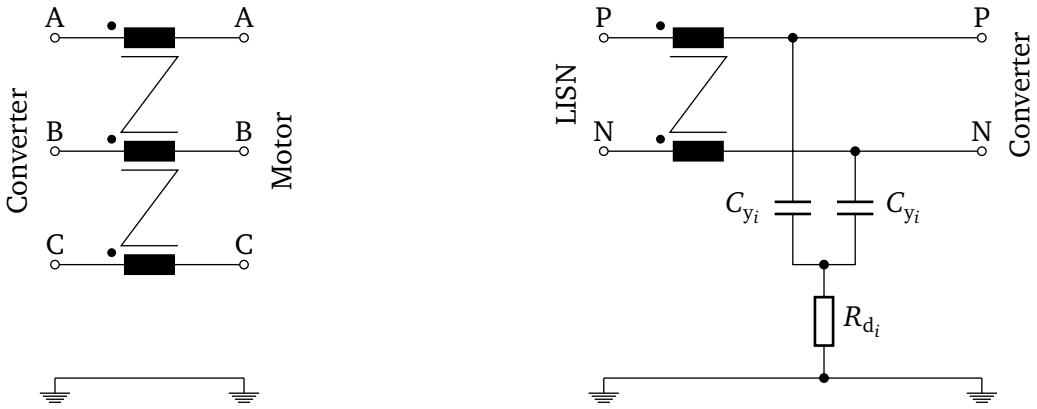
As far as currents and voltages at the input/output of VSC are defined, the control system can calculate the reference voltage for PWM. However, an implementation of the real closed-loop control system will make an investigation on the EMI of VSC more difficult. This is due to the fact that in the closed-loop control, the reference voltage fluctuates near the steady-state value. It would be then difficult to ensure the value of some parameters such as modulation index during the measurements. It was decided to operate the system in the open-loop control where the motor is rotating according to the frequency and amplitude of the applied PWM voltage (U/f-mode) [27]. The U/f characteristics were measured for the applied induction machine. Such an approach ensures the value of the modulation index.

3.1.3 EMI Filters

The maximum noise levels are restricted for all input and output power lines of the EUT according to DO-160 [24]. For the studied AC drive system (see Figure 1.6), it is necessary to provide the corresponding levels of conducted EMI at the input DC line and output three-phase AC cable. It means that the EMI filters should be installed at the input and output of VSC. As it is discussed in Section 1.4, the application of EMI filters cannot be avoided because the other noise reduction techniques influence only a particular frequency range. The improvement of VSC design shows a lower level of noise attenuation in comparison to the EMI filters. The performance of EMI filters can be optimised using different materials, components and structures. According to the goal of the research project, it is required to investigate the influence of EMI filters topologies on the conducted noise as well as the impact of VSC design on the EMI filter. For these purposes, two elementary cells of EMI filters were designed for the installation at the input and output of VSC respectively. Using these cells, it is possible to build the basic structures of EMI filters shown in Table 1.1. The circuits of cells are shown in Figure 3.4. As it is explained in Section 1.2, CM current is the main source of EMI in the AC drives. Therefore, the EMI filters are designed only for the CM noise attenuation using the CM chokes and Y-capacitors.

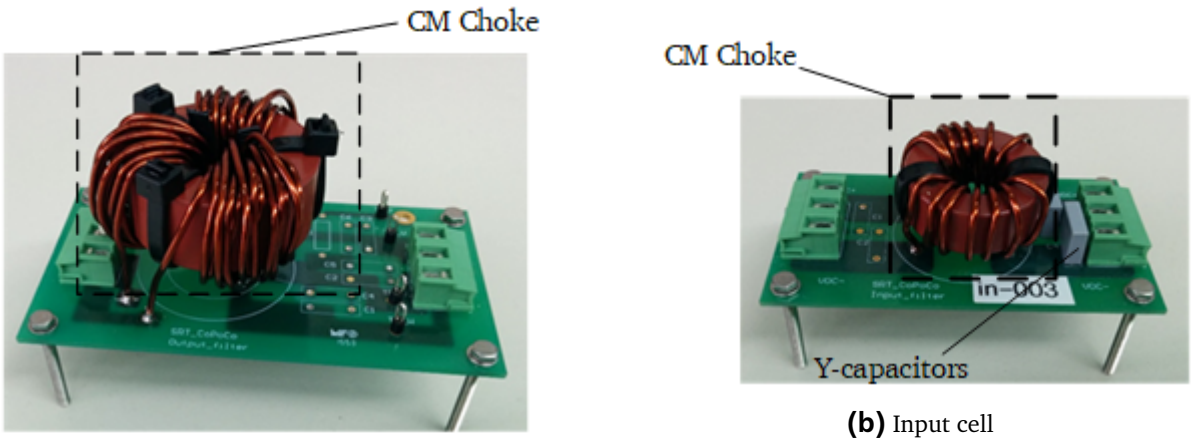
The single cell of the output filter is represented by the three-phase CM choke in Figure 3.4a. It means, that it is possible to implement only one structure of EMI filter (series inductor) at the output of VSC. The lack of Y-capacitors in the output EMI filter is explained by the practice of AC drive application for the civil aircraft. It is hard to ensure the lightning protection of the system in the presence of Y-capacitors at the output of VSC [49]. If lighting will hit the motor, which can be placed in the wing for example, the high voltage pulse will be applied to the Y-capacitors causing the huge leakage currents to the ground. Hence, only the inductor can be implemented at the output of VSC. Through the chain connection of several elementary cells, it is possible to increase the value of CM inductance and attenuation of the output EMI filter. However, only one cell was applied during the measurements.

The elementary cell of the input EMI filter is shown in Figure 3.4b. This cell is based on the CM choke and two Y-capacitors C_{y_i}, which have also additional damping resistance R_{d_i}, where i is the number of the cell. Combining two cells in different directions, it is possible to implement all structures presented



(a) Output cell **(b)** Input cell

Figure 3.4.: The elementary cells for the EMI filter design.



(a) Output cell

(b) Input cell

Figure 3.5.: Photos of elementary cells of EMI filters.

in Table 1.1. Only 2 cells were implemented during the measurements. The following structures can be evaluated with these cells: LC, LCL, LCLC. The conditions for the lighting protection limit the amount of capacitance to ground at the input as well. The total value of Y-capacitors of the whole input EMI filter cannot exceed 150 nF. The lighting pulse can cause high ground leakage currents through the input of VSC with the increased value of Y-capacitance.

The cells of input and output EMI filters are shown in Figure 3.5. The cells are implemented on separate PCBs. They are connected to the VSC using the power cables. The CM chokes of the output filter in Figure 3.5a and input filter in Figure 3.5b were made using cores with the same nanocrystalline material [153]. Nanocrystalline cores are preferable for the design of EMI filters in power electronics due to the increased values of saturation currents in comparison to ferrite. The design of the CM choke has a huge influence on the resulting attenuation of the EMI filter [61]. Optimization of the CM choke itself is already considered in some publications [13]. However, the CM chokes were not changed during the measurements in the conducted research work. The detailed parameters of the applied CM chokes are given in Appendix C.

The input cell is supplied with the CM choke, Y-capacitors and damping resistors according to Figure 3.4b. The resistors cannot be seen in Figure 3.5b because they are placed on the bottom side of the board. Two cells were built which are supplied with the same CM chokes. However, different values of C_{y_i} and R_{d_i} were applied during the measurements for the investigation purposes. Similar to the cell of the output EMI filter, only one type of the CM choke was designed within the project using the same nanocrystalline cores. The parameters of input CM choke can be found in Appendix C as well.

Observing the output and input EMI filter cells in Figure 3.5, it can be concluded that the size of EMI filter is defined mostly by the CM choke. At the same time, the total amount of Y-capacitance is limited making the size of CM choke even bigger. The resulting size of the EMI filter is comparable with other parts of the power core: switches, gate driver and DC link capacitors.

3.1.4 Power Core Functionality

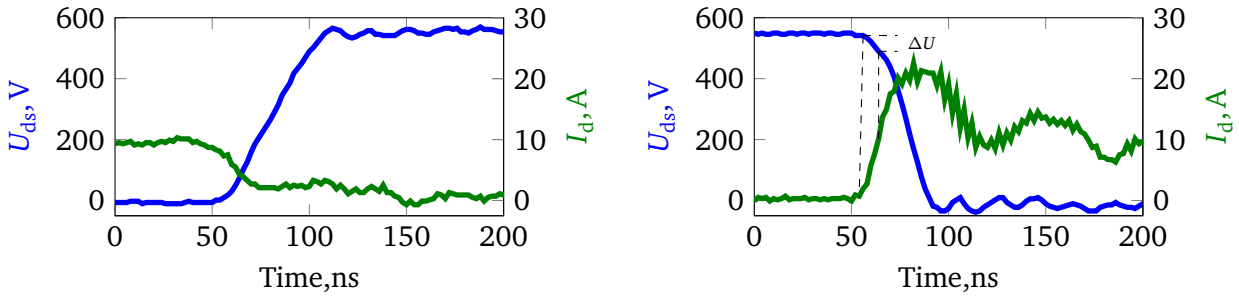
All components of the power core were assembled building the VSC. For the newly designed systems, it is necessary to make commissioning of all parts in order to prove their functionality. This section presents some of the measurements results which were obtained during the commissioning of the designed VSC. These results are helpful for further investigation in Chapter 4.

As it is explained in Subsection 1.4.4, the hardware design of the VSC influences the EMI behaviour of the AC drive. The RF part of the conducted noise generated by the VSC is influenced by the switching behaviour of power semiconductors and by the impedance of the whole converter (power core). The initial information about the switching process (rise and fall times, energy loss and etc.) can be found in the datasheets of the applied power switches [141, 142]. However, the switching behaviour is influenced by the gate drivers and by the stray parameters in the commutation path, i.e. the design of the VSC. Therefore, it is preferred to measure the switching behaviour of VSC during the commissioning in order to ensure the exact values of switching losses. The switching behaviour of designed VSC was measured using the inductive load switching (double pulse test) similar as in [100]. The inductive load was set to be equal to 3 mH that is close to the inductance of the typical induction machine. The considered inductor was applied to each phase of the studied VSC. The DC link voltage is equal to the nominal input voltage of the studied system (540 V). The test were conducted under the output current of 9 A that is equal to the average value of the drain current at the maximum load. One power switch conducts only one half-wave of the output sinusoidal current [27].

According to (1.19), it is required to measure the drain current I_d and drain-source voltage U_ds to estimate the value of energy loss during one switching event. These parameters were measured using the differential probe and Rogowski coils (see Appendix D) for the voltage and current respectively. The resulting graphs are shown in Figure 3.6. It can be seen, that the measured switching behaviour differs slightly from theoretical curves in Figure 1.24b. The voltage U_ds starts to increase during the turn-off in Figure 3.6a as it is expected (see Figure 1.24b). However, the drain current I_d decreases at the same time. This effect is caused by the external Schottky free-wheeling diodes which are not considered in Figure 1.24. If the external diodes are applied, the part of the I_d moves in the external diode to charge the anode-cathode capacitance. As it is explained in Subsection 1.4.4, the duration of voltage rise time is defined by the output current and by the value of C_ds. Due to the relatively small value of the output current, the voltage overshoot is not observed in the measurements. However, some ringing is presented in U_ds similar to the measurements results which were obtained in [100].

The measured turn-on process, which is presented in Figure 3.6b, corresponds to the theoretical behaviour in Figure 1.24. The only difference is that the turn-on process in Figure 1.24 was considered for the low side switch S_2. The drain-source voltage on low side switch S_2 is equal to $U_\mathrm{dc} - U_\mathrm{ds}$. The turn-on process in Figure 3.6b starts with a current rise. After the drain current I_d reaches the value of output current (9 A), the drain-source voltage starts to fall. Despite, that the Schottky free-wheeling diodes with almost zero reverse recovery were applied, current overshoot can be observed due to the discharge of C_ds. This corresponds also to the results obtained in [99, 100].

Due to the presence of stray inductance in the commutation path, a small value of the voltage decrease $\Delta U = 52\,\mathrm{V}$ can be observed during the current rise in Figure 3.6b. By measuring the rise time of the drain



(a) Turn-off **(b)** Turn-on

Figure 3.6.: The measured switching behaviour of VSC under inductive load switching ($R_g = 0\,\Omega$).

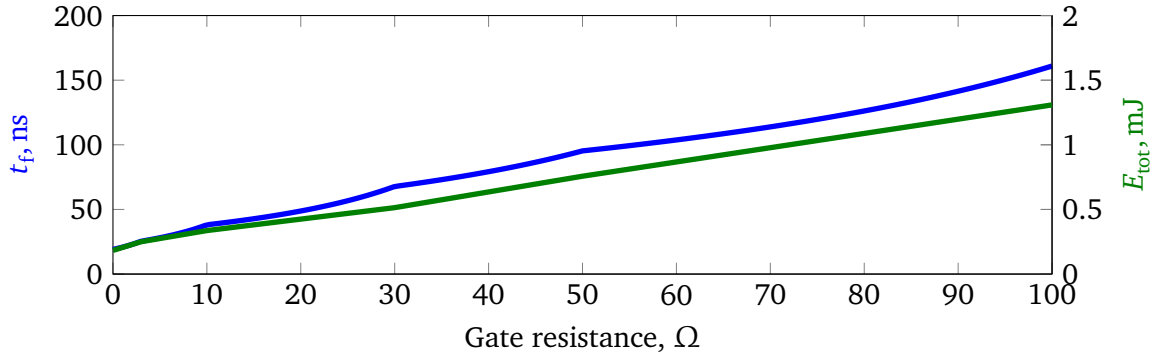


Figure 3.7.: Impact of gate resistance on switching energy loss and voltage fall time.

current ($t_{r.i}$) which is equal to 15 ns, it is possible to find the approximate value of total stray inductance in the commutation path [27]. For the current test, the estimated value of L_Σ is equal to 35 nH. Taking into account the value of DC link capacitors ESL (25 nH) and lead inductance of the TO-247 package (7 nH according to [146]), it is possible to conclude that the applied field cancellation techniques are efficient (see Section 3.1).

Using (1.19) and the measured data in Figure 3.6, the total switching energy loss E_{tot} per one commutation can be defined for the designed power core. Together with the sampling frequency of PWM, these values define the switching losses in the VSC. The duration of the turn-on process increases with the value R_g leading to the higher switching losses. As it is discussed in Subsection 1.4.4 and shown in Subsection 2.3.1, the RF spectrum of VSC output voltage is also influenced by the voltage fall time t_f of SiC MOSFET during turn-on. The value of t_f is defined between 10% and 90% of the input DC link voltage [27].

Because the value of E_{tot} and t_f are essential for the design of VSC and for the EMI analysis, these two values were estimated using the measurements under different values of R_g. The dependence of the total energy loss per one commutation cycle and voltage fall time during turn-on from the value of gate resistance is shown in Figure 3.7. Both parameters rise linearly with the increase of the gate resistance. The lowest value of 20 ns for t_f and 0.2 mJ of E_{tot} were achieved with $R_g = 0$. Increase of the voltage fall time reduces the amplitudes of RF harmonics in VSC output voltage but at the cost of the switching losses.

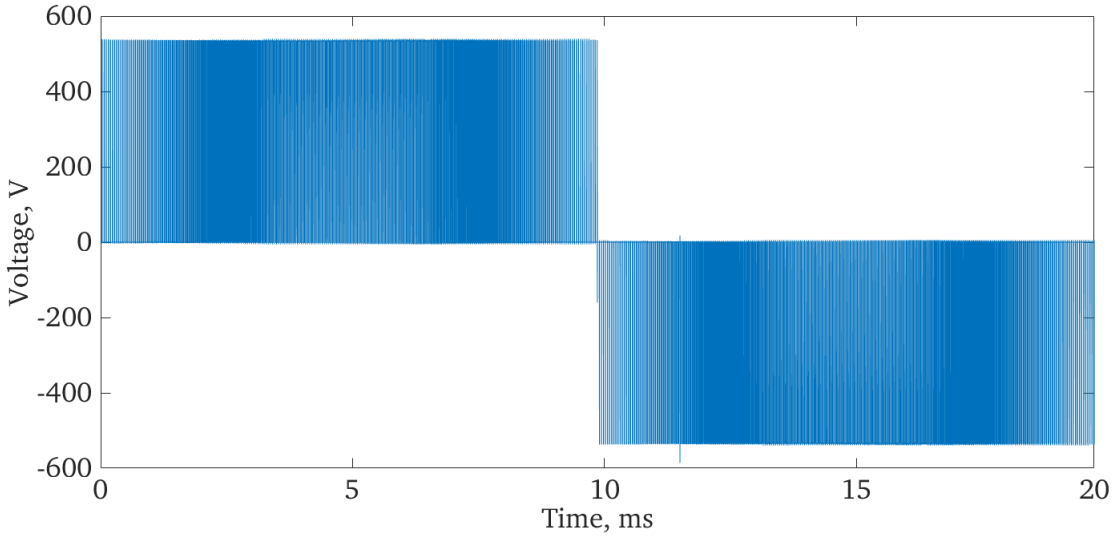


Figure 3.8.: The measured output line voltage (DM_1) of designed VSC in the idle mode.

After analysis of the switching process, the designed VSC was operated under PWM with the motor in the idle mode. The phase-to-phase voltage (DM_1) was measured to ensure the correctness of the applied control software. The shape of output PWM voltage under operation with the reference sampling frequency of 24 kHz is shown in Figure 3.8. Due to the relatively high sampling frequency, the pulses can be hardly recognized with the available resolution on the fundamental period of 20 ms. However, the curve and its spectrum correspond to the theoretical values of SVPWM presented in [27]. The phase currents, which are presented in Figure 2.12 and Figure 2.12, were obtained with the same PWM voltage during operation with the motor in different modes.

The functionality of the designed VSC (power core) is explored using the measurements in this section. The presented results have also a practical meaning. In Subsection 2.3.1, the voltage shown in Figure 3.8 is analysed in order to improve the spectral representation of voltage sources for the frequency domain models. All rising and falling edges of the considered waveform are evaluated showing the effect of MOSFET and diode commutations described in Subsection 1.4.4. The dependence of MOSFET voltage fall time from gate resistance in Figure 3.7 is used to generate the spectrum of the inverter output voltage under different load conditions (see Figure 2.14). The switching energy loss was also estimated during the measurements to ensure the capability of the applied cooling system of the power core.

3.2 Description of the Measurement Setup

This section describes the implementation of the setup for conducted noise measurements. The obtained results are used further in Chapter 3 for the investigation and model validation purposes. The section gives also some details about the other parts of the AC drive system beside the VSC. Due to the high cost of aerospace components, they were replaced with standard industrial solutions. Moreover, some aspects of the applied standard, which were ignored during the measurements, are also discussed in this section.

Table 3.1.: Cable parameters.

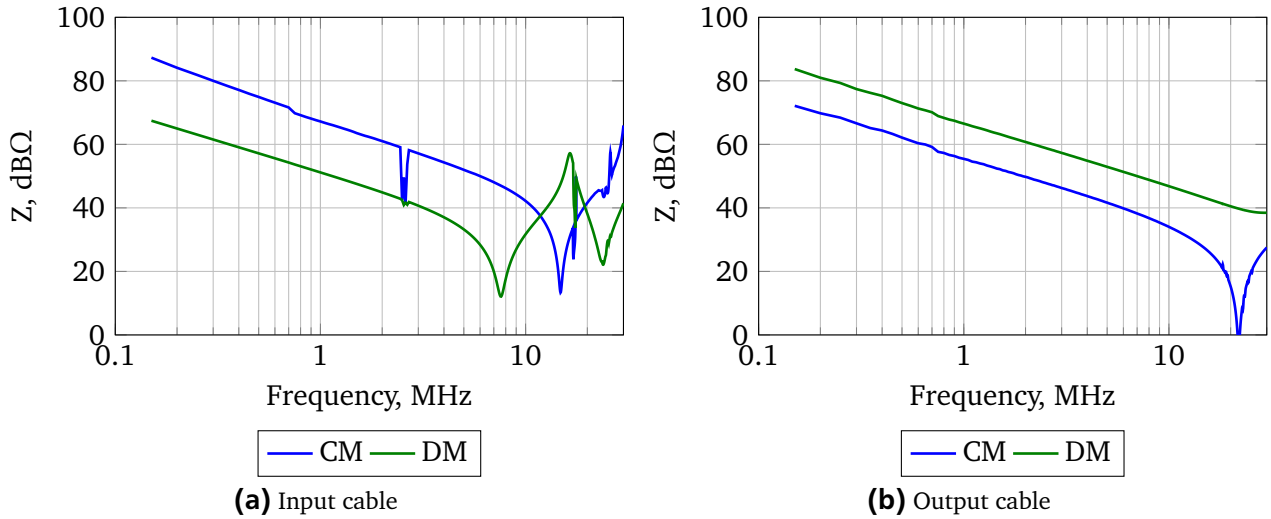
Type	Length, m	Wire cross section, mm^2	C', $pF\,m^{-1}$	Ľ, $nH\,m^{-1}$
2-Wire, unshielded cable	5	4	13	115
3-Wire, shielded cable	1	4	117	290

The structure of the setup for conducted noise measurements according to DO-160 can be seen in Figure 1.1. The EUT is the power core, which contains the VSC, its control and EMI filters (see Section 3.1). The power supply is not predefined by DO-160 [24]. But it should be able to provide the required voltage of 540 V and power of 10 kW. The LISN with 10 μF decoupling capacitors were ordered from the selected supplier. Its resulting impedance corresponds to the impedance presented in Figure 1.2. The input and output cables, which connect the EUT with power supply and load respectively, should be taken according to the specification of the AC drive [24]. The simple industrial cables were applied. Their parameters are listed in Table 3.1.

According to the specification, the input cable should be unshielded, whereas the output three-phase cable should be equipped with a shield. The lengths of the cables were provided in the specification as well (see Table 3.1). The cross-section area was chosen to be the same for the input and output cables. The value of the capacitance and inductance per unit length were estimated using single-ended S-parameter measurements. The 6-port S-parameters of the output cable were measured connecting the shield of the cable to the ground of VNA. Then, the S-parameters were converted to Z- and Y-parameters (see Appendix B). The resulting parameters are used to obtain the values of C' and Ľ. In order to provide the common ground path for the unshielded cable, it was put over the copper plate with 10 cm distance. This distance is also specified by DO-160 for the EMI measurements [24]. The copper plate was connected to the ground of VNA. The 4-port S-parameters of the input cable were measured giving the possibility to obtain the values of C' and Ľ. As it is expected, the value of capacitance per length of input cable is much smaller in comparison to the shielded output cable (see Table 3.1). In opposite the inductance per length is lower in case of the shielded cable. The measured values correspond to the values of typical power cables which were estimated experimentally and theoretically in [114].

The measured single-ended Z-parameters of the cables were converted further into MM by means of (2.13) for the simulation purposes. According to the presented in Subsection 2.2.2 conversion, the resulting impedances Z_{11} and Z_{22} are representing the open-circuit impedances for the CM and DM respectively. These impedances are often used to characterize the components of an AC drive for EMI simulation [42, 44]. The corresponding impedances for the applied power cables can be observed in Figure 3.9. Both cables show capacitive behaviour in the lower frequency range. However, the resonances can be observed in both cases after the frequency of 10 MHz that corresponds to the transmission line theory [114].

Due to the higher value of the specified length for the input cable (see Table 3.1), the effect of travelling waves in Figure 3.9a is observed at 15 MHz and 8 MHz for CM and DM respectively. The behaviour of the CM impedance depends on the position of the cable due to the lack of the shield. If a lower distance between cable and copper ground is applied, the value of capacitance per unit length increases. The CM and DM open-circuit impedances of the output cable are presented in Figure 3.9b. Due to the smaller



(a) Input cable

(b) Output cable

Figure 3.9.: The CM (Z_{11}) and DM (Z_{22}) open-circuit impedances of the cables.

Table 3.2.: Motor parameters.

Type	Power, kW	Voltage, V	Frequency, Hz	Speed, min^{-1}	$\cos\phi$
ACM 160MA-2/HE	11	400	50	2930	0.88

length of the output cable, the effect of travelling waves starts to influence the CM impedance only above 20 MHz. The effect of long cables is not observed for the DM open-circuit impedance of the output cable in Figure 3.9b. Due to the presence of shield, the CM und DM impedances are almost independent from the cable position towards the copper plate.

As it is explained in Subsection 2.2.2, the MM parameters can be used to analyse and to model the DM and CM separately by combining the respective 2-port networks from the components of 4-port or 6-port networks. Moreover, the Z-parameters can be converted to Y-parameters that gives the possibility to consider short-circuit impedance of the system too. These parameters are not presented here. However, they were also analysed within the conducted research showing good accordance with the theoretical behaviour.

The last part of the EMI measurements according to DO-160 is the load which is also defined by the specification of equipment. In the case of the AC drive, the motor is assumed to be the load for the EUT (VSC). An industry-standard induction motor was considered for the experiments. Its nominal parameters are listed in Table 3.2. These parameters are valid for the delta connection of the windings. Alternatively, the same motor can be connected in star with an increased voltage. It can be also supplied with 60 Hz that leads to increase of the nominal speed.

In order to implement the various loading conditions, the induction machine was mechanically coupled with a DC motor. The whole assembly is shown in Figure 3.10. The applied DC machine was supplied with a 4-quadrant rectifier. It gives the possibility to operate the DC machine in the generator mode. The DC motor is used to apply the mechanical load (torque) to the induction motor. The resulting load can be varied from 0 up to nominal power of the DC machine (15 kW). The mechanical coupler, which connects the shaft of the AC motor and DC generator, is electrically isolated. However, the DC machine

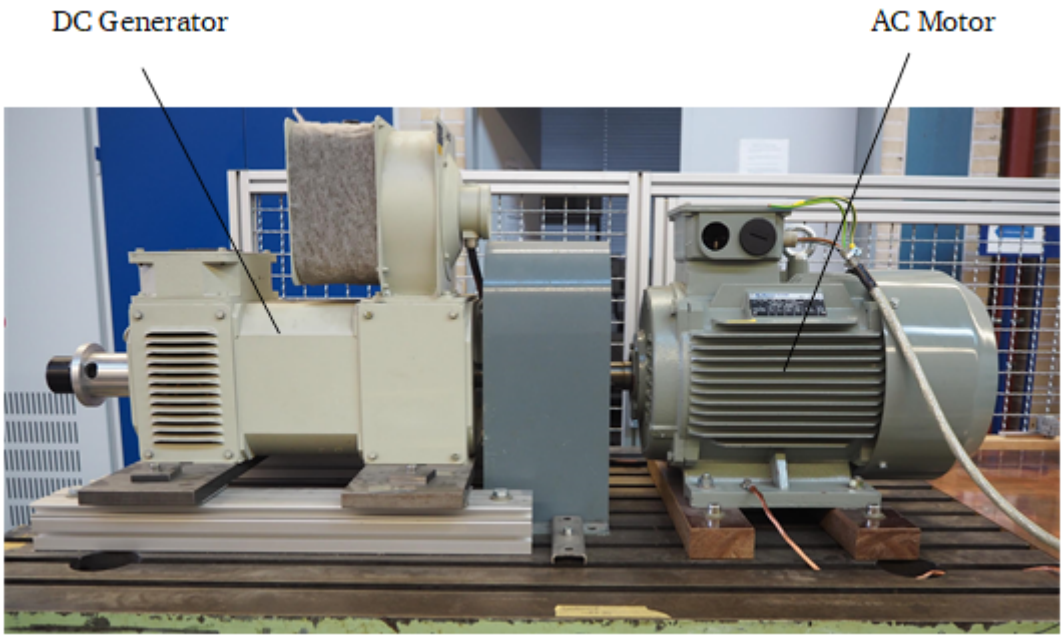


Figure 3.10.: Photo of motor-generator setup.

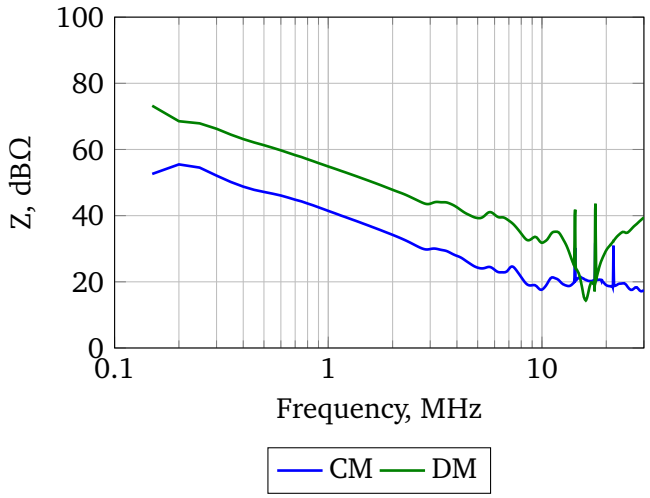


Figure 3.11.: The CM (Z_{11}) and DM (Z_{22}) open-circuit impedances of the motor.

can influence the impedance of the motor. Therefore the S-parameters of the motor were measured including the whole load fixture. Similar to the cables, the S-parameters of the motor were converted to MM Z-parameters that gives the possibility to study its DM and CM impedance behaviour. In Subsection 2.2.3, it is explained how to apply MM conversion to the delta connected motors. The resulting open-circuit CM/DM impedances of the applied AC motor are shown in Figure 3.11 (Z_{11} and Z_{22} of MM parameters for CM and DM respectively).

As can be seen in Figure 3.11, the motor shows the capacitive behaviour in the frequency range of interest (from 150 kHz to 30 MHz) in both cases for DM and CM. Such behaviour corresponds to the measurements which were conducted in [44]. In the 1st frequency domain models [116], the motor was represented by a single capacitor. According to Figure 3.11 such representation is valid only up to

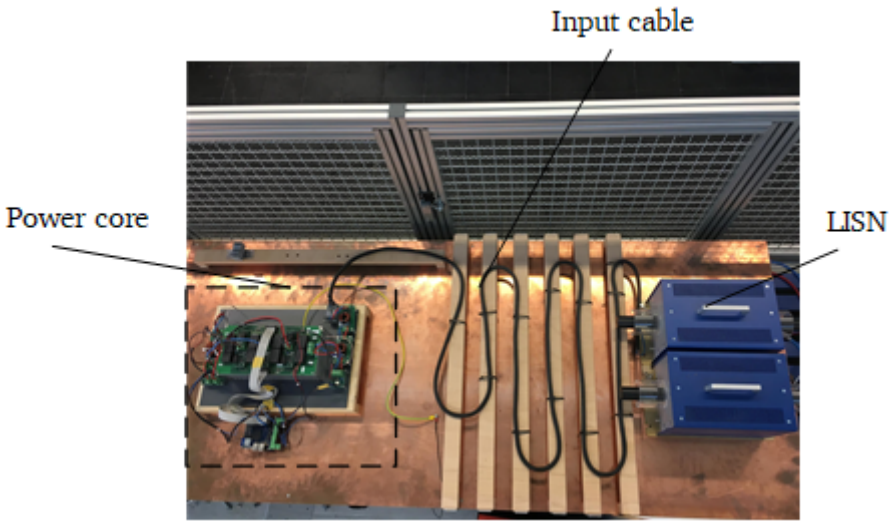


Figure 3.12.: Photo of setup for conducted EMI measurements (top view).

several MHz. For the applied motor a resonance can be observed at DM impedance at the frequency above 10 MHz.

All components of the specified AC drive system were arranged according to the DO-160 for conducted noise measurements. The photo with a top view of the constructed setup for EMI measurements is shown in Figure 3.12. On the right, two LISNs for each phase connect the DC power supply and the input cable. The cable is connected on the other side with the designed power core. The output cable is not shown in Figure 3.12. However, it is arranged in a similar manner as the input cable. All components of the system are allocated above the copper plate.

According to the requirements given in DO-160 [24], the noise is measured with the current probes on all interconnections on the distance of 50 mm from the EUT. The applied current probe is 6600 from Pearson which has a bandwidth (−3 dB) from 40 Hz up to 120 MHz. The main characteristic of the current probe is the transfer impedance. It describes the relationship between the measured current and output voltage [154]. The transfer impedance is normally given as a curve in the frequency domain. This curve should be then added to the measured values acquired by the spectrum analyser. All parameters of the current probe including its transfer impedance are given in Appendix D. The signals from the current probe were applied either to spectrum analyser with settings according to DO-160 or to the scope in order to provide the time domain analysis. The time domain data was also converted to the frequency domain utilizing SWDFT. Subsection 2.4.2 explains how to consider parameters of the spectrum analyser during the conversion of time domain data to the frequency domain. The parameters of utilized spectrum analyser and oscilloscope are also presented in Appendix D.

This section describes all components of the AC drive system besides the power core which have the most significant impact on the impedance of the noise propagation path. Using components of the MM Z-parameters, the CM and DM open-circuit impedances of the cables and motor are extracted and presented in this section. It is shown that the applied components have mostly capacitive behaviour below certain frequencies. However, the impedances can change in a wide range due to the transmission line effects at RF. Finally, the arrangement of the setup for the conducted EMI measurements is presented.

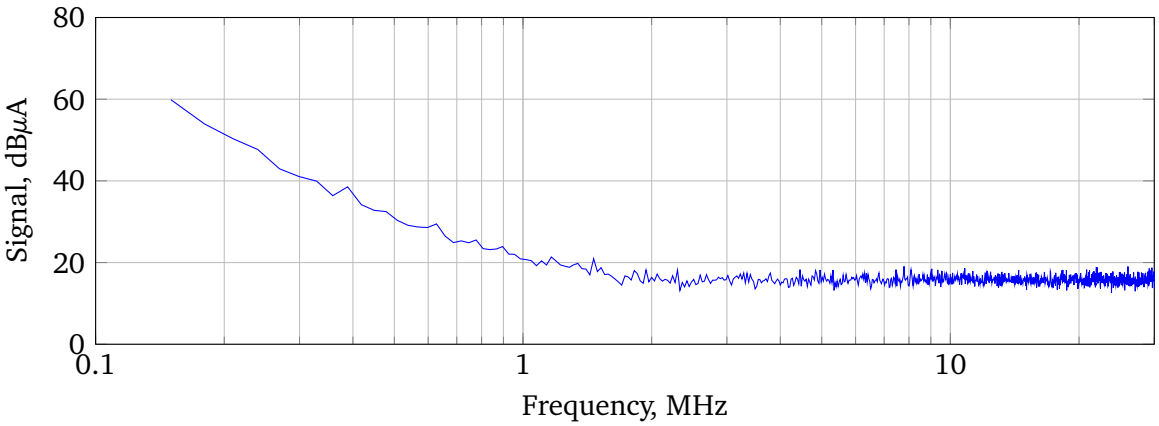


Figure 3.13.: The noise floor achieved with the applied measurement devices.

The presented setup was constructed trying to fulfil the basic requirements according to DO-160. However, the presented setup neglects some aspect of DO-160 that can cause some uncertainties. These uncertainties are discussed in the next section.

3.3 Measurement Uncertainties

The implemented VSC and the setup for EMI measurements are described in the previous section. It is explained that the VSC was designed in order to have the flexibility for the investigation purposes. For example, it is possible to detach and to replace the gate drivers. In that case, the designed VSC has some differences with a real industrial prototype of an inverter. Moreover, some aspects of DO-160 were ignored. This can impact the evaluation of measurements results which are further compared with a simulation results in Chapter 4. This section discusses the uncertainties of the measurement setup.

The first uncertainty is caused by the limitation of the applied spectrum analysers. This limitation is the noise floor. It defines the value of the lowest possible amplitude of the signal which can be measured. Initial information about the noise floor of the spectrum analyser can be found in its datasheet [155]. However, this value depends strongly on the device settings (frequency range, RBW, type of detection, etc.). Moreover, the measured signal in dBm should be further converted to dBμA using the transfer impedance of the applied current probe (see Appendix D). In order to evaluate the maximum and minimum values, which can be measured with the applied measurement devices, the transfer impedance was multiplied numerically with a signal which was acquired with the spectrum analyser. The parameters of the spectrum analyser were set according to DO-160. Its input port was connected with 50 Ω impedance during the measurement. The resulting curve can be observed in Figure 3.13. The level of the measured signal decreases with a frequency increase. This corresponds to the behaviour given in the datasheet of N9020A [155]. The minimum value reached at RF is equal to 18 dBμA.

Comparing the measured curve in Figure 3.13 with the limits according to DO-160 (see Figure 1.4), it can be concluded that the resulting noise floor lies exactly under the limit of category L, M, H. In that case, it is hard to evaluate the noise level to which this limit should be applied (the input noise of VSC, see Section 1.1). Therefore, current work is mostly concentrated on the noise level observed at the output of VSC according to DO-160. Due to the relatively high amplitude of the CM current at the

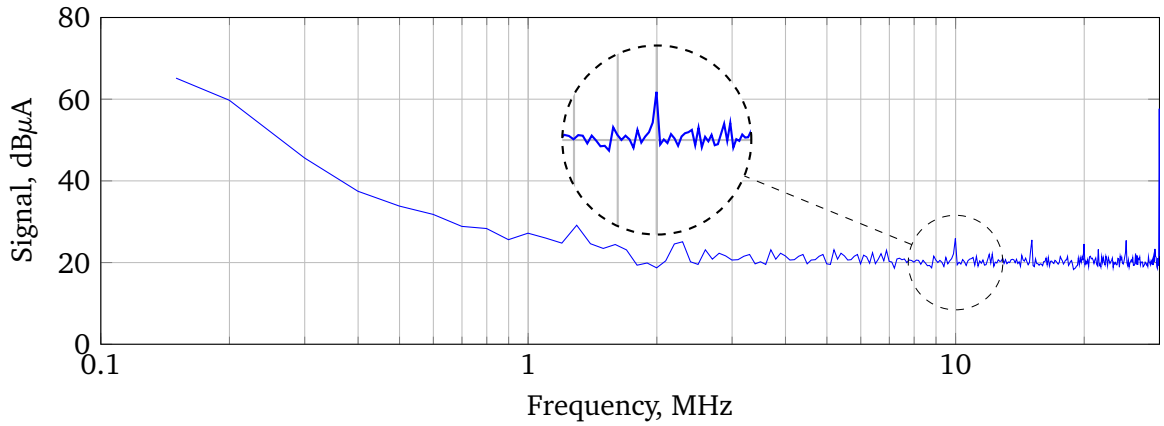


Figure 3.14.: The output conducted noise generated by the low voltage components of VSC.

output at the frequency equal to the sampling frequency of PWM (see Table 4.1), the output conducted noise is always measured with 4 dB attenuation. Application of attenuators increases the noise floor at the same level as well. But even in this case, there is a suitable margin between the limit for the output current (category B in Figure 1.4) and the resulting noise floor in Figure 3.13.

The noise level of EUT is defined on all power lines which are connected to the EUT [24]. Besides the main power line, the designed power core is also supplied with a low voltage power supply of 28 V. This value corresponds to the low voltage bus of the typical aircraft electrical power system [32]. The low voltage is required for the control and electronic circuits (e.g. measurements and logic circuits) and for the gate drivers. All these elements generate conducted EMI as well [156]. In this case, it is also necessary to apply the DO-160 requirements to the low voltage power line. This line should be also connected through the LISN and wired according to the specification. However, as the research is concentrated only on the conducted noise generated by the VSC, this part was ignored during the construction of the setup for the EMI measurements. The low voltage power supply was connected directly to the VSC. The power supply itself contribute in that case to the system impedance and can also be a source of additional EM noise. It should be also mentioned, that the VSC can be operated without a low voltage supply. But such operation will require the implementation of a DC/DC converter which generates EM noise too.

The parametrization of the control system (PWM sampling frequency, modulation index, dead time, etc.) is provided using the USB connection between the PC and control board. This connection can also contribute to the impedance of VSC and can also cause additional noise. In order to see the influence of the connection between PC and control board as well as the impact of low voltage power supply, the output conducted noise was measured at the output of VSC in the standby mode. In this mode, the VSC was not supplied with the input 540 V DC supply. The PWM signals were not generated as well. The resulting noise level in the standby mode can be observed in Figure 3.14. The noise was measured at the output with 4 dB attenuation. It explains the increased level in comparison to measurements with terminated spectrum analyser Figure 3.13. The significant additional noise levels are not observed in Figure 3.14 besides the small narrow-band peaks at 10 MHz. This noise is almost always observed in

the measurements results in Chapter 4. The considered peaks can be caused by any reason mentioned above: low voltage power supply, gate driver or connection to PC.

This section discusses the non-ideal conditions of the designed setup for EMI measurements. Due to the limitation of the available measurement devices, current work is mostly concentrated on the output noise which can be studied with a better resolution. The impact of the auxiliary low voltage power supply and USB connection is also discussed in this section. Due to the presence of such uncertainties, the additional narrow-band noise level can be observed in the measurements results. Such type of noise is out the research scope. Therefore, it is simply ignored during investigation and model validation.

3.4 Description of Simulation Related Parameters

Section 3.1 describes the VSC which was built for the experiments. The module design of the VSC can suffer from the EMI behaviour point of view. But it provides the possibility to test and to evaluate different configurations of the converter itself and/or EMI filters. Implementation of such a structure was aimed to reach two goals of the research project: to test different conducted noise reduction techniques (see Section 1.4) and to validate the model for the EMI prediction proposed in Chapter 2. The number of system parameters, which can be considered in the simulation, is very high. Most of them can be implemented on the developed setup. This section gives a link between parameters which were considered in the model and which were implemented in the measurement setup. A brief overview of the impact of these parameters on the conducted EMI in the AC drives is also given with an explanation of how these parameters were changed during the measurements.

All parameters of the studied system are summarised in Table 3.3. The 1^{st} group of the parameters presented in Table 3.3 corresponds to the control system of the VSC. These are the clocking frequency of the control unit f_{clk} (FPGA) and the type of PWM. The value of f_{clk} defines the resolution of PWM (the minimum time step of the PWM signal). This value is defined by the chosen FPGA platform (DBC5CEFA7). The 2^{nd} parameter of the control system is a type of PWM. Three types of PWM were implemented for the tests: conventional symmetric SVPWM (see Figure 1.21a), DPWM (see Figure 1.21b) and AZPWM (see Figure 1.22). All these techniques and their influence on the conducted EMI were considered in Subsection 1.4.3

The next group of parameters is related to the PWM itself. All these parameters can be easily changed in the designed control system. The impact of the sampling frequency and modulation index on the spectrum of output PWM voltage is explained in Section 1.2. The dead time, which influences the switching behaviour, is also considered in Section 1.4. All these parameters are also taken into account during the generation of time domain output voltage in Figure 2.14 for the simulation.

The layout and components of the inverter were fixed during the measurements. Therefore, they are not considered in Table 3.3 for the group of VSC parameters. The parameters presented in Table 3.3 define the shape of the output PWM voltage. The input DC voltage is given by the AC drive specification. Its value is equal to 540 V (±270 V bipolar DC power supply). Such parameters as drain-source charge Q_{ds} and switching time during commutation of MOSFET are required for the representation of the real switching behaviour in the simulation (see Section 2.3). The value of t_f is defined by the MOSFET and its gate driver. The commutation time of MOSFET was varied during the measurements by means of the gate resistance R_g (see Figure 1.25). The relationship between R_g and t_f was obtained during the

Table 3.3.: Simulation related parameters of the measurement system.

Parameter	Symbol	Values Range	Reference Value
Control system			
System frequency	f_{clk}	50 MHz	50 MHz
Type of PWM	-	SVPWM, DPWM, AZPWM	SVPWM
PWM			
Sampling frequency	f_{s}	10..50 kHz	24 kHz
Modulation index	m	0.2..0.9	0.9
Dead time	t_{dt}	300..1000 ns	500 ns
VSC			
Input voltage	U_{dc}	540 V	540 V
Voltage commutation time (MOSFET)	t_{f}	20..100 ns	20 ns
Drain-source charge	Q_{ds}	4 nC	4 nC
Load			
Motor inductance	L_{m}	3.3 mH	3.3 mH
Motor load	P	1.5..7.5 kW	1.5 kW
EMI Filters			
Input filter structure	-	LC, LCL, LCLC	LCL
Input Y-capacitance 1$^{\mathrm{st}}$-section	C_{y_1}	0.1-33 nF	33 nF
Input Y-capacitance 2$^{\mathrm{nd}}$-section	C_{y_2}	0.1-33 nF	33 nF
Input damping resistance 1$^{\mathrm{st}}$-section	R_{d_1}	1-10 Ω	1 Ω
Input damping resistance 2$^{\mathrm{nd}}$-section	R_{d_1}	1-10 Ω	1 Ω
Output filter structure	-	L	L

switching behaviour measurements. This relationship is presented in Figure 3.7. All parameters of VSC are also considered in the generated PWM signal for simulation (see Figure 2.14).

From the EMI point of view, the motor defines the impedance of the propagation path for the conducted noise. However, as it is shown in Section 2.3, the fundamental frequency behaviour of the load impacts the spectrum of the VSC output voltage through the diode commutations. The motor inductance was measured and used to obtain the value of the reactive power for the calculation of time domain waveform of PWM voltage (see Figure 2.14). As it was explained in the previous sections, the motor is loaded mechanically by means of the DC machine. This provides the ability to change the value of the active power in the AC drive. However, the minimum value of the active power of 1.5 kW is required to rotate the motor with the coupled rotor of the DC machine at the nominal speed (idle mode power).

Different structures of the EMI filters were also applied during the measurements. Because conducted noise level is limited at DC and AC sides (see Section 1.1), it is required to install the EMI filters at the input and output of the VSC. The proposed in Section 3.1 cells can be used to achieve different structures of the EMI filters. The input cells were implemented using the CM choke and Y-capacitors with the damping resistors. Using 2 input cells, it is possible to build various structures of the input EMI filter according to Table 3.3. The input CM choke was fixed during the measurements. Its parameters can be found in Appendix C. However, different values of C_{y_i} and R_{d_i} were evaluated in the research work. Due to the limitation associated with lightning protection (see Section 3.1), the output cell of the EMI filter consist only of the CM choke. The impedance of this choke is also given in Appendix C. The CM chokes were characterised using measured MM parameters for the proposed frequency domain model. The capacitors were represented by the simple 1^{st}-order models (see Figure 1.15) during the simulation.

The number of parameters is very high according to Table 3.3. It gives the possibility to investigate different noise reduction techniques which were presented in Section 1.4. All these parameters can be also considered during the simulation in the model proposed in Chapter 2. For all presented in current work measurement and simulation results, it is assumed that the experiments are conducted under the reference parameters from Table 3.3. If some parameters were changed for a certain experiment, it is clearly mentioned under the corresponding results.

4 Investigation on Conducted Noise Reduction Techniques

The problem of the conducted noise generated by the VSC in the AC drives is considered in Chapter 1. Different types of conducted EMI are discussed (CM, DM and MM) as well as the methods for the improvement of the EMI behaviour. It is shown that besides the classical approach such as EMI filters, the generated conducted noise can be reduced by means of the converter design. Different aspects of the VSC design influence the respective types of the conducted emission: DM or CM, low- or high-frequency. The techniques of conducted noise reduction considered in Section 1.4 can influence the different parameters of a VSC such as efficiency, power density, reliability. Moreover, all these techniques can be combined with each other improving the overall performance of the VSC from the EMI point of view. At the moment, there is a lack of research works which consider all types of EMI reduction in the AC drives combined with each other. This chapter provides such an investigation using experimental and simulation results. It is almost impossible to investigate absolutely all noise reduction techniques within one research project. For example, the topology of the VSC was fixed during the investigation because only FB inverter was designed during the research work (see Chapter 3). However, the conducted experiments provide the possibility to investigate the impact of VSC on the conducted EMI.

Chapter 2 shows that the model is required for the prediction of conducted EMI in AC drives which can be used to consider the EMI during the design of a VSC. A new frequency domain model is proposed which takes into account all possible reduction techniques including the EMI filters. The proposed model has a low computational demand that allows the application of this model in the optimization procedure. However, increase of the computational efficiency is obtained at the cost of the simulation accuracy. Some effects of the real behaviour of the VSC are ignored. This chapter compares also the conducted noise levels which were obtained by means of simulation and measurements. A relationship between the model parameters and the designed VSC is described Section 3.4.

Despite, that some reductions techniques were not considered during the experiments, the number of VSC and AC drive parameters, which were changed during the investigation, is very high. The listing of all parameters for each experimental result would overload this chapter. Therefore, for all given results, it is assumed that the simulation and measurements were conducted under the reference parameters from Table 3.3. If some parameters of AC drive or VSC were changed for a particular experiment, it is clearly mentioned for the corresponding figure.

All results were evaluated for the frequency range from 150 kHz up to 30 MHz because another RBW of the spectrum analyser is required according to DO-160 for the frequencies above 30 MHz [24]. Representation of the whole frequency range (up to 152 MHz according to DO-160) on the same figure can introduce some inconvenience to the readers. However, the proposed model can be easily applied to the RF range. All results are also obtained only for the CM mode current because it has the most significant impact on the noise level measured according to DO-160 (see Section 1.3).

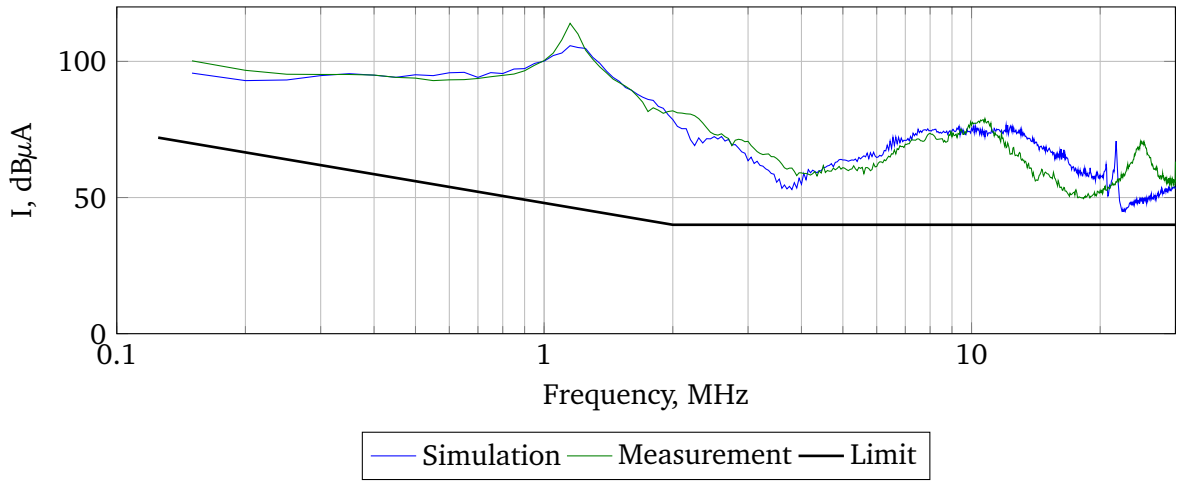
4.1 Application of EMI Filters

After the setup with the AC drive was prepared for the experiments, the first results of conducted emission were obtained for the converter operation without any EMI filter. Such an experiment was conducted mostly for the model validation. At the same time, the measured noise level can be used for the EMI filter selection, if the classical "cut and try" method is applied. The respective terminals of the VSC were connected directly to the input and output cables. The current probe was attached on the whole cable bundle both at input and output. It means that only the CM current was measured in both cases. The same currents were obtained during the simulation. For this, the respective ABCD-parameters of the input/output EMI filters were replaced by thy unity matrices in the model in Figure 2.21. The simulation and experimental results can be observed in Figure 4.1. The output CM current $I_{\mathrm{cm.o}}$ is shown in Figure 4.1a whereas the input CM current can be observed in Figure 4.1b.

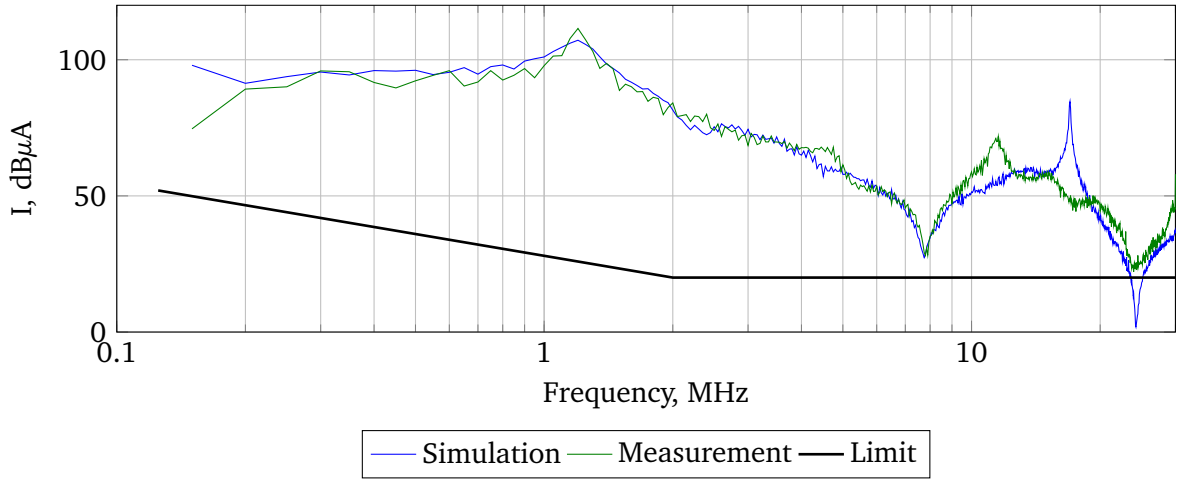
It can be concluded that the proposed simulation approach has very high accuracy in the frequency range below 10 MHz. The accuracy of the model decreases with the frequency increase. The peaks in the measurement results are slightly shifted in comparison to the peak levels in the simulation results. The measured output current shows the peak level at 22 MHz whereas a similar peak is observed at 21 MHz in the simulated CM current in Figure 4.1a. All these can lead to the frequency shift of the resonance points in the simulation. The 10 dB difference is also observed in the RF peaks of input CM current in Figure 4.1b. These peaks are allocated at 11 and 18 MHz for the measured and simulated input CM current respectively. The difference in RF behaviour occurs due to several reasons. Despite, that the model of VSC is improved in Section 2.3, it considers only the most relevant stray parameters which can be easily obtained for the time-efficient simulation. Moreover, some parasitics are also obtained using the simplified equations (2.28)..(2.30). The difference between levels of RF peaks in the measured and simulated CM current is caused by the accuracy of S-parameters which were applied to characterize all components in the model beside the VSC. Due to the noise floor and signal delay in VNA, the real components can be introduced in the measured S-parameter [132]. Despite the slight inaccuracy at RF, it can be clearly observed that the behaviour of CM noise is repeated on the whole frequency range in Figure 4.1, both for the output and input CM currents.

The predicted and measured CM noise levels in Figure 4.1 are also compared with the respective limits according to DO-160. It can be concluded that the conducted noise should be reduced in the whole frequency range in order to fulfil the requirements. In this case, an EMI filter cannot be avoided because noise reduction techniques, which are related to the VSC design, are efficient only in a particular frequency range (see Section 1.4). Therefore, the EMI filters were designed and tested in order to provide the EMC of the considered AC drive system. As it is explained in Section 3.1, the EMI filters have a cell structure. It gives the possibility to obtain different structures of the EMI filters. The applied EMI filters are built with the CM chokes and Y-capacitors. They are aimed to reduce the CM current because it is the most significant contributor to the noise level measured according to DO-160 in the AC drives (see Section 1.3)

The measured and simulated conducted noise levels for the reference parameters from Table 3.3 are shown in Figure 4.2. The reference parameters assume the implementation of the EMI filters both at the input and output of the VSC. As it can be observed, the resulting CM noise in Figure 4.2 was reduced



(a) Output CM current

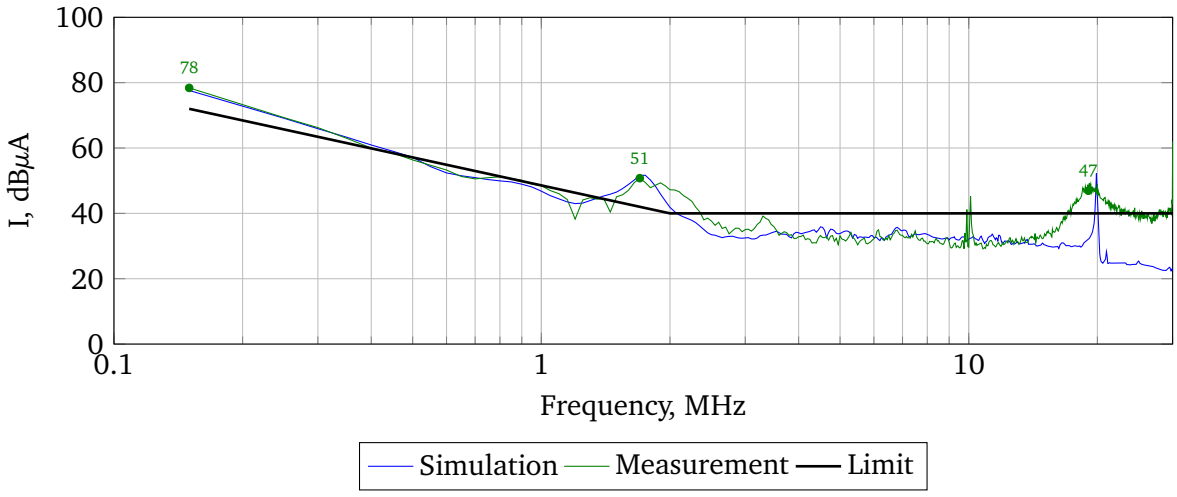


(b) Input CM current

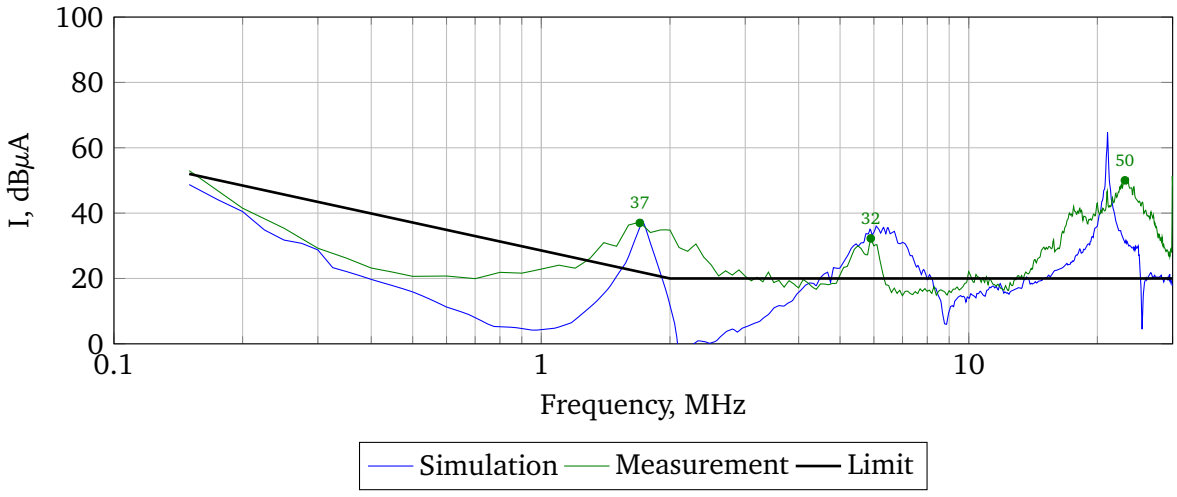
Figure 4.1.: Simulation and measurements results for CM current (without EMI filters).

almost to the limit according to DO-160. The improvement can be seen in both cases of output (Figure 4.2a) and input (Figure 4.2b) CM currents. In the case of the output CM current in Figure 4.2a, the noise level is predicted very carefully on the whole frequency range with a slight 5 dB deviation above the frequency of 15 MHz. The respective peak levels at 1.8 MHz are observed in the simulation and measurements results. This peak level is caused by the crosstalk between DM and CM (MM noise), as it is discussed in Section 4.3. Some narrowband peaks at 10 MHz, which are not presented in the simulation results, are caused by the low voltage components of the VSC as it is explained in Section 3.3.

An additional explanation should be given to the results obtained for the input CM current shown in Figure 4.2b. As it was discussed in Section 3.3, the noise floor of the applied spectrum analyser with the corresponding settings lies exactly below the limit for the input CM current according to DO-160. Comparing the measured CM current in Figure 4.2b with the respective noise floor (see Figure 3.13), it can be observed that the measured level of the CM noise repeats the shape of the noise floor on the whole range besides some peak levels. The actual level of the CM current is lower than the noise floor and cannot be obtained with the applied measurement devices. This complicates the model validation for the input current. As it can be seen in Figure 4.2b, the simulated CM current at the input is much



(a) Output CM current



(b) Input CM current

Figure 4.2.: Simulation and measurements results for CM current with reference parameters.

lower than the measured values and the noise floor for the frequencies below 1 MHz. However, for the higher frequencies, some peak levels can be observed both in the simulation and measurements results. The measured noise levels at 1.8, 6, and 22 MHz are also reflected by the simulation with the required accuracy. Taking into account the simulation results of input CM current for the VSC without EMI filter (see Figure 4.1b), it can be concluded that the proposed model predicts carefully the conducted noise level at the input cable bundle on the whole frequency range. However, due to the inconvenience, which can be caused by the noise floor, further investigation is provided only for the output CM current.

Using the cells of the EMI filters, it is possible to apply different structures for the filter at the input of VSC. Another possible EMI filter structure is the LCLC according to Table 3.3. For the next experiment, the LCLC input filter was constructed with the same CM chokes and Y-capacitors in each cell (reference values). The conducted CM noise at the AC side of VSC was measured and simulated. The results are presented in Figure 4.3. As can be seen, the noise levels below 10 MHz remain almost the same level as the measurements with reference input filter (see Figure 4.2a). However, the peak level, which exceeds the limit, has appeared both in the simulation and measurements results at the frequency of

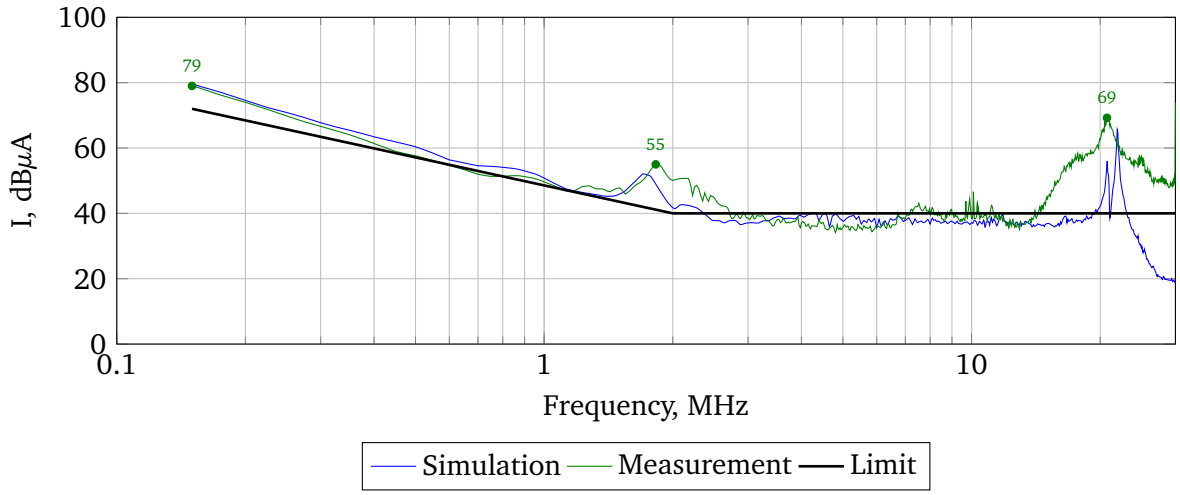


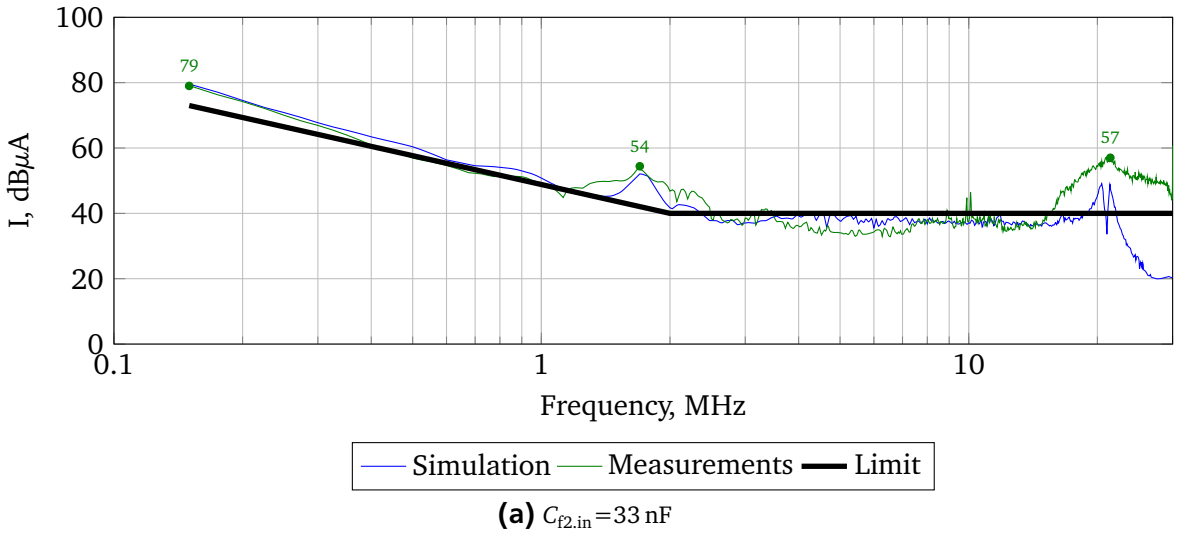
Figure 4.3.: Simulation and measurements results for the output CM current with LCLC input filter.

21 MHz. Moreover, comparing the reference LCL filter with LCLC structure (Figure 4.2a and Figure 4.3 respectively), it can be seen that the noise level was increased on 3 dB in the 2nd case for the frequencies above 2 MHz.

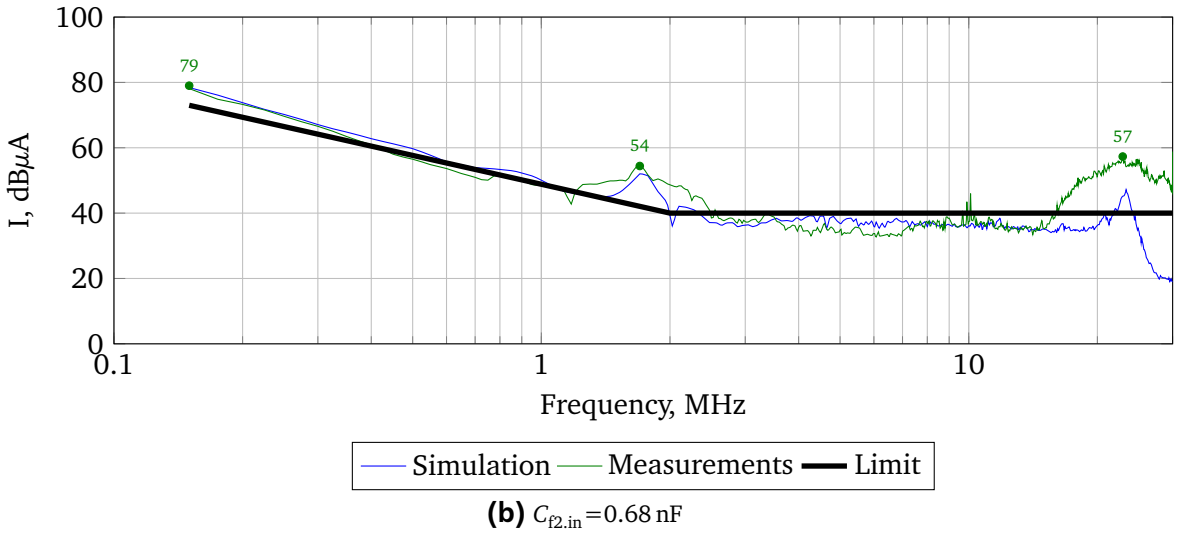
The simulated values of the output CM noise in Figure 4.3 are also repeating the measurement results. However, the shape of the additional peak at the frequency of 21 MHz is quite different. This difference is due to the main drawback of the frequency domain models - lack of ability to calculate the transients. Due to the switching nature of the VSC output voltage, the transients of output current occur at each switching instant. The transients are localized in time in comparison to the sinusoids which are infinite in time. The spectrum of transients has a wideband nature. As it is discussed in [38], the oscillations in drain-source voltage are recognised as a wideband noise after the application of the spectral analysis. From the other side in any frequency domain model, the model is excited by the sinusoids with infinite duration (steady-state). It results in the narrowband noise levels in the simulation results.

Application of the EMI filters reduces the CM noise. The CM current is much higher than the limit according to DO-160 in the system without EMI filters (see Figure 4.1). As it is shown, the structure of an input filter has a huge influence on the output CM current in the current system. Additional Y-capacitors, which was installed just before the VSC in the input filter, lead to the resonance at 21 MHz and additional CM noise level of 69 dBμA in the output current in Figure 4.3. The output CM noise was also evaluated with the LCLC filter. But the value of damping resistance R_{d2} of the 2nd cell of the input EMI filter was increased up to 5 Ω. The output noise was also evaluated with the various values of the Y-capacitance ($C_{f2.in}$) in the same cell. The simulation and measurements results can be observed in Figure 4.4. It can be concluded, that the value of damping resistance R_{d2} and Y-capacitance $C_{f2.in}$ in the 2nd section of input EMI filter has an influence only on the RF peak of the output CM noise because the noise level below 10 MHz is the same as in Figure 4.3.

In Figure 4.4a, the output CM noise was measured and evaluated with the reference value of Y-capacitance. It can be clearly seen that the simple increase of the damping resistance R_{d2} leads to the decrease of the peak level at 21 MHz from 69 to 57 dBμA. The same amount of attenuation is observed in the simulation and experimental results. However, as it was already explained, the shape of the



(a) $C_{f2.in}$=33 nF



(b) $C_{f2.in}$=0.68 nF

Figure 4.4.: Simulation and measurements results for the output CM current with LCLC filter, with R_{d2}=5 Ω and various values of $C_{f2.in}$.

RF peak is not the same as in the simulation results. The output CM current under decreased valued of Y-capacitance in the 2nd cell of LCLC input filter is shown in Figure 4.4b. As it was expected the reduction of $C_{f2.in}$ leads to the shift of RF peak to 23 MHz. The same behaviour was simulated as well. It can be clearly concluded that the additional RF peak level in case of LCLC structure of the input EMI filter is caused by the resonance due to the additional Y-capacitance in the 2nd cell.

Even though the LCLC filter should provide the better attenuation of the conducted noise, it can also cause an increase of the RF noise at the output due to the resonance. The proposed model was able to predict such behaviour. The simulation results were repeating the measurements under different parameters of EMI filters as well as operation without any filter. However, due to the accuracy of the measured S-parameters, the RF peaks in simulation results can be slightly shifted in the frequency. Moreover, the shape of the high-frequency peaks cannot be repeated within the frequency domain model because the RF noise is mostly defined by the transients due to the switching nature of inverter.

4.2 Impact of Modulation Index and Saturation of CM Chokes

The results presented in the previous section are obtained for the reference operation point of the AC drive: modulation index m=0.9 and active load $P = 1.5\,\text{kW}$. However, these values can be changed in a wide range during the operation of the AC drive. For all operation points, the measured noise level should be lower than the limit according to DO-160 [24]. All cells of the EMI filters include the CM chokes which are based on the nanocrystalline cores. The parameters of the input and output CM chokes are given in Appendix C. The design of the CM chokes is a complicated task because lots of the parameters should be taken into account: the final value of inductance, losses, stray capacitance and self-resonance. It is also required to pay attention to the saturation of the magnetic material. This section considers the impact of the modulation index on the saturation of CM chokes which was observed under the decreased value of the modulation index.

As it is explained in Subsection 1.4.3, the shape of VSC output voltage in the time domain and the corresponding spectrum in the frequency domain are defined by the PWM technique and its parameters. It is also discussed that decrease of the modulation index leads to an increase of the zero vectors duration (time t_0 according to (1.13)) in the SVPWM. The highest value of the CM voltage is applied during zero vectors according to Table 1.3. Therefore, it can be concluded that the decrease of the modulation index leads to an increase of the VSC output CM voltage. Otherwise, the CM current increases with the decrease of the modulation index. Such a condition can occur in the AC drive if the speed of the motor reduces according to u/f-control [27]. This effect can be easily studied in the simulation and measurements. The value of the modulation index m was reduced to 0.45 (speed of the motor was reduced twice as well) in the control system of the VSC converter. In the simulation, the reduction of m was taken into account by the value of U_{ref} during the generation of PWM voltages (see Figure 2.14). The CM currents under the reduced value of the modulation index were evaluated.

The output CM current under the reduced modulation index with the reference LCL filter is shown in Figure 4.5. It can be observed that there is a huge deviation between the measured and simulated results up to the frequency of 4 MHz. Below this frequency, there is 15 dBμA difference between the measured and simulated output CM current. The measured noise is much higher than limit leading to the absolute limit violation according to DO-160. For the higher frequencies, the accuracy of the model increases. Moreover, the results are similar to the CM current under the reference value of the modulation index for the RF range (see Figure 4.2a).

The measured results do not correspond to the expected behaviour. The twice smaller value of the modulation index should provide only several dB increase of VSC output CM voltage. The corresponding CM currents should be then increased in the same range as well. However, an increase of m has lead to much higher values of the output CM current (see Figure 4.5).

After the analysis, it was concluded that the CM choke was saturated due to the reduction of the modulation index. It explains the huge difference between the measured and simulated values of CM current in Figure 4.5. The frequency domain models are not able to predict the conducted noise with non-linear behaviour under the saturation of the choke. At the frequency of 4 MHz, the output CM choke observes the self-resonance (see Appendix C). Therefore, the impact of core material reduces explaining the accordance between simulation and measurements results at the higher frequencies in Figure 4.5.

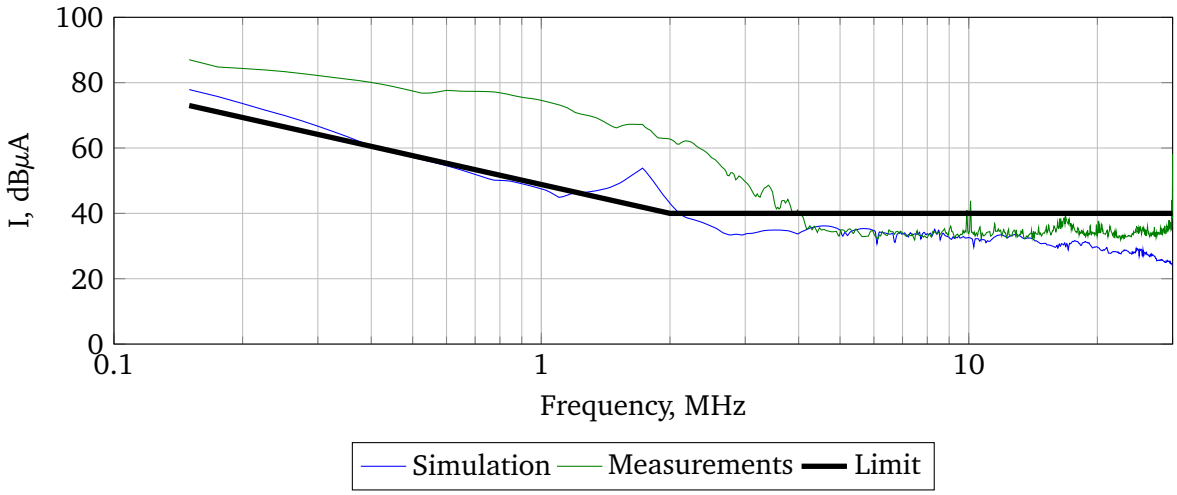


Figure 4.5.: Simulation and measurements results for the output CM current under m=0.45.

The saturation of CM chokes was analysed and explained in [16]. It was shown that the impedance of the CM path and the modulation index influence the value of the volt-second across the CM inductor which in turns defines the saturation of the CM choke. It can be then concluded that in the case of VSC operation with reduced m, the volt-second across the output CM choke is also too high.

The calculation of the volt-second across an inductor requires the knowledge about voltage source and the components which are applied in the circuit with an inductor. The voltage sources were already obtained both in the time and frequency domains (see Section 2.3). However, the estimation of the system parameters requires the fitting procedure because most of the components in the proposed model are described by the n-port networks of MM parameters. These parameters are the "black boxes" and do not provide any information about the internal structure. However, the proposed model can be used to evaluate the saturation of the CM choke in the EMI filters. Under several assumptions, it is possible to use only the fundamental part of the CM current in order to indicate, if the choke is saturated or not. For the considered topology of the inverter and the applied PWM technique, the fundamental frequency is equal to the sampling frequency (see Figure 1.21). As it was mentioned already several assumptions should be taken into account:

- Firstly, it is assumed that the magnetic flux density decreases with a frequency increase. This is due to the fact that the value of relative permeability of core material reduces with a frequency increase (see Appendix C). Taking into account that the amplitudes of higher-order harmonics of the output CM voltage decrease with a frequency, the amplitude of the magnetic flux in the core is defined mostly by the fundamental part of the CM current.

- Further, it can be assumed that the RF currents with huge peaks, which occur due to the transients [38], do not contribute to the amplitude of the magnetic flux. The frequency of such transients is higher than the self-resonance frequency of the choke.

The value of the saturation current I_{sat} for the output CM choke was estimated using the parameters which are given in the Appendix C. It was assumed that the maximum flux density and relative permeability at 24 kHz (PWM frequency according to Table 3.3) are equal to $B_{\text{max}} = 1.2\,\text{T}$ and $\mu = 50000$

Table 4.1.: Fundamental amplitude of the output CM current under different modulation indexes and PWM techniques.

VSC parameters	Simulated value, mA	Measured value mA,	Choke saturation
SVPWM, m=0.9	115	124	no
SVPWM, m=0.45	266	237	yes
DPWM, m=0.9	127	129	no
DPWM, m=0.45	269	240	yes
AZPWM, m=0.9	122	128	no
AZPWM, m=0.45	88	92	no

respectively. For the applied amount of windings ($n = 12$ for each phase) $I_{\text{cm.sat}}$ is equal to 162 mA. The amplitude of the output CM current for the fundamental harmonic (sampling frequency of PWM) was evaluated using frequency domain simulation. For such a calculation, the spectrum of CM voltage was estimated with the lowest possible value of RBW (fundamental frequency of reference voltage - 50 Hz). In this case, the average value of the CM current on one fundamental period is obtained during the simulation (see Section 2.4). The same amplitude was also obtained using measured time domain data of the output CM current. The length of the measured time domain data corresponds to the period of the fundamental output voltage (20 ms). These values were also evaluated under the reference parameters and with different modulation indexes as well as with different PWM techniques. The other system parameters were fixed to be equal to the reference values according to Table 3.3. The resulting amplitudes of CM current on the fundamental frequency can be compared in Table 4.1.

As can be seen in Table 4.1, the output CM current is lower than the saturation current under the reference parameters of the VSC. The simulated and measured values of the fundamental amplitude are also in accordance with each other. As it was predicted by the proposed model, that a decrease of m leads to an increase of the fundamental amplitude of the CM current. The simulated value under $m = 0.45$ is much higher than the value of the saturation current of the applied CM choke. Therefore, it can be concluded that the output CM choke is saturated. This is also observed in Figure 4.5.

In [90], the impact of PWM techniques on choke saturation was studied using the volt-second characteristic. It was shown, that the PWM techniques with the reduced CM voltage (see Section 1.4) can be used to reduce the volt-second of the applied CM chokes (in the case then resonance is not presented in the system at higher frequencies). Therefore, the amplitudes of the fundamental harmonic of the output CM current were also evaluated for the VSC operated under DPWM and AZPWM (see Table 4.1). The fundamental amplitude of CM current under DPWM is slightly higher than under SVPWM. Decrease of the modulation index leads to the saturation of the output CM choke in case of the DPWM as well. The amplitude of CM current at switching frequency for AZPWM is much lower than the saturation current for all values of m. The saturation was not observed during the measurements with AZPWM (see Figure 4.11). It means, that AZPWM can be used to avoid the saturation of the output CM chokes for the operation points with the reduced modulation index. The final impact of AZPWM on the resulting CM noise is studied in Section 4.4. It can be seen in Table 4.1 that with high values of m there is almost no difference

between the conventional SVPWM and AZPWM. This is due to the fact that the duration of zero vectors, which are avoided in AZPWM, is very low and does not influence the amplitude of CM current with m almost equal to one (see Section 1.4).

Special care should be provided during the selection of the CM chokes for the EMI filters. As it is shown, the chokes can be saturated leading to the increased noise levels under different operation conditions (lower speed of the motor) of a variable speed drive. The saturation of the CM choke at the output is observed during the measurements with reduced modulation index. The saturation is a non-linear effect of the magnetic materials which cannot be predicted by the small-signal frequency domain models. But it is shown that such models can be used to indicate the saturation of CM chokes. Using the proposed model, the saturation of CM choke is indicted using an estimated value of the output CM current on the fundamental frequency. However, such an approach should be applied carefully. The property of the applied magnetic material is used assuming that only the fundamental harmonic of CM current contribute to the value of the flux density in the core of the output CM choke. If relative permeability of the core material does not reduce with a frequency increase, the harmonics can also contribute to the magnetic flux density. The efficiency of the frequency domain models for the evaluation of saturation for such cases is offered for further research.

4.3 Investigation on MM Noise

Due to the small asymmetries between phase impedances, some amount of energy can be transferred from CM to DM and vice versa (see Section 1.3). This type of conducted EMI is called the MM noise. During the experiments, it was figured out that peak levels of CM noise cannot be predicted by the simple frequency domain models with the separated circuits for CM and DM. This noise was observed with all possible structures of EMI filters (noise level at 1.8 MHz in Figure 4.2-4.4). Several facts shows that the additional noise level at CM is a MM noise:

- The resonance was observed in the DM at the frequency of 1.8 MHz. This resonance was defined by the stray DM parameters of the motor and cable and by the stray DM inductance of the output CM choke. The ripples with a frequency of interest were also observed during the measurements (see Figure 2.16). The same resonance was also predicted by the DM model.

- Additional X-capacitors at the output lead to a decrease of the resonance frequency at DM. The similar shift of the corresponding peak was also observed during the measurements of output CM current.

The proposed model can be used to estimate which peak levels are caused by the crosstalk between CM and DM. In order to do this, it is necessary to calculate the required currents without the respective voltage sources. The model in Figure 2.21 was calculated with reference parameters with various configurations: without DM voltage source $U_{\mathrm{dm1}} = U_{\mathrm{dm2}} = 0$ and without CM source $U_{\mathrm{cm}} = 0$. The simulation results can be compared with the measured noise under the reference parameters in Figure 4.6. As can be seen, the simulation without CM voltage source (blue line) is repeating the measurements results up to 500 kHz. Then the simulated noise without DM voltage sources is much lower than the measured CM

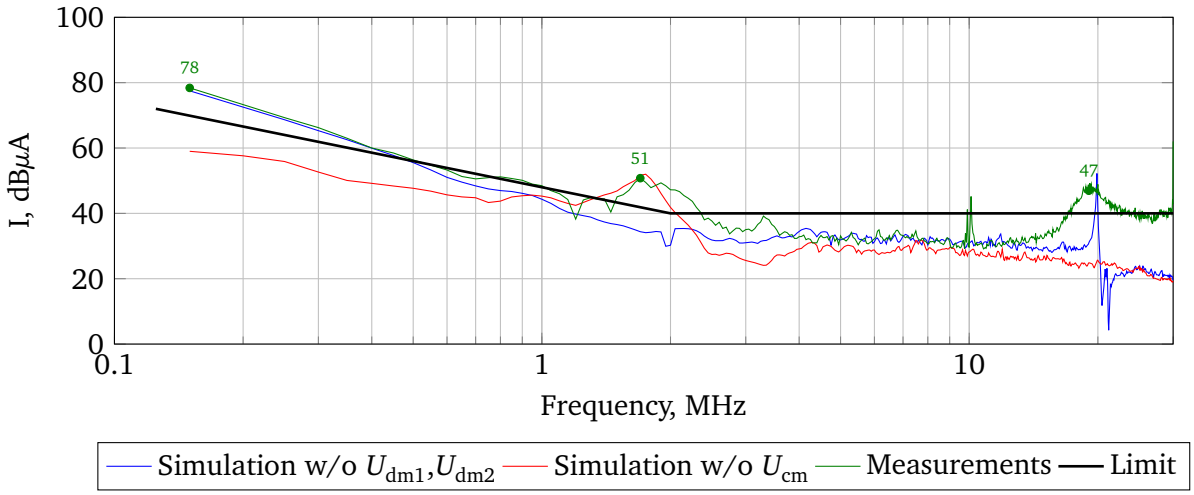


Figure 4.6.: Simulation and measurements results for the output CM current with reference parameters (simulations without DM and CM voltage sources).

noise during the frequency range of interest. The accuracy of the results with pure CM current increases repeating the measured CM noise with a further frequency increase.

The output CM current was also evaluated using the developed model with DM voltage sources U_{dm1} and U_{dm2} and without CM voltage source (red line in Figure 4.6). The resulting current is a pure MM noise. As can be seen, this noise is much lower than the measured and simulated CM noise except the considered peak level (1.8 MHz). Using the superposition principle, MM and CM can be summed showing the same results as in Figure 4.2a. Assuming the analysis mentioned above, it can be concluded that the MM noise is presented in the system under study. Moreover, the proposed model can be used to evaluate the amount of MM noise.

The additional peak of the output CM current at the frequency of 1.8 MHz is higher than the respective limit. Increase of the CM inductance (by means of the additional CM choke at the output) would not decrease significantly the considered MM noise. The peak would be slightly shifted towards lower frequency due to the DM stray inductance of the additional CM choke. An attempt to reduce the considered noise with CM choke would lead to an oversize of the CM choke. Therefore, it is necessary to apply the DM filters at the output as well. The simplest DM filter, which was also implemented on the setup, is a three equal ($L_{\mathrm{a}}=L_{\mathrm{b}}=L_{\mathrm{c}}$) single-phase inductors connected in series with the output CM choke. The inductors of 10 μH were applied for the experimental evaluation. The applied DM inductors have a nominal current of 15 A and the self-resonance frequency of 43 MHz [157]. The DM filter based on these single-phase inductors contributes to the CM behaviour as well. However, the influence of such a filter on the CM is very low because its resulting CM inductance (3.3 μH) is much lower than the inductance of the reference output CM choke (see Appendix C).

Besides additional DM filters, the other parameters were left to be similar to the reference parameters from Table 3.3. The measurement results together with the simulated output CM current can be observed in Figure 4.7. As can be seen, the additional inductors at the output do not affect the low-frequency CM noise. Nevertheless, as it was also predicted by the proposed model, the additional peak was shifted

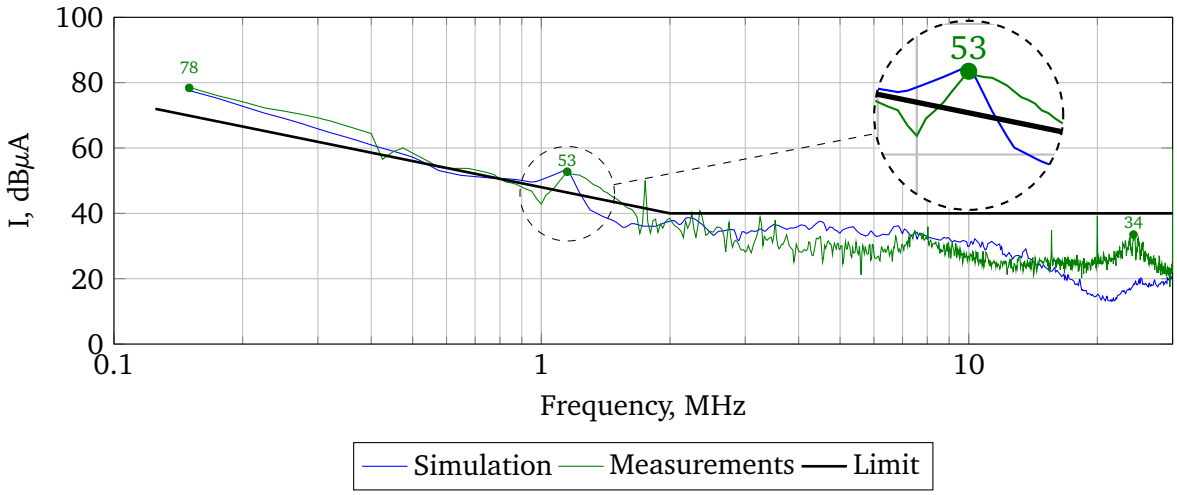


Figure 4.7.: Simulation and measurements results for the output CM current with additional DM filter at the output of VSC (L_a=L_b=L_c=10 μH).

towards the lower frequency (from 1.8 MHz to 1.2 MHz). Some changes can be also observed in the RF range. The results show also that the considered noise is caused by the coupling between DM and CM.

It can be also observed in Figure 4.7 that the amplitude value of the MM noise peak was increased on 2 dB. However, due to the increase of the respective limit with a frequency decrease, the difference between noise level and the limit was reduced. In order to comply with DO-160, it would be necessary to increase the value of the applied inductors to shift the MM noise to the lower frequency. Under the particular value of DM inductance, the noise level will be lower than the limit. However, the single-phase inductors have to handle the whole phase current including fundamental frequency. The peak value of DM current is very high that can lead to the saturation of the applied choke. The required DM choke could greatly reduce the power density of the VSC.

Another benefit of the simulations based on the MM parameters is the ability to simulate the asymmetric structures of the EMI filters. Because the additional MM noise is caused by small asymmetries in the system, it should be possible to compensate them. Using the proposed model, the output current was evaluated under different values of phase inductances: 0, 2, 6 and 10 μH. These inductors were changed during the simulation separately for each phase considering all possible combinations including asymmetric. Using such a model-based filter design, it was estimated that the asymmetric DM filter with phase inductances L_a=L_b=6 μH and L_c=10 μH should lead to the lowest level of CM current between 1 and 2 MHz. Similar asymmetric DM filter was built using the available DM chokes. The chokes of asymmetric filter have the same parameters of nominal current and resonance frequency as the chokes applied in the symmetric DM filter [157, 158]. The simulation and measurements results can be compared in Figure 4.8.

The simulation and measurements results show that the output CM current is not influenced by the presence of the asymmetric DM filter except the additional peak of MM noise. The peak level of MM noise was reduced from 53 to 49 dBμA in comparison to the symmetric DM filter in Figure 4.7. This is very close to the required limit. The final impact of the asymmetric filter structure should be studied further in details. Nevertheless, it can be concluded that the asymmetric DM filter is more effective

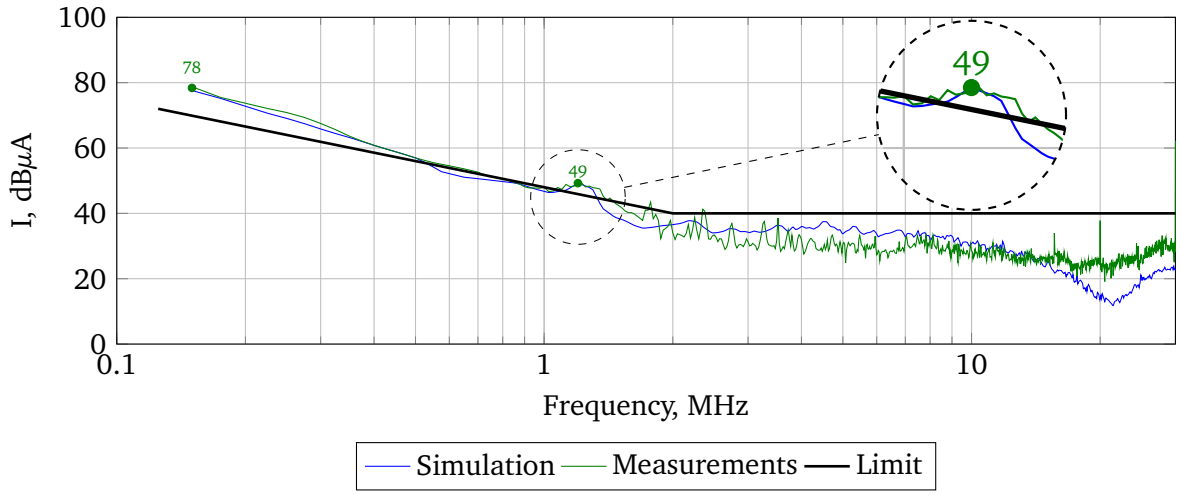


Figure 4.8.: Simulation and measurements results for the output CM current under reference parameters with additional asymmetric DM filter at the output of VSC (L_a=L_b=6 μH,L_c=10 μH).

than the symmetric one for the attenuation of the MM noise (see Figure 4.7). Moreover, the proposed frequency domain model estimates the level of MM noise with the required accuracy.

The effect of MM noise is investigated in this section. It is shown that additional noise levels can be observed in the CM current due to the crosstalk to DM. It is also discussed that the wrong understanding of MM noise origins can lead to the oversize of an EMI filter. The asymmetric EMI filter structure is also investigated in this section. The asymmetric filter was designed using the proposed model based on the MM parameters. The experimental results show that it is possible to reduce the MM noise level more effectively with an asymmetric filter in comparison to the symmetric one. However, the impact of asymmetric EMI filters should be investigated further. The asymmetries in the system, which lead to the MM noise, can have a probabilistic character. Under some deviations, the asymmetric filter can lead to an increased level of MM noise. Such an investigation is proposed for further research.

4.4 Tuning Converter Parameters

The previous sections investigate the reduction of CM noise level by means of the EMI filters. Different effects of EMI filters were considered: the impact of filter structure and saturation of CM chokes. All investigations are provided using experimental and simulation results showing good accordance of the proposed model. Therefore, the proposed model can be applied to design the EMI filters. Moreover, it can be also utilized for the design of asymmetrical structures. Consideration of asymmetric structures requires additional effort in the simplified frequency domain models with decoupled DM and CM.

However, the CM noise level at the output was not reduced to the appropriate level according to DO-160 with the applied EMI filters. The measured and predicted CM noise levels violate the limit at some places in low and high-frequency ranges. Additionally, the output CM choke can be saturated under different operation points of the AC drive. To overcome these problems, the core of output CM choke can be increased. But it will lead to an increase of the weight and size of the EMI filters. However, Section 1.4 explains that besides the EMI filters, conducted noise can be reduced by means of the VSC

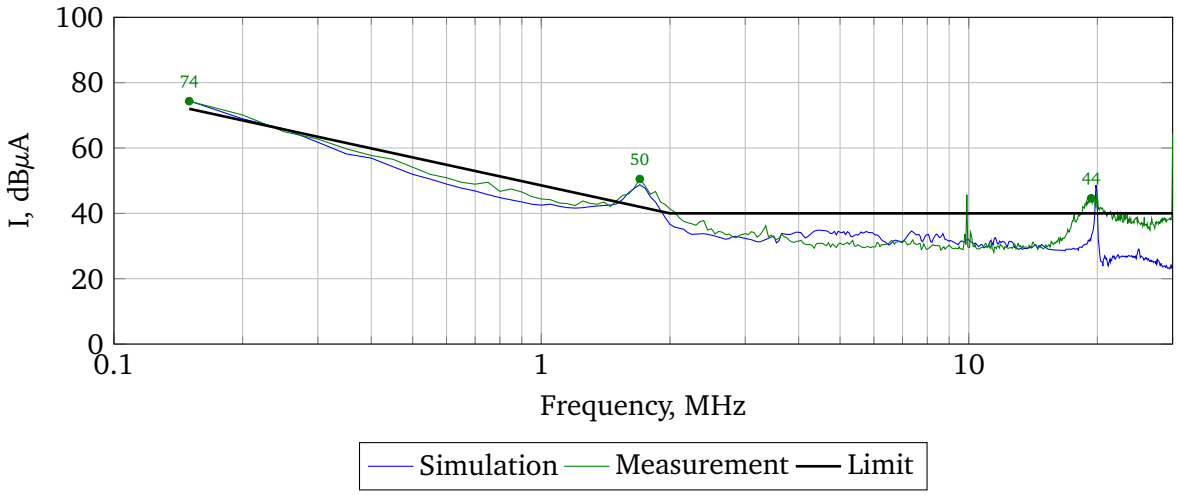


Figure 4.9.: Simulation and measurements results for the output CM current under DPWM.

design. All these conducted noise reduction techniques related to the VSC design show a lower level of attenuation in comparison to the EMI filters. They influence also only a particular frequency range. In this section, an attempt is made to tune the parameters of VSC in order to comply with DO-160 for the output CM noise with the applied reference EMI filters. Moreover, the impact of the AC drive load conditions is also studied in this section. All results are obtained using the measurements and simulation in order to validate the developed frequency domain model.

4.4.1 Usage of Different PWM Techniques

Different PWM techniques are described in Subsection 1.4.3. These techniques can be used to reduce the output CM voltage of the VSC. The first type of PWM with reduced CM voltage, which is considered for the investigation, is a DPWM. This type of modulation is based on the reference SVPWM. But only one zero vector is applied during the single switching cycle. In this case, the DC bias is introduced in the output CM voltage. But the AC amplitude of CM voltage is reduced (see Figure 1.21b). Moreover, the amount of switching events during one sampling period decreases in comparison to SVPWM. This effect of DPWM is also used to reduce the switching losses in inverter [34]. There are also several types of DPWM techniques according to the applied zero vector. The so-called "flat-top" DPWM is used for the investigation. This modulation ensures that one phase-leg of the FB inverter is not switched for a certain period of time during the amplitude of the fundamental output DM voltage [34].

The measurements and simulation results can be observed in Figure 4.9 for the output CM current for the VSC operated with DPWM. The results show good accordance of the model. It means that the spectrum of the output voltage is generated appropriately (see Section 2.3). As can be also seen in Figure 4.9, the output CM current was reduced on the whole frequency range in comparison to the reference SVPWM modulation (see Figure 4.2a). The low-frequency CM current was reduced on 5 dBμA from 79 to 74 dBμA at the frequency of 150 kHz. The RF peak level at 19 MHz was slightly reduced from 48 to 45 dBμA in case of DPWM. This reduction occurs due to the decrease of the switching events on one sampling period. Moreover, the application of DPWM has an influence on the MM as well (peak level

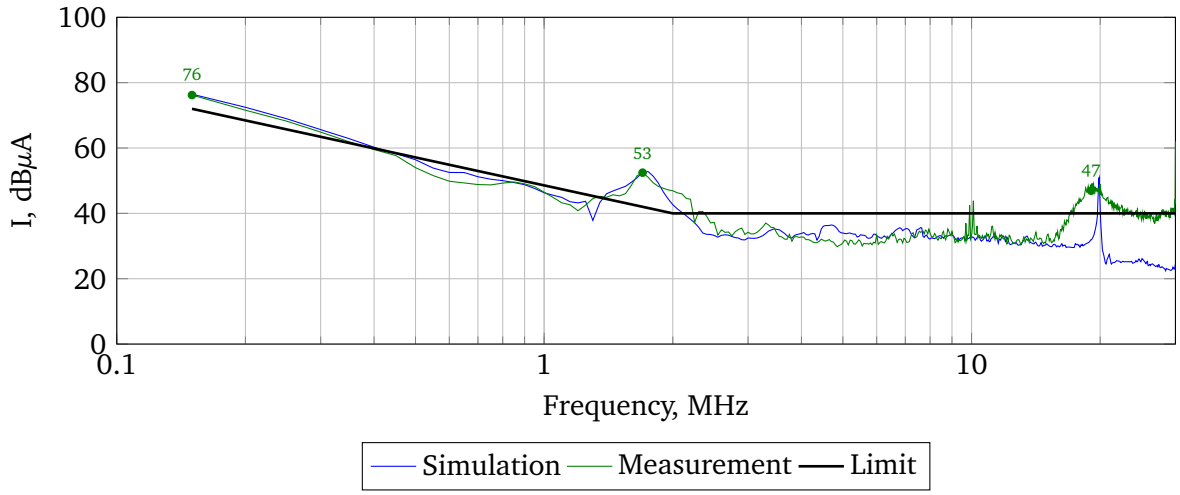


Figure 4.10.: Simulation and measurements results for the output CM current under AZPWM.

at 1.8 MHz, see Section 4.3). Its maximum value was reduced only on 1 dBμA, but the peak itself has a narrower shape in case of DPWM that can be also seen in the simulation results in Figure 4.9. The resulting impact of DPWM on the output CM current was predicted on the whole frequency range by the developed frequency domain model.

As it can be observed in Figure 4.9, the application of DPWM for the VSC operation reduces the output CM noise almost to the required level. As it was already mentioned in Section 4.3, the MM noise can be reduced with an additional asymmetrical DM filter. However, as it is shown in Section 4.2, if the AC drive is operated with variable speed, the output CM choke can be saturated under the operation points with low modulation indexes. For DPWM, the saturation of the CM choke was also observed during the measurements. Similar to the SVPWM, the saturation was also indicated by the fundamental amplitude of the CM current (see Table 4.1). According to Table 4.1, the AZPWM can be used for the operation with a wide range of modulation index variation. This type of PWM avoids the usage of zero vectors completely. Therefore, as it was discussed in Section 1.4, it should reduce the value of the output CM voltage.

The conducted CM noise was measured for the VSC operated with AZPWM. All other parameters of the system were fixed to the reference values according to Table 3.3. The simulation and measurements results can be observed in Figure 4.10. It can be observed in Figure 4.10 that the output CM current at lower frequencies was reduced only on 2 dBμA in comparison to SVPWM in Figure 4.2a. The peak level at 19 MHz keeps the same value under AZPWM and SVPWM. At the same time, the level of MM noise at 1.8 MHz was slightly increased. The increased level of MM noise corresponds to the expected behaviour because the level of DM voltage increases with AZPWM due to the bipolar switching of phase-to-phase voltage (see Figure 1.22b). The behaviour of the output CM current in Figure 4.10 was also predicted by the simulation.

The application AZPWM for the control of inverter does not introduce any changes in the RF noise for the studied system. Comparing Figure 4.9 and Figure 4.10, it can be also concluded that the DPWM technique shows an improved CM noise at lower frequencies in comparison to AZPWM. But as it was discussed above, the application of AZPWM provides the possibility to use the designed output CM

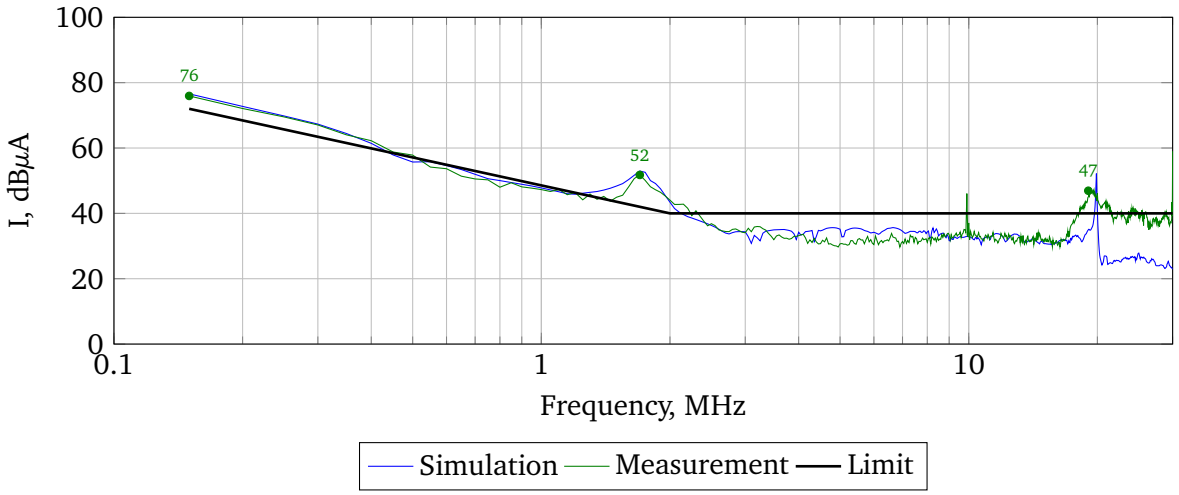


Figure 4.11.: Simulation and measurements results for the output CM current under AZPWM and $m = 0.45$.

choke for the operation mode with a low modulation index (see Table 4.1). The output CM current was simulated and measured for the VSC operated with AZPWM and low modulation index. The results can be observed in Figure 4.11. It can be concluded that the modulation index does not have a noticeable impact on the output CM current in the case of AZPWM. Such behaviour proves also that the output CM choke was saturated under operation with the reference PWM technique and low modulation index in Figure 4.5. The saturation was not indicated for the AZPWM with $m = 0.45$ in Table 4.5. The level of the output DM voltage decreases with the reduction of the modulation index. Therefore, the MM noise level at 1.8 MHz in Figure 4.11 was also slightly reduced in comparison to AZPWM with the reference value of m in Figure 4.10.

Two different PWM techniques are studied in this section: DPWM and AZPWM. Both of them have a certain impact on the resulting level of output CM noise. The DPWM reduces the CM current on the whole frequency range including MM which appears due to the coupling between DM and CM. All peaks except MM noise were reduced almost to the appropriate levels. However, the DPWM technique does not allow to avoid the saturation of the CM choke under operation with low modulation indexes for the reference output EMI filter. In the case of AZPWM, the reduction of CM current was observed as well. But AZPWM is less efficient in comparison to DPWM. Moreover, the MM noise can be even increased, if AZPWM is applied. However, the RCMV-PWM techniques such as AZPWM can be used to avoid the saturation of the reference output CM choke under operation with low modulation indexes.

4.4.2 Improvement of Switching Behaviour

The type of PWM technique influences the low-frequency noise except DPWM which reduces the RF noise due to the decreased amount of the switching events. As it was considered in Section 1.4, the RF noise can be influenced by the hardware design of VSC. The hardware design of a converter influences the spectrum of output voltage from one side and impedance of converter from the other side. The

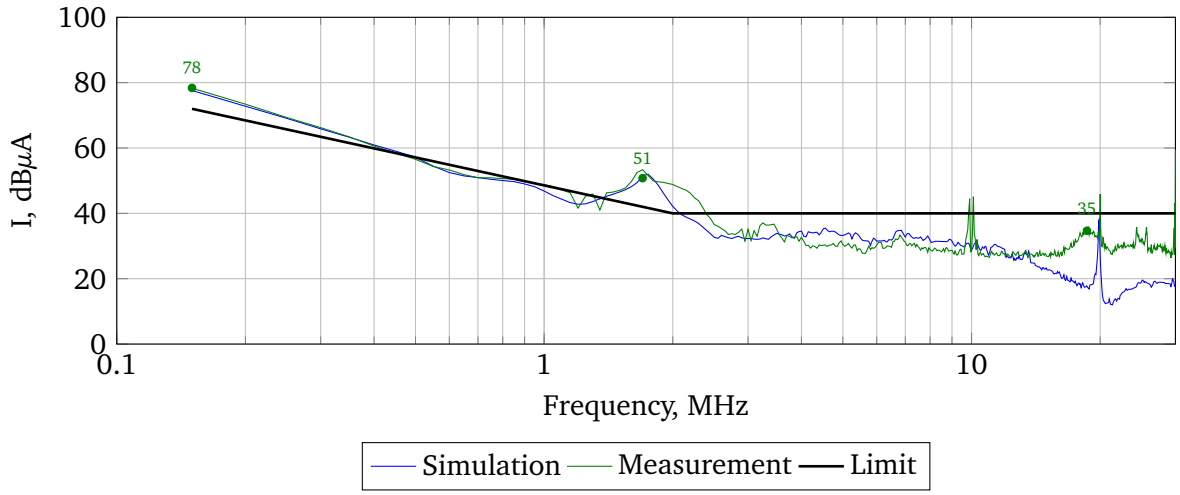


Figure 4.12.: Simulation and measurements results for the output CM with t_f=50 ns (R_g=15 Ω).

spectrum of the output voltage at RF can be influenced by the switching behaviour which is in turns defined by the applied power switches and gate drivers.

In this subsection, an attempt is made to reduce the RF CM noise by means of the gate drivers design. As it was explained in Subsection 1.4.4, the switching behaviour can be easily influenced by the appropriate selection of the gate resistance R_g (see Figure 1.24). Increase of R_g leads to an increase of MOSFET commutation time (see Figure 3.7). The RF noise can be reduced by the appropriate selection of rise/fall time (t_f). The high-frequency peak value of 47 dBμA was observed in simulation and measurement results in Figure 4.2a for the VSC operated with the reference parameters. According to Table 3.3, the VSC with reference parameters is switched with the minimum possible value of t_f equal to 20 ns. This value is observed during the switching of the applied SiC MOSFETs with zero value of R_g (see Figure 3.7). In order to reduce the level of CM current at 19 MHz, it is required to increase the commutation time of MOSFET t_f up to 50 ns. For the applied switches, it means that the value of R_g should be increased up to 15 Ω according to Figure 1.25. The corresponding resistors were applied to the gate drivers. The respective value of MOSFET voltage fall time was also considered during the generation of the time domain data for VSC output voltage (see Figure 2.14). The corresponding simulation and measurements results can be seen in Figure 4.12.

Comparing the results in Figure 4.12 with the measurements and simulation under reference parameters in Figure 4.2, it can be concluded that the peak level of CM current at 19 MHz was significantly reduced to the appropriate level according to DO-160 (from 47 down to 34 dBμA). As it is also expected the increase of t_f by means of gate driver design does not have any impact on the lower frequency range.

A further increase of MOSFET commutation time can be used to improve the noise level for the lower frequencies. For example, it is possible to reduce the peak value of MM noise at 1.8 MHz. But according to Figure 3.7, the further increase of R_g will increase the value of switching losses in the VSC. For the provided in Figure 4.12 results, the value of total energy loss per one commutation was increased from 200 up to 400 μJ. Moreover, as it is shown in the next subsection, with the decrease of MOSFET commutation time increases the impact of the output current on the RF noise.

4.4.3 Impact of Load

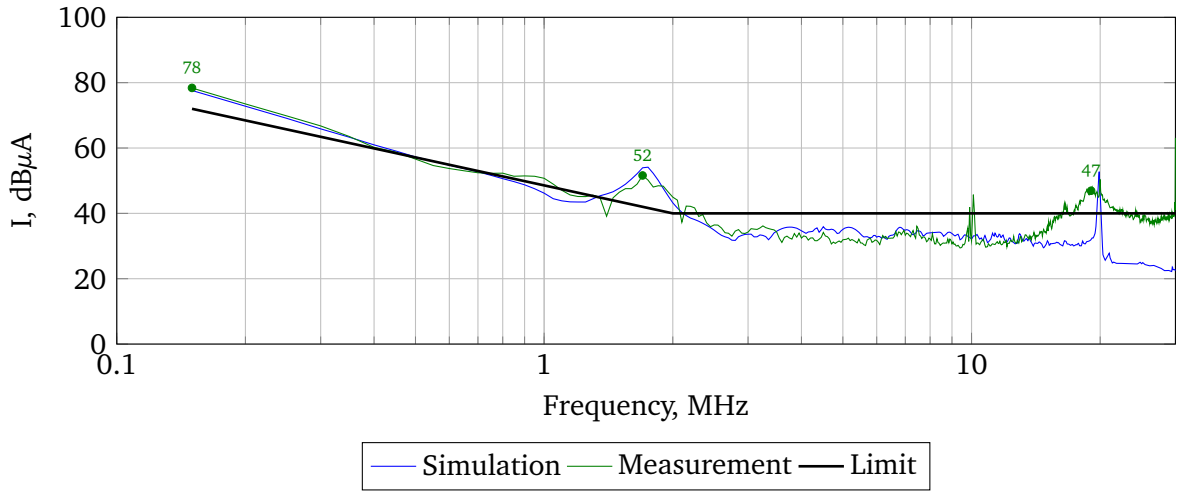
The impact of the MOSFET commutation time on the generated CM noise is considered in the previous subsection. It is shown that it is possible to reduce the RF peaks by means of the gate driver design. However, some edges of the PWM voltage depend on the vale of the output phase current of an inverter (see Section 1.4). Depending on the direction of the output current at the beginning of the switching process, the commutation can be provided either through the power MOSFET or through the free-wheeling diode (in-built diode). In the case of diode commutation, the rise or fall time of the VSC output voltage depends on the value of drain-source capacitance (charge) and on the value of the output current at the beginning of the switching process.

The analysis of the PWM output voltage provided in Section 2.3 shows that some falling and rising edges of pulses vary during the fundamental period indicating diode commutations. Whereas edges, which are constant during the fundamental period, are caused by the MOSFET commutations. A simplified algorithm is also proposed for the generation of time domain PWM signal including variable rise/fall times. In Section 2.4, it is explained how to consider these effects during the calculation of the frequency domain model by means of SWDFT. The final measured noise level, which is observed on the EMI receiver, is also defined by such parameters as RBW and type of detector. The proposed approach of spectral analysis considers the effect of an EMI receiver as well.

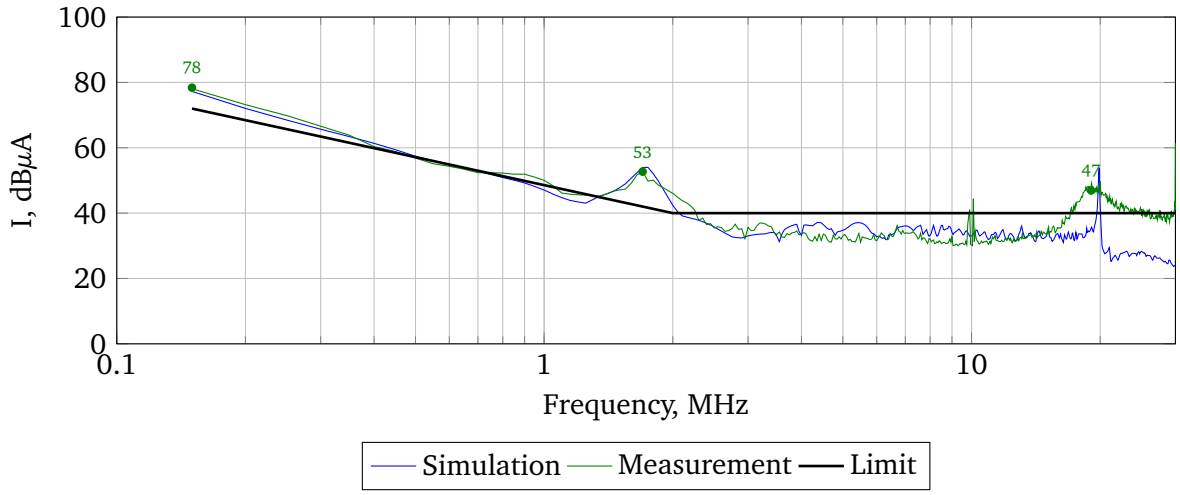
In order to investigate the influence of MOSFET and diode commutations on EMI behaviour, the studied AC drive was operated with different load conditions. All other parameters of the system were assumed with the reference values (see Table 3.3). The load is varied by means of the DC machine which is connected mechanically with the AC motor (see Section 3.2). It should be mentioned that the phase shift between the output voltage and current changes with the load increase leading to a slightly different spectrum of PWM voltage as well. The value of the output CM noise was obtained using measurements and simulation. The results can be observed in Figure 4.13.

The load of the motor was increased up to 3 kW. The corresponding simulation and measurements results can be observed in Figure 4.13a. Comparing the observed CM current with the results under reference parameter of load (idle mode of the motor in Figure 4.2a), it can be concluded that the slightly increased load does not introduce an additional level of EMI. The low- and high-frequency peaks have the same values. Some minor impact can be observed on the MM noise at 1.8 MHz which was increased on 1 dBμA. The same results can be observed in Figure 4.13b with the further increase of the load applied to the induction machine (7.5 kW). The shape of the output CM current and peak values are almost similar to the results obtained with the reference parameters of VSC in Figure 4.2a.

At the first view, it can be concluded that the load does not influence the generated by the VSC conducted noise despite the variation of the output voltage fall and rise times. But this effect can be easily explained using the analysis of fall and rise times in PWM voltage which is provided in Section 2.3. As can be seen in Figure 2.13, the minimum value of fall/rise time during the fundamental period with the load of 7.5 kW is almost equal to 20 ns. This value is equal to the commutation time of MOSFET under reference parameters (see Table 3.3 and Figure 3.7). Such behaviour is observed in the case of peak detection because the highest noise level is caused by the MOSFET commutation. It means that an increase of load up to 7.5 kW should not have any impact only for the reference value of MOSFET



(a) P=3 kW



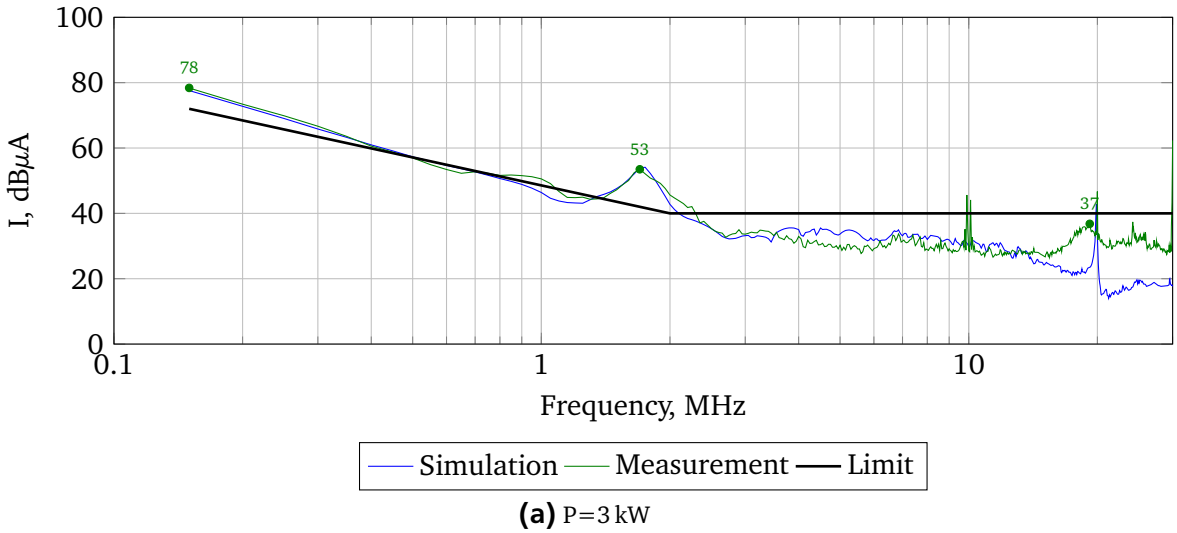
(b) P=7.5 kW

Figure 4.13.: Simulation and measurements results for the output CM current under different loads.

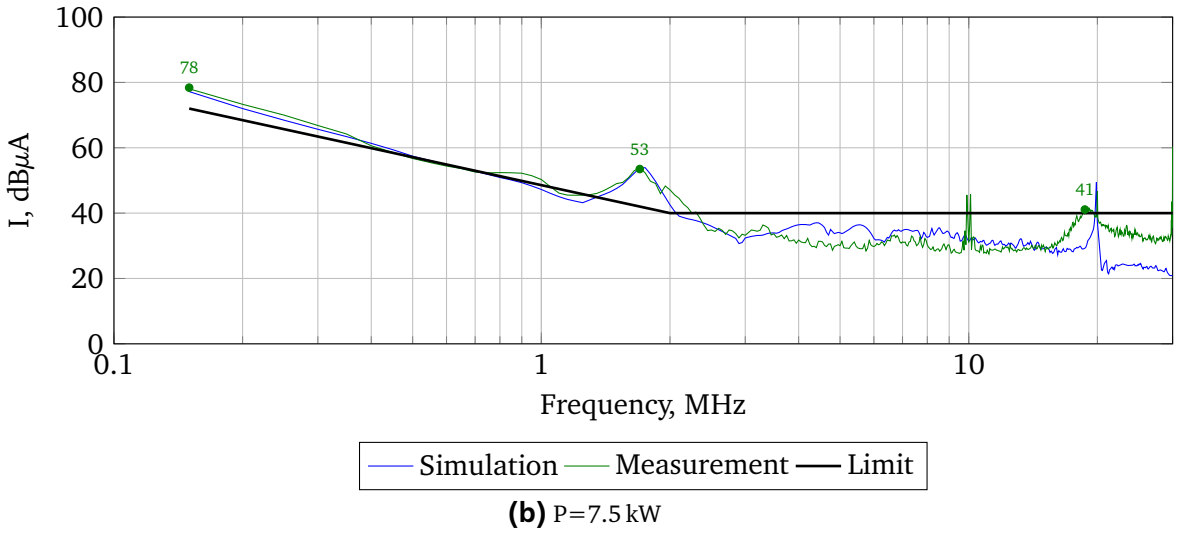
commutation time. The reference value of t_f=20 ns is always shorter than the diode commutation time in the considered load range.

However, the value of t_f was reduced down to 50 ns in order to eliminate the RF peak level in the previous subsection (see Figure 4.12). In this case, the minimum value of rise/fall time of PWM output voltage is observed during the diode commutation with high values of the output current. It means that for the peak detection, which is applied according to DO-160, the noise level at RF depends more on the value of load current. Such an assumption was validated using the experimental and simulation results. The VSC with $t_f = 50$ ns was operated under different loads applied to the AC machine. The results are presented in Figure 4.14.

Similar to Figure 4.13, the load applied to the motor was increased up to 3 kW and up to 7.5 kW. Even a small amount of additional active power in Figure 4.14a leads to an increase of RF peak at 19 MHz. Its value was increased on 2 dBμA in comparison to the results obtained under the same value of t_f but with the idle mode operation (see Figure 4.12). The MM noise was also slightly increased up to 53 dBμA. A further increase of the load leads to the noise level of 41 dBμA at the frequency of 19 MHz



(a) P=3 kW



(b) P=7.5 kW

Figure 4.14.: Simulation and measurements results for the output CM current under different loads with t_f=50 ns (R_g=15 Ω).

in Figure 4.14b. The resulting level exceeds the limit according to DO-160 despite the increased MOSFET commutation time.

This subsection discusses the impact of the VSC output current on the resulting CM noise. The output phase current was changed applying different loads to the induction motor. With a maximum commutation time of MOSFET, the phase currents do not influence the measured conducted noise in the considered load range. However, in case of increased MOSFET commutation time, load variation can lead to higher levels of EMI. The MOSFET commutation time was increased by means of gate resistance in order to reduce the noise level at RF. The results show that this kind of noise reduction techniques can be efficient only for the particular range of AC drive load. It should be also mentioned that this relationship is also defined by the type of peak detection. The proposed frequency domain models provide the possibility to evaluate such effects during the simulation.

4.5 Conclusion

This chapter provides an investigation on the different conducted noise reduction techniques which can be implemented in the AC drive. All these techniques are explained in Section 1.4. Moreover, this chapter presents the effect of MM noise which is rarely discussed for EMI of the AC drives. The investigation was provided using the simulation and measurements.

Firstly, the implementation of the EMI filter is considered. The conducted EMI was measured in the studied system with and without EMI filters. It is shown that the noise levels without any filter in the VSC are much higher than the limit according to DO-160. The designed EMI filters can reduce the noise almost to the appropriate level. Then, the structure of the input EMI filter was changed and the measurements were conducted again. The results show the relationship between the input and output sides of an AC drive. The resonance due to the additional Y-capacitors at the input was observed in the output CM current. The behaviour of EMI filters was also studied under different operation points. It is shown that a decrease of the modulation index can cause saturation of the designed output CM choke. Therefore, the design of EMI filters should be also coupled with the analysis of the operations points of the AC drive.

Due to the non-ideal components of the AC side, some amount of DM current is transferred into the CM. This effect can be observed in the CM current under reference parameters. The reference EMI filters are aimed to reduce the CM current. Therefore the MM noise (coupling to DM) becomes visible. The level of MM in the CM current was decreased by means of additional DM filter. Two structures were considered: symmetric and asymmetric. It is also explained that the ignoring of MM noise origins can lead to an oversize of the output EMI filter.

Finally, different noise reduction techniques related to the design of VSC are investigated. The goal was to reduce the level of noise avoiding the additional stages of EMI filters. Different PWM techniques are compared with the reference SVPWM. It is shown that DPWM can be used to reduce the noise level on the whole frequency range. DPWM is more effective in comparison to AZPWM. AZPWM belongs to the so-called RCMV-PWM techniques which avoid the usage of zero vectors leading to a decrease of the output CM voltage. The slight decrease of the output CM current is observed in the low-frequency range with the application AZPWM. Moreover, application of RCMV-PWMs can lead to an increase of MM noise because more energy is shifted in DM in such kind of techniques. However, AZPWM can be used to avoid the saturation of CM chokes under operation with low modulation indexes. The saturation of the CM choke was observed with SVPWM and DPWM during operation with the low value of modulation index. The level of RF noise was reduced by means of the hardware design of VSC. For these purposes, the value of gate resistance was increased in order to obtain the lower value of commutation time. But it is also shown that the load starts to impact the level of CM current with the reduced value of gate resistance. This effect was not observed with the zero value of R_g.

The results presented in this chapter are also used to validate the model proposed in Chapter 2 for the prediction of conducted EMI. The measurements show the good accordance of the simulation results for all experiments. Some minor differences are observed only for the frequencies above 10 MHz. The peak levels in RF are slightly shifted vertically and horizontally in the simulation results. This is due to the accuracy of the measured impedances (S-parameters) in the model that cannot be avoided in

any model for the conducted EMI. The shape of the RF peaks is also different in the simulation and measurements results. These peaks have the narrowband shape in the simulation and the wideband shape in the measurements results. This is due to the application of the frequency domain model. It is not possible to consider the behaviour of the switching transients which are observed during operation of VSC. However, all noise levels are reflected in the simulation results. The model is capable to analyse all considered conducted noise reduction techniques. Moreover, it is shown how can be used the proposed model to predict the saturation of CM chokes. The saturation can be also estimated for the various PWM techniques. The results show also that the method of spectrum generation for the frequency domain models proposed in Subsection 2.3.1 represents the switching behaviour of the real SiC MOSFETs with the required accuracy. The method of spectral analysis considered in Subsection 2.4.2 improves the simulation results considering the parameters of the spectrum analysers such as RBW and detection type. Consideration of these parameters is required in the AC drives that is also shown in this chapter. Last but not least, the model can predict the MM noise. The presented in the CM current additional noise levels of MM noise are easily recognized by means of the proposed model. The model can be also used to design the asymmetric EMI filters which cannot be considered in the conventional frequency domain models.

Summarizing all mentioned above, it can be concluded that the conducted noise in the VSC drive shows very complex behaviour. Different noise reduction techniques can be efficient more or less under particular conditions. These conditions are the impedance of the system which defines the resonances and the operation point of the AC drive. Combination of the different noise reduction techniques can be used to improve the overall EMI behaviour of the VSC in the particular AC drive. However, the operation points of the system should be analysed before the implementation of reduction techniques. The model developed during the research is a tool to provide such an analysis.

5 Summary and Outlook

This work discusses the effect of EMI in AC drives applied in the More Electric Aircraft. The main objective of the thesis is to consider the generated conducted EMI during the design of VSC. The work explains the nature of conducted EMI in AC drives. It presents also techniques which can be used to reduce the generated noise. An improved frequency domain model was also developed during the research. This model predicts the level of conducted EMI including all effects observed in the AC drive: different techniques of noise reduction including EMI filter and VSC design, MM noise, operation points and effect of EMI receiver. It is an attempt to consider the problem of the conducted noise in AC drives as a whole giving the link between the conducted EMI and parameters of the VSC and AC drive. A setup for EMI measurements was built during the research. The measurements are used to investigate different reduction techniques and to validate the developed model.

Conclusion

The 1st part of the thesis presents the general standard for EM emission in the civil aircraft: section 21 of DO-160. The most relevant requirements are clearly highlighted. These requirements are essential for further analysis, model building and investigation. Then, the nature of conducted EMI in the AC drives is analysed in relation to the applied standard. It is shown that the problem of EMI increases in modern power converters based on WBG power semiconductors. This is due to the high switching frequency and increased switching speed of the WBG devices. The conducted noise in AC drives is considered further in the details indicating the difference between noise at the DC and AC side of VSC. The provided analysis explains the importance of CM noise. At the same time, the DM noise, as well as the MM noise, are also considered in details. Finally, different techniques for the reduction of conducted noise are presented at the end of the 1st chapter. The conventional EMI filters are very efficient for the reduction of EMI generated by the VSC. But they can lead to a decrease of power density. The methods of EMI reduction by means of the inverter design are also presented in the 1st chapter. It is shown that these techniques can influence the noise of the particular mode (CM and/or DM) and/or in the defined frequency range. The benefits and drawbacks of such techniques are discussed as well. The 1st attempt to structure the impact of power converter hardware design on the conducted noise is provided at the end of Chapter 1. It is shown that the hardware design influences the RF EMI through the parasitics of VSC and by the switching behaviour.

The 2nd chapter of the thesis provides information about the simulation of conducted noise in the AC drives. The requirements for the model are stated in order to fulfil the objectives of the research work. The main criteria are the ability to consider all noise reduction techniques and reduced computational effort. It is shown that the frequency domain models can provide the required performance regarding the computational effort. However, the existing models should be improved in order to increase accuracy,

especially in the RF range. The MM noise cannot be considered directly in the available models. The following improvements were achieved during the research work:

- The MM noise, which occurs due to the asymmetry of the components, is considered by means of the MM n-port networks. These networks are used to describe all components of the AC drive beside the VSC. They can be obtained from the measured S-parameters. The theory of MM parameters is given in details. The MM parameters are also extended in order to apply them for the three-phase AC side of the VSC.

- A new simplified algorithm is proposed to generate the output PWM voltages of the inverter in the time domain. This data can be used in frequency domain models after the application of the Fourier transform. The proposed algorithm considers the behaviour of rising and falling edges in the VSC based on SiC MOSFETs. At the same time, the proposed algorithm requires relatively low computational resources and can be used without preliminary measurements of the switching behaviour.

- The most significant parasitics of VSC are analysed in order to improve its representation (impedance) in the frequency domain. The impedance of the designed inverter is also obtained using a FEM model that considers the parasitic capacitance between the PCB and heatsink. The proposed FEM model calculates only the parasitics of the PCB. All other components of the inverter are considered analytically in order to reduce the computational demand of the model.

- Finally, the effect of EMI receiver is also taken into account during the simulation by means of time-frequency analysis of the generated time domain PWM voltages. Application of SWDFT gives the possibility to consider the RBW and type of detection during the calculation of the frequency domain model.

The resulting model shows low computational time. Another benefit of the proposed model is that it is compatible with conventional frequency domain models. The MM parameters can be replaced by simple CM and DM impedances of the AC drive components. The algorithm for the generation of time domain and the spectral analysis can be applied in any frequency domain simulation. At the same time, the proposed model based on MM parameters can be calculated representing the PWM voltage by the trapezoidal signal. This property is essential for the 1st design stages of the VSC then some parameters of the system such as switching behaviour are unknown.

The 3rd chapter gives some details about the implemented hardware for the EMI measurements according to DO-160. The design of VSC and EMI filters is explained giving the link between hardware and simulation. The whole AC drive system is also described considering the uncertainties of the measurement setup.

The last chapter of the thesis is an investigation of the different conducted noise reduction techniques. The effect of the considered techniques is summarised in Table 5.1. The results show that EMI is a complex phenomenon in AC drives. Different reduction techniques are efficient under particular conditions. This research provides also a detailed investigation of the MM noise and its possible reduction. The additional noise level was observed in the CM current due to crosstalk to the DM. The MM noise was reduced by means of the symmetric and asymmetric DM chokes.

Table 5.1.: Impact of conducted noise reduction techniuqes on the AC drive.

Technique	Impact: Advantage(+)/Disadvantage(-)		Conditions
	EMI	VSC	
EMI filter	(+) LF and RF EMI ↓	(-) Size of passive components ↑	Possible saturation with low m Possible resonance
Switching frequency decrease (DPWM)	(+) LF and RF EMI ↓	(+) Switching losses ↓ (-) Acoustical noise ↑ (-) Size of passive components ↑ (-) THD ↑	Possible saturation
RCMV-PWM	(+) LF EMI ↓ (-) DM and MM noise ↑	(+) No passive components (-) Switching losses ↑ (-) THD ↑	Efficient with low m
Gate driver design	(+) RF EMI ↓	(+) No passive components (-) Switching losses ↑	Efficient with low output currents

The measurements results are compared with the simulation for the model validation purposes. The proposed model is able to predict the measured results correctly with small deviations in the RF range. Despite that the frequency domain models cannot be used to simulate the conducted noise under the saturation of CM chokes, it is shown how to indicate the saturation of chokes using the proposed model. The proposed model is also a very efficient tool for the analysis of MM noise. It can be used to recognize the MM noise and to design the asymmetric EMI filters. The obtained model provides the required computational efficiency. Therefore, it can be used further for the optimization procedure of the inverter including EMI behaviour.

A Three-phase Reference System Transform for EMI Analysis

The three-phase systems is a very efficient way the production of the rotating magnetic field. These systems are efficient for the transfer of electric power. The three-phase machines are the main type of motor even for modern drives. In modern electrical drives, the VSC produces three-phase PWM voltage to operate the AC machine. The components of the three-phase system (current and voltages) can be represented by three vectors which are allocated on the reference plane. The ideal system is represented by 3 vectors with equal length and 120° phase shift from each other (see Figure A.1). If the system is symmetric, it is possible to solve the circuit only for one phase. All other phases are assumed to be described with the same amplitude of voltage/current with an appropriate phase shift.

However, it is sometimes more comfortable to transform the conventional coordinates of the three-phase system depending on the application. Different transforms are presented hereunder and compared regarding its application for the simulation of conducted EMI in the AC drives.

Symmetrical components transformation

The real three-phase system is normally asymmetric with different values of voltage/current amplitudes and phase shifts. The method of symmetrical components was proposed in order to simplify the analysis of asymmetrical three-phase systems. The idea of this transform is shown in Figure A.2. Any asymmetrical three-phase system can be represented by the 3 components: positive, negative and zero sequences. Each component represents the symmetrical three-phase system. Therefore each of them can be described by only the single phasor value. The positive component has the same phase shift between vectors as in Figure A.1, whereas the negative component has the opposite values of the phase shift between $\vec{V}_a$ and $\vec{V}_b$, $\vec{V}_c$. All vectors of zero component have the same angle.

The three-phase currents and voltages can be considered using the symmetrical components. Analysing each component separately, it is possible to evaluate the amount of asymmetry in the three-

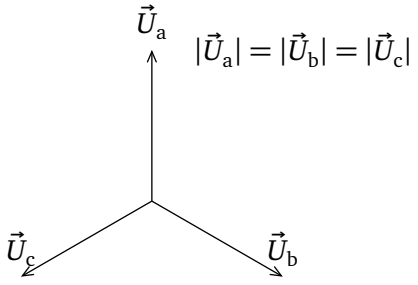


Figure A.1.: Three-phase system of voltage.

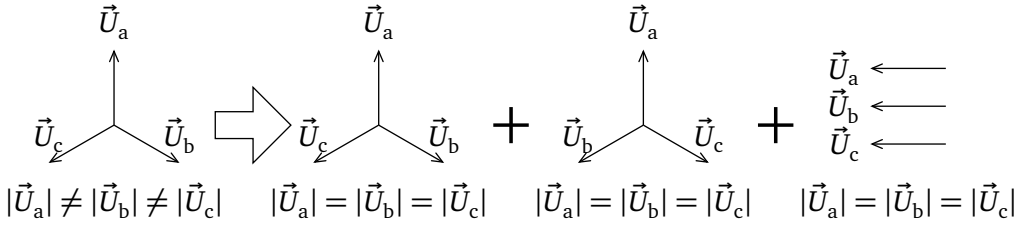


Figure A.2.: Principle of the symmetrical components.

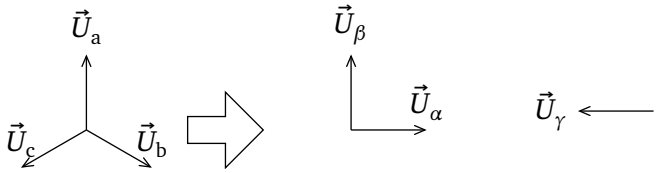


Figure A.3.: Principle of the Clarke transformation.

phase system. The transformation from three-phase voltages to symmetric components is done by means of (A.1).

$$\begin{bmatrix} U_0 \\ U_{\text{pos}} \\ U_{\text{neg}} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} \tag{A.1}$$

, where $a = -0.5 + j\frac{\sqrt{3}}{2}$ is a 120° rotation operator and U_{pos}, U_{neg}, U_0 are the amplitudes of positive, negative and zero sequences respectively.

Clarke transformation

Another commonly used type of transformation applied to three-phase systems is the so-called Clarke transform or $\alpha\beta\gamma$-transform. The principle of this transformation is explained in Figure A.3. The Clark transform divides the three-phase system on two orthogonal vectors ($\alpha\beta$) and one homopolar vector (γ).

The homopolar vector U_γ equals the zero sequence in the case of the symmetrical components transformation. The orthogonal vectors can be then used for the representation of a three-phase system by the single rotating vector $U_s = U_\alpha + jU_\beta$. The transformation from abc frame to $\alpha\beta\gamma$ coordinates is done by means of (A.2). A similar transformation can be applied to the three-phase currents.

$$\begin{bmatrix} U_\alpha \\ U_\beta \\ U_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} \tag{A.2}$$

This type of transformation is normally applied to symmetrical three-phase currents and voltages that leads to zero value of the γ coordinate. The Clarke transform is a basic transformation for SVPWM. This transformation finds the application in the control of electric drives and grid-connected converters.

Modal transformation

In Section 1.3, the principle of modal conversion, which is applied to the two-phase systems (differential lines), is explained. This principle is also extended to three-phase systems. Finally, the equations are obtained which leads to the modal transform of the three-phase coordinates. The modal conversion can be applied to the currents and voltages using (A.4) and (A.3) respectively.

$$\begin{bmatrix} U_{\mathrm{CM}} \\ U_{\mathrm{DM1}} \\ U_{\mathrm{DM2}} \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{3} & \frac{1}{3} \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} U_{\mathrm{a}} \\ U_{\mathrm{b}} \\ U_{\mathrm{c}} \end{bmatrix} \tag{A.3}$$

$$\begin{bmatrix} I_{\mathrm{CM}} \\ I_{\mathrm{DM1}} \\ I_{\mathrm{DM2}} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix} \begin{bmatrix} I_{\mathrm{a}} \\ I_{\mathrm{b}} \\ I_{\mathrm{c}} \end{bmatrix} \tag{A.4}$$

It is also possible to obtain similar transforms assuming another combination of DM voltage. In the current research works, it was decided to use modal transform with DM_1 and DM_2.

Comparison of Different Transformations

The last type of three-phase transformation is closely related to the classical two-phase modal representation which is always applied for EMI analysis. However, this kind of transform is rarely applied for the analysis in the AC drives. The proposed modal transformation is used to extend the MM parameters for the simulation of the three-phase components of an AC drive in Section 2.2. Similar extensions can be obtained using any other type of three-phase coordinate transformation. Such works were provided in [159, 41, 140] for the characterization of the three-phase EMI filters.

In order to show that the modal transformation is more beneficial in comparison to other types of transformation, the simplified 2-level three-phase inverter is considered in Figure A.4 with the input and output currents. The inverter is represented by the ideal switches and DC link capacitor. All other components of the system are ignored. The switching state of inverter in Figure A.4 corresponds to the first active state of the 2-level inverter (see Table 1.2).

The output currents in Figure A.4 are presented in the normal three-phase coordinate system (A, B and C). The currents at the input of VSC, which are flowing between the DC link capacitor and the inverter, are written in the modal form with CM and DM currents. Currents I_{p} and I_{n} are the normal

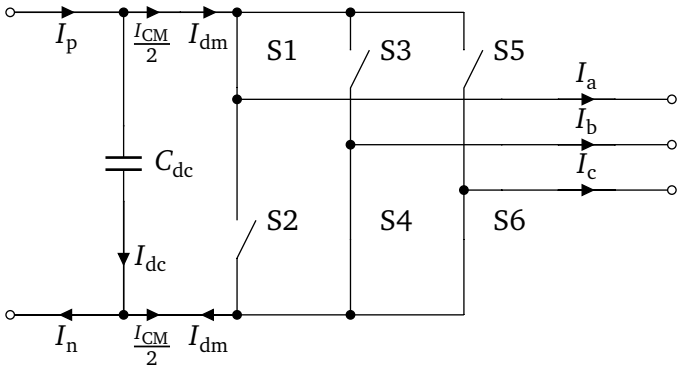


Figure A.4.: Input and output currents of the three-phase 2-level inverter in the first active state.

input currents of VSC of positive and negative rail respectively. According to Figure A.4, the sum of CM and DM current is equal to the phase current I_a, whereas the difference between these currents is equal to the sum of I_b and I_c.

$$\frac{I_{CM}}{2} + I_{DM} = I_a \tag{A.5}$$

$$\frac{I_{CM}}{2} - I_{DM} = I_b + I_c \tag{A.6}$$

Using (A.5) and (A.6), it is possible to obtain the relationship between input CM and DM currents and output phase currents.

$$I_{CM} = I_a + I_b + I_c \tag{A.7}$$

$$I_{DM} = \frac{I_a - I_b - I_c}{2} \tag{A.8}$$

Applying any reverse transformation to the phase currents I_a, I_b and I_c and replacing these currents in (A.7) and (A.8), it is possible to obtain a relationship between CM and DM at the input of VSC and output currents in different systems of coordinates.

Symmetrical components:

$$I_{CM} = 3I_0 \tag{A.9}$$

$$I_{DM} = \frac{-I_0 + (1-a^2)I_{pos} + (1-a)I_{neg}}{2} \tag{A.10}$$

Clarke transformation:

$$I_{\mathrm{CM}} = 3I_{\gamma} \tag{A.11}$$

$$I_{\mathrm{DM}} = \frac{-I_{\gamma} + I_{\alpha}}{2} \tag{A.12}$$

Three-phase modal transformation

$$I_{\mathrm{CM}} = I_{\mathrm{CM}} \tag{A.13}$$

$$I_{\mathrm{DM}} = -\frac{I_{\mathrm{CM}}}{6} + I_{\mathrm{DM1}} \tag{A.14}$$

As can be seen in (A.9)..(A.14), the input CM current is always proportional to the output homopolar component. From the CM point of view, all types of transformation are equal that is also observed in (A.1)..(A.4). At the same time, it can be concluded that the output homopolar component is presented in the input DM current as well. This effect is considered in Section 1.3 as the natural MM noise. The input DM current is also defined by the other components depending on the transformation. For the modal transform, DM_1 component is included in (A.14) without any coefficient. And this is the main benefit of the modal transformation. Considering only the AC components of the currents and ideal DC link capacitor, it can be stated that the input DM of VSC is short-circuited. In this case, the DC link capacitor closes the loop for the DM current and balances the CM currents. For the modal transformation, the current in DC link capacitor and current of the power supply are defined:

$$I_{\mathrm{p}} = -I_{\mathrm{n}} = \frac{I_{\mathrm{CM}}}{2} \tag{A.15}$$

$$I_{\mathrm{dc}} = -\frac{I_{\mathrm{CM}}}{6} - I_{\mathrm{DM1}} \tag{A.16}$$

For an ideal DC link capacitor, DM noise is observed in the form of voltage ripples (voltage drop) which reduce with a frequency increase. These ripples consist of MM noise and DM_1 according to (A.16). Similar relationships between the input and output currents can be obtained for the other states of VSC from Table 1.2. Providing such an analysis, it can be stated that under ideal conditions the CM is always fully coupled between input and output of VSC and balanced through the DC link capacitor. In the case of zero states, the DM between input and output is absolutely decoupled due to the short-circuit through the ideal switches. Depending on the active states, the input DM is coupled only with one DM of three-phase modal representation: DM_1, DM_2 and DM_3.

B Conversion of n-Port Networks Parameters

The model proposed in Chapter 2 for the conducted noise prediction in the AC drives utilizes the n-port (6- and 4-port networks for AC and DC side respectively) for the characterization of the components. During the calculation of the proposed model, it is comfortable to switch between different parameters: Z, Y and ABCD. In order to understand the conversion of n-port networks, it is necessary to represent the corresponding matrix of Z-parameters using the block matrices.

$$\begin{bmatrix} U_1 \\ U_2 \\ . \\ . \\ U_\mathrm{n} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & . & . & Z_{1\mathrm{n}} \\ Z_{21} & Z_{22} & . & . & Z_{2\mathrm{n}} \\ . & . & . & . & . \\ . & . & . & . & . \\ Z_{\mathrm{n}1} & Z_{\mathrm{n}2} & . & . & Z_{\mathrm{nn}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ . \\ . \\ I_\mathrm{n} \end{bmatrix} = \begin{bmatrix} \mathbf{Z_{11}} & \mathbf{Z_{12}} \\ \mathbf{Z_{21}} & \mathbf{Z_{22}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ . \\ . \\ I_\mathrm{n} \end{bmatrix} \tag{B.1}$$

In (B.1), it is assumed that the network has an equal number of inputs and outputs, whereas inputs are numbered from 1 to $\frac{n}{2}$ and outputs are numbered from $\frac{n}{2}+1$ to n. Using the block matrices, the separated equations for input and output voltages can be derived:

$$\begin{bmatrix} U_1 \\ . \\ . \\ U_{\frac{\mathrm{n}}{2}} \end{bmatrix} = \mathbf{u}_\mathrm{in} = \mathbf{Z_{11}}\mathbf{i}_\mathrm{in} + \mathbf{Z_{12}}\mathbf{i}_\mathrm{out} \tag{B.2}$$

$$\begin{bmatrix} U_{\frac{\mathrm{n}}{2}+1} \\ . \\ . \\ U_\mathrm{n} \end{bmatrix} = \mathbf{u}_\mathrm{out} = \mathbf{Z_{21}}\mathbf{i}_\mathrm{in} + \mathbf{Z_{22}}\mathbf{i}_\mathrm{out} \tag{B.3}$$

Using (B.3) it is possible to obtain the vector of input currents:

$$\mathbf{i}_\mathrm{in} = \mathbf{Z_{21}}^{-1}\mathbf{u}_\mathrm{out} - \mathbf{Z_{21}}^{-1}\mathbf{Z_{22}}\mathbf{i}_\mathrm{out} \tag{B.4}$$

The vector of input currents from (B.4) can be substituted in (B.2):

$$\mathbf{u}_{\text{in}} = \mathbf{Z}_{11}\mathbf{Z}_{21}{}^{-1}\mathbf{u}_{\text{out}} + \mathbf{Z}_{12} - \mathbf{Z}_{11}\mathbf{Z}_{21}{}^{-1}\mathbf{Z}_{22}\mathbf{i}_{\text{out}} \tag{B.5}$$

The ABCD parameters can be also written using the block matrices. The output currents of ABCD-parameters have a negative sign that is required for the chain connection. Comparing the block matrices of the n-port network of ABCD parameters with (B.4) and (B.5), the equation for the conversion from Z- to ABCD-parameters can be derived:

$$\begin{bmatrix} \mathbf{u}_{\text{in}} \\ \mathbf{i}_{\text{in}} \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix} \begin{bmatrix} \mathbf{u}_{\text{out}} \\ -\mathbf{i}_{\text{out}} \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{11}\mathbf{Z}_{21}{}^{-1} & \mathbf{Z}_{11}\mathbf{Z}_{21}{}^{-1}\mathbf{Z}_{22} - \mathbf{Z}_{12} \\ \mathbf{Z}_{21}{}^{-1} & \mathbf{Z}_{21}{}^{-1}\mathbf{Z}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{u}_{\text{out}} \\ -\mathbf{i}_{\text{out}} \end{bmatrix} \tag{B.6}$$

The conversion from ABDC- to Z-parameters can be obtained in a similar way:

$$\begin{bmatrix} \mathbf{u}_{\text{in}} \\ \mathbf{u}_{\text{out}} \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_{11} & \mathbf{Z}_{12} \\ \mathbf{Z}_{21} & \mathbf{Z}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{i}_{\text{in}} \\ \mathbf{i}_{\text{out}} \end{bmatrix} = \begin{bmatrix} \mathbf{A}\mathbf{C}^{-1} & \mathbf{A}\mathbf{C}^{-1}\mathbf{D} - \mathbf{B} \\ \mathbf{C}^{-1} & \mathbf{D}^{-1}\mathbf{C} \end{bmatrix} \begin{bmatrix} \mathbf{i}_{\text{in}} \\ \mathbf{i}_{\text{out}} \end{bmatrix} \tag{B.7}$$

The matrix of Y-parameters is equal to the inverse matrix of Z-parameters:

$$\mathbf{i} = \mathbf{Y}\mathbf{u} = \mathbf{Z}^{-1}\mathbf{u} \tag{B.8}$$

Depending on the connection of ports the so-called hybrid h-parameters can be required for the calculation. The number of all possible hybrid parameters is very high and increases with the number of ports. However, using block matrices it is also possible to obtain them.

C CM Chokes for EMI Filters

Section 3.1 describes the designed EMI filters which are applied to the input and output of VSC. Both filters are based on the CM chokes. Due to the size of the cores and wires, the CM chokes show the most significant impact on the weight and power density of the power core (VSC). The design of a choke requires a huge effort because it is necessary to select the core material and to apply the appropriate winding technique. Hence, only two types of CM chokes (for input and output) were designed and evaluated experimentally. The designed CM chokes are based on the nanocrystalline material Vitroperm 500F from Vacuumschmelze [153].

The main problem, which comes during the design of the CM choke, is a frequency-dependence of the magnetic material. The permeability, as well as the losses in the core, vary with the frequency increase even under small amplitudes of the current (without saturation). These two values define the broadband impedance of the choke, its real and imaginary parts. A useful tool for core characterization of magnetic core is a complex relative permeability ($\bar{\mu} = \mu' + j\mu''$) [56, 53]. Its real part defines the value of inductance of the choke. The imaginary part is associated with a resistive part (losses) of the choke impedance.

The simplest representation of a CM choke consists of series-connected inductance $L_s(f)$ and resistance $R_s(f)$ as it is shown in Figure 1.17. For the given complex permeability these values can be found using:

$$L(f) = A_L N^2 \frac{\mu'(f)}{|\bar{\mu}(f=0)|} \tag{C.1}$$

$$R(f) = A_L N^2 \omega \frac{\mu''(f)}{|\bar{\mu}(f=0)|} \tag{C.2}$$

, where A_L is an inductance per turn, N is a number of windings. The curves of complex permeability of applied material are presented in Figure C.1. Such curves are given by the manufacturer [153].

Figure C.1 shows that the magnetic properties of the considered material decrease with a frequency increase above 10 kHz. At the same time losses are increasing with a frequency making CM choke to behave like a resistor at RF. The respective elements of the CM choke replacement circuit (see Figure 1.17) are also frequency depended.

Two ring cores were selected for the design: W423 and W453 for the input and output filter respectively. Both cores are based on the same nanocrystalline material. The cores were winded as a simple CM choke with the same coated magnet wires with the diameter equal to 1.8 mm. The relevant parameters of the core and CM chokes are summarized in Table C.1. All data was obtained from the datasheet of applied cores [153].

Using the given curves of complex permeability (Figure C.1), it is possible to obtain the value of series resistance and inductance in the replacement circuit of the CM choke (see Figure 1.17). But, the RF behaviour of the CM choke is also defined by the stray parallel capacitance C_p which is also shown in

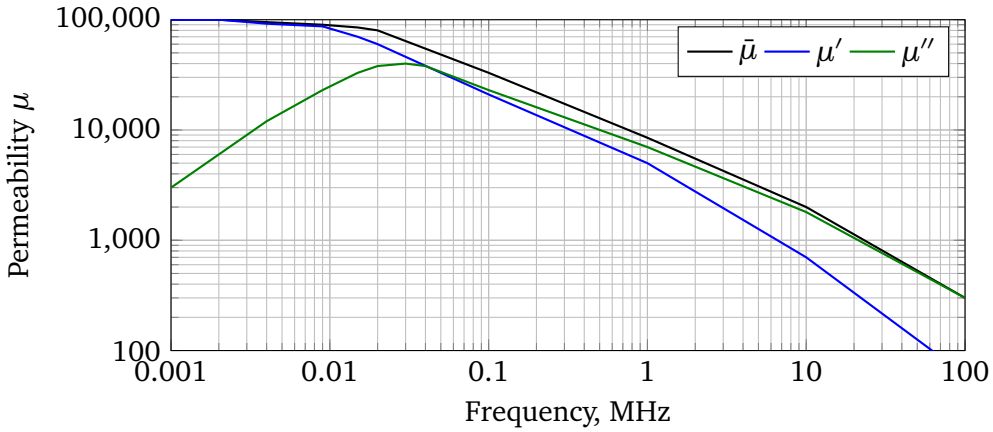


Figure C.1.: Complex permeability of the applied nanocrystalline core (Vitroperm 500F).

Table C.1.: The parameters of cores for the design of CM chokes.

Filter	Inner ⌀, mm	Outer ⌀, mm,	Height, , mm	$A_L(f = 10\,\text{kHz}), \mu\text{H}$	N	I_{sat}, mA
Input	30	20	10	59.3	7	71
Output	40	25	15	25.4	12	162

Figure 1.17. The value of C_p is formed by the stray capacitance between each turn of winding, as well as by the capacitance between winding and core [44]. Estimation of these values requires the application of complex calculation or FEM simulation as it was done in [54]. The behaviour of the core material and presence of stray capacitance complicate the characterization of the real physical CM choke. Therefore, the designed CM chokes were characterized using measured n-port networks and MM parameters as it is proposed in Section 2.2. The S-parameters of the designed CM chokes (see Figure 3.5) were measured and converted further to the MM parameters. Using ABCD-parameters, the series CM impedance of the input and output chokes were derived which can be observed in Figure C.2.

Due to the higher amount of turns, the output choke has a much higher amplitude of impedance. The behaviour of both chokes is defined mostly by values of $R_s(f)$ and $L_s(f)$ before the frequency of self-resonance (9 MHz and 1.2 MHz for the input and output cores respectively). This can be observed in the phase behaviour of the CM choke impedance in Figure C.2. In both cases, the phase before the self-resonance is lower than 90° showing the presence of losses in the considered frequency range. Such behaviour corresponds to the complex permeability shown in Figure C.1. After the self-resonance, the impedance of CM chokes decreases showing a capacitive nature. The phase changes its value to −90°. Due to the non-linear behaviour of the core material, it is relatively hard to fit the parameters of the 1st-order model of an inductor (Figure 1.17) with the measured values of the CM impedance C.2. However, as it was mentioned in Section 2.2, the fitting procedure can be avoided in the frequency domain models.

Ideally, the DM inductance of the CM choke should be equal to zero as the magnetic flux in the core formed by the DM currents is compensated. However, some amount of DM inductance is formed by the winding itself (leakage). Using MM ABCD-parameters, it also possible to extract the DM impedance of the choke. The DM impedances for the input and output CM chokes are presented in Figure C.3. The DM

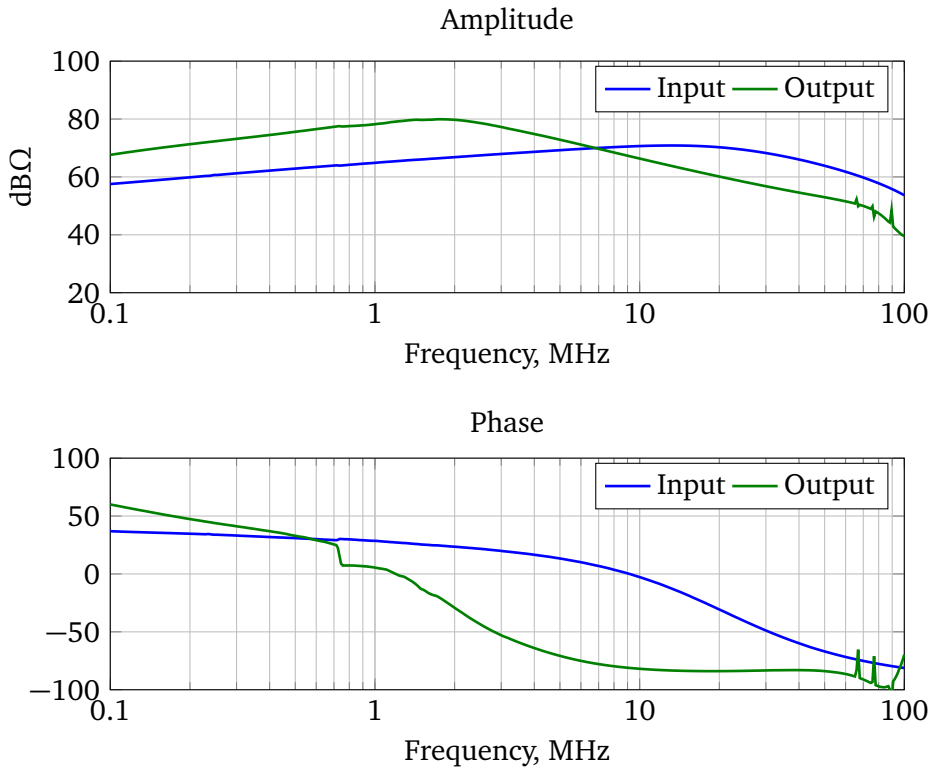


Figure C.2.: The series CM impedance of the input and output EMI filter chokes.

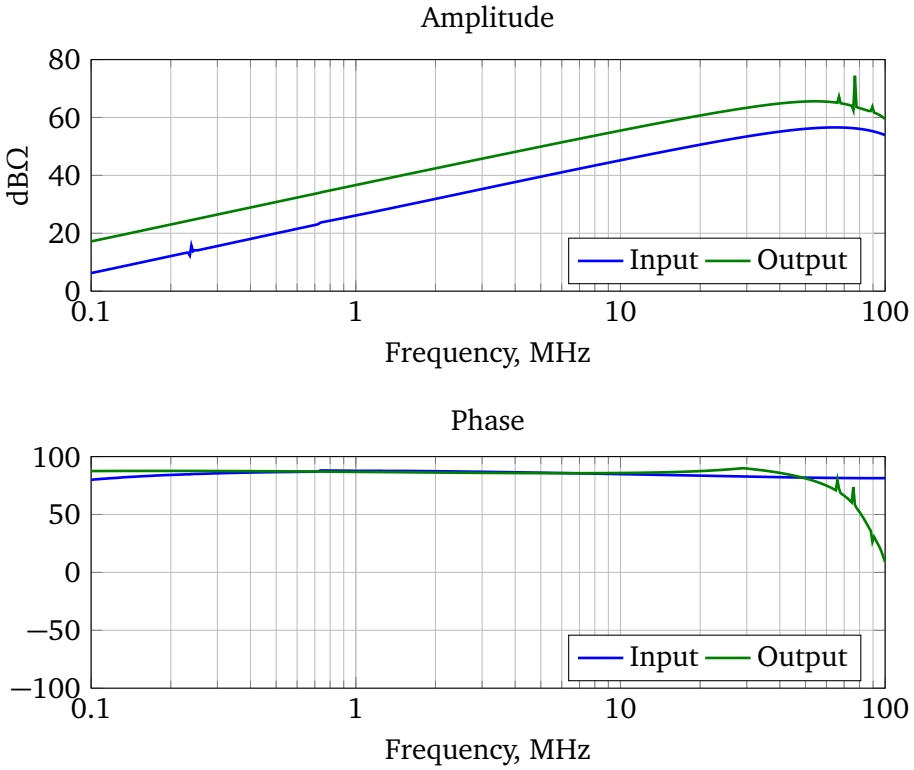


Figure C.3.: The series DM impedance of the input and output EMI filter chokes.

impedance of the CM choke is much lower than the CM in Figure C.2. The resonance at DM of the CM chokes is shifted towards higher frequency in both cases of input and output choke. The core material does not influence DM impedance. The resistive part of the DM impedance is very low because the phase is almost equal to 90° at the whole frequency range in Figure C.3. Despite, that CM inductance is much higher, the presence of stray inductance influences the DM noise in the system.

D Measurement Devices

During the conducted research the following measurement devices were applied:

- The vector network analyser was used to measure the S-parameters of the AC drive components. The applied VNA has also in-built impedance analyser which was also used during the tests.
- The oscilloscope was applied during the measurements in the time domain (voltage and currents). The oscilloscope was also used as an EMI receiver (spectrum analyser) with an application of the Fourier transform to the measured time domain data.
- Rogowski coil (active current probe) was used for the measurements of the MOSFET drain current and the output phase currents of VSC.
- The differential high voltage probe was applied for the galvanic isolated voltage measurements.
- The passive current probe was used to measure the VSC input and output CM currents which are recognized as a noise according to DO-160.
- The spectrum analyser was utilised as an EMI receiver.

The most relevant parameters of the applied measurements devices are summarized in Table D.1.

One important characteristic of the passive current probe is the transfer impedance. Its value changes with a frequency. Therefore, it should be taken into account during the acquisition of the conducted noise. The curve for the transfer impedance is normally provided by the manufacturer. For the applied probe (6600), the transfer impedance is presented in Figure D.1. The presented curve should be multiplied with the data obtained by the spectrum analyser in order to convert the results into the current.

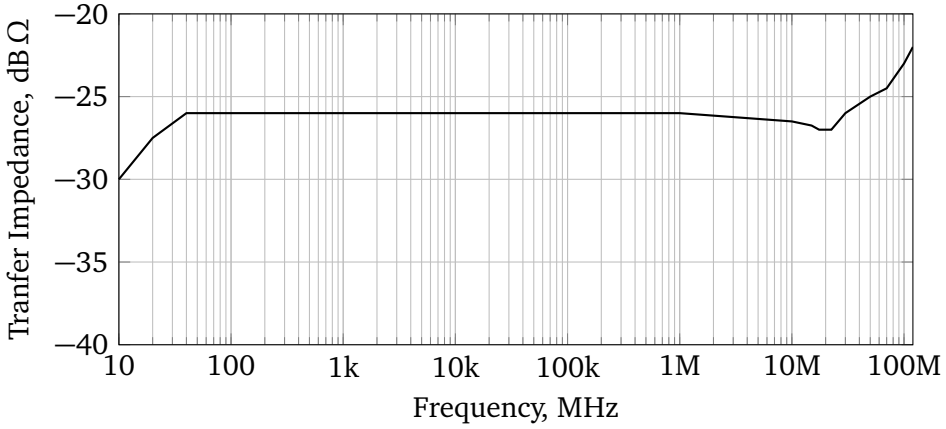


Figure D.1.: The transfer impedance of the applied passive current probe.

Table D.1.: The parameters of the applied measurements devices.

Parameter	Description
VNA	
Part number (manufacturer)	E5061B (Keysight Technologies)
Frequency range (impedance analyser)	5 Hz to 30 MHz
Frequency range (network analyser)	100 kHz to 3 GHz
Amount of ports	2
Oscilloscope	
Part number (manufacturer)	DSOS054A (Keysight Technologies)
Bandwidth	DC to 500 MHz
Vertical resolution	16 bits
Rogowski Coil	
Part number (manufacturer)	CWT03 (PEM)
Bandwidth (−3 dB)	67 Hz to 30 MHz
Current range	±60 A
Differential Probe	
Part number (manufacturer)	TT-SI 9110 (Testec)
Bandwidth (−3 dB)	DC to 100 MHz
Voltage range	±140 V 1:100 ±1400 V 1:1000
Passive Current Probe	
Part number (manufacturer)	6600 (Pearson)
Bandwidth (−3 dB)	40 Hz to 120 MHz
Current range (rms)	±40 A
Current range (peak)	±2000 A
Spectrum Analyser	
Part number (manufacturer)	N9020A (Keysight Technologies)
Frequency range	10 Hz to 26.5 GHz
Bandwidth options	25 standard, 40, 85, 125, 160 MHz
Maximum dynamic range	116 dB

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Own Publications

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Erklärung laut Promotionsordnung

§ 8 Abs. 1 lit. c PromO

Ich versichere hiermit, dass die elektronische Version meiner Dissertation mit der schriftlichen Version übereinstimmt.

§ 8 Abs. 1 lit. d PromO

Ich versichere hiermit, dass zu einem vorherigen Zeitpunkt noch keine Promotion versucht wurde. In diesem Fall sind nähere Angaben über Zeitpunkt, Hochschule, Dissertationsthema und Ergebnis dieses Versuchs mitzuteilen.

§ 9 Abs. 1 PromO

Ich versichere hiermit, dass die vorliegende Dissertation selbstständig und nur unter Verwendung der angegebenen Quellen verfasst wurde.

§ 9 Abs. 2 PromO

Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient

Darmstadt, den 27. November 2019

Danil Drozhzhin