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Non-isolated resonant link DC–DC converter for use with GaN devices

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Abstract: As new wide band-gap (WBG) devices are developed and improved, new topologies and control schemes are required to take advantage of the ultra-fast switching turn on/off speeds that are now available, without the limitations of switching losses and unacceptable EMI from fast switching transitions. This paper presents a non-isolated DC–DC resonant link converter that allows for soft switching over an extended load range that is particularly suited to GaN devices.

1 Introduction

The development of wide band-gap (WBG) devices provides an opportunity to dramatically increase the achievable switching frequencies in switch-mode power supplies. However, the incorporation of WBG devices in high-frequency hard-switched converters is limited by both the switching losses and the EMI resulting from the fast switching transitions [1, 2], in addition to the EMI generated at high switching frequencies by circuit parasitics. Thus to fully utilise their ultra-fast turn on/off times in EMI sensitive environments, WBG devices are inherently suited to soft-switched topologies. Additionally, the use of resonant passive components can allow circuit and device parasitics to be incorporated into the circuit design, further reducing EMI.

The WBG resonant converters can exploit device capacitance to achieve both low switching loss and controlled EMI. However, output voltage control of these converters requires a variable switching frequency, limiting the soft-switching load range, and resulting in unavoidable spread-spectrum switching harmonics. The resonant link converter offers the potential to exploit the ultra-fast switching capability of resonant WBG converters, while maintaining PWM-type control of the output voltage by generating high-frequency resonant pulses.

Additionally, resonant topologies generally require devices and components to be rated up to 2.5 times the supply voltage, however the clamping circuit in the resonant link topology reduces this to as low as 1.2 times the supply voltage. [3]

Much of the current research into the use of GaN switches in resonant topologies has focused on variants of the LLC converter and wireless power transfer applications [2, 4–7]. While the DC–DC resonant link converter also utilises a resonant tank, it is a non-isolated topology that does not require an output rectifier.

An 150 W 50 V to 20 V converter operating at a resonant switching frequency of 100 kHz using standard silicon devices has been simulated at the device level to demonstrate the concept. An 150 W 50 V to 20 V converter operating at a resonant switching frequency 1 MHz has also been simulated to show that converter frequency is scalable and, therefore, suitable for use with GaN devices.

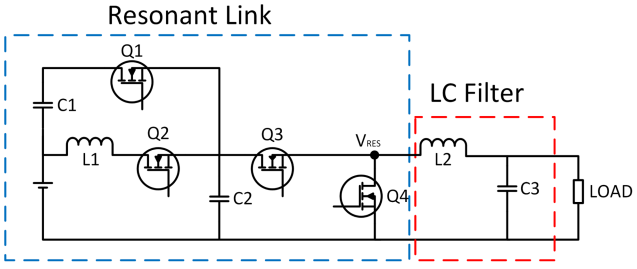

Fig. 1 *Resonant Link Topology*

2 Operation

The DC–DC non-isolated resonant link converter, as shown in Fig. 1, is a continuation of the resonant link concept, originally utilised for soft-switched resonant inverters. It uses a resonant tank to deliver energy in high-frequency pluses that together form a PWM waveform [3, 8–13] as shown in Fig. 2. This approach results in a combination of near ZVS (zero-voltage switching) and ZCS (zero-current switching) over a wide range of input and load conditions as neither the on- or off-time of the duty cycle is restricted by the resonant frequency.

The achievable voltage resolution at the load is dependent on the number of pulses per PWM duty cycle. Thus, depending on the application, the resonant frequency must be several times higher than the duty cycle frequency. For the power density of the DC–DC resonant link converter to be comparable to other soft-switched topologies such as the LLC converter, the desired switching frequency of the resonant tank would be in the region of 2–3 MHz, hence why this topology is suited to WBG devices [14].

Fig. 3 shows the conduction modes of the resonant link circuit and Fig. 4 shows the output from the resonant tank over the five stages of the resonant pulse. For the purpose of this analysis, the converter is assumed to be operating in CCM, in a steady-state condition with ideal components.

2.1 Stage 1: t_0–t_1

Initially, the load is short-circuited and the voltage at the output of the resonant tank is zero. This is the off-period for the pulsed PWM waveform. When the duty cycle changes to the 'ON' condition, $Q2$ and $Q3$ are turned on. This short-circuits the resonant link inductor $L1$ to ground, reversing the current in switch $Q4$ allowing the inductor to charge. The turn-on losses in $Q3$ and $Q4$ are significantly reduced by the limited current rise allowed by the resonant inductor, resulting in near ZCS switching.

2.2 Stage 2: t_1–t_2

During this period, the $L1$ is short-circuited, the purpose being to charge the inductor to an initial current value, $I_{L;\text{charge}}$. If the circulating current in the inductor is not high enough, there will not be enough energy in the LC tank to resonate $C1$ during Stage 3.

The length of time the inductor is short-circuited during each resonant cycle is referred to as the 'dwell time' and is estimated

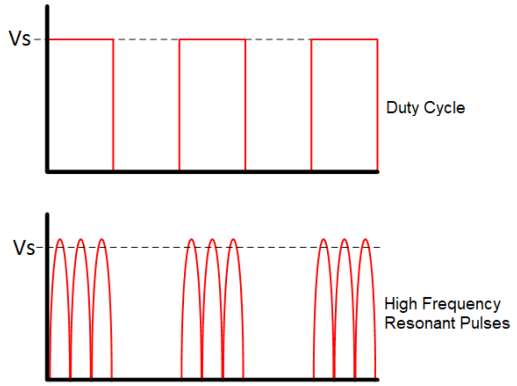

Fig. 2 *Pulsed PWM*

using (1). However, the turn-on and turn-off characteristics of the switch must also be considered.

$$v_S = v_{L1} = L1\frac{d}{dt}(i_{L1}) \Rightarrow \delta t = L1\frac{i_{L,\text{charge}}}{v_S} \tag{1}$$

2.3 Stage 3: t_2–t_3

When the current in the inductor is high enough, $Q4$ is turned off and the LC tank begins to resonate. The voltage across the $C2$ will increase until it reaches the supply voltage (v_s). At this point, the body diode of $Q1$ will begin to conduct.

During this stage, the resonant capacitor voltage is given by (2) and resonant inductor current is given by (3). Thus, the rise time for the voltage across C_2 can be calculated.

$$\begin{aligned} V_{C2}(t) = v_S - V_S\cos\left(\frac{1}{\sqrt{C_2L_1}}t\right) \\ -\frac{I_{L1}(0)\sqrt{L_1}sin(t/\sqrt{C_2L_1})}{\sqrt{C_2}} \\ +\frac{I_{\text{OUT}}\sqrt{L_1}\sin(t/\sqrt{C_2L_1})}{\sqrt{C_2}} \end{aligned} \tag{2}$$

$$\begin{aligned} I_{L1}(t) = I_{\text{OUT}} + I_{L1}(0)\cos\left(\frac{1}{\sqrt{C_2L_1}}t\right) \\ -\frac{I_{\text{OUT}}\sqrt{L_1}\cos((t/\sqrt{C_2L_1})t)}{\sqrt{L_1}} \\ +\frac{V_S\sqrt{C_2}\sin((t/\sqrt{C_2L_1})t)}{\sqrt{L_1}} \end{aligned} \tag{3}$$

2.4 Stage 4: t_3–t_4

The circuit clamp is now engaged. As the circuit resonates, the current flowing through $Q1$ will reverse polarity. The clamp switch is turned on when the clamp current reaches zero, resulting in near ZVS and ZCS. The voltage across $C2$ now resonates back down to the supply voltage. When $C1$ is fully discharged, $Q1$ is turned off.

$$v_{C1}(t) = \frac{\sin(t/\sqrt{L_1(C_1+C_2)})L_1(i_{L1}(0) - i_{\text{out}})}{\sqrt{L_1(C_1+C_2)}} \tag{4}$$

$$i_{L1}(t) = i_{\text{out}} + \cos\left(\frac{t}{\sqrt{L_1(C_1+C_2)}}\right)(i_{L1}(0) - i_{\text{out}}) \tag{5}$$

2.5 Stage 5: t_4–t_5

Once Q_1 has been turned off, the voltage across $C2$ resonates to 0 V and $S4$ is turned on under ZVS. If the duty cycle is in the 'ON' condition, the circuit continues to stage 2 and the inductor begins to charge again. If the duty cycle is in the 'OFF' condition, Q_2 and Q_3 are turned off and the circuits reverts to stage 1.

3 Design considerations and component choice

The operation of this circuit presents challenges with regard to the level of precision required for the gating signals. Control of the circuit can be simplified by using standard control techniques at a lower frequency to regulate the duty cycle and a high-frequency control loop to regulate the resonant link circuit. The required dwell time must also be calculated every duty cycle. The high speed control of the resonant link circuit can be implemented with an FPGA and the lower frequency control loop can be implemented on a DSP or an emulated C core on the FPGA.

The primary limitation to the resonant link circuit the achievable voltage resolution at the load; however, this could be greatly improved with some frequency dithering in the duty cycle, this is also desirable from EMI perspective.

There are several key design choices that must be considered when sizing passive components for the resonant link circuit; desired duty cycle frequency, desired resonant frequency, allowable overshoot, allowable circulating current, dwell time, and nominal load.

3.1 Circulating current, load current, and dwell time

One of the drawbacks to the resonant link DC–DC converter, as with other resonant topologies [15], is the high circulating current required for its operation resulting in poor low-load performance. However, the circulating current can be minimised by accurate calculation of the required dwell time at the beginning of each PWM 'ON' period. The dwell time is obtained using (2). The $I_{L1}(0)$ component must be larger than the I_{OUT} component of the sin wave. In practice, the $I_{L1}(0)$ must always be 10–20% larger than the calculated values to account for conduction losses. $I_{L1}(0)$ can then be used to calculate to dwell time for a given V_{IN} and load current by applying (1).

3.2 Resonant frequency

The resonant frequency of the circuit is defined as $1/(t_1 \rightarrow t_5)$, meaning that the resonant frequency of the circuit is dependent on the load current. While the resonant pulse spans four switching conditions, the period of the pulse is dominated by stage 3 when the clamp is engaged. The maximum possible period for Stage 4 is half of the period of (4).

$$f_{\text{resonant}} = \frac{1}{4\pi\sqrt{L_1(C_1+C_2)}} \tag{6}$$

Thus, an approximation of the minimum resonant frequency for a particular set of passive components can be given by (6).

3.3 Overshoot

The overshoot above the supply voltage seen in Stage 3 is dictated by (3).

The size of the clamp capacitor in comparison with the resonant inductor is key design trade-off that must be considered. A larger clamp capacitor reduces the voltage overshoot above the supply voltage but requires a larger circulating current to resonate, increasing conduction losses and reducing efficiency.

3.4 Duty cycle frequency

The maximum achievable duty cycle frequency is dictated by the load requirements and the maximum resonant frequency. Thus, in order for the duty cycle frequency to remain constant over a range of loads, it must be at least an order of magnitude higher than the maximum resonant frequency; i.e. there are at least 10 resonant pulses per duty cycle period. This is to ensure that output voltage can be controlled to a high level of accuracy. If some change in the duty cycle frequency is allowable, the output voltage can be controlled more accurately with a fewer number of pulses per duty cycle.

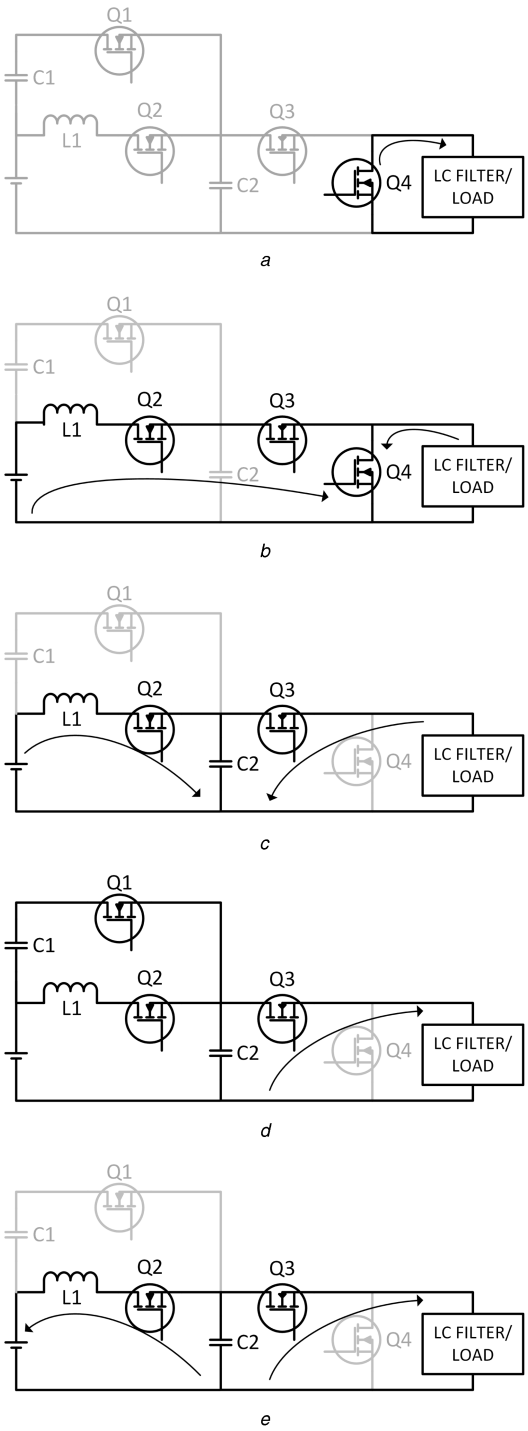

Fig. 3 *Conduction Modes*
(a) Stage 1: t_0–t_1, ***(b)*** Stage 2: t_1–t_2, ***(c)*** Stage 3: t_2–t_3, ***(d)*** Stage 4: t_3–t_4 and ***(e)*** Stage 5: t_4–t_5

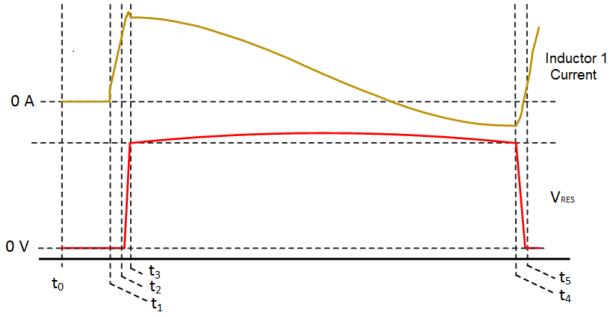

Fig. 4 *Resonant Pulse Current and Voltage*

4 100 kHz resonant link PSpice simulation

A 160 W 50 V to 20 V converter has been simulated using Infinion IPA086N10N3 MOSFET PSpice device models in SIMetrix. The control for the resonant link circuit has been implemented using discreet logic models. The propagation delay of the logic model was set to the predicted propagation delay of the control scheme implemented on an FPGA. Fig. 5 shows the simulated resonant pulse current and voltage. Table 1 shows the circuit details, and Table 2 shows the component values used in the simulation.

4.1 Losses

As can be seen from Table 3, the losses in the converter can almost be entirely attributed to conduction losses. The switch with the highest losses is $Q4$ as it is connected directly to ground during Stage 1. $Q3$ experiences some switching losses as it is not entirely soft-switched.

4.2 Switching transitions

i. $Q1$ *Switching Transitions*: Fig. 6 shows the turn-on and turn-off switching transitions for $Q1$. Both turn-off and turn-on switching transitions occur under ZVS conditions as $C1$ is fully discharged and the dv/dt is limited by the frequency of the resonant tank.
ii. $Q2$ *Switching Transitions*: Fig. 6 shows the turn-on and turn-off switching transitions for $Q2$. Both the turn-on and turn-off of transitions occur under ZCS conditions.
iii. $Q3$ *Switching Transitions*: Fig. 7 shows the turn-on and turn-off switching transitions for $Q3$. $Q3$ turn-off occurs under ZVS as $C2$ is fully discharged. There are some switching losses across $Q3$ during turn on because $Q4$ is conducting the load current and as $Q3$ turns on, this current reverses causing ring on the switch.
iv. $Q4$ *Switching Transitions*: Fig. 7 shows the turn-on and turn-off switching transitions for $Q4$. Both turn-off and turn-on switching transitions occur under ZVS conditions. During turn-off, the dv/dt across the switch is limited by the resonant tank, and during turn-on, $C2$ is fully discharged allowing $Q4$ to turn-on under ZVS. Tables 4 and 5.

5 1 MHz DC–DC resonant link converter PSipce simulation

A 1 MHz resonant link converter was simulated in SIMEtrix using Spice switch models for the GaN Systems 100 V, 90 A GaN device (GS61008P), the details of which are shown in IV. The converter operates at an efficiency of 96.4% showing that the increased switching frequency had no effect on efficiency. The GaN switch model used in this simulation has a lower on-state resistance, and the smaller passive components allowed for lower conduction losses. Fig. 8 shows resonant pulse, output voltage, and output current.

6 Hardware

For hardware and control verification, both the 100 kHz and 1 MHz resonant converters presented here will be built and tested. The 100 KHz converter will have the capability to switch between different values of C_1 and C_2 allowing for the efficiency of the converter to be examined at different resonant frequencies while using the same devices. This will present several practical challenges including high-speed current sensing, driving the devices, and high-speed control.

7 Conclusion

These simulations have shown the resonant link can achieve soft-switching and high efficiency. This converter topology could be used to manage the EMI generated as the result of ultra-fast switching transitions. However, the control of this converter is very complex and sensitive to propagation delay. Any mistimed

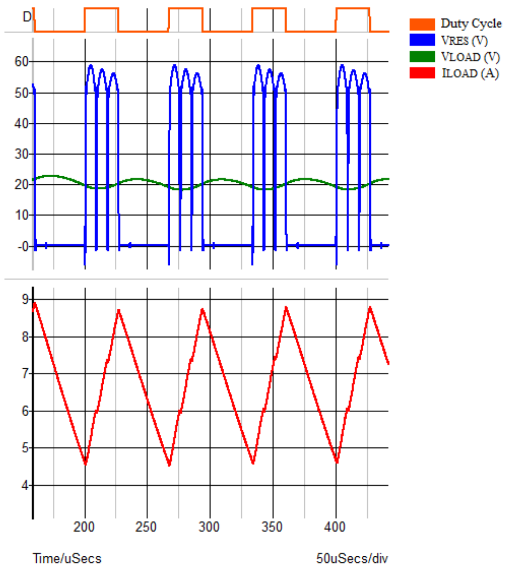

Fig. 5 *100 kHz resonant pulse voltage, output current and output voltage*

Table 1 100 kHz resonant link

Resonant link circuit details	
resonant frequency	100 kHz
power rating	152 W
PWM frequency	20 kHz
V_{IN}	50 V
V_{LOAD}	20 V
load current	7.6 A

Table 2 100 kHz resonant link component values

Resonant link passive components		
L1	3 μH	20 m Ω ESR
C1	2 μF	3 m Ω ESR
C2	10 nF	3 μ Ω ESR
	LC filter values	
L2	200 μH	100 m Ω ESR
C3	10 μF	100 m Ω ESR

Table 3 100 kHz resonant link losses

Resonant Link Circuit: Losses Break Down		
overall efficiency	95.7%	—
L1	721 mW	—
LC Filter	1467 mW	—
—	Conduction losses	Switching losses
Q1 Losses	269 mW	114 mW
Q2 Losses	435 mW	131 MW
Q3 Losses	326 mW	211 MW
Q4 Losses	412 mW	218 mW

switching signals can result in large overshoots and excessive ringing. Future work will include hardware verification of the simulation results presented here.

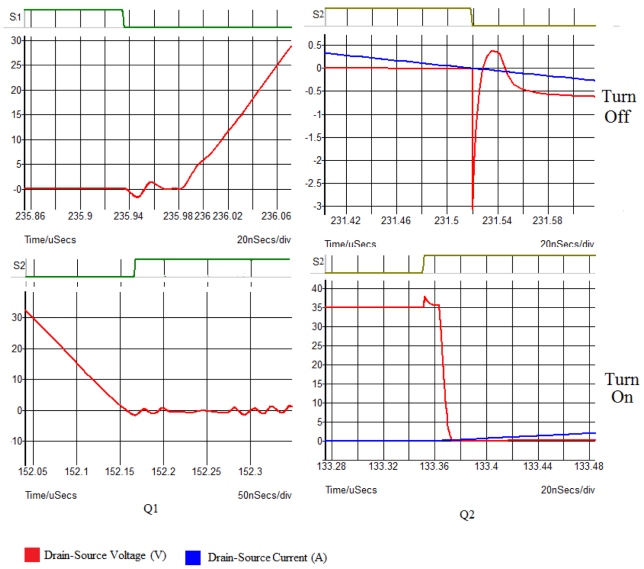

Fig. 6 *Q1 and Q2 switching transitions*

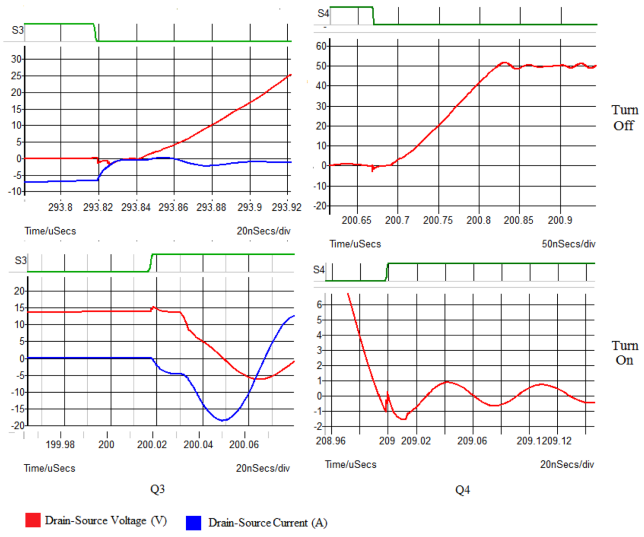

Fig. 7 *Q3 and Q4 switching transitions*

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Table 4 100 kHz resonant link

Resonant link circuit details	
resonant frequency	1 MHz
power rating	151 W
PWM frequency	150 kHz
V_{IN}	50 V
V_{LOAD}	21 V
load current	7.1 A

Table 5 100 kHz resonant link component values

1 MHz DC-DC resonant link passive components		
L1	300 nH	1 M Ω ESR
C1	2 µF	1 m Ω ESR
C2	200 nF	1 m Ω ESR
LC filter values		
L2	200 µH	100 m Ω ESR
C3	10 µF	100 m Ω ESR

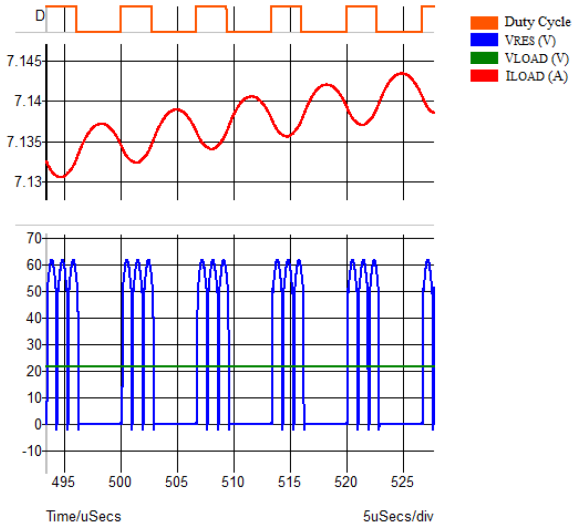

Fig. 8 *1 MHz resonant pulse voltage, output current and output voltage*