Development of Silicon Photonic Multi Chip Module Transceivers

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Abstract

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The exponential growth of data generation–driven in part by the proliferation of applications such as high definition streaming, artificial intelligence, and the internet of things–presents an impending bottleneck for electrical interconnects to fulfill data center bandwidth demands. Links now require bandwidths in excess of multiple Tbps while operating on the order of picojoules per bit, in addition to constraints on areal bandwidth densities and pin I/O bandwidth densities. Optical communications built on a silicon photonic platform offers a potential solution to develop power efficient, high bandwidth, low attenuation, small footprint links, all while building off the mature CMOS ecosystem. The development of silicon photonic foundries supporting multi project wafer runs with associated process design kit components supports a path towards widespread commercial production by increasing production volume while reducing fabrication and development costs. While silicon photonics can always be improved in terms of performance and yield, one of the central challenges is the integration of the silicon photonic integrated circuits with the driving electronic integrated circuits and data generating compute nodes such as CPUs, FPGAs, and ASICs. The co-packaging of the photonics with the electronics is crucial for adoption of silicon photonics in datacenters, as improper integration negates all the potential benefits of silicon photonics.

The work in this dissertation is centered around the development of silicon photonic multi chip module transceivers to aid in the deployment of silicon photonics within data centers.

Section one focuses on silicon photonic integration and highlights multiple integrated transceiver prototypes. The central prototype features a photonic integrated circuit with bus waveguides with WDM microdisk modulators for the transmitter and WDM demuxes with drop ports to photodiodes for the receiver. The 2.5D integrated prototype utilizes a thinned silicon interposer and TIA electronic integrated circuits. The architecture, integration, characterization, performance, and scalability of the prototype are discussed. The development of this first prototype identified key design considerations necessary for designing multi chip module silicon photonic prototypes, which will be addressed in this section. Finally, other multi chip module silicon photonic prototypes will be overviewed. These include a 2.5D integrated transceiver with a different electronic integrated circuit TIA, a 3D integrated receiver, an active interposer network on chip, and a 2.5D integrated transceiver with custom electronic integrated circuits.

Section two focuses on research that supports the development of silicon photonic transceivers. The thermal crosstalk from neighboring microdisk modulators as a function of modulator pitch is investigated. As modulators are placed at denser pitches to accommodate areal bandwidth density requirements in transceivers, this thermal crosstalk will become significant. In this section, designs and results from several iterations of custom microring modulators are reported. Custom microring modulators allow for scaling up the number of channels in microring transceivers by offering the ability to fabricate variable resonances and provide a platform for further innovation in bandwidth, free spectral range, and energy efficiency. The designs and results of higher order modulation format modulators, both microring based and Mach Zehnder based, are discussed. High order modulators offer a path towards scaling transceiver total throughput without having to increase the channel counts or component bandwidth.

Together, the work in these two sections supports the development of silicon photonic transceivers to aid in the adoption of silicon photonics into data generating systems.

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Glossary

AFE Analog Front End.

ASIC Application Specific Integrated Circuit.

BER Bit Error Rate.

BGA Ball Grid Array.

BW Bandwidth.

CDR Clock Data Recovery.

CGIP Ceramic Glass Interposer.

CMOS Complementary Metal Oxide Semiconductor.

CPU Central Processing Unit.

CPW Coplanar Waveguide.

DC Direct Current.

DFE Decision Feedback Equalization.

DP Dual Polarization.

DPSK Differential Phase Shift Keying.

DSA Digital Serial Analyzer.

DSP Digital Signal Processing.

DWDM Dense Wavelength Division Multiplexing.

EDFA Erbium Doped Fiber Amplifier.

EIC Electronic Integrated Circuit.

ENEPIG Electroless Nickel Electroless Palladium Immersion Gold.

ER Extinction Ratio.

FDTD Finite Difference Time Domain.

FEC Forward Error Correction.

FinFET Fin Field Effect Transistor.

FPGA Field Programmable Gate Array.

FSR Free Spectral Range.

FWHM Full Width Half Maximum.

Gbps Gigabits Per Second.

GDS Graphic Design System.

GPIB General Purpose Interface Bus.

GPU Graphics Processing Unit.

GSG Ground Signal Ground.

HPC High Performance Computing.

I/O Input/Output.

IC Integrated Circuit.

IL Insertion Loss.

IQ In-Phase/Quadrature.

ISI Inter Symbol Interference.

LTCC Low Temperature Co-fired Ceramic.

MCM Multi Chip Module.

MDM Mode Division Multiplexing.

MPW Multi Project Wafer.

MRM Microring Modulator.

MZI Mach Zehnder Interferometer.

MZM Mach-Zehnder Modulator.

NRZ Non Return to Zero.

OOK On Off Keyed.

OSA Optical Spectrum Analyzer.

PAM Pulse Amplitude Modulation.

PCB Printed Circuit Board.

PD Photodiode.

PDK Process Design Kit.

PDM Polarization Division Multiplexing.

PIC Photonic Integrated Circuit.

PIN P-type/Intrinsic/N-Type Diode.

PM Polarization Multiplexing.

PN P-type/N-type Diode.

PNA Precision Network Analyzer.

PP Power Penalty.

PPG Pulse Pattern Generator.

PRBS Pseudo Random Binary Sequence.

QAM Quadrature Amplitude Modulation.

QFN Quad Flat No Leads.

QLL Quadrature Locked Loop.

QPSK Quadrature Phase Shift Keying.

QSFP Quad Small Form Factor Pluggable.

RF Radio Frequency.

RSSI Received Signal Strength Indicator.

RX Receiver.

SERDES Serializer Deserializer.

SiN Silicon Nitride.

SiP Silicon Photonics.

SMA Sub Miniature Version A.

SNR Signal to Noise Ratio.

Tbps Terabits Per Second.

TCI ThruChip Interface.

TE Transverse Electric.

TIA Transimpedance Amplifier.

TM Transverse Magnetic.

TSV Through Silicon Via.

TX Transmitter.

VCO Voltage Controlled Oscillator.

VCSEL Vertical Cavity Surface Emitting Laser.

VOA Variable Optical Attenuator.

WAFT Waveguide Array to Fiber Transposer.

WDM Wavelength Division Multiplexing.

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Dedication

This dissertation is dedicated to my parents, Arne and Elaine.

Chapter 1: Introduction

1.1 High Performance Interconnect Traffic Growth

With global internet traffic expected to reach 350 exabytes per month by 2022, the demand on data center interconnect bandwidths continues to increase at an exponential rate [1], as shown in Figure 1.1a. This growth is driven by an increase in devices connected to the internet (Internet of Things and personal smartphones) and a rise of traffic heavy applications (high definition streaming, cloud computing, and big data).

Similarly, data center energy consumption trends predict a worldwide 3 PWh electricity usage by data centers by 2030, with worst case estimates as high 8 PWh, as shown in Figure 1.1b [2]. Keeping up with the internet traffic requires data center node bandwidths approaching 10 Tbps [3], while also reducing energy consumption from tens of pJ/bit to sub-pJ/bit to combat the data center energy consumption trends [4, 5]. The number of input/output (I/O) pins per package tends to double every six years, which is outpaced by the total I/O bandwidth doubling every three to four years. Resolving these rate discrepancies requires that every three to four years the bandwidth per I/O is doubled [6].

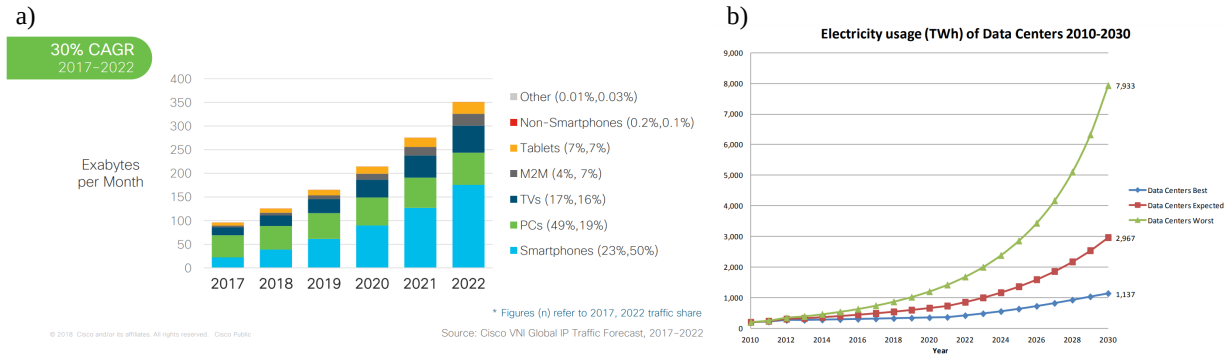

Figure 1.1: a) Total internet traffic per month, broken down by device type, adopted from [1]. b) Total data center energy consumption, adopted from [2].

Increasing the I/O data rate can be attempted by simply increasing the electrical data rate; however, attenuation and intersymbol interference from dispersion become significant issues at higher frequencies. Intersymbol interference can be combatted with additional equalization circuitry, with the tradeoff of higher energy consumption. The data rate at which equalization is necessary depends on the electrical cable type—for an eight-inch high-performance cable, the cutoff is 20 Gbps [7]. Equalization can increase the achievable data rate, but a second cutoff rate exists for which equalization becomes prohibitively energy expensive due to timing path limitations of the CMOS technology node. For the 45 nm and 16 nm nodes the cutoff rates are 20 Gbps and 40 Gbps, respectively [7]. As a result, electrical interconnects are facing a bottleneck in keeping pace with the data center bandwidth and energy consumption requirements.

The idea of using optical interconnects as a potential solution to overcome this electronic bottleneck has existed for decades [8]. Optical interconnects have played a role in long haul telecommunications since the 1970s [9]. But now, as the bandwidth and energy consumption requirements become more stringent within data centers and other datacommunication interconnects, optical interconnects are being looked at for increasingly shorter distances [10, 11]. The demands of data center interconnects have made silicon photonics an ideal candidate for ushering optics into the datacommunication regime. Integrating silicon photonics into the data center provides a path to keep up with the datacommunication interconnect requirements due to minimal signal attenuation, low energy consumption, high bandwidth, and the ability to leverage the mature Complementary Metal Oxide Semiconductor (CMOS) ecosystem [12, 5, 13, 14].

1.2 Silicon Photonic Devices

1.2.1 Passive Devices

Silicon presents a favorable platform for guiding optical signals on chip. The combination of minimal crystal defects in silicon and silicon dioxide with the strong mode confinement due to the high index contrast between silicon and silicon dioxide (3.47 and 1.44, respectively [15]) make for the construction of silicon photonic waveguides. The minimal crystal defects support low

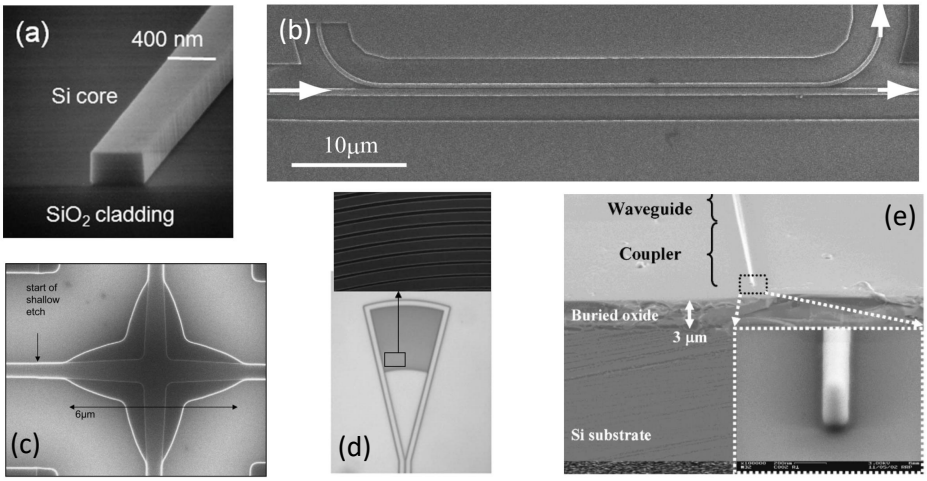

Figure 1.2: Examples of passive components fabricated in silicon platforms. a) A silicon photonic wire waveguide, adopted from [15]. b) A polarization splitter-rotator, adopted from [27]. c) A low-loss, low-crosstalk waveguide crossing, adopted from [28]. d) A silicon photonic grating coupler, adopted from [21]. e) A reverse tapered edge coupler, adopted from [29].

loss waveguide performance, and the high index contrast supports tight bending radii to enable the fabrication of small footprint photonic devices. Silicon photonic platforms have demonstrated consistent losses below 1 dB/cm [16, 17, 18], with losses as low as 0.3 dB/cm reported [19]. Microrings with bending radii of 1.5 μm have been fabricated, demonstrating the potential for small footprint silicon photonic devices [20]. Passive components have been developed to support the functionality of the silicon photonic platform. Light can be coupled into a silicon photonic integrated circuit (PIC) both vertically and horizontally. Vertical coupling is achieved through grating couplers created from a partial silicon etch [21]. Horizontal coupling is achieved through a reverse taper of the silicon waveguide to expand the waveguide mode to provide modal matching between the edge coupler and the fiber [22]. Low loss waveguide crossings [23, 24] and polarization rotators and splitters [25, 26] have been demonstrated to allow for the fabrication of more complex photonic architectures.

1.2.2 Active Devices

Active silicon photonic devices operate through changing the effective index of the optical mode. Within silicon photonics, the two most common approaches are the thermo-optic effect and the plasma dispersion effect. Silicon exhibits a strong thermo-optic coefficient [30, 31]:

$$\Delta n_{\mathrm{Si}} = 1.8 \times 10^{-4} \Delta T \ \mathrm{K}^{-1} \tag{1.1}$$

enabling resistive heaters to be constructed from metal layers or doped silicon to tune the effective index of silicon devices. The tuning efficiency and response time depend largely on the heater design, but the non-instantaneous rate of heat diffusion means that thermal tuning typically exists in the microsecond to millisecond regime [32], with switching speeds below 10 µs considered to be high speed for thermo-optic tuning [33]. To operate at higher speeds in silicon, it is necessary to utilize the plasma dispersion effect. In silicon, the presence of free carriers affects the real and imaginary refractive index, which changes the refractive index and absorption in silicon. At 1550 nm, the effects can be quantified as [34, 35]:

$$\Delta n = \Delta n_{\mathrm{e}} + \Delta n_{\mathrm{h}} = -[5.40 \times 10^{-22} \times \Delta N_{\mathrm{e}}^{1.011} + 1.53 \times 10^{-18} \times \Delta N_{\mathrm{h}}^{0.838}] \tag{1.2}$$

$$\Delta \alpha = \Delta \alpha_{\mathrm{e}} + \Delta \alpha_{\mathrm{h}} = 8.88 \times 10^{-21} \times \Delta N_{\mathrm{e}}^{1.167} + 5.84 \times 10^{-20} \times \Delta N_{\mathrm{h}}^{1.109} \tag{1.3}$$

In the above equations, n is the index, α is the absorption, N is the carrier concentration, and the e and h subscripts correspond to electrons and holes, respectively. The performance of the plasma dispersion effect depends on the diode structure used to implement it. Early modulators employed carrier injection with a forward biased PIN diode: p-type, intrinsic, n-type. While the plasma dispersion effect impacts the optical absorption, the change in absorption is not strong enough to construct effective waveguide electro-absorption modulators capable of high speed modulation. Electro-absorption modulators in silicon platforms have been demonstrated, but require introduc-

ing an additional material, such germanium for waveguide GeSi electro-absorption modulators [36]. Thus, modulation employing the plasma dispersion effect focuses on changing the refractive index. Developing modulators that take advantage of the index change requires inserting the high speed phase modulators in larger structures to transform the phase modulation to amplitude modulation. The most common approaches for this are Mach-Zehnder modulators (MZM) and resonant microring modulators (MRM). The main drawback for carrier injection is the modulation speed limitation due to the minority carrier lifetime [37]. Carrier injection modulators typically exhibit bandwidths on the order of 1 GHz [38, 39, 40]. While pre-emphasis driver techniques have extended carrier injection devices with bandwidths of 800 MHz up to modulation rates of 25 Gbps [41], the main application of carrier injection is now for fast optical switching. The large carrier concentration change from intrinsic to injected carriers allows for large enough refractive index changes to support the extinction ratios necessary for switching applications, and the GHz bandwidth is sufficient for switching applications.

The most common approach for increasing the modulation rate of the plasma dispersion effect is to utilize a carrier depletion approach with a reverse biased PN diode. Varying the reverse bias varies the depletion width of the diode, which alters the carrier density in the waveguide to modulate the index of refraction. This approach is not bounded by the minority carrier lifetime and was predicted to have a theoretical bandwidth of 50 GHz [42]. Modulators utilizing carrier depletion in PN diodes have demonstrated data rates of 64 Gbaud in both MZMs [43] and MRMs [44]. The combination of silicon passive and active components creates a platform on which a variety of functionalities can be developed, such as modulating, filtering, and switching. However, creating a full photonic interconnect link requires lasing sources and photodetectors.

1.2.3 Lasers and Detectors

Silicon has an indirect bangap, which prevents electrons from directly emitting photons [48], which makes developing integrated lasing sources and photodetectors in silicon challenging. Raman lasers have been demonstrated in silicon [47, 49], but struggle with free carrier absorption and

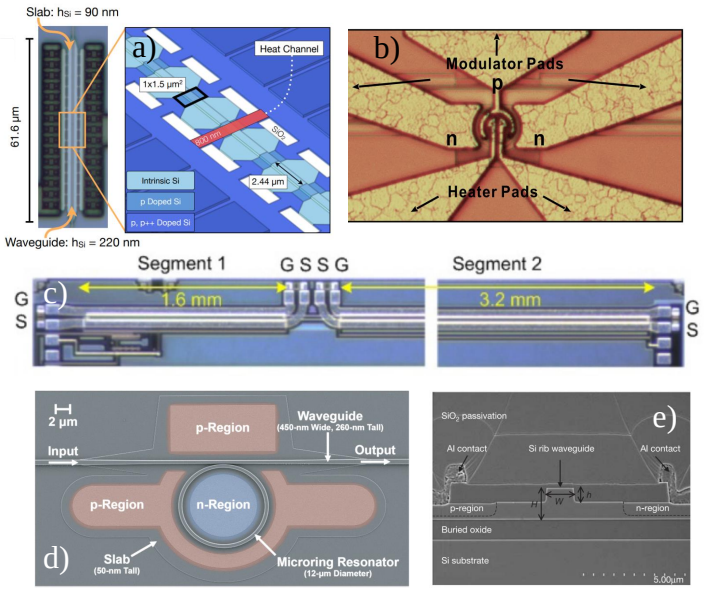

Figure 1.3: Examples of active devices in silicon photonic platforms. a) A thermo optic heater, adopted from [45]. b) A PN depletion microring modulator, adopted from [44]. c) A PN depletion Mach Zehnder modulator, adopted from [43]. d) A PIN injection microring modulator, adopted from [46]. e) A side profile of a PIN diode, adopted from [47].

two-photon absorption [50]. Integration of III-V materials with silicon to develop lasers within a silicon photonic platform has been successful, but they sometimes struggle with yield [51, 52, 53, 54]. While all silicon photodetectors have been explored [55], they do not perform as well as germanium photodetectors in terms of electro-optic bandwidth, dark current, and responsivity. Germanium integrates well with silicon, as it is also a group IV material, and is utilized in CMOS fabs [56]. For those reasons, germanium on silicon is the most common approach for fabricating photodetectors within a silicon platform [57, 58, 59]. Germanium on silicon photodiodes have been demonstrated with bandwidths above 100 GHz [60].

1.3 Silicon Photonic Foundries

The deployment of silicon photonics into datacenters and other high performance datacommunication applications is further supported by the rise of silicon photonic foundries. While multi project wafer (MPW) runs utilizing process design kit (PDK) components have been a staple in the elctronic CMOS fabrication flow, it is a recent development for silicon photonics. MPWs

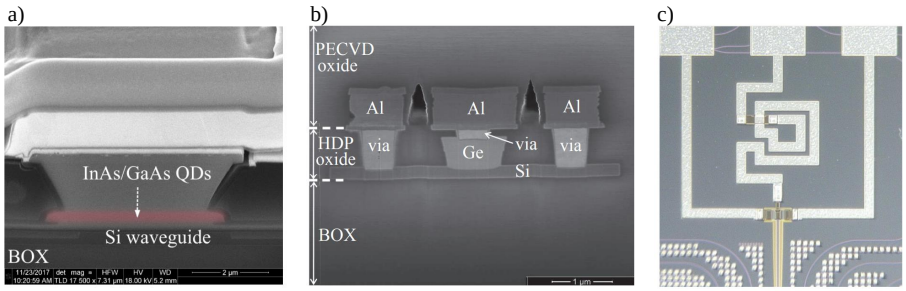

Figure 1.4: Examples of lasers and detectors fabricated in a silicon platform. a) A quantum dot InAs/GaAs DFB laser integrated on a silicon waveguide, adopted from [53]. b) A germanium waveguide photodiode side profile, adopted from [57]. c) A germanium photodetector with inductive gain peaking, viewed from above, adopted from [61].

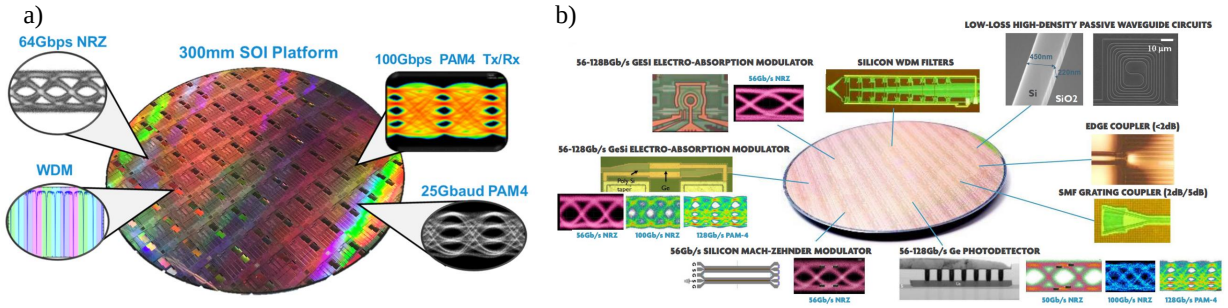

Figure 1.5: Examples of MPW PDK foundry offerings. a) AIM MPW PDK, adopted from [63]. b) iMEC MPW PDK, adopted from [64].

lower the bar to entry, as an organization can purchase a tile on wafer rather than the full wafer. The regularly scheduled runs allow designers to develop research or commercial plans utilizing MPWs. Foundries offering silicon photonic only MPWs include IME, IMEC, Leti, AIM, and TowerJazz. GlobalFoundries offers a monolithically integrated silicon photonic and electronic MPW [62]. Foundries offering MPW runs will often include PDK components that can be used on the MPW run. PDKs provide known good designs for various components, allowing a designer to focus on the high-level architecture or focus on the design of speciality components while employing PDKs elements for the other components. Silicon photonic PDK components have included grating couplers, edge couplers, waveguide crossings, MZI switches, microring switches, MZI modulators, microring modulators, and photodetectors.

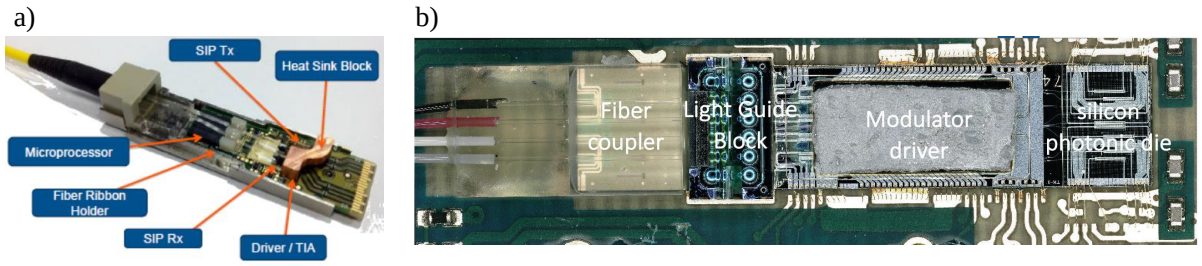

Figure 1.6: Examples of commercial silicon photonic transceivers. a) From Mellanox, adopted from [69]. b) From Intel, adopted from [68].

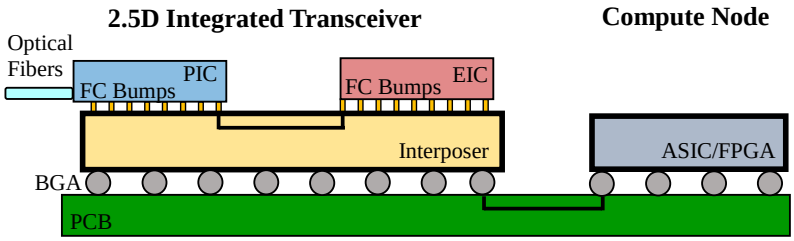

Figure 1.7: The integration approach for how the 2.5D integrated transceiver would integrate with the compute node, such as an ASIC or FPGA. While the 2.5D approach is highlighted here, other integrations would interface to a compute node in a similar manner.

1.4 Silicon Photonic Integration

The purpose of introducing silicon photonics into data centers is to increase I/O bandwidth and minimize energy consumption. Commercial silicon photonic transceivers have already been introduced to the market by Luxtera [65], Elenion [66], MACOM [67], and Intel [68].

While device performance and yield can be improved, one of the paramount challenges for widespread adoption of silicon photonics in data centers is the integration with both the driving electronic integrated circuits and the compute nodes: application-specific integrated circuits (ASICs)—such as central processing units (CPUs), graphics processing unites (GPUs), and memory—or field programmable gate arrays (FPGAs).

How the PIC is integrated with the driving EICs and the compute ICs can have a major impact on the areal bandwidth density, edge bandwidth density, and packaging parasitics. In turn, these factors directly influence the transceiver's I/O bandwidth and energy consumption—thus,

improper integration of photonics with electronics can negate all the potential benefits of silicon photonics. Parasitics between the electronic modulator driver and photonic modulator introduce parasitic poles that impact the modulator's electro-optic frequency response. In the extreme case, the parasitics can be the limiting factor in the modulator's bandwidth. Even if the modulator's bandwidth is acceptable, the effective driving voltage may be reduced, resulting in a smaller optical extinction ratio. Compensating the smaller extinction ratio requires either higher driving voltages or power-hungry multi-tap equalization circuits within the transmit (TX) or receive (RX) ICs [7]. On the receive side, the major concern is the parasitic capacitance. The total photodiode capacitance (photodiode's junction capacitance plus the parasitic capacitance) dictates the transimpedance amplifier's (TIA) dominant pole, which ultimately limits the TIA's bandwidth [70]. Receiver signal-to-noise (SNR) is inversely proportional to the squared receiver bandwidth (BW) multiplied by the total photodiode capacitance (C_{PD}): $SNR \approx (BW^2 C_{\mathrm{PD}})^{-1}$ [11]. Increased parasitic capacitance results in a lower SNR for a given bandwidth or requires reducing bandwidth to maintain the SNR. Finally, the components that make hybrid integration possible—pads, wirebonds, solder bumps, copper pillars, and through silicon vias (TSVs)—are difficult to control from an impedance perspective. Reflections from impedance mismatch can reduce the effective driving voltage and introduce additional noise to the signal [6]. A number of multi chip module (MCM) approaches for integrating silicon photonics with electronics to develop transceivers have been explored: monolithic, 2D, 3D, 3D active interposer, and 2.5D.

1.4.1 Monolithic Integration

Monolithic integration is when the photonic components are developed into an existing electronic process node with minimal to no process alterations, as shown in Figure 1.8. In this approach, parasitics are kept to an absolute minimum as the active photonics and their driving electronics are co-located within the same die. Removing the need for pads and bumps to interface between the PIC and EIC minimizes the potential for impedance mismatch due to packaging. By combining two potential dies into one, the required packaging is simplified—a monolithic

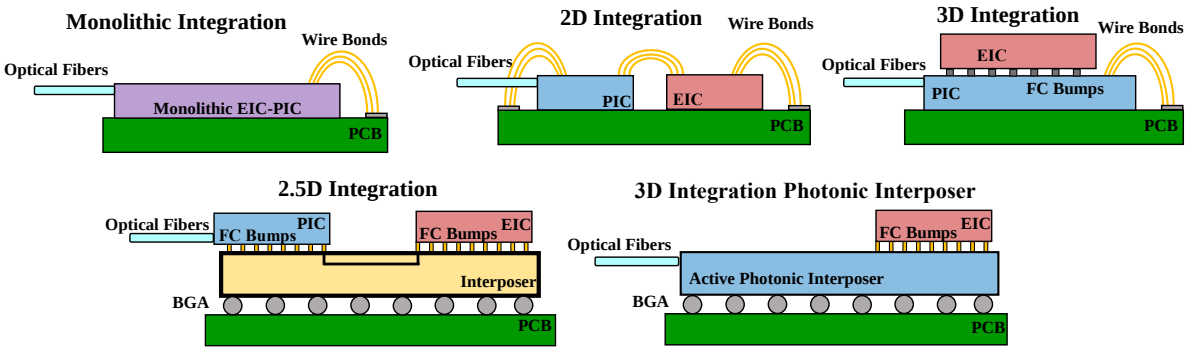

Figure 1.8: The various integration approaches to integrate PICs with driving electronic integrated circuits (EIC). Flip chip (FC) bumps are used to interface between flipped dies and ball grid arrays (BGAs) are used to interface between an interposer and a PCB: monolithic integration, 2D integration, 3D integration, 3D integration with a photonic interposer, and 2.5D integration.

transceiver's I/O to a compute node can be through wirebonds or flip-chipped to an interposer.

While theoretically ideal, in practice monolithic integration uses older CMOS nodes which are not optimized for photonic performance. The most advanced nodes developed for monolithic integration are the 45 nm [71] and 32 nm [72] processes, which still lag in performance compared to the cutting edge FinFET 10 nm and below nodes [73]. Additionally, these monolithic processes suffer from high waveguide loss, low photodiode responsivity, and low photodiode bandwidth—in the 45 nm node these values at 1310 nm are 3.7 dB/cm, 0.5 A/W, and 5 GHz, respectively [72]. Other monolithic processes have demonstrated improved photonic performance at the expense of decreased transistor performance, as they exist in technology nodes between 90 nm and 250 nm [74, 75, 76, 77]. As energy per bit often scales with technology node size, monolithic integration in older CMOS nodes results in greater than 14.5 pJ/b EIC transceiver consumption [75, 76, 78]. The monolithic integrations that use 65 nm nodes and below have sub pJ/b consumption for the EIC drivers [72, 79]. From a practical perspective, the process development cost for monolithic is very expensive, and the resulting technology is less flexible than heterogenous process development. Luxtera initially developed a monolithic transceiver [78], but ultimately switched to hybrid 2.5D integration for the above reasons [80].

1.4.2 2D Integration

On the other end of the integration spectrum is 2D integration. In this approach, the PIC and EIC are placed side by side, typically on a PCB, as shown in Figure 1.8. Wirebonds are used to connect the two dies and to interface to the PCB. An example of this can be seen in [81], where a five channel microring transmitter operating at 25 Gbps per channel PIC was wirebonded to an EIC that provided PRBS generation, differential drivers, and thermal stabilization. The benefit of 2D integration is the ease of packaging; however, the reliance on wirebonds has its drawbacks. While wirebonds can reach pitches of 25 μm [82], the connections between the PIC and EIC are limited to a single edge, severely limiting the aggregate I/O. Additionally, wirebonds introduce a significant parasitic inductance in the typical range of 0.5 – 1.0 nH/mm [83]. Techniques such as ribbon bonding can reduce the parasitic inductance but do so by using ribbons that are over 100 μm wide, placing further limitations on the wirebond pitch. Limiting the I/O to the edge of the EIC also impacts the connection to the compute node, as the remaining edge space must accommodate I/Os to the compute node, grounds, supplies, and bias signals. The two demonstrations outlined in table 1 consume more than 5 pJ/b for the EIC drivers [81, 84], which is an order of magnitude higher than the best 3D integration demonstrations.

1.4.3 3D Integration

Minimizing packaging parasitics between the EIC and PIC makes 3D integration an attractive solution. In 3D integration, the EIC is flip chipped on top of the PIC, as shown in Figure 1.8. Typically, the I/Os to the compute node and DC signals for both the EIC and PIC are routed out through to the edge of the PIC and wirebonded to a PCB. The most common types of flip chip bumps (FC bumps) are copper pillars and microsolder bumps. Copper pillars between PICs and EICs have been demonstrated with parasitic capacitances below 30 fF, parasitic resistances below 1 Ω, and neglible parasitic inductance [85]. Microsolder bumps between PICs and EICs have been demonstrated with parasitic capacitances below 25 fF and parasitic resistances below 1 Ω [86]. Microsolder bumps and copper pillars in transceiver MCMs have achieved similarly

dense pitches—in the range of 40 µm to 50 µm [85, 86, 41]. Microsolder bumps and copper pillars are expected to be able to reach pitches of 20 µm and 10 µm, respectively [87]. For denser pitches, direct bonding Cu-Cu has been demonstrated at 15 µm pitch [87] and is expected to be able to support pitches below 4 µm [88]. When fabricating bumps at these ultra-dense pitches, the most common approach is bump growth at wafer scale. While this is acceptable for transceiver production at large scale, procuring a full wafer can be unfeasible for smaller prototypes utilizing multi-project wafer (MPW) runs. However, there are some vendors offering bare die bumping at dense pitches for solder bumps and copper pillars—35 µm and 25 µm, respectively [89]. The 3D integrated demonstrations exhibit a range of energy consumptions per bit. The energy per bit roughly scales with the EIC technology node. On one end, the 14 nm node EIC transceiver consumes 229 fJ/b [85]; on the other end, the 130 nm node EIC transceiver consumes 11.2 pJ/b [90, 91]. While 3D integration allows for dense pitches and minimal packaging parasitics, it does not provide the best approach for thermal dissipation from the EIC and offers minimal thermal isolation between the EIC and PIC. Heat generated by the flip chip assembled EIC can be transferred to the PIC. Temperature increases for the PIC of 20 °C above ambient temperature have been observed for IC input powers of approximately 0.5 W [92]. This can be especially problematic for thermally sensitive photonic components, such as microrings. Moving beyond lab prototypes can require thermo-electric coolers (TECs) with unique configurations to allow for thermal management [93]. A second potential constraint of 3D integration is the I/O to the compute node, as the most common method of interfacing to the 3D integrated PIC-EIC is through wirebonds to the PIC. This places limitations on the transceiver bandwidth and introduces non-trivial parasitic inductance.

1.4.4 3D Active Interposer Integration

Interposers can be used to combat bandwidth limitations and parasitic inductance. An interposer is a substrate that commonly serves as passive electrical redistribution for active chips that sit on top of the interposer. The interposer's redistribution is commonly for fanning signals out to larger pitches or for enabling connectivity between multiple active chips. The material used to

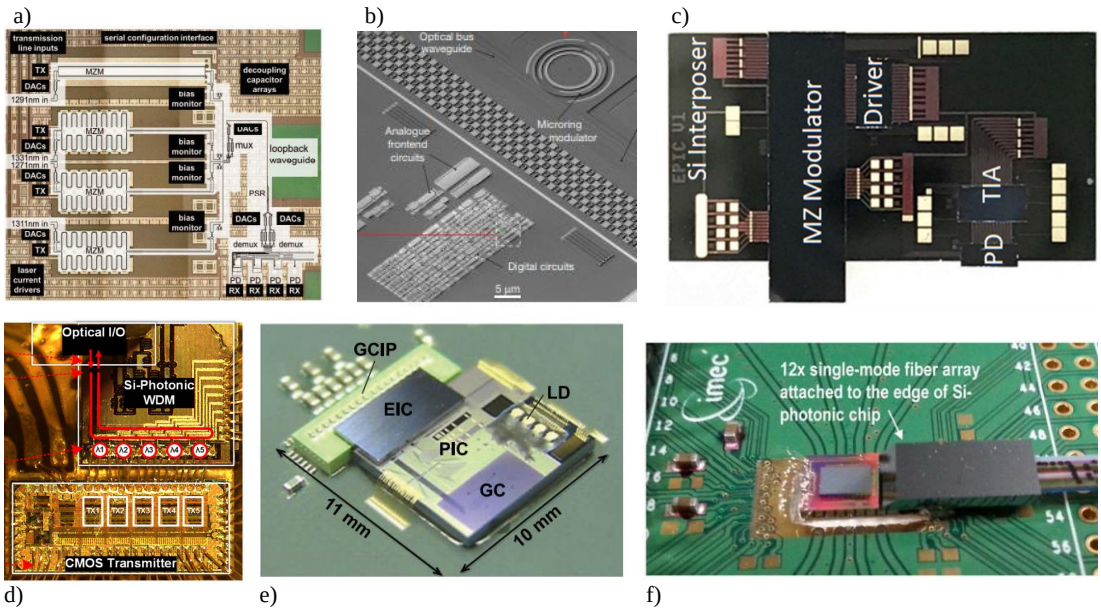

Figure 1.9: Examples of various MCM transceivers. a) Monolithic with MZMs, adopted from [94]. b) Monolithic with MRMs, adopted [79]. c) 2.5D integration with MZMs, adopted from [95]. d) 2D integration with MRMs, adopted from [81]. e) 3D integration with MZMs, adopted from [96]. f) 3D integration with MRMs, adopted from [97].

construct the interposer varies, but common types are silicon, glass, and organic substrates. With silicon interposers, TSVs can be used to enable connectivity between the front and back of the interposer. Passive optical redistribution can also be included in silicon interposers by adding a silicon nitride waveguide layer to route optical signals between photonic chips. Finally, active silicon photonics can be incorporated into silicon interposers to form active photonic interposers to combine the interposer's redistribution functionality with the PIC's functionalities. One specific 3D integration solution utilizing an interposer is to hang the EIC partially off the edge of the PIC, and then use a high-density ceramic glass interposer (CGIP) to interface to the package [95]. A second potential solution is to replace the PIC with an active photonic interposer to enable dense, low-parasitic I/O on both the front and back side of the active photonic interposer [6, 98], as shown in Figure 1.8.

Table 1.1: Notable demonstrations of MCM integrated transceivers, with integration approaches including monolithic, 2D, 3D, and 2.5D.

Integration Approach	EIC-PIC Bump Type	Interposer Type	MCM Interface	Channel Data Rate	Channel Count	Energy per Bit	EIC Node	Modulator Type	Ref
Monolithic	N/A	N/A	-	25 Gbps NRZ (TX, RX)	4	14.6 pJ/b	90 nm	Mach-Zehnder	[76, 94, 99]
Monolithic	N/A	N/A	Wirebonds	10 Gbps NRZ (TX, RX)	4	65.5 pJ/b	130 nm	Mach-Zehnder	[75]
Monolithic	N/A	N/A	Wirebonds	26 Gbps NRZ (TX, RX)	4	16.25 pJ/b	130 nm	Mach-Zehnder	[78]
Monolithic	N/A	N/A	Wirebonds	10, 7 Gbps NRZ (TX, RX)	10	600 fJ/b	65 nm	Microring	[79]
Monolithic	N/A	N/A	-	8 Gbps NRZ (TX, RX)	4	400 fJ/b	45	Microring	[72]
2D	Wirebonds	N/A	Wirebonds	25 Gbps NRZ (TX)	5	5.34 pJ/b	65 nm	Microring	[81]
2D	Wirebonds	N/A	Wirebonds	112 Gbps PAM-4 (TX)	1	6 pJ/b	28 nm	Microring	[84]
3D	Solder Bumps	N/A	Wirebonds	10 Gbps NRZ (TX, RX)	64, 42 (TX, RX)	530 fJ/b	40 nm	Microring	[100]
3D	Cu Pillars	N/A	Wirebonds and Pads	56 Gbps NRZ (TX, RX)	2	11.2 pJ/b	130 nm	Mach-Zehnder	[90, 91]
3D	-	N/A	Wirebonds	20 Gbps NRZ (TX, RX)	4	1.9 pJ/b	40 nm	Microring	[97]
3D	Solder Bumps	N/A	Wirebonds	10 Gbps NRZ (TX,Bumps RX)	8	1.3 pJ/b	40 nm	Microring	[101]
3D	Solder Bumps	N/A	Wirebonds	10 Gbps NRZ (TX, RX)	8	1.37 pJ/b	40 nm	Electro-Absorption	[102]
3D	Solder Bumps	Build-Up Substrate	C4 Bumps	25 Gbps NRZ (TX, RX)	1	4.9 pJ/b	28 nm	Microring	[41]
3D	Cu Pillars	N/A	Wirebonds	25 Gbps NRZ (RX)	1	170 fJ/b	28 nm	N/A	[70]
3D	Cu Pillars	N/A	Wirebonds	50 Gbps PAM-4 (TX, RX)	2	-	-	Mach-Zehnder	[103]
3D	Solder Bumps	Glass Ceramic	Wirebonds and C4 Bumps	25 Gbps NRZ (TX, RX)	16	5.91 pJ/b	28 nm	Mach-Zehnder	[96]
3D	Cu Pillars	N/A	Wirebonds and Pads	40 Gbps NRZ (TX, RX)	4, 1 (TX, RX)	229 fJ/b	14 nm	Microring	[85]
3D Photonic Interposer	Solder Bumps	Silicon	Cu Pillars	40 Gbps NRZ (TX, RX)	12	4.4 pJ/b	-	VCSELs	[104]
2.5D	-	LTCC Substrate	BGA	200 Gbps 16-QAM (TX, RX)	1	-	-	Mach-Zehnder	[98]
2.5D	Cu Pillars	Silicon	Wirebonds	50 Gbps NRZ (TX, RX)	4	-	-	Mach-Zehnder	[95]
2.5D	Cu Pillars	Ceramic	BGA	272 Gbps DP 16-QAM (TX, RX)	1	-	-	Mach-Zehnder	[105]
2.5D	Solder Bumps	Silicon	BGA	[Target] 10 Gbps NRZ (TX, RX)	4	-	-	Microdisk	This work

1.4.5 2.5D Integration

Active photonic interposers are an ideal combination of heterogenous process optimization, low EIC-PIC packaging parasitics, and high I/O bandwidth to a compute node. However, they are still a relatively recent technology, and as a result come with high process development costs and long fabrication timelines. A compromise is 2.5D integration, where both the EIC and PIC are flip chipped onto a passive interposer with TSVs to interface to the back side, as shown in Figure 1.8. The interposer can be electrical only, or also include a waveguide layer for optical redistribution. The flip-chipping can be achieved with micro solder bumps or copper pillars with the same pitch and parasitics as with 3D integration. If the compute node die is flipped onto the same interposer, the I/O connections can be made with micro solder bumps or copper pillars. A drawback of 2.5D integration is that the parasitics between the EIC and PIC are higher than 3D integration as critical signals must pass through two bump interfaces and a trace on an interposer. However, this additional source of parasitics can still be manageable, as dies on an interposer can be placed several hundred micrometers apart. For longer connections to the compute node, high quality transmission lines can be developed within silicon interposers, with 8 mm long coplanar waveguides transmission lines demonstrating better than 50 GHz bandwidth with less than 2 dB S21 loss [95]. If the compute node is housed in a larger package, connections from the back of the transceiver's interposer can be made to a PCB with a ball grid array (BGA) [98, 105], as shown in Figure 1.7. Standard BGA packages can be developed with pitches as low as 0.5 mm [106], with limitations a result of PCB spacing and routing. PIC integration to a PCB through a BGA package has demonstrated signal paths with better than 3 dB insertion loss with a bandwidth of 40 GHz [107]. The 2.5D demonstrations did not report energy per bit metrics. For our first iteration of prototypes, we elected to use a 2.5D integration approach to provide a balance of performance with cost and fabrication turnaround.

1.5 Scope of Dissertation

The work in this dissertation is centered around developing MCM silicon photonic transceivers for their insertion into high performance datacommunication interconnects. The dissertation is composed of two sections. The first section focuses on the architecture, design, integration, and characterization of a number of different silicon photonic MCM transceivers, and spans chapters 2 through 4. The second section focuses on research that aids in the development of silicon photonic transceivers, and spans chapters 5 through 7.

In chapter 2, we focus on our version 1 MCM silicon photonic transceiver–a wavelength division multiplexed (WDM) microdisk based, 2.5D integrated, MCM transceiver. We present the high-level architecture, the specifics of the PIC and EIC, the bare die PIC performance, and the transceiver performance. In chapter 3, we present the key design considerations that were identified during the development of our version 1 prototype and apply those design considerations to the development of our second generation prototypes. These design considerations are: integration approach, photonic equivalent circuit model, PIC to EIC interface model, MCM data I/O model, and design for assembly. In chapter 4, we overview additional MCM transceiver prototypes are either in progress or had to be terminated due to a variety of issues. These prototypes include a design developed in parallel with our version 1 prototype with different EICs, a 3D integrated active interposer network on chip, and our second generation prototypes with custom EICs.

In chapter 5, we present on our development of custom silicon photonic microresonator modulators. This research supports the development of MCM transceivers by allowing the transceiver design to expand beyond utilizing PDK components. The iterations of custom modulators include microdisk, racetrack, and coupling modulators. In chapter 6, we focus on research for higher order modulation formats implemented with silicon photonics. This research provides another avenue for scaling up the MCM transceiver design to higher total throughput. The transmitters include a self optimizing MZM PAM-4 modulator, arbitrary QAM signals utilizing microring modulators, and microdisk based QAM-16 and PM-WDM-QPSK transmitters. In chapter 7, we overview a variety

of research projects that contribute to silicon photonic transceivers, including the development of graphene modulator interconnects, testing strategies for high volume bandwidth characterization, an approach for optical deserialization, and the analysis of thermal crosstalk in microdisk modulators as a function of modulator spacing. Finally, we provide conclusions and recommendations for future work in chapter 8.

Part I

Silicon Photonic Multi Chip Module Transceivers

Chapter 2: Silicon Photonic 2.5D Integrated Transceiver

In this chapter, we present the research on the first prototype of our work toward developing silicon photonic transceivers. At a high level, the transceiver is a 2.5D integrated multi-chip module (MCM) for 4-channel wavelength division multiplexed (WDM) microdisk modulation targeting 10 Gbps per channel. A silicon interposer is used to provide connectivity between the photonic integrated circuit (PIC) and the commercial transimpedance amplifiers (TIAs). The chapter first presents the architecture of the prototype in terms of photonics, electronics, and integration. Next, the performance of the transceiver is presented, both for the transmitter and the receiver. The debugging and repackaging necessary to fix a fabrication issue on the receiver portion of the transceiver is presented. Finally, the chapter presents the energy consumption of an interconnect built upon this transceiver and discusses the scalability of the transceiver.

2.1 Transceiver Architecture

In this section, we overview the transceiver architecture used for the first prototype of our silicon photonic MCM transceiver, including the photonic architecture, the electronic driver architecture, and the integration architecture.

2.1.1 Photonic Architecture

The silicon photonic transceiver architecture, for both transmitter and receiver, is built on bus waveguides with microdisk elements coupled to the waveguide, as shown in Figure 2.1. The photonic integrated circuit was fabricated at AIM Photonics on an multi project wafer (MPW) using the AIM process design kit (PDK) components. On the transmit side, four microdisk modulators are coupled to the bus waveguide. The modulators were measured to be evenly spaced across a 25

nm free spectral range (FSR), resulting in channel spacings of approximately 6.25 nm. A 99-1 tap is positioned after each modulator, with the 99% output continuing on the bus waveguide. The 1% output leads to a monitor photodiode, which allows for feedback signals for thermal stabilization of the microdisk modulators. The difference between the monitor photodiode before and after a modulator corresponds to the power coupled into that modulator. Thermal stabilization architectures have been demonstrated with a single monitor photodiode at the end of a bus of microring modulators, but they typically require measuring RF power [108] or dithering [81]. Other thermal stabilization architectures require a drop port on the modulator [109, 110], reducing the Q factor of the ring. Using a more direct measurement of the power coupled into the modulator, without requiring a drop port, allows for a simpler implementation of the feedback. The bus waveguide is routed to edge couplers at a 127 μm pitch to allow for coupling to a standard zero polish fiber array. On the receive side, four microdisk demux filters are coupled to the bus waveguide. The resonances are fabricated to match the four transmit resonances. At the drop port of each demux filter is a high-speed photodetector. The end of the bus waveguide is split with a 50-50 tap: one end is routed to a monitor photodiode and the other end is routed to the edge coupler array. The thermal stabilization feedback signal is simpler on the receive side for two reasons. One, the output of the high-speed photodetectors can be used as the feedback signal to thermally stabilize the data dropped by the demux microdisks. Two, the optimal operating condition is directly on resonance, unlike the transmit side.

The goal for this iteration of prototypes was to provide a highly scalable, ultralow energy consumption, and very dense bandwidth platform that future prototypes could build on. For this reason, the target data rate for each channel is 10 Gbps. The microdisk modulator occupies approximately 250 μm^2 and the combination of the microdisk demux and high-speed photodiode occupies approximately 750 μm^2. The small microdisk footprint allows transceivers to designed very densely and to still achieve system data rates in the Tbps regime [85]. Additionally, microdisk modulators have lower device capacitances and typically require smaller swing voltages compared to Mach Zehnder modulators (MZMs) [111], allowing the microdisk modulators to consume less

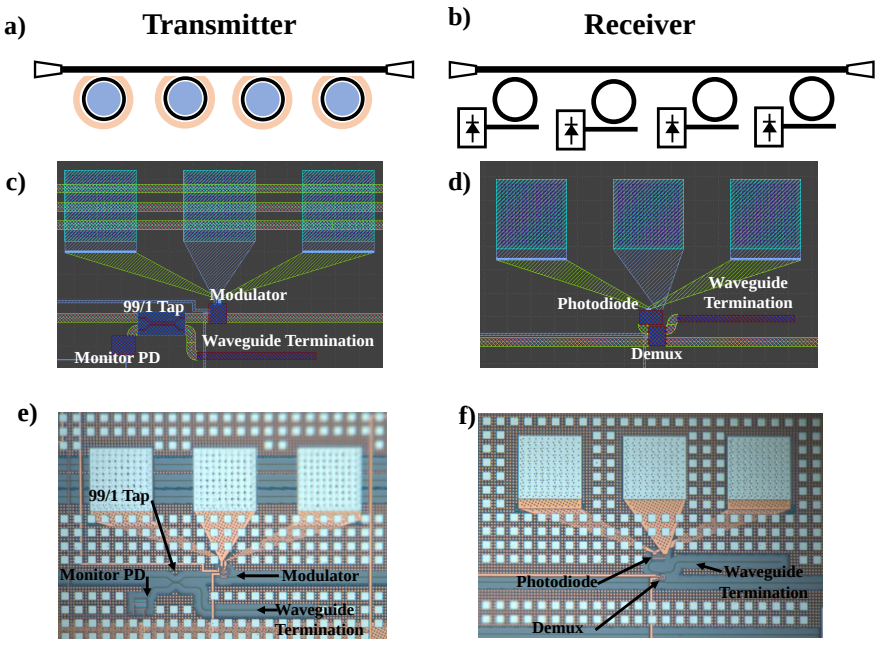

Figure 2.1: The architecture of the transceiver. (a) Schematic of the transmitter. (b) Schematic of the receiver. (c) Layout of one channel of the transmitter. (d) Layout of one channel of the receiver. (d) Image of one channel of the fabricated transmitter. (e) Image of one channel of the fabricated receiver.

modulation power. To fully compare the MZM and microdisk modulators, the thermal power consumption for tuning the microdisks must be considered. In [72], the thermal tuning control logic contributed 18 fJ/b of the total 700 fJ/b for the EIC. The energy consumption for microdisk heaters is very dependent on link design and the fabrication variability of microdisks. Thermal tuning energy per bit is dependent on data rate because the thermal tuning power is independent of rate, so higher data rates will reduce the energy per bit. If the laser wavelengths are fixed, then the burden of accounting for resonance fabrication variability is placed on microdisk's thermal heaters. The standard deviation for the microdisk's resonance is 2.14 nm [112]. If the thermal heaters are to account for this variation, the operating wavelength must be set above the expected resonance because the heaters can only tune the microdisk in one direction. Ensuring that 95% of the fabricated resonances fall below the operating wavelength requires an operating wavelength 3.5 nm above intended fabricated resonance. Using the same thermal tuning efficiency and channel rate as [72] results in an average expected heater energy per bit of approximately 186 fJ/b. Paths towards

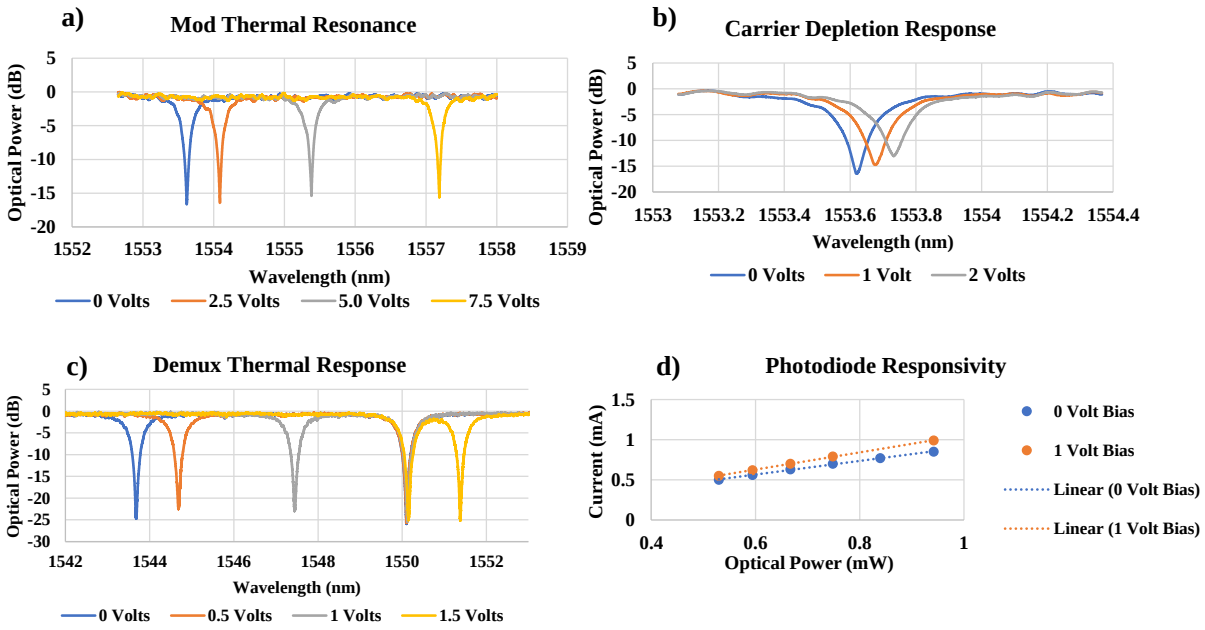

Figure 2.2: The DC performance of the bare die PIC. (a) The resonance response of the microdisk modulator's heater. (b) The resonance response of the depletion modulator. (c) The resonance response of the demultiplexer microdisk's heater. (d) The responsivity of the photodiode.

reducing the heater energy per bit are operating at higher data rates, developing more efficient heaters, and reducing the fabrication variability.

The DC response for the modulator's heater can be seen in Figure 2.2a. The heater was tested up to 7.5 volts, which produced over a 3.5 nm shift in the microdisk's resonance. The heater efficiency for these modulators was extracted to be 0.54 ± 0.05 nm/mW. These measurements allowed additional parameters to be extracted: the FSR was 24.3 nm, the full width at half maximum (FWHM) was 0.18 nm, and the extinction ratio (ER) was 12 dB. The DC response of the depletion modulator can be seen in Figure 2.2b. A voltage range of 0 to 2 volts was applied to the depletion modulator. From the response, the modulator efficiency was extracted to be 62 ± 2 pm/V. As the reverse bias voltage is increased, the ER of the ring decreased, demonstrating that the microdisk was overcoupled.

The eye diagram of the microdisk modulator can be seen in Figure 2.3a. The eye diagram at 10 Gbps was recorded with a drive voltage of 1.5 V_{PP} biased at -0.5 volts. The measurements for the modulator's bandwidth and the bit error rate curve can be seen in Figure 2.3b and 2.3c, respectively.

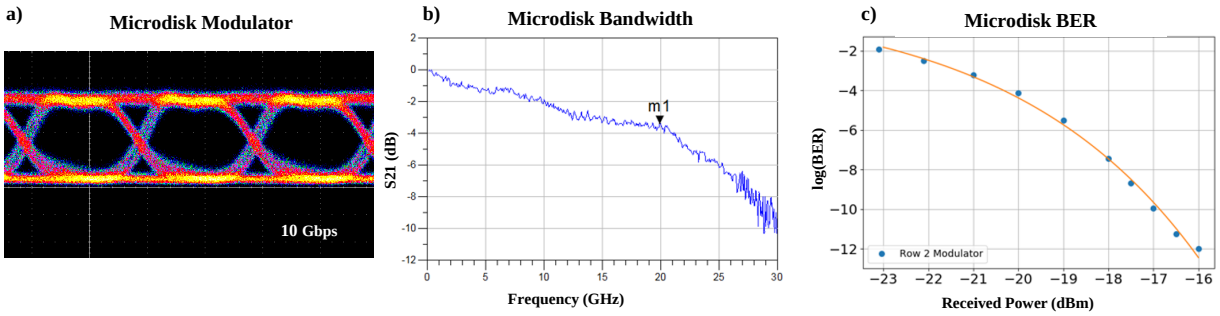

Figure 2.3: The microdisk modulator's AC performance. (a) The eye diagram at 10 Gbps driven with a 1.5 V_{PP} signal. (b) The bandwidth of the modulator. (c) The BER at 10 Gbps driven with a 1.5 V_{PP} signal.

From these measurements, the modulator produces an error free rate (10^{-12}) at a received power of -16.0 dBm using a commercial receiver. The bandwidth was measured to be 20 GHz. The demux filter's through response can be seen in Figure 2.2c. From the response, the heater's efficiency was extracted to be 0.66 ± 0.03 nm/mW. From this resonance response, static parameters can be extracted: the filter's FSR was 25.1 nm, the filter's FWHM was 0.54 nm, the filter's ER was 24 dB. The photodiodes at the drop port of the demux filter are designed to be operated with 1 volt of reverse bias. The measured DC photodiode response can be seen in Figure 2.2d. The input power was varied and the output current from the photodiode was measured. This was done with 0 volts and 1 volt reverse bias. Higher voltages were tested, but there was minimal difference from the 1 volt reverse bias. The photodiode responsivity was 0.94 A/W when the photodiode was biased at 0 volts. The photodiode responsivity was 1.11 A/W when the photodiode was reverse biased at 1 volt.

2.1.2 Electronic Architecture

For the first iteration of prototypes, the transceiver design used a commercial Texas Instruments ONET8551 TIA. The driver featured a TIA, voltage amplifier, and output buffer. The TIA was designed for wirebonds, but the pad pitch is 115 µm and the aluminum terminated pads were ideal candidates for stud bumps, making flip chipping feasible. While the TIA was single channel, its small size (870 µm by 1036 µm) made it possible to place four dies to interface to the four received

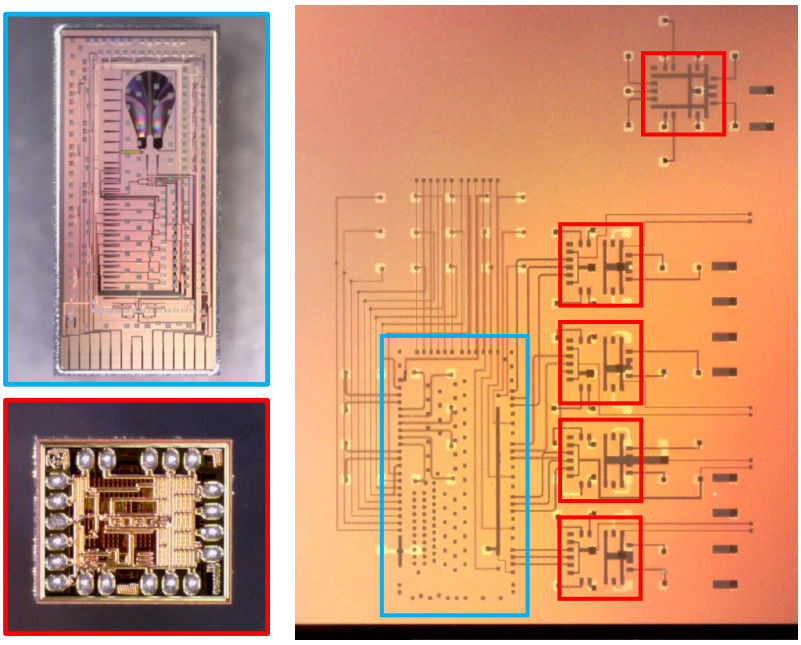

Figure 2.4: The PIC, EIC, and interposer used in the transceiver prior to assembly. The interposer is shown on the right. The PIC and its bonding location on the interposer are shown in blue. The EIC and its bonding locations on the interposer are shown in red.

channels on the PIC, as shown in Figure 2.4. The PIC is shown in blue and the EICs are shown in red. The 9 GHz bandwidth was designed for a maximum data rate of 11.3 Gbps, which matched with the target photonic rate of 10 Gbps. The TIA had a sensitivity of -20 dBm and differential outputs. A single V_{CC} of +3.3 V was able to be used to power both the input stage for the TIA and the output stage for the voltage amplifier and buffer. The EIC consumed 9.2 pJ/b when receiving a 10 Gbps signal. The EIC also featured Received Signal Strength Indicators (RSSIs) that were connected to ground via surface mount resistors on the printed circuit board (PCB) to translate to a voltage indicator signal. An additional test TIA was placed on the same interposer, designed to receive external input signals from SubMiniature version A connectors (SMAs) on the PCB for debugging purposes. For this prototype, the microdisk modulators on the PIC were externally driven as we were unable to procure an appropriate commercial bare die modulator driver that had a pad configuration conducive to flip chipping. Future prototypes, discussed in Chapter 4, will feature separate custom TX and RX EIC drivers flip chipped onto the interposer.

2.1.3 Integration Architecture

The integration approach for the prototype was a 2.5D integrated MCM. The 2.5D integration was achieved with a silicon interposer. The silicon interposer had TSVs to provide a connection between the metal layers on the front side and the back side of the interposer. An interposer wafer can be seen in Figure 2.5. Both the PIC and EICs were flipped on top of the interposer, as shown in Figure 2.6. The backside of the interposer was used to connect to a PCB to fan out the signals and to house decoupling capacitors and resistors for the RSSIs. Assembly of the prototype was done at the Tyndall National Institute. The flip chip connections for both the PIC and EIC to the interposer was done using stud bumps at a minimum of 100 µm pitch. Stud bumps are gold wire bond segments that are bonded to aluminum pads on the PIC, EIC, and interposer. The initial wirebond can be attached to the aluminum pads and serves as a pillar that the solder can adhere to. Ball grid array (BGA) connections on 300 µm pads were used to connect the backside of the interposer to the PCB with electroless nickel electroless palladium immersion gold (ENEPIG) finish at 500 µm pitch. The PIC and EICs were connected to the interposer via stud-bumps prior to attaching the interposer to the PCB, so the reflow temperature of the BGA-type solder must be below the reflow temperature of the stud bump solder. The PIC was positioned such that it hanged off the interposer by 200 µm to allow for a clear interface to the edge couplers and to provide a visual sight of the edge couplers to aid alignment.

The fabricated PIC was 4.15 mm by 1.87 mm, and the photodiodes are evenly spaced out at a 0.75 mm pitch along the edge of a 4.15 mm. The spacing between the TIAs and between the TIA and PIC was 0.5 mm. As a result, the TIAs were not able to be placed directly in line with the photodiodes on the PIC. The top-level aluminum trace between the photodiode and the TIA input was 30 µm wide and ranges from 0.75 mm to 2.6 mm long. Each photodiode to TIA input connection was a cathode-anode-cathode configuration, and the TIA provided a 2.35 V reverse bias to the photodiode. The trace configuration and interposer stack-up yielded an approximate effective relative permittivity of 2. As a result, a 10 GHz signal yielded a $\lambda/4$ length of 3.75 mm. This meant that even the longest trace length could be treated as a lumped element, meaning that

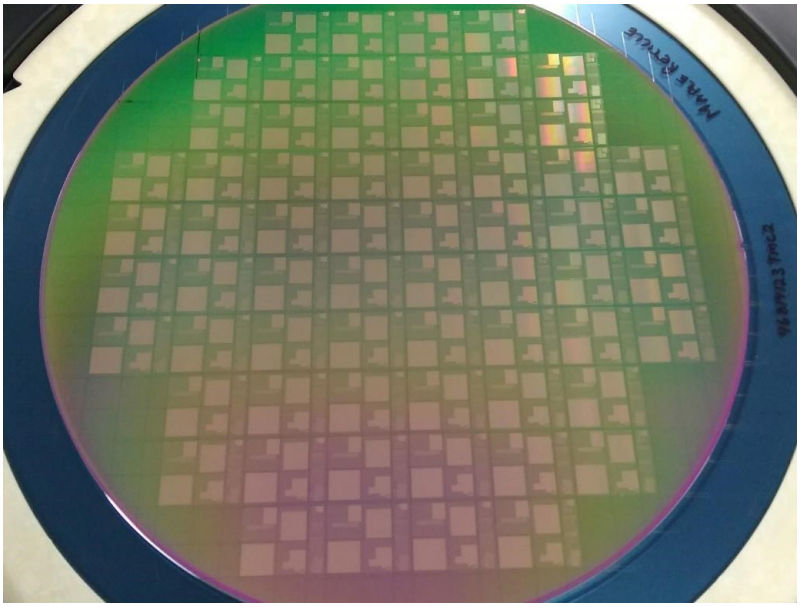

Figure 2.5: The interposer wafer on which the interposer chiplets used in the transceiver were fabricated.

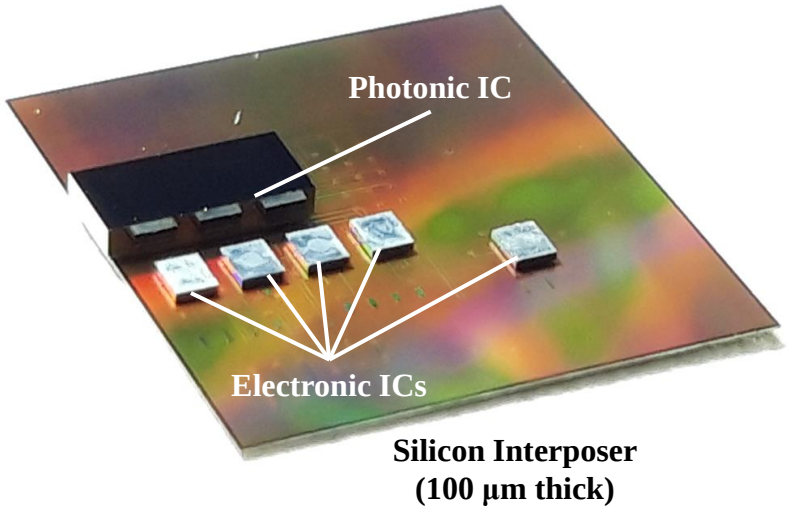

Figure 2.6: The assembled MCM showing the silicon interposer, which provides connectivity between the four TIA EICs and the PIC. The isolated EIC is not connected to the PIC and used for TIA-only tests.

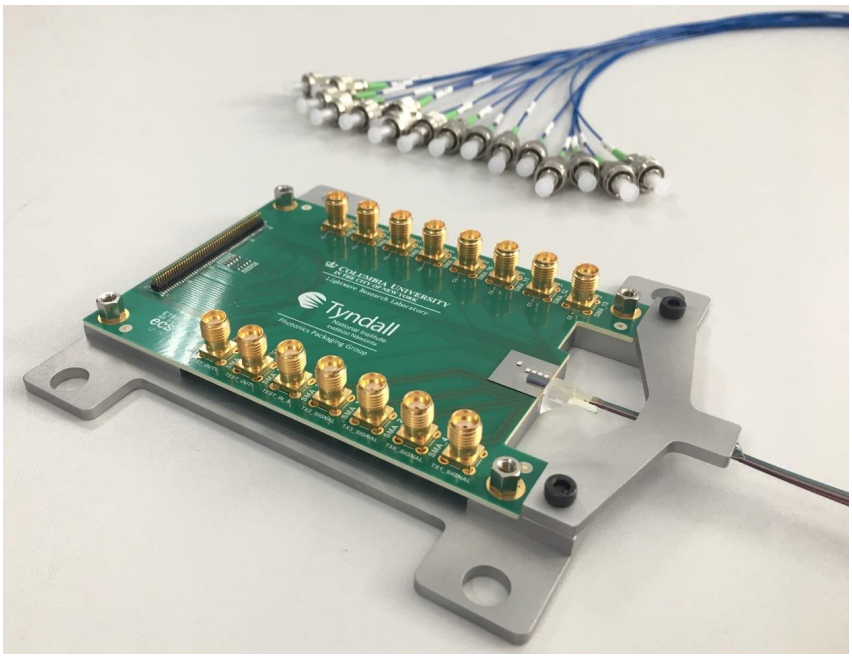

Figure 2.7: The fully packaged MCM 2.5D integrated transceiver. The interposer sits on a fan out PCB, which sits on a mechanical substrate that mounts to an optical table for testing. The optical fiber array couples to the PIC and connects to the mechanical support in several locations.

reflections from impedance mismatch should not impact performance.

All electrical signals-—DC and RF signals for the PIC and EIC—-were routed to the back of the interposer through the TSVs to BGA-type connections. The RF signals used coplanar waveguide and microstrip transmission lines on the PCB to fan out to SMAs. The DC signals connected to a dense DC mezzanine to interface to a second DC fanout board. All optical connections on the PIC routed to edge couplers at a 127 µm pitch. The overhanging PIC was coupled with a standard flat polish fiber array, which was connected to the prototype's mechanical substrate.

2.2 Transceiver Performance

In this section, the performance of the assembled prototype is presented. Initial coupling losses were measured to be approximately 5 dB per facet. The DC responses of the heaters for the TX and RX were characterized, as well as the DC response of the PN depletion modulator—these can be seen in Fig. 8. The heater efficiency was extracted to be 0.49 ± 0.01 nm/mW. The RX heater

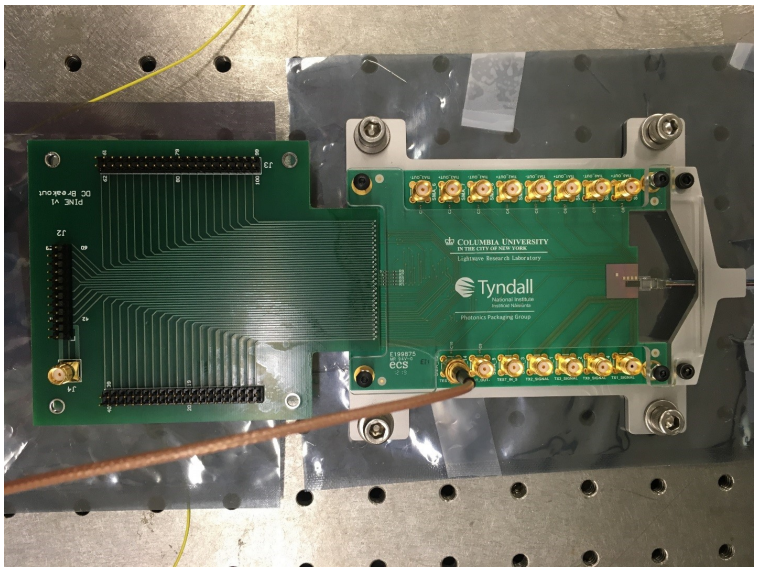

Figure 2.8: The fully packaged transceiver as seen from above, which the additional breakout board mounted on the back of the main PCB.

response was used to extract the demux heater efficiency, which was determined to be 0.71 ± 0.10 nm/mW. The energy per bit for thermally tuning the microdisks will be dependent on the resonance shift required. If the required resonance shift is 2.14 nm—-the standard deviation in the fabricated microdisk resonance reported in [112]-—then at 10 Gbps the heaters will consume 437 fJ/b and 301 fJ/b for the modulator and demux, respectively. The modulation efficiency was extracted to be 60 ± 3 pm/V.

The bandwidth response of the four TX channels of the prototype can be seen in Figure 2.10b. While the response of the four channels were in good agreement, a significant drop in the bandwidth occurs at 8.5 GHz. We are currently investigating to determine the exact cause of the bandwidth limitation. The two most likely culprits are impedance mismatch (which would be resolved when the modulator driver is integrated near the microdisk modulator) and electrical resonance from a combination of interposer trace parasitics and packaging parasitics. The interposer design for the connection to the microdisk modulators was not impedance controlled, as the main concern was keeping the trace length below $\lambda/4$ at 10 GHz. Subsequent prototypes were designed with 50-ohm transmission lines connecting to the RF I/Os of the EIC. Additionally, subsequent designs have data generation occurring within the TX EIC, and deserialization occurring within the RX

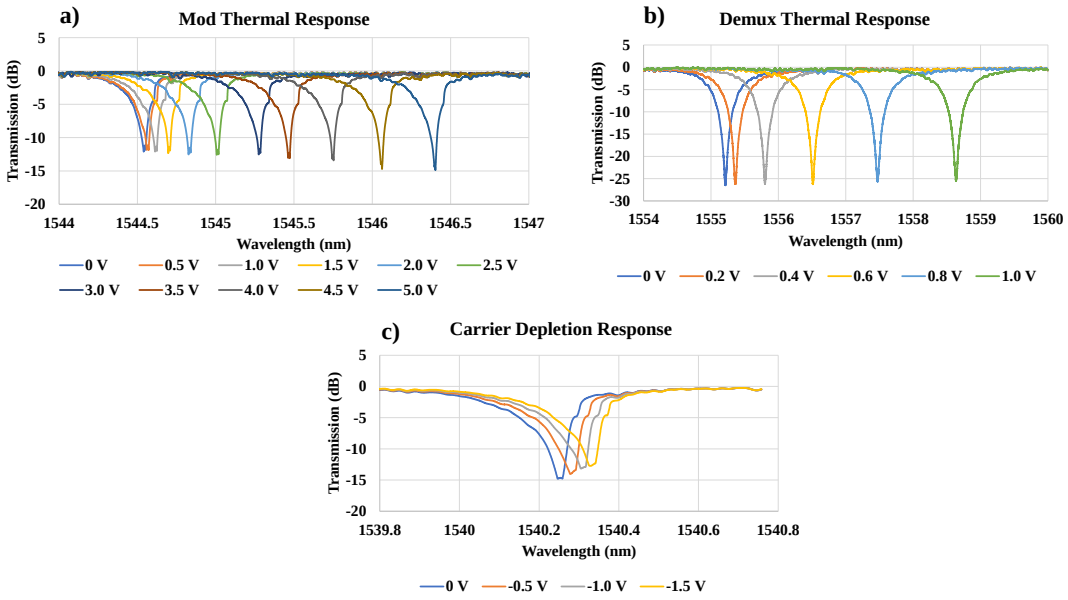

Figure 2.9: The DC performance of the PIC components of the MCM integrated transceiver. (a) The resonance response of the microdisk modulator's heater. (b) The resonance response of the demultiplexer microdisk's heater. (c) The resonance response of the depletion modulator.

EIC to bring a 10 Gbps data rate down to 2.5 Gbps, which is supported by this prototype's bandwidth. The bit error rates (BERs) for various data rates can be seen in Figure 2.10c. For data rates of 6 Gbps and below, error free performance was achievable at -15 dBm received power or better. Data rates at or above the electrical bandwidth degradation produced significantly worse BERs.

Prior to testing the receiver's performance, we verified the functionality of the test TIA flipped onto the interposer. A small current supply was approximated by placing a voltage signal in series with a 22 kΩ resistor to provide a Thevenin equivalent of a µA current supply. For this test, alligator clips were used to clip to the resistor, which degraded the bandwidth and added noise to the test. A 400 MHz square wave signal was varied from 0.05 V_{PP} to 1.1 V_{PP} to replicate a current source of 7 μA_{PP} to 50 μA_{PP}. We see that with a current source of 14 μA_{PP}, the output was a clean 0.16 V_{PP} square wave. At current swings below 14 μA_{PP}, the signal was severely degraded, as seen in Figure 2.11. Increasing the current source's swing beyond this threshold did not impact the output voltage, as the EIC has a limiting amplifier in the output portion of the driver. The TIA was expected to exhibit a sensitivity of -20 dBm. With a 1 A/W photodiode, this would correspond to

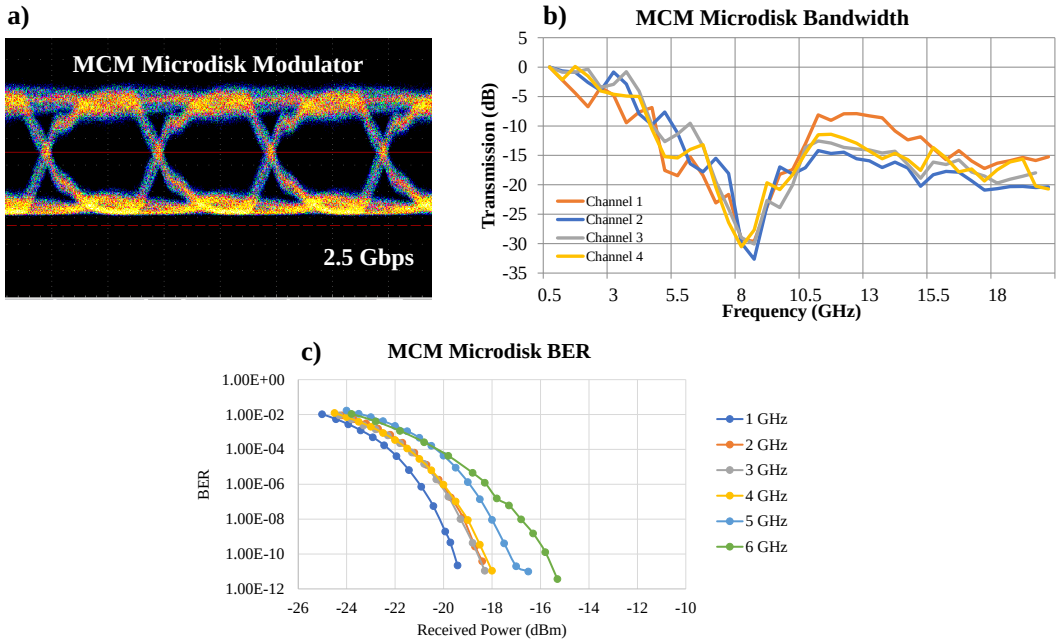

Figure 2.10: The microdisk modulator's AC performance of the PIC components of the MCM integrated transceiver. (a) The eye diagram at 2.5 Gbps driven with a 1.5 V_{PP} signal. (b) The bandwidth of the microdisk modulators of the four channels. (c) The BER driven with a 1.5 V_{PP} signal at different data rates.

an input current swing of 10 μA_{PP}, which is in relative agreement with the results observed from the test TIA. During the initial characterization of the receiver portion, it was discovered that the PDK component photodiodes were fabricated with the anode and cathode flipped, which resulted in the TIAs providing a forward bias to the photodiodes, which destroyed them. We repackaged an additional prototype with the PIC offset by one pad pitch: 100 µm. This reduced the functionality of the prototype and removed the ability to thermally tune some channels. However, as the signal configuration was intended to be cathode-anode-cathode, this offset provided the correct polarity between the TIAs and the photodiodes.

The bandwidths for the four RX channels can be seen in Figure 2.13a. The bandwidth was measured by modulating an external MZM with a sine wave source. For each channel, a tunable laser was set to the appropriate microdisk demux's resonance, and the sine wave source was swept from DC to 20 GHz. The output of the TIA was sent to an electrical spectrum analyzer to measure the received tone's power and were normalized with the bandwidths of the cables and modulator.

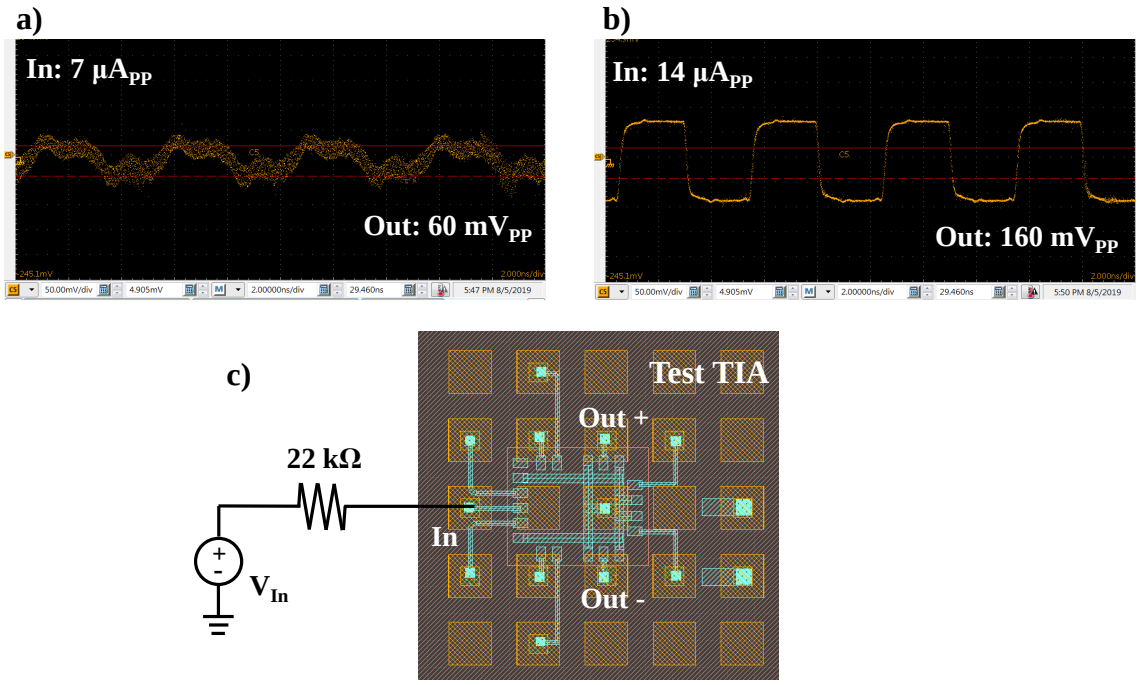

Figure 2.11: The results of the test TIA of the MCM prototype. (a) the test setup to mimic a small swing input current. (b) The signal from Out+ when driven with the equivalent of a 7 μA_{PP} input signal. (c) The signal from Out+ when driven with the equivalent of a 14 μA_{PP} input signal.

The measured bandwidths suggested an electrical resonance in the assembled receiver prototype at 7.5 GHz. Additionally, channel 1 was about 20 dB below the other channels, suggesting that there might have been a partial connection in one of the stud bumps or BGA bumps. The BERs for channel 3 can be seen in Figure 2.13b. The BERs were measured by modulating the external MZM with pseudo random binary sequence (PRBS) 2^{15}-1 data from a pulse pattern generator (PPG). The external laser was set to be dropped by the microdisk demux's resonance, and the output of the TIA was sent to a bit error rate tester. The input power into the prototype was varied with an external variable optical attenuator. The optical power into the prototype was measured, and the received power was calculated by subtracting the combined 7.4 dB optical loss from the edge coupler and demux microdisk. Error free performance (10^{-9}) was achieved at 5 Gbps with -10.5 dBm received power.

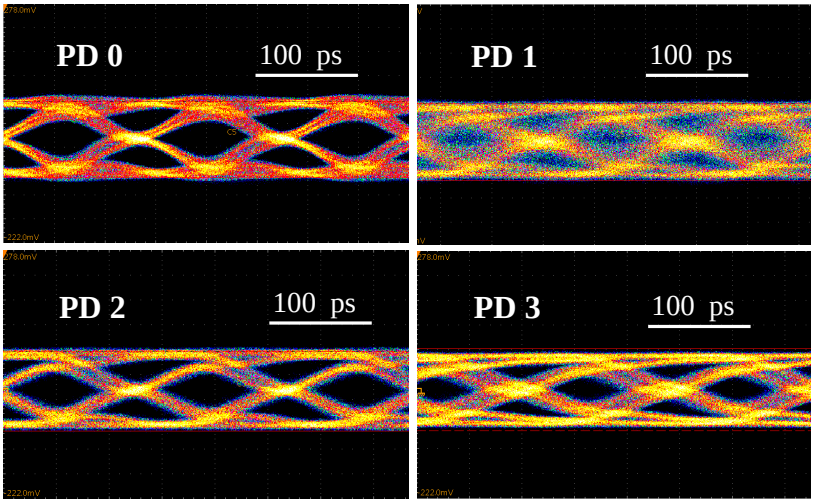

Figure 2.12: The eye diagrams for the outputs of the four receiver channels at 7 Gbps. As shown in the PD1 image, there is a degradation in quality, likely due to a bump issue.

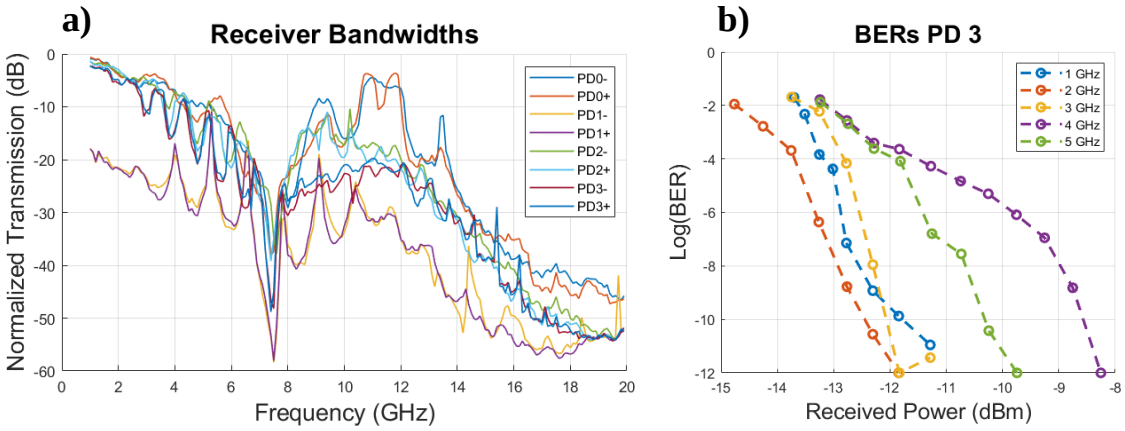

Figure 2.13: a) The bandwidths for the both the positive and negative outputs of the four receiver channels. b) The BERs at different data rates for a single channel of the receiver prototype.

2.3 Energy Analysis

To analyze the total energy consumption for an interconnect built upon the MCM transceiver, we must first identify all the individual energy consumption components. These components can be separated into laser consumption, PIC consumption, and EIC consumption.

2.3.1 Component Energy Consumption

The explicit energy consumption for the laser is the required laser launch power divided by the wallplug efficiency of the laser. This value implicitly depends on the receiver's optical sensitivity and the total optical losses throughout the interconnect. For the MCM transceiver, the receiver achieved error free performance (BER of 10^{-9}) at -4.6 dBm received optical power when measured from the fiber into the receiver portion with a high-quality commercial modulator [6]. Accounting for the receiver edge coupler loss, demux through loss, demux insertion loss, and demux power penalties puts the error free performance to approximately -12 dBm received power when measured at the photodiode. The total optical loss for the passive components on the transmitter side was 12.9 dB. This was due to 5.0 dB of loss for each of the two edge couplers, 1.6 dB of loss for 8 mm of waveguide within the transmitter, and 1.3 dB of loss for insertion loss of the four modulators. Additional modulator power penalties were calculated using the approach in [113] to account for the finite extinction ratio and the on off keyed (OOK) modulation format. Using the measured modulation extinction ratio of 9.7 dB [85], this results in a modulator power penalty of 4.2 dB. Working from the -4.6 dBm receiver sensitivity (measured prior to the bonded fiber array) and incorporating the transmitter insertion losses and power penalties results in a 12.5 dBm required laser launch power. As this MCM transceiver is intended to scale to higher total throughputs by scaling to large numbers of WDM channels, it is best suited to utilizing a comb laser. For microresonator-based combs, the overall efficiency is the product of the pump's wallplug efficiency and the pump to comb conversion efficiency. For this analysis, the pump wallplug efficiency will be taken to be 45% [114] and the pump to comb conversion efficiency will be taken to be 40%

[115], for an effective comb wallplug efficiency of 18%. This corresponds to a power consumption of 98.8 mW for the required 12.5 dBm channel launch power.

The PIC's power consumption is dominated by thermal tuning of the microdisk modulators and demuxes. The dynamic consumption of the modulator must also be considered. The energy consumption for the heaters will be dependent on the heater tuning efficiencies and the required resonance shifts. The heater efficiency for the modulator was extracted to be 0.49 nm/mW and the heater efficiency for the demux was extracted to be 0.71 nm/mW [116]. For this analysis, the required static resonance shift is taken to be 2.14 nm, as this was the measured standard deviation for the modulator's fabricated resonances [116]. Combining these measurements yields a 4.37 mW power consumption for the modulator and 2.93 mW power consumption for the demux. The dynamic power consumption for the modulator can be calculated as $\frac{fCV^2}{4}$, where f is the data rate, V is the modulator drive voltage and C is the sum of the junction capacitance and parasitic capacitance. The equation is $\frac{1}{4}$ rather than $\frac{1}{2}$ because the on-off keyed PRBS signal is only expected to require a transition for half the pattern on average. The microdisk modulator was driven with a 1.5 V_{PP} voltage and the capacitance sum was measured to be 233 fF [117], which yields a power consumption of 1.31 mW at 10 GHz. Combined, the PIC consumes 8.61 mW.

The TI TIA used for the MCM transceiver is expected to consume 28 mA between the input and output stages when powered with a 3.3 V supply voltage. The average current draw for the four receiver channels in the MCM prototype was 30.8 mA. The resulting EIC power consumption is 101.7 mW.

2.3.2 Interconnect Energy Consumption

The total power consumption from the laser, PIC, and EIC is 209.1 mW. At the target channel rate of 10 Gbps, the energy per bit is 20.91 pJ/b. The energy per bit is dominated by the EIC and the laser, as shown in Figure 2.14a. This energy breakdown is encouraging for a first prototype, as the dominating sources of energy consumption present clear paths towards reduction. Customized EICs designed for lower energy consumption have been demonstrated with an order of magnitude

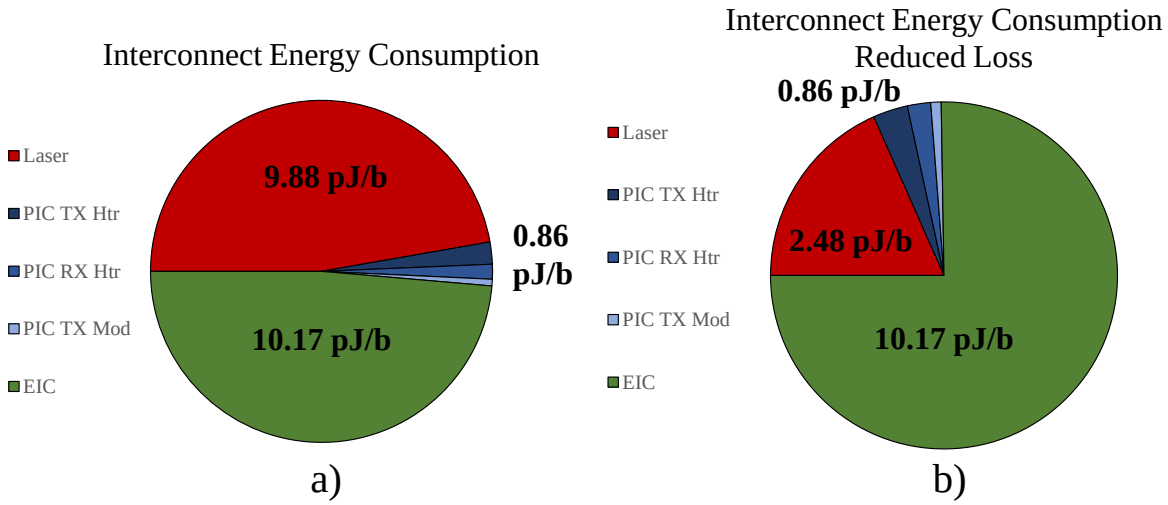

Figure 2.14: The energy consumption breakdown for an interconnect based on the MCM transceiver. a) shows the energy consumption of an interconnect of the current transceiver prototype and b) shows the energy consumption of an interconnect of the current transceiver prototype if it were repackaged to reduce insertion loss.

lower consumption, especially as the EIC node is advanced to 40 nm and below [118]. The laser's energy consumption is largely due to the high sources of optical loss, particularly the insertion loss between the fiber array and the edge coupler. While this prototype had 5 dB of loss per bonded edge coupler, edge couplers have been demonstrated with approximately 0.25 dB of insertion loss [119], presenting a clear path for reducing the interconnect's insertion loss, which plays a large role in dictating the laser's energy consumption for the interconnect.

The total power consumption of an interconnect based on these components can be easily improved through repackaging the MCM transceiver, as shown in Figure 2.14b. The PIC used in the transceiver has been coupled with 3 dB of insertion loss with non-bonded edge couplers. The decrease in edge coupler insertion loss will result in a total passive optical loss of 6.9 dB for the interconnect. Using the same receiver sensitivity (measured prior to the fiber array) and incorporating the reduced total passive losses and power penalties results in a 6.5 dBm required laser launch power. With the same effective comb wallplug efficiency of 18% results in a laser power consumption of 24.8 mW for the 6.5 dBm channel launch power. Assuming no improvement in the EIC or PIC power consumption results in a total power consumption of 135.2 mW. At the

target channel rate of 10 Gbps, the energy per bit is 13.51 pJ/b.

2.4 Scaling to Higher Transceiver Throughput

2.4.1 Increasing Channel Data Rates

Two main approaches for scaling up the total throughput of a WDM MCM are increasing the data rate per wavelength and increasing the number of wavelengths. Scaling up the data rate per wavelength can be achieved by multiplexing channels of data together on the same wavelength or by increasing the data rate on the wavelength. Multiplexing multiple channels to a single wavelength can be achieved via polarization division multiplexing (PDM) [120] and mode division multiplexing (MDM) [121]. PDM is a mature enough approach that silicon photonic foundries are beginning to offer polarization splitters and rotators on MPW runs [122, 123]. One of the drawbacks for PDM is polarization drift that will occur in fiber-based transmission. While work has been explored to expand PDM beyond dual polarization systems [124], practical integrated systems are limited to the dual polarization of TE and TM, limiting the scalability of PDM. MDM presents another avenue for multiplexing on a single wavelength. While challenges related to MDM exist—such as mode crosstalk and coupling MDM data to a multimode fiber—MDM systems with 11 modes have been demonstrated on a single polarization [125]. The direct approach to scale up the data rate per wavelength is to increase the data rate. Scaling up to 50 Gbps per wavelength is possible with non return to zero (NRZ) modulation. Microdisk modulators have been demonstrated with 64 Gbaud signals [44] and photodiodes have been demonstrated with bandwidths above 100 GHz [60]. Interposer transmission lines with bandwidths up to 50 GHz have been demonstrated [126, 127]. Driving EICs to interface to silicon photonic MZMs have been shown to operate up to 56 Gbaud [90, 91]. Combining all these elements together presents a path for NRZ 50 Gbps. To achieve data rates of 100 Gbps and beyond, it is necessary to move to higher order modulation formats. Data rates of 200 Gbps on a single wavelength have been demonstrated with MZM-based 16-QAM (quadrature amplitude modulation) in an MCM transceiver [98]. While coherent modulation schemes present the path towards the highest data rates, they often require power hungry signal

processing to recover the signal. A compromise is to use PAM-4 (pulse amplitude modulation), which has been demonstrated at 128 Gbps in microring resonators [44].

2.4.2 Increasing Channel Counts

Our preferred approach for scaling up the total throughput is to increase the number of wavelengths in the transceiver. The cascaded bus-microdisk modulator and demux architecture is scalable to tens of channels. Ultimately, the number of channels that can be placed on a single bus waveguide is bounded by the FSR of the resonant devices and minimum channel spacing that can be supported by the link. To further increase the scalability of the architecture, an interleaving structure can be used to route different groups of channels to different cascaded buses of modulators or demuxes [115]. Such an approach can be scaled to hundreds of wavelengths to provide a clear path towards links with multiple Tbps of data. This system provides a natural integration with CMOS-compatible comb lasers that produce hundreds of evenly spaced wavelengths [70]. Constructing massively parallel links with 10 Gbps channel rates provides an energy efficient path towards Tbps links. With over 100 channels, it is reasonable to allocate one or more wavelengths for clock forwarding, removing the need to perform clock recovery at the receiver. The 10 Gbps channel data rate avoids a heavy reliance on serialization and deserialization (SERDES), which typically dominate power consumption of optical transceivers [6]. SERDES with clock and data recovery (CDR) can consume up to 60% of a transceivers total power [128]. Using 10 Gbps channel rates also avoids the reliance on digital signal processing (DSP). In coherent commercial optical transceivers, the DSP application specific integrated circuit (ASIC) consumes as much power as the rest of the transceiver combined [129]. Additionally, channel rates of 10 Gbps are close to the most efficient rate for resonant modulators/demuxes in silicon photonics requiring thermal stabilization [130, 131]. This architecture provides the foundation for a highly parallel system that combines energy efficiency, high throughput, and high areal bandwidth density.

Chapter 3: Design Considerations for MCM Prototypes

In this chapter, we present the key design considerations that were identified during the development of our version 1 prototype and apply those design considerations to the development of our generation 2 prototypes. These design considerations are: integration approach, equivalent circuit model development for the photonic components, model for the PIC to EIC interface, MCM I/O design, and design for assembly. Identifying and incorporating these considerations is important, as ineffective integration with the electronic circuitry can negate any potential benefit from the silicon photonics.

3.1 Integration Approach

The integration architecture for an MCM transceiver directly impacts the transceiver's areal bandwidth, edge bandwidth, and packaging parasitics. These metrics constrain the transceiver's total bandwidth, energy consumption, and performance. While silicon photonics can address the bandwidth demands in data centers and high-performance computers, the benefits can be negated if the MCM transceiver is not integrated appropriately. The main integration approaches for silicon photonic MCM transceivers are monolithic, 2D, 3D, and 2.5D.

Monolithic integration is defined as when both the driving electronic circuits and the photonic components are fabricated within the same process, as shown in Figure 3.1. This approach offers the minimum parasitics, as the photonics and electronics can be tightly integrated with only microns of separation. Additionally, the packaging for monolithic integration is the most straightforward, as separate EICs and PICs don't need to be integrated by an additional fabrication process. The main drawback of monolithic integration is the difficulty of developing a process that is simultaneously optimized for photonic performance and electronic performance. The monolithic

integrations are built on older CMOS nodes—the most cutting edge is a 32 nm node demonstration that is still under development [72]. The alternative to monolithic integration is hybrid integration, where the EIC is fabricated in an electronic-only process and the PIC is fabricated in a photonic-only process. Photonic performance in monolithic processes lags compared to photonic-only processes, as they have high waveguide loss and low photodiode bandwidth [72]. Finally, the development cost for a monolithic process can be prohibitively expensive when compared to separate processes with hybrid integration.

With 2D integration, the PIC and EIC are situated adjacent to each other and connected by wirebonds, as shown in Figure 3.1. This approach is the most straightforward hybrid integration, but introduces comparatively high parasitic inductance, as wirebonds typically have 0.5 – 1.0 nH/mm [83]. Additionally, 2D places a limit on I/O, as connections between the PIC and EIC can only be made on the shared edge, which can limit total bandwidth. 3D integration can be used to increase the I/O between the PIC and EIC, as the I/O connections are no longer limited to a single edge, as shown in Figure 3.1. The I/O connection can be made with microsolder bumps or copper pillars, with pitches down to 50 μm or below [85, 86, 41]. In addition to increasing I/O, parasitics are reduced compared to 2D integration, as the bumps have parasitic capacitance below 30 fF [85, 86]. One of the drawbacks of 3D integration is the poor thermal isolation between the PIC and EIC. PICs have been observed to vary by 20 ºC in the presence of a driving EIC [92], which can introduce operational challenges to thermally sensitive microdisk resonant photonics. Additionally, interfacing the driving electronic integrated circuits of a 3D integrated MCM to compute integrated circuits introduces similar drawbacks as 2D integration. Wirebonds from the MCM will introduce inductive parasitics and limit I/O. A final hybrid approach is 2.5D integration, where both the PIC and EIC are flipped on top of an interposer, as shown in Figure 3.1. An interposer is a thin substrate that serves as electrical redistribution, and can be constructed from silicon, organics, or glass. In the case of a silicon interposer, TSVs can be used to connect to the back side of the interposer to interface to a PCB or another substrate. The benefits of 2.5D integration are that it enables high I/O counts with microsolder bumps or copper pillars at the same pitches as 3D integration, while also

Table 3.1: A comparison of the various integration approaches in terms of performance, parasitics, areal bandwidth density, and MCM I/O bandwidth

Integration Approach	EIC-PIC Performance	EIC-PIC Parasitics	Areal Bandwidth Density	MCM I/O Bandwidth
Monolithic	Requires performance compromise	On-chip parasitics only	No bump pitch restrictions	Full chip area for I/O
2D	PIC and EIC separately optimized	Wirebond parasitics	One shared chip edge for wirebonds	Three edges for I/O
3D	PIC and EIC separately optimized	Microbump parasitics	Full chip area for flip chip bumps	Four edges for I/O
2.5D	PIC and EIC separately optimized	Microbump and interposer parasitics	Full chip area for bumps but interposer routing limits	Full interposer area for I/O
Active Interposer	PIC and EIC separately optimized	Microbump parasitics	Full chip area for flip chip bumps	Full interposer area for I/O

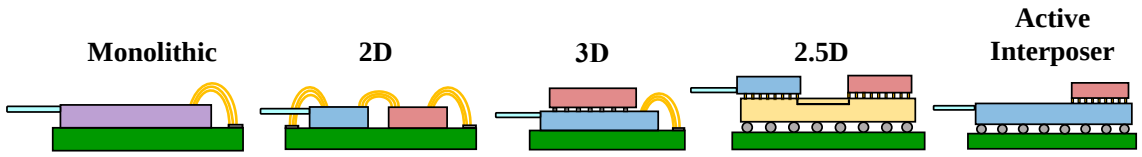

Figure 3.1: The various integration approaches compared in Table 3.1.

providing a platform for further scalability by allowing compute integrated circuits to be flipped on the same interposer or interfaced through the connections on the backside of the interposer. A drawback of the 2.5D integration is that the parasitics at the interface between the PIC and EIC will be larger, as signals must pass through a pair of bumps and the trace on the interposer.

3.2 Photonic Equivalent Circuit Model

Developing integrated MCM transceivers requires close co-development of the photonic components with the electronic driving circuits. While commercial electronic drivers can be purchased, to develop energy efficient transceivers with the highest performance, the driving circuitry needs to be developed to match the specific photonic components. In order to design around the specific photonic components (modulators and photodiodes), compact equivalent circuit models for these

components need to be developed. Equivalent circuit models can vary widely in complexity; it is best to make the model as simple as possible, while still capturing the physical properties of the components, to avoid creating a model susceptible to overfitting [132]. Models can be as simple as a resistor and a capacitor in series to model a silicon photonic depletion phase shifter [133]. The capacitor represents the PN junction capacitance and the resistor represents the series resistance of the slightly doped P/N silicon and the contact resistance to the silicon. Such a model does not include parasitics, pad models, or trace models, but serves as a first order model that is adequate for some applications. More complex models can be developed for transmission line equivalent circuits for travelling wave carrier depletion phase shifters in MZMs. These models can include tens of individual circuit components in the equivalent model [134, 135], and are required to be distributed models rather than lumped models to account for the changing phase across the photonic component. Additional silicon photonic equivalent circuit models have been developed and fit for electro-absorption modulators [136], microring carrier injection modulators [137], microring carrier depletion modulators [138, 139], and Germanium photodetectors [136, 138, 140].

In developing our model, we followed the base model outlined in [139]. The base model, along with additional circuit components added to reflect our layout and measurement setup, can be seen in Figure 3.2. The C_J and R_S represent the modulator's junction capacitance and the series resistance from the doped silicon and contacts to the silicon, respectively. The C_P represents the parasitic capacitance. The C_{Pad} and R_{Pad} represent the capacitance from the pads to the silicon substrate and the resistance within the substrate, respectively. Inductance components were added between the pad portion and the modulator portion. Additionally, a RF probe was used to measure the device—parasitic inductance, resistance, and capacitance were added to the model, as well as the transmission line length component to account for the phase dependence across the frequencies of interest.

The modulator was probed with a ground signal ground (GSG) FormFactor RF probe. A precision network analyzer (PNA) was used to measure the S_{11} of the modulator. Biasing the modulator to the operating 0.5 V reverse bias was achieved with a bias-T in between the PNA and the RF

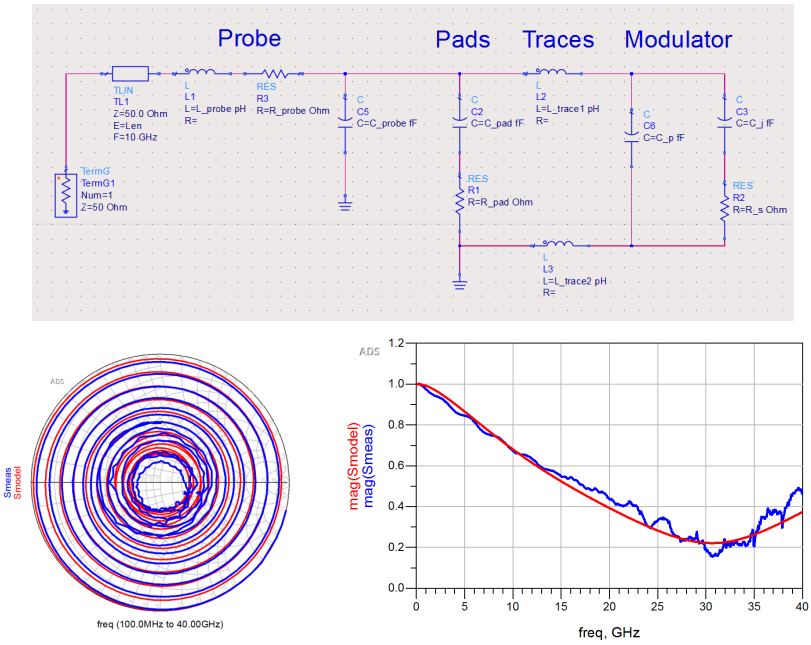

Figure 3.2: a) The equivalent model used for the modulator, showing the probe, pad, trace, and modulator junction components. b) The Smith chart showing the measured and model data for the S11 measurement. c) The S11 magnitude measurement showing the measured and model data.

probe. The measurement setup was calibrated with a calibration kit up to the probe input. The S_{11} measurement was recorded from DC to 40 GHz for several DC bias voltages. The S_{11} data was used to fit the model, shown in Figure 3.2, using ADS. Key values extracted from this process are 93 fF for C_J, 55 fF for C_P, and 133 Ω for R_S. For future work, we intend to model the photodiode used in the MCM transceiver, utilize a on chip calibration substrate to allow for a simpler model, and use a lightwave network analyzer so S_{21} parameters can also be measured.

3.3 PIC to EIC Interface

Similar to developing the equivalent circuit models for the active photonic elements, it is necessary to model the parasitics of the interface between the driving circuits in the EIC and the active photonic elements to achieve high performance interconnects. For 2D integration, the wirebond connecting the PIC and the EIC can essentially be modelled by an inductor, with the inductance per mm ranging between 0.5 and 1.0 nH [83]. Some models can include resistive elements and

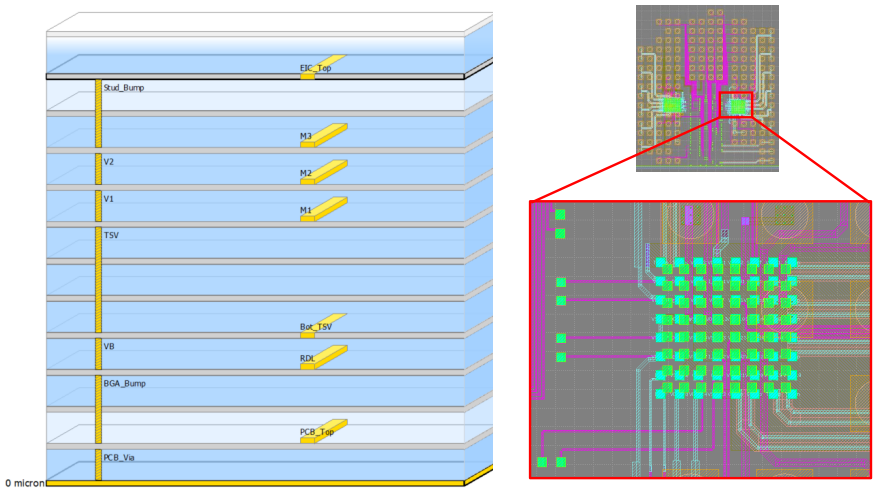

Figure 3.3: On the left, the interposer stackup used for simulations. The stackup includes the interposer, top layer of the PCB and PIC/EIC, stud bumps, and BGA bumps. On the right, the GDS of interposer depicting the connection between the PIC and the RX EIC zoomed in.

capacitive elements for the pads [141] but should not be included if the pads are already incorporated into the photonic equivalent circuit. The parasitics for micro solder bumps and copper pillars tends to be quite small—negligible inductance, less than 1 Ω of resistance, and less than 30 fF of capacitance [85, 86]. While small, the bump's parasitic capacitance is still within the same order of magnitude as the equivalent model's junction capacitance and parasitic capacitance for both the photodiode and disk modulator. This parasitic capacitance is especially important on the receiver portion of the transceiver, as the total capacitance—photodiode junction capacitance, photodiode parasitic capacitance, and bump parasitic capacitance—dictate the dominant pole of the TIA, which impacts the TIA's bandwidth [70].

Moving to 2.5D integration increases the parasitics for the PIC to EIC interface. The interconnect will have two bumps rather than one, and the trace on the interposer also introduces additional parasitics. To determine the parasitics for our 2.5D MCM transceiver with custom EICs, the S parameters for the interposer trace were simulated using EMX up to 40 GHz. Initially, we intended to fit the S parameters to a simple pi model, as shown in Figure 3.4a. Initial results produced a pi models with several Ω for the resistor, less than one nH for the inductor, and tens of fF for each capacitor. However, the pi model did not fit the simulated S parameters very well. There was also

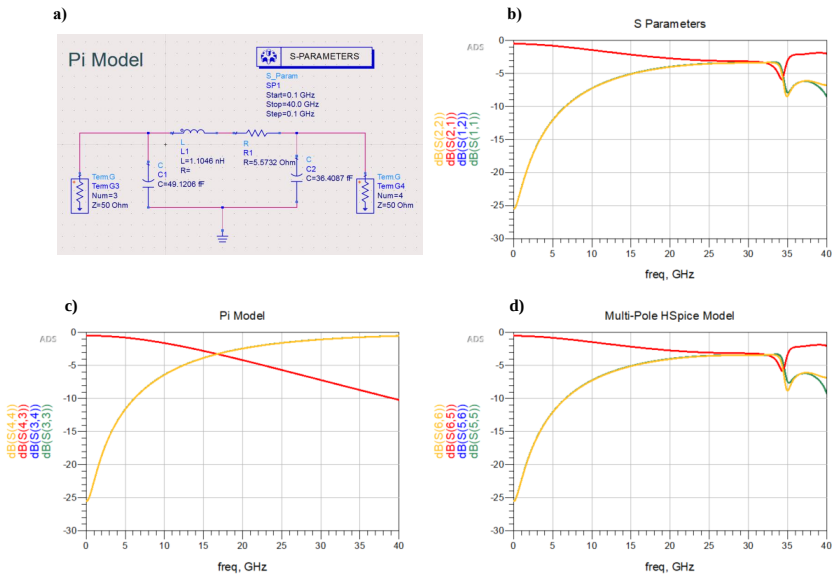

Figure 3.4: The S parameter, pi model, and multi pole HSpice model for a data trace on the interposer between the PIC and EIC. The pi model's parameters were fit with Matlab, and the multi-pole HSpice model was fit in ADS. b) The simulated S parameters for the interposer trace. c) The S parameters from the pi model. d) The S parameters for the multi-pole HSpice model.

concern that the interposer's trace has parasitic capacitance and inductance distributed across the trace, rather than the consolidated representation of the pi model. To better reflect the physical model of the interposer trace, the S parameters were fit to a 30-pole rational polynomial HSpice model using ADS. The resulting model featured over 1000 components to accurately model the interposer trace. The simulation S parameters for one interposer trace can be seen in Figure 3.4b. The pi model's S parameters can be seen in Figure 3.4c and the multi-pole HSpice model's S parameters can be seen in Figure 3.4d. The multi-pole HSpice model accurately models the simulated S parameters, while the Pi model begins to diverge after 15 GHz.

3.4 MCM Data Input and Output

Designing a silicon photonic MCM transceiver requires careful consideration with regards to how the I/O data interfaces electrically to the transceiver. Improper design of the I/O can limit the transceiver's performance, potentially negating innovations in the PIC and EIC. Improper I/O can introduce parasitics and impedance mismatches that limit system performance. The I/O choices

will depend on the MCM integration approach.

For 2D or 3D integration, wirebonding is the most common approach to interface to the MCM transceiver. The main drawback of wirebonding is the parasitic inductance from the bond: it is typically between 0.5 and 1.0 nH/mm [83]. Additionally, wirebonds are typically restricted to the edges of the chips. If the design requires a large number of connections, the larger required fanout will increase the parasitics and enlarge the impact of impedance mismatch. Wirebonds connections can be made as dense as 25 μm pitches [82], but the tradeoff is that denser pitches require thinner wires which increases the parasitic inductance. An alternative I/O approach for 3D integration hangs the EIC off the edge of the PIC, where a high density glass ceramic interposer (GCIP) is used to provide a vertical connection from the MCM transceiver and the package substrate [96]. This allows for denser pitches and lower parasitics compared to wirebonds, with the tradeoff being assembly complexity.

For 2.5D integration, the PIC and EIC are both flipped onto an interposer, which provides the connectivity between the two dies with electrical traces. Common interposer materials include silicon, glass, and organic substrates. Data I/O from the MCM transceiver can be achieved with vias to the backside of the interposer—which interfaces to the package substrate—or with bridges to interface between the MCM and another die or interposer. The bridge can be on top of two interposer tiles to provide connectivity [142] or embedded within an organic substrate, enabling trace densities beyond what may be supported by the organic substrate alone [143]. A common approach for implementing a vias is to use a thinned silicon interposer and create the connectivity between the front and back of the interposer using TSVs. TSVs are often in the range of 100 μm to 200 μm tall, which makes it difficult to control the impedance of the TSVs. This impedance mismatch can introduce reflections, resulting in reduced signal strength and increased noise [6]. While it is difficult to control the impedance in TSVs, they can be design around—equivalent circuit models have been developed [144], and transmission lines incorporating TSVs in the critical path have been demonstrated up to 50 GHz [126].

More exotic alternatives to metal vias exist, such as the ThruChip Interface (TCI), which uses

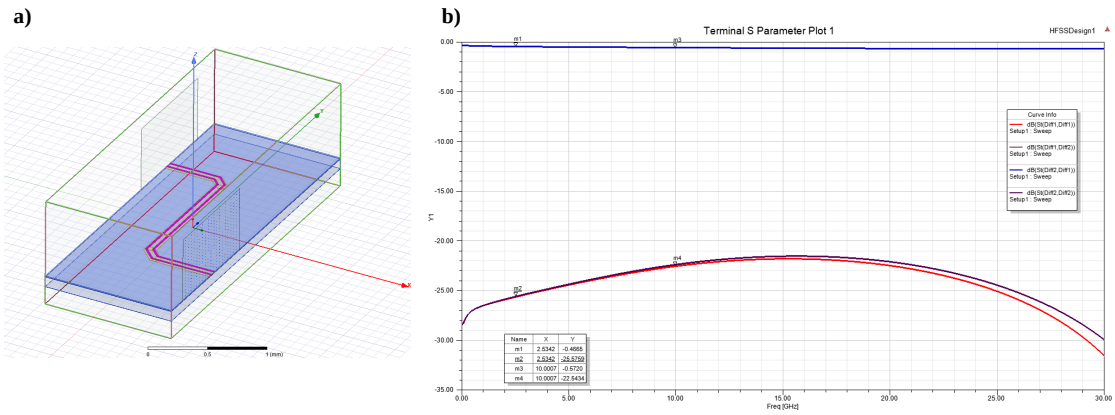

Figure 3.5: a) The model for two traces to simulate the interposer's transmission lines. b) The S parameters for the simulated interposer transmission line up to 30 GHz.

wireless connections through near-field inductive coupling [145]. The transmitter inductive coils produce a magnetic field through the silicon which is vertically received with a similar receiver coil. This approach offers a lower cost alternative to TSVs and has been demonstrated with 30 Gbps links [146]. A drawback of the TCI approach is the size of the coils—the diameter needs to be approximately three times the vertical distance transmitted [147], for an aspect ratio of 1:3 (height to width). Comparatively, TSVs can be fabricated with an aspect of 10:1 [148], allowing for much denser pitches.

Whether vias through an interposer to the backside or a bridge on top of the interposer are used, the data I/O will often require fanout traces on the interposer. For high speed signals, these traces should be transmission lines to minimize impedance mismatch. Our 2.5D integrated MCM transceiver utilized a silicon interposer. Numerous types of transmission lines have been demonstrated in silicon interposers, including microstrip, coplanar waveguide (CPW), grounded CPW, differential CPW with good performance up to 50 GHz [85, 70]. In developing the second generation of our MCM transceivers, three variations of 10 mm long transmission lines were investigated: a microstrip line using top level metal layers, a CPW using the top metal layer, and a CPW using the backside metal. For each variation, a transmission line was designed for 50 Ω impedance, as well as versions with slightly thicker and slightly thinner signal lines.

The top level microstrip transmission line was used in the MCM transceiver—the model used

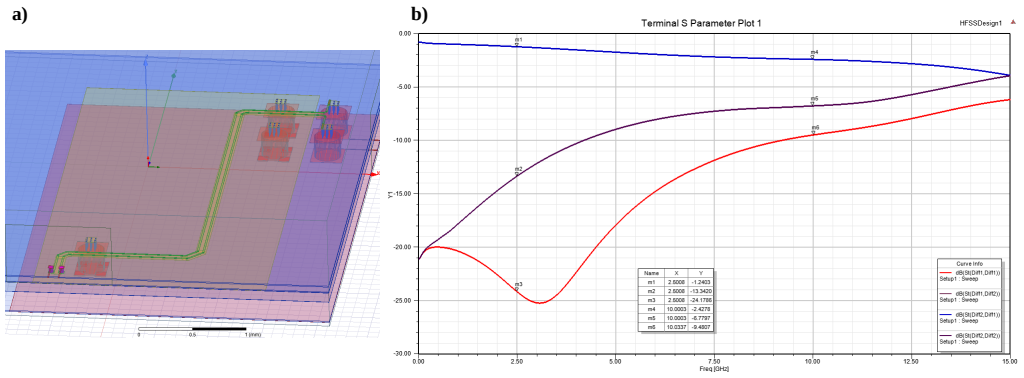

Figure 3.6: a) The model in HFSS used to simulate the pair of transmission lines with the micro bumps and BGA-type solder balls included. b) The simulated S parameters up to 15 GHz.

for simulation can be seen in Figure 3.5a. The performance of a differential pair can be seen in Figure 3.5b. The simulation shows that at 30 GHz S_{21}/S_{12} is better than -1 dB and S_{11}/S_{22} is less than -21 dB. While the performance of just the transmission lines on the interposer is expected to be good, it is necessary to include the bumps to the interposer in the simulation. For our MCM transceiver, 50 µm diameter stud bumps were used between the EIC/PIC and interposer, and 300 µm diameter BGA-type connections were used between the interposer and the PCB. The model used to simulate the interposer in HFSS can be seen in Figure 3.6a. Including these bumps in the simulation degraded the performance, as seen in Figure 3.6b. In the MCM transceiver, deserialization occurs in the EIC prior to fanout on the interposer, which results in a target data rate of 2.5 Gbps for the interposer transmission lines. Including the bumps at 2.5 GHz resulted in a S_{21}/S_{12} of -1.2 dB, a S_{11} of -24.2, and a S_{22} of -13.3 dB for the simulated transmission lines.

To aid in designing interposer transmission lines for future MCM inputs and outputs, we designed and test transmission lines to optimize for impedance matching and attenuation. Three designs of transmission lines were fabricated, which each design featuring three variations to fine tune the impedance. For each design, variations were simulated in ADS LineCalc to achieve slightly below 50 Ω, 50 Ω, and slightly above 50 Ω. The three transmission line designs were: CPW using the top level aluminum traces, microstrip using the top level aluminum as the signal layer and an inner level copper as the ground layer, and CPW using the back level copper layer. In addition to the transmission line tests, various tests were designed to extract parasitics related to

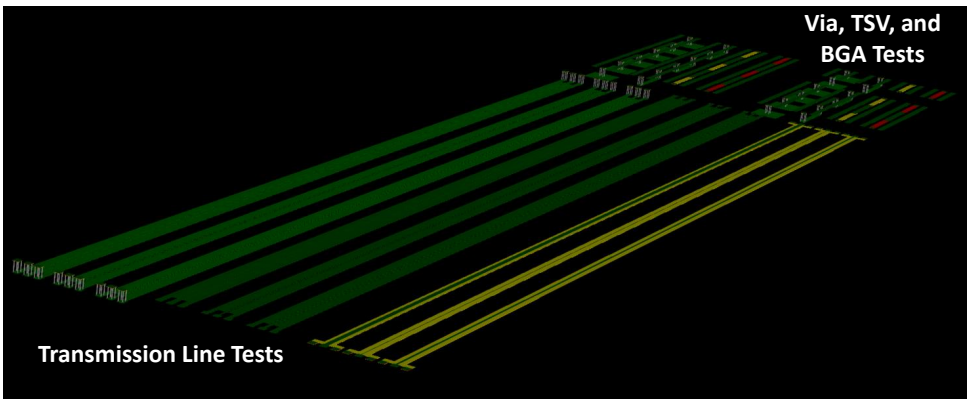

Figure 3.7: The test structure portion of the version two interposer. On the left are three variations of transmission lines, each with three different designed impedances. On the right are loopback structures for the various vias of varying numbers of loops to extract parasitics of the vias.

different features in the signal path: vias, TSVs, and BGAs. These tests featured a varying number of loopbacks for each of the features to determine the parasitics and impact on the signal path.

3.5 Design for Assembly

Designing the MCM transceiver to facilitate the assembly of the optical interface to the transceiver is a key component of the design process. For 2D and 3D integration, the integration with the EIC generally introduces minimal restrictions to optical coupling to the PIC. For 2D integration, the top area of the PIC is unaffected—with 3D integration, the EIC is flipped on top of the larger PIC, leaving top areas of the PIC uncovered. As a result, vertical coupling to grating couplers on the PIC is the most common optical coupling method in 2D and 3D MCM demonstrations [85, 70, 96], though edge coupling has also been demonstrated [102].

When implementing more complex integrations-—such as 2.5D integration-—the top area of the PIC may be mostly covered due to being flipped on top of an interposer. In this scenario, edge coupling is preferred approach, but can be challenging as most of the PIC's top is covered. To facilitate edge coupling to the PIC, one approach is to overhang the PIC off the edge by several hundred microns to a visual contact to the location of the edge coupler [95]. This approach was followed in developing our 2.5D MCM transceivers, as seen in Figure 3.8. While overhanging the

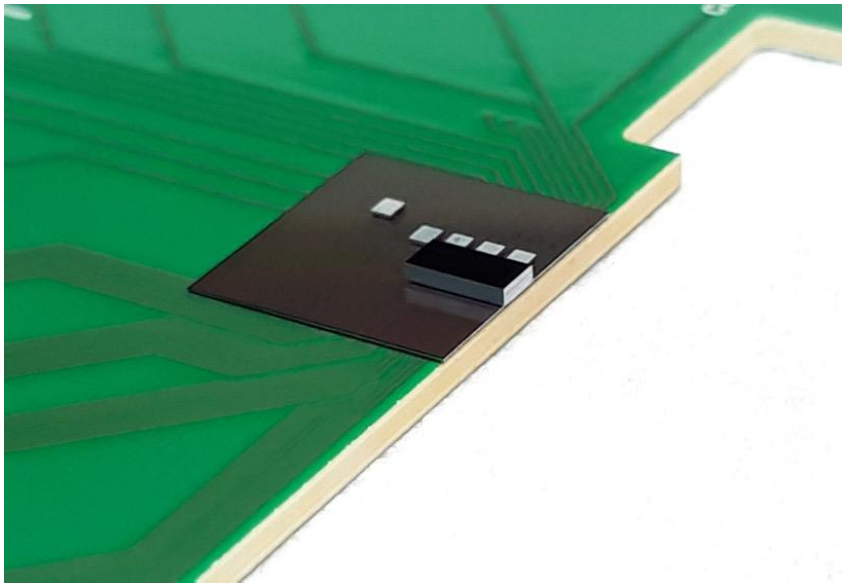

Figure 3.8: The prototype without the optical fiber attached. The PIC overhangs off the interposer to facilitate optical coupling by providing a visual sight of the edge couplers from below.

PIC enables easier optical coupling, an alternative is to fabricate the interposer substrate with a trench to allow a fiber array to be coupled to the PIC in the middle of the MCM [98]. Another approach transforms the interposer to an optical interposer, which incorporates an optical waveguide layer to the interposer. With a silicon interposer, this optical waveguide can be implemented with a silicon nitride (SiN) layer [149]. Etching shallow trenches into the interposer enables the edge couplers of the flipped PIC to butt couple to the SiN waveguides in the interposer. The SiN waveguides can then route out to the edge of the interposer for conventional edge coupler fiber array attach. For integration requiring vertical optical routing through an interposer, optical TSVs have been developed, such as to allow a vertical cavity surface emitting laser (VCSEL) output to route through an interposer to an optical printed circuit board [104]. The optical TSV can either be implemented with an air-filled TSV or a waveguide TSV. To design the waveguide TSV, the TSV needs to be coated with a low index material to shield the mode from the silicon that the TSV traverses [150].

Similarly, designing the MCM transceiver with the electrical assembly process in mind can aid in ensuring that the prototype can be successfully assembled. One main consideration is the bump

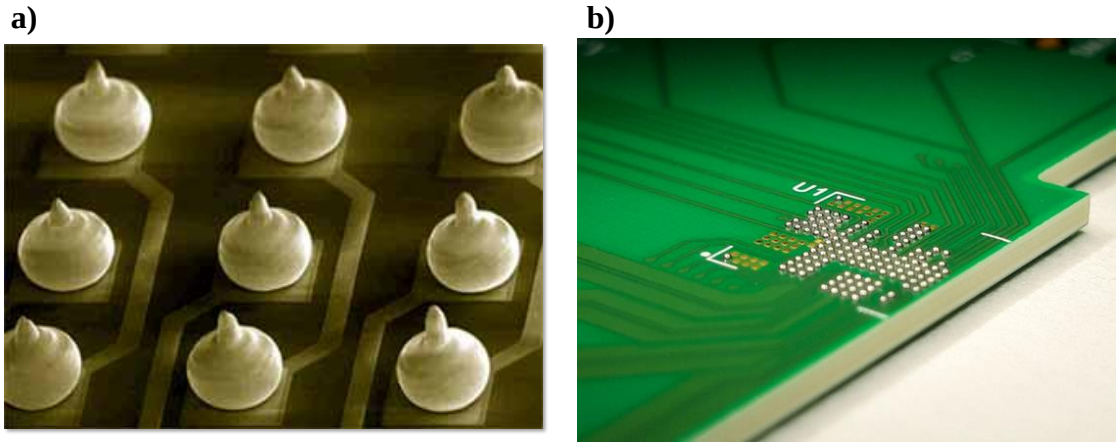

Figure 3.9: a) Examples of stud bumps, with the solder ball around the wire stud. b) The BGA bumps on the PCB prior to interposer placement and reflow.

pitch for the PIC and EIC. Denser bump pitches allow for higher I/O counts, resulting in higher bandwidth densities. For bump pitches below 100 µm, the most common approach is full wafer bump growth for both copper pillars and microsolder bumps. Full wafer bump growth may be acceptable for full transceiver development, but for smaller prototypes it may be too costly. While the standard for dense bump pitches is full wafer growth, some vendors do advertise single die bump growth as dense as 25 µm [89]. For electrical I/O, the pitch limitations are dependent on the MCM substrate. While interposers support pitches comparable to those for EICs and PICs, PCBs are not able to be fabricated with as dense of pitches. Typical PCB fabrication minimums are three mil trace width and three mil trace spacing, which translates to a pitch of approximately 150 µm. For our 2.5D integrated MCM transceiver, the backside of the interposer interfaced to a PCB with a BGA type connection. Standard BGA packages can be supported with pitches down to 0.5 mm [106]—and we implemented our BGA type connections with 0.5 mm, as shown in Figure 3.9b. For our second iteration of prototypes, this dense BGA pitch made routing out on the PCB difficult, resulting in requiring a six-layer board and via-in-pads. A final consideration is bump reflow temperatures across a variety of bumps. For our MCM transceiver, we utilized stud bumps between the interposer and both the PIC and EIC, as shown in Figure 3.9a. The assembly order was PIC and EIC reflowed the interposer, and then interposer reflowed to the PCB. The

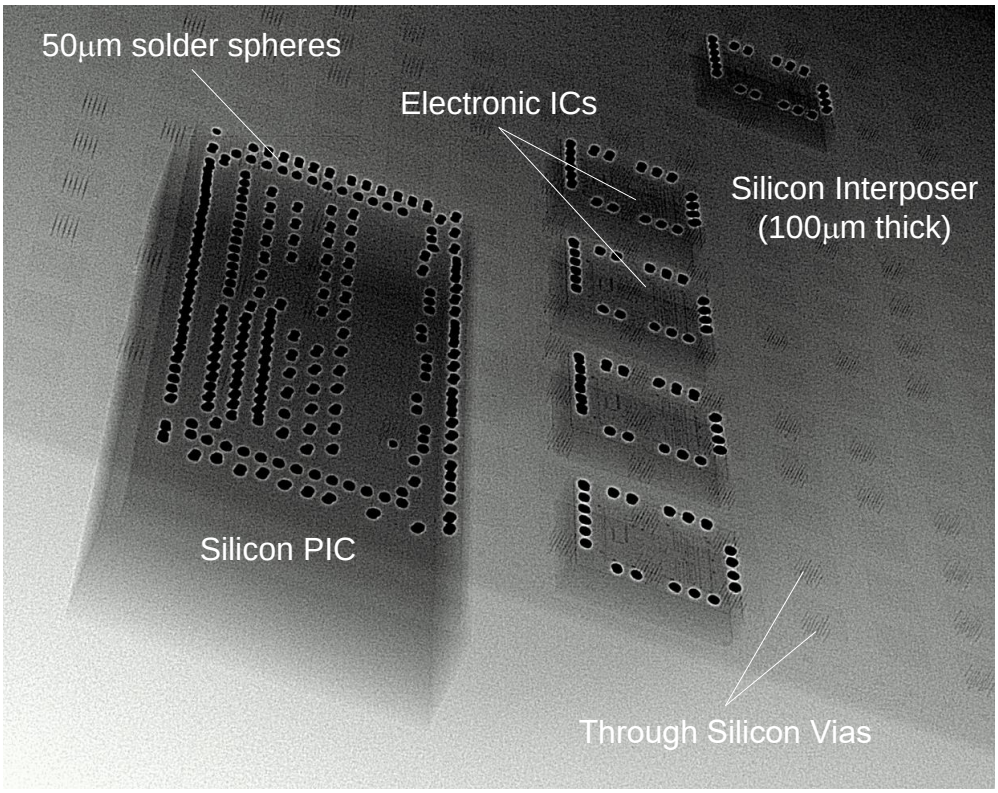

Figure 3.10: An X-ray image of the interposer with the PIC and EICs flipped on top, taken prior to being placed on the PCB. The TSVs and stud bump solder balls can be seen in the image, as well as the PIC hanging off the interposer to facilitate optical coupling.

reflow temperature of the stud bumps needed to be high enough that it would not reflow when the interposer was being attached to the PCB.

3.6 Conclusion

In this chapter, we identified five areas of design regarding developing silicon photonic MCM transceivers: integration architecture, equivalent circuit model development, PIC to EIC interface model development, MCM I/O design, and design for assembly. The process of developing the version 1 prototype helped identify the five design areas that were used to develop the second generation prototypes. Each of these design areas can impact the performance of the MCM transceiver, and if neglected can negate the potential benefits of introducing silicon photonics to data centers and high-performance computers.

Chapter 4: Additional MCM Prototypes

In this chapter, we present the design of additional MCM transceiver prototypes. The prototypes in this chapter are either still in the fabrication process or were either unable to be completed for various reasons. The prototypes span two generations–the first generation aligns with the 2.5D integrated MCM with TI TIA EICs detailed in chapter 2. The second generation of prototypes were developed after, using custom EICs. The additional first generation prototypes include a 2.5D integrated MCM transceiver prototype with EICs from Cisco and a 3D integrated active interposer MCM network on chip. The second generation prototypes include a 3D integrated MCM receiver prototype with a custom EIC and a 2.5D integrated MCM transceiver prototype with custom EICs.

4.1 Generation One Prototypes

4.1.1 MCM Transceiver – 2.5D Integration with Cisco EICs

The 2.5D integrated MCM transceiver prototype with Cisco TIAs was developed in parallel with the transceiver presented in chapter 2, utilizing the same PIC. The transmitter on the PIC was identical, but the receiver was located in a different portion of the PIC and interfaced to bare die TIAs from Cisco. The TIAs were single channel, designed to operate at 56 Gbps, and had pre-bumped copper pillars for flip chipping at an 80 um pitch. The receiver utilized a two channel design with the channels on opposite sides of the PIC, as the Cisco EICs required a significant area for connection fanout, as seen in Figure 4.1. The integration approach was the same as the prototype in chapter 2. The PIC and EICs were flipped on top of the silicon interposer, which provided signal fanout and redistribution, as shown in Figure 4.2. Interposer TSVs provided connectivity to the backside of the interposer, where BGA connections were used to interface to a breakout board PCB, as shown in Figure 4.3. The receiver for this version was ultimately unable to be tested due to

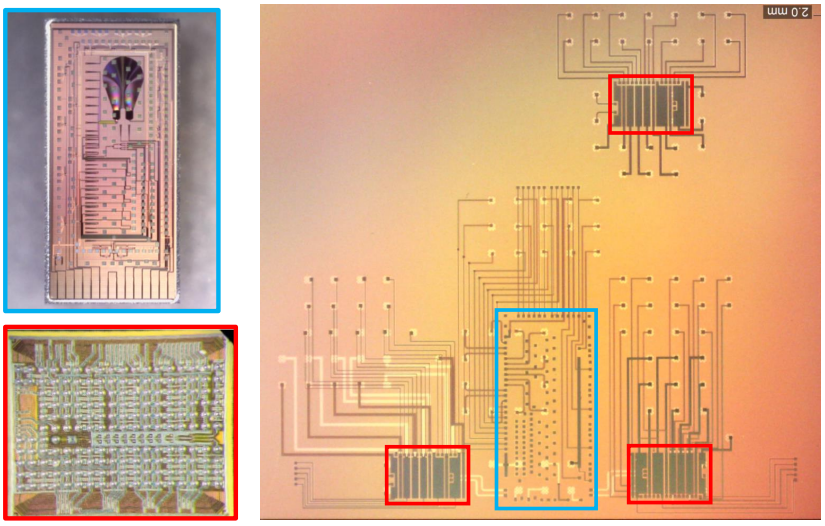

Figure 4.1: The PIC, EIC, and interposer used in the generation 1 transceiver with Cisco EICs prior to assembly. The interposer is shown on the right. The PIC and its bonding location on the interposer are shown in blue. The EIC and its bonding locations on the interposer are shown in red.

the fabrication issue with the cathode-anode flip for the PDK photodiode. The Texas Instruments TIA in chapter 2 featured a cathode-anode-cathode pad connection, which allowed a pad offset to provide the correct polarity in a repackaged version of the prototype. Such an approach was not available for the Cisco TIA as the pad connection was cathode-anode.

4.1.2 MCM Network on Chip – 3D Integration with Active Interposer and Texas Instruments EICs

The focus of this prototype was to utilize the benefits of the active interposer. As mentioned, the active interposer is functionally a single structure that contains a portion serving as the interposer with electrical redistribution as well as a portion containing the active silicon photonics components, as shown in Figure 4.4. The active interposer is composed of a thinned interposer wafer and a thinned PIC wafer, and then the two are wafer bonded with connections between them, such that the PIC wafer is on top of the interposer wafer. From the design perspective, it is a single active interposer. The active interposer is especially attractive since it provides a platform

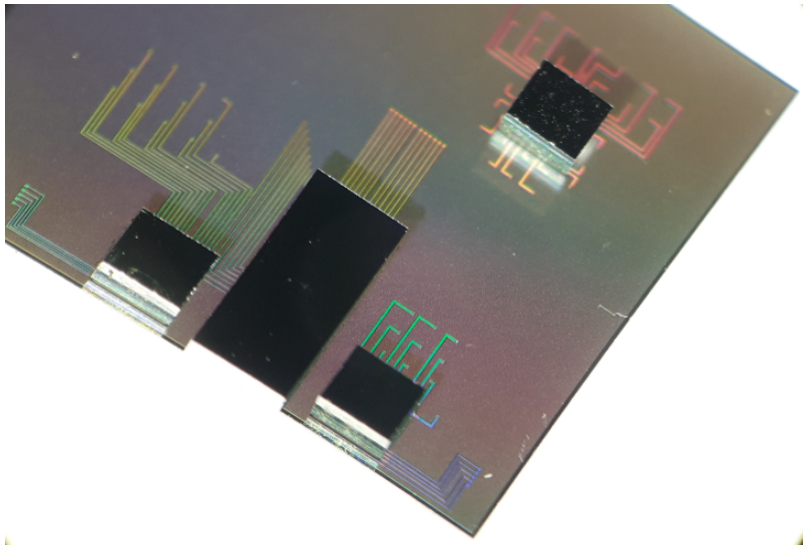

Figure 4.2: The assembled MCM showing the silicon interposer, which provides connectivity between the two TIA EICs from Cisco and the PIC. The isolated EIC is not connected to the PIC and used for TIA-only tests.

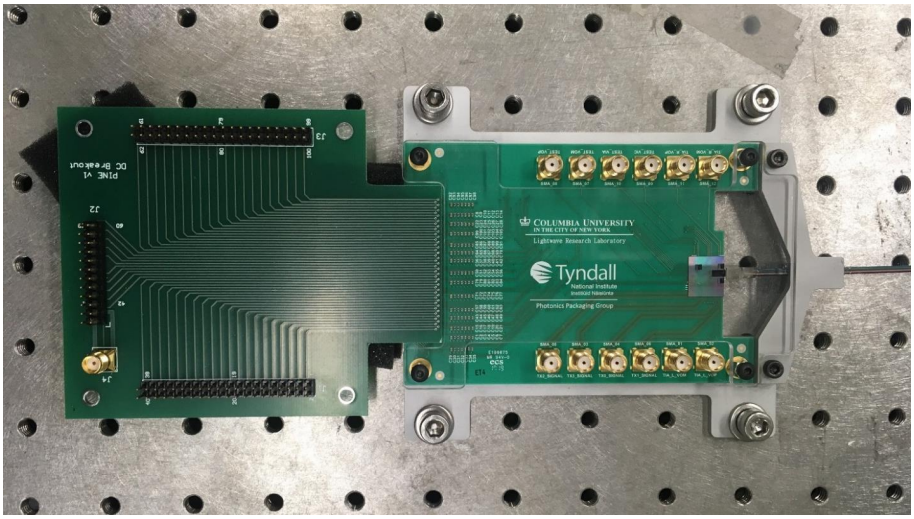

Figure 4.3: The fully packaged generation 1 transceiver with Cisco EICs as seen from above, which the additional breakout board mounted on the back of the main PCB.

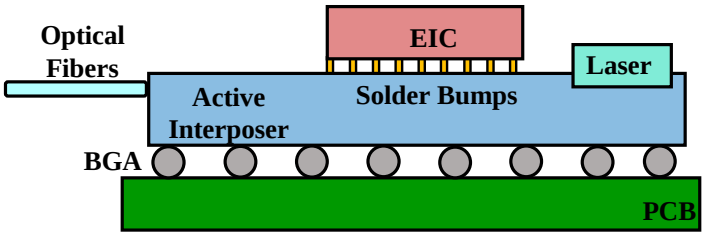

Figure 4.4: The side profile of the active interposer used in the generation 1 prototype. The thinned active interposer has TSVs to interface to the PCB and allows for trenches to be fabricated in the interposer for integrating lasers.

to minimize the electrical parasitics between the EIC and PIC while providing significant MCM I/O. For a 2.5 integrated MCM, the connection between the EIC and PIC in the passive interposer must traverse through two sets of flip chip bonds (either stud bumps or copper pillars) as well as a trace on the interposer. With the active interposer, the connection only requires one set of flip chip bonds, minimizing parasitics. As a result, the active interposer combines the interposer integration benefits with low parasitics. This active interposer run was an experimental run for which we were collaborating with SUNY.

For this prototype, the active interposer was used as the platform to create an integrated network on a chip. An 8 x 8 Mach Zehnder interferometer (MZI) non-blocking Beneš switch was placed in the middle of the active interposer to provide the connectivity and reconfigurability of the network on chip. The schematic is shown in Figure 4.5. Half of the inputs and outputs of the switch were connected directly to edge couplers. The remaining inputs were connected to bus waveguides—each with four microdisk modulators at different wavelengths. The modulators were externally driven. The remaining outputs were connected to bus waveguides-—each with four microdisk demuxes with the drop ports connected to high-speed photodiodes. Bare die TIA EICs were flipped on top of the active interposer to interface to the photodiode outputs of the active interposer. The EICs were the same single channel Texas Instruments bare die TIAs that were used in the 2.5D integrated MCM prototype in chapter 2 and were designed to operate at 11.3 Gbps. The flip chip bonds for this prototype were stud bumps.

In addition to the active interposer prototype, there were test structures contained within the

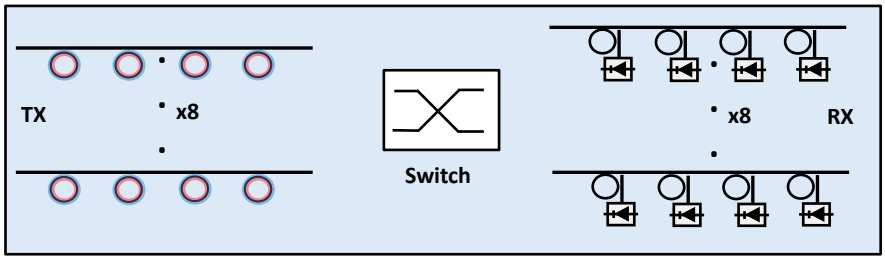

Figure 4.5: The schematic of the active interposer network on chip, showing the switch providing connectivity to eight bus waveguides for transmit and receive microdisks.

active interposer to aid in future development. Lasers were intended to be integrated in a small trench in the active interposer, with the laser outputs coupling to silicon nitride waveguides in the active interposer, in a similar manner to a trench for a PIC to be flipped into a passive interposer. Experimental switch designs, higher order microdisk modulators, and an optical deserializer were also integrated within the free space of the design. The GDS for the active interposer can be seen in Figure 4.6.

The active interposer is currently in fabrication at SUNY CNSE. One of the significant unknowns is how the thermal characteristics and responses of the thermal tuners will change with the PIC's substrate being removed and with the PIC being wafer bonded to a thinned interposer. An additional challenge is the fabrication and assembly of the active interposer. Similar to a thinned passive interposer, the active interposer requires a temporary bond and back grind to remove the substrate prior to a final bond. Earlier prototypes with passive interposers encountered issues with cracking in the wafer during the temporary bond and back grind. As mentioned earlier, the development time and costs will be higher than integration approaches like 2D, 3D, and 2.5D integration.

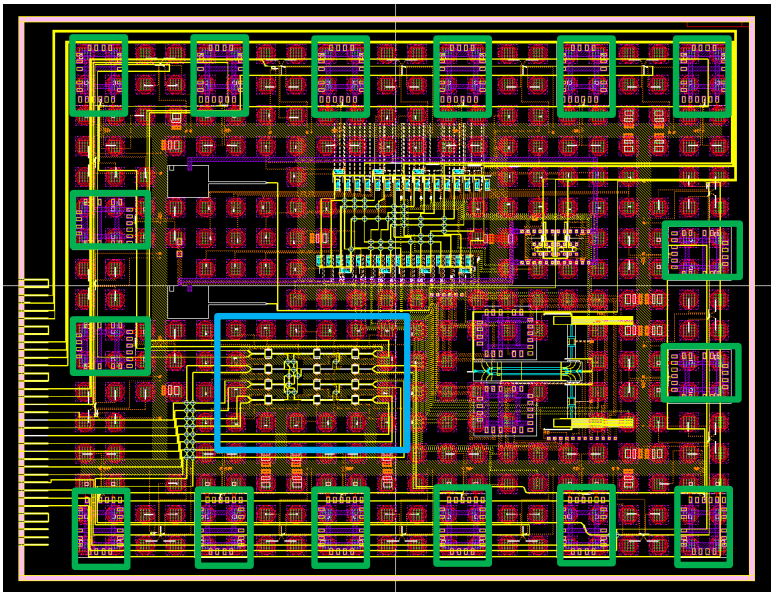

Figure 4.6: The GDS of the active interposer. The landing locations for the TIA EICs shown in green. The MZI switch is shown in blue. There are additional various test components in the middle of the active interposer.

4.2 Generation Two Prototypes

4.2.1 MCM Receiver – 3D Integration With Custom EIC

Two integration approaches were pursued in the second generation prototypes: 2.5D integration and 3D integration. As mentioned, the 3D integration approach should allow for lower parasitic capacitance due to signal propagation between the PIC and EIC only needing to traverse through one bump rather than a pair of bumps and an interposer trace. As mentioned, increased parasitic capacitance reduces the bandwidth of the receiver for a given SNR. Increased parasitic capacitance could be combated by reducing the resistance across the TIA (to maintain the RC time constant), but this reduces the gain of the TIA and therefore lowers the receiver sensitivity, which then requires a higher laser launch power for the channel. The assembly approach can be seen in Figure 4.7. In addition to utilizing a different integration approach, this receiver prototype differed from the version 1 prototypes because it employed a custom EIC developed by collaborators for the receiver EIC, rather than commercial TIAs from Texas Instruments and Cisco. The RX chip was

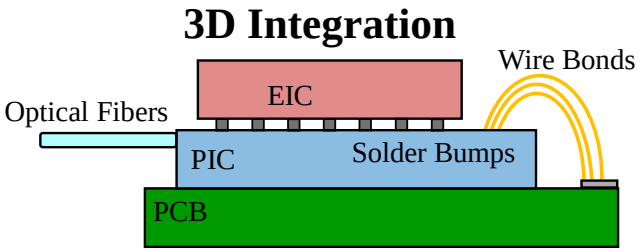

Figure 4.7: The side profile of the 3D integrated receiver with wirebonds to interface from the PIC to the PCB.

fabricated in TSMC 28 nm HPC RF using a MUSE Semiconductor MPW run. The chip was 1.0 mm by 1.2 mm and used 80 flip chip pads spread over the chip area with evenly spaced pads in an 8 by 10 orientation with a pad pitch of 100 µm.

The components within the low voltage (0.9V) RX EIC included a TIA with a DC current offset cancellation loop, single-ended to differential conversion, a variable gain amplifier, 1-tap decision-feedback equalization (DFE) to reduce inter-symbol interference (ISI), a quadrature locked loop (QLL) for deserialization, and an output buffer. The RX chip featured two data channels and one clock channel, as the interconnection were to be implemented with clock forwarding to reduce energy consumption when scaling to many channel DWDM prototypes. The EIC was designed for low power consumption to target sub pJ/b interconnect energy consumption; this was supported in the EIC with the low supply voltage, DFE to reduce the required received optical power - reducing the required laser launch power, and clock forwarding to remove the need for clock recovery. The simulated power consumption will be highlighted in the following section, as it includes the energy consumption of both the receiver and the transmitter EICs. The circuit diagram can be seen in Figure 4.8.

The PIC that interfaces to the EIC featured a bus waveguide with three demux microdisks with integrated doped heaters for thermally tuning the resonances of the drop ports. At the drop port of each demux was a high-speed germanium photodiode. There were three channels for the two data channels and one clock channel on the RX EIC. At the end of the bus waveguide there was a 50-50 splitter. One output went to a monitor photodiode to provide a signal for thermal stabilization. The other output was routed back to the edge of the chip. Optical coupling to the chip was achieved via

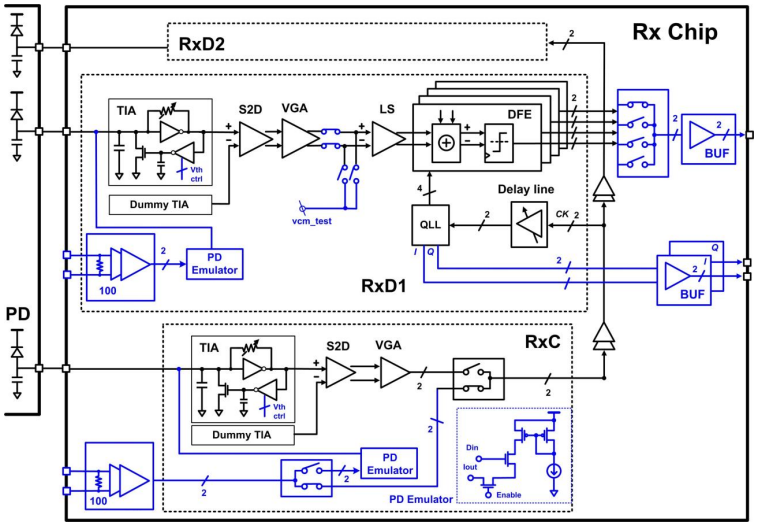

Figure 4.8: The circuit diagram of the custom EIC that is flipped on top of the PIC for the 3D integrated receiver. The EIC features two data channels and one clock channel. The data path includes TIAs, single end to differential conversion, variable gain amplifier, decision feedback equalization, deserialization, and an output buffer.

edge couplers. The PIC was fabricated in an AIM MPW run. The bare die images for the PIC and EIC can be seen in Figure 4.9.

The integration was designed so that the EIC was flipped on top of the PIC. All the PIC and EIC signals were routed out to the edge of the PIC to pads on three sides of the PIC to enable wirebonding to the PCB which the PIC sits on. The fourth side of the PIC was reserved for optical coupling with a 127 µm fiber array. Both the PIC and EIC are terminated with Al pads. Assembly was to be done using Quik-Pak, a packaging vendor. Both the EIC and PIC were to be bumped with Au stud bumps at 100 µm pad pitches. The EIC was intended to be flipped on top of the PIC using thermo-compression of the Au to Au bumps. After die mounting to the PCB, wirebonding, and partial encapsulation of the wirebonds, the prototype was to be sent to PLC Connections to optically attach a fiber array to the PIC with mechanical supports to the PCB. The PCB was designed so the PIC sat on one edge of the board. High speed connections were routed to edge coupled SMAs on the sides of the PCB and DC signals were routed to the far side of the PCB to a mezzanine connector. The PCB can be seen in Figure 4.10.

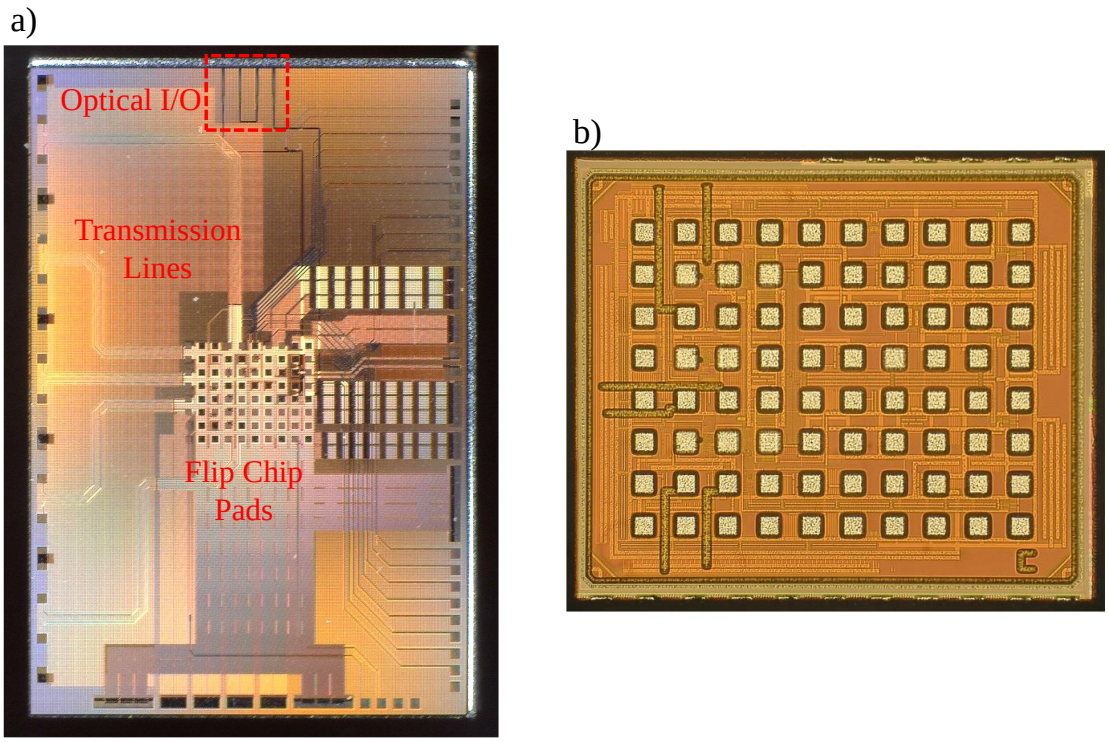

Figure 4.9: The chip images of the PIC and EIC used for the 3D integrated receiver. a) The PIC, highlighting the optical edge couplers, the flip chip pads for the EIC, and the transmission lines from the EIC to the edge of the PIC for wirebonding to the PCB. b) The EIC with the 80 flip chip locations.

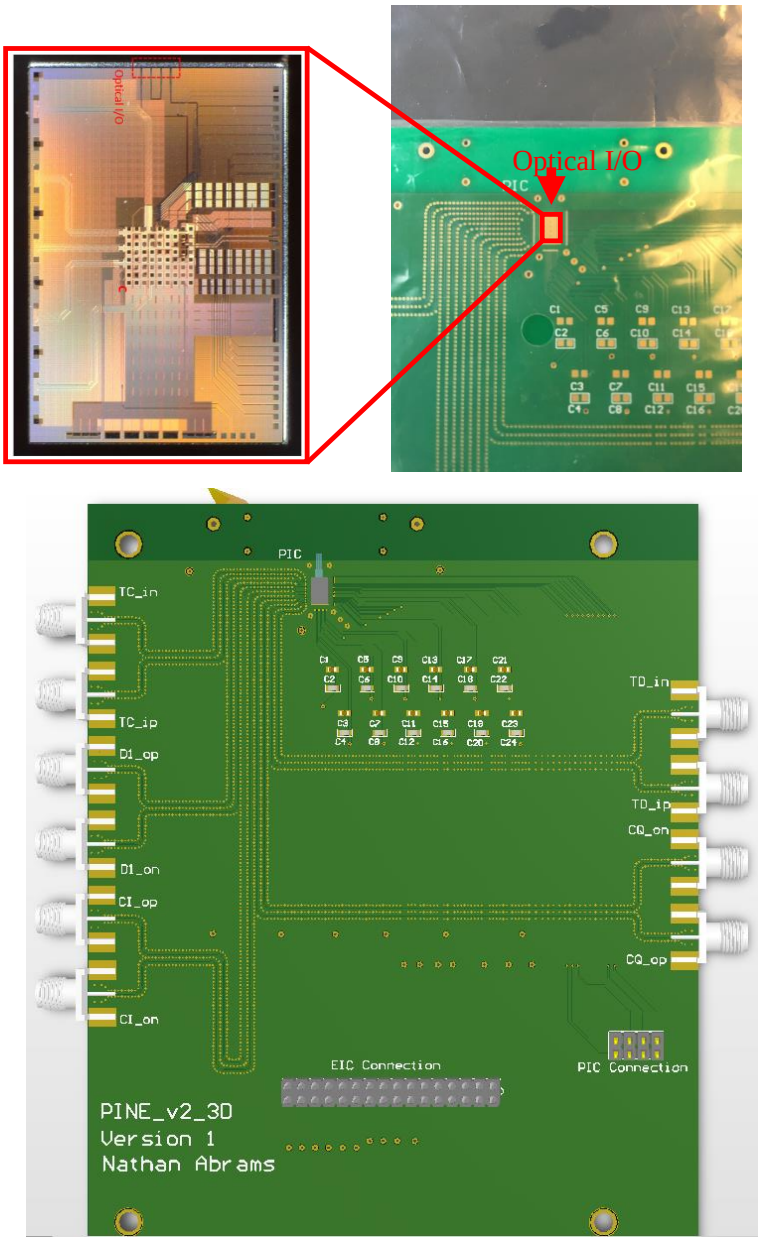

Figure 4.10: The integration overview for the 3D integrated receiver prototype. The PIC (with the EIC flip chipped on top) was to be glued to the PCB with wirebonds providing the interface between the PIC and EIC. The PCB would provide fanout for the RF and DC signals.

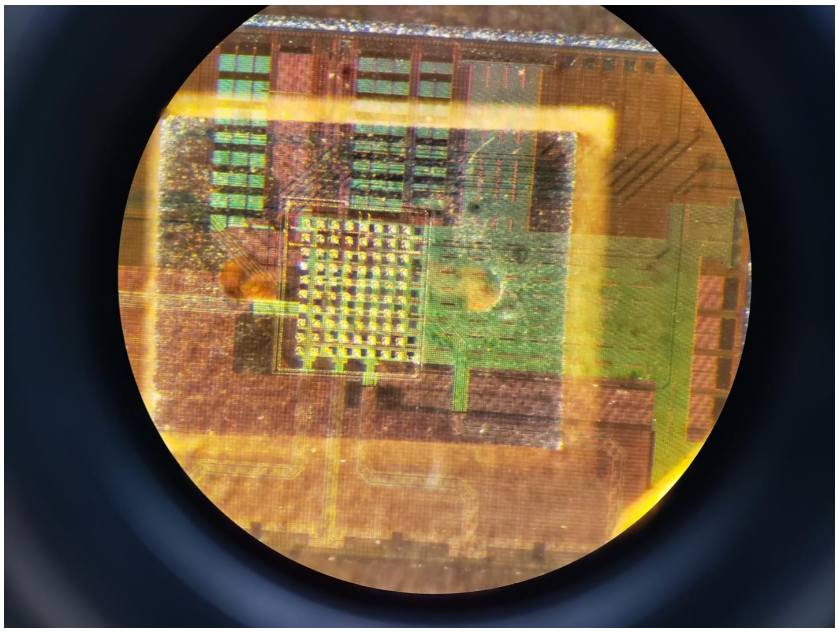

Figure 4.11: The overlay of the PIC and EIC showing the pad mismatch between the PIC and EIC. The PIC pitch was 100 µm and the EIC was 90 µm due to the 90 % linear shrink of the TSMC EIC. In the overlayed image, the EIC is bumped but the PIC is not bumped.

This prototype was ultimately unable to be assembled due to a fabrication issue. The TSMC 28 nm node is a 90% linear shrink of the TSMC 32 nm node, which was not accounted for when designing the EIC. As a result, the pads for the EIC were fabricated with a 90 µm pitch, meaning that assembly was not possible with the 100 µm pitch on the PIC. This can be seen in Figure 4.11, where the PIC and EIC microscope images are overlaid on top of each other. The EIC is shown with the microbumps whereas the PIC was not bumped. In the overlaid image, pads diverge, showing the pitch mismatch. While the 3D prototype was not able to be assembled, the knowledge gained from the assembly attempt allowed for a successful adjustment to be made for the following prototype – the second generation 2.5D integrated prototype.

4.2.2 MCM Transceiver – 2.5D Integration With Custom EICs

The second prototype pursued in the second generation of designs was a 2.5D integrated transceiver, similar to the 2.5D integrated transceivers in the version 1 prototype, but with cus-

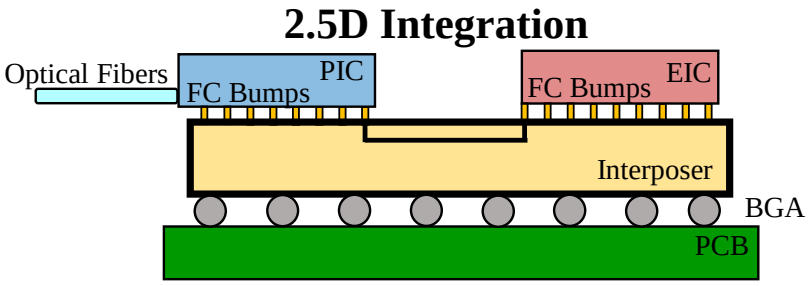

Figure 4.12: The side profile of the 2.5D integration approach. The PIC and EIC are flipped on top of the same silicon interposer, which interfaces to the PCB through TSVs.

tom EICs for both the transmitter and receiver, as shown in Figure 4.12. The RX EIC used for this transceiver is the same as the one outlined in the previous section. The TX EIC chip was also fabricated in a TSMC 28 nm HPC RF using the same MUSE Semiconductor MPW run. The chip was 1.0 mm by 1.0 mm and used 64 flip chip pads spread over the chip area with evenly spaced pads in an 8 by 8 orientation with a pad pitch of 100 µm.

The components within the low voltage (0.9V) TX EIC included two one chip PRBS generators for PRBS 2^7 and PRBS 2^{15} patterns, serialization, single-end to differential conversion, and a programmable output driver to adjust to the parasitics associated with the signal path to the photonic modulator. Like the RX EIC, the TX chip featured two data channels and one clock channel to clock forward along the interconnect to the RX chip. The TX targets low power consumption through the low supply voltage and the programmable output driver to adjust to the overall parasitics. The circuit diagram for the TX EIC can be seen in Figure 4.13.

The energy consumption for both the TX and RX EICs was simulated to be 2.2 pJ/b. This energy consumption in the EICs came from the clock distribution, serialization and deserialization (SERDES), TX driver, and RX analog front end (AFE). The clock distribution and SERDES were necessary for the transition from the compute node signals (2.5 Gbps) to the optical channel data rate (10 Gbps). The TX driver and RX AFE were necessary for the associated electric-optic and optic-electrical domain conversions. The energy consumption breakdown can be seen in Figure 4.14. The plurality of the energy consumption was due to the clock in the EICs, accounting for

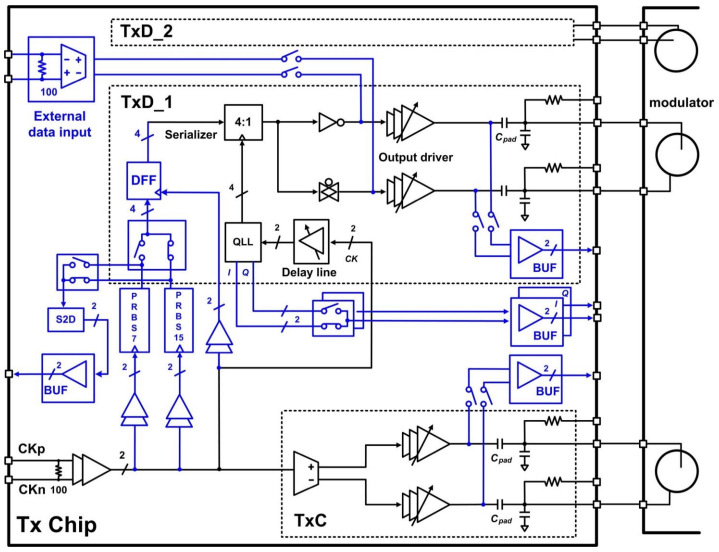

Figure 4.13: The circuit diagram for the TX EIC. The EIC features two data channels and one clock channel. The data path includes PRBS generators, serialization, and a tunable output driver.

essentially half of the overall energy consumption. The clock energy consumption was composed of the phase rotators, voltage controlled oscillator (VCO), in phase/quadrature (I/Q) correction, and the global distribution of the clock. The overview of the energy consumption can be seen in Figure 4.14.

The PIC for the 2.5D integrated version 2 prototype was designed to interface to two TX EICs and two RX EICs, for a total of four data channels and two clock channels, for a total of six channels for both the transmitter and receiver. The active PDK components were the same as the version 1 prototypes: microdisk modulators, demux microdisk filters, high speed photodiodes, and monitor photodiodes. Similar to the earlier 2.5D integrated version 1 prototypes, the TX portion of the PIC featured a bus waveguide with six microdisk modulators with 90-10 taps in between the microdisk modulators to provide signals for thermal stabilization for the modulators. On the RX portion, the PIC featured a bus waveguide with six microdisk demuxes with a 50-50 tap. One side wass routed to a monitor photodiode and the other was routed back to the chip edge. The electrical pads for the PIC were Al terminated and the densest pitch was 100 µm. The RF connections for the photodiodes and modulators were on the two edges of the PIC. Thermal DC connections were located closer to the center of the PIC, with all the thermal controls sharing a

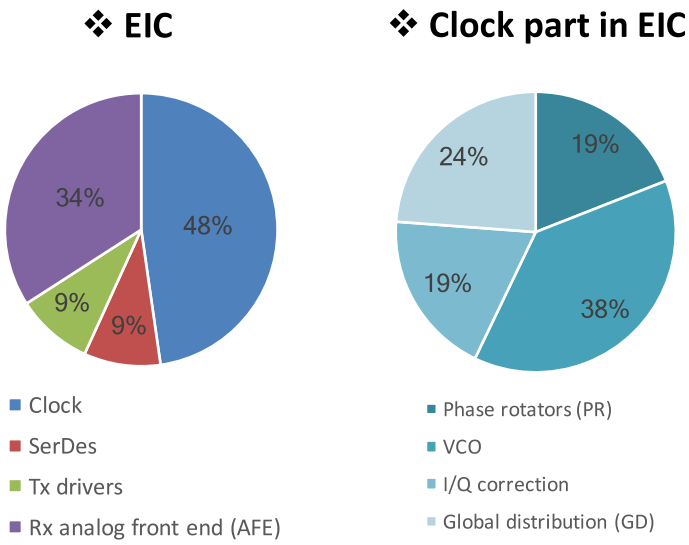

Figure 4.14: The simulated energy consumption for the custom TX and RX EICs. The clock routing is largely for the purpose of the SERDES, so combined the SERDES related components consume the majority of the power for the TX and RX EICs.

common ground with multiple pads interfacing to the common ground. Optical connection to the PIC was achieved through edge couplers on one edge of the PIC. In additional to the connections to the transmitter and the receiver, the edge couplers also featured loopbacks for alignment purposes. The arrangement of the edge couplers was three groups of three edge couplers. Within a group, the pitch of the edge couplers was 60 µm. Between the edge coupler groups, the pitch was 300 µm. The abnormal edge coupler arrangement was because the PIC was initially designed to interface to an interposer with SiN optical waveguides. The interposer would have had a slight trench that the PIC sat in such that PIC's edge couplers were aligned with the SiN waveguides. The abnormal edge coupler arrangement was so mechanical supports could be in between the three edge coupler groups. The waveguides on the interposer would be used to fan out the waveguides to edge couplers on the interposer at 127 µm pitch. We ended up not utilizing the trench version of the interposer and instead used the electrical-only interposer like the 2.5D integrated version 1 prototypes. In order to couple to the non-standard edge couplers, a waveguide array to fiber transposer (WAFT)

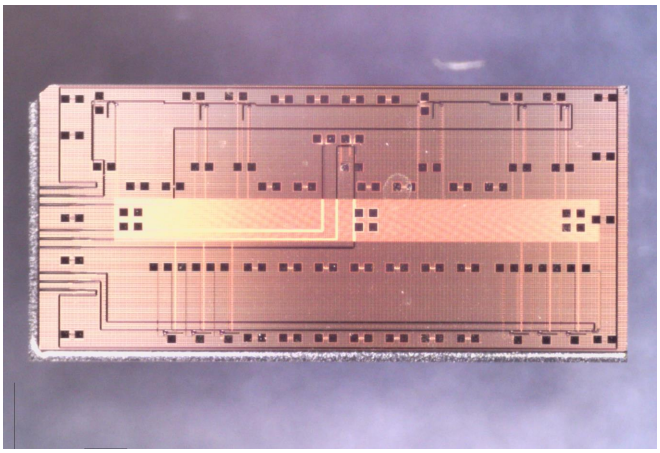

Figure 4.15: The PIC used in the generation 2 transceiver with 2.5D integration and custom EIC drivers. The optical edge couplers are on the left of the image. The middle portion is a common ground for the heater elements on the PIC.

was fabricated to translate from the fabricated pitch to a standard 127 µm pitch fiber array. In addition to transmitter and receiver, a single TX channel and a single RX channel were fabricated, each with separate waveguides and edge couplers. The PIC can be seen in Figure 4.15.

The interposer used in the 2.5D integrated version 2 prototype was the same interposer architecture as the 2.5D integrated version 1 prototype. The silicon interposer was approximately 100 µm thick with TSVs to provide connectivity between the front and the back of the interposer. The connectivity between the interposer and the integrated circuits was through stud bumps. Connection between the backside of the interposer and the PCB was through BGA type bumps at a 500 µm pitch. In the first prototype, only two EICs were designed to interface to the PIC: one TX EIC and one RX EIC. The separation between the PIC and each EIC was 300 µm, and the connection between them was through layer two Cu traces at 10 µm wide. Connections from the outputs of the EIC were routed on the interposer using CPW transmission lines using the layer one Al as the signal and layer three copper as the ground. The interposer GDS can be seen in Figure 4.16.

As mentioned in the previous section, the EIC was fabricated with 90 µm pad pitches due to TSMC 28 nm being a 90% linear shrink of the 32 nm node. This made assembly of the 3D

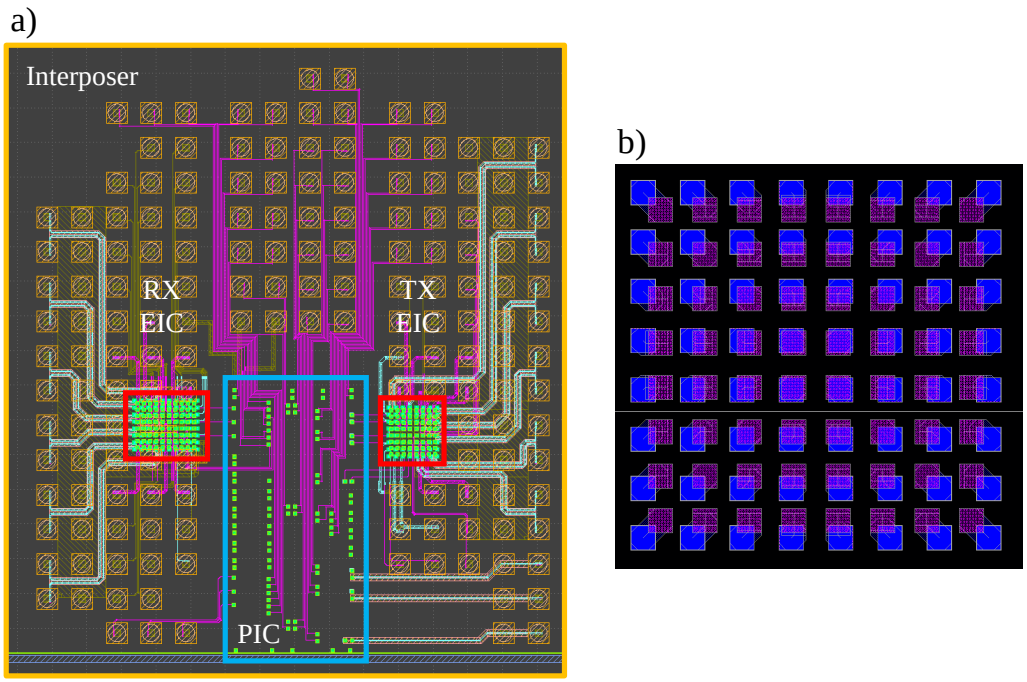

Figure 4.16: a) The GDS of the interposer used in the generation 2 transceiver utilizing 2.5D integration. The landing locations for the PIC, RX EIC, and TX EIC are labelled. b) A zoomed portion of the TX landing pads, showing the fan in using the additional metal layers to account for the 90% linear shrink of the EIC.

integrated receiver impossible. While the interposer was already partially fabricated by the time this issue was realized and altering the top metal layers was not possible, it was still possible to add additional metal layers on top of the already fabricated layers. Two extra metal layers and vias were added to the interposer to allow for fan in from the 100 µm pitch to the 90 µm pitch to allow the interposer to interface to the actual fabricated pitch of the EIC.

To account for the dense BGA bump pitch of the interposer, the PCB utilized six layers and via-in-pad. To maintain 50 Ω grounded CPW transmission lines, Rogers 4350B dielectric was used between the top signal layers and the ground layer. This was because Rogers 4350B offers thicknesses at 6.6 mils and 4 mils, which was necessary as the transmission line signals were necessarily narrow to interface to the 500 µm pitched BGA bumps. Close to the interposer, decoupling capacitors were surface mounted for the voltage supplies and other control signals for the EICs. Horizontal and vertical SMAs were used to interface to the high speed signals for the transceiver, both for data signals and debugging signals. DC signals were routed to the top of the

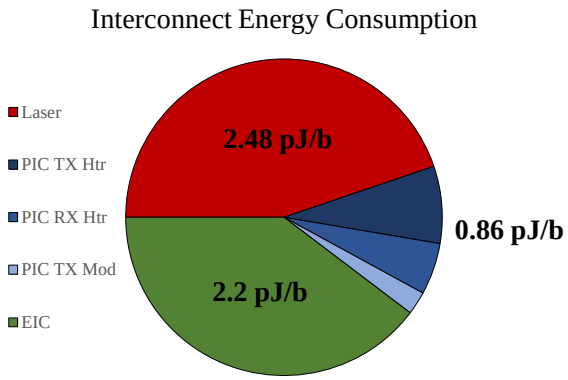

Figure 4.17: The estimated energy consumption of the generation 2 prototype, incorporating the simulation results from the transmit and receiver custom EICs.

PCB, where mezzanine connectors were used to connect to breakout boards for the PIC and EIC. The PCB also featured test points for all the connections on the PCB. The dense connections to the interposer constrained the RF connections for the transmission lines. Figure 4.18 shows the dense connections, and the resulting ADS simulations for a portion of the transmission lines. The channel closest to the board edge did see a slight degradation in transmission, but this is a debugging channel and the performance impact is minimal. It is important to note that the deserialization from the EICs will mean that the data signals propagating through the PCB will be at 2.5 Gbps, where the simulated transmissions show good performance. The PCB and related simulations for this prototype transceiver can be seen in Figure 4.18. For this 2.5D integrated version 2 prototype, all the components are fabricated except for the interposer.

4.2.3 MCM Transceiver Version 2 - Interconnect Energy Consumption

While the second generation MCM transceiver prototype has not completed fabrication, we are able to estimate the energy consumption based on the second generation components. Assuming a successfully repackaged MCM transceiver with 3 dB of insertion loss for edge couplers, the total passive optical loss will be 6.9 dB for the interconnect. Assuming the same receiver sensitivity would result in a 6.5 dBm required laser launch power, although it is expected that the sensitivity will be improved. With the effective wallplug efficiency of 18% results in a laser power consump-

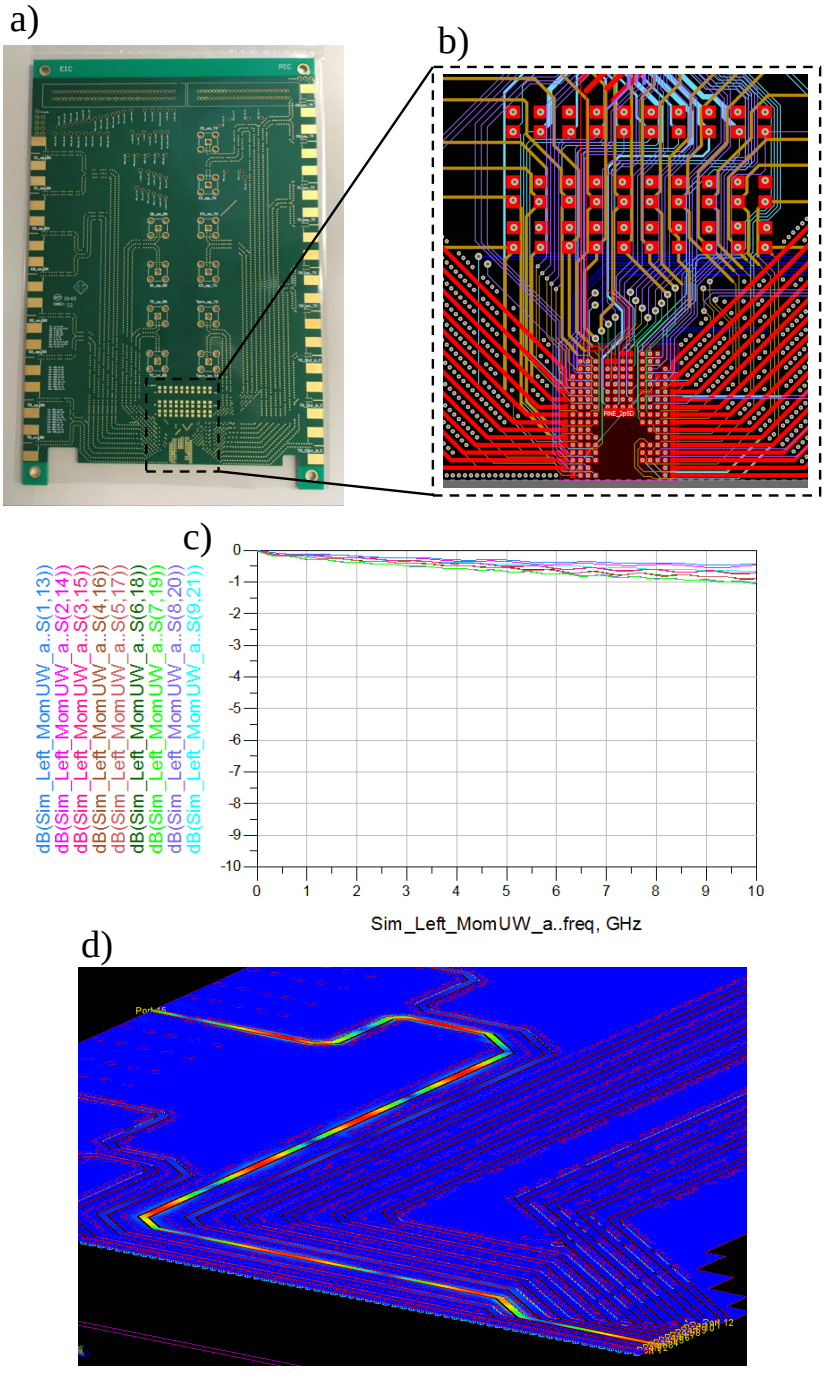

Figure 4.18: a) The fabricated PCB for the generation 2 prototype with 2.5D integration. b) The design of the PCB in Altium for the interposer landing location. The dense routing was a result of the 500 µm BGA pitch. c) The simulation for the RF transmission lines on the PCB for routing on the PCB. d) A simulation of one transmission line on the PCB.

tion of 24.8 mW. With the same PIC energy efficiencies, the power consumption is 8.61 mW for the TX and RX heaters, and for the charging and discharging of the modulator. With the custom EICs, the power consumption for both the TX and RX EICs was simulated to be 22 mW. With a 10 Gbps data channel, this results in a interconnect energy per bit of 5.54 pJ/b as shown in Figure 4.17. This marks a substantial improvement from the initial version 1 energy per bit of 20.91 pJ/b. The actual efficiency of the second generation 2.5D MCM could be even better if the receiver sensitivity of the custom EICs is better than the TI TIA sensitivity.

Part II

Silicon Photonic Transmitters

Chapter 5: Custom Microresonator Modulators

In this chapter we focus on the development of custom microresonator modulators. Custom modulators, as opposed to PDK modulators, are crucial to continuing to innovate in developing MCM silicon photonic transceivers. The number of unique resonances from PDK modulators is limited to what is offered within the PDK. For example, with the AIM Photonics PDK, there are currently four unique resonances for microdisk modulators within the C and L band [123]. Custom resonators allow for fabrication at arbitrary resonances, allowing the maximum number of channels per bus waveguide to be fabricated. Additionally, custom microresonator modulators provide a platform for further innovation. Modulators can be optimized according to the key parameters for the targeted performance for specific interconnects. Microresonator modulator parameters that can be optimized for include bandwidth, free spectral range, and energy efficiency. Three variations of custom microresonators are highlighted: microdisk modulators, racetrack modulators, and coupling modulators with varying junction types.

5.1 Custom Microdisk Modulators

Microdisk modulators are attractive for several reasons. They support landing contacts to the depletion diode in the middle of the microdisk, as shown in Figure 5.1a [151], removing the need to have a rib waveguide that is common for microring modulators to allow for contacts to be landed outside the microring, as shown in Figure 5.1b [152].

At tight bend radii, the optical mode will leak out through the partial etch portion of the rib waveguide, increasing the loss. Fabricating critically coupled microresonators requires low loss within the resonator, so when this bending loss of the rib waveguide becomes significant it becomes the limiting factor in reducing microresonator radius. The radius, along with the effective index,

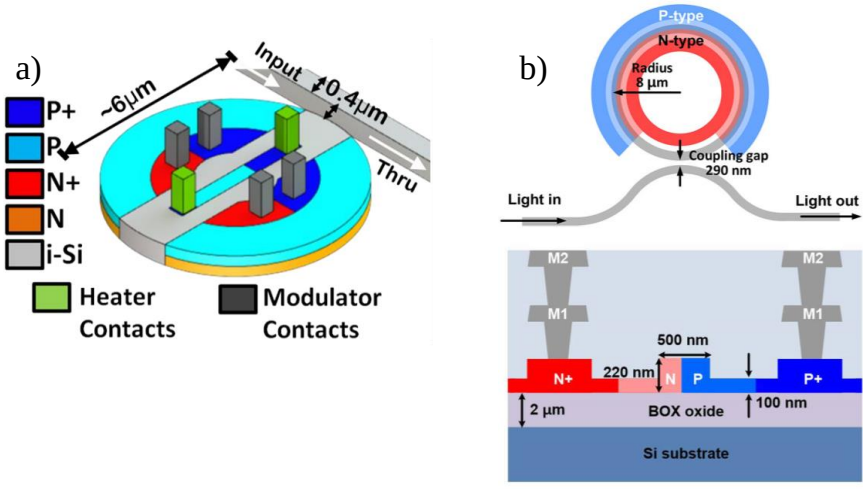

Figure 5.1: Examples of microresonator modulators. a) Shows a microdisk modulator with a vertical junction, where the P doped silicon is above the N doped silicon. Adopted from [151]. b) Shows a microring modulator with a horizontal junction, where the P doped and N doped silicon are side by side. Adopted from [152]. In both cases, the metal contacts are landed on the more heavily doped P+ and N+ silicon.

dictates the optical path length of the resonator. The optical path length of the resonator, L, impacts the free spectral range, FSR:

$$FSR = \frac{\lambda^2}{n_g L} \tag{5.1}$$

where λ is the wavelength and n_g is the group index. Therefore, a smaller microresonator radius corresponds to a larger FSR, which is beneficial since it allows more resonantor channels to be placed on a bus waveguide within the FSR of the modulator.

The other benefit of microdisks is that it allows for the junction to be a vertical one, where the P doped silicon to be on top of the N doped silicon (or vice versa). This allows for a larger junction to be fabricated, as waveguides in silicon are typically wider than they are tall–for example, a 220 nm tall and 500 nm wide waveguide. The larger junction means that the optical mode overlaps with more depletion region–which allows for a larger index change. Larger index changes correspond with higher modulation efficiencies, which allows for smaller modulator driving voltages.

Microdisk modulators do come with challenges, especially on the fabrication side. Fabricat-

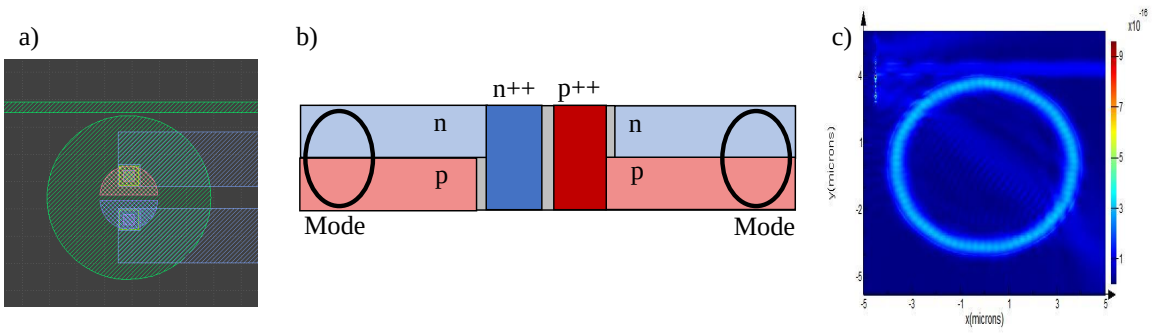

Figure 5.2: a) The GDS of the custom microdisk modulator, where the silicon is shown in green. b) The side profile of the custom microdisk modulator. c) The Lumerical simulation of the microdisk. In hindsight, the mode shown is likely not the fundamental mode.

ing a vertical junction is more difficult compared to a horizontal junction, and a vertical junction will likely require more development time with a higher development cost. Additionally, as the microdisk is essentially a wide waveguide it will support more optical modes beyond the fundamental mode. A microdisk modulator requires careful design to only excite the fundamental mode, which can be achieved with an adiabatic taper.

An example of a custom microdisk we fabricated can be seen in Figure 5.2. The GDS in a) shows the microdisk without the P and N doping windows for clarity, with the red and blue portions in the center representing the N++ and P++ doping. The side profile can be seen in b). The Lumerical simulation showing the microdisk being excited can been seen in c). Multiple devices were fabricated with different coupling gaps to account for fabrication variations, and because there was interest in both over coupled and critically coupled microdisks. The fabricated diameters ranged from 6 µm to 12 µm and the coupling gap ranged from 100 nm to 200 nm.

The full spectrum of a near critically coupled fabricated microdisk can be seen in Figure 5.3. The seemingly random resonances were evidence that multiple modes were excited within the microdisk, as the coupler between the bus waveguide to the microdisk was not adiabatic. The different modes had different losses, which was why they varied in terms of ER (or in other words, how close they were to critical coupling–which occurs when the coupling rate is equivalent to the loss rate). The different modes also had different refractive indexes, which was why the resonances

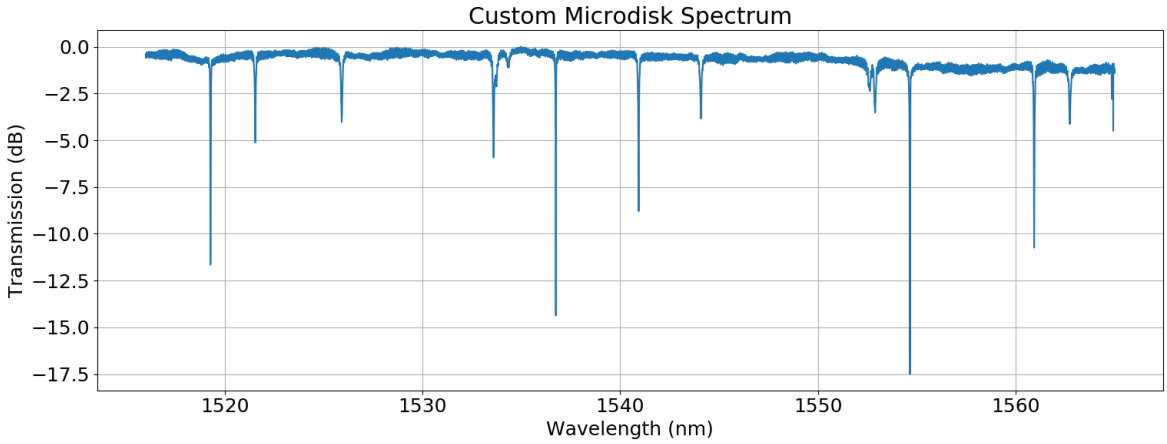

Figure 5.3: The optical spectrum of a sample custom microdisk. The resonances do not show an even FSR or ER. This is likely due to multiple optical modes are being excited within the microdisk.

for the different modes occured at different wavelengths. The fact that multiple modes were excited made this microdisk less useful for WDM transceivers coupled to bus waveguides. Normally, the fabricated resonances for the microdisks coupled to the bus waveguide would be spread out in between the resonances of one particular modulator. With the multiple modes excited within the microdisk, the spectrum would have resonances corresponding to the higher order modes, which would likely lead to significant crosstalk between channels.

The response of a fabricated over coupled microdisk can be seen in Figure 5.4. The ripples in the spectrum were in part due to the fiber array being relatively far away from the edge couplers due to a ledge on the PIC. As the microdisk's modulator was pushed into injection up to 1.0 V forward bias, the resonance moved to lower wavelengths and the extinction ratio of the microring increased. The presence of free carriers reduced the index of refraction and increased the optical loss. Reducing the index of refraction pushed the resonance to lower wavelengths. The fact that increased injection increased the extinction meant that initially the coupling rate was larger than the loss rate (in other words, over coupled), as increasing the loss in the microdisk pushed them to being equal. Increasing the injection voltage beyond 1.0V reduced the extinction ratio and pushed the resonance to higher wavelengths. This was because the heat generated from the

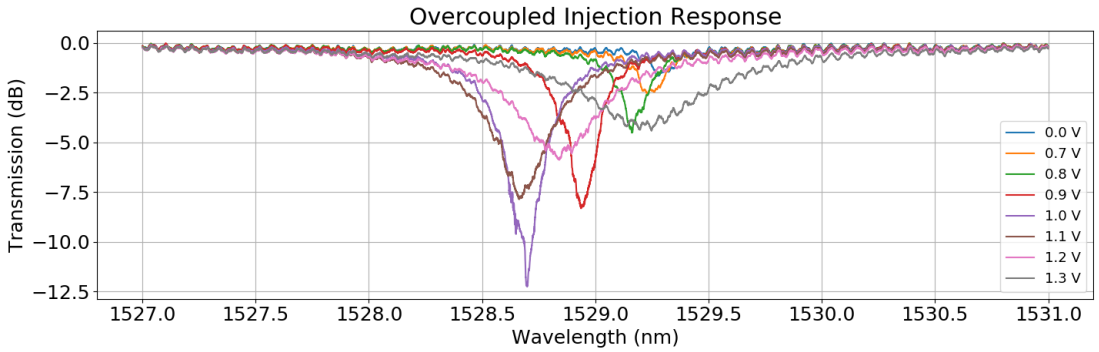

Figure 5.4: The resonance response of an over coupled microdisk. As is shown, increasing the injection voltage causes the resonance to lower wavelengths and higher extinction ratio as the injected carriers lower the effective index and increase the loss in the microdisk. At 1.0 V, the microdisk is critically coupled, and continuing to inject more carriers causes the loss to dominate over the coupling to lower the extinction ratio. The resonance moves back to higher wavelengths as the heat generated from the PN diode operating in forward bias results in a thermally driven increase in effective index that dominates over the carrier response.

diode in injection produced a thermo-optic increase in index that dominated the reduction in index from increased carriers. The extinction ratio was reduced because the extra carriers from injection continued to introduce more loss into the microdisk.

The microdisks in this generation did not have a depletion response–high speed or DC. While we initially believed the PN junction in the MPW process to be a vertical junction, it was in fact a horizontal junction. As a result, the design of custom microresonator modulators was shifted to microring modulators.

5.2 Custom Racetrack Modulators

After learning that the junction was a horizontal junction, the next custom modulator design we pursued was a racetrack modulator. Since the racetrack modulator was larger than a typical microring resonator, the FSR was smaller. However, this device was intended to verify the performance, rather than optimize for parameters, such as increased FSR. The racetrack design allowed the transition from ridge to rib waveguide to occur within the racetrack, as can be seen in Figure 5.5. This was beneficial, as the design rules for minimum space for the partial etch silicon would require the coupling gap between the bus waveguide and the racetrack to be larger than 500 nm

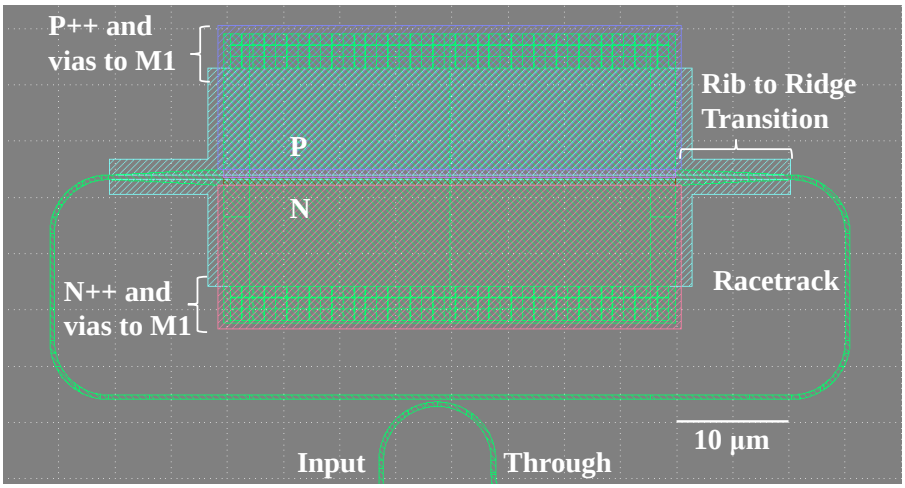

Figure 5.5: The GDS for the custom horizontal junction racetrack modulator. The GDS shows the location of the P, N, P++, N++ doping, as well as the coupling region to the bus waveguide and the transition from rib to ridge waveguide.

if the transition from ridge to rib waveguide occurred outside the racetrack. Additionally, we did not need to worry about excess bending loss from the rib waveguide at too small of bend radii, as the PN junction occupied a straight portion of the racetrack. The structure of the PN junction for the racetrack was similar to Figure 5.1b, with the P and N doping occupying the full height of the silicon waveguide. Etched silicon doped with P and N was used to fan out the junction to full height silicon doped with N++ and P++, which allowed vias to be landed from the above metal layer. The PN junction within the racetrack was 40 µm, and multiple designs were fabricated with coupling gaps ranging from 100 nm to 350 nm.

The depletion resonance response for one of the approximately critically coupled racetrack modulators can be seen in Figure 5.6. The extinction ratio of the optical resonance was approximately 15 dB. The DC reverse bias response was tested up to 6 V, and exhibited a 5 pm/V modulation efficiency. This modulation efficiency is low and would be a barrier to energy efficient modulation. The current highest modulation efficiency for a silicon photonic microresonator modulator is a microdisk modulator with 250 pm/V [111]. For a microring resonator to be suitable for high speed modulation, the modulation efficiency should be on the order of 10-40 pm/V [153, 154, 155]. For this racetrack modulator, the PN junction only occupied approximately one fourth of the

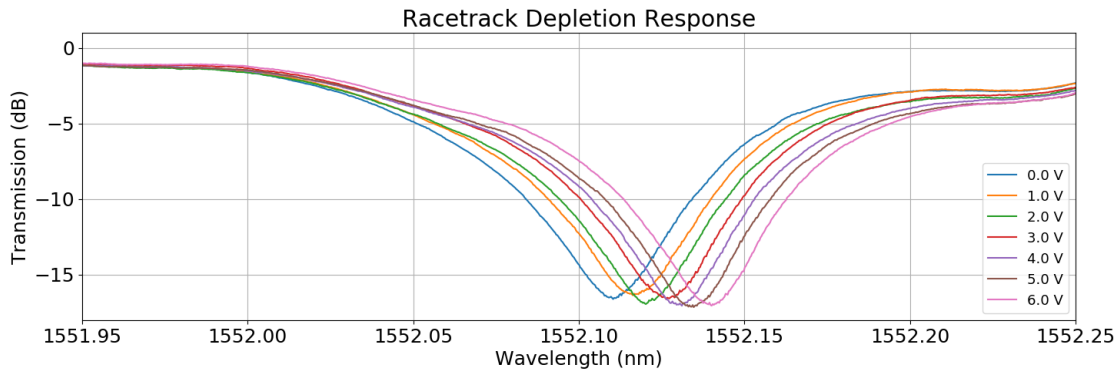

Figure 5.6: The resonance response of the racetrack modulator operating in depletion. Increasing the reverse voltage increases the width of the depletion region, reducing the carrier concentration overlapping with the optical mode, pushing the resonance to higher wavelengths.

racetrack's path length. The resonance wavelengths of a microresonator can be expressed as:

$$\lambda_{\text{res}} = \frac{n_{\text{eff}} L}{m} \tag{5.2}$$

where n_{eff} is the effective index, L is the resonator's path length, and m is an integer value that corresponds to the number of wavelength multiples to equal a 2π phase shift through the path length of microring. If the PN junction were to occupy the full racetrack, then $\Delta n_{\text{eff}} L$ would be four times as large, which would result in an estimated modulation efficiency of 20 pm/V. Looking at Equation 5.2, it would appear that increasing the microresonator size would increase the modulation efficiency. However, that is not the case, as an increased L will correspond to a proportionally increased m for the resonance occurring at approximately the same wavelength, so a Δn_{eff} produces the same $\Delta \lambda_{\text{res}}$ as the smaller microring, as the L and m scale together for a given λ_{res} of interest.

The racetrack modulator's bandwidth can be seen Figure 5.6a, along with the qualitative response in Figure 5.6b. While the 3 dB bandwidth was below 10 GHz, there exists a number of approaches to improve the bandwidth, as the purpose of this device was to demonstrate functionality rather than optimize performance. Moving the more highly doped P++ and N++ closer to to the waveguide would reduce the series resistance. Moving to smaller modulators would reduce the

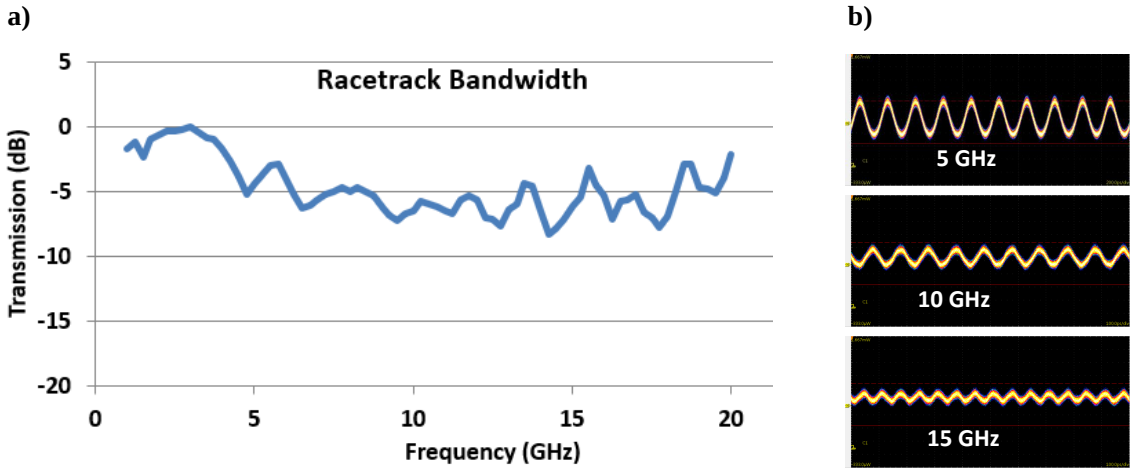

Figure 5.7: a) The bandwidth of the custom racetrack modulator, shown up to 20 GHz. b) Example sine waves at different driving frequencies for the racetrack modulator.

junction capacitance (in addition to increasing the FSR). These approaches would both reduce the RC time constant. To increase the modulation efficiency, the PN junction could be placed around the full microring, and different junction approaches could be explored to increase the mode overlap with the depletion region.

5.3 Custom Coupling Modulators with Varying Junctions

The next iteration of custom modulators focused on a coupling modulator base structure, similar to the base structure outlined in [156]. The majority of the microresonator modulators discussed previously operated by inducing an intracavity change in the free carrier concentration, which changed the resonance condition, allowing a laser wavelength to modulate between being on and off resonance. The coupling modulator instead varies the coupling strength between the bus waveguide and the microresonator, so the microresonator can modulate between under coupled and critically coupled. This is achieved by essentially introducing a MZM to the resonator, with the bottom input and bottom output of the MZM connected together to form a resonator, as shown in Figure 5.8. By modulating the phase difference between the two arms, the portion of the optical input that couples into the cavity can be modulated, thus modulating the coupling strength of the bus waveguide to the resonator. The bandwidth of high Q intracavity resonators can be limited

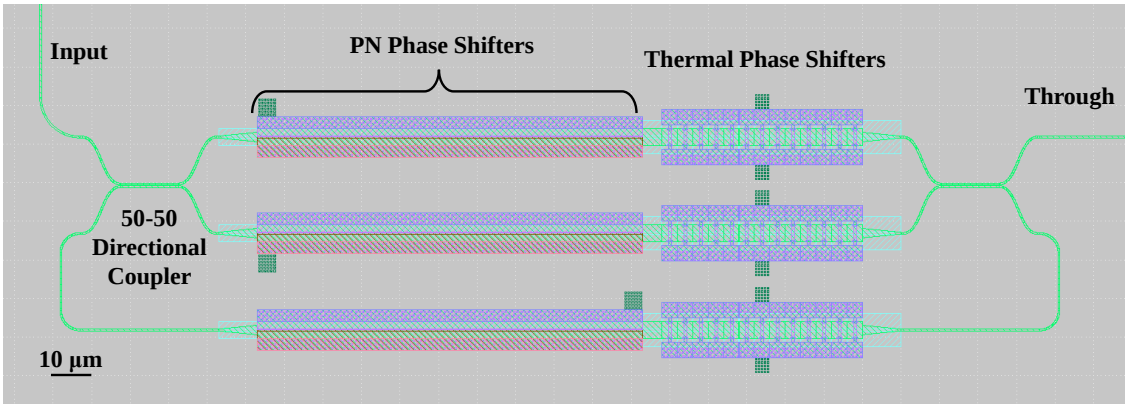

Figure 5.8: The GDS of the custom coupling modulator. The custom PN phase shifters, thermal phase shifters, and directional couplers can be seen. Six different variations of PN phase shifters were fabricated.

by the cavity's photon lifetime. Coupling modulation avoids this issue, allowing higher achievable bandwidths for high Q resonators [156]. However, the MZM within the resonator results in a larger cavity size, increasing the modulator's footprint and reducing the modulator's FSR.

Multiple designs were fabricated, with different high speed PN phase shifters. As noted in the previous section, the modulation efficiency for a normal lateral PN junction occupying the full resonator is expected to be approximately 20 pm/V. The different junctions can be seen in Figure 5.9. The arrow represents the waveguide path where the silicon was the full 220 nm height. The etched silicon allowed the junction to be connected to highly doped N++ and P++ to land contacts. The first type of junction was the same lateral junction used in the racetrack modulator in the previous section. The second junction was an interleaved (or striped) junction at a 1 µm period. This junction could allow for a larger overlap of the optical mode with the depletion region. In [154], an interleaved microring resonator with a 600 nm period produced a modulation efficiency of 40 pm/V. The third junction combined the lateral and striped junctions to produce a snaked junction, which could provide the largest overlap of the optical mode with the depletion region. The period of the snaked junction was 1 µm. In addition to the three junction types outlined, three more junction types were also fabricated. The three additional junctions followed the same structure as the previous three junctions, but the P and N doping were replaced with P+ and N+, respectively. This

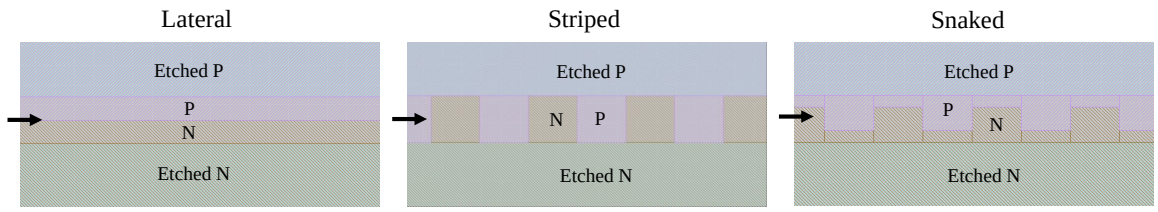

Figure 5.9: The three different horizontal PN junctions that were fabricated, viewed from above. For each variation, a PN and P+N+ version was fabricated.

would allow for a larger change in free carrier concentration during modulation, as the initial doping concentration was higher, which would produce higher modulation efficiencies. The tradeoff was that higher carrier concentration would introduce more loss and result in a higher insertion loss for the modulator. The increased loss in the cavity from the PN phase shifter would also reduce the Q of the resonator.

These custom coupling modulators will allow the a comparison to be made between the junction types. Additionally, they will provide a platform to perform an analytical comparison for the intermodulation crosstalk between a coupling modulator and an intracavity modulator. Previous work comparing a silicon microring intracavity modulator and a graphene assisted silicon nitride coupling modulator showed that the intermodulation crosstalk for the coupling modulator was lower due to the static resonance, allowing for denser WDM channel placement [157]. These coupling modulators will allow for a more direct comparison, as the same phase shifters were used for both the coupling modulation and intracavity modulation.

In order to support the fabrication of the coupling modulators, several additional custom components were fabricated. One was a custom 50-50 directional coupler. The PDK component 50-50 directional coupler was relatively long. To support smaller FSRs for the custom modulator, the custom modulator was designed to be approximately 30 µm long. The design can be seen in Figure 5.10a, with the simulated performance showing even power splitting at 1550 nm in Figure 5.10b. The FDTD simulation from Lumerical at 1550 nm can be seen in 5.10c.

The second custom component was a thermo-optic phase shifter. Similar to the custom directional coupler, the motivation for the custom thermal phase shifter was a shorter length than the

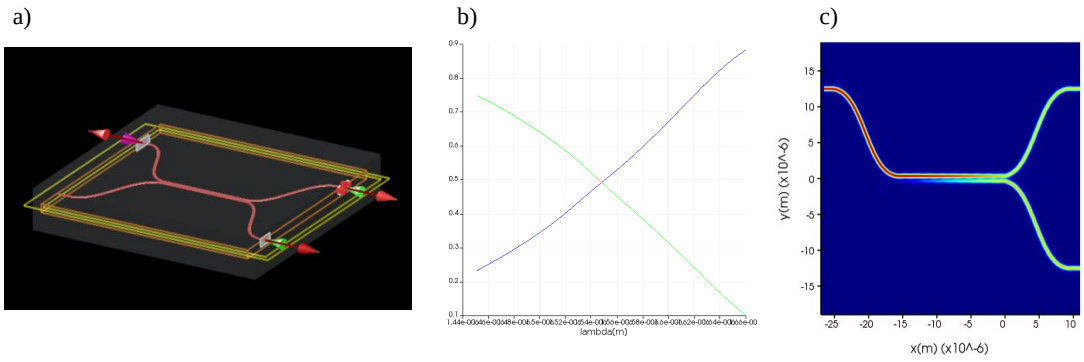

Figure 5.10: The custom direction coupler that was fabricated for the custom coupling modulator. a) The 3D model of the directional coupler. b) The transmission for the two outputs for the directional coupler, as simulated through Lumerical. c) The mode amplitude simulation for the directional coupler at 1550 nm.

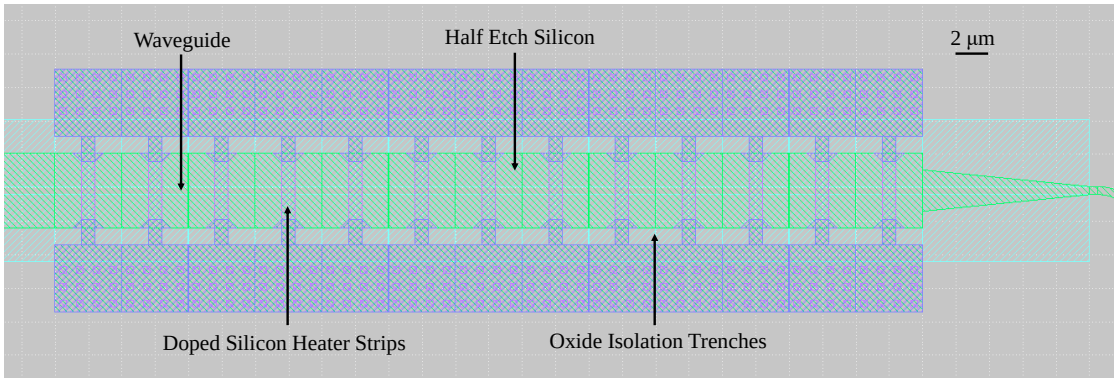

Figure 5.11: The GDS of the custom thermal phase shifter that was fabricated for the coupling modulators. The doped silicon heater strips and rib to ridge waveguide transition can be seen.

existing PDK thermal phase shifter to allow for a larger FSR. The heater design was modelled after the design in [158] and can be seen in Figure 5.11. The heater design featured doped silicon heater strips crossing the waveguide to provide the resistive component for heat generation when a voltage is applied across. To increase the heat confinement, and therefore increase the heater tuning efficiency, oxide isolation trenches were placed on either side of the waveguide. The custom coupling modulators are expected back from fabrication in July 2020.

Chapter 6: Higher Order Modulation Transmitters

While our preferred approach for scaling transceivers is to increase the channel counts to keep energy consumption low, the more common approach is to increase channel data rates, either through increasing the baud rate or through increasing the number of bits per symbol with higher order modulation formats. In this chapter, we present our efforts towards developing and utilizing silicon photonic higher order modulation format modulators. These efforts include developing a self-optimizing PAM-4 Mach Zehnder modulator, exploring the potential for generating arbitrary QAM constellations with only two microring modulators, and designing microdisk based QAM-16 and PM WDM QPSK modulators.

6.1 A Self-Optimizing PAM-4 Mach-Zehnder Modulator

In this section, we demonstrate four channel PAM-4 modulation in a silicon photonic platform driven by push-pull binary electrical signals. The subsystem self-optimizies through a gradient descent algorithm across the full range of starting voltages.

6.1.1 Introduction

Silicon photonic devices offer the potential for improving traditional electronic interconnected systems in terms of energy consumption, footprint, and bandwidth [159, 160]. The bandwidth density of a silicon photonic system can further be improved by employing advanced modulation formats, such as quadrature amplitude modulation (QAM), quadrature phase shift keying (QPSK), and pulse amplitude modulation (PAM). PAM-4 has been demonstrated in silicon modulators and is an attractive modulation format due to a two times bandwidth density advantage compared to on-off keying (OOK) while still allowing for direct detection [161]. Optical PAM-4 can be generated

by driving a device with a 4-level electrical pattern generator, or by driving in push-pull mode with two binary electrical patterns [162].

A significant concern with any modulation format is actively tuning and maintaining optimal signal quality. Systems that can automatically self-optimize signal quality offer the benefit of ease-of-use and repeatability, with the potential for scaled integration into larger systems. Previous work has explored optimizing OOK modulation with BER monitoring [163], but the complexity of self-tuning increases as the modulation formats become more advanced.

This work investigated the increased bandwidth of WDM with PAM-4. The result was a subsystem that achieved binary drive PAM-4 and self-optimized using a gradient descent algorithm executed on an external, software-programmable system.

6.1.2 Device

The device consisted of four concurrent MZMs, spatially multiplexed using two stages of MZIs. Each arm of the four MZMs contained a PN junction operated in depletion mode with fully independent differential drive and a thermal control. The PIC can be seen in Figure 6.1a. The device was electrically packaged in a high-speed chip carrier with gold wire bonds and optically packaged using a 5-port optical grating coupler epoxy-bonded at surface normal. The packaged device was mounted on a printed circuit board with connected breakouts for control of both high-speed and DC-biased electrical contacts, as seen in Figure 6.1b.

6.1.3 Experimental Setup

Figure 6.2a depicts the experimental setup. Two tunable lasers were polarized and injected into two MZMs. The WDM output was amplified using an erbium-doped fiber amplifier (EDFA) followed by an optical grating filter, and finally sampled on a digital serial analyzer (DSA).

Two electrical OOK data streams were driven on both arms of a single MZM using a PPG with PRBS $2^{31} - 1$ data and were DC-biased using DC voltage supplies. The signals were phase-aligned using electrical delays to ensure push-pull operation, and were driven with different voltage

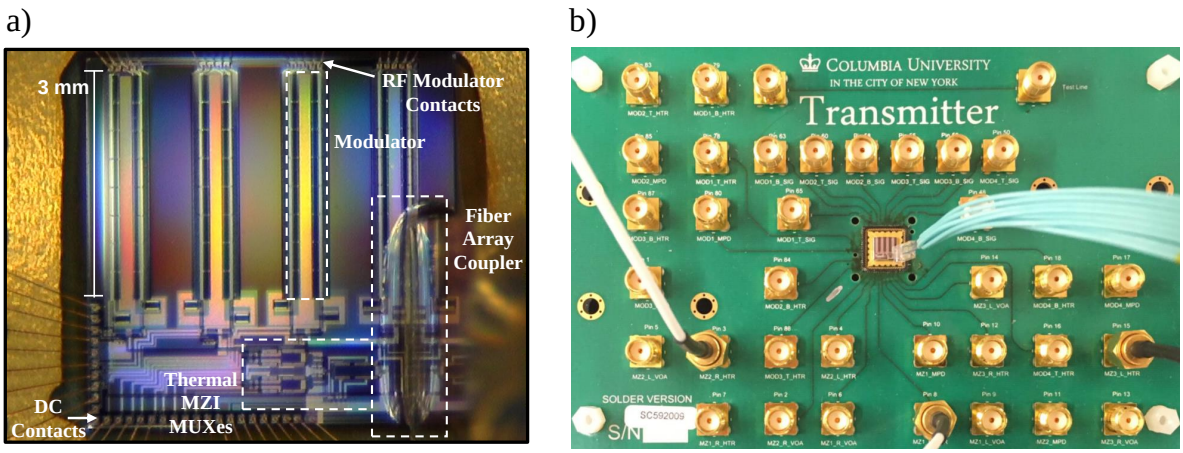

Figure 6.1: a) An image of the wirebonded four channel MZM transmitter PIC. The device is approximately 3 mm by 3 mm and includes the MZI modulators and MZI thermal muxes. b) The PCB, QFN package which houses the PIC, and fiber array.

amplitudes to create the PAM-4 modulation. One driving voltage was delayed with respect to the other to ensure the two arms were not correlated. Static voltages for the MZI and MZM bias heaters were provided via DC voltage supplies. A control layer was implemented using GPIB interfaces and a Python script orchestrated the control of the PPGs, DSA, and DC voltage sources.

6.1.4 Gradient Descent Optimization Algorithm

The self-optimizing algorithm was based on a two-dimensional gradient descent using real-time data from the DSA. The data was processed by applying a scaling metric, after which the control logic separated and histogrammed 8000 data points into 50 bins. The PAM-4 signal levels corresponded to the four largest peaks in the histogram. An objective function was calculated according to the following:

$$\Theta = \frac{1}{(L_4 - L_3)^{1.5}} + \frac{1}{(L_3 - L_2)^{1.3}} + \frac{1}{(L_2 - L_1)^{1.0}} \tag{6.1}$$

The various levels of the PAM-4 signal in terms of optical power were represented by the variable L, with L_4 corresponding to the level with the largest optical power. These exponent values produced the most symmetrical levels across several heuristic trials. Bias voltages with

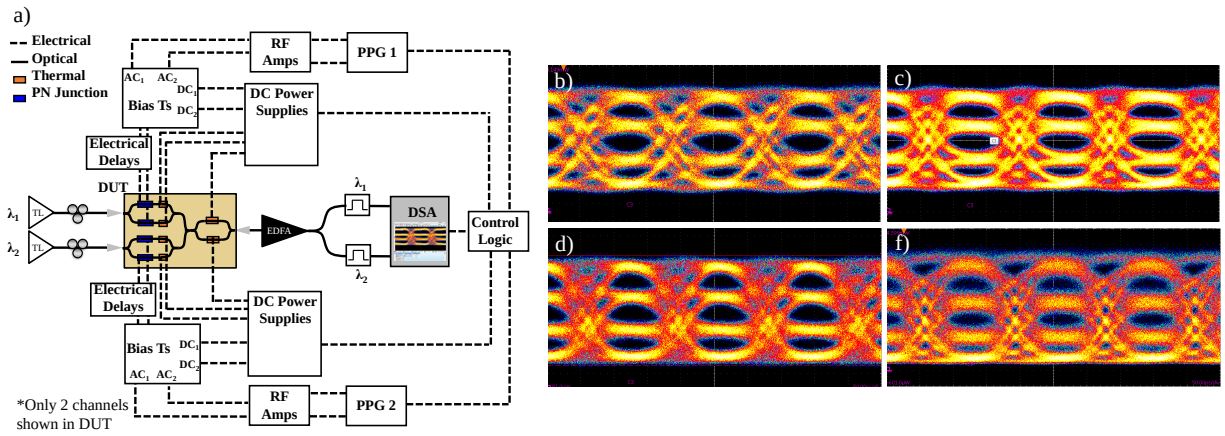

Figure 6.2: a) The experimental setup, depicting the control subsystems for two channels of the device. b-f) PAM-4 signals at 7.5 Gbaud/s for each of the four modulator channels.

PAM-4 levels that were close together would result in a large objective function. This approach allowed us to evenly space the PAM-4 levels as we minimized the objective function.

Each iteration of the gradient descent involved multiple steps, depicted in Figure 6.3. First, the updated voltage was applied, and the objective function was calculated. Then, the voltage was probed in one dimension, which meant that either the top or bottom PN junction was either increased or decreased by 0.1 volts. The objective function was again calculated, and the driving voltage was adjusted as shown in Equation 6.1. The process was repeated for the other PN junction. For each iteration, the order of the modulators and whether the probe voltage was positive or negative was randomly selected. This randomization allowed the objective function to decrease faster, as the algorithm appeared more effective when it was probing in the direction of descending gradient.

$$V = V - \eta \nabla \Theta(V) \tag{6.2}$$

The voltages for the next iteration were calculated by subtracting the gradient, scaled by a step size η, from the current voltages. The step size was ± 0.05, with sign determined by the probing voltage polarity. The gradient descent converged faster when each voltage dimension was probed and updated separately.

```
1   i = 0
2   while (i < number_iterations) do
3       initialize_probe_directions()
4       apply_volt(v_top[i], v_bot[i])
5       hist_data = histogram(trace_data)
6       peaks = find_peaks(hist_data)
7       obj[i] = calculate_obj(peaks)
8       apply_volt(v_top[i] + v_probe, v_bot[i] + v_probe)
9       hist_data = histogram(trace_data)
10      peaks = find_peaks(hist_data)
11      obj_temp = calculate_obj(peaks)
12      v_top[i+1], v_bot[i+1] = update_volts(v_top[i], v_bot[i], obj[i], obj_temp)
13      i = i + 1
```

Figure 6.3: Simplified psuedo code for the PAM-4 self-optimization algorithm.

If the control system was unable to find four prominent peaks, then this gradient descent could not be performed. In the case where four prominent peaks were not found in one section of an iteration, the objective function was symbolically set to 100, and the voltage settings were restored to the previous state with four sufficient peaks. In the case where four prominent peaks were not found across all the steps of an iteration, the voltages were randomized to move to a different location in the voltage space on the next iteration.

6.1.5 Optimization Data

The system encountered one of two initial conditions: a signal with four prominent peaks (sub-optimal), or one without four prominent peaks (unidentifiable). The data for a sub-optimal starting position can be found in Figure 6.4. The gradient descent algorithm ran for 50 iterations for each of the 20 trials. The objective function decreased sharply in the first 10 iterations. The standard deviation for both the final voltages was approximately 0.2 volts. The data from an unidentifiable starting position is shown in Figure 6.5. By about iteration 15, nearly all of the 20 trials identified a voltage combination with four distinct peaks, and the objective function could be appropriately optimized. The two later spikes were cases when the algorithm was unable to identify four prominent peaks, and jumped to an objective function of 100 before restoring to the

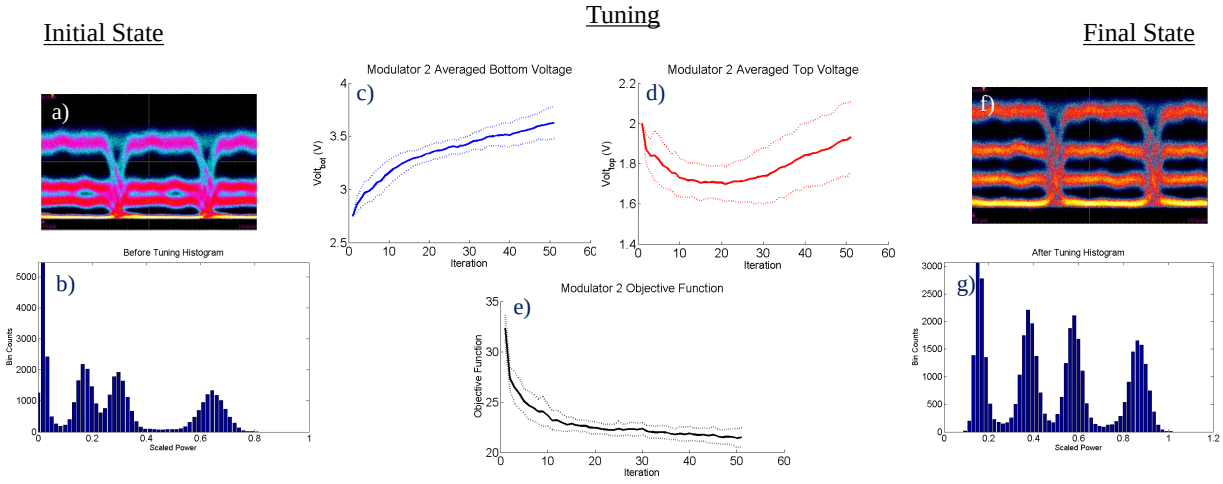

Figure 6.4: 20 repeated trials for suboptimal starting position tuning for modulator 2. a) The waveform before tuning. b) A histogram before tuning. c) The averaged bottom PN voltage with standard deviation. d) The averaged top PN voltage with standard deviation. e) The averaged objective function with standard deviation. f) The waveform after tuning. g) A histogram after tuning.

previous voltage state.

Simultaneous tuning of multiple modulators was less reliable than tuning a single modulator. With dual tuning, the heat from thermal tuning on one modulator affected the thermal tuning of a different modulator. Additionally, the EDFA in the setup resulted in output power of the two wavelengths proportional to the input power of the two wavelengths. As a result, if tuning on one modulator resulted in a change in average power, then the ratio of the power of the two wavelengths would change, and so the output power of the non-adjusted channel was also affected.

The tuning for these cases was done at 2 Gbaud/s. The voltage levels were still optimized when the frequency was increased to 7.5 Gbaud/s. The optimized PAM-4 modulation for all four channels is shown in Figure 6.2b-f. Error free operation (BER < 10^{-12}) with OOK was achieved on all channels with simultaneous modulation.

6.1.6 Conclusion

We demonstrated four channel PAM-4 modulation driven by binary electrical signals in a push-pull manner. A WDM signal was transmitted through a SiP transmitter chip that self-tuned to an

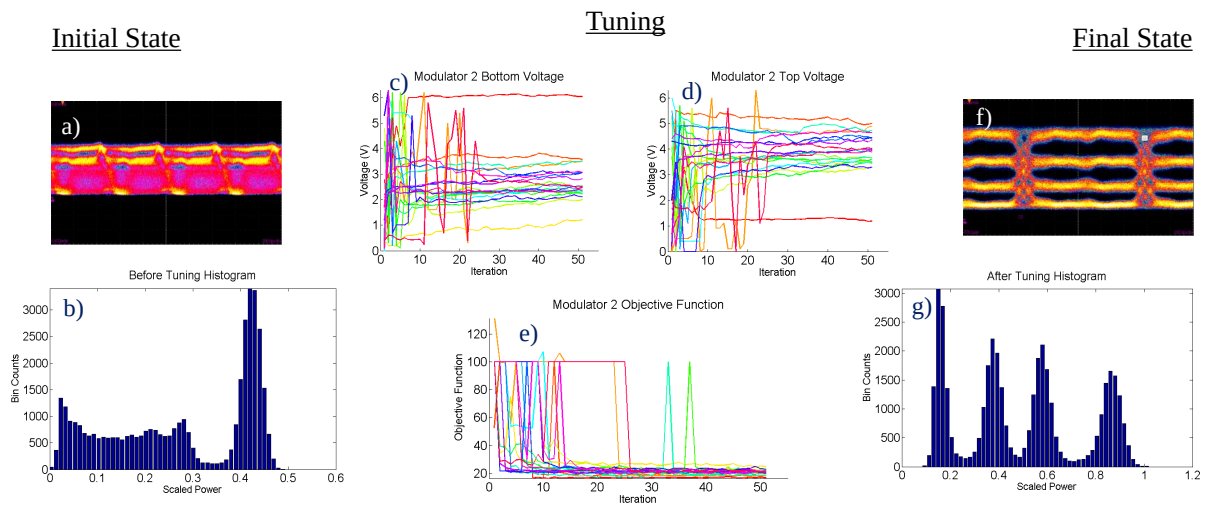

Figure 6.5: 20 repeated trials for unidentifiable starting position tuning for modulator 2. a) A waveform before tuning. b) A histogram before tuning. c) The bottom PN voltage. d) The top PN voltage. e) The objective function. f) The waveform after tuning. g) A histogram after tuning.

optimal bias point via the gradient descent algorithm. This process allowed for improved modulation along each data channel, a proof-of-concept that greatly optimized signal recovery of higher-order data modulation formats.

6.2 Two Ring Modulator Arbitrary QAM Constellations

One of the motivations for developing custom microring modulators was to provide a path towards fabricating strongly over coupled microring modulators. This was attractive as it was necessary towards fabricating an arbitrary QAM constellation modulator using only two microring modulators. QAM is quadrature amplitude modulation and is a higher modulation format that incorporates amplitude and phase to increase the number of bits per baud. QAM is typically generated by adding two modulated carrier waves together–the carrier waves are the same frequency but out of phase by $\pi/2$ [164]. Microrings represent an alternative approach to generating QAM signals, due to the fact that a microring coupled to waveguide affects both the amplitude and phase of light propagating through the waveguide, and that the manner that the microring affects the light varies on the strength of the coupling between the waveguide and the microring. A strongly

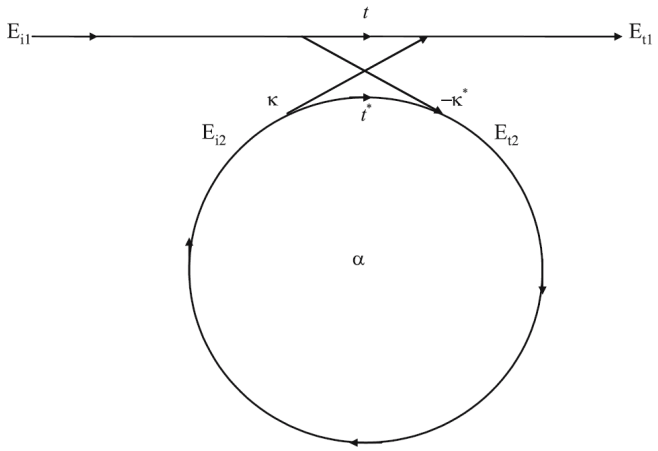

Figure 6.6: A model of a ring resonator. In the model, t and k are coupling strength parameters, E is mode amplitude, and α is loss. Adopted from [166].

under coupled microring impacts the amplitude and phase minimally. A critically coupled microring impacts the amplitude and phase substantially. A strongly over coupled microring impacts the amplitude minimally and the phase substantially [165]. The model for the waveguide and ring resonator can been seen in figure 6.6.

In this model, t and k are coupling parameters, the E parameters correspond to complex mode amplitudes, and α represents the loss of the ring with no loss corresponding to one. The transmitted complex mode amplitude can be represented as:

$$E_{t1} = \frac{-\alpha + t\mathrm{e}^{-\mathrm{j}\theta}}{-\alpha t^* + \mathrm{e}^{-\mathrm{j}\theta}} \tag{6.3}$$

where θ corresponds to the accumulated phase from one round trip through the ring and can be represented as:

$$\theta = \frac{wL}{c} = \frac{4\pi^2 n_{\mathrm{eff}}}{\lambda} \tag{6.4}$$

In this equation, w is the angular frequency, L is the circumference of the ring, c is the mode's phase velocity, r is the ring radius, λ is the vacuum wavelength, and n_{eff} is the effective refractive

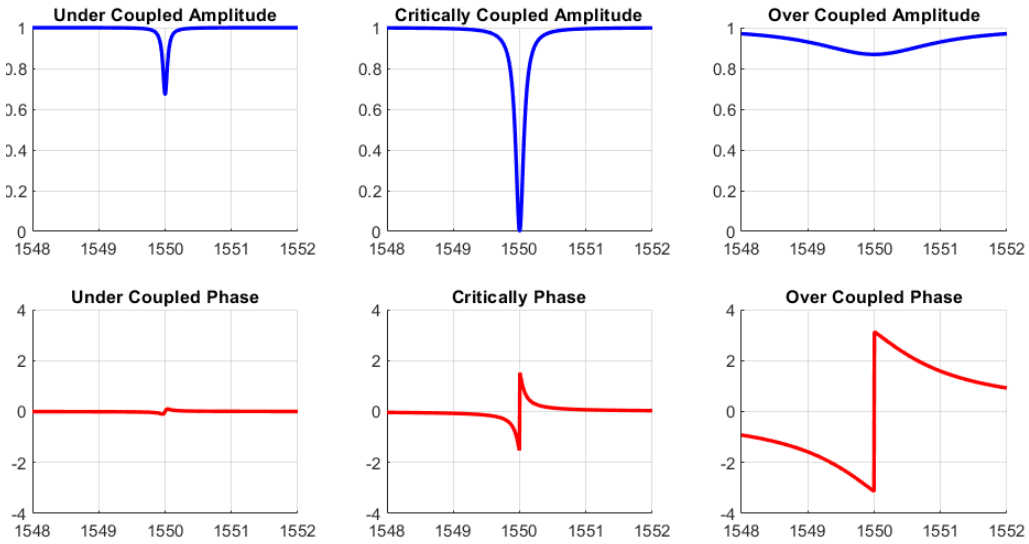

Figure 6.7: The amplitude and phase response for a sample microring with various levels of coupling. On the left, the microring is under coupled. In the middle, the microring is critically coupled. On the right, the microring is over coupled.

index. The transmitted power on the bus waveguide can be represented as [166]:

$$P_{t1} = |E_{t1}|^2 \tag{6.5}$$

Taking reasonable values for the rings for the ring radius, effective index, and loss, we can see the transmission amplitude and phase for three coupling scenarios in Figure 6.7. The only change between the rings is varying the coupling between the bus waveguide and microring. The most common approach to change the coupling strength is to change the distance between microring and bus waveguide during fabrication.

As seen in Figure 6.7, the over coupled ring has limited impact on amplitude but a strong impact on phase. As a result, it presents an opportunity for resonant based phased modulation. It should be noted, however, that the increased coupling between the bus waveguide and microring reduces the ring's ability to store energy, which reduces the Q of the ring. Due to the lower Q, it will require a larger resonance shift to transition from on resonance to fully off resonance.

For a single microring, amplitude modulation and binary phase shift keyed (BPSK) can be achieved [167]. BPSK can occur when the ring modulated to opposite sides of the resonance with

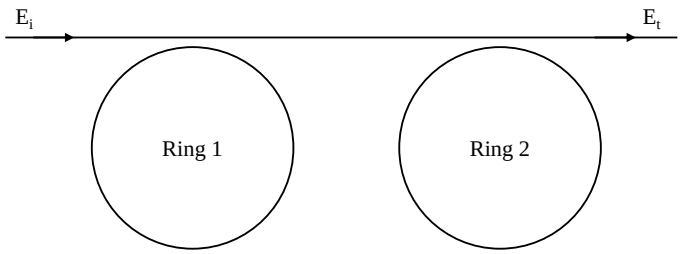

Figure 6.8: The arrangement of two microring resonators coupled to a bus that will allow for arbitrary QAM constellations. To cover the full IQ space, one ring should be over coupled and one ring should be critically coupled.

the same transmission, which results in constant amplitude with a phase shift. Higher modulation formats beyond PAM is not possible with a single microring as the amplitude and phase track together. With two rings coupled serially to the same bus waveguide, as seen in Figure 6.8, the phase and amplitude of the transmitted signal can be decoupled, enabling QAM constellations [168, 169].

If both rings are critically coupled, only a portion of the IQ space is reachable, which will result in reduced performance or will require reducing the QAM constellation size. The achievable IQ space with two critically coupled rings can be seen in Figure 6.9b with the black portion representing the achievable space. A potential mapping of QAM-16 points with noise added for visualization purposes can be seen in 6.9c.

To reach the majority of the IQ space, one of the rings must be over coupled. This allows for the phase response to be decoupled from the amplitude response, which is not possible with only two rings. The critically coupled ring can be used to set the desired amplitude, and the over coupled ring can be used to both correct for the induced phase response from critically coupled ring and to impart the desired phase response with minimal impact on the amplitude. The achievable IQ space can be seen in Figure 6.10, with a potential mapping of QAM-16 points with the same noise values as Figure 6.9, showing the path towards improved performance.

It should be noted that covering the shown IQ space requires being able to scan over the full ring response, which is challenging for high speed depletion modulation due to the relatively small resonance response compared to the injection or thermal response. Additionally, QAM modulation

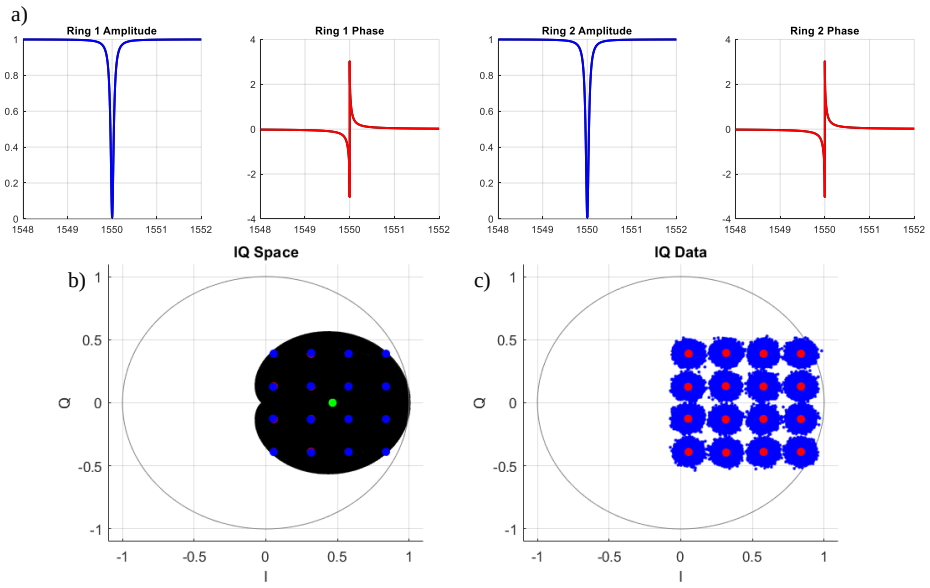

Figure 6.9: a) The amplitude and phase responses for the two critically coupled microrings. b) The achievable IQ space for the two critically coupled rings. While this space is generated through scanning over 1 nm centered on the resonance center, this could be achieved through intracavity modulation. The blue dots represent potential locations for QAM points. c) Simulated data points based on the QAM constellation from b).

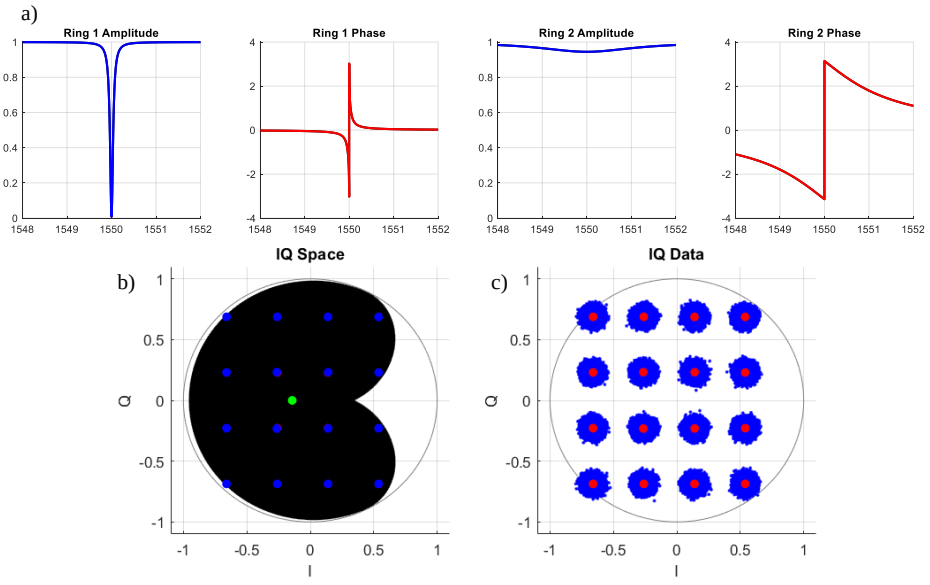

Figure 6.10: a) The amplitude and phase responses for the one critically coupled microring and one strongly over coupled microring. b) The achievable IQ space for the two critically coupled rings. While this space is generated through scanning over 1 nm centered on the resonance center, this could be achieved through intracavity modulation. The blue dots represent potential locations for QAM points. c) Simulated data points based on the QAM constellation from b).

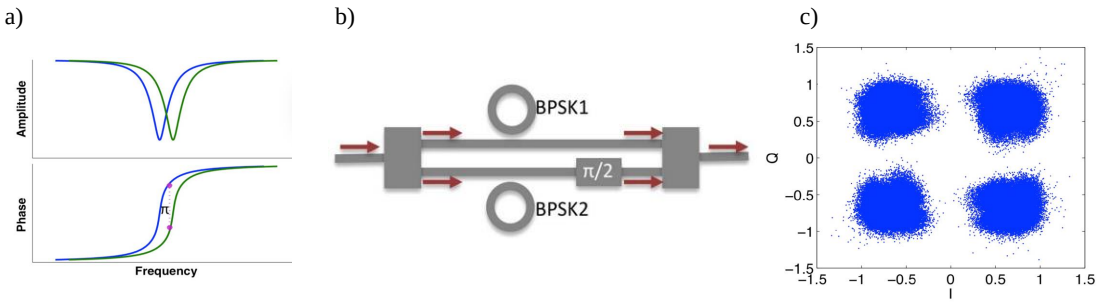

Figure 6.11: a) The amplitude and phase response for a single ring driven in BPSK. b) Two microring modulators embedded in a MZI structure to allow for QPSK generation with each microring operating in BPSK. c) The resulting QPSK signal from the structure in b). Adopted from [171].

using this approach requires two rings to be tuned to the same wavelength, which can increase the thermal stabilization challenges associated with the thermally sensitive microrings.

6.3 Microdisk QAM-16

While the previous section presents an approach for arbitrary QAM constellations using only two microrings, it requires being able to tune across the full resonance of an over coupled ring, which can be difficult at high modulation speeds. Additionally, the driving electrical voltages will not be binary signals, as each point in the QAM constellation will require a unique driving voltages for each of the two microrings. This is achievable, but it is preferable if the QAM constellation can be achieved with two-level or four-level voltage signals from an implementation point of view.

A single microring modulator can be used to generate BPSK modulation with a binary driving voltage, as shown in Figure 6.11 a. Utilizing two microrings embedded in a Mach Zehnder structure with a phase shift between the two arms will result in quadrature phase shift keyed (QPSK) modulation when each microring is driven to produce BPSK [170], as shown in Figure 6.11 b-c, respectively.

This approach can be scaled to higher modulation formats, by nesting additional phase modulation elements within additional MZIs. This has been demonstrated with bus waveguide phase shifters [172], but these elements are large compared to microrings and do not present the same op-

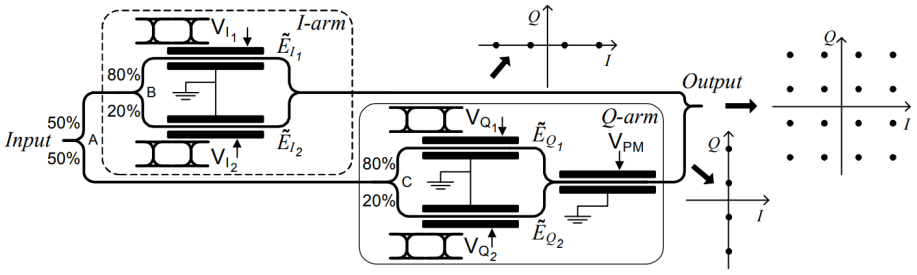

Figure 6.12: An example of embedding phase modulators within uneven MZI structures to produce I and Q arms, which are combined within a larger MZI structure to generate QAM-16. Adopted from [172].

portunity for easily scaling up through WDM operation. An example of this approach in a silicon photonic platform can be seen in Figure 6.12.

We adopted this approach to fabricate a QAM-16 modulator employing four microdisk modulators designed to operate as individual BPSK modulators and other AIM PDK components. A similar idea was proposed in [173]. To allow for flexible operation, the 80-20 coupler used in the MZM QAM-16 approach was replaced with a thermo-optic switch, allowing the splitting ratio to be tuned. Both arms of the unbalanced MZI had thermo-optic phase shifters. This allowed for tuning to account for imbalance in the arms and keep the arms symmetric for loss. There was an additional thermo-optic phase shifter in the Q arm to rotate the signal by $\pi/2$ to generate the QAM-16 signal.

As shown in Figure 6.13, the signal after a single microdisk modulator was a BPSK signal, with approximately even amplitude but a near π phase difference. The result of the unbalanced 80-20 MZI with both microdisk modulators operating in BPSK was four distinct points in the same line within the IQ plane. When the I and Q paths were added together with the Q arm rotated by $\pi/2$, the result was a QAM-16 signal, as shown in Figure 6.13. The simulation was performed in RSoft with imported models for the AIM PDK components.

The GDS for the fabricated microdisk based QAM-16 transmitter can be seen in Figure 6.14. The transmitter was composed of AIM PDK components. The DC pads were routed to one edge

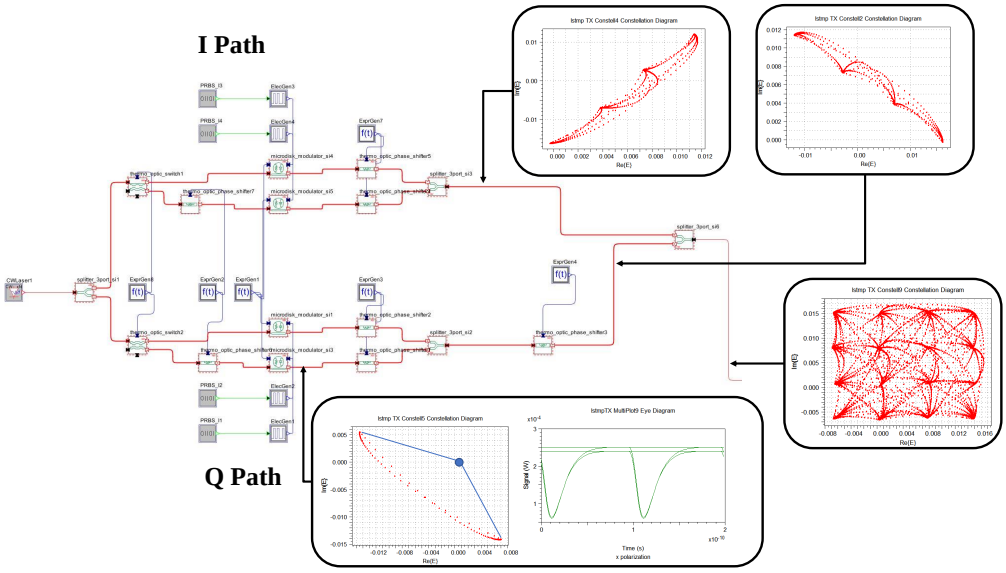

Figure 6.13: The interconnect simulation performed in RSoft using AIM PDK components to generate QAM-16 with microdisk components. As shown, each modulator operated in BPSK, with the 80-20 split coming from a thermal switch. The modulation of the I and Q paths before and after combining can be observed.

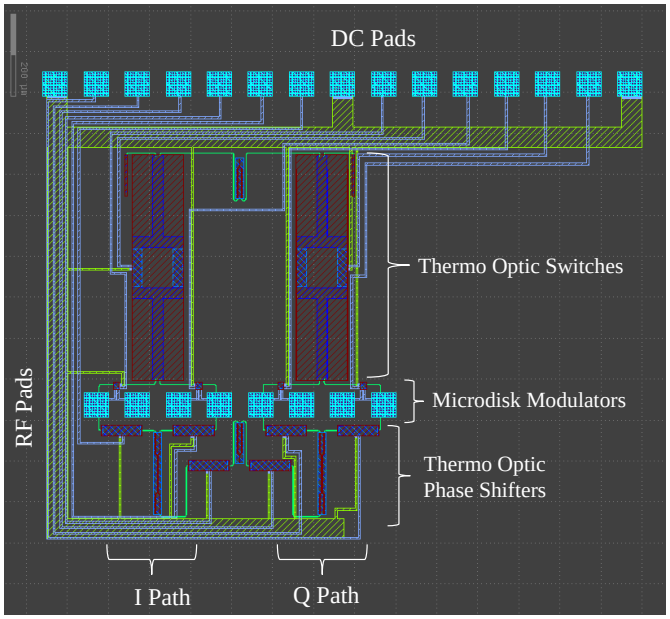

Figure 6.14: The GDS for the fabricated microdisk based QAM-16 transmitter. The thermal switches, microdisk modulators, and thermal phase shifters in both the I and Q arms are visible.

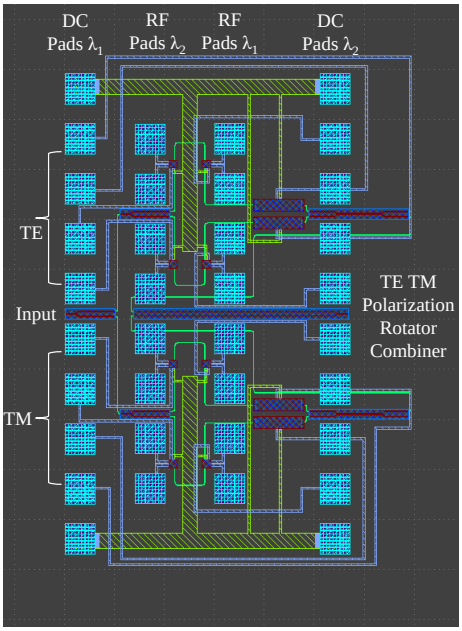

Figure 6.15: The GDS for the fabricated microdisk based PM WDM QPSK transmitter.

of the transmitter, and utilized a common ground for all the heater control elements to save space. The RF pads for the microdisk modulators were on the opposite side of the design to allow both sets of pads to be probed simultaneously. Waveguides from the QAM-16 transmitter routed away from the transmitter, and coupling was achieved with grating couplers. The QAM-16 microdisk transmitter is back from fabrication.

6.4 Microdisk WDM PM QPSK

Another microdisk based transmitter we have fabricated for higher order modulation formats built off of the microring based QPSK transmitter outlined in the previous section. To scale up to higher data rates, the approach was scaled by incorporating WDM and polarization multiplexing (PM). A similar approach was proposed utilizing PM QPSK [174]. The transmitter is shown in Figure 6.15 and featured eight microdisk modulators. Light was split with a 50-50 directional coupler. Each arm was routed to a WDM QPSK transmitter, which was a MZI with two microdisk modulators in each arm and thermal optic phase shifters for phase tuning between the two arms. The resonances were fabricated so that each arm had the same two resonance wavelengths. The

two WDM QPSK transmitters were combined with a polarization rotator combiner, so that one arm was kept TE but the other was rotated to TM. The output of this transmitter was coupled out of the PIC with a TE-TM edge coupler. The PIC was designed to be probed, with each of the two wavelengths in the circuit probed independently. There were two RF pad columns and two DC pad columns with common grounds to reduce pad counts. The PM WDM QPSK transmitter is back from fabrication.

6.5 Conclusion

We outlined four approaches for scaling up to higher data rates through advanced modulation format transmitters. The approaches were an MZM PAM-4 transmitter, a two ring microdisk QAM-16 transmitter, a QAM-16 microdisk transmitter, and a PM WDM QPSK microdisk transmitter. The last two transmitters are back from fabrication and ready to be characterized.

Chapter 7: Supplemental Silicon Photonic Interconnect Research

In this chapter, we present additional avenues of research in silicon photonics for transceiver development. The work in this section spans across a number of areas, but all contribute to silicon photonic transceivers. The chapter first includes research on thermal crosstalk from adjacent microdisk modulators, which becomes significant at the ultra compact pitches necessary to meet high areal bandwidth densities. Next, the chapter presents work on the development and performance of graphene-enabled silicon nitride microring modulators within an optical interconnect. This research is important for the development of silicon photonic transceivers, as it explores the benefits of introducing additional materials into a CMOS process to push the performance of a silicon photonic platform. Next, the chapter presents a method for high throughput bandwidth characterization of silicon photonic modulators. As silicon photonic transceivers mature, the role of testing to determine yield and identify unideal devices becomes more crucial to scale up the production of transceivers. The characterization approach outlined provides an approach to characterize the bandwidths of multiple modulators simultaneously to aid in scaling the necessary testing up to production. Finally, the chapter presents an approach to implement photonic deserialization. Deserialization is often necessary to translate from the high bandwidth optical transceivers to the widely parallel, but lower bandwidth, connections to the compute nodes such as CPUs, GPUs, and ASICs. However, deserialization in EICs often consumes significant power. We implement the deserialization within the optical domain to investigate if the approach reduces the energy consumption of the end-to-end link.

7.1 Thermal Crosstalk in Silicon Photonic Microdisk Modulators for Ultra Compact Dense WDM Systems

In this section, the thermal crosstalk for WDM silicon photonic microdisk modulators is experimentally determined as a function of microdisk pitch with 10 Gbps signals. We show that it is advisable to fabricate microdisk modulators with at least 50 μm pitch to reduce the thermal crosstalk power penalty.

7.1.1 Introduction

With communication bandwidth demands placing increased emphasis on areal bandwidth densities, >Tbps/mm^2 silicon photonic transceivers are now being developed [175]. These densities require increasingly smaller photonic elements to be fabricated at increasingly narrower pitches, which makes the small footprint of microdisk modulators an attractive alternative to Mach-Zehnder modulators. The wavelength selective response of the microdisk modulators allows for dense WDM transmitters to be coupled to a bus waveguide. Scaling to higher bandwidths with this architecture can be achieved by increasing the number channels rather than increasing the channel data rate. The lower channel data rate reduces the reliance on SERDES and digital signal processing, and the numerous channels makes clock forwarding feasible. These features typically dominate energy consumption in optical transceivers [116, 117], and reducing the dependence on them allows for more energy efficient Tbps links.

While compact, microdisks are typically sensitive to thermal variations. Microresonators can be made to be athermal [176], but some thermal sensitivity is generally desired to provide a means to tune the device and to correct for fabrication variations. Achieving >Tbps/mm^2 interconnects with the energy efficient lower channel rates will require ultra-dense integration. Aggressive modulator pitches mean that heat generated during operation will affect the performance of neighboring devices. Thermal stabilization techniques can be used [177], but proper implementation requires characterizing the thermal crosstalk. Previous work characterized thermal crosstalk in terms of the

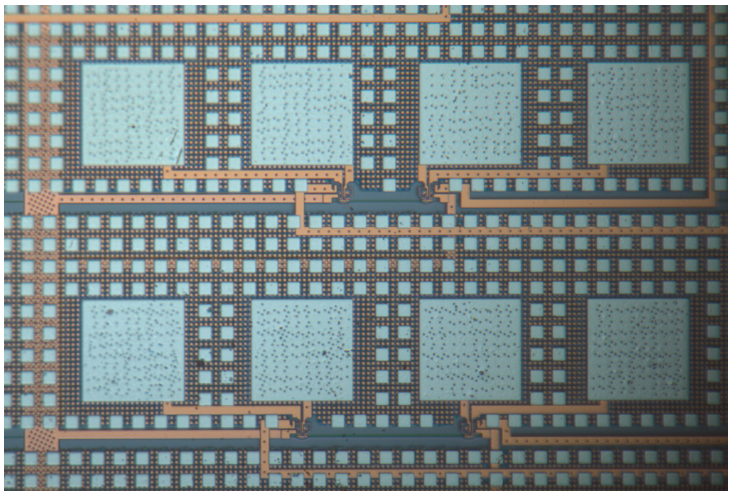

Figure 7.1: Two of the seven rows of the thermal crosstalk test device. The 49.5 μm and 99.5 μm pitches are shown.

ratio of resonance shifts of neighboring channels [178] but did not investigate the thermal crosstalk modulation power penalty. We characterized the thermal crosstalk modulation power penalty as a function of microdisk pitch to determine an optimal pitch for reducing the effects of thermal crosstalk for ultra dense WDM systems.

7.1.2 Device

The microdisk modulators were fabricated on an AIM Photonics MPW. Heaters wre used to tune the microdisk resonance and data was encoded with a high speed PN depletion modulator. The modulators had an FSR of approximately 25 nm. The test device featured seven rows of microdisk modulators, with two modulators on each row, as shown in Figure 7.1. The resonances of the two modulators were separated by approximately 12.5 nm. The thermal and PN response of the modulators can be seen in Figure 7.2. The pitch between the modulators was varied with each row; the pitch values were 15.5 μm, 24.5 μm, 49.5 μm, 99.5 μm, 199.5 μm, 399.5 μm, and 599.5 μm.

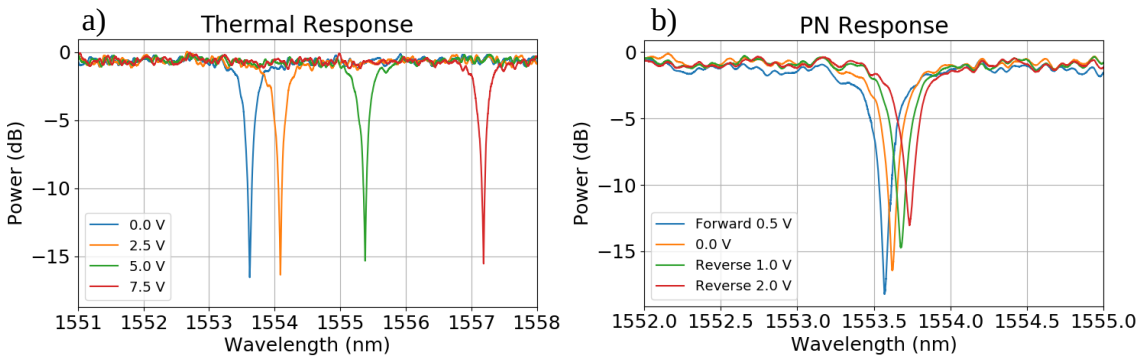

Figure 7.2: a) The thermal response of the modulator's integrated resisitive heater. b) The diode response of the modulator.

7.1.3 Experimental Setup

For each row, the left mircodisk was modulated with a 2^{31}-1 PRBS signal at 10 Gbps. The PRBS signal from the PPG was 1.4 V_{PP} signal biased at 0.5 V. The laser was set to the lower wavelength edge of the modulator's resonance and tuned to produce optimal modulation. Thermal crosstalk was generated from the right modulator's heater and from the right modulator operating in injection. The injection heat generation served as a representation for high speed switches and (de)muxes, which would be operated in injection with comparable current draw. For each row, data was collected for five thermal crosstalk variations: no thermal crosstalk, 2.5 V on the right modulator's heater, 5.0 V on the right modulator's heater, 0.9 V injection on the right modulator, and 1.1 V injection on the right modulator. The four crosstalk scenarios corresponded to approximately 1.1 mW, 4.4 mW, 2.3 mW, and 8.1 mW, respectively. BER curves were generated by amplifying the optical output of the test device with an EDFA, and varying the received optical power with a variable optical attenuator (VOA) prior to sending the signal to a commercial receiver and bit error rate tester.

7.1.4 Results

BER curves were generated for each thermal crosstalk variation of each row. The power penalty was determined as the difference in received power required to produce error free operation (BER

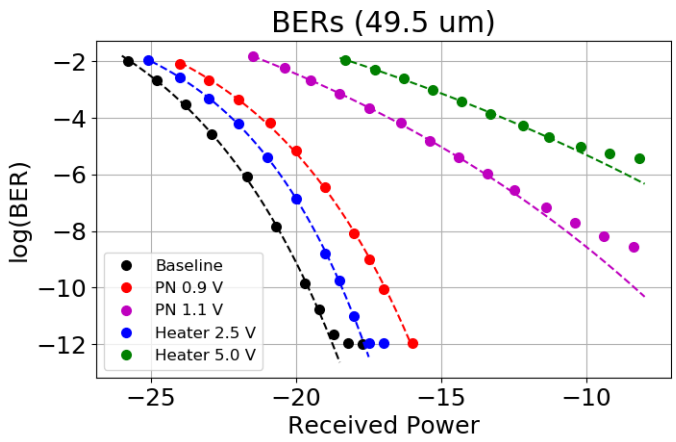

Figure 7.3: The BER curves for the 49.5 µm pitch row for the five operating conditions: no thermal XT, PN 0.9V, PN 1.1V, heater 2.5V, and heater 5.0V.

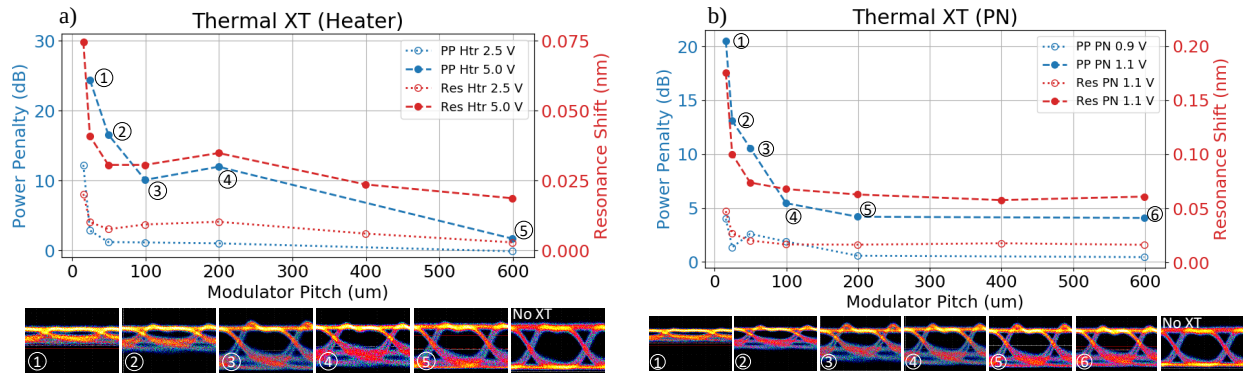

Figure 7.4: The power penalties and DC resonance shifts as a function of modulator pitch for the heater generated crosstalk (a) and PN generated crosstalk (b), as well as the corresponding eye disagrams.

of 10^{-9}) between a specific thermal crosstalk condition and the corresponding no thermal crosstalk measurement. The power penalties for the 5.0 V heater were the largest, even though 1.1 V injection dissipated more power, as seen in Figure 7.3 for the 49.5 µm pitch row. The heaters shared a common metal ground, which may have provided a path for enhancing thermal crosstalk. The PN diodes did not share a common ground. The power penalties and resonance shifts as a function of modulator pitch can be seen in Figure 7.4a and b for the heater generated crosstalk and diode generated crosstalk, respectively.

The impact of thermal crosstalk was most significant at pitches below 50 µm, and increasing the

pitch past 100 μm yielded diminishing returns. For higher thermal generation situations, such as the 5.0 V heater and 1.1 V injection, the power penalty and resonance shift did not reach negligible values within the investigated pitch range. The increase in power penalty for the heater at 199.5 μm was due to the heater's resistance being lower than normal, resulting in increased heat generation. The 199.5 μm and 24.5 μm pitch heaters had a resistance of approximately 1.5 kΩ, compared to the expected 6 kΩ. The heat generation for the diode operating in injection was more consistent, with standard deviations of 0.2 mW and 0.4 mW for the 0.9 V and 1.1 V operating conditions, respectively. In real systems the thermal crosstalk would be more significant, as most modulators would be subjected to heat generated from neighboring modulators on both sides, as well as from additional parallel bus waveguides.

7.1.5 Conclusions

We characterized the thermal crosstalk power penalty and resonance shift for microdisk modulators as a function of modulator pitch. The results indicated that pitches below 50 μm should be avoided to minimize extreme thermal crosstalk. For high thermal generation conditions, thermal crosstalk was unavoidable with reasonable pitches. The results demonstrated that ultra-dense pitches to meet bandwidth density requirements would necessitate thermal stabilization solutions and thermal isolation approaches to preserve system performance.

7.2 Graphene Enabled Optical Interconnects

In this section, the intermodulation crosstalk of graphene modulators integrated on silicon nitride is experimentally characterized for the first time on 1 Gbps signals. We show that 25 GHz channel spacings are supported with < 0.1 dB penalty for DWDM applications. Additionally, a FPGA based FEC system is developed and applied to graphene electro-absorption modulators at 1.25 Gbps, improving error rate by up to 104. Additionally, adaptive FEC was demonstrated, allowing 11% more data to be transmitted compared to normal FEC.

7.2.1 Intermodulation Crosstalk Overview

For optical interconnects to be integrated into data centers, high performance computing platforms, and multi-core processor units, they need to be competitive in terms of interconnect footprint, energy consumption, and bandwidth density [179]. In the optical domain, microrings occupy a substantially smaller area than MZMs and their operation has a strong wavelength dependence.

Due to this wavelength selectivity, an ultra-compact Dense WDM system can be constructed where a series of microring modulators are adjacent to a bus waveguide. Each microring is constructed such that a different wavelength of light meets the resonance condition, thus allowing for independent wavelength modulation and data multiplexing. In silicon photonic platforms, high speed modulation is achieved through the free-carrier plasma dispersion effect. The presence of carriers increases optical loss due to free carrier absorption and decreases the index of refraction due to the free carrier dispersion effect, which alters the resonance wavelength. In a WDM system, wavelengths placed too close will suffer from intermodulation crosstalk due to the Lorentzian lineshape of an adjacent modulator when a voltage is applied and the resonance wavelength shifts [180, 181].

7.2.2 Graphene Modulator Device

Due to graphene's high carrier mobility and broadband absorption [182], it has the potential to be used as an optoelectronic material. The graphene-enabled microring modulator device was fabricated at the Cornell Nanofabrication Facility and can be seen in Figure 7.5a. The modulation is provided through a graphene-insulator-graphene capacitor on a portion of the SiN waveguide of the microring. An applied voltage results in decreased round-trip ring loss via gating the interband absorption. While this changes the Q factor of the ring, it has a weak effect on the index of refraction, leading to a negligible shift in the resonance wavelength (Figure 7.5b) [183]. The static resonance (no spectral shift) makes the graphene-enabled microring device an attractive modulator for dense WDM systems.

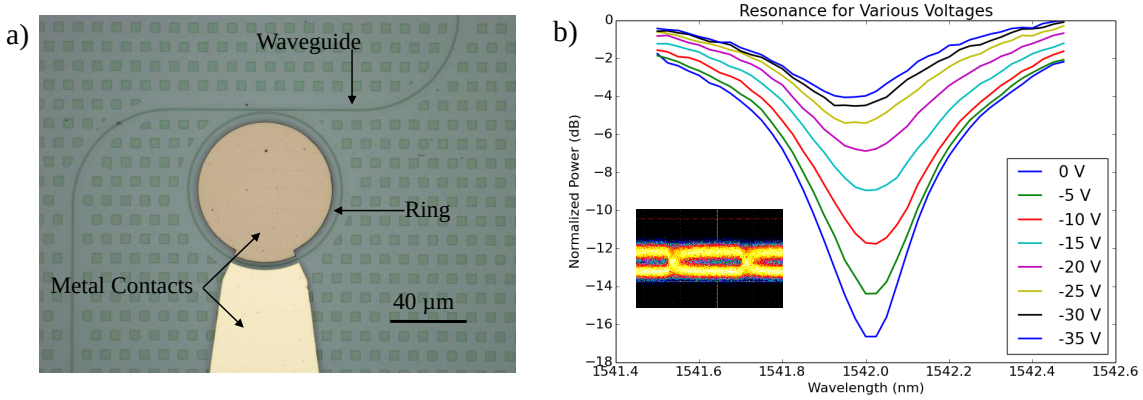

Figure 7.5: a) The graphene modulator used in the experimental interconnect to measure the intermodulation crosstalk. b) The optical resonance response for various bias voltages, with an example of the eye from modulation.

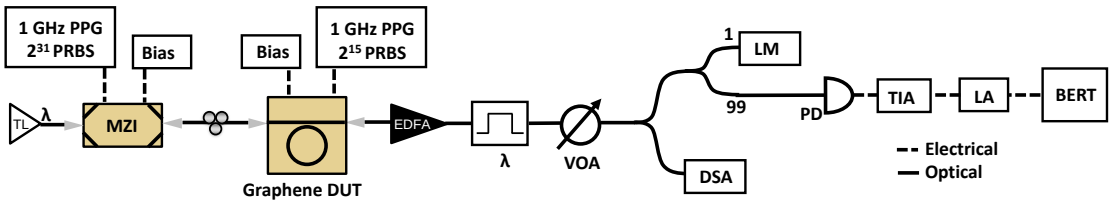

Figure 7.6: The experimental setup. TL: Tunable Laser. DUT: Device Under Test. VOA: Variable Optical Attenuator. LM: Lightwave Multimeter. PD: Photodiode. TIA: Transimpedance Amplifier. LA: Limiting Amplifier. BERT: Bit Error Rate Tester. DSA: Oscilloscope.

7.2.3 Intermodulation Crosstalk Experimental Setup

The experimental setup is shown in Figure 7.6. Light was modulated by the MZM and coupled into the graphene modulator. The graphene modulator was driven with an 8 V_{PP} signal biased at 4 V. The graphene was modulated with a 2^{15}-1 PRBS signal and the commercial modulator was modulated with a 2^{31}-1 PRBS signal, both at 1 GHz. The power penalty was measured by observing the performance (BER) of the MZM at various frequencies around the resonance wavelength of the graphene modulator, i.e. reducing the channel spacing.

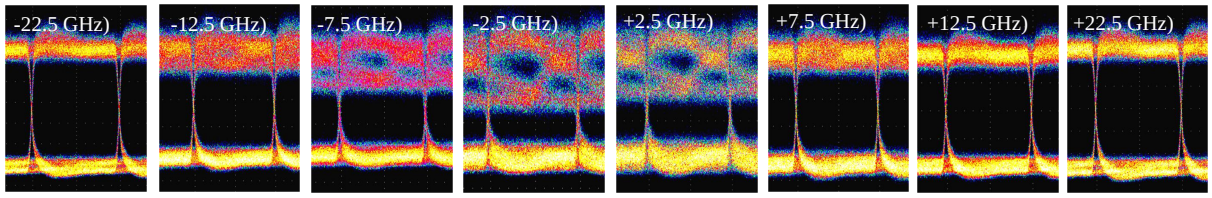

Figure 7.7: The MZI eye diagrams with increasing frequency separation from the graphene modulator's resonance shown at 1 GHz modulation and 1.5 dBm received power.

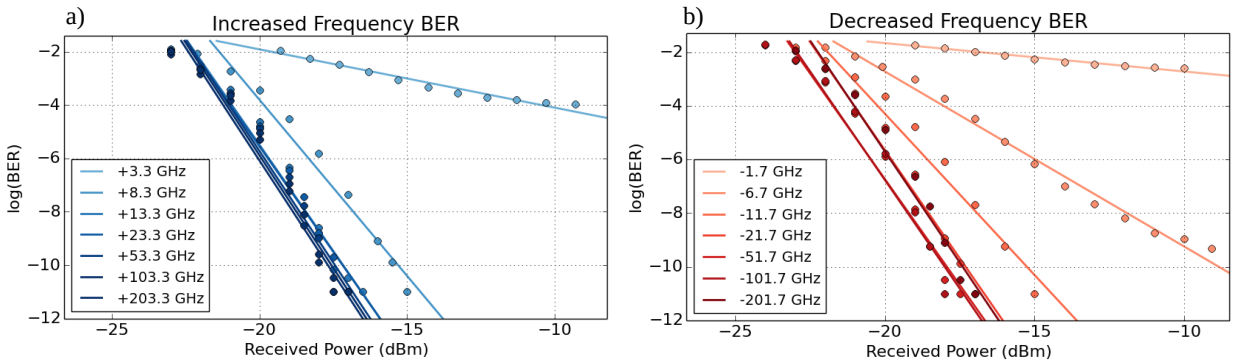

Figure 7.8: MZI BERs for channels above (a) and below (b) the resonance wavelength of the graphene modulator.

7.2.4 Intermodulation Crosstalk Results

Eye diagrams and BER measurements were collected for various channel spacings around the resonance wavelength of the graphene modulator. These results are shown in Figure 7.7 and 7.8, respectively. The BER data trendline was used to extract the received power necessary to produce a BER of 10^{-9}. The degradation of the MZM's eye diagram was observed as the frequency of the light moved towards the operation wavelength of the graphene microring (Figure 7.7).

A power penalty was then defined as the difference in received power needed to produce a BER of 10^{-9} between a particular channel spacing and the baseline measurement (+102.5 GHz or –102.5 GHz away, depending on the side). These results can be seen in Figure 7.9a. Each side of the power penalty curve was fit to an exponential curve independently. Experimentally, we found that a 0.1 dB power penalty occured at +19 GHz and –24 GHz. It is important to note that there are other sources of power penalty besides intermodulation crosstalk. Figure 7.9b

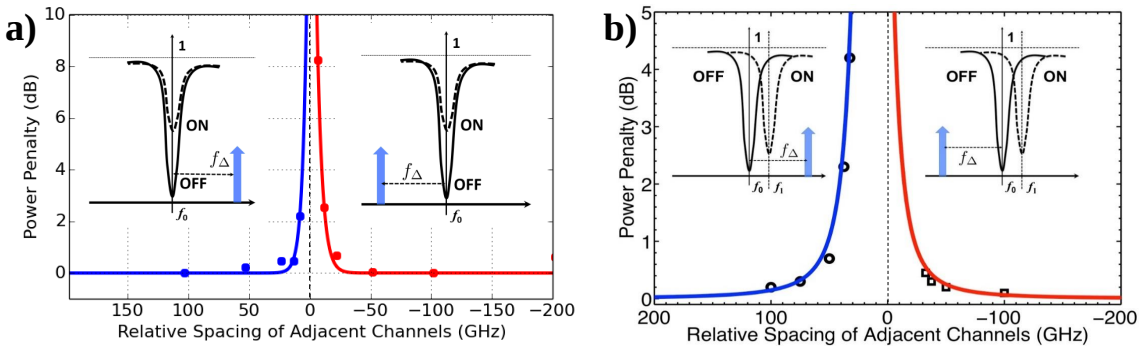

Figure 7.9: a) Power penalty analysis for the graphene modulator. b) Power penalty analysis for a carrier-based silicon microring modulator [184].

shows the intermodulation power penalty for carrier-based microring modulators [184]. Due to the presence of a spectral blueshift, an asymmetric behavior with higher power penalties was observed, indicating the superior crosstalk performance of graphene-based modulators.

7.2.5 Intermodulation Crosstalk Conclusion

We characterized the intermodulation crosstalk power penalties of novel graphene-enabled microring modulators, both experimentally and with a model built up from the DC spectral response of the device. The power penalty curve was significantly more symmetric than that of carrier-based microrings. This was the first evaluation of intermodulation crosstalk for graphene-based microring modulators. The results indicated relatively good agreement between model and experiment and suggest that channel spacings as small as 25 GHz could be employed by a WDM modulation system based on these graphene-enabled modulators.

7.2.6 Graphene FEC Introduction

Next, the performance of these graphene enabled silicon photonic modulators was explored in a FPGA link intended to model a free space link, where silicon photonic systems are beginning to be deployed [185].

Issues related to beam divergence and atmospheric attenuation often impinge on free space

links, resulting in much higher BERs than terrestrial links; however, higher BERs (up to 10^{-6}) may be considered acceptable [186]. A common practice to counter the extra attenuation is to employ forward error correction (FEC) to improve the link BERs. While FEC improves the BER of a link, it lowers the effective data rate. A potential solution is to employ an adaptive FEC setup [187], which does not use FEC when the attenuation is low, and enables FEC when extra attenuation is present, increasing the total data transmitted. We develop and demonstrate a photonic link driven by an FPGA with adaptive FEC.

7.2.7 FPGA Platform

The FPGA platform enabled transmission of PRBS data on a synchronized link between a master FPGA and a slave FPGA at rates up to 10 Gbps [188]. Both FPGAs were connected out-of-band via ethernet to a central computer. An embedded processor on the FPGA received and parsed packets from the central computer, formed using C++ software. These packet transactions propagated commands down a message bus to registers to control the hardware logic.

Prior to data transmission, the link was established. The master FPGA transmitted a synchronization frame, and the slave FPGA sent an out of band-of-band ethernet acknowledgement after receiving it. The frame also served to align the data window. After link synchronization, the PRBS block began transmitting 50-bit words that were injected into the FEC encoding block, where six parity bits were added. The 56-bit word was then serialized and transmitted from the quad small form factor pluggable (QSFP) breakout cable. The flow was mirrored on the receive side with the slave FPGA: the signal entered the QSFP breakout cable and was de-serialized. This 56-bit word was sent to the FEC decoding block, which returned a 50-bit corrected word to the data checker block. Data error statistics were then transmitted to the control computer via ethernet.

7.2.8 Forward Error Correction

Forward error correction was implemented using a custom block for Hamming encoding. To fit within the dimensions of the FPGA platform, a truncated version of Hamming (63, 57) was

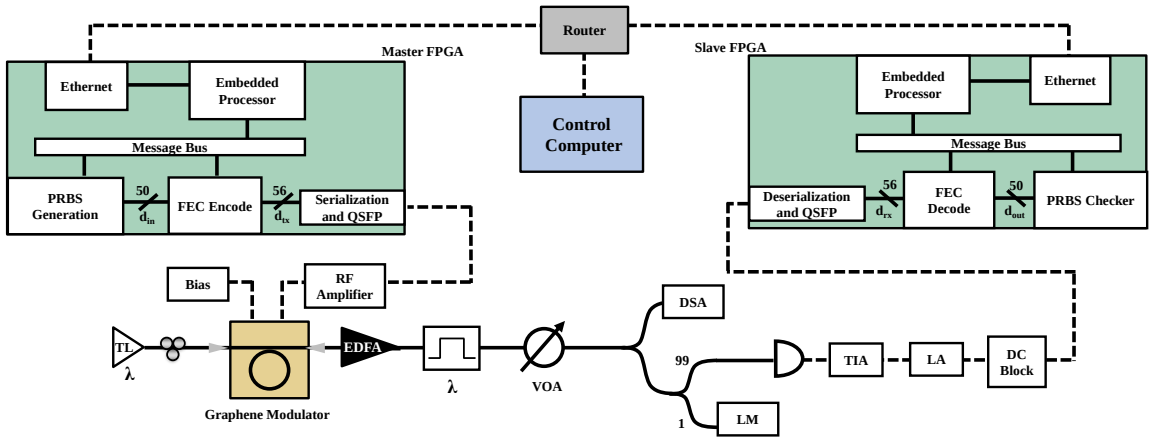

Figure 7.10: The experimental setup. TL: Tunable Laser. VOA: Variable Optical Attenuator. LM: Lightwave Multimeter. PD: Photodiode. TIA: Transimpedance Amplifier. LA: Limiting Amplifier. BERT: Bit Error Rate Tester. DSA: Digital Serial Analyzer Sampling Oscilloscope.

used to encode 50 data bits with 6 parity bits to produce Hamming (56, 50). In the master FPGA, the 50-bit word from the PRBS generator was multiplied modulo 2 by a generator matrix, G, to produce the 56-bit word sent over the QSFP: $d_{tx} = Gd_{in}$. In the slave FPGA, the received data was multiplied modulo 2 with a parity check matrix, H, to determine the error location if one occurred: $e = Hd_{rx}$. The error was corrected and the parity bits were removed to obtain d_{out}, which was sent to the PRBS checker. This approach was able to correct one error per 50-bit word.

7.2.9 FEC Experimental Setup

The experimental setup is shown in Figure 7.10. The tunable laser's output was coupled into the graphene modulator chip. The output from the master FPGA's was amplified and to drive the graphene modulator biased at 40 V. The optical signal was amplified with an EDFA and filtered with a grating filter at the tuneable laser's wavelength. The received power was adjusted with a variable optical attenuator, before being split between a digital serial analyzer sampling oscilloscope and a photodiode for error testing. The photodiode signal passed through a transimpedance amplifier, a limiting amplifier, and a DC block before entering on the receive cable of the slave FPGA's QSFP.

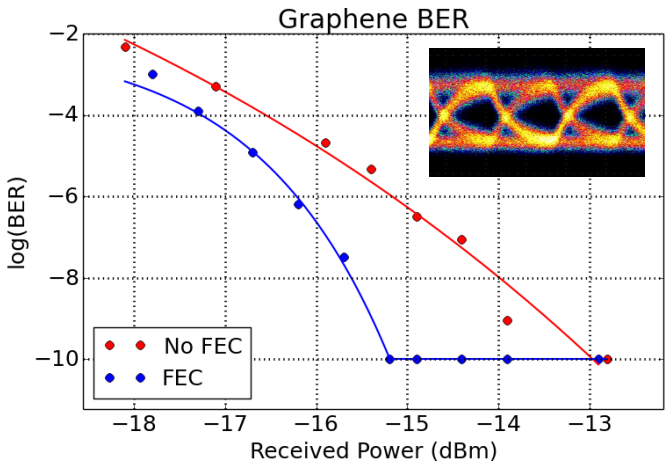

Figure 7.11: The BER curves of the graphene modulator at 1.25 Gbps with and without forward error correction and the eye diagram taken after the grating filter.

7.2.10 Graphene FEC

Due to bandwidth limitations of the graphene modulators, the FPGA project was compiled to operate at 1.25 Gbps. For the purposes of this experiment, we considered a BER of 10^{-10} to be error free performance. Without forward error correction, the graphene modulator was error free at -13 dBm received power. With forward error correction, the graphene modulator was error free at -15.2 dBm, for an improvement of 2.2 dBm. At the FEC's error free power (-15.2 dBm), the BER with FEC disabled was four orders of magnitude higher (10^{-6}). As the attenuation was increased, the BERs of both versions converged. The results and eye diagram can be seen in Figure 7.11.

7.2.11 Adaptive FEC

In situations with low data rates and limited transmit windows, a lower effective data rate becomes a more serious issue, such as for data transmission in satellites. One potential solution is to use an adaptive forward error correction approach, which extends the data transmission window and minimizes the percentage of the data that is transmitted at the lower effective rate to maximize the total data transmitted.

To explore the extent that adaptive FEC can improve total data transmission compared to reg-

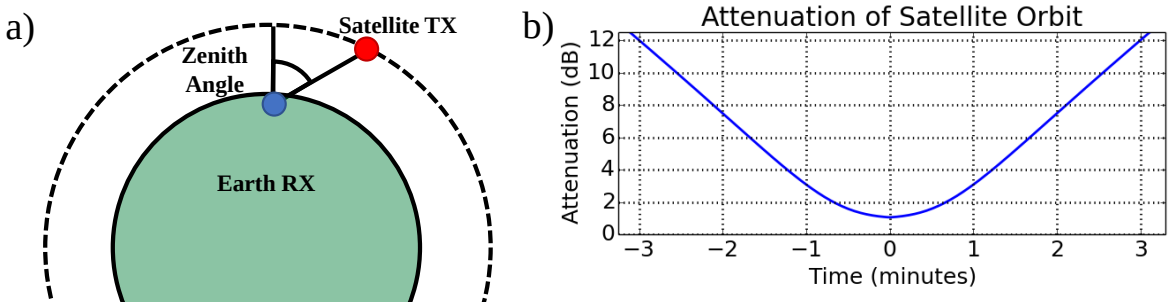

Figure 7.12: Diagram depicting the transmission link for adaptive FEC. a) and the attenuation profile as a function of time b).

ular FEC, an attenuation profile was modelled from the data in [187]. Below 70 degrees, the attenuation roughly scaled exponentially with zenith angle. By making the same assumption of a 90-minute orbit, the zenith angle, and therefore attenuation, could be represented as a function of time.

For a more stable link over time, the graphene modulator was replaced with a commercial modulator at 5 Gbps, as seen in Figure 7.13. This was because the graphene modulator link had difficultly consistently syncing over an extended period of time, which was a necessity for adaptive FEC. Similar to the graphene FEC experiment, error free operation (10^{-11} BER) was achieved with 2.5 dBm lower received power. Additionally, at -20.5 dBm, the FEC version had a BER four orders of magnitude lower.

To allow for more data points, the experiment was performed at one fifth the speed of the orbit window. Across the same attenuation profile, BERs were collected in three cases: FEC disabled, FEC enabled, and adaptive FEC. For the adaptive case, FEC was initially enabled and was disabled when the data rates reached error free (10^{-10} BER). FEC was enabled once the BER was worse than 10^{-6}. The total data transmitted increased at a 5 Gbps (scaled for effective rate when FEC was enabled) any time that the link had a BER better than 10^{-6}. The transition between FEC enabled and disabled for the adaptive run can be clearly seen in the BER jumps in Figure 7.14. The FEC disabled case was able to send 0.48 Tb. In comparison, the FEC enabled case transmitted 0.63 Tb and the adaptive case transmitted 0.70 Tb.

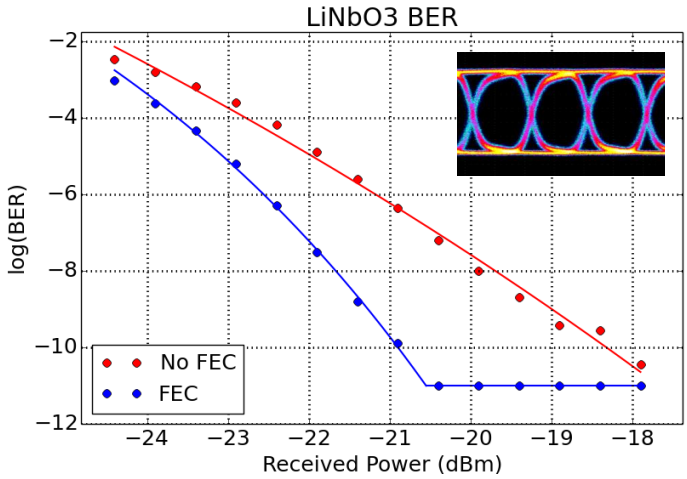

Figure 7.13: The BER curves of the commercial modulator at 5 Gbps with and without forward error correction and the eye diagram taken after the grating filter.

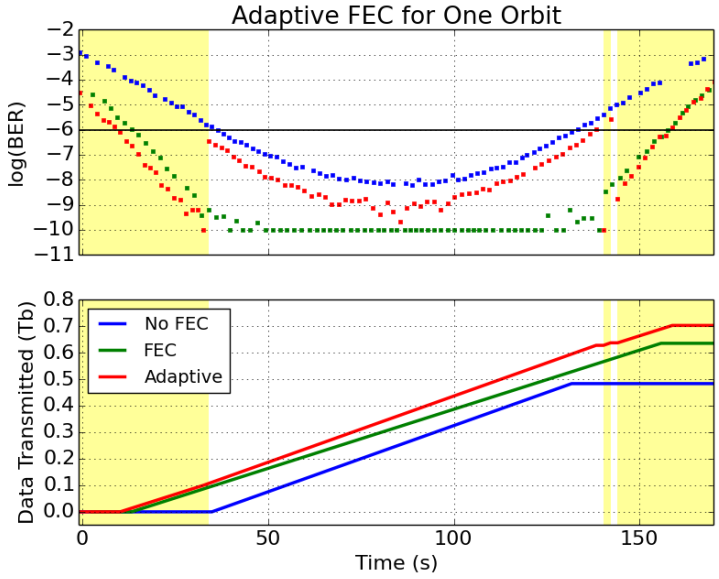

Figure 7.14: The BERs for the three cases (No FEC, FEC, and adaptive FEC) over time as the attenuation is varied to simulate a low earth orbit's attenuation profile. The yellow bands indicated when the FEC was enabled for the adaptive case.

7.2.12 FEC Conclusion

We demonstrated a FPGA system to enable forward error correction in optical links. This approach was applied to a graphene modulator to produce error free operation with 2.2 dBm lower received power, and an error rate four orders of magnitude lower at the same received power. Additionally, an adaptive FEC system was developed and tested. During a transmission window for a simulated low earth orbit satellite, FEC enabled 29% more data to be transmitted compared to normal operation, and adaptive FEC enabled 46% more data to be transmitted compared to normal operation.

7.3 High Throughput Bandwidth Characterization of Silicon Photonic Modulators using Offset Frequency Combs

We developed a low complexity, high-throughput testing technique for concurrently characterizing the bandwidths of multiple in-series modulators with independent frequency combs. The approach was demonstrated on two serial modulators at 9.2 GHz and 15.5 GHz.

7.3.1 Introduction

Photonic integrated circuits can contain thousands of photonic elements [189]. As the complexity of these circuits continues to grow, the increasing scale of photonic integrated circuits pushes testing and characterization to be integral components of photonic manufacturing. For testing to keep pace with design complexity, high throughput testing strategies must be developed.

The demand for high data rate interconnects pushes transceivers to combine WDM with high speed devices, increasing the number of photonic elements in transceivers [190, 191]. For WDM transmitters, it is necessary to determine the bandwidth of all the modulators, as the slowest modulator will establish the system bandwidth. Approaches that measure the frequency response of optical modulators include calibrated vector network analyzers [192], optical spectrum analysis of sidebands [193], sweeping frequency measurements [194], and self-calibrating two-tone mod-

ulation [195], all measuring the modulation bandwidth of one device at a time. We developed a high throughput testing strategy for WDM transmitter frequency responses by measuring multiple modulators simultaneously, which decreased measurement time and simplified the testing setup. We demonstrated two experimental setups using two different receiver methods. The first approach used a photodiode and electrical spectrum analyzer, and the second approach used an optical spectrum analyzer. This high throughput testing method allows device characterization to keep pace with photonic design complexity.

7.3.2 Electrical Receiver Experimental Setup

We measured the frequency response of multiple devices simultaneously by generating multiple electronic frequency combs. Each frequency comb had the same tone spacing, with the combs offset so there was no overlap between them. The frequency combs were applied to different microring modulators. At the output, the individual device bandwidths were discernable with minimal processing because the frequency combs were staggered. The device was a silicon photonic eight-channel microring based modulator for WDM modulation. PN depletion phase shifters drove the RF microring modulation, and thermal tuners were used to adjust the resonances of the ring modulators. Light was coupled into and out of the chip with grating couplers. Thermal and RF control was achieved through electrical probes.

For this experiment, only two microring modulators were used, as seen in Figure 7.15. A tunable laser was set to 1546 nm, and the microring modulators were tuned with both ring resonances overlapping so that the laser was located on one side of the resonance. Ring one was driven with a 29-tone frequency comb from 1.0 GHz to 22.0 GHz with 0.75 GHz spacings. Ring two was driven with a 29-tone comb from 1.3 GHz to 22.3 GHz with 0.75 GHz spacings. Both frequency combs were generated by independent outputs from an arbitrary waveform generator with 65 GSa/s. The output from the device was amplified with an EDFA before being received by a photodiode and sent to an electrical spectrum analyzer. The frequency combs were calibrated for the cables and connectors along the signal path to provide equal tone power to the microring modulators and

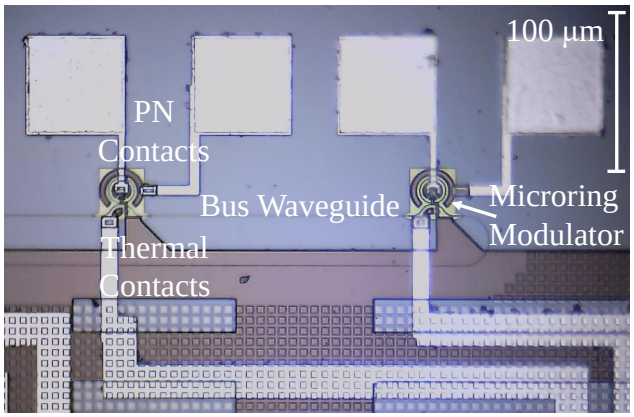

Figure 7.15: The test device used for implementing the dual comb bandwidth characterization. The device structure is two microring modulators coupled to the same bus waveguide.

compensate for the attenuation of higher frequencies. While the calibration did not account for the photodiode or the contact probes, they were selected because their bandwidths are 70 GHz (photodiode) and 40 GHz (contact probes) to mitigate effects on the signal path.

7.3.3 Electrical Receiver Results

All frequency combs were visible at the electrical spectrum analyzer. Since the tone locations of the frequency combs were known, we separated the spectrum analyzer's signal into the separate frequency combs to determine the separate device bandwidths, as shown in Figure 7.17. For this particular example, ring one's 3 dB bandwidth was at 9.2 GHz and ring two's 3 dB bandwidth was at 15.5 GHz. By measuring the bandwidth of the two rings together, the overall measurement time took half as long. This approach could also be applied to more than two modulators by increasing the number of frequency combs which would further increase the overall measurement speed.

7.3.4 Optical Receiver Experimental Setup

Introducing a modern, high resolution optical spectrum analyzer (OSA) allowed for the measurement process to be simplified. With an electrical receiver, the resonance of the WDM modulators needed to be determined prior to making a bandwidth measurement, and required an equipment

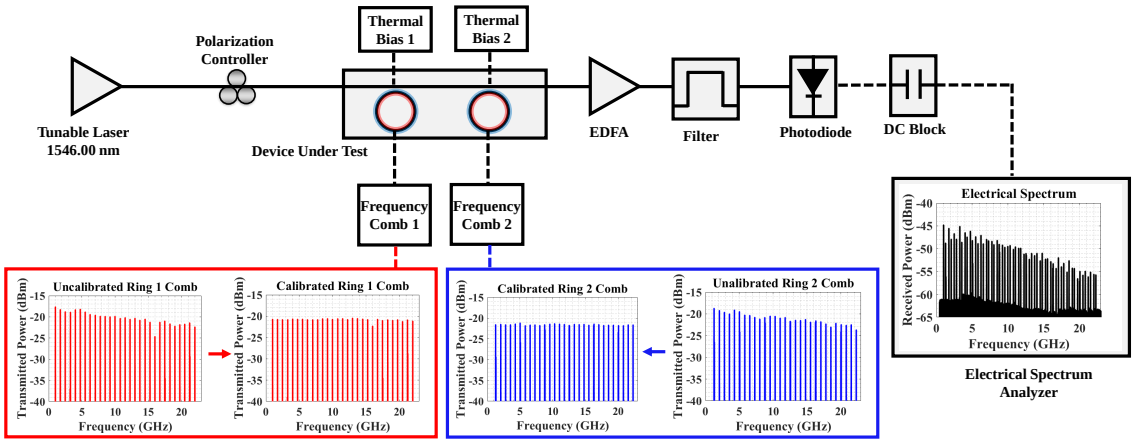

Figure 7.16: The experimental setup for the electrical receiver approach. A tunable laser is coupled into the WDM modulator. The microring modulators are each driven by an independent frequency comb that is calibrated to account for the electrical signal path attenuation. The output of the WDM modulator is amplified and filtered before being received by an electrical spectrum analyzer.

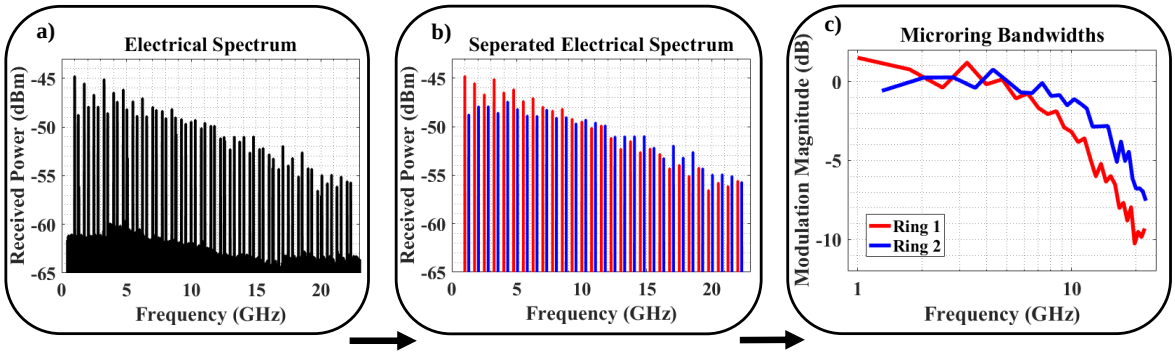

Figure 7.17: a) The initial spectrum from the electrical spectrum analyzer. b) The electrical spectrum separated into the two independent frequency combs. c) The frequency response of the microring modulators extracted from the frequency combs.

switch. With the OSA, a laser was able to be swept to determine the modulator's resonance and the tones of the separate electrical frequency combs was measured with one piece of equipment. The setup for the optical receiver was similar to the electrical receiver case but there was no longer a need for a photodiode or DC block as the optical signal was inputted directly into the OSA. Since the OSA had a limited dynamic range and could not filter the carrier away, the tone strength of the modulation combs needed to be larger compared to the electrical receiver case, which introduced the need for RF line amplifiers. The frequency combs were again calibrated to account for the frequency dependent attenuation of the electrical path. For ring one, there were 20 tones spaced from 1.0 GHz to 20.0 GHz and for ring two there were 20 tones spaced from 0.5 GHz to 19.5 GHz. Our OSA measurement approach offered several advantages compared to the electrical spectrum analyzer approach. First, it required less equipment, so the setup was less complex, potentially less expensive, and faster because there was no need to switch equipment. Second, the frequency comb calibration needed to account for fewer elements because there was no electrical path on the receive side, which had the potential to produce higher precision measurements. Finally, the OSA approach future-proofed the system for increasing device modulation bandwidths. Electrical spectrum analyzers have a maximum frequency, but with the OSA approach increased modulation frequencies result in modulation sidebands further away from the laser frequency.

7.3.5 Optical Receiver Results

Figure 7.19 shows the measurement steps taken in the OSA to determine the WDM modulator bandwidths. Images (a) through (c) show the tuning of the micorings with overlapping resonances. Image (d) shows the optical spectrum with the laser set at 1546.0 nm and both frequency combs turned on, with the modulation sidebands generated by the frequency combs clearly visible. Similar to the electrical receiver, the received frequency tones were separated into the two separate combs, which were then used to generate the bandwidth responses of the modulators. The bandwidth curves from this approach were not as clean as the electrical receiver setup, which could be due to the OSA resolution of 150 MHz. OSAs with higher resolutions exist and would improve

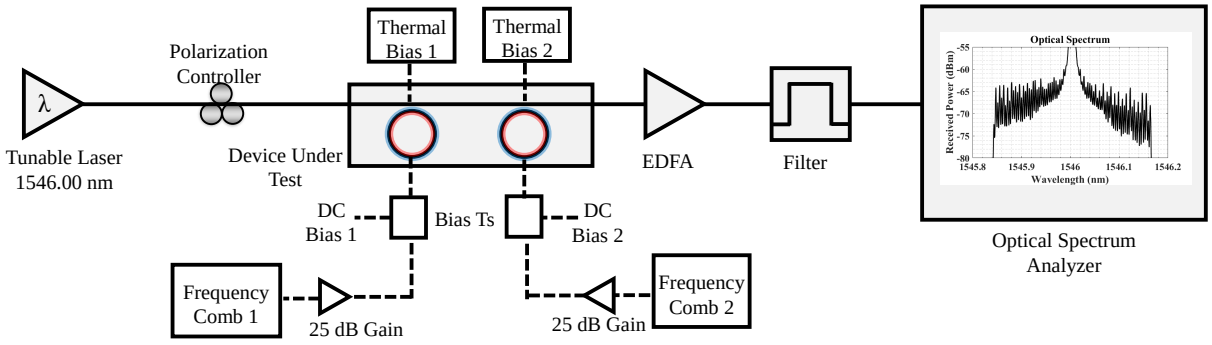

Figure 7.18: The experimental setup for the optical receiver approach. A tunable laser is coupled into the WDM modulator. The microring modulators are each driven by an independent frequency comb that is calibrated to account for the electrical signal path attenuation. The output of the WDM modulator is amplified and filtered before being received by an optical spectrum analyzer.

the results. Additionally, there was a noticeable asymmetry in image (d) which was a result of differences in DC power due to the laser positioned on one edge of the superimposed modulator resonances. From image (f), we determined the 3 dB bandwidth for ring one to be approximately 10 GHz and for ring two to be approximately 14 GHz. It should be noted that the rings used in the electrical and optical experiments were not the same modulators.

7.3.6 Conclusions

We developed a testing strategy to enable faster bandwidth characterization of serial WDM modulators by applying calibrated offset frequency combs to separate modulators, allowing simultaneous measurement of multiple modulators. Additionally, we expanded the idea to an all optical receiver setup that simplified the measurement process by removing the need to switch between optical and electrical receivers. The testing strategy was demonstrated on a WDM microring modulator chip, and 3 dB modulation bandwidths were determined to be 9.2 GHz and 15.5 GHz. As silicon photonics device testing strategies continue to grow in importance, this characterization approach will simplify measurements and reduce measurement time.

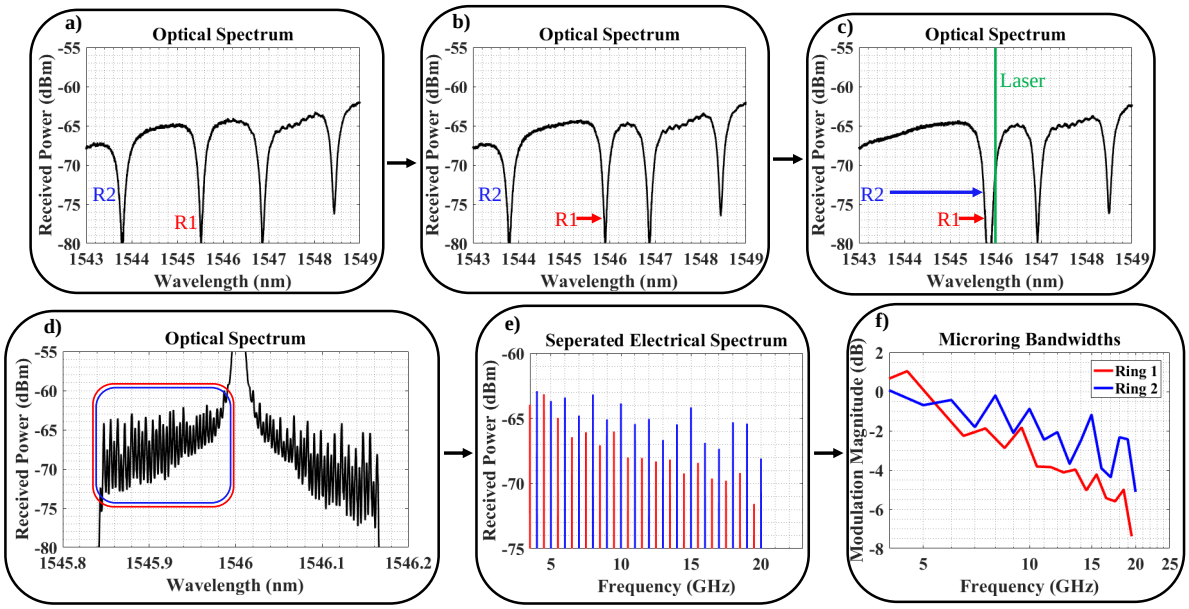

Figure 7.19: a) The initial optical spectrum. b) Ring 1 tuned. c) Ring 1 and 2 tuned. d) The spectrum with the laser on and frequency combs applied. e) The separated frequency combs. f) The resulting frequency responses of the rings.

7.4 Silicon Photonic Deserialization for Energy Efficient Links

We developed a novel optical deserialization system in silicon photonics to reduce electrical deserialization power consumption and improve receiver sensitivity. The results demonstrated a path to increasing receiver sensitivity by 2.5 dB with improved modulators.

7.4.1 Introduction

With the limit that Exascale systems have to operate on less than 20 MW [196], optimizing power consumption in optical links becomes an important consideration. Optical links operate at tens of Gbps despite the fact that the surrounding CMOS electronics operate more efficiently at slower data rates [130]. Energy consumption in optical transceivers that is rate independent, such as thermal stabilization, push the optimal data rate to higher speeds. Additionally, a higher data rate creates a compromise between energy efficiency and throughput [197].

There are several benefits for operating optical links at slower data rates. Electrical receiver

sensitivities increase with slower data rates [130] since the smaller receiver bandwidth integrates over less input referred noise, which goes as f^2 [198]. This reduces the required laser power, significantly reducing the energy consumption of the link due to the low wall-plug efficiencies of lasers (on the order of 15% for on chip lasers) [199]. Additionally, higher data rates in optical links require electrical deserialization, which consumes mWs of power [116]. Optical deserialization could create an attractive compromise. Data is modulated and routed at higher serial data rates to operate at the energy efficient rate for thermal stabilization, and to increase throughput. On the receive side, the data is optically deserialized to take advantage of the increased receiver sensitivity and to reduce the energy consumed by electrical deserialization.

We proposed and demonstrated an approach for optical deserialization in silicon photonics. Serial bits of the data stream were alternatingly routed to two outputs of a MZM synchronized with the data, which operated as a fast switch. The switched data streams were then each sent to electro-optic delay lines to stretch the data, producing two parallel data streams at half the rate of the original serial data transmission. For optical deserialization to be more energy efficient, the gain in receiver sensitivity must be greater than the sum of all the power penalties associated with the deserialization process, which include the MZM's insertion loss (IL) and any power penalties associated with degradation of data quality during the deserialization process (PP_{Des}). Fitting a trendline to the collection of receiver sensitivity versus data rate presented in [130] suggests that reducing the data rate from 10 Gbps to 5 Gbps could increase the receiver sensitivity by 7.5 dB. Since ILs of less than 2 dB have been demonstrated [200], there exists a window to improve the link's energy efficiency with optical deserialization if PP_{Des} is less than 5.5 dB.

7.4.2 Experimental Setup

Serial PRBS 2^{15}-1 data generated at 10 Gbps with a commercial modulator was coupled into a SiP MZM with two outputs, fabricated at the AIM Photonics foundry (Figure 7.20). The MZM was driven with a stream of alternating ones and zeros at 10 Gbps to act as a switch. The MZM was synchronized so the transitions occured at the same time as the transitions in the data. This

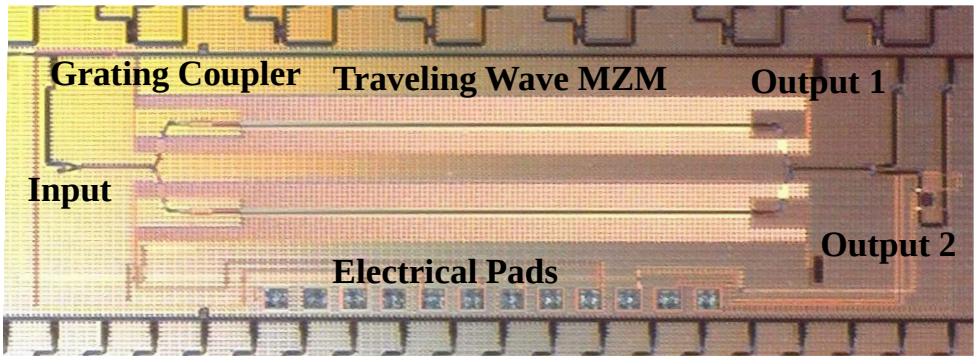

Figure 7.20: The fabricated device used for the optical deserialization. Grating couplers are used to connect to a dual output MZM, with pads for probing.

resulted in splitting the data into two parallel paths where each path was gated to produce valid data every other 100 ps window. The gated data was converted into continuous 5 Gbps data by evenly splitting it into two arms. Each of the two arms were converted to an electrical signal with a receiver consisting of a photodiode and a transimpedance amplifier (TIA). Before the electrical signals were combined together, one arm was delayed by 100 ps with a tunable electrical delay, so that the end of the 10 Gbps pulse in the leading arm coincided with the beginning of the 10 Gbps pulse in the trailing arm. The result was that the data window was doubled to 200 ps, resulting in a 5 Gbps data stream. The combined signal was amplified with a limiting amplifier (LA). The same process occured in the path from the second output of the SiP switch, producing two parallel 5 Gbps data streams.

7.4.3 Results

Due to the high coupling loss for the SiP chip, the received power was measured after the chip. The BERs for the two deserialized outputs of the SiP chip are shown along with the BER of the original 10 Gbps data in Figure 7.23. The SiP modulator's extinction ratio was 4 dB, meaning the modulator only partially gated the 10 Gbps signal when it should have been zero (Figure 7.22). Additionally, the SiP's rise/fall times were slower than the rise/fall times of the commercial

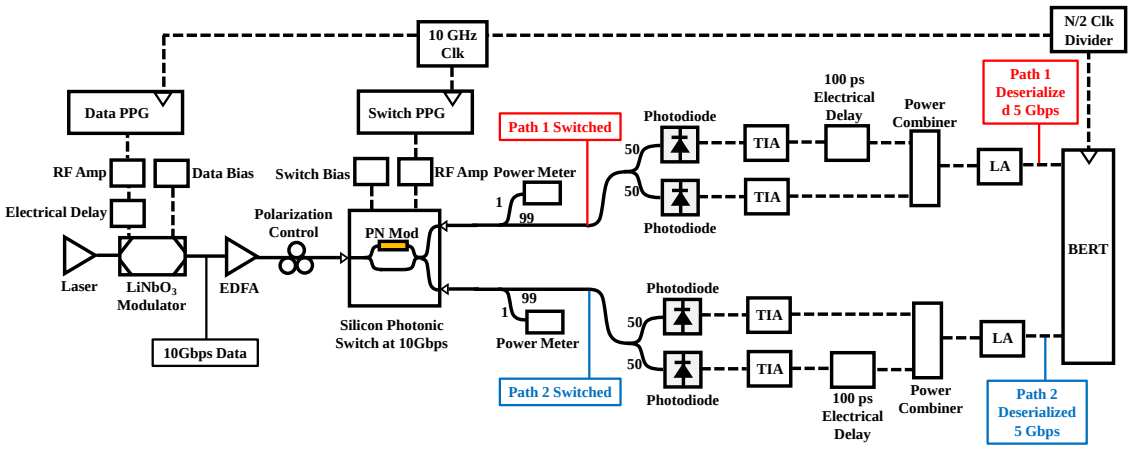

Figure 7.21: The experimental setup with the two output SiP modulator acting as a fast switch to gate the serial data. The gated data is stretched to half the initial data rate in the two electro-optic delay lines.

modulator, resulting in multiple transitions in the gated data. These effects resulted in a PP_{Des} of 4.7 dB when measured at a BER of 10^{-12}. The deserialization experiment was repeated using a commercial modulator as a single output switch to improve the extinction ratio and rise/fall times. With this approach, PP_{Des} was reduced to 3.0 dB. Since the break-even point is a PP_{Des} of 5.5 dB, optical deserialization with the SiP modulator results in a 0.8 dB improvement, and the results from the commercial modulator show that a 2.5 dB improvement is possible with an improved SiP modulator.

7.4.4 Future Prototype

A second version of the optical deserializer was fabricated so that the delay process occurs in the optical domain. Following a fast MZI switching modulator, the delay arms incorporated a polarization splitter and rotator to transform the delayed portion to TM light. As a result, the TE from the non-delayed arm will not constructively or destructively interfere with the TM light from the delayed arm at the integrated photodiode. The output from the photodiode goes directly to the input of a TIA, as two TIAs are designed to be flipped on top of the PIC. Since the photodiode's responsivity is expected to be lower for TM light, a thermal switch is placed before the delay arms

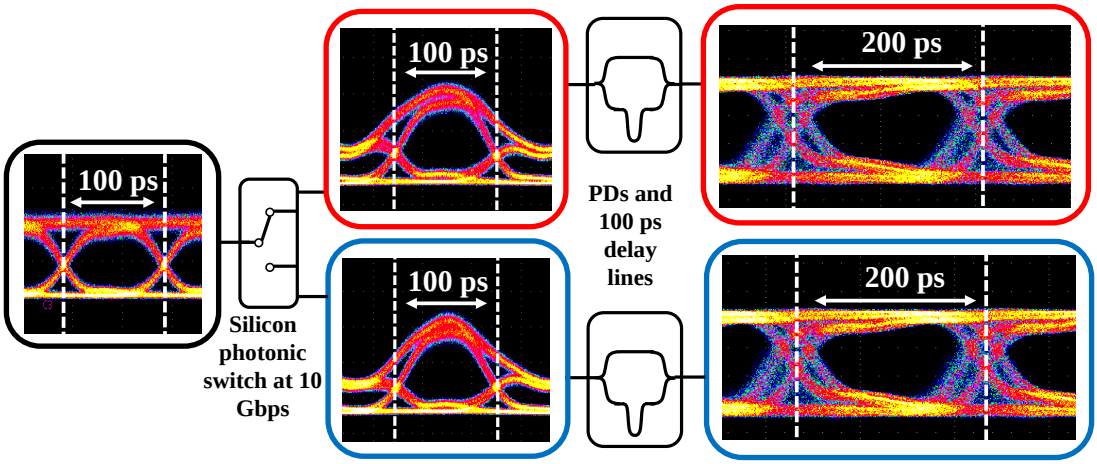

Figure 7.22: The eye diagrams for the initial data, the gated data, and the parallel deserialized data.

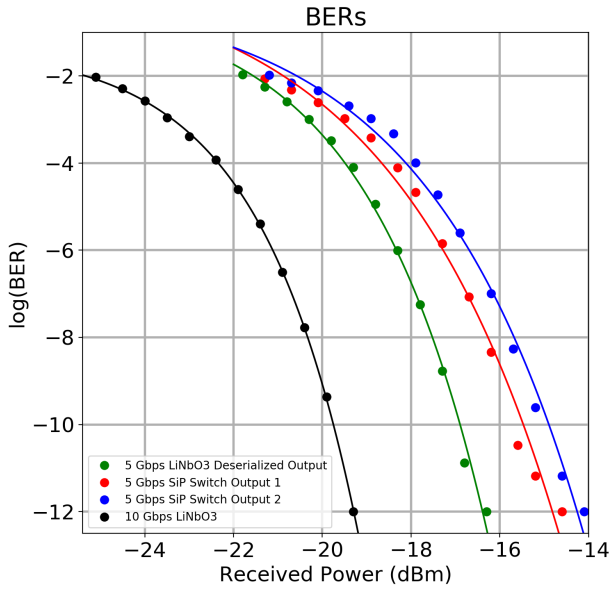

Figure 7.23: The BERs for the initial data (black), the SiP deserialized data (red and blue), and the commercial modulator's deserialized data (green).

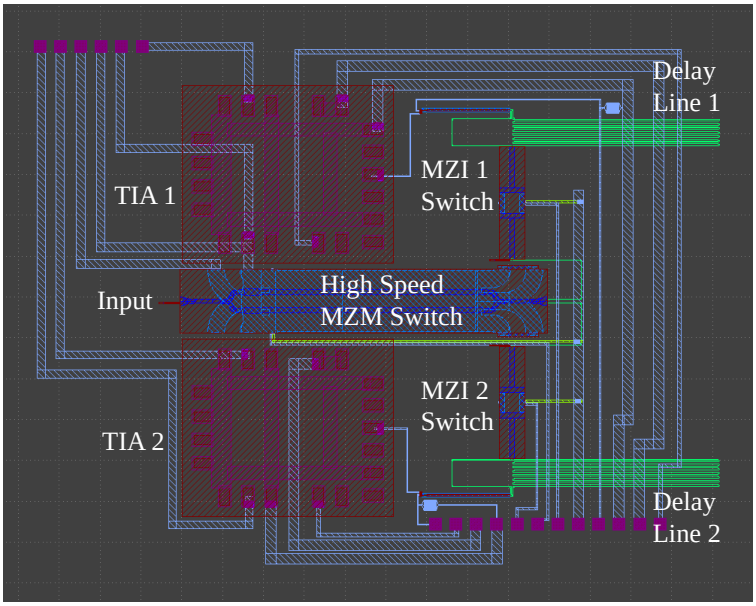

Figure 7.24: The GDS of the future optical deserialization prototype, showing the high speed MZM switch with two outputs with their respective delay lines.

in place of directional coupler, to allow for the splitting of light to tuned to match the difference in responsivity. The device is designed to be electrically probed at a 100 um pitch.

7.4.5 Conclusions

We developed a method of optical deserialization using a SiP dual output modulator as a fast switch synchronized with the serial data, followed by an electro-optic stretching system to convert serial 10 Gbps data into two parallel 5 Gbps data streams. Optical deserialization resulted in the potential for a 0.8 dB improvement with the SiP modulator and 2.5 dB improvement with a commercial modulator. This approach demonstrates the ability to reduce optical link power consumption by removing the need for electrical deserialization and reducing the required laser launch power due to the increased sensitivity of electrical receivers at slower data rates, which is greatly amplified by the poor wall-plug efficiencies of lasing systems.

Chapter 8: Conclusions

8.1 Summary of Contribution

The work presented in this dissertation focused on developing and integrating and silicon photonic devices and subsystems for their insertion into data centers and other high performance interconnect systems. Silicon photonics offers a promising path towards overcoming the bottleneck facing electrical interconnects to keep up with the exponential growth of data traffic. One of the major challenges for the widespread deployment of silicon photonics with real data generating systems is the integration of the photonics with the driving electronics and compute nodes such as CPUs, FPGAs, and ASICs. If the photonics is improperly integrated all the potential benefits may be negated, and result in limiting transceiver bandwidth and increasing transceiver energy consumption.

With these goals in mind, we developed a silicon photonic multi chip module 2.5D integrated transceiver which combines a microdisk based WDM PIC transceiver with commercial bare die TIAs and a thinned silicon interposer to provide signal fan out. This prototype is the first demonstrated 2.5D integrated silicon photonic transceiver utilizing microresonator modulators and demultiplexers. In the first portion of the dissertation, we discussed the prototype's architecture, integration, characterization, performance, and scalability. Through developing the prototype, key design considerations for MCM transceivers were identified: integration approach, photonic equivalent circuit modelling, PIC to EIC interface modelling, MCM data I/O modelling, and design for assembly. The identified design considerations include were then used in the development of the additional prototypes, which were discussed in the remainder of first portion of the dissertation. These additional prototypes included a 2.5D integrated transceiver with custom driving EICs, a 3D integrated receiver with a custom driving EIC, and a 3D integrated network on chip utilizing an

active interposer.

In the second portion of the dissertation, we discussed additional work that indirectly supports the development of integrated silicon photonic multi chip module transceivers. This work included analyzing thermal crosstalk from areal dense microdisk modulators to determine the modulator pitch at which thermal crosstalk becomes significant in transceivers. Additionally, the second portion of the dissertation overviewed several iterations of custom microresonator modulators, which provided the platform for improving transceiver design by allowing for optimization based on key interconnect parameters, such as bandwidth, FSR, and energy efficiency. The theory, design, and performance of the various custom microresonator modulators were presented. The design and performance of several higher order modulation format transmitters were presented in section two. Higher order modulation presents another avenue for scaling up total throughput in silicon photonics transceivers. The transmitters included modulators constructed from Mach Zehnders, microrings, and microdisks, and included formats such as PAM-4, QPSK, and QAM-16. Finally, the second portion of the dissertation included work supporting the development of silicon photonic transceivers in a broad sense and included the development of high volume bandwidth testing strategies and analysis of the interconnect performance of graphene assisted silicon modulators.

The development of multi chip module silicon photonic transceivers, custom microresonator modulators, and higher order modulation format modulators are key components in the deployment of silicon photonic transceivers in high performance interconnect systems.

8.2 Recommendations for Future Work

The work in this dissertation provides the foundation for a number of research projects to continue the development of silicon photonic multi chip module transceivers. The most direct avenue for future work is to test the prototypes that are finishing fabrication–the 2.5D integrated MCM with custom EICs and the 3D integrated network on chip active interposer. Through fabrication in a 28 nm process, optimization for low energy consumption, and clock forwarding, the 2.5D integrated MCM with custom EICs should provide a significantly improved pJ/b performance. The

3D integrated network on chip prototype should improve performance by moving to a reduced parasitic integration approach, and would be the first thinned photonic MCM network on chip demonstration.

The performance of MCM integrated transceivers can continue to be improved through future work. The performance of the earlier prototypes was likely hampered by packaging parasitics. Future prototypes should continue to improve by reducing the parasitics to improve bandwidth and energy consumption. Additionally, future prototypes can look to scale up in terms of total throughput and areal bandwidth density, by increasing the channel counts and reducing the pitch between transmitter modulators and receiver photodiodes.

An additional avenue for future work is characterizing the coupling modulators with varying junctions due back from fabrication in July 2020. These modulators will help determine the optimal junction to employ in future microring modulators, and provide an avenue for developing a custom modulator that can serve as the base modulator platform that can be fine tuned to optimize based on the interconnect performance of interest, such as FSR, channel bandwidth, or energy efficiency.

A final approach for future work is the continued development of microresonator based, higher order modulation format, modulators. Initially, this involves characterizing the QAM-16 microdisk based transmitter and the PM WDM QPSK modulator, but should evolve into optimizing their performance. Additionally, overcoupled custom modulators provide an avenue to explore microresonator phase modulators, which allows for small footprint phase modulators for WDM operation. Custom overcoupled microresonator modulators also provide an approach for continuing to explore arbitrary QAM modulation with two microresonator modulators.

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Appendix : Relevant Author Publications

- **N. C. Abrams**, M. Glick, and K. Bergman, "Silicon Photonic Multi-Chip Module Interconnects for Disaggregated Data Centers," *Conference on Optical Network Design and Modeling*, May 2020.

- **N. C. Abrams**, Q. Cheng, M. Glick, and K. Bergman, "Thermal Crosstalk in Silicon Photonic Microdisk Modulators for Ultra-Compact Dense-WDM Systems," *Optical Interconnects Conference*, June 2020.

- C. Browning, Q. Cheng, **N. C. Abrams**, L. Y. Dai, M. Ruffini, L. P. Barry, and K. Bergman, "A Silicon Photonic Switching Platform for Flexible Converged Cloud Radio Access Networking," *Journal of Lightwave Technology*, September 2020.

- **N. C. Abrams**, Q. Cheng, M. Glick, M. Jezzini, P. Morrissey, P. O'Brien, and K. Bergman, "Silicon Photonic 2.5D Integrated Multi-Chip Module Receiver," *Conference on Lasers and Electro-Optics*, May 2020.

- **N. C. Abrams**, Q. Cheng, M. Glick, M. Jezzini, P. O'Brien, and K. Bergman, "Silicon Photonic 2.5D Multi-Chip Module Transceiver for High-Performance Data Centers," *Journal of Lightwave Technology*, March 2020.

- **N. C. Abrams**, Q. Cheng, M. Glick, E. Manzhosov, M. Jezzini, P. Morrissey, P. O'Brien, K. Bergman, "Design Considerations for Multi-Chip Module Silicon Photonic Transceivers," *Photonics West*, February 2020.

- Q. Cheng, Y. Huang, H. Yang, M. Bahadori, **N. C. Abrams**, X. Meng, M. Glick, Y. Liu, M. Hochberg, and K. Bergman, "Silicon Photonic Switch Topologies and Routing Strategies

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- Y. Shen, X. Meng, Q. Cheng, S. Rumley, **N. C. Abrams**, A. Gazman, E. Manzhosov, M. Glick, and K. Bergman, "Silicon Photonics for Extreme Scale Systems," *Journal of Lightwave Technology*, Volume 35, Issue 2, February 2019.

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