LIGHT-LOAD POWER MANAGEMENT IN DIFFERENTIAL POWER PROCESSING SYSTEMS

BY

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DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2020

Urbana, Illinois

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ABSTRACT

Series stacking is used as a means of implicitly raising DC bus voltages without additional power processing and has been explored widely in the context of photovoltaic sources and batteries in the past. More recently it has also been explored in the context of server loads and microprocessor cores. Supplying power at a higher voltage supports a reduction in conduction losses and reduces complexity in power supply design related to the high current at low voltage nature of microprocessor loads.

However, series stacking of DC voltage domains forces the dc voltage domains to share the same currents. In the context of series stacked loads, this would lead to failure of voltage regulation of individual dc voltage domains. Additional power electronics, commonly referred to as differential power processing (DPP) units are required to perform this vital task. The idea is to let the DPP converters (which need to have bidirectional capability) process the difference between currents of adjacent voltage domains, so that the load voltages are regulated.

Although series stacking and DPP has been explored in significant detail, the importance of light load efficiencies of these DPP converters has not been highlighted enough in the past. In this document we discuss the importance of light load control in common series stacked systems with DPP and propose a light load power management scheme for bidirectional buck-boost converters (which is the building block of most DPP converter topologies). Extending efficient operation load range of converters (to process higher power in rare heavily mismatched conditions and to maintain good light load efficiencies at the same time) with multiphase converters and asymmetric current sharing is also discussed in the context of DPP converters. We finally propose to build a series stacked system of low voltage loads and DPP regulators to demonstrate the advantages of series stacking as opposed to the conventional parallel connection.

To my parents, for their love and support.

ACKNOWLEDGMENTS

It has been almost seven years since I came to Champaign-Urbana, and it has been an incredible journey as a graduate student at one of the best engineering schools in the world. I would like to thank my advisor Professor Philip T. Krein for accepting me into his research group and giving me the opportunity to grow and learn from the amazing people here at the University of Illinois at Urbana-Champaign. I am grateful for his guidance and valuable insights into our project, and in general for always directing me towards the correct track.

I would also like to thank Professor Robert Pilawa-Podgurski, Professor Pavan Kumar Hanumolu, Professor Arijit Banerjee and Professor Andrew Stillwell for serving on my doctoral committee and providing valuable feedback that has helped in improving the content of this dissertation. I would specially like to thank Professor Pilawa and Professor Banerjee for letting me be a Teaching Assistant for ECE 469. Serving as a Teaching Assistant for the Power Electronics Lab was one of the best learning experiences I have had in the past years.

I am grateful to have had Srikanthan Sridharan, whose energy and positive attitude I look up to, as a friend/colleague/mentor-of-sorts for my first two years over here. I must also thank Jason Galtieri for his friendship right from the beginning of this journey. Thanks to Enver Candan and Andrew Stillwell whose work on DPP and insights have helped me improve my own work. Also I want to acknowledge the support of Chris Barth, Andrew Yoon, Phuc Huynh, Melody Yi, Siddhartha Nigam, Adriano Abrantes, Avinash Madavan, Shivang Agrawal and many other former and present members of the Power Group, without whom my experience would not have been so enjoyable. Special thanks to Joyce Mast and Robin Smith for their administrative support and for organizing the many social events that bring the Power Group together. Thanks to Kevin for managing the research and teaching labs and for always being there to help me find equipment.

Thanks to Grainger Center for Electric Machinery and Electromechanics (CEME), without whose generous support this research would not have been possible.

Finally, I would like to express my gratitude to my parents, who have always selflessly supported me in every decision I have made and through everything I have wanted to pursue. This dissertation would not have been possible without that, and is dedicated to them.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 Series stacking of loads

Modern microprocessor loads need low voltage supplies (typically 0.7 V - 1.3 V after the final power stage, which might be integrated on the microprocessor die itself) and at the same time the currents sinked can be in excess of 100 A. These extreme high currents at low voltages make voltage regulator design very difficult as PCB impedances start playing a big part in determining output impedance of converters. Along with that, microprocessor load transients can be very fast. Intel's Voltage Regulator Module (VRM) [1] specifications indicate that slew rates in excess of 300 A/μs can be encountered. To ensure that these high slew rates (inductance limitations) and high load currents (resistance limitations) can be supported, PCB impedances between the VRM and the actual microprocessor cores need to be extremely low. This requires carefully designed power delivery networks to be placed between the VRM and the microprocessor core to regulate the impedances. Fig 1.1 shows a typical model of impedances between a VRM and the processor. The VRM itself has some bulk capacitance (electrolytic) placed at its output. These bulk capacitances (several millifarads) are capable of storing a lot of energy, but due to their build they have significant parasitic inductance which make them slow to respond to load transients. The next stage in the power delivery network is the bank of some high frequency multilayer ceramic capacitors (MLCC) placed at the edge of the microprocessor mount on the motherboard. These capacitors are responsible for compensating the inductive effect of the PCB between the VRM and the microprocessor. Some more capacitance is placed inside the microprocessor socket itself to compensate for the effect of the PCB layer between the edge of the processor and the processor pins.

The voltage regulator itself may be modeled as a controlled current source with limited bandwidth due to limited slew rate of the inductor current. Processor specifications allow for a slight droop in output voltage with load current and provide a target load line (Z_{LL}) in their datasheets. This load line is usually less than 1 mΩ (at 100 A load current, load voltage

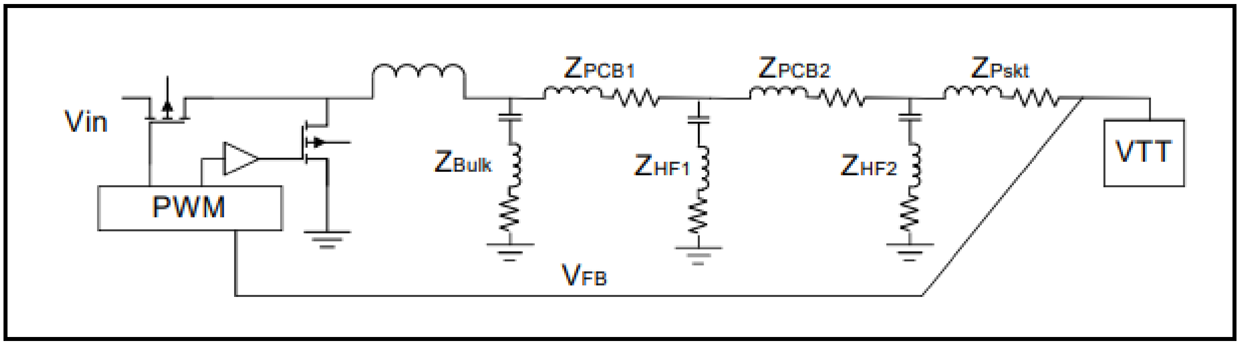


Figure 1.1: Typical voltage regulator parasitic impedances and capacitor distribution for modern microprocessors. Figure adapted from [1].

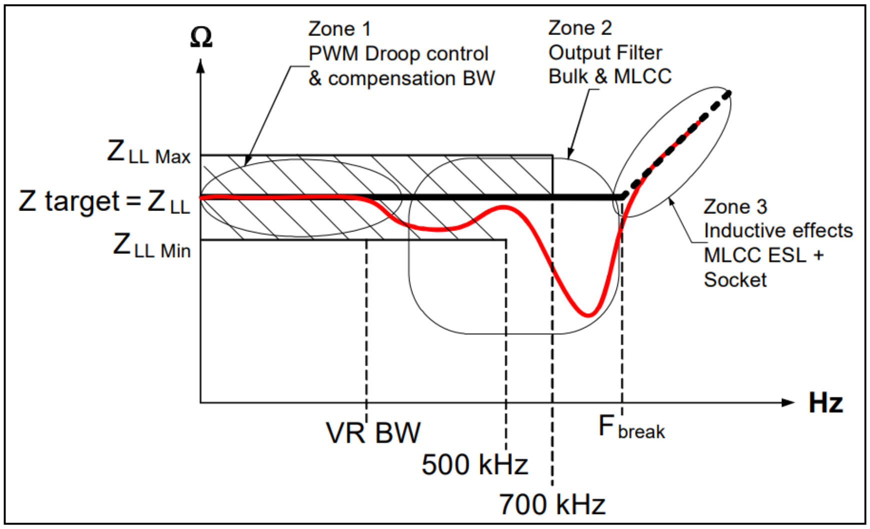


Figure 1.2: Expected voltage regulator load line. The targeted Z_{LL} is usually less than a mΩ. Figure adapted from [1].

may not deviate below 10 mV of the set point). The inductor current cannot respond fast enough if the load current perturbation occurs faster than the bandwidth of the VRM. For those cases, voltage regulation is the responsibility of the capacitances in the power delivery network. The bulk capacitances cannot respond to perturbations beyond 500 kHz due to their parasitics. The MLCC capacitances placed in the socket and near the processor can offer low impedances up to a few MHz. Beyond that frequency, it is not possible to regulate the load line to be held below the target Z_{LL}. Fig 1.2, from [1], shows a typical load line expected from a VRM and power delivery network supplying a modern microprocessor. To limit the effect of the socket inductance (Z_{pskt}), often more than half of the pins connecting the PCB and the microprocessors are dedicated to power supply and ground.

To counter PCB and socket impedance related problems, some microprocessors have added

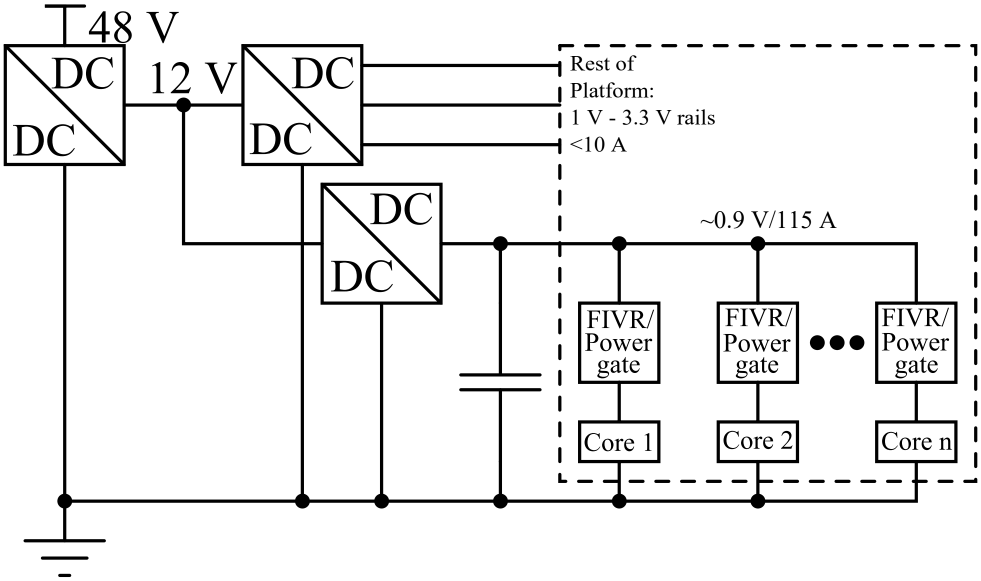


Figure 1.3: General architecture for power delivery to a microprocessor.

fully integrated voltage regulator (FIVR) modules to step down the core voltage internally from a slightly higher voltage supplied from on board VRMs. Microprocessors that tend to sink more than 100 A of current also tend to have a number of cores for improved processing power. These cores may be supplied by separate integrated voltage regulators allowing independent control over core voltages. This ensures that each core can be supplied from a separate voltage rail and allows for optimization of power consumption by dynamic voltage frequency scaling (DVFS) [2], [3], [4].

Some of Intel's 4th generation of processors required a 1.8 V rail that was rated up to 200 A [5], and highly paralleled FIVRs were implemented on the package and the die itself to step down the 1.8 V rail to core voltage (0.7 V - 1.3 V). The FIVRs were designed to be capable of delivering 400 A of current (700 A limited by thermal management and input power stage [6]) by employing a massively paralleled system of hard switched buck converters. This was implemented in the processors which consume excessive amounts of power (highest clock rates and core counts) so that current ratings of on board voltage regulators do not exceed efficient power delivery limits, and have more relaxed output impedance requirements. Integrated voltage regulators tend to be inefficient due to hard switching at very high switching frequencies. Even though efficiencies nearing 90% ([7], [8]) have been reported, this is not nearly enough since the density at which these converters are integrated is too high. For a chip that already dissipates 200 W of power, an additional 20 W of power dissipation due to integrated voltage regulator inefficiencies might prove to be a thermal bottleneck.

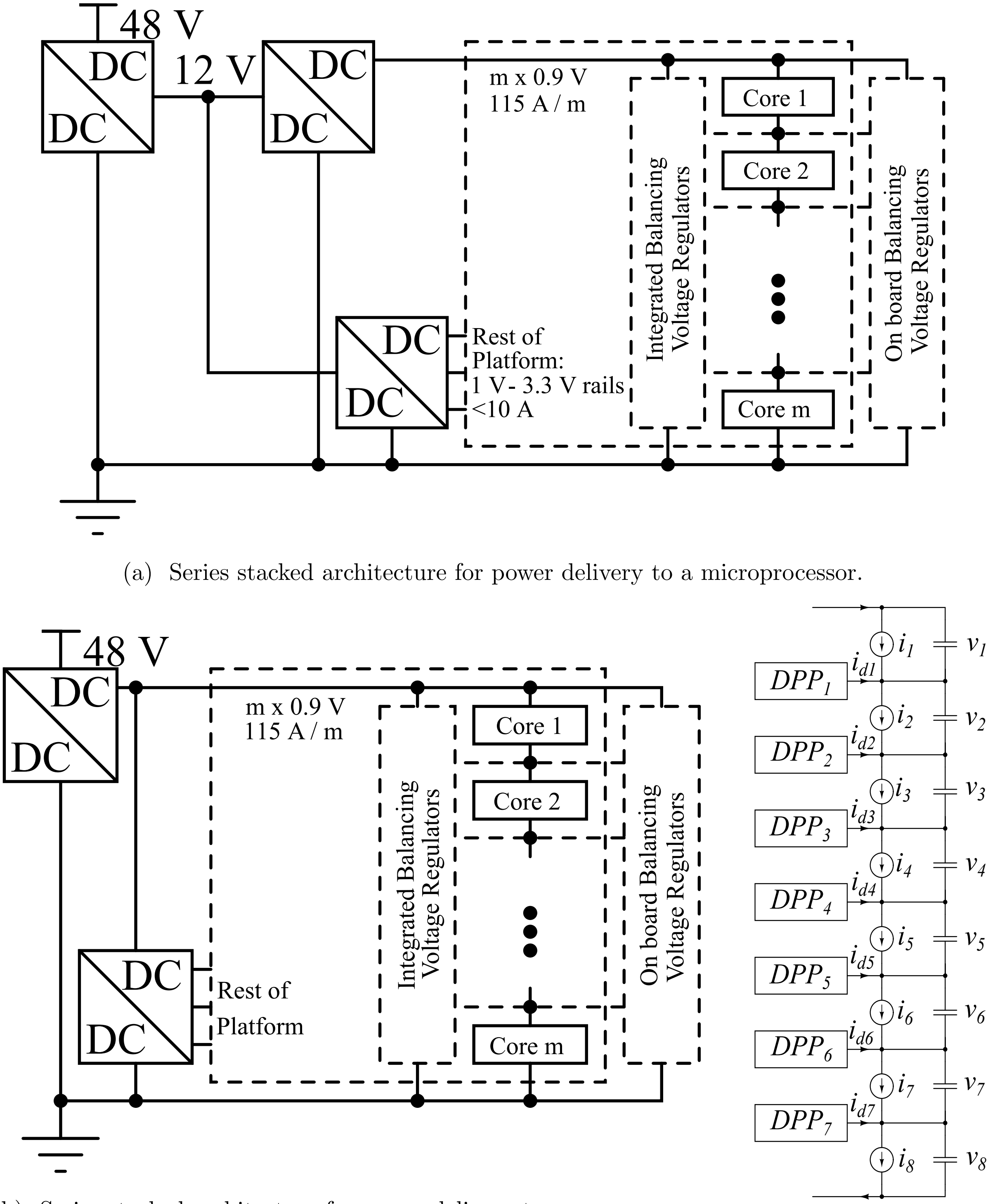
Some of the processors in the later generations discarded the idea of integrated voltage regulators, and other measures such as power gating ([9], [10], [11]) were introduced to reduce power consumption of processors. A single low voltage rail regulated by on board voltage regulators supplies the cores of the processor, but power gates are introduced to disconnect parts of the digital logic when they are not in use. The processor itself employs DVFS by communicating with the on board VRMs, but independent optimization of core voltages is not possible (and probably not necessary for most cases). However, this allows for a reduction in static power consumption due to leakage in new semiconductor processes.

The general power delivery architecture for processors on a motherboard is shown in Fig 1.3. Recently there has been a significant amount of research on extreme duty ratio power conversion such as 48 V - 1 V for high current systems. While it was previously expected that such a step down conversion has to be done with two stages with a 12 V rail as an intermediate bus, direct 48 V - 1 V conversion may soon become typical in most telecommunication systems. Some of the proposed topologies for direct 48 V - 1 V conversion involve transformer based step down [12], [13] or coupled inductor based step down conversion [14], [15]. These topologies require bulky and complicated transformer or coupled inductor designs due to high current ratings of the low voltage windings. Other solutions involve some type of implicit step down using switched capacitor and switched inductor hybrid converters such as the series capacitor buck converter [16] or the multi-inductor hybrid converter [17] or the quadruple step down buck converter [18]. While these are inherently more power dense than the magnetics based step down converters, they suffer from less than ideal PWM duty ratio limitations or poor light-load power management, and in general more research is necessary to make direct 48V-1V high current power supplies viable for deployment on motherboards.

The complexity and inefficiency of delivering power at a low voltage and high current has inspired ideas that allow power delivery at a higher voltage, such as core unfolding [19] and series stacking [20], [21], [22], [23]. Stacking the n processor cores in series instead of the conventional parallel connection intrinsically increases supply voltage by n times and the supplied currents decrease by the same factor. This supports an n^2 order increase in power supply impedance, which simplifies its design. Rating limitations on a semiconductor process may prevent all n cores to be connected in series, but building an IC with m series connected domains and placing the cores in an $m \times \frac{n}{m}$ array is possible.

The idea is illustrated in Fig 1.4a. Depending on how many voltage levels can be reliably stacked in a single chip, it might be possible to reduce the number of power conversion stages in the system. For example, it might be possible to convert the rail supplying the stack of cores into a 3.6 V rail ($m = 4$ for nominal core voltage of 0.9 V) and derive all other lower power voltage rails (Rest of Platform) from there. The idea is illustrated in Fig 1.4b.

Conventional buck converter designs become inefficient at extremely low duty ratios and



(a) Series stacked architecture for power delivery to a microprocessor.

(b) Series stacked architecture for power delivery to a microprocessor. A power stage can be reduced without extreme duty ratio power conversion.

(c) General balancing voltage regulator architecture.

Figure 1.4: Series stacking architecture and differential power processing.

series stacking processor cores would simplify bulk power delivery to processors. If there is some software overhead to match core power consumption in an average sense, series stacking would lead to higher system level efficiencies. One of the reasons for a system level efficiency improvement is that the converter supplying the stack does not need to process power at an extreme duty ratio anymore. However, voltage regulation of the intermediate domains adds complexity to the power delivery system. If there is mismatch between each of the consecutive load domains, voltage regulation fails. Balancing remaining mismatches is the responsibility of the balancing voltage regulators. The general architecture of the balancing voltage regulators is shown in Fig 1.4c. The dynamics of the balancing action can be described by:

$$C\frac{d}{dt}\left(v_{k+1} - v_k\right) = i_{dk} + \left(i_k - i_{k+1}\right) \tag{1.1}$$

where C is the net capacitance across each voltage domain and the current injected at each node i_{dk} is considered a control input. Depending on the dependency of the load currents i_k on the domain voltages v_k (resistive, constant current or constant power or a mix), a stabilizing control law can be designed. Under stable operation at steady state,

$$I_{dk} = I_{k+1} - I_k \tag{1.2}$$

This forms the essence of differential power processing. The balancing converters are only required to process the difference between the currents of consecutive domains. If low mismatches are ensured, the balancing regulators need to process only a fraction of the total power delivered to the loads unlike the two stage power delivery scheme of Fig 1.3. It should be noted that when the system operates at near peak power, the balancing converters inherently process very little power. The efficiency of the stack is expected to be near unity and overall system level efficiency is limited only by the efficiency of the converter that processes bulk power and regulates the stack voltage (referred to as the stack converter). Even if we consider that the efficiency of our balancing converters is at par or slightly lower than that of the converter supplying the core in the architecture of Fig 1.3, we can expect higher system level efficiencies from the series stacked system.

There has been research in the past on voltage regulation in series stacked digital loads. Recently series stacking has been successfully attempted with loads such as servers, [24] and hard drives [25]. The series stacked architecture allows direct power delivery from a high voltage bus (48 V) to the servers (48 V to four 12 V series stacked domains) and the hard disks (50 V to ten 5 V series stacked domains). DPP converters are used to provide voltage regulation for individual loads. This has been shown to eliminate one or more power conversion stages allowing improved system efficiencies. Given the opportunity to match server loads, efficiencies beyond 99% have been reported. Series stacking has also been explored in the context of microprocessor/core loads [21], [23], [26], [27].

The proposed series stacked architecture in [21] uses push-pull linear regulators for processing the differential currents between series connected domains. Power delivery to a chip with three 1.8 V domains from a 5.4 V rail was demonstrated [22]. Although linear regulators provide excellent regulation bandwidth, they are inefficient and would lead to low system efficiencies if tight matching of core power is not ensured. The architectures in [28], [27] show the use of a switched capacitor ladder converter for equating voltages of series connected DC domains. In [27] a series stack of four 0.9 V domains was implemented in an IC and core power balancing with dynamic frequency scaling was also demonstrated. Switched capacitor DPP converters are very efficient at light loads, and light-load efficiency is what we are going to discuss in the next subsections. However, in a stack with switched capacitor voltage balancing converters, only domain voltage equalization (with a load line dependent on mismatch) is possible [28]. Voltage equalization does not support localized adaptive voltage for a series stacked microprocessor system. This problem might not be significant enough to discard the idea of switched capacitor balancers entirely, since our main assumption (motivation for series stacking) is that the load in each domain will be matched for most of the time and localized voltage scaling for each domain might not be necessary.

Several different topologies for switched mode DPP regulators can be derived from architectures proposed for charge equalization of series connected battery strings [29] and for optimized photovoltaic power generation [30]. Of these architectures, transformer based DPP topologies (such as load-to-virtual bus [24], or direct load-to-load [25]), although very scalable, are not easily integrated on chip. The original bus-to-load architecture proposed in [31] would have some DPP converters operating in extreme duty ratios, a scenario which we are trying to avoid. The load-to-load architecture (Fig 1.5) is scalable, and also easily integrable because of lower switch voltage ratings.

1.2 Switched inductor ladder topology

The switched inductor ladder converter [32] (or the buck-boost element-to-element topology [31]), shown in Fig 1.5, is one possible option for balancing converter implementation that allows independent voltage regulation of the domains. This topology has been widely studied in literature in other applications where series stacking is important such as battery balancing [33], and photovoltaics [34], [35], [36]. Duty ratio control of individual DPP

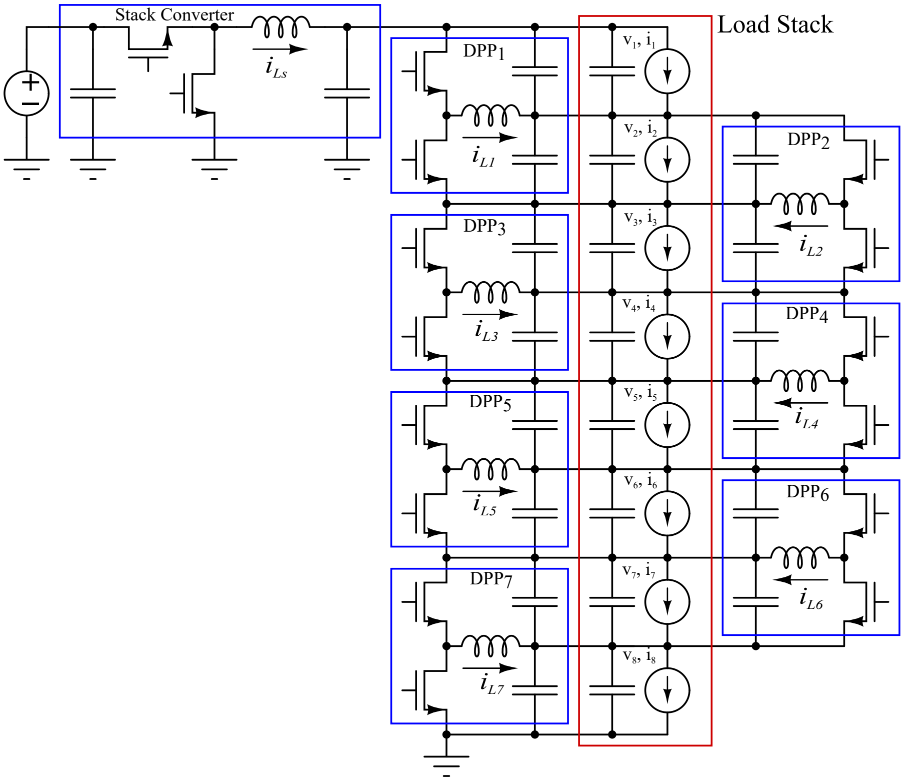


Figure 1.5: Switched inductor ladder topology for voltage regulation of a series stack.

converters allows independent domain voltage control. This topology has been popular in recent research on the topic of series stacking of low voltage loads as well, the primary reason being the modularity of the topology. The switch ratings required for the DPP converters are low (double the maximum voltage of each domain), which makes it suitable for on chip integration.

Consider stable steady state operation of the ladder converter in Fig 1.5. The steady state inductor currents in this topology are

$$\begin{bmatrix} -D_1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ D_1' & -D_2 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & D_2' & -D_3 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & D_3' & -D_4 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & D_4' & -D_5 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & D_5' & -D_6 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & D_6' & -D_7 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & D_7' & 1 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ I_{L5} \\ I_{L6} \\ I_{L7} \\ I_{Ls} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \\ I_8 \end{bmatrix} \tag{1.3}$$

where

$$D_k = \frac{V_{k+1}}{(V_k + V_{k+1})} \tag{1.4}$$

$$D'_k = \frac{V_k}{(V_k + V_{k+1})} \tag{1.5}$$

and V_k are the steady state voltages of the dc domains. In continuous conduction mode (CCM), it can be directly claimed that the D_k's are the steady state duty ratios of the top switches of each DPP unit. No such claim can be made about the D_k's in discontinuous conduction mode (DCM, or any kind of light-load mode where both switches remain open during some periods). However, the relations in Equations (1.2) and (1.3) are still valid.

Considering a case where voltages are equalized, the relations between all inductor currents and the load currents at steady state can be written as

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ I_{L5} \\ I_{L6} \\ I_{L7} \\ I_{Ls} \end{bmatrix} = \begin{bmatrix} -1.75 & 0.25 & 0.25 & 0.25 & 0.25 & 0.25 & 0.25 & 0.25 \\ -1.5 & -1.5 & 0.5 & 0.5 & 0.5 & 0.5 & 0.5 & 0.5 \\ -1.25 & -1.25 & -1.25 & 0.75 & 0.75 & 0.75 & 0.75 & 0.75 \\ -1 & -1 & -1 & -1 & 1 & 1 & 1 & 1 \\ -0.75 & -0.75 & -0.75 & -0.75 & -0.75 & 1.25 & 1.25 & 1.25 \\ -0.5 & -0.5 & -0.5 & -0.5 & -0.5 & -0.5 & 1.5 & 1.5 \\ -0.25 & -0.25 & -0.25 & -0.25 & -0.25 & -0.25 & -0.25 & 1.75 \\ 0.125 & 0.125 & 0.125 & 0.125 & 0.125 & 0.125 & 0.125 & 0.125 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \\ I_8 \end{bmatrix} \tag{1.6}$$

For fast varying loads like processor cores, load balancing in software or by processor architecture itself can be on a millisecond time scale at best. But core loads can change much faster and load balancing cannot be ensured on the microsecond time scale (time scale at which voltage balancers/regulators are expected to respond). The balancing converters might need to operate such that they can process heavy mismatches for transient durations. Considering a uniform distribution of load currents, the distribution of inductor currents can be shown as in Fig 1.6.

The current and power processed by the DPPs are normalized to the maximum power of each load. It should be noted that the DPP converters in the middle of the stack process more power on an average than the converters at the beginning or the end of the stack. Also, the worst case current ratings of all the DPP converters exceed the peak mismatch current. DPP converters 1 and 7 need to be rated for 175% of the peak mismatch current. DPPs 2 and 6 need a 300% rating. DPPs 3 and 5 need a 375% rating while DPP 4 needs a 400% rating in order to maintain voltage regulation in worst case scenarios. These conditions might rarely occur, but the converters need to be rated to handle those conditions anyway. Under the

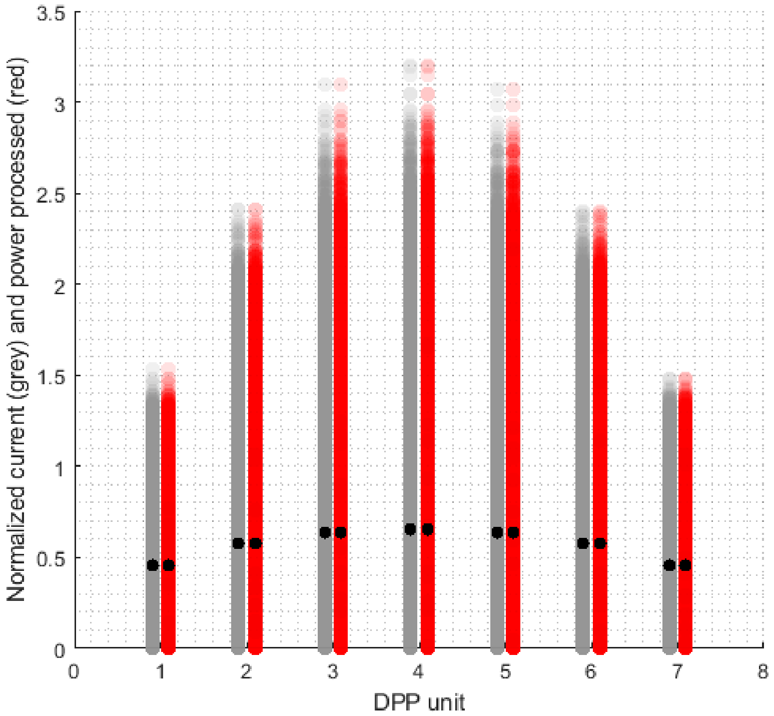


Figure 1.6: DPP inductor current distribution for the element-to-element topology under uniform distribution of load currents.

assumption that core currents are not going to be heavily mismatched for a majority of the time, the power processed by the balancing converters should still be lower in an average sense compared to the conventional parallel topology [23].

In the context of dynamics, it has been shown that distributed control of the DPP converters leads to unsatisfactory settling times as the stack size increases [37]. This is a direct consequence of the coupled nature of inductor currents. From the relationship between DPP currents and the load currents, it can be seen that in order to respond to any change in one particular load current, all DPP inductor currents need to be reconfigured. A MIMO feedforward controller has been suggested in [32] for improved control of the balancing and the stack converters together in a stack of four low voltage loads. However, for high numbers of loads in series, a nested/hierarchical architecture is expected to perform better dynamically than the ladder topology. For a stack of eight loads, a three level nested/hierarchical architecture is proposed in the next subsection.

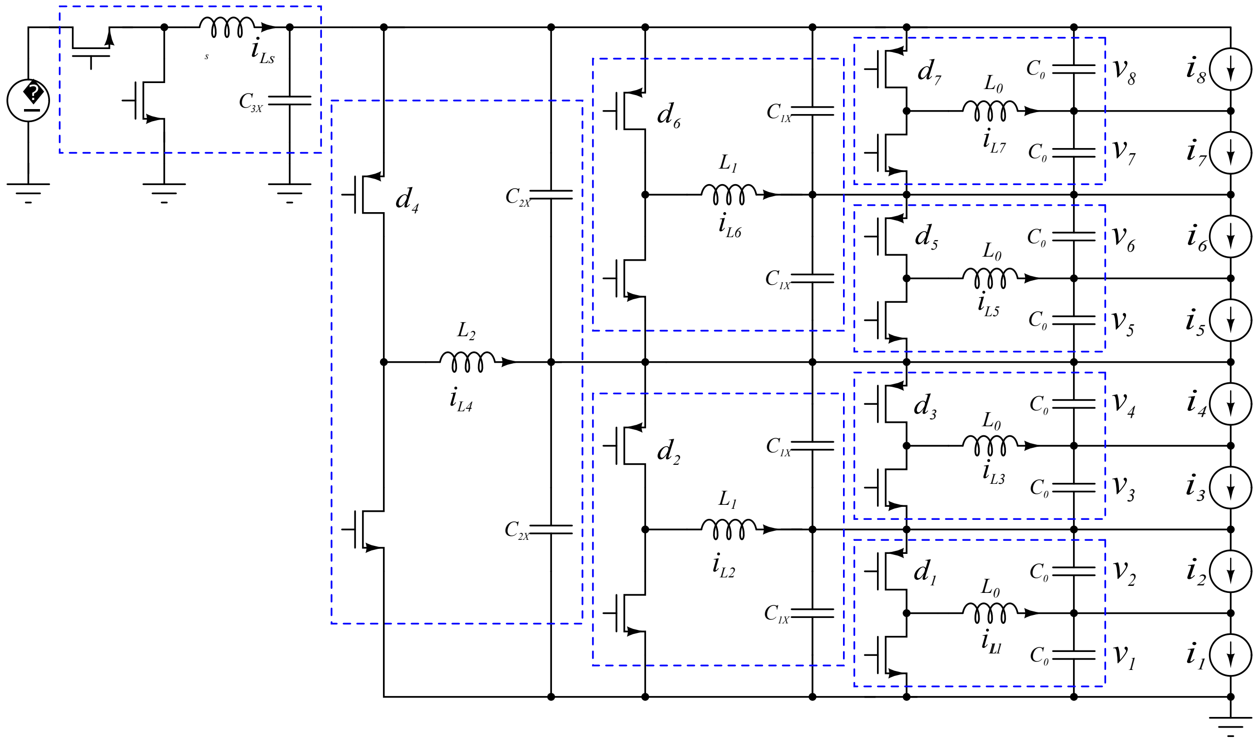


Figure 1.7: Hierarchical DPP topology for voltage regulation of a series stack.

1.3 Hierarchical topology

The hierarchical DPP topology in Fig 1.7 has several advantages compared to the switched inductor ladder topology. The inductor current dynamics are less coupled in nature than the element-to-element topology, allowing us to easily develop a distributed controller for fast voltage regulation of the loads [37]. Moreover, the current ratings for the DPPs are easy to determine in this case as they will never process more current than the maximum load current of each element. The steady state DPP inductor currents can be written as

$$\begin{bmatrix} D_1 & D_2 & 0 & D_4 & 0 & 0 & 0 & -1 \\ -D_1' & D_2 & 0 & D_4 & 0 & 0 & 0 & -1 \\ 0 & -D_2' & D_3 & D_4 & 0 & 0 & 0 & -1 \\ 0 & -D_2' & -D_3' & D_4 & 0 & 0 & 0 & -1 \\ 0 & 0 & 0 & -D_4' & D_5 & D_6 & 0 & -1 \\ 0 & 0 & 0 & -D_4' & -D_5' & D_6 & 0 & -1 \\ 0 & 0 & 0 & -D_4' & 0 & -D_6' & D_7 & -1 \\ 0 & 0 & 0 & -D_4' & 0 & -D_6' & -D_7' & -1 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ I_{L5} \\ I_{L6} \\ I_{L7} \\ I_{Ls} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \\ I_8 \end{bmatrix} \tag{1.7}$$

where

$$D_k = \begin{cases} \dfrac{V_k}{(V_k + V_{k+1})} & \text{for } k = 1, 3, 5 \text{ and } 7 \\ \dfrac{V_{k-1} + V_k}{(V_{k-1} + V_k + V_{k+1} + V_{k+2})} & \text{for } k = 2 \text{ and } 6 \\ \dfrac{V_1 + V_2 + V_3 + V_4}{V_1 + V_2 + V_3 + V_4 + V_5 + V_6 + V_7 + V_8} & \text{for } k = 4 \end{cases} \tag{1.8}$$

Considering a case where voltages are equalized, the relations between all inductor currents and the load currents can be written as

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ I_{L4} \\ I_{L5} \\ I_{L6} \\ I_{L7} \\ I_{Ls} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0.5 & 0.5 & -0.5 & -0.5 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0.25 & 0.25 & 0.25 & 0.25 & -0.25 & -0.25 & -0.25 & -0.25 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.5 & 0.5 & -0.5 & -0.5 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 \\ 0.125 & 0.125 & 0.125 & 0.125 & 0.125 & 0.125 & 0.125 & 0.125 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \\ I_8 \end{bmatrix} \tag{1.9}$$

and

$$D'_k = 1 - D_k \tag{1.10}$$

Considering the same uniform current distribution as in the case of the switched inductor ladder, the processed power and DPP converter current distribution are plotted in Fig 1.8. It can be seen that DPP_4 needs to be rated to process 4 times the power of each individual domain, and the converters DPP_2 and DPP_6 need to be rated for twice the power of each domain. However, all the DPP converters need to be rated to supply the same currents. The current rating does not exceed the maximum mismatch current or the rated current of each domain. Processing higher power at higher voltage and low current is an advantage for this application, where we are delivering power with low-voltage high-current loads and losses in power delivery are expected to be conduction loss dominant.

A second advantage of this topology is in the decoupled nature of the regulators. DPPs 1, 3, 5 and 7 are decoupled from each other (the dynamic equations of these DPP converters are independent as will be elaborated in a later chapter). Similarly DPPs 2 and 6 can be operated completely independent of each other. Consider, for example, a change in the load current i_3. To respond to this change, only DPPs 4, 2 and 3 need to reconfigure their inductor currents, unlike in the switched inductor ladder converter where all DPPs need to be reconfigured. This allows much easier distributed control to be designed for the balancing regulator stack.

With the hierarchical DPP architecture, fast voltage regulation of individual voltage domains can be achieved. The DPP converters in Fig 1.7 can be operated with carefully designed closed loop compensators with integral control to very accurately drive each domain voltage to a reference value. However, under the assumption that there is some software overhead that regulates load mismatches in an average sense, a simple droop based control can be sufficient. Our focus in this thesis is to build a series stacked system of eight 1.8 V (nominal) domains. Each domain is capable of sinking 10 A of current. These specifications are significantly higher than that demonstrated before, both in the number of series stacked domains and in terms of the power consumption of the loads. This is deemed as a necessary step towards emulating a real world processor if series stacking of cores were to be implemented.

The thesis is structured into three main sections which are briefly described in the following subsections.

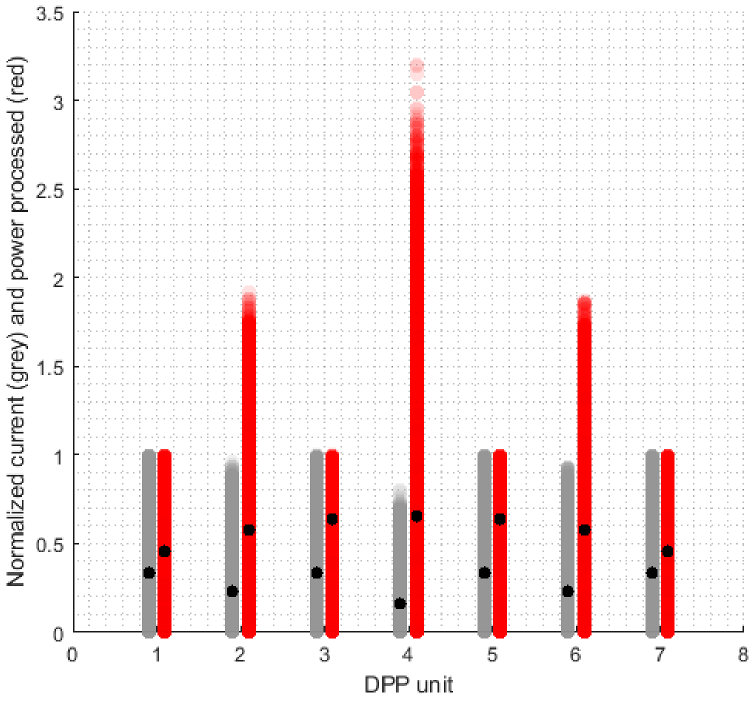


Figure 1.8: DPP inductor current distribution for the hierarchical topology under uniform distribution of load currents.

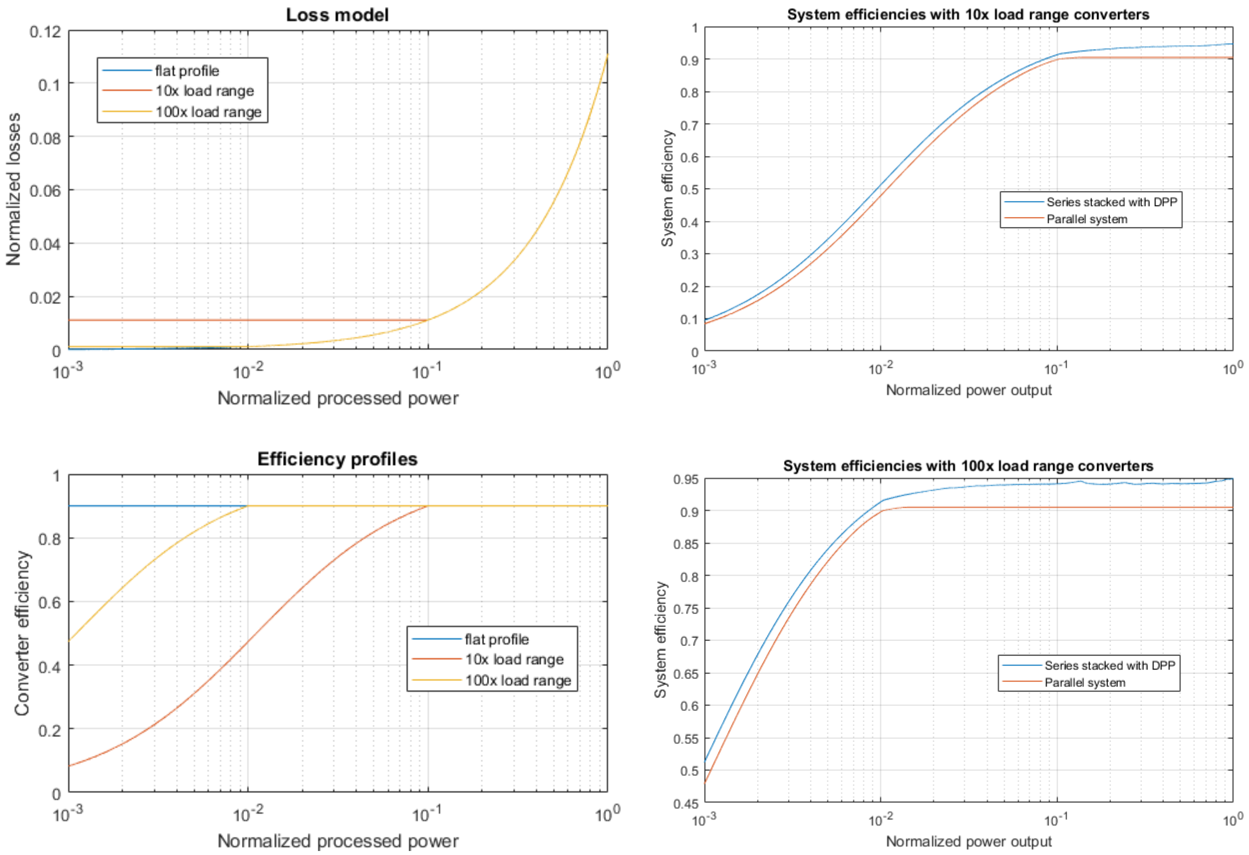
1.4 Light-load control

In Chapter 2 of this thesis we propose methods to improve light-load efficiency of DPP converters. To highlight the importance of light-load control in DPP converters, let us consider a simple but effective loss model. We assume a linear dependence between power loss P_{loss} and processed power P_{pr} by the DPPs. This would give us an efficiency curve which is flat over all processed power ranges. The DPP converters proposed in the hierarchical topology are synchronous buck/boost converters. Since they need to be bidirectional, we could simply operate the top and bottom switches in a complementary fashion. However, as the differential current approaches zero, the average inductor current also approaches zero. The losses remain more or less fixed, limited to the switching losses in the switches and gate drivers, and AC losses in the inductor. To make this loss model more realistic, we assume that the power losses are constant if the processed power is below a certain limit. A square law power loss formula would be more accurate to incorporate conduction losses at higher currents, but for generality (over different converter topologies and control techniques) a linear loss model is sufficient to show the importance of light-load efficiency in DPP systems. The model is

$$P_{loss} = \begin{cases} P_s & \text{for } |P_{pr}| \leq P_{ll} \\ k\,|P_{pr}| & \text{for } |P_{pr}| > P_{ll} \end{cases} \tag{1.11}$$

In one case we assume a flat converter efficiency (a linear power loss vs power output characteristic) over all values of processed power. We define light-load power P_{ll} as the value of processed power at which efficiency rolls off to 90% of its peak value. All power expressions are normalized to maximum panel power. We consider peak efficiency η_{pk} to be fixed for all simulations. Only variation is in P_{ll}. Given different values for P_{ll} the constants P_s and k in Equation 1.11 can be evaluated as $k = \frac{1}{\eta_{pk}} - 1$ and $P_s = \frac{P_{ll}}{9\eta_{pk}}$. The three cases are shown in Fig 1.9a. The stack converter is assumed to have a flat 95% efficiency. Considering uniformly distributed loads, the averaged system-level efficiency of the stacked system is plotted as in Fig 1.9b.

In one case the DPP converters are assumed to have a 10x load range (a slightly optimistic but an effective assumption for a converter operating in CCM at all loads). In the second case we assume that the DPP converters have a 100x load range (an achievable load range if a light-load power management technique is implemented). In a stack of 8 domains, when each of the loads draws near peak power, the system-level efficiencies approach the stack converter's efficiency for both cases. This high system-level efficiency was our initial



(a) Model efficiency profiles for converters with infinite, 100x and 10x load range.

(b) Averaged system-level efficiencies for the three cases.

Figure 1.9: System-level efficiencies for different load ranges of DPP converters.

motivation for series stacking processor loads. However, at light load, when each load only sinks about 1% of peak power, the system-level efficiency obtained with 10x DPP converters degrades to 50%, and no longer are we completely able to demonstrate the benefits of series stacking processor cores.

Operation in discontinuous conduction mode (or any other form of light-load power management) is usually a requirement for most modern power supplies to reduce power losses at light load to ensure good battery life (or just in general for lower energy consumption). Intel VRM specifications require on board voltage regulator modules to have a flat efficiency between at least 10% and full load. On board VRMs usually far exceed this load range requirement to ensure low battery drain during sleep modes and long periods of inactivity. Usually measures such as phase shedding in multiphase VRMs and pulse frequency modulation (PFM) operation at ultra-light loads ensure that a flat efficiency is maintained over a wide load range.

Light-load power management techniques for bidirectional DPP regulators are discussed in Chapter 2 of this thesis:

- A light-load power management technique that ensures variable frequency discontinuous conduction mode operation at light loads, for bidirectional DPP converters, is developed. A single phase converter operating in burst mode at light loads and CCM at heavy loads is demonstrated. Significant efficiency improvements at light loads is observed.

- In an effort to further improve load range of the DPP converters beyond what is achievable with PFM mode in a single phase converter, multiphasing is investigated. A logarithmic current sharing 4-phase converter (phases sized in 1:1:2:4 current sharing ratios) with phase shedding controls and PFM operation at light loads is then discussed and a wide load range is demonstrated experimentally.

- An asymmetric current sharing 2-phase DPP converter with arbitrary current sharing is developed (and proposed for use in the system). Different current sharing ratios are considered and the impact of sharing ratios on system level efficiency is discussed. Finally a 1:4 current sharing ratio is chosen. The 2-phase converter shows similar performance to the 4-phase design and better performance than the single phase converter design, and its implementation is discussed in Chapter 2.

1.5 Stack converter

The stack converter is the only converter in the system that is expected to process peak power for significant amounts of time. The increased output voltage (14.4 V nominal) and reduced load current requirements compared to the conventional VRM architectures make it easier to achieve higher efficiencies while processing moderate to peak power. A two phase synchronous buck converter is sufficient to meet our load current needs (10 A). However, it needs to be ensured that the load range of the stack converter is higher than or almost as high as that of the DPP converters regulating the domain voltages. Otherwise, a good system level efficiency over a wide load range cannot be achieved. The stack converter can be implemented as a unidirectional buck converter but synchronous rectification comes at a very low cost, and control techniques such as PFM or burst mode can be implemented improve light-load efficiency over a significant range.

In Chapter 3 of this thesis, we discuss a sensorless approach to current mode control to achieve regulation of the stack voltage. The proposed sensorless current mode control achieves satisfactory current sharing performance and closed loop performance comparable to peak current mode control. Small signal modeling of the sensorless current mode controller is discussed in detail and we further incorporate a light-load power management control into the sensorless current mode controller. The developed hardware setup for the stack converter demonstrates over 90% efficiency over a load range between 100 mA and 10 A (100x). This wide load range is extremely difficult to achieve for direct 48 V to 1 V conversion ratios either due to high core losses in bulky magnetics in transformer coupled topologies or due to the inability to shed phases with some switched capacitor hybrid topologies [18], further highlighting the importance of power delivery at higher voltage.

1.6 Load design and dynamics

Power dissipation in digital circuit loads such as microprocessors is usually modeled as $P_{diss} = \alpha f_{clk} C V_{dd}^2$, where α is the activity factor of the digital circuit and represents the fraction of CMOS elements that undergo switching while performing a particular operation, f_{clk} is the clock frequency, C is a measure of the capacitance at switching nodes and V_{dd} is the supply voltage. The power dissipation model behaves like a resistor, as we can conclude from the V_{dd}^2 term. However, if additional integrated voltage regulators are incorporated between the on-board voltage regulator and the actual digital core, a current source model (or constant power model depending on the type of regulator and the control of the integrated voltage regulator) might be deemed more appropriate for the digital loads. A constant current model is usually the most commonly used model for on-board voltage regulator designs, as shown in Fig 1.7. In an attempt to replicate the behavior of digital electronic circuit loads that can sink 10 A of current from 1.8 V domains, an array of switching loads based on charging and discharging capacitors is implemented. The currents drawn by the implemented load circuits are controllable by a square wave of variable frequency.

- Design of the frequency controlled loads and their implementation details are discussed in Chapter 4 of the thesis.

- Stability and dynamics of the hierarchical DPP topology are discussed in Chapter 4. It is shown that a droop based distributed control of the inductor currents of the DPPs is sufficient to maintain stability of the stack voltages.

- Finally, we demonstrate assembly and operation of the entire system of eight series stacked voltage domains (efficiency over a wide load range and transient performance) at the end of Chapter 4.

CHAPTER 2

LIGHT-LOAD POWER MANAGEMENT FOR DPP CONVERTERS

2.1 Light-load control scheme

Let us consider the basic buck-boost converter block in the element-to-element or hierarchical DPP topology shown in Fig 2.1. The DPP converter needs to be bidirectional, and the block inherently supports that if the switches are operated in a complementary manner. The converter operates in forced continuous conduction mode and inductor current can assume an average positive or negative value in this mode of operation. At light loads, this leads to inefficient operation. When no power is being processed the converter still has switching losses, inductor core losses, and conduction losses. Usually synchronous buck converters, widely used in low voltage power delivery, employ some sort of discontinuous conduction mode at light loads so that the lower switch does not let current flow in the reverse direction (diode emulation). Many different light-load power management techniques [38], [39], [40], [41] have been studied and applied, and they have been shown to be highly effective in improving light-load efficiencies in synchronous buck converters.

Our target is to implement a variable frequency discontinuous conduction mode (similar to PFM or burst mode or pulse skipping control in synchronous buck converters) for the bidirectional DPP converter block. With accurate sensing of the direction of the differential current i_o, the DPP block can be operated in variable frequency light-load mode, by operating the lower switch as a “lossless” diode when the differential current is positive (buck mode), and the top switch as a diode when the differential current is negative (boost mode). However, even if we carefully design a current measurement circuit that is fast and accurate to measure i_o's, offset errors will be a problem for arbitrarily low values. This will cause the controller to operate in variable frequency discontinuous mode either with positive average inductor current at some arbitrary low negative differential current or the opposite, and eventually cause voltage regulation to fail at arbitrarily light loads (here we assume that the load currents are independent of load voltage).

Our solution to this problem involves the use of current mode control. Fig 2.1 shows

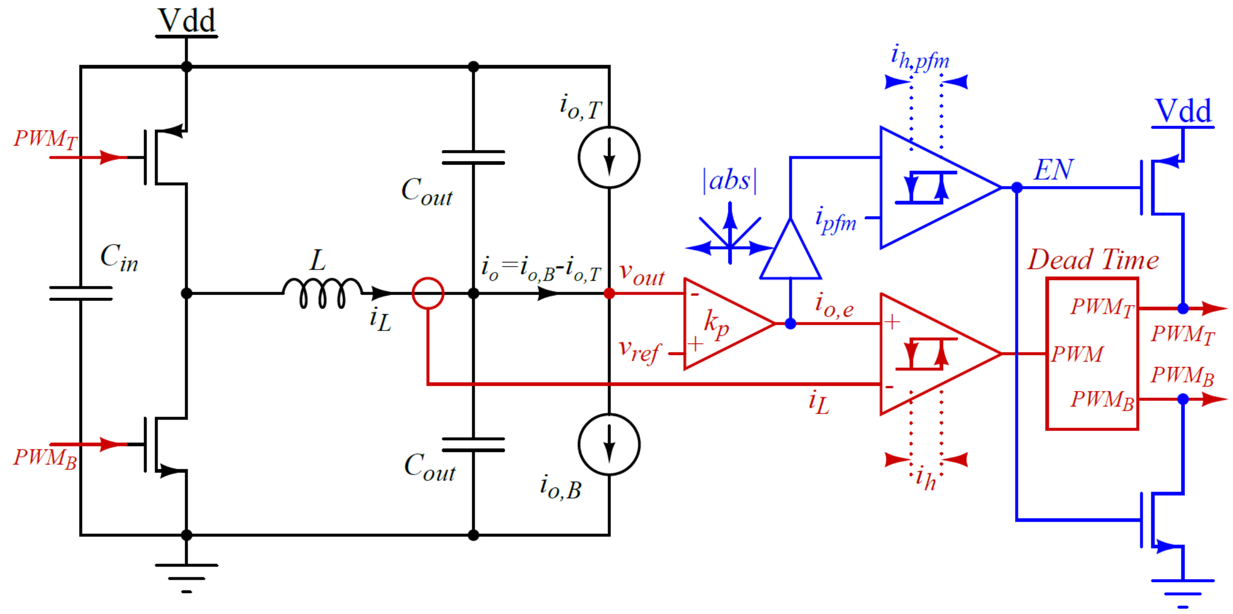


Figure 2.1: Light-load controller for a buck-boost DPP converter block.

a hysteretic current mode controller. The components in the control schematic shown in red form the basic hysteretic current mode control loop. The components shown in blue are additional components needed for light-load control. Instead of sensing the differential currents directly, current mode control uses an estimate, $i_{o,e}$, of the differential current generated from the output voltage error. In this case, the estimator takes the form of a simple proportional controller. The estimated differential current is then used to control the inductor current for voltage regulation. The switching signals are enabled only when the absolute value of estimated load current is above a certain limit, $i_{pfm,max} = i_{pfm} + {}^{i_{h,pfm}}\!/_{2}$, and disabled once the same is lower than $i_{pfm,min} = i_{pfm} - {}^{i_{h,pfm}}\!/_{2}$. So, under light-load operation, the inductor current is maintained at an average value of approximately ${}^{\left(i_{pfm,max}+i_{pfm,min}\right)}\!/_{2} = i_{pfm}$ whenever the converter is enabled and is zero when disabled. The frequency of the enable signals decrease with decreasing load, and variable frequency discontinuous conduction mode operation is achieved at light load.

Considering V_{dd} to be an ideal supply, the dynamic equation for v_{out} can be written as:

$$2C_{out}\frac{d}{dt}v_{out} = i_L - \left(i_{o,B} - i_{o,T}\right) \tag{2.1}$$

The inductor current dynamics can be represented as:

$$L\frac{d}{dt}i_L = u_1 V_{dd} - \left(u_1 + u_2\right) v_{out} \tag{2.2}$$

where u_1 and u_2 are the switching signals to the top and bottom switches respectively. The reference for the inductor current $i_{o,e}$ is generated as

$$i_{o,e} = k_p \left(v_{ref} - v_{out} \right) \tag{2.3}$$

During CCM operation the switches turn on and off in a complementary manner, leading to $u_1 + u_2 = 1$. The inductor dynamic equation can be reduced to

$$L \frac{d}{dt} i_L = u_1 V_{dd} - v_{out} \tag{2.4}$$

The dynamic equations of the converter represented by Equations (2.1) and (2.4) resemble exactly the dynamics of a buck converter which has $2C_{out}$ capacitance at its output. To determine the relationship between i_L and $i_{o,e}$ we should note that hysteretic current mode control offers control of both the valley and peak inductor currents, and in general tracks the reference current within two switching cycles. High frequency characteristics of the hysteretic current loop have been studied in the past and it has been established that the inner current loop is unconditionally stable and almost no tracking delay exists between average i_L and $i_{o,e}$ [42], [43], [44]. So in a small signal sense, it is safe to assume that the relation $\langle i_L \rangle = i_{o,e}$ is valid. Even in a large signal sense, the relation $\langle i_L \rangle = i_{o,e}$ can be considered to be valid to a certain extent due to the sliding mode nature of the inner current loop as shown in [45]. The limited slew rate of the inductor current is a nonlinear phenomenon and it has been modeled in the past as an additional pole in [46]. However, it has to be noted that the additional pole frequency is inversely proportional to the magnitude of a transient load (nonlinear phenomenon) and becomes relevant only when a large load transient is applied. So it is safe to conclude that in CCM operation,

$$2C_{out} \frac{d}{dt} v_{out} = \langle i_{o,e} \rangle - \left(i_{o,B} - i_{o,T} \right) \tag{2.5}$$

$$\langle i_{o,e} \rangle = k_p \left(v_{ref} - v_{out} \right) \tag{2.6}$$

adequately define the dynamics of the DPP converter.

In discontinuous conduction mode, the relation $\langle i_L \rangle = i_{o,e}$ no longer remains valid. Instead, to incorporate the effect of the enable action we can introduce a new variable e. When the converter is enabled, the inductor current tracks the reference current.

$$2C_{out}\frac{d}{dt}v_{out} = e\left\langle i_{o,e}\right\rangle - \left(i_{o,B} - i_{o,T}\right) \tag{2.7}$$

$$\left\langle i_{o,e}\right\rangle = k_p\left(v_{ref} - v_{out}\right) \tag{2.8}$$

The hysteretic enable and disable action during operation in light-load mode always maintains the value of $i_{o,e}$ within $[i_{pfm} - {}^{i_{h,pfm}}/_{2}, i_{pfm} + {}^{i_{h,pfm}}/_{2}]$ for positive differential currents and within $[-i_{pfm} - {}^{i_{h,pfm}}/_{2}, -i_{pfm} + {}^{i_{h,pfm}}/_{2}]$ for negative differential currents. There is no further scope for studying the dynamics of the converter in light-load mode. The output voltage consequently is maintained at an average value of $V_{ref} - {}^{i_{pfm}}/_{k_p}$ for light positive differential currents and at $V_{ref} + {}^{i_{pfm}}/_{k_p}$ for light negative differential currents. The light-load output voltage ripple can be evaluated as ${}^{i_{hpfm}}/_{k_p}$. An PLECS simulation is set up for a 7.2 V to 3.6 V DPP converter illustrating the light-load control of Fig 2.1. The simulation setup is shown in Fig 2.2. This simulated DPP converter is expected to fit a converter in the second level of our hierarchical stack. The simulation parameters are as follows: $V_{dc} = 7.2$ V, $V_{ref} = {}^{V_{dc}}/_{2}$, $L_1 = 1$ μH, $r_L = 10$ mΩ, $C_b = C_t = 100$ μF, $g_i = 100 = {}^{1}/_{r_L}$, $k_p = 100$, $R_sC_s = {}^{L}/_{r_L}$, hysteresis for the PWM relay $i_h = 1$ A, hysteresis for enable relay $i_{h,pfm} = 1$ A and $i_{pfm} = 1.5$ A. The simulation results are detailed in Figs 2.3 and 2.4.

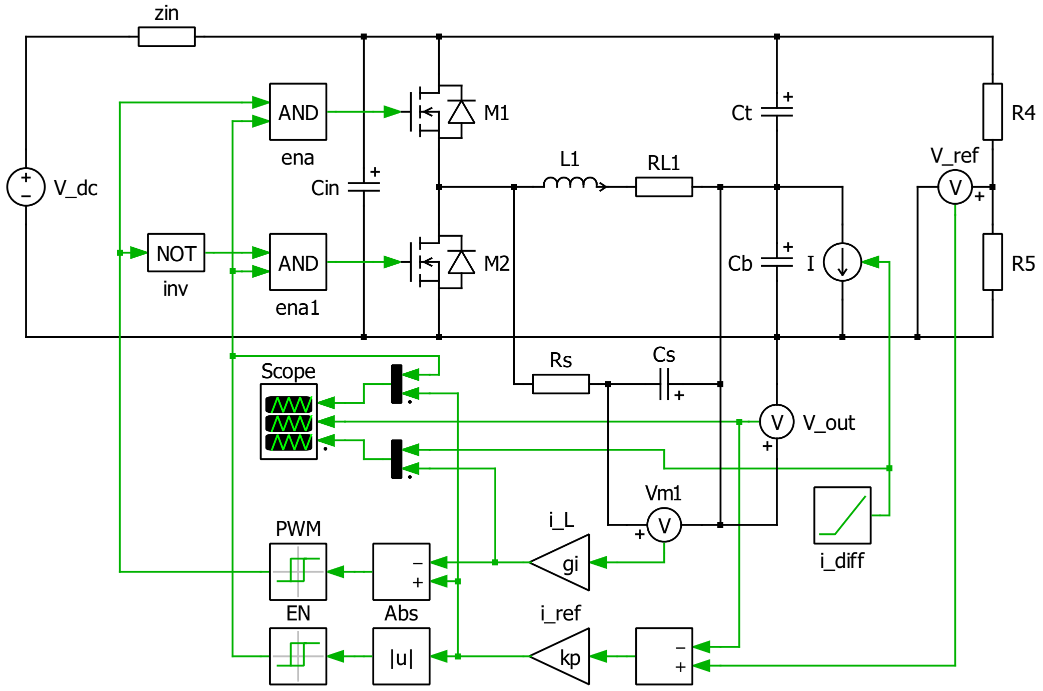


Figure 2.2: PLECS simulation circuit for single phase DPP unit.

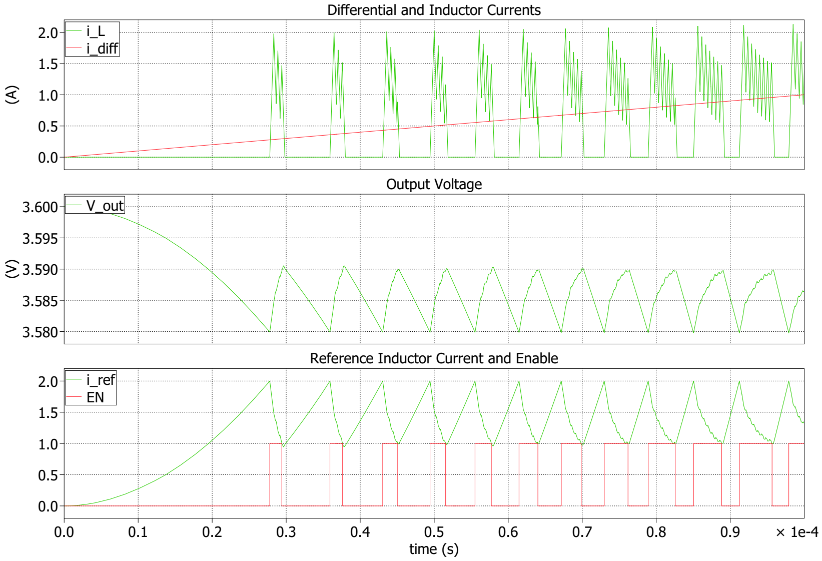


Figure 2.3: PLECS simulation showing bidirectional light-load operation with a slow ramp of differential current. The switching operations are enabled whenever the reference current reaches 2 A. This causes the output voltage error to reduce in magnitude, causing the reference current to decrease. The switching actions are disabled when the reference current is lower than 1 A.

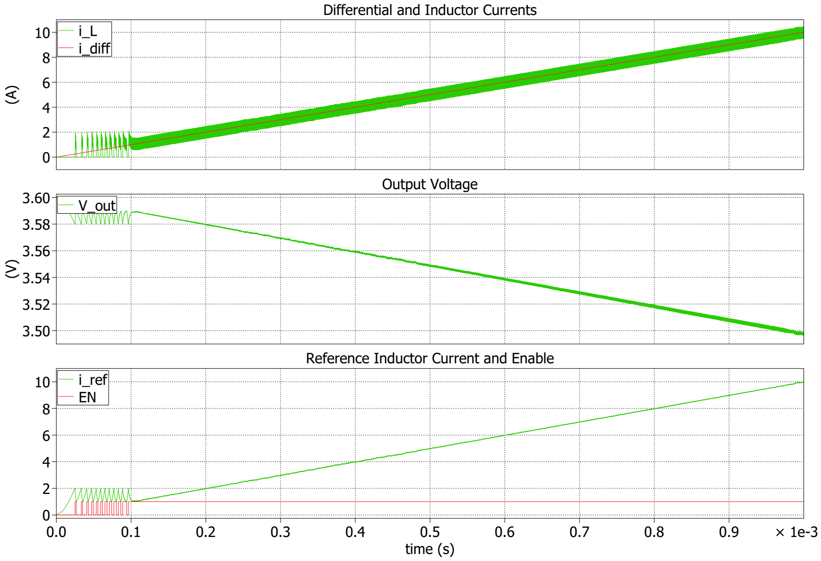


Figure 2.4: PLECS simulation showing the load line of the DPP converter with respect to differential current. Initially during light-load operation (up to 1.5 A of differential current), the average output voltage does not change with load. In CCM operation, a constant load line is maintained.

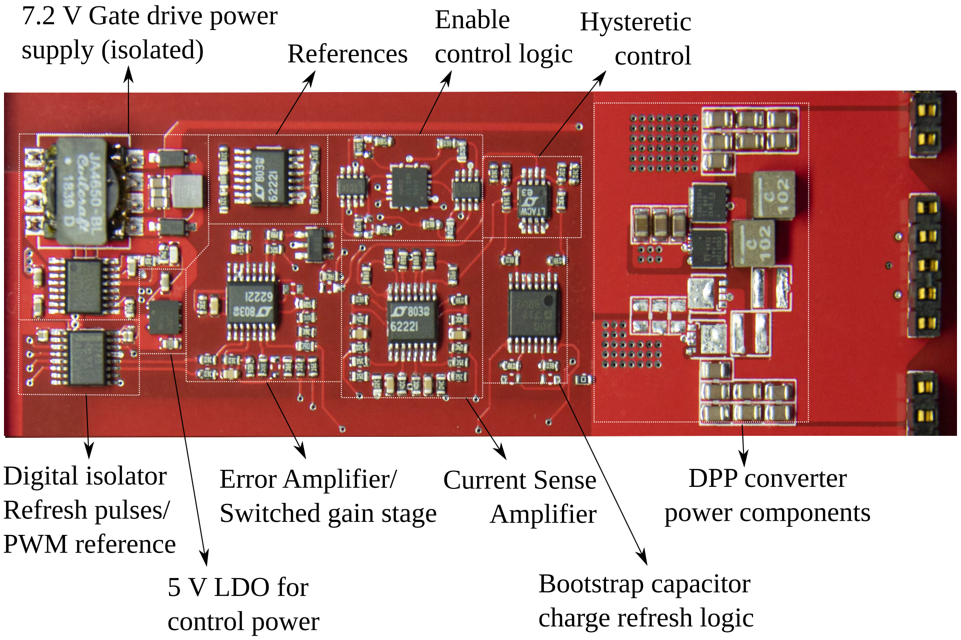

7.2 V Gate drive power supply (isolated)
References
Enable control logic
Hysteretic control
Digital isolator Refresh pulses/ PWM reference
5 V LDO for control power
Error Amplifier/ Switched gain stage
Current Sense Amplifier
Bootstrap capacitor charge refresh logic
DPP converter power components

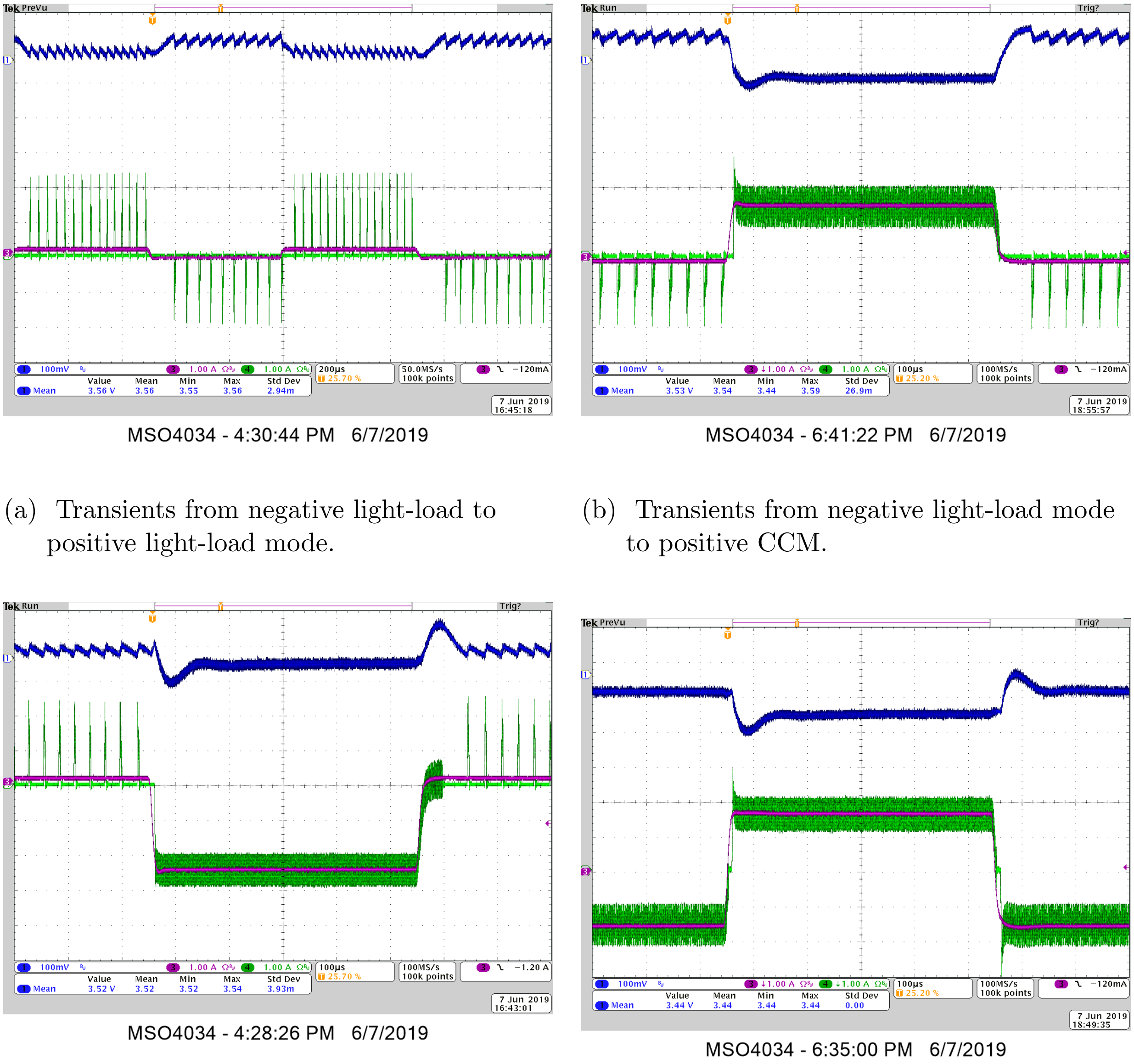
Figure 2.5: Annotated photograph of the single phase DPP hardware prototype.

Table 2.1: 1 Phase DPP Converter components

Component	Part Number	Specifications
Switch	CSD17304Q3D	30 V, $r_{DS,on} = 5$ mΩ, $Q_g = 5.1$ nC
Inductor	XEL4030	2×1.0 μH, $r_L = 9.89$ mΩ
C_{out}	GRM21BR61E226ME44K	7×22 μF, $R_{esr} = 3$ mΩ
C_{in}	GRM21BR61E226ME44K	3×22 μF, $R_{esr} = 3$ mΩ
Gate Driver	TPS28225	7.2 V, 2 A source, 4 A sink

To validate the light-load performance improvement obtained with the control scheme, a hardware prototype of DPP_2 was built with following specifications: $V_{in,nominal} = 7.2$ V, $V_{out,nominal} = 3.6$ V, $|I_{dpp,max}| = 10$ A. The chosen components for the converter are shown in Table 2.1. An annotated photograph of the hardware prototype is shown in Fig 2.5. The same hardware prototype is used for an improved two phase DPP converter discussed later in this chapter and details of the hardware implementation of the converter is discussed there. The transitions between different modes of operation for changing differential load currents can be seen in the oscilloscope captures shown in Fig 2.6.

If the ESR of the output capacitor is neglected, the light-load ripple value is determined by the value of k_p and $i_{h,pfm}$ and is not dependent on i_{pfm}. The parameter k_p is primarily determined from transient performance and target load line. If the highest value of k_p that ensures non-oscillatory behavior for the worst case load transient does not provide a



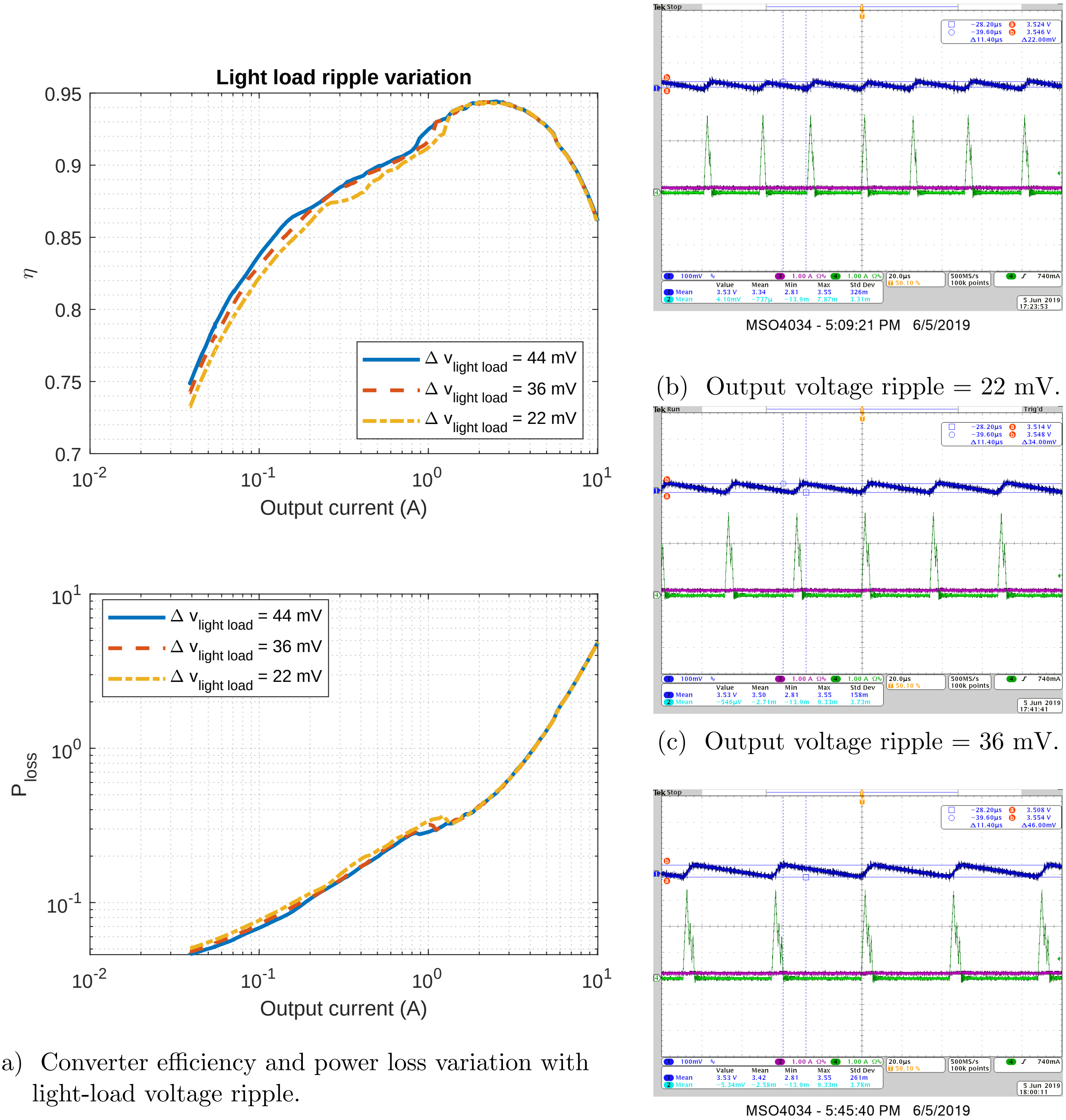
(a) Transients from negative light-load to positive light-load mode.

(b) Transients from negative light-load mode to positive CCM.

(c) Transients from positive light-load mode to negative CCM.

(d) Transients from negative to positive CCM.

Figure 2.6: Single phase DPP converter transient performance waveforms. It should be noted here that the inductor currents settle much faster than the output voltage. This is because the converter is configured to track half of the input voltage. The source voltage of the DPP unit is a slow-responding bench power supply which droops significantly whenever it is loaded. Horizontal time scale for (a) = 200 μs/div, for (b), (c) and (d) = 100 μs/div.



(a) Converter efficiency and power loss variation with light-load voltage ripple.

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(b) Output voltage ripple = 22 mV.

(c) Output voltage ripple = 36 mV.

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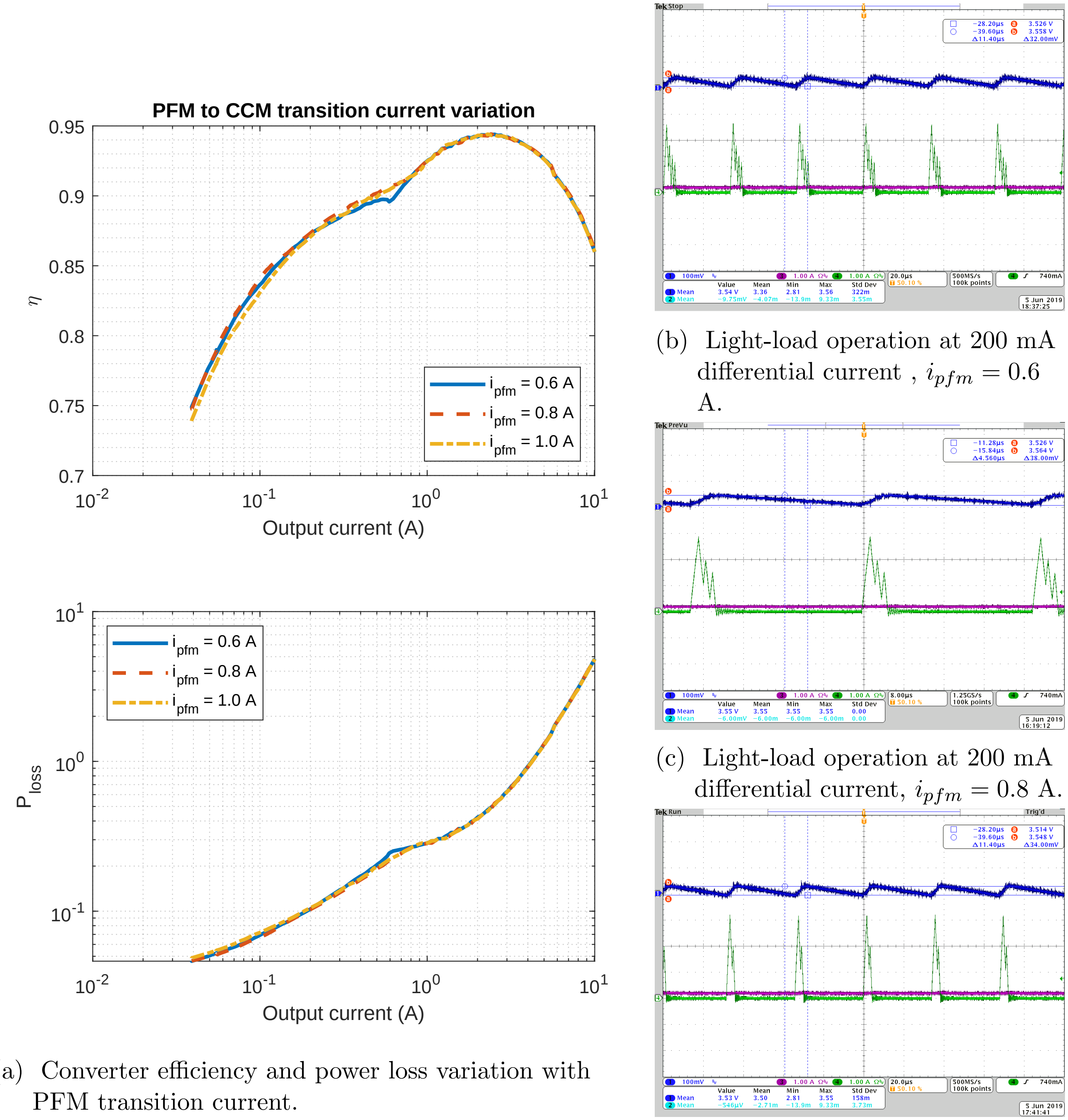
(d) Output voltage ripple = 44 mV.

Figure 2.7: Single phase DPP converter, light-load performance. Waveforms under different $i_{h,pfm}$ settings. Load current for the three waveforms = 200 mA. For oscilloscope captures: Channel 1 shows output voltage with a 3.6 V offset and 100 mV/div, Channel 3 shows differential current at 1 A/div and Channel 4 shows inductor current at 1 A/div. Horizontal time scale = 20 μs/div.

satisfactory load line, then both the output capacitance and k_p need to be increased until a satisfactory load line is achieved [46]. Hence the preferred way to vary the light-load ripple of the converter would be to vary the hysteretic limit $i_{h,pfm}$. Fig 2.7 shows efficiency plots for a few different values of light-load ripple. For these plots, the transition points from PFM mode to CCM mode were tuned to be approximately the same (around 1 A) and the hysteresis band $i_{h,pfm}$ was varied. It can be seen that approximately 2% efficiency is gained by doubling the light-load output voltage ripple from 22 mV to 44 mV. This might not be significant for our case where the converter efficiency around the 100 mA range is less than 85%, but it could be significant for more efficient setups.

The parameter i_{pfm} has a less significant impact on light-load ripple. It primarily controls the peak value of the inductor current at light load and the point at which PFM to CCM mode transition occurs. Choosing too low an i_{pfm} value may cause the inductor current to reverse direction for brief durations before the converter gets disabled and could cause slightly higher conduction losses. Choosing a value too high would cause large spikes in the inductor current at light load. These increase input filtering requirements and also induce more core losses in the inductor. Moreover, choosing a value too high for i_{pfm} would also cause an increase in the light-load ripple because of the effect of output capacitor ESR. Fig 2.8 shows efficiency plots and waveforms of the single phase converter under the same values of light-load ripple but with varying values of i_{pfm}. It can be seen that choosing a higher value of i_{pfm} can improve efficiency of the converter at intermediate loads (in the 1 A load region). At lighter loads, however, the losses are dominated by the static losses due to the control circuit and quiescent currents. Since we have not made any active effort to reduce those losses and used off-the-shelf ICs to implement controls in this research, those losses are higher than quiescent power losses of off-the-shelf DC-DC converter controllers [47].

To summarize, we observe that there is a tradeoff between light-load ripple and light-load efficiency. If we allow higher light-load ripple then it is possible to achieve slightly higher light-load efficiencies. Light-load ripple is a function of both $i_{h,pfm}$ and k_p and the preferred way to increase light-load ripple to achieve significant gain in light-load efficiency is to reduce k_p. However, with our low complexity control scheme, k_p and transient performance are coupled together. Increasing light-load ripple and efficiency is possible by decreasing the value of k_p which in turn slows down transient response of the and degrades the load line of the converter. A different method to further reduce light-load power losses is discussed in the next sections.



(a) Converter efficiency and power loss variation with PFM transition current.

	Value	Mean	Min	Max	Std Dev
1 Mean	3.54 V	3.36	2.81	3.56	322m
2 Mean	−9.75mV	−4.07m	−13.9m	9.33m	3.55m

(b) Light-load operation at 200 mA differential current , $i_{pfm} = 0.6$ A.

	Value	Mean	Min	Max	Std Dev
1 Mean	3.55 V	3.55	3.55	3.55	0.00
2 Mean	−6.00mV	−6.00m	−6.00m	−6.00m	0.00

(c) Light-load operation at 200 mA differential current, $i_{pfm} = 0.8$ A.

	Value	Mean	Min	Max	Std Dev
1 Mean	3.53 V	3.50	2.81	3.55	158m
2 Mean	−546µV	−2.71m	−13.9m	9.33m	3.73m

(d) Light-load operation at 200 mA differential current, $i_{pfm} = 1.0$ A.

Figure 2.8: Single phase DPP converter, light-load performance. Waveforms under different i_{pfm} settings. Output voltage ripple at light load kept constant at around 35 mV. Load current for the three waveforms = 200 mA. Horizontal time scale = 20 μs/div.

2.1.1 Light-load power loss model

A simple model for light-load power losses is proposed in this subsection. The losses considered in the efficiency data from the previous section can be broadly distributed into three groups: the gate driver power losses, power losses in the converter itself and the power losses in the control circuit. As such, for these experiments, minimizing control circuit power was not a target for our research (although reducing quiescent power is one of the most crucial aspects of light-load power management in power management IC designs). The control power losses included in measurements were only the direct losses from our power train, i.e. losses from the resistor dividers used for output voltage feedback and the losses from the switching node for dc resistive (DCR) current sensing. These losses were estimated from LTspice simulations to be around 40 mW. Efficiency plots for the converter after subtracting the resistor divider power losses are shown in Fig 2.9. It can be seen that without these fixed power losses, the light-load efficiency remains flat over a significant load range (seen more clearly in the power loss curve as power loss varies linearly with output current). Based on this, a simple power loss model for light-load operation can be formulated as

$$P_{loss} = P_{fixed} + P_{loss}\left(i_{pfm}\right)\frac{i_{load}}{i_{pfm}} \tag{2.9}$$

i.e. the power losses in the drive train scale down linearly from the value at the PFM to CCM transition current. This is not an accurate approximation since the pulse count at every enable action does not remain constant with load. At extremely light loads around the 30 mA mark, the enable signal remains on for only one switching action to take place, while around the current at which PFM to CCM transition takes place the enable signal remains on for several switching actions. The associated conduction and switching losses (in switches) can be modeled in detail, but the behavior of inductor core and AC losses with respect to pulse count are more difficult to model.

Light-load efficiency improvement by introducing variable frequency discontinuous conduction mode is demonstrated. Significant reduction in power losses at light load was observed. Further improvements can be achieved by optimizing the converter design itself. It is common knowledge that a higher inductance is preferable for improving converter efficiencies at light load (inductor core volume remaining constant, i.e. the lower and higher inductances in this argument are not expected to have the same current ratings). This is supported by converter loss modeling results shown in Fig 2.10. Various inductors from the XEL4030 series are paired with a small switch (CSD17484F4) and switching frequency was varied. Data for AC losses in the inductors were gathered from Coilcraft's online tools [48] and an accurate loss model for switching and conduction losses in switches was formulated. Efficiency at critical current can be assumed to be a qualitative estimate of efficiency at light load. The plots show that using a higher inductance can offer significant light-load efficiency improvements at critical current both on account of having to switch at a lower switching frequency and lower core losses of higher valued inductors.

However, using a higher inductance for the converter implies lowering the bandwidth and

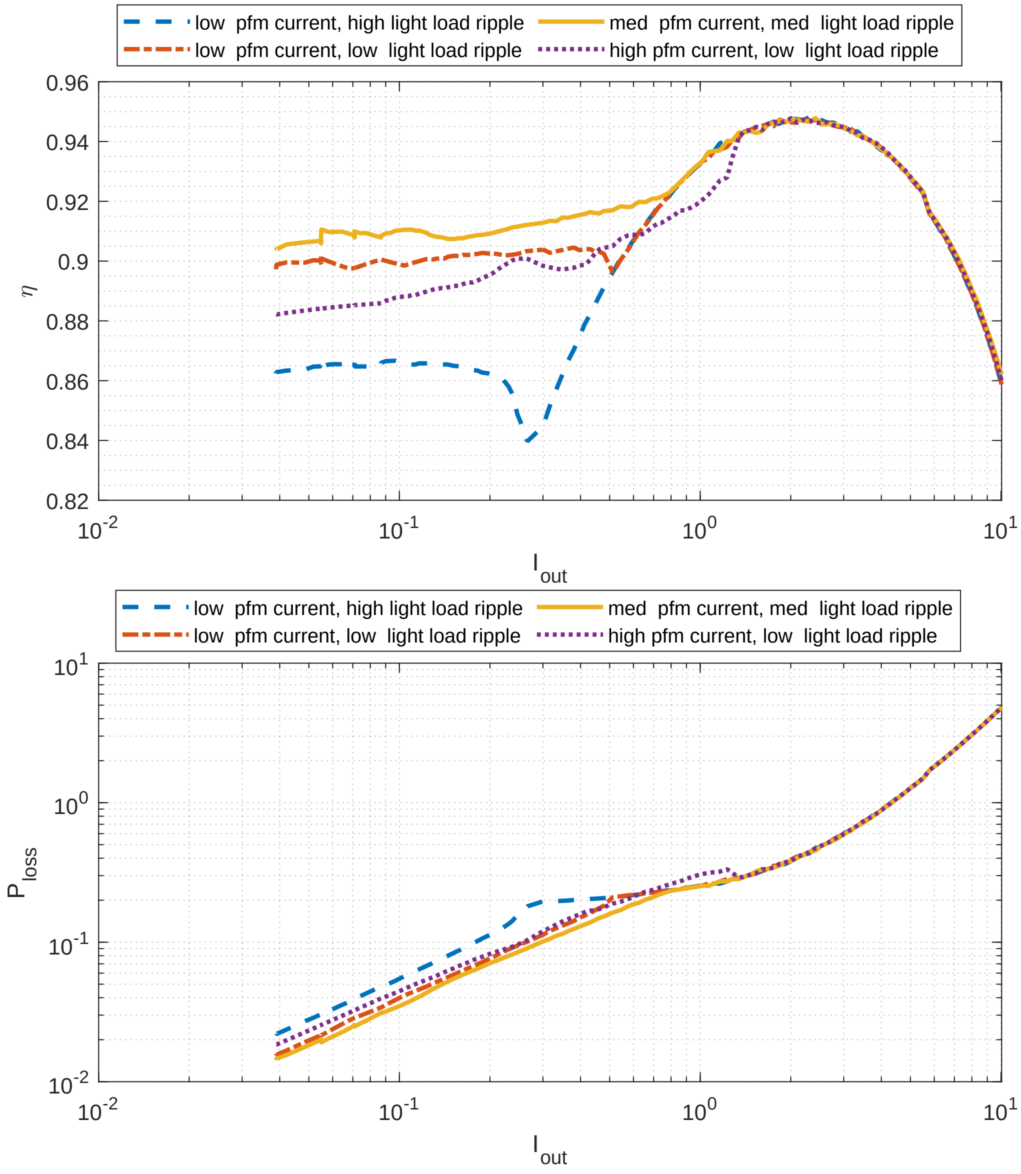


Figure 2.9: DPP converter efficiencies for different values of PFM current and light-load ripple after subtracting 40 mW of power losses in resistor divider for feedback and DCR current sensing.

slew rate of the converter. Also since the inductors are of the same sizes (from the same series), the saturation current ratings of higher inductances would be lower than design requirements. An approach to designing converters which counter these limitations is discussed in the next two sections.

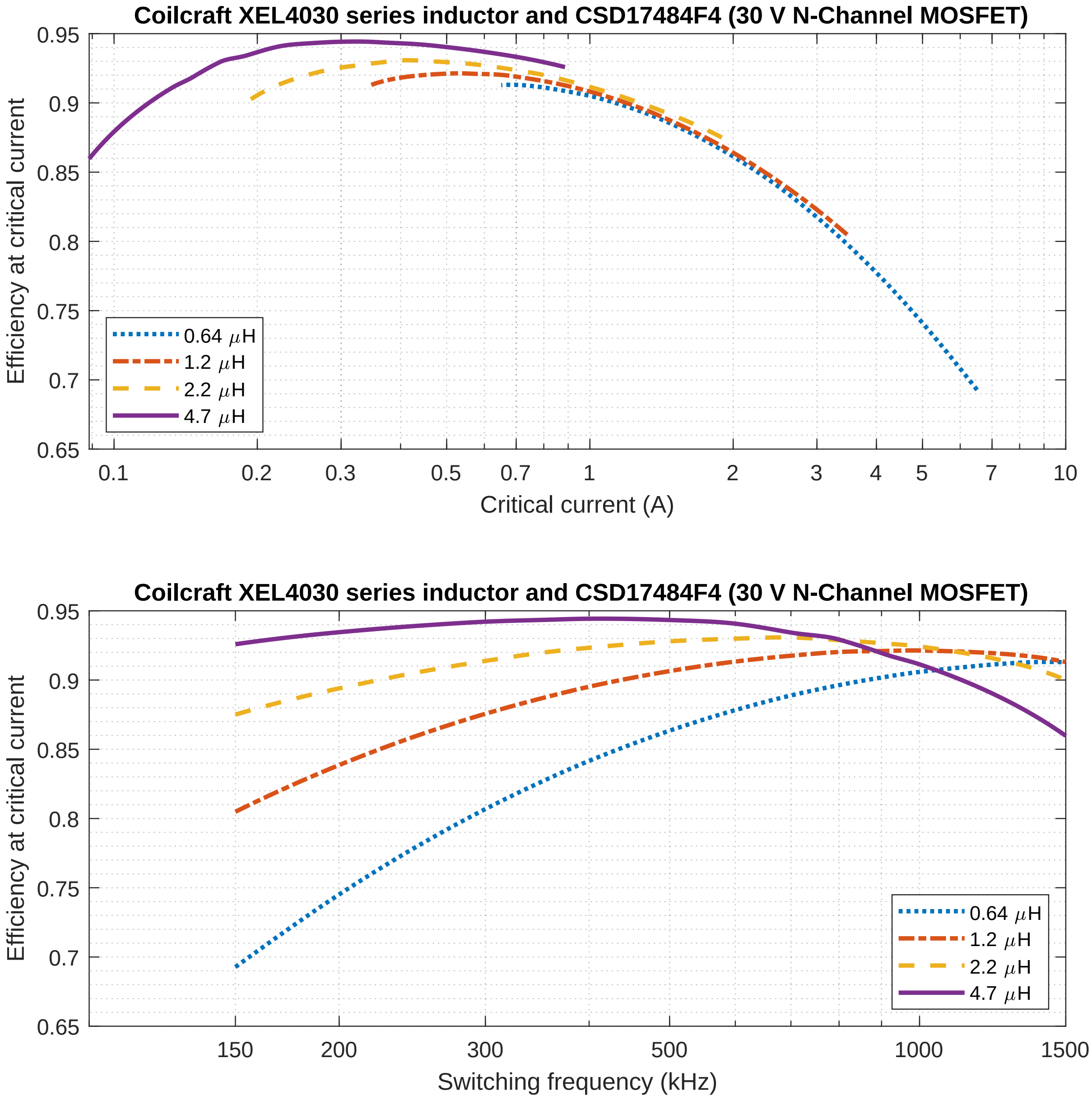


Figure 2.10: Converter efficiencies at critical current with different inductances from the XEL4030 series. The switch (CSD17484F4) sizes and inductor volumes are the same in all cases. The switching frequency was varied for these simulations to obtain efficiencies at different critical currents.

2.2 Four-phase DPP converter - logarithmic current sharing

At light loads, power losses are dominated by switching losses and core losses in the inductor. Reducing switching frequency serves to reduce both of these losses. However, reducing switching frequency also implies that a higher inductance value has to be used, and if we are using a single phase converter, a higher inductance value with the same current rating implies using a larger inductor in terms of volume (which counters the argument that reducing switching frequency will reduce core losses). Also, a higher inductance value will deteriorate dynamic performance of the DPP converter which could be critical to the system of series stacked processors we are considering. In order to ensure that we can switch at a lower frequency while operating at light load while still not having to compromise on dynamic performance and current rating, a multiphase converter is proposed in this subsection.

Multiphasing and shedding phases when not required, can lead to relatively flat power supply efficiency over a wide load range [49]. Previously multiphasing has been used to improve current output of converters when load current requirements are too high for a single converter to handle. Interleaving the switching actions of different phases leads to reduction in overall ripple current and output voltage ripple. However, even for relatively low current applications, splitting a supply into multiple lower current phases can be beneficial for light-load efficiency.

Many modern applications of multiphase buck converters (specially power delivery to laptop processors and mobile system on chips) have low peak load duty cycles, i.e. the maximum current capacity of the converters is utilized only for short intervals. In our application, where we expect the DPPs to process low mismatch currents most of the time, it would be inefficient to devote extensive board area to a high phase count multiphase buck converter just to improve light-load performance. For this reason, we discuss a multiphase design with asymmetric current sharing. Asymmetric multiphase converters retain good efficiency over a wide load range by using phases optimized for different current ranges [50] or with general approaches such as logarithmic scaling [51].

Our design approach for an asymmetric multiphase converter is to condense phases. Let us start from a 8-phase symmetric converter with each phase having an inductance L. The maximum load current is 10 A, and the 8-phase design was made solely for the purpose of obtaining a flat efficiency profile over a wide load range by phase shedding. Since our current requirement is not very high for on board designs and we can expect that the high phase count will only be required for short durations, we can combine 4 phases of the converter into one phase with inductance $^{L}/_{4}$. We can combine another two phases into one phase with inductance $^{L}/_{2}$. This reduces the 8-phase symmetric converter to the 4-phase

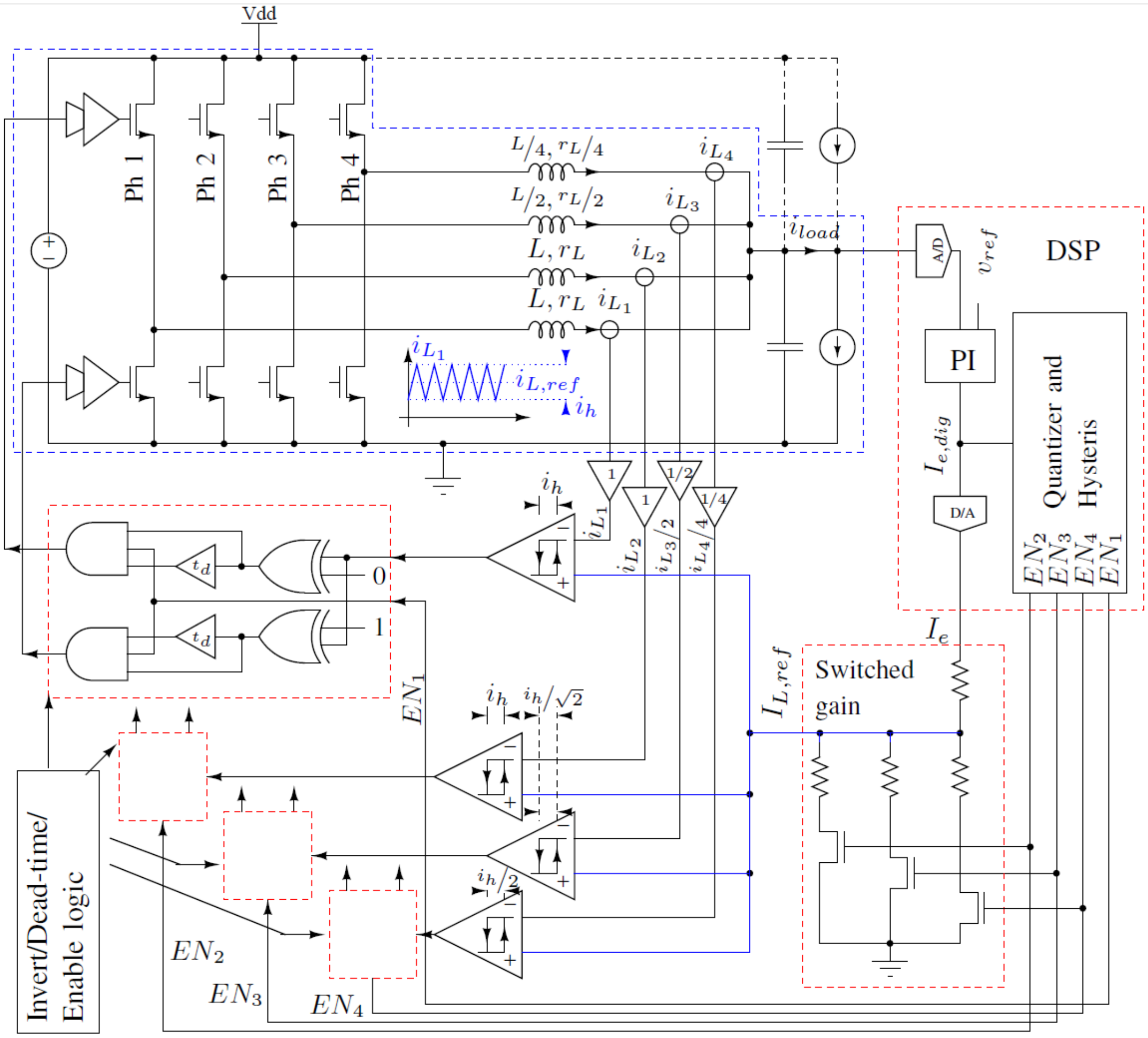


Figure 2.11: 4-phase DPP converter with logarithmic current sharing.

equivalent asymmetric converter shown in Fig 2.11, while retaining the same maximum slew rate possible for the combined inductor currents (so that dynamic performance is not compromised). However, it does not retain the ripple cancellation benefits of the original symmetric design.

Appropriate switching frequencies for the various phases are chosen such that the output voltage ripple contributions of the individual phases are the same. This implies that higher current phases should use a higher switching frequency, which may seem counterintuitive for efficiency improvement. However, the higher current phases are only active at higher load currents, where conduction losses dominate over switching losses. Since the inductances of the higher current phases are progressively lower, their series resistances are also progressively

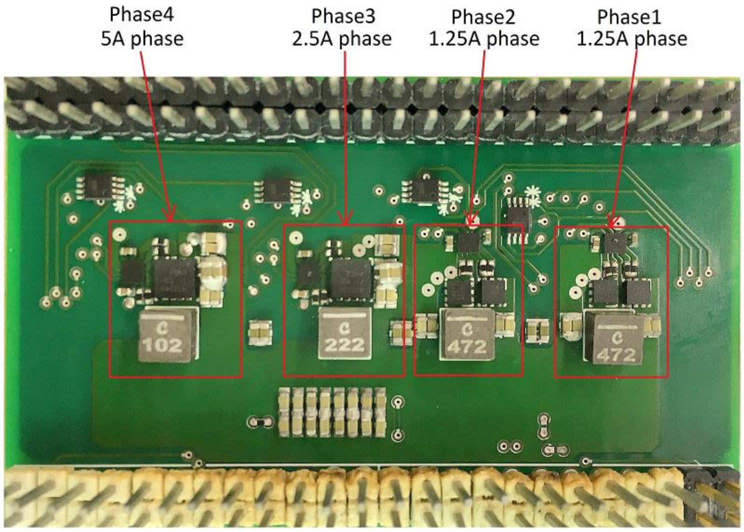


Figure 2.12: Hardware prototype of the proposed multiphase converter with asymmetric phases. Note that the relative sizes of the phases with different rated currents are nearly the same.

lower. Although the efficiency of the new composite phase will be slightly lower than that of the 4-phase equivalent, the board area benefit is much larger (Fig 2.12).

2.2.1 Phase shedding and adding control

Our phase shedding and adding strategy is to emulate the behavior of the baseline 8-phase converter as closely as possible with a 4-phase equivalent asymmetric converter. To accomplish this, we develop a similar 8-step phase shedding and adding controller. The entire controller schematic is shown in Fig 2.11.

A PI controller generates the reference current (I_e) from the output voltage error. A 4-bit quantizer similar to the one described in [51] is then used to generate phase enable signals (EN_2, EN_3, EN_4) from the reference current. The quantizer has hysteretic limits for each phase-shedding or adding operation, which helps avoid unstable behavior during phase shedding or adding. A switched gain stage then generates the current reference for the phases, $I_{L,ref}$ (according to Table 2.2). The current sensing gains of the third and fourth phases are respectively $1/2$ and $1/4$ of that of the first two phases. Accordingly, under current hysteretic control the third and fourth phases will track $2I_{L,ref}$ and $4I_{L,ref}$, respectively, when enabled.

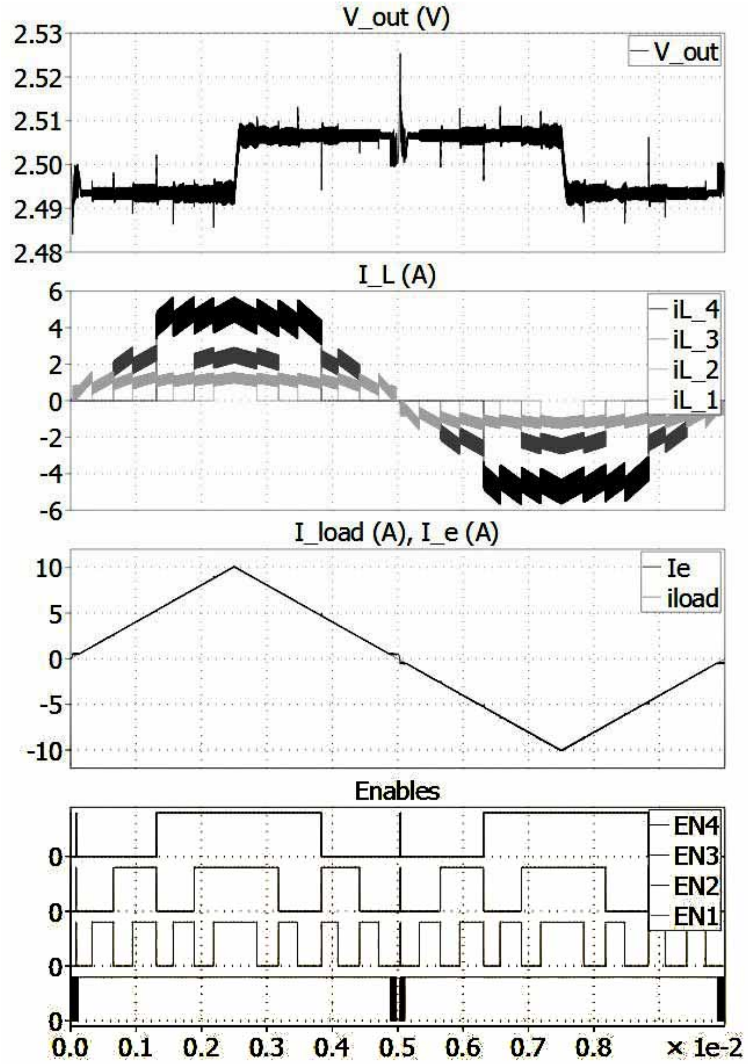
The light-load controller discussed before is implemented on one of the two low current phases of the multiphase converter. In light-load operation the controller switches between

Table 2.2: Phase shedding scheme

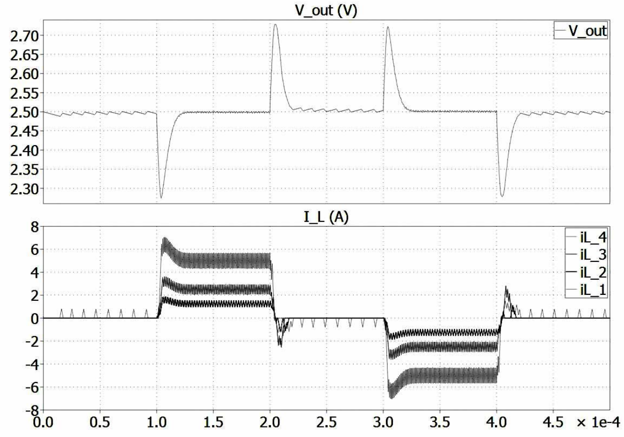
Mode	$abs(I_e)$	EN_1	EN_2	EN_3	EN_4	$I_{L,ref}$
0	$(0, I_{PFM,lim})$	0	0	0	0	I_e
1	$(I_{PFM,lim}, {}^{I_{max}}/_{8})$	1	0	0	0	I_e
2	$({}^{I_{max}}/_{8}, {}^{I_{max}}/_{4})$	1	1	0	0	${}^{I_e}/_{2}$
3	$({}^{I_{max}}/_{4}, {}^{3I_{max}}/_{8})$	1	0	1	0	${}^{I_e}/_{3}$
4	$({}^{3I_{max}}/_{8}, {}^{I_{max}}/_{2})$	1	1	1	0	${}^{I_e}/_{4}$
5	$({}^{I_{max}}/_{2}, {}^{5I_{max}}/_{8})$	1	0	0	1	${}^{I_e}/_{5}$
6	$({}^{5I_{max}}/_{8}, {}^{3I_{max}}/_{4})$	1	1	0	1	${}^{I_e}/_{6}$
7	$({}^{3I_{max}}/_{4}, {}^{7I_{max}}/_{8})$	1	0	1	1	${}^{I_e}/_{7}$
8	$({}^{7I_{max}}/_{8}, I_{max})$	1	1	1	1	${}^{I_e}/_{8}$

mode 0 and mode 1 to ensure that the output voltage (error) is within hysteretic limits. But at any point other than light-load operation, the switched gain stage in the controller enables us to keep track of the actual load current irrespective of how many phases are on at a certain time (the controller maintains a constant load line). This is helpful in reducing spurious phase shedding and adding behavior common in hysteretic phase shedding and adding controllers. The switched gain stage also ensures that a constant load line is maintained (constant dc load line if a simple proportional controller is used for generating I_e), which could be desirable.

The control is similar to the one described in [51]. The idea in [51] was to develop logarithmically sized phases which are optimized for operation at one particular value of load current. When those phases are enabled, they provide a portion of the load current in the most efficient way possible from the setup. The lowest current phase was supposed to balance the difference between load current and the sum of currents provided by the highly optimized phases. Our implementation is slightly different: the average currents in phases 3 and 4 are always 2 and 4 times that of the first two phases whenever they are enabled. This allows the currents in phases 2, 3 and 4 to vary slightly around the point of operation they are optimized for. This adds more complexity to the controller but allows us to share transient currents logarithmically among the phases (Fig 2.13b). Also, scaling the phases in this manner allows the high current phases to respond to transients faster than the low current phases (due to slew rate of the inductor currents). Simulations performed in MATLAB/Simulink using the PLECS blockset to demonstrate light-load and phase shedding and adding behavior are shown in Fig 2.13a. Note the narrow range of the inductor currents when each of the phases are enabled. The inductances in the various phases are 4.7 μH, 2.2 μH and 1 μH, sufficiently close enough to the 4:2:1 ratio that is ideal. The hysteretic current boundaries for switching operations were set such that at no load the phases operate at 500 kHz, 750 kHz and 1 MHz, respectively.



(a) Phase shedding and adding behavior.



(b) Load transient response.

Figure 2.13: Transient simulations of proposed 4-phase converter.

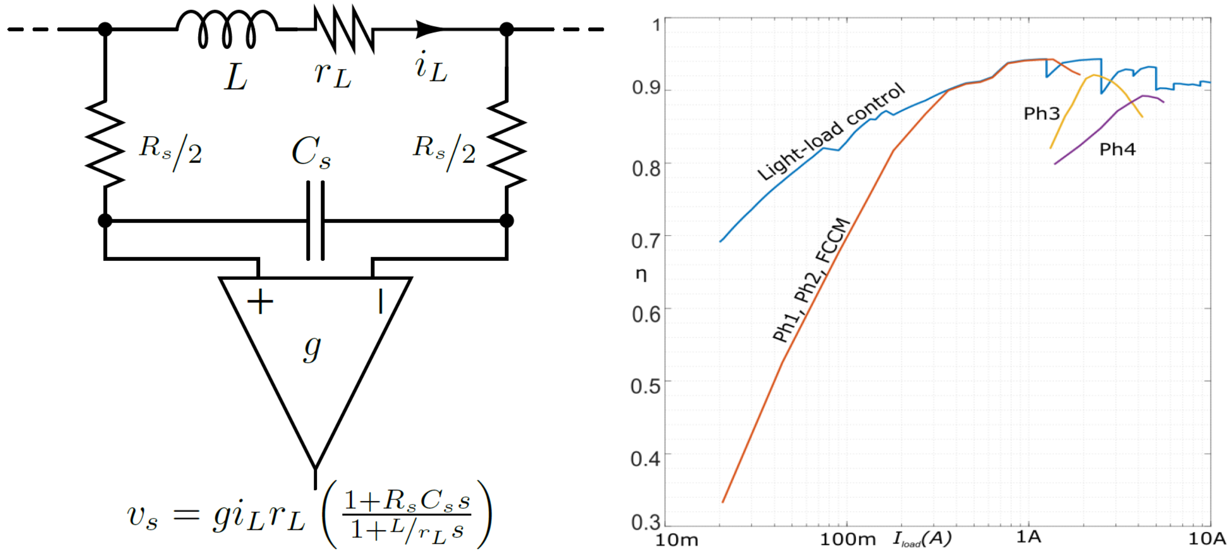
Table 2.3: 4-phase converter components

Component	Part Number	Specifications
Phase 1/2 Switch	CSD16301Q2	30 V, $r_{DS,on} = 5$ mΩ, $Q_g = 5.1$ nC
Phase 1/2 Inductor	XEL4030	4.7 μH, $r_L = 40$ mΩ
Phase 1/2 Gate Driver	LM5113	1 A source/5 A sink, 5 V supply
Phase 3 switch	CSD87333Q3D (DrMOS)	$r_{DS,on} = 5$ mΩ, $Q_g = 5.1$ nC
Phase 3 Inductor	XEL4030	2.2 μH, $r_L = 19$ mΩ
Phase 4 switch	CSD87334Q3D (DrMOS)	$r_{DS,on} = 5$ mΩ, $Q_g = 5.1$ nC
Phase 4 Inductor	XEL4030	1.0 μH, $r_L = 9.89$ mΩ
C_{out}	GRM21BR61E226ME44K	7 × 22 μF, $R_{esr} = 3\ m\Omega$
C_{in}	GRM21BR61E226ME44K	3 × 22 μF, $R_{esr} = 3\ m\Omega$

A hardware setup to validate the operation of the proposed controller was prepared with the components shown in Table 2.3. The goal was to create a converter with as wide load range as possible operating from a 5 V input and regulating a 2.5 V output. The maximum load current to be encountered was 10 A. The PI controller was implemented with an analog opamp circuit; the phase shedding and adding control and hysteretic PWM generation were performed using a C2000 digital signal processor (DSP). Current sensing was done using the DCR sensing method shown in Fig 2.14a. Accurate pole-zero cancellation of the inductor parameters and the sensing parameters will give an exact current waveform; however, this is not possible due to parameter variations. Both inductance and dc resistance change with current and temperature. It is therefore useful to ensure that leading or lagging behavior of the sensed inductor current with respect to the actual inductor current is preserved over all inductor current and temperature ranges. In this design $R_sC_s \approx {}^{L}/{}_{2r_L}$ was chosen. This gives twice the ripple/average current ratio that would appear with resistive current sensing. The dc value of the sensed inductor current is a fixed multiple of the drop across the inductor and remains preserved as long as there is limited (or known) DCR variation with current and temperature.

Although in principle there should be no switching action when the converter is not loaded, activation of the low-side switch is necessary to maintain charge in the bootstrap capacitor. If charge is not maintained, the converter fails to turn on when the load current takes a positive value after a long interval of operating at no load. To solve this problem, a timer was used to generate short enable pulses at 500 Hz. These low-frequency pulses have negligible effect on light load efficiency. Light-load waveforms at various positive and negative loads are shown in Figs 2.15a, 2.15b, 2.15c and 2.15d. Efficiency measurements were performed and are shown in Fig. 2.14b.

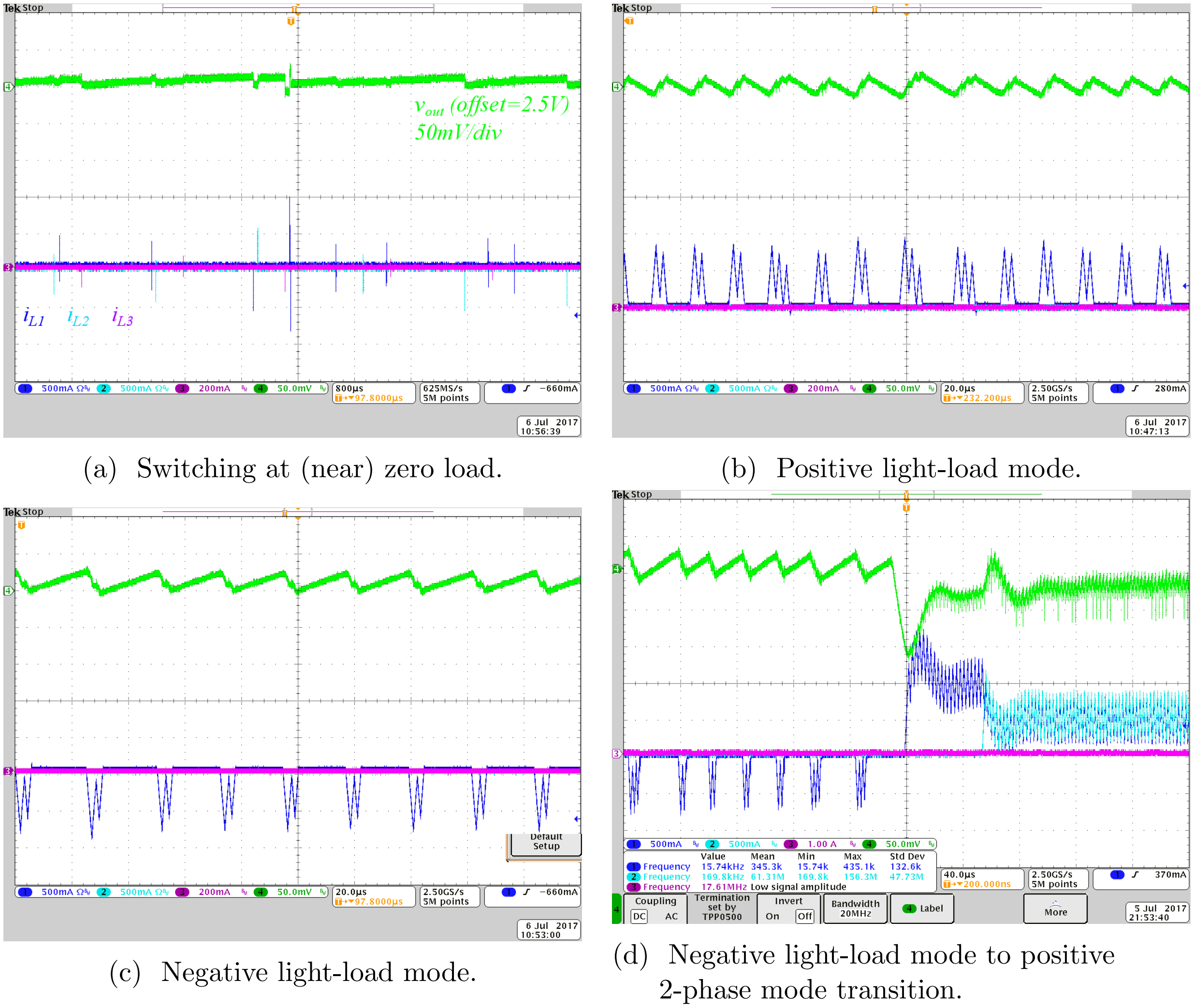
The bootstrap capacitor charging issue is also encountered during phase-shedding or adding control operations. Although short enable pulses to the different inactive phases at 500 Hz can solve this problem, care must be taken so that transients due to the 500 Hz pulses are well damped by the control loop. The analog PI controller output was sampled at 1 MHz (with 12 bit resolution) and a first order low pass IIR filter was used to obtain a clean estimated current value. The four most significant bits could directly be used to control the phase enable signals but some hysteresis is required for each phase transition to ensure jitter-free operation at currents near the phase transitioning currents. One possible solution is to incorporate the hysteresis directly into the comparators of the quantizer. Another solution is to use a state-machine controller. A state machine which sequences through all the phases between the initial phase and the final phase (in the event of a transient) was implemented on the C2000 controller. Phase transitions with low jitter were obtained by tuning the hysteretic limits. The low pass IIR filter also helps reduce spurious phase transitions, although it also adds a significant delay between a load transient and a corresponding phase transition. Some critical phase transitions are shown in Figs 2.15d 2.16a and 2.16b. Fig 2.16c shows the controller's response to an 8 A load transient. The sequential transition between phases can clearly be seen. The delays in the initial phase transitions were significant enough to cause a 0.7 V drop in the output voltage (for reference Fig. 2.16d shows an 8 A transient response when no phase transitioning is involved). To obtain faster phase transitions when there are multiple phases between the initial and final phase counts, a state machine which skips between modes can be built. However, the complexity of the



(a) DCR current sensing.

(b) Efficiency of hardware prototype.

Figure 2.14: Hardware results.



(a) Switching at (near) zero load.

(b) Positive light-load mode.

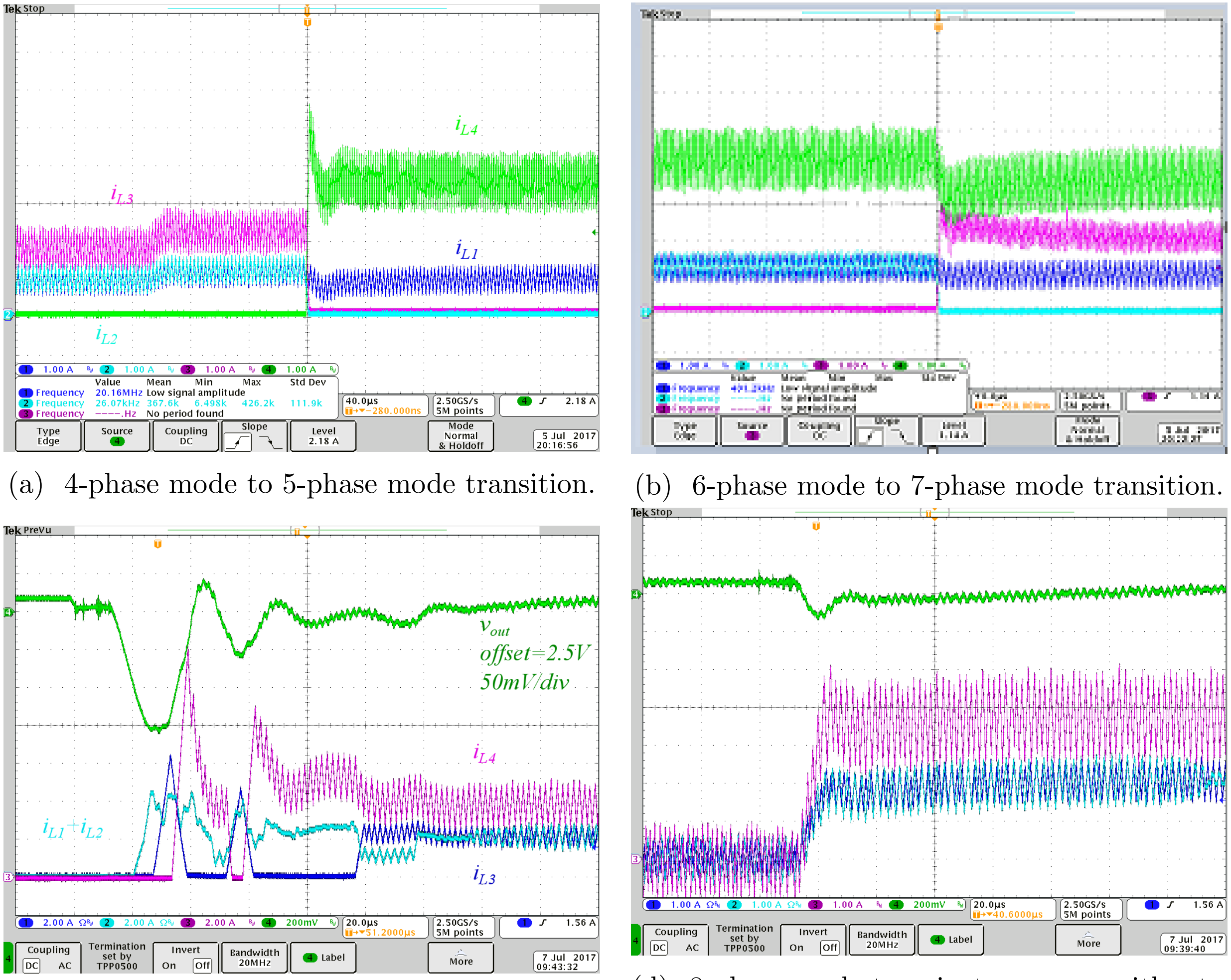
(c) Negative light-load mode.

(d) Negative light-load mode to positive 2-phase mode transition.

Figure 2.15: Light-load operation in 4-phase DPP converter.

state machine increases substantially if skipping phases is incorporated, and as such was unsuitable for implementation on a C2000 microcontroller.

Without considering controller power dissipation, it can be seen that the converter maintains a fairly flat efficiency between 100 mA and 10 A (which is a 100x load range). However, the efficiency curves obtained show that the phases themselves were not entirely optimized for the current ranges in which they are operational. Smaller inductors and switches were required for optimized efficiencies in the system where peak I_{out} is only 10 A. The Dr-MOS switches used for higher current phases were too big for efficient operation at the high switching frequencies attempted. To improve performance (by optimizing component sizes in a more streamlined manner suitable for on board converters) and to reduce the complexity of a single DPP converter a two phase asymmetric design is proposed in the next



(a) 4-phase mode to 5-phase mode transition.

(b) 6-phase mode to 7-phase mode transition.

(c) light-load to 8-phase mode transition (8A).

(d) 8-phase mode transient response without phase-enabling (8A).

Figure 2.16: Phase shedding/adding operations in 4-phase DPP converter.

subsection. The two phase converter allows operation of the phases over a wider range of load currents more suitable for on board converter designs. It also allows us to investigate arbitrary current sharing ratios and their impact on overall system efficiency.

2.3 Two-phase DPP converter - asymmetric current sharing

An asymmetric current sharing two-phase DPP converter is proposed in this subsection. Instead of following a logarithmic current sharing approach as in the previous subsection, we start with the assumption that the current sharing ratio between the two phases can be arbitrary and is a subject for optimization. The general converter structure and control is described in Fig 2.17. We maintain the same design specifications as for the single phase converter discussed in a previous section. To choose a particular current sharing ratio we consider several converter designs subjected to two main constraints. The board area dedicated to the converters being considered is the same in all cases. The overall inductor current slew rate for a large load transient should be the same for all designs.

First we take the case of a two phase converter with equal current sharing as a baseline for the board area. We consider the typical switch model for a commercial NMOS transistor (CSD17484F4) and assume that we are going to use a particular non-integer multiple of these switches as the switches for our two phase converter (to apply scaling laws on $R_{ds,on}$ and other parasitic components associated with switching loss calculations). Consider m_1

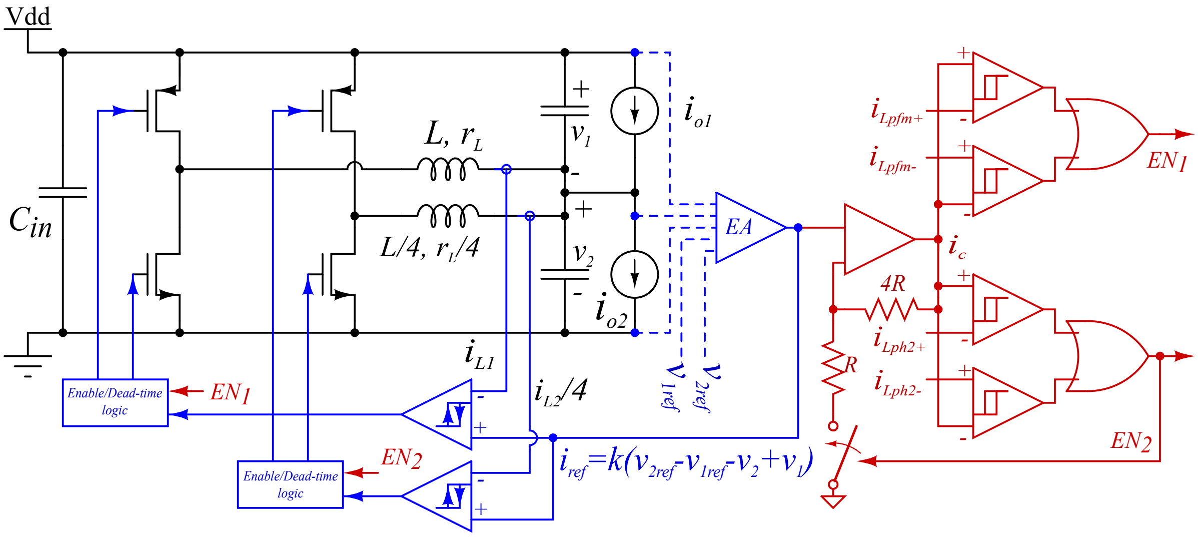


Figure 2.17: 2-phase DPP converter with 4:1 current sharing.

as the size of the switch used in the first phase (low current phase) and m_2 as the size of the switch to be used for the second phase. Of course, for the baseline case of equal current sharing, $m_1 = m_2 = m$.

The XEL4030 series of inductors was chosen since it was appropriate for our design specifications. Also, well defined power loss (DCR and AC losses) data was available for the series, and the inductance values offered allowed several current sharing ratios to be evaluated in simulations. Current sharing ratios of 1:1, 1:2, 1:4 and 1:8 are considered. The switching frequencies are chosen in manner similar to that for the converter in the previous section: all designs of phases are such that they contribute equal output voltage ripple, so f_{sw} is inversely proportional to $\sqrt{L}$. The multiplicity of the low current phase, m_1, is optimized for highest efficiency at critical current for ensuring good PFM mode efficiencies. m_2 is then calculated as $m_2 = 2m - m_1$ so that same switch area is maintained for all converters. The MATLAB script for the optimization of switch sizes, converter loss and efficiency calculations are provided in Appendix A.

The efficiency curves obtained for the four different sharing ratios are shown in Fig 2.18. The modeled efficiency curves show that significant efficiency improvements can be obtained from transitioning from a symmetric two phase design to an asymmetric design. Also, while the improvement is very significant between 1:1 ratio and 1:2 ratio, it is less so as we go for higher current sharing ratios. In these simulations, we have assumed a 5mA of constant current draw (for fixed power loss) from the output voltage rail. Output voltage ripple at light load can be estimated as shown in Fig 2.19.

2.3.1 Current sharing ratios and stack efficiency

To evaluate the impact of DPP converters with different current sharing ratios on the efficiency of the stack, Monte Carlo simulations were performed on a stack of eight voltage domains, each domain rated at 1.8 V. The efficiency models developed in the previous section were for a 7.2 V to 3.6 V DPP converter, which are the converters in the middle of the hierarchy in the hierarchical DPP topology (DPP_2 and DPP_6). We assume that the efficiency curves for the other DPP converters in the DPP stack are similar. If we define a loss function for the DPP_2 and DPP_6 as $loss\left(|i_L|\right)$ then the overall losses in the DPP stack are

$$\begin{aligned} P_{loss}\left(\mathbf{i_o}\right) =& \frac{1}{2}\left(P_{loss}\left(|i_{L1}|\right) + \left(P_{loss}\left(|i_{L3}|\right) + \left(P_{loss}\left(|i_{L5}|\right) + \left(P_{loss}\left(|i_{L7}|\right)\right)\right.\right.\right. \\ &+ \left(P_{loss}\left(|i_{L2}|\right) + \left(P_{loss}\left(|i_{L6}|\right) + 2P_{loss}\left(|i_{L4}|\right)\right.\right., \end{aligned} \quad (2.10)$$

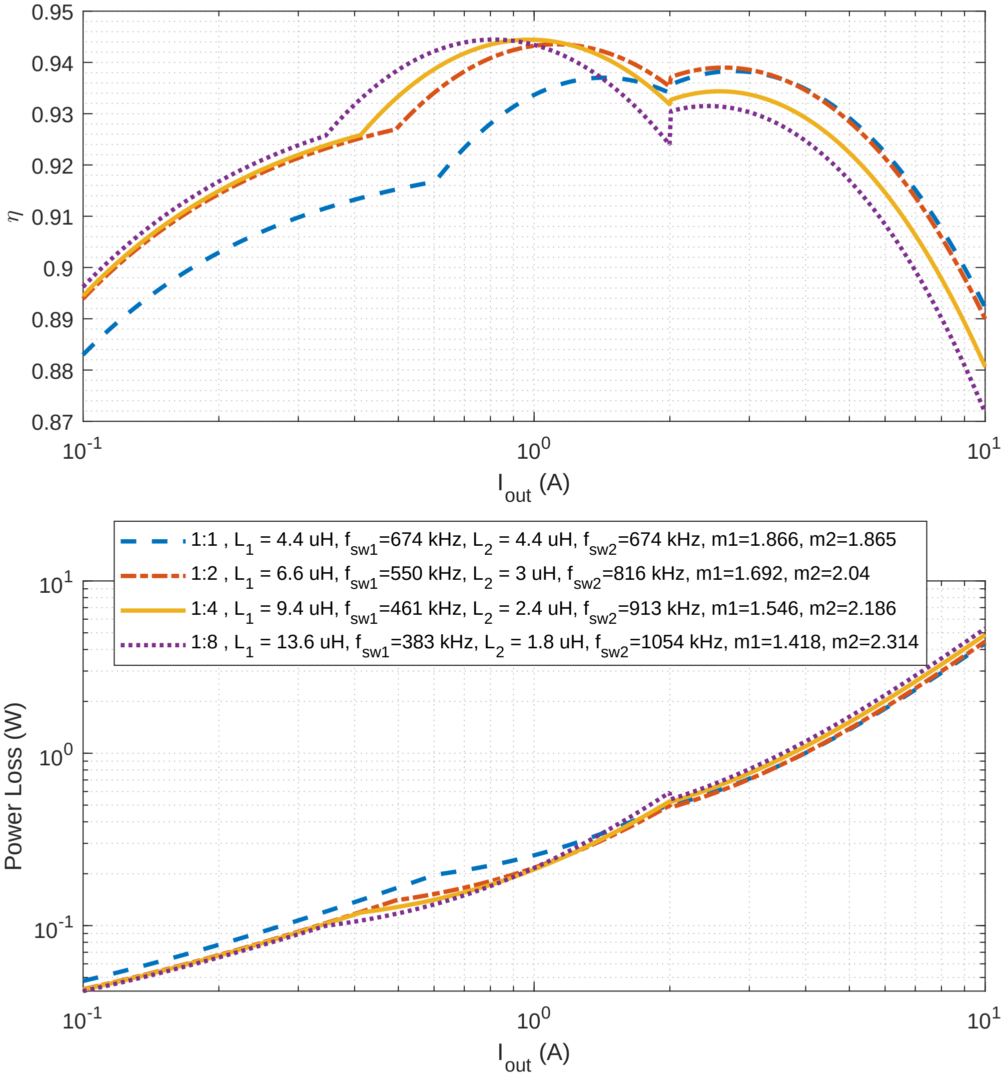


Figure 2.18: Efficiency comparison between two phase converter designs with different current sharing ratios. Note that even though the converters do not share current equally, the optimal switching point between 1 phase and two phase mode was observed to be around 2A in all cases.

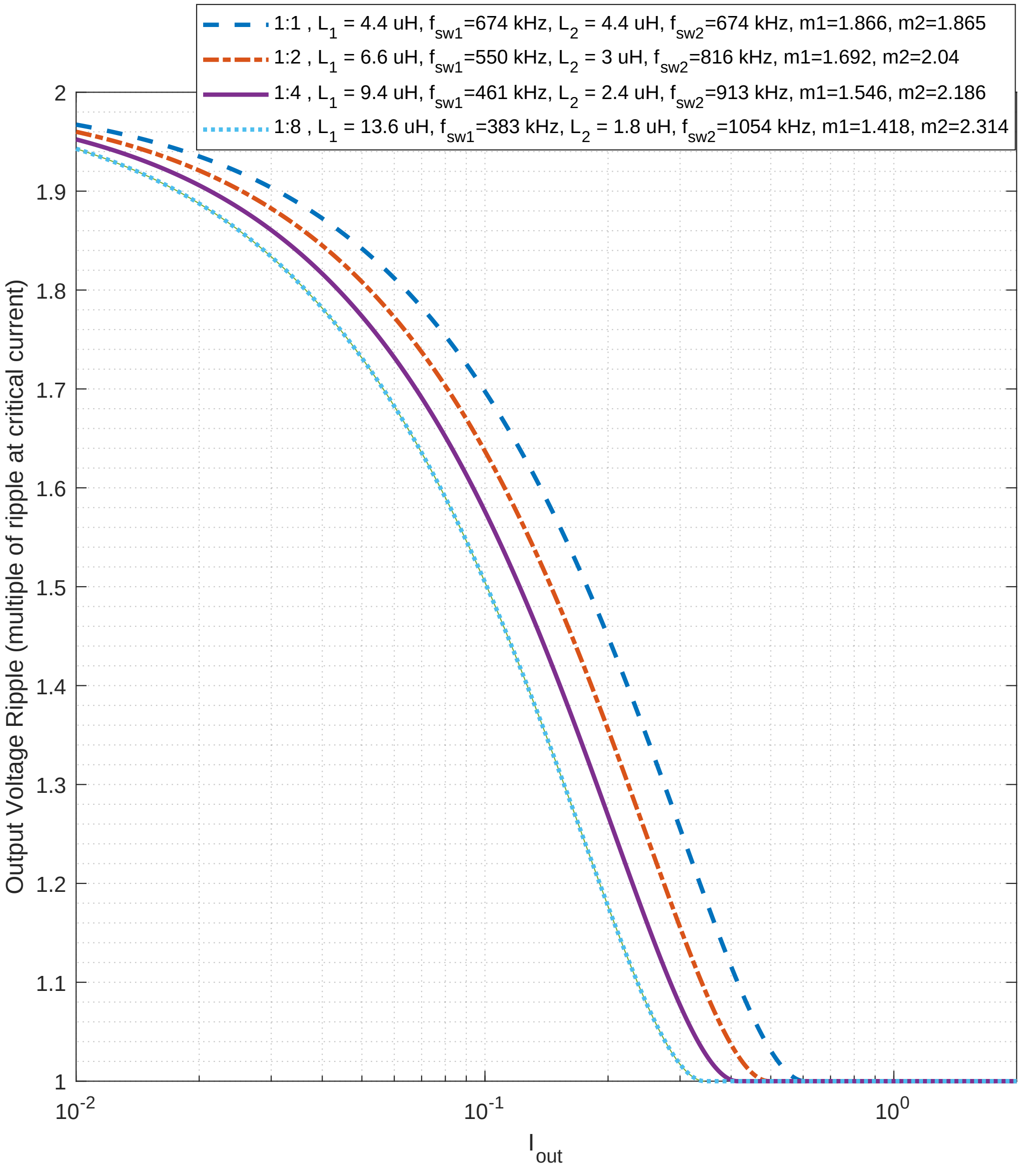


Figure 2.19: Light-load ripple comparison between different low current phase designs. Note that all the phases have been designed so that their individual contributions to output voltage ripple are the same while operating in continuous conduction mode.

where $\mathbf{i_o} = [i_{o,1}, i_{o,2}, i_{o,3}, i_{o,4}, i_{o,5}, i_{o,6}, i_{o,7}, i_{o,8}]'$ is the vector of load currents limited to 10 A. The steady state inductor currents of the DPP converters are as follows:

$$i_{L1} = i_2 - i_1 \tag{2.11}$$

$$i_{L3} = i_4 - i_3 \tag{2.12}$$

$$i_{L5} = i_6 - i_5 \tag{2.13}$$

$$i_{L7} = i_8 - i_7 \tag{2.14}$$

$$i_{L2} = \frac{1}{2}\left(i_4 + i_3 - i_2 - i_1\right) \tag{2.15}$$

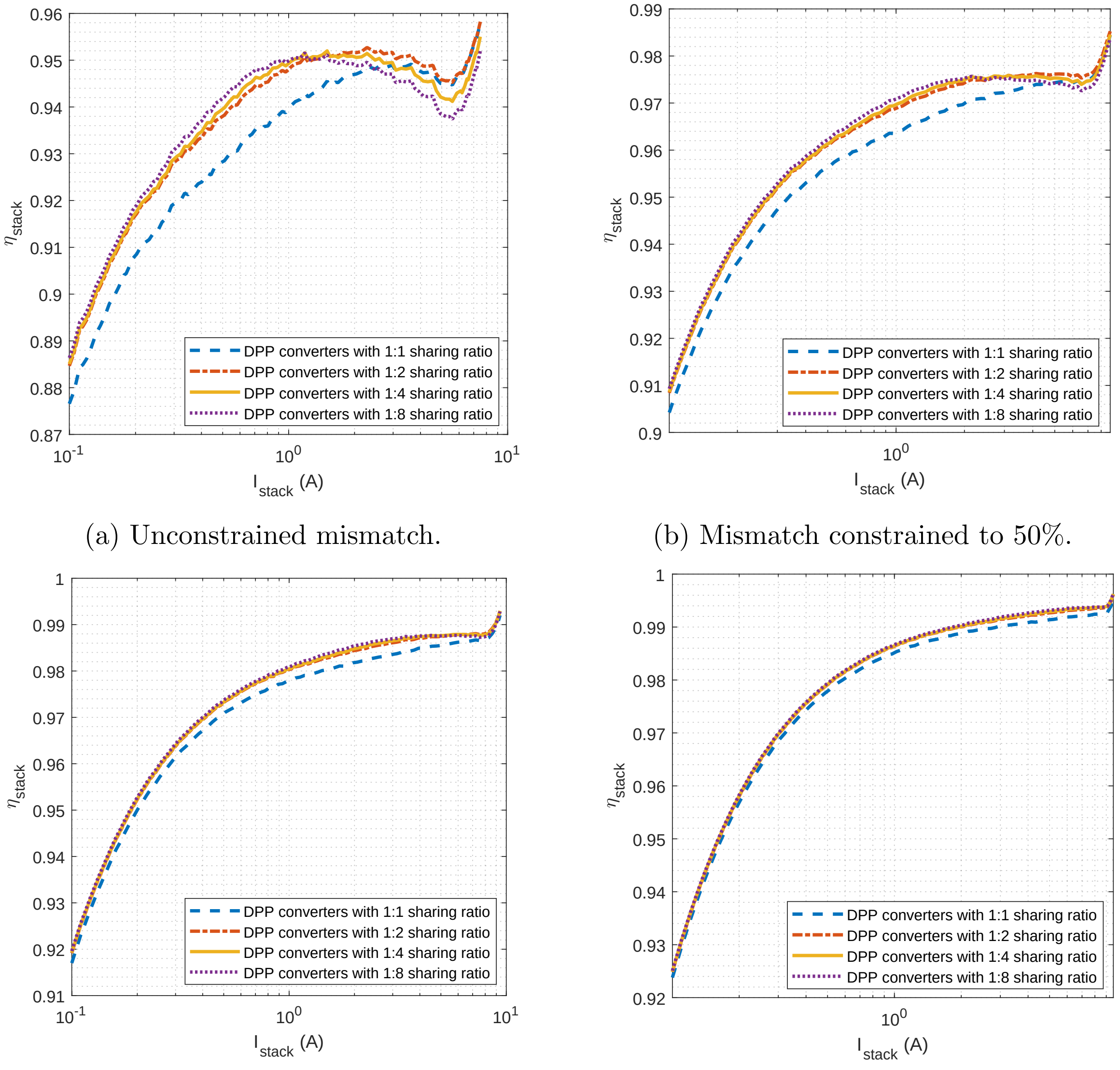
$$i_{L6} = \frac{1}{2}\left(i_8 + i_7 - i_6 - i_5\right) \tag{2.16}$$

$$i_{L4} = \frac{1}{4}\left(i_8 + i_7 + i_6 + i_5 - i_4 - i_3 - i_2 - i_1\right) \tag{2.17}$$

Monte Carlo simulations were performed to obtain averaged stack efficiencies for the DPP converters of different current sharing ratios. A uniform distribution of load currents was considered and four constraints were studied. As can be observed form the DPP stack efficiency simulations in Fig 2.20, all of the asymmetric current sharing cases offer improved light-load efficiencies for the whole stack over the symmetric DPP converter. It can even be seen that the 1:2 current sharing converter offers better average efficiency than the 1:1 current sharing converter in the unconstrained mismatch case (over the entire range of stack currents). The 1:4 current sharing converter matches the 1:1 converter in efficiency when mismatches are constrained to 50%. And the 1:8 converter offers better stack efficiencies than the 1:1 converter when mismatches are constrained to 25%. It is to be noted that all the DPP converter designs approach very high efficiency in the 98/99% range when the stack operates at near peak load and converter efficiencies almost become irrelevant. In the following section we discuss the implementation of a 1:4 current sharing DPP converter and present some hardware results.

2.3.2 Hardware Implementation

The specifications of the 1:4 current sharing DPP converter are the same as for the single phase design discussed before (7.2 V input - 3.6 V input, 10 A peak load current). These specifications are for the DPP converters in the middle of the hierarchy. The components used are listed in Table 2.4. The overall inductor current slew rate is approximately the same as for the single phase converter, and the output capacitance is also the same. So for hysteretic current mode control, the proportional output voltage regulation loop gain can also be kept the same for equivalent transient response and stability. The overall schematic



(a) Unconstrained mismatch.

(b) Mismatch constrained to 50%.

(c) Mismatch constrained to 25%.

(d) Mismatch constrained to 12.5%.

Figure 2.20: DPP converter stack efficiencies for varying stack current.

of the controller is shown in Fig 2.17. Simulations of the DPP converter were performed in LTSpice. Implementations of the converter and the control scheme of Fig 2.17 are shown in Fig 2.21.

The output capacitor voltage dynamics can be represented as:

$$i_{L1}\left(en_1\right) + i_{L1}\left(en_1\right) = C\frac{d}{dt}\left(v_2 - v_1\right) + \left(i_{o,2} - i_{o,1}\right) \tag{2.18}$$

The sensed currents of the two phases are in the ratios of the DC resistances of the two phases and can be represented as:

$$i_{L1,s} = gr_{L1}i_{L1}\frac{1 + s\left({}^{L_1}\!/_{r_{L1}}\right)}{1 + sr_sC_s} \tag{2.19}$$

$$i_{L2,s} = gr_{L2}i_{L2}\frac{1 + s\left({}^{L_2}\!/_{r_{L2}}\right)}{1 + sr_sC_s} = \left(\frac{gr_{L1}}{4}\right)\frac{1 + s\left({}^{L_1}\!/_{r_{L1}}\right)}{1 + sr_sC_s} \tag{2.20}$$

where r_s, C_s and g are the components of the DCR current sensing circuit described in the previous section. For current hysteretic control, a fast inner current loop imposes $i_{L1,s} = i_{ref}$ and $i_{L2,s} = i_{ref}$. For a proportional controller that equalizes the voltages of the two domains regulated by the DPP, $i_{ref} = k_p\left(v_1 - v_2\right)$. The dynamics of the fast inner current loop for hysteretic current control are assumed to be very fast. The hysteretic current controller sets the average inductor current to the reference current always in less than two switching cycles, and as long as a converter bandwidth close to the switching frequency is not targeted, this assumption is very realistic (even in a large signal sense [45]).

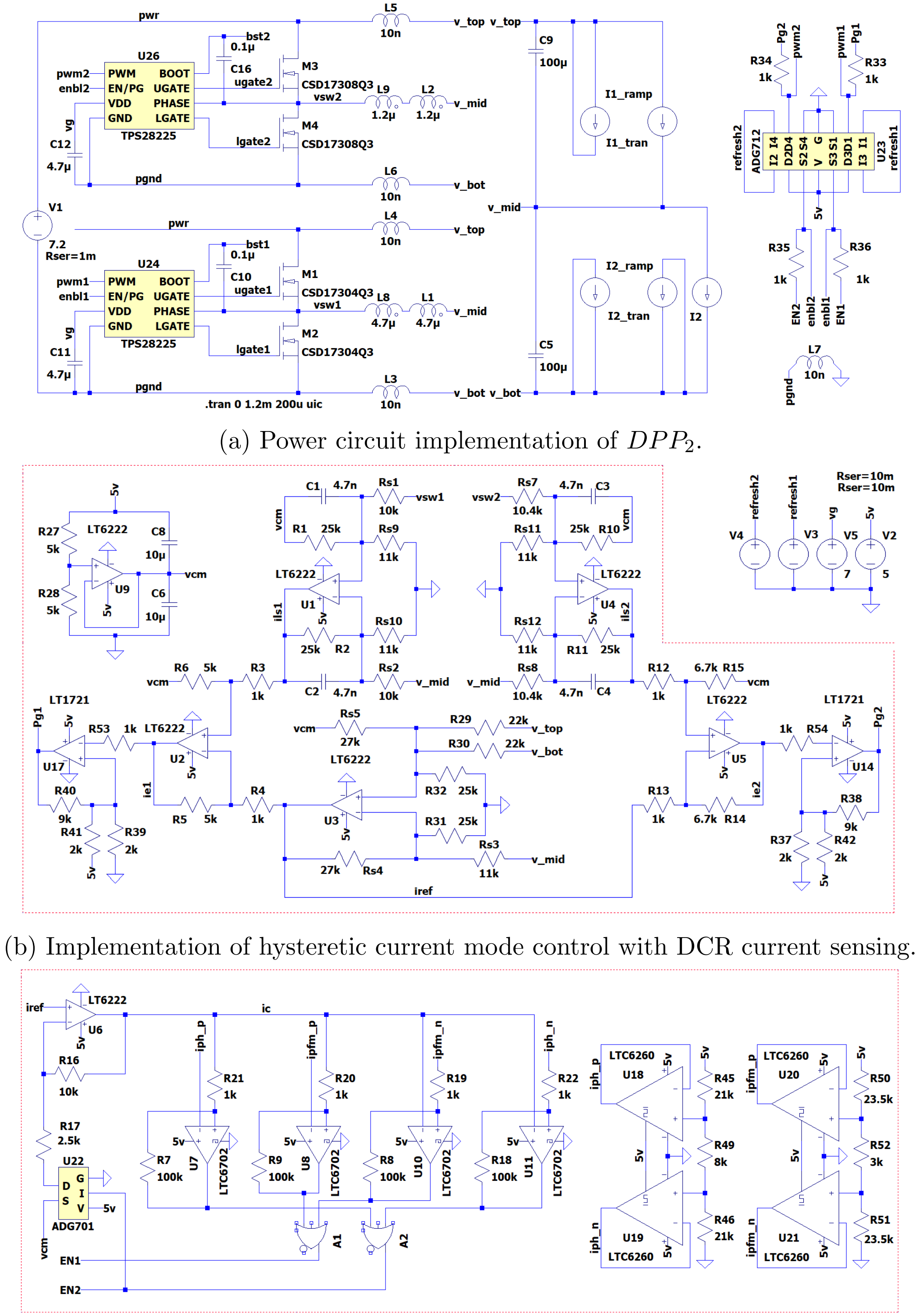
$$i_{L1} = \frac{k_p}{gr_{L1}}\left(\frac{1 + sC_sr_s}{1 + s\left({}^{L_1}\!/_{r_{L1}}\right)}\right)\left(v_1 - v_2\right) \tag{2.21}$$

$$i_{L2} = \frac{k_p}{gr_{L2}}\left(\frac{1 + sC_sr_s}{1 + s\left({}^{L_2}\!/_{r_{L2}}\right)}\right)\left(v_1 - v_2\right) = \frac{4k_p}{gr_{L1}}\left(\frac{1 + sC_sr_s}{1 + s\left({}^{L_1}\!/_{r_{L1}}\right)}\right)\left(v_1 - v_2\right) \tag{2.22}$$

Denoting $v_2 - v_1 = \Delta v$ and $i_1 - i_2 = \Delta i$, the transfer function ${}^{\Delta v(s)}\!/_{\Delta i(s)}$ can be derived as

$$\frac{\Delta v(s)}{\Delta i(s)} = \frac{1 + s\left({}^{L_1}\!/_{r_{L1}}\right)}{k_{sw} + s\left(C_o + k_{sw}C_sr_s\right) + s^2\left({}^{C_oL_1}\!/_{r_{L1}}\right)} \tag{2.23}$$

where the gain term $k_{sw} = {}^{k_p}\!/_{gr_{L1}}\left[en_1 + 4en_2\right]$ is dependent on the number of phases enabled and is a parameter for design. Denoting $\omega_L = {}^{r_{L1}}\!/_{L_1}$ and $\omega_s = {}^{1}\!/_{r_sC_s}$. The transfer function can be rewritten as



(a) Power circuit implementation of DPP_2.

(b) Implementation of hysteretic current mode control with DCR current sensing.

(c) Implementation of bidirectional PFM and phase shedding controller.

Figure 2.21: Implementation of the second stage DPP converters (LTspice).

$$\frac{\Delta v(s)}{\Delta i(s)} = \frac{1 + {}^{s}\!/_{\omega_L}}{k_{sw} + s\left(C_o + \frac{k_{sw}}{\omega_s}\right) + s^2\left({}^{C_o}\!/_{\omega_L}\right)} \tag{2.24}$$

The system is always small signal stable. For $\omega_s \leq \omega_L$ it can be shown that the poles of the system are always placed on the real axis and no oscillatory behavior is encountered. An imaginary component of the poles may appear for low values k_{sw} when $\omega_s > \omega_L$. Since the controller's phase shedding operation is coupled with the current sensing amplifier, it is necessary that the sensed current is an accurate representation of the actual inductor current. So, in our design we keep $\omega_s = \omega_L$ and design k_{sw} for an appropriate time constant (fraction of the switching time period of the lower current phase).

SPICE simulations in Fig 2.22 shows the operation of the converter in PFM mode at light load. The reference current i_{ref} increases when en_1 is low during a light positive differential current load. At this point en_2 is low, so the gain of the switched gain amplifier is set to 1 and $i_c = i_{ref}$. When i_c hits the upper hysteretic limit, en_1 goes high and the low current phase tracks the reference current. This causes i_{ref} to decrease, and eventually when i_c hits the lower hysteretic limit en_1 is turned low. Phase addition operation during a slow ramp of differential current is shown in Fig 2.23. When the droop in voltage becomes too high for the low current phase and i_c reaches the upper hysteretic limit for phase addition, en_2 is turned high. This causes the switched gain amplifier to operate at a gain of 5. The control current i_c, which is supposed to be a measure of the total differential current load, is now set to $5 \times i_{ref}$. This prevents the high current phase from turning off immediately after turning on and avoids jittering. SPICE simulation results for a transient from light load to maximum differential current load are shown in Fig 2.24. A transient response from medium positive differential load to a medium negative load is shown in Fig 2.25. Both these transient responses show that there is significant delay in phase addition operation due to the hysteretic nature of the controller that determines phase addition. The delay can be lowered by increasing the gain of the error amplifier that generates i_{ref} but it is a tradeoff against transient stability.

The hardware prototype is shown in Fig 2.26. The controller schematic shown in Fig 2.17 is implemented in analog domain using the parts shown in the SPICE simulation setup of Fig 2.21. The same prototype is used to validate the single phase design discussed before; the second phase was desoldered and instead the first phase was populated with components corresponding to Table 2.1. Efficiency data obtained from this two phase prototype is compared with that from the single phase converter in Fig 2.28. Fig 2.27 show a close cor-

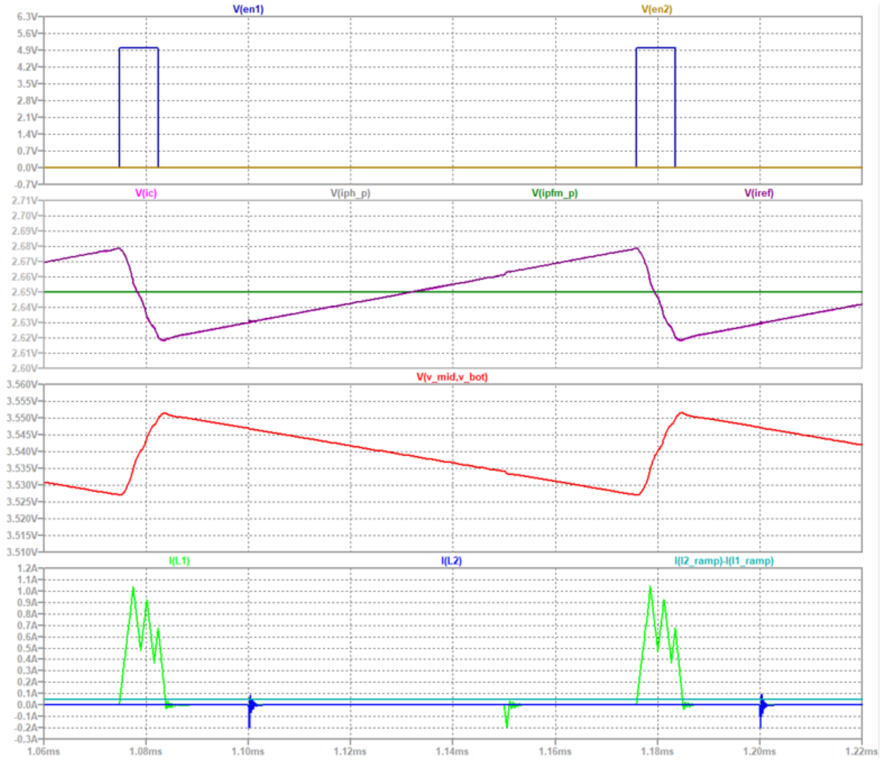


Figure 2.22: Light-load operation at 50 mA differential current (SPICE simulations).

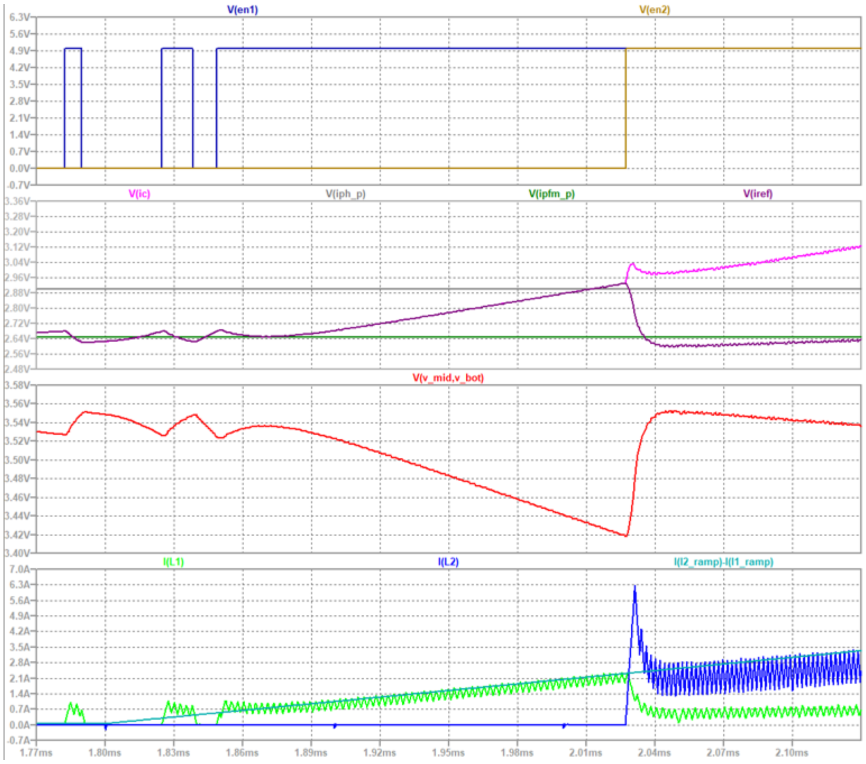


Figure 2.23: Phase addition during a slow ramping load (SPICE simulations).

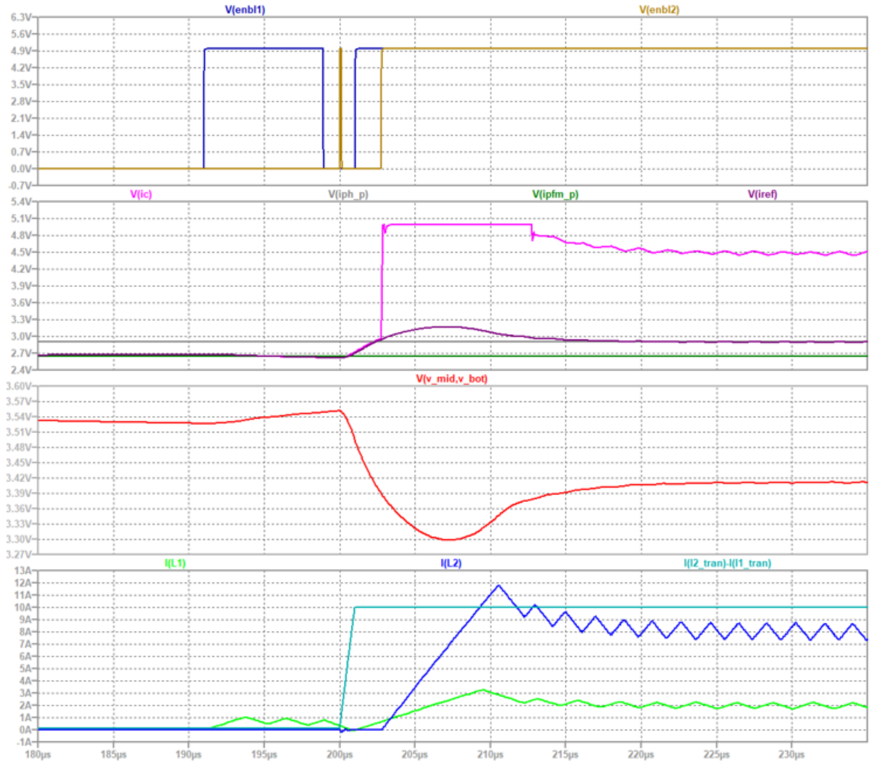


Figure 2.24: Response to a positive differential current transient (SPICE simulations).

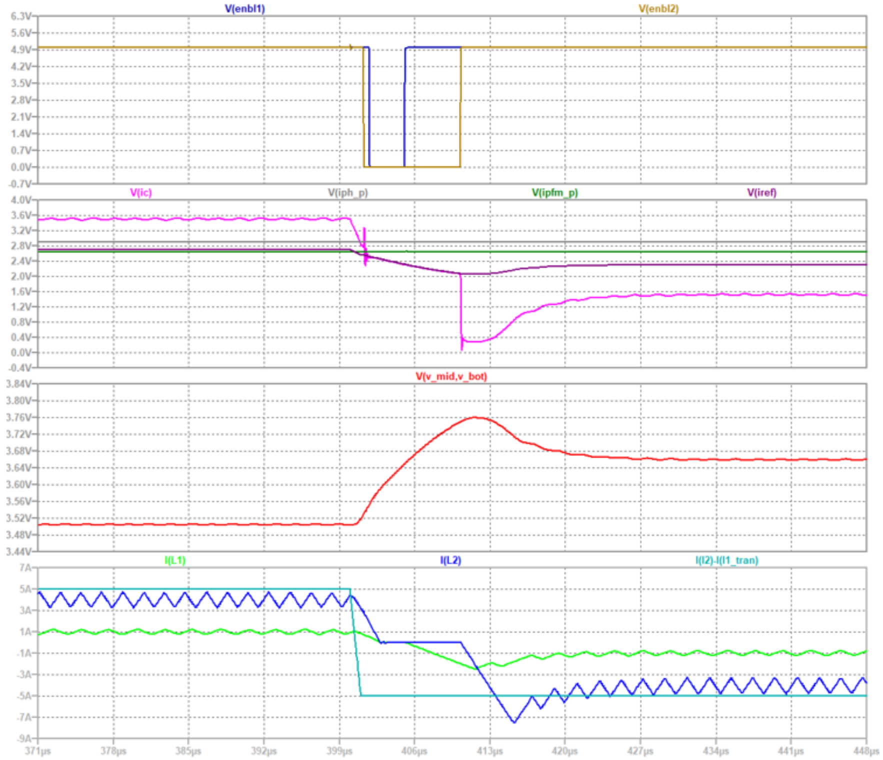


Figure 2.25: Response to a negative differential current transient (SPICE simulations).

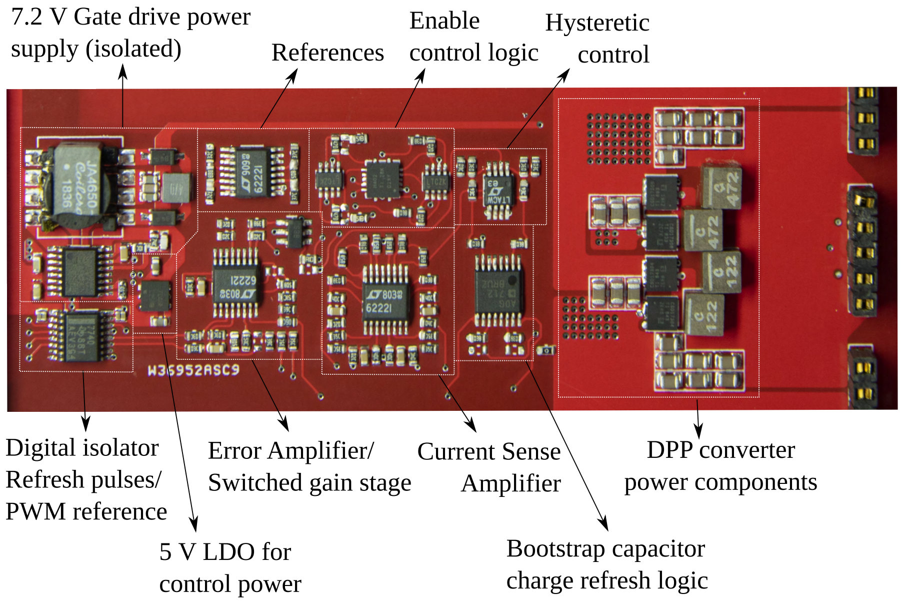


Figure 2.26: Hardware prototype of the two-phase asymmetric current sharing DPP converter.

Table 2.4: Two-Phase DPP converter components

Component	Part Number	Specifications
Switch (Phase 1)	CSD17308Q3D	$r_{DS,on} = 9\text{m}\Omega$, $Q_g = 3.9$ nC
Inductor (Phase 1)	XEL4030	2×4.7 μH, $r_L = 40$ mΩ
Switch (Phase 2)	CSD17304Q3D	$r_{DS,on} = 5$ mΩ, $Q_g = 5.1$ nC
Inductor (Phase 2)	XEL4030	2×1.2 μH, $r_L = 11$ mΩ
C_{out}	GRM21BR61E226ME44K	7×22 μF, $R_{esr} = 3m\Omega$
C_{in}	GRM21BR61E226ME44K	3×22 μF, $R_{esr} = 3m\Omega$
Gate Driver	TPS28225	7.2 V, 2 A source, 4 A sink

respondence between simulated and experimental efficiencies. Figs 2.29, 2.30 and 2.31 show experimental transient responses of the DPP converter for several types of load transients. Fig 2.31 shows some heavy load transients where the second phase needs to be enabled. The current sharing ratio observed in the experimental waveforms shows a slight deviation from the targeted 1:4 ratio. This is due to the additional resistance of the wiring introduced for inductor current observation. The apparent heavy droops in output voltage (500 mV for a 10 A differential load) are due to the input voltage drooping at heavy loads as can be confirmed from Fig 2.31d. The droops encountered in the fully assembled system (with a PI controlled stack converter) are much lower as will be shown in Chapter 4.

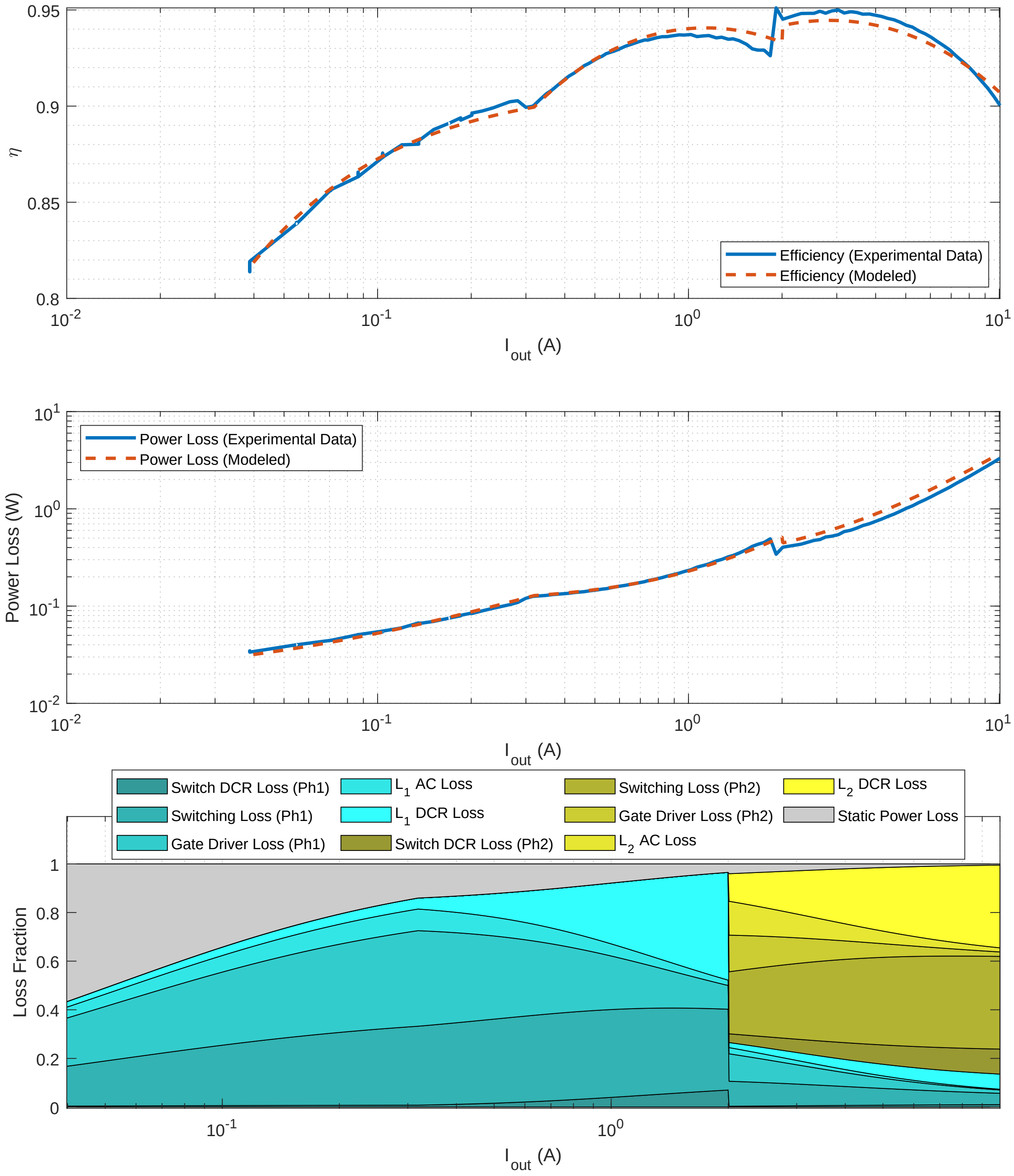


Figure 2.27: Efficiency of 7.2 V - 3.6 V DPP converter. Blue shows hardware efficiency and red shows modeled efficiency.

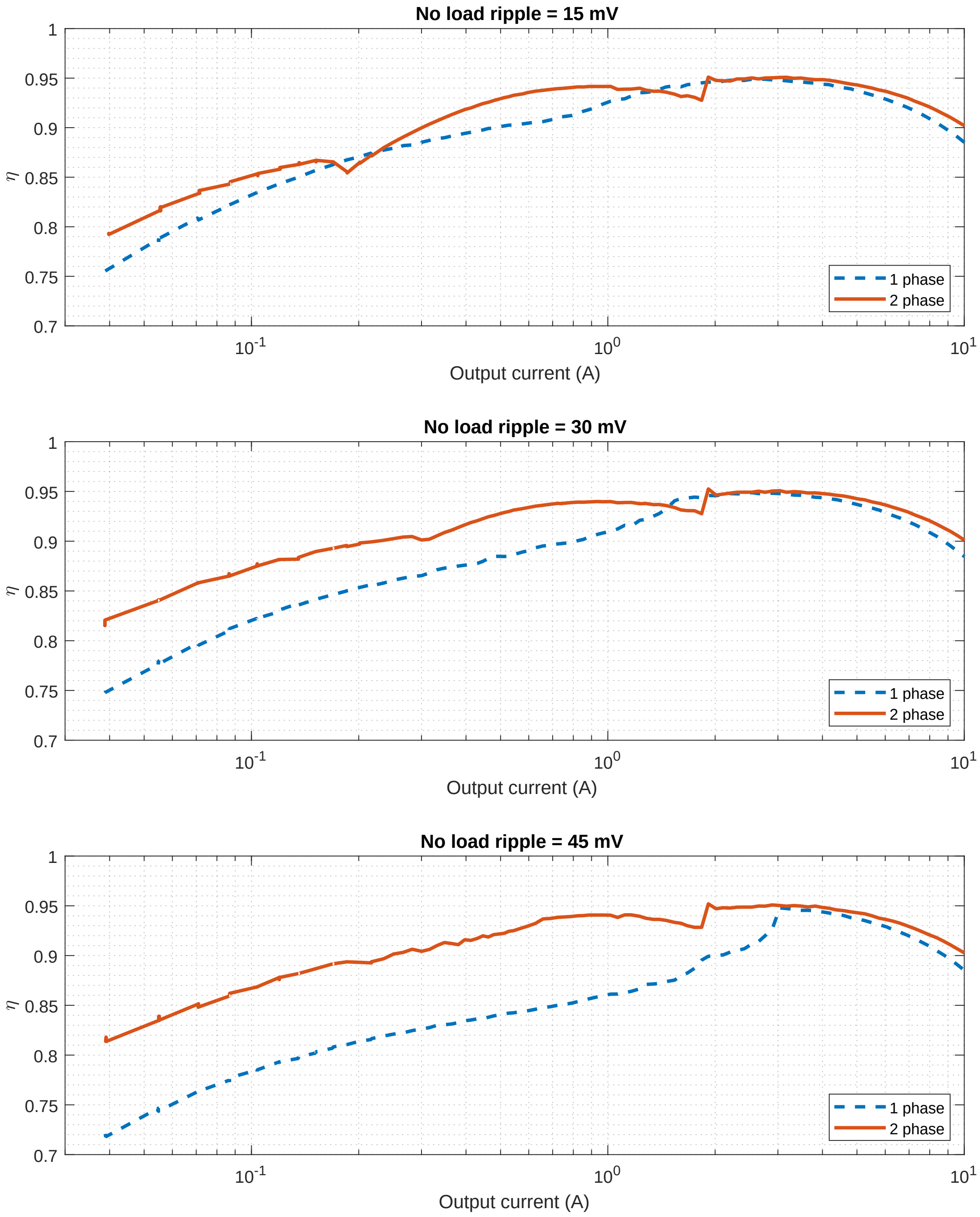
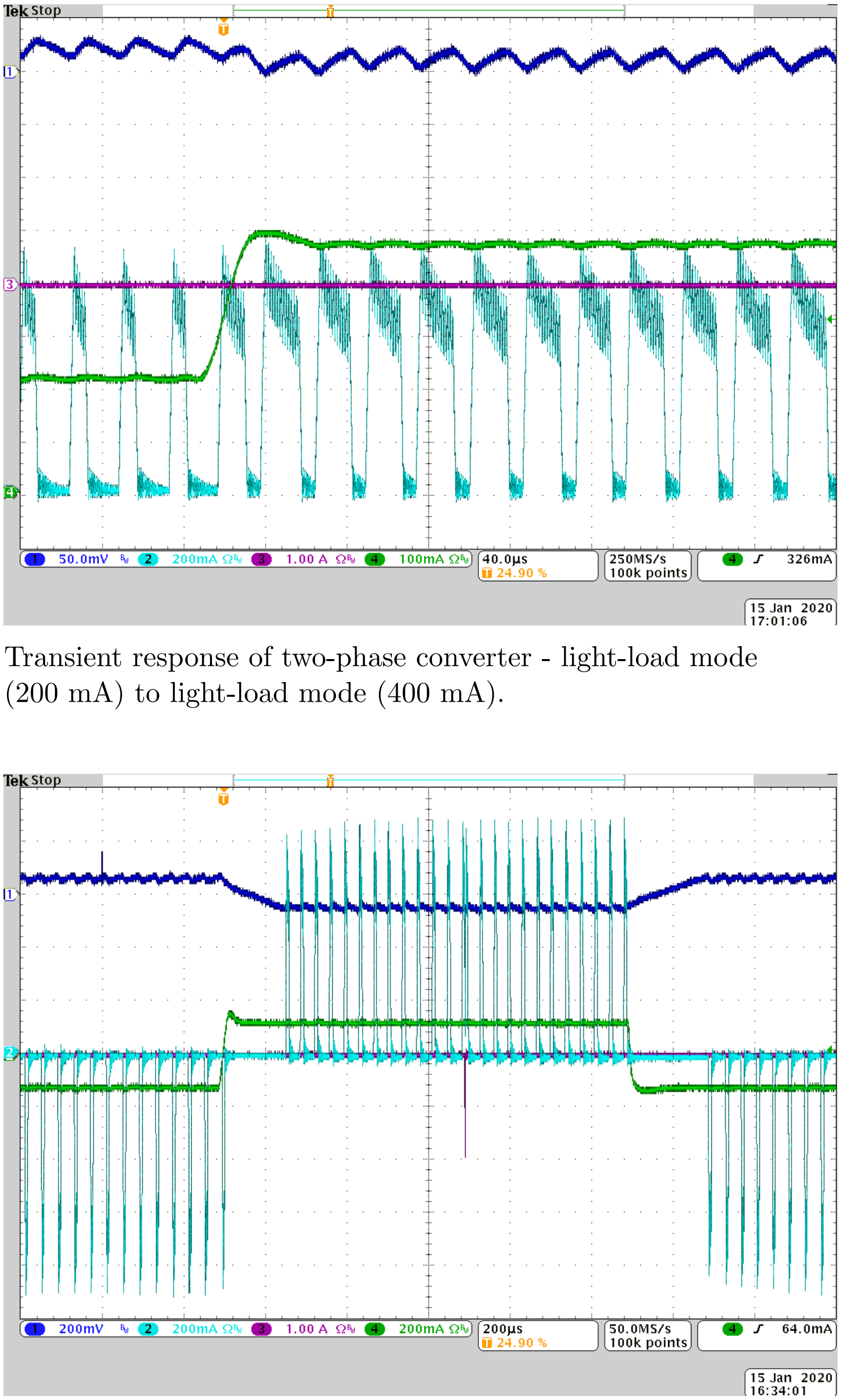


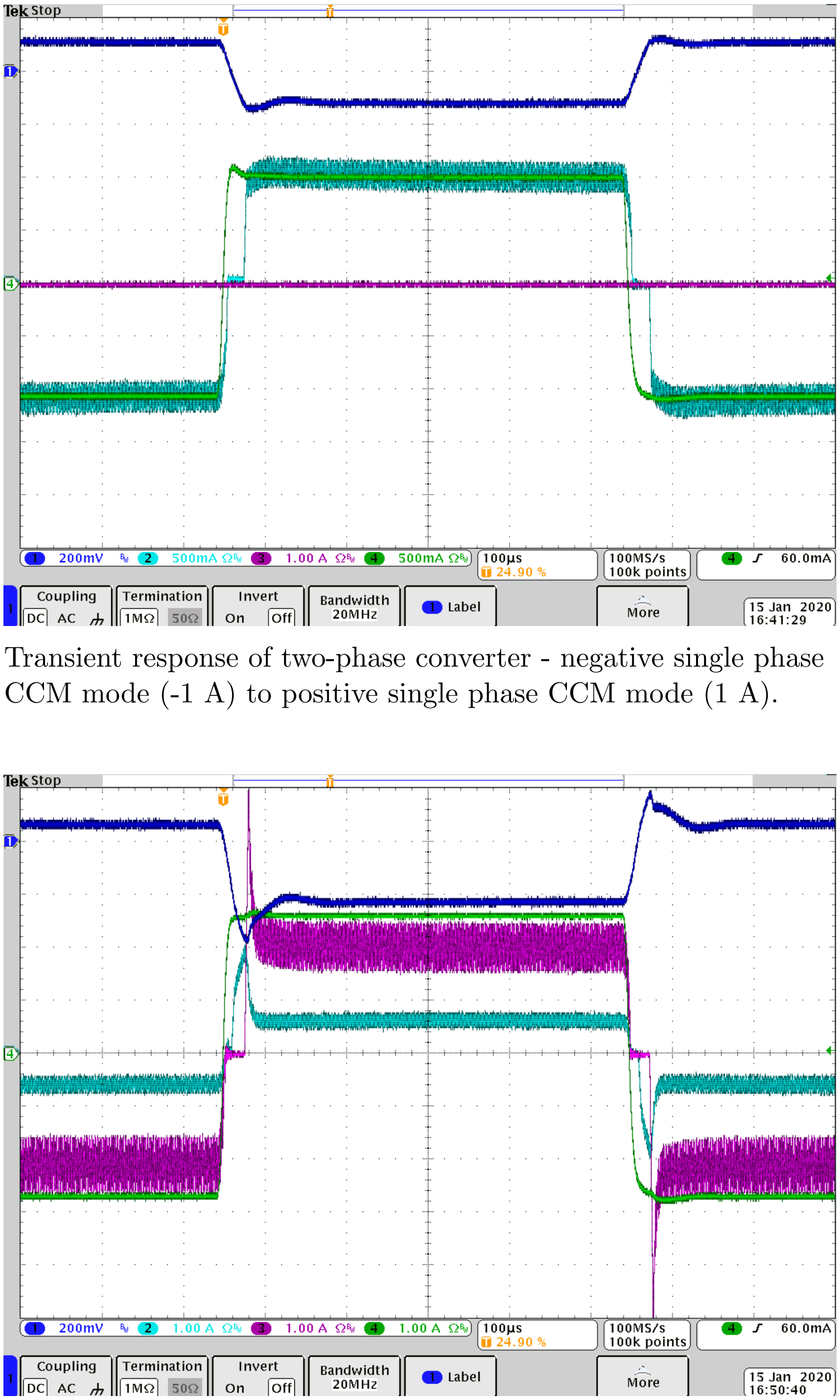
Figure 2.28: Efficiency comparison between two-phase converter with 1:4 current sharing and single phase converter.



(a) Transient response of two-phase converter - light-load mode (200 mA) to light-load mode (400 mA).

(b) Transient response of two-phase converter - negative light-load mode (-200 mA) to positive light-load mode (200 mA).

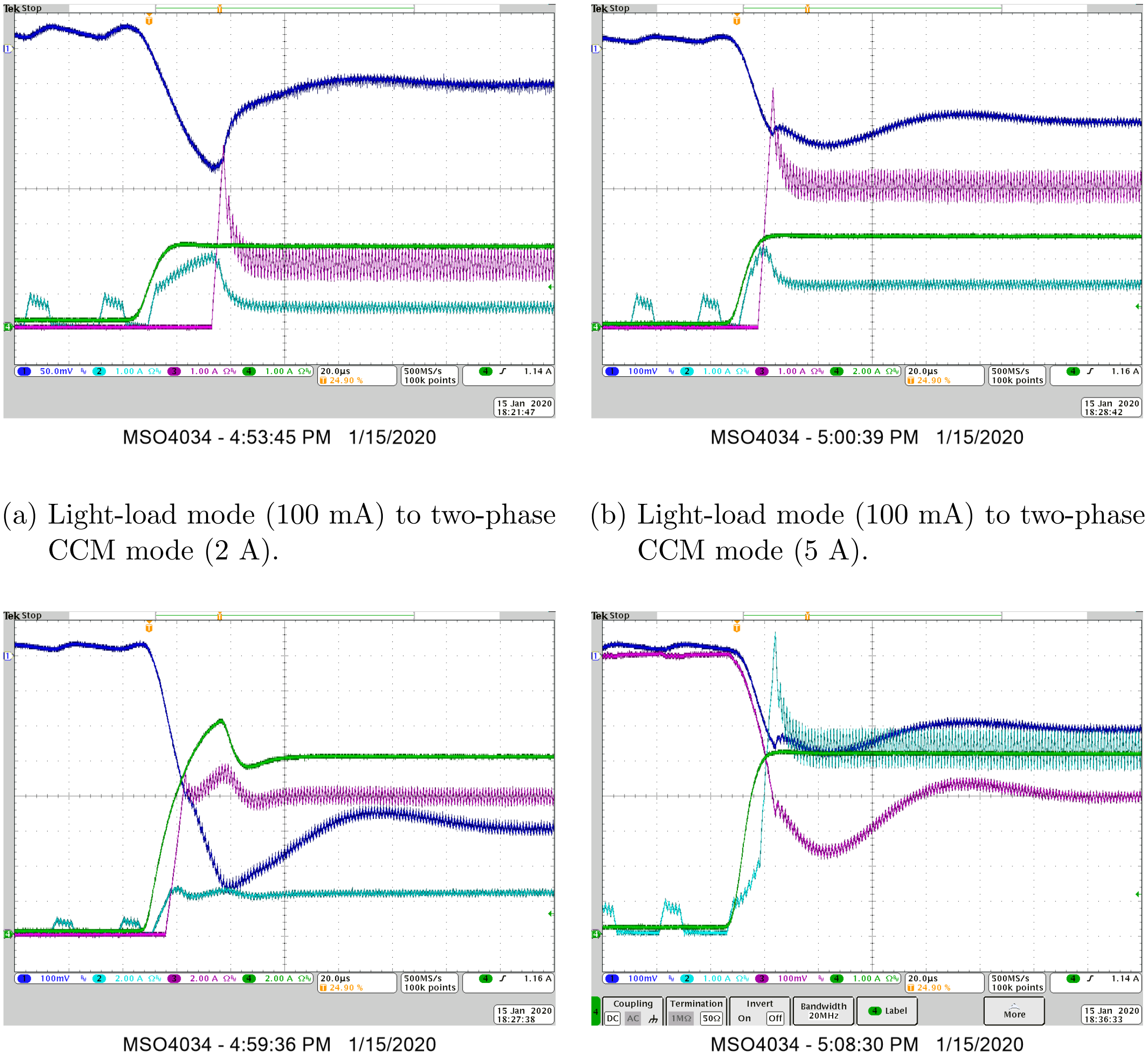
Figure 2.29: Light-load operation transients. Channel 1: Output voltage (3.6 V offset). Channel 2: Low current phase inductor current. Channel 3: High current phase inductor current. Channel 4: Differential load current.



(a) Transient response of two-phase converter - negative single phase CCM mode (-1 A) to positive single phase CCM mode (1 A).

(b) Transient response of two-phase converter - negative two-phase mode (-2.5 A) to positive two-phase mode (2.5 A).

Figure 2.30: Intermediate/heavy load operation transients. Channel 1: Output voltage (3.6 V offset). Channel 2: Low current phase inductor current. Channel 3: High current phase inductor current. Channel 4: Differential load current.



(a) Light-load mode (100 mA) to two-phase CCM mode (2 A).

(b) Light-load mode (100 mA) to two-phase CCM mode (5 A).

(c) Light-load mode (100 mA) to two-phase CCM mode (10 A).

(d) Light-load mode (100 mA) to two-phase CCM mode (5 A). Input voltage droop.

Figure 2.31: Intermediate/heavy load operation transients. For subfigures (a), (b) and (c): Channel 1 shows output voltage (3.6 V offset, 50 mV/div), Channel 2 shows low current phase inductor current (1 A/div), Channel 3 shows high current phase inductor current (1 A/div) and Channel 4 shows differential load current. For subfigure (d): Channel 2 shows sum of inductor currents and Channel 3 shows input voltage. Horizontal time scale = 20 μs/div.

CHAPTER 3

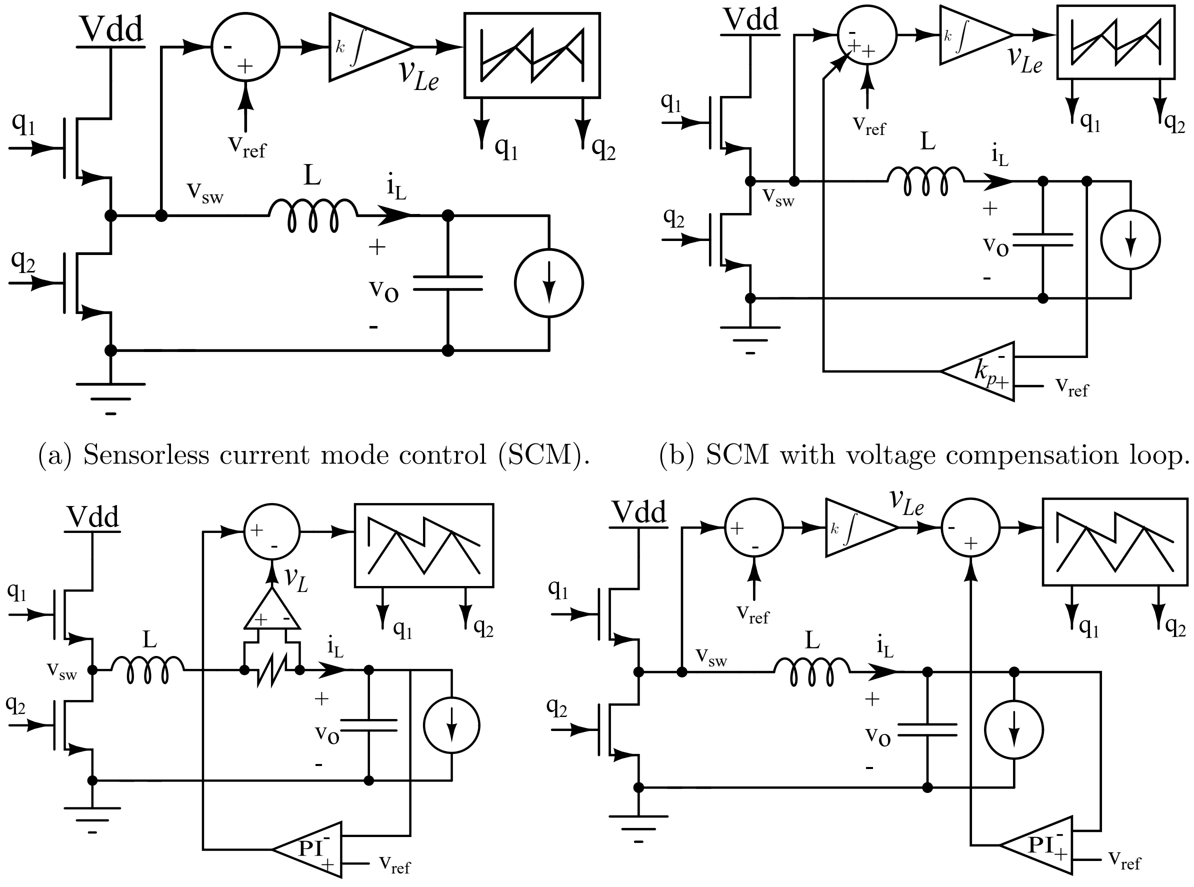
STACK CONVERTER

3.1 Design of the stack converter

The converter supplying the stack of eight loads is to be powered from a 48 V bus. It is to be rated for the full stack current 10 A at 14.4 V output. Since the input voltage is considerably higher than for the DPP converter designs, switching at a high frequency like the DPP converters is not a viable option. We propose a two-phase interleaved buck converter design for the stack converter for its ripple cancelling properties. The stack converter needs to be efficient at light loads as the system's overall efficiency is the product of the efficiency of the stack converter and the efficiency of the DPP converter stack (not referring to the individual DPP converter efficiency). To achieve a wide load range we propose a phase rotating light-load pulse skipping control scheme. The converter is shown to maintain above 90% efficiency without phase shedding over nearly a 100x load range. It also needs to provide fast load transient response (not nearly as stringent as it would be for the original parallel connected system), since the voltage regulation of the intermediate nodes can only be as fast as the stack converter's load transient response is. This requirement would recommend the use of current mode control as it has been known to ensure faster and stabler closed loop control designs in dc-dc converters in general. Current mode control also has the added advantage of offering near ideal line transient response (audio susceptibility) which may be important for slow 48 V buses.

A variant of sensorless current mode control [52], [53] is proposed in this section. Instead of directly sensing the inductor current with a shunt resistor or sensing switch currents as in conventional current mode control implementations, an observer is used to estimate the inductor current (or flux) as shown in Fig 3.1a. Sensorless current mode control scheme provides load regulation to some extent in open loop (current mode control itself is not operable without an outer voltage control loop) like a conventional PWM duty ratio controller. It has the additional advantage of achieving near ideal line regulation (like current mode control) while operating in open loop. To compensate for the voltage drops or optimize load transient responses, an additional error compensation term could be included in the controller as shown in Fig 3.1b. However, with sensorless current mode control in its original form, only ac information of the inductor current is observed. The modified sensorless current mode control scheme is designed to retain the dc information of the inductor currents, which facilitates multiphase designs and light load control.

The modified sensorless current mode controller shown in Fig 3.1d has some similarities with a conventional current mode control loop in that the voltage error provides a load current estimate. The scheme for the inductor current observer from sensorless current mode control is the same. A peak current mode type of modulator with slope compensation is then used to compare the estimated inductor current to a reference current (generated by an output voltage feedback loop) to generate the switching pulses for the individual phases for generating interleaved switching pulses.



(a) Sensorless current mode control (SCM).

(b) SCM with voltage compensation loop.

(c) Peak current mode control (PCM).

(d) Modified SCM used in this thesis.

Figure 3.1: Current mode control. (v_L and v_{Le} are the sensed and estimated inductor currents). The outer voltage compensation loop is repositioned so that a dc estimate of the load current can be obtained and used for light load control.

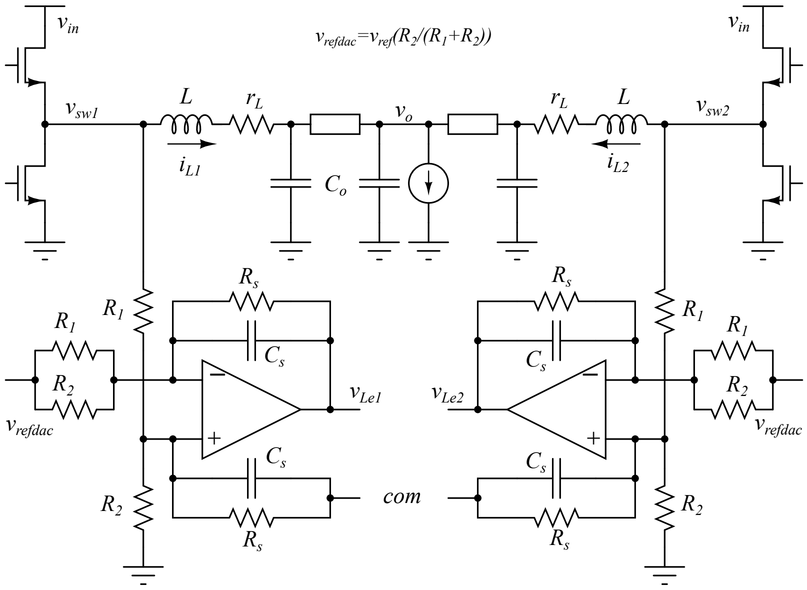


Figure 3.2: Schematics of 2-phase converter and inductor current observer.

3.2 Small signal modeling and control design

The schematics for the inductor current estimator for the two phases of the stack converter is shown in Fig 3.2. The switching node voltage can be directly used to estimate the voltage across the inductor. The observed inductor current is

$$\begin{aligned}
v_{Le} =& \frac{R_s\left(v_{sw} - v_{ref}\right)}{R_1\left(1 + sR_sC_s\right)} && (3.1)\\
=& i_L\left(\frac{r_LR_s}{R_1}\right)\left(\frac{1 + s\left(L/r_L\right)}{1 + sR_sC_s}\right) + \left(\frac{R_s}{R_1}\right)\frac{v_o - v_{ref}}{1 + sR_sC_s} \\
=& i_LR_i\left(\frac{1 + s\left(L/r_L\right)}{1 + sR_sC_s}\right) + \left(\frac{R_s}{R_1}\right)\frac{v_o - v_{ref}}{1 + sR_sC_s} && (3.2)
\end{aligned}$$

Similar to the DCR current sensing method applied in the last chapter, the time constants L/r_L and R_sC_s can be matched to obtain a simplified expression for the estimated inductor current. Considering R_i as the DC gain of the current sensing system, the inductor current observer can be expressed as

$$G(s) = \left(\frac{1 + s\left(L/r_L\right)}{1 + sR_sC_s}\right) = 1 \tag{3.3}$$

$$v_{Le} = R_i\left(i_L + \frac{v_o - v_{ref}}{Z_L}\right)G(s) = R_i\left(i_L + \frac{v_o - v_{ref}}{Z_L}\right) \tag{3.4}$$

The peak current mode type of modulator with slope compensation is shown in Fig 3.3a.

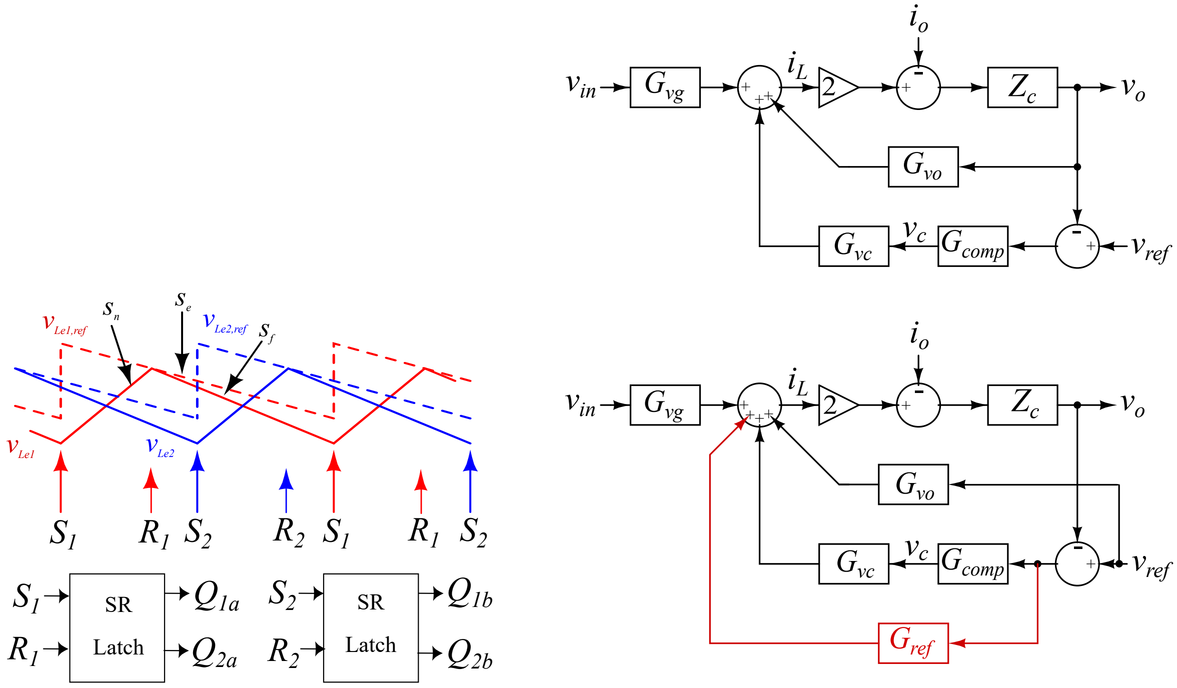
When the inductor current is directly controlled by this type of modulator, the small signal model in general can be represented as

$$\hat{i_L} = G_{vg}\hat{v_{in}} + G_{vo}\hat{v_o} + G_{vc}\hat{v_c} \tag{3.5}$$

In the case of the observer based controller we directly control the observer instead of the actual inductor current. The same modulator model can be used in case of the observer based controller with a small adaptation. The output voltage does not play any part in the computation of the inductor current observer and is replaced by v_{ref}.

$$\hat{i_{Le}} = \frac{v_{Le}}{R_i} = G_{vg}\hat{v_{in}} + G_{vo}\hat{v_{ref}} + G_{vc}\hat{v_c} \tag{3.6}$$

Modeling of peak current mode control in multiphase buck converters has been studied in great detail in the last few decades, and small signal models of the peak current mode modulator of various degrees of accuracy exist in literature. Averaged modeling based approaches, although accurate over low frequencies, fail to accurately predict converter behavior at higher frequencies (nearing half the switching frequency) [54]. Sampled data modeling of convert-



(a) Modulator for sensorless current mode control (peak mode).

(b) Small signal model for peak and modified sensorless current mode controllers.

Figure 3.3: Sensorless current mode control modulator and small signal model.

ers, [55], yields much more accurate control to output models for current mode control and ultimately leads to one of the most popular models of the peak current mode modulator [56]. Other than frequency domain approaches to modeling of the peak current mode modulator there have also been time domain modeling approaches such as [57] and [58]. The models that we utilize here are elaborated in [59] and [60] because of their accuracy and proven extendability to multiphase converters.

From the expression of estimated inductor current v_{Le} in Equation 3.4, we can see that there is a current component with sensing gain and an additional output voltage feedback term which is modulated by the peak current mode modulator shown in Fig 3.3a. The small signal equivalent model of the peak current mode controller is shown in Fig 3.3b, where the transfer functions G_{vg}, G_{vo} and G_{vc} are given as

$$G_{vc} = \frac{\hat{i_L}}{\hat{v}_c} = \left[\frac{(s_n + s_f)\left(1 - e^{-sT_{sw}}\right)}{(s_n + s_e) + (s_f - s_e)\, e^{-sT_{sw}}} \right] \frac{f_s}{R_i s} \tag{3.7}$$

$$G_{vg} = \frac{\hat{i_L}}{\hat{v}_g} = \left[D - \frac{(s_n + s_f)\left(1 - e^{-sDT_{sw}}\right)}{(s_n + s_e) + (s_f - s_e)\, e^{-sT_{sw}}} \frac{f_s}{s} \right] \frac{1}{Ls} \tag{3.8}$$

$$G_{vo} = \frac{\hat{i_L}}{\hat{v}_o} = \left[\frac{(s_n + s_f)\left(1 - e^{-sT_{sw}}\right)}{(s_n + s_e) + (s_f - s_e)\, e^{-sT_{sw}}} \frac{f_s}{s} - 1 \right] \frac{1}{Ls} \tag{3.9}$$

where s_n is the rising slope of the sensed inductor current, s_f is the falling slope of the sensed inductor current and s_e is the slope of the compensation ramp. The sensorless current mode controller introduced above has form very similar to that of peak current mode control with G_{ref} introduced due to the additional term in the expression derived for the estimated inductor current. G_{ref} is given by

$$G_{ref} = \frac{1}{Ls + r_L} \tag{3.10}$$

The validity of this analytical small signal model is tested by simulating four closed loop performance parameters, loop gain, output impedance, audio susceptibility and reference tracking, and comparing them with actual switching models. A simple PI controller that offered a 25 kHz bandwidth and 70° phase margin for both peak and sensorless current mode controllers was used to close the output voltage control loop (Fig 3.4). The compensated loop gain for the peak current mode controller is shown in Fig 3.4. With peak current mode control, the inherent double pole of the output filter of the buck converter gets separated because of the fast inner current loop, and improved phase margin is obtained with respect to conventional voltage mode control. The loop gain of the sensorless current mode control looks similar to loop gain of voltage mode control loops with unseparated double poles. However, the additional G_{ref} component in case of the sensorless current mode control loop is responsible for placing a low frequency zero in the control loop which improves phase margin. Comparable phase margins are obtained by the two methods using the same outer voltage loop controller in both cases. Different values of slope compensation have similar effects on phase margin for both these cases. Moreover, it is possible to obtain near null audio susceptibility from peak and sensorless current mode controls with $s_e = {}^{s_f}\!/_2$, [61]. This is true for the modified version of sensorless current mode control as well. The PI controller output was sampled at the switching frequency and it was modeled to have a time delay of half the switching time period. The continuous time domain transfer function of the PI controller used in the simulations is given by

$$G_{comp} = \left(k_p + \frac{k_i}{s}\right) e^{-sT_{sw}/2} \frac{\left(1 - e^{-sT_{sw}}\right)}{sT_{sw}} \tag{3.11}$$

For $V_{in} = 48$ V, $V_{ref} = 14.4$ V, $L = 22$ μH, $r_L = 20$ mΩ, $C = 100$ μF, $r_c = 1$ mΩ and $f_{sw} = 250$ kHz, values $k_p = 10$ and $k_i = 150000$ were chosen (based on peak current mode loop gain plots). For slope compensation $s_e = {}^{s_f}\!/_4$, the analytical models for the output impedance $Z_o(s)$, audio susceptibility $G_{vin}(s)$ and reference tracking $G_{vref}(s)$ transfer functions for peak current mode and sensorless current mode controlled two-phase buck converters are compared. Along with the analytical models, frequency responses obtained from actual switching models are shown in Figs 3.5, 3.6 and 3.7. The MATLAB scripts for simulating the analytical models and generating the frequency responses of the actual switching models are provided in Appendix B. Note that near identical closed loop performance can be obtained from sensorless current mode control compared to peak current mode control without sensing the inductor current.

3.3 Light-load control

The stack converter needs to be efficient over a wide load range. Unlike the DPP converters, where light-load efficiency was the priority, the stack converter has to maintain good efficiencies at both heavy and light loads. We have already chosen a symmetric two-phase converter for the purpose of achieving good efficiency at peak load conditions. Light-load efficiency needs to be improved by implementing a variable frequency discontinuous conduction mode scheme. Instead of the previously adopted scheme of operating only one phase in CCM at intermediate loads and operating one phase in PFM at lighter loads, a simple rotating pulse

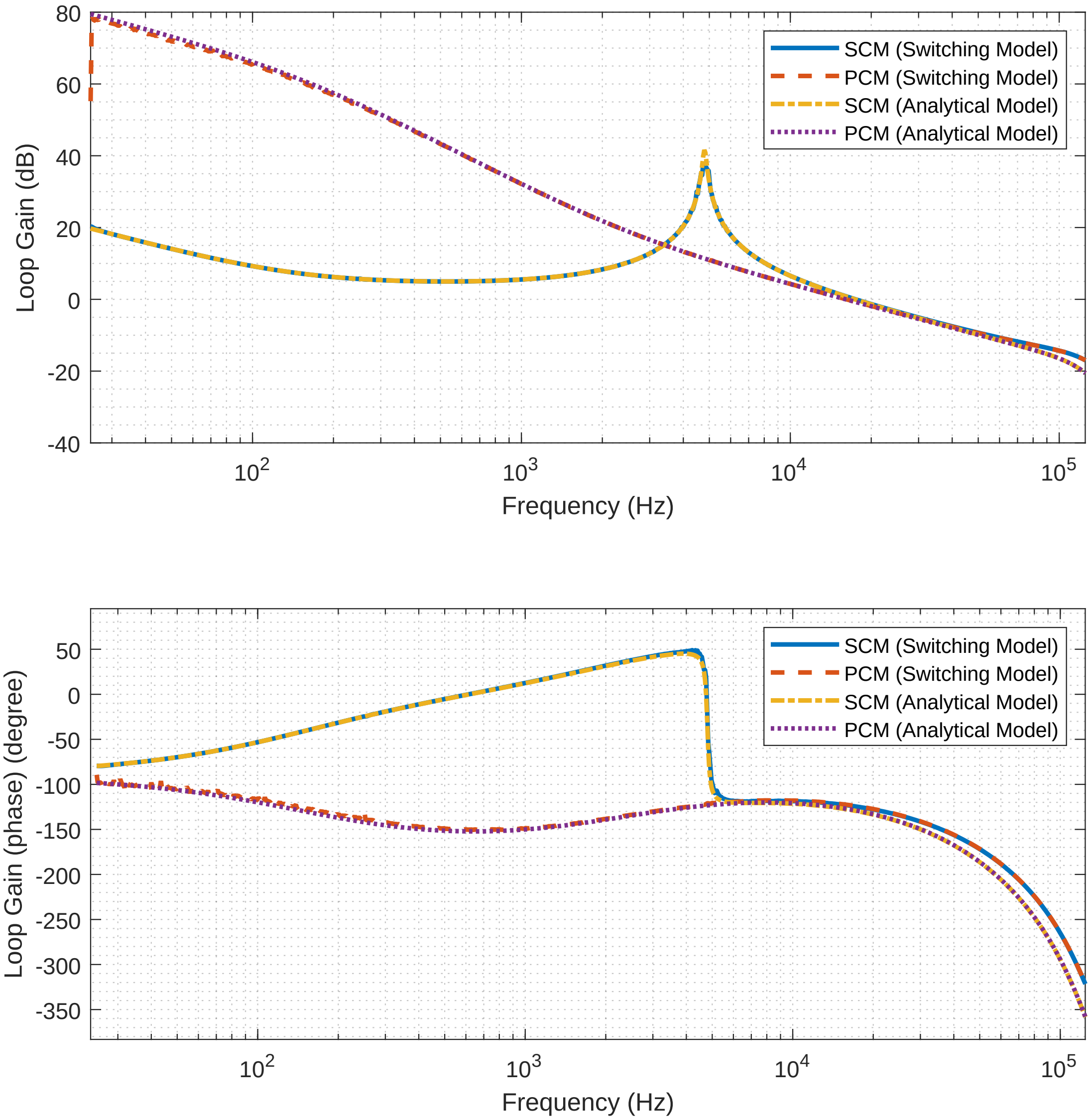


Figure 3.4: Compensated loop gain with a PI voltage loop for peak current mode and sensorless current mode controllers. The slope compensation used is $s_e = {}^{s_f}/_{4}$.

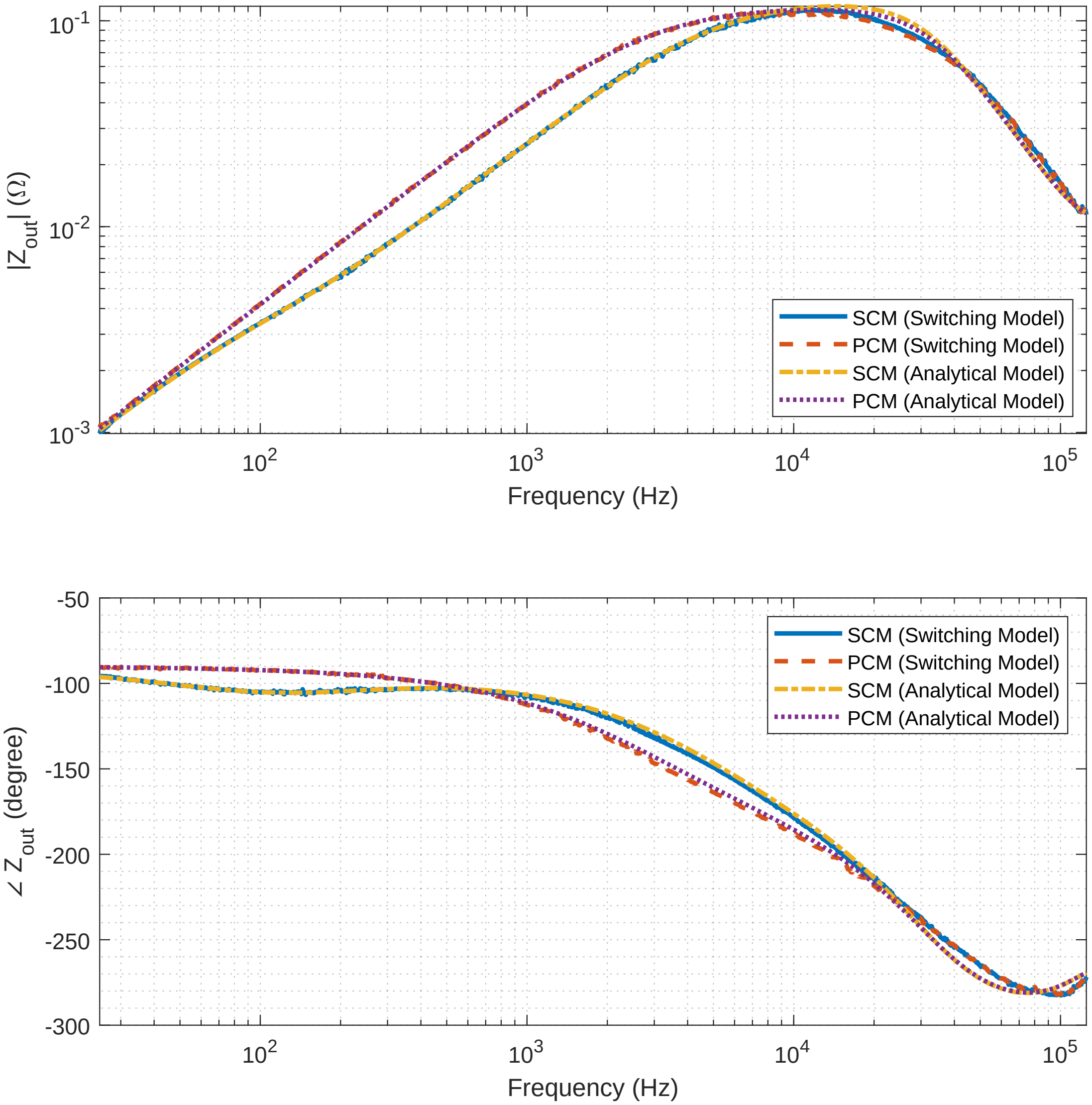


Figure 3.5: Comparison of peak and sensorless current mode controllers in closed loop, analytical model and switching model, output impedance.

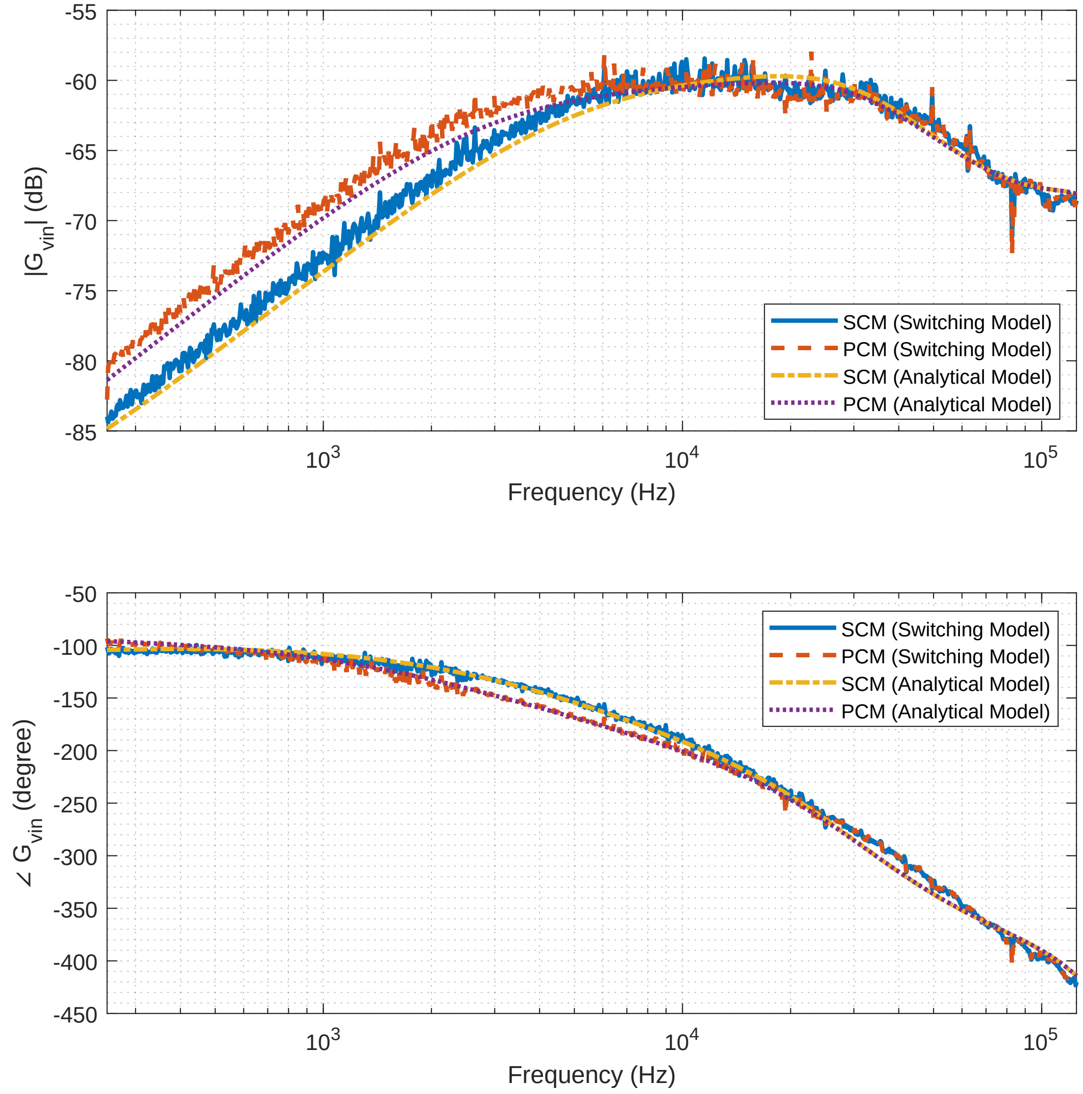


Figure 3.6: Comparison of peak and sensorless current mode controllers in closed loop, analytical model and switching model, audio susceptibility.

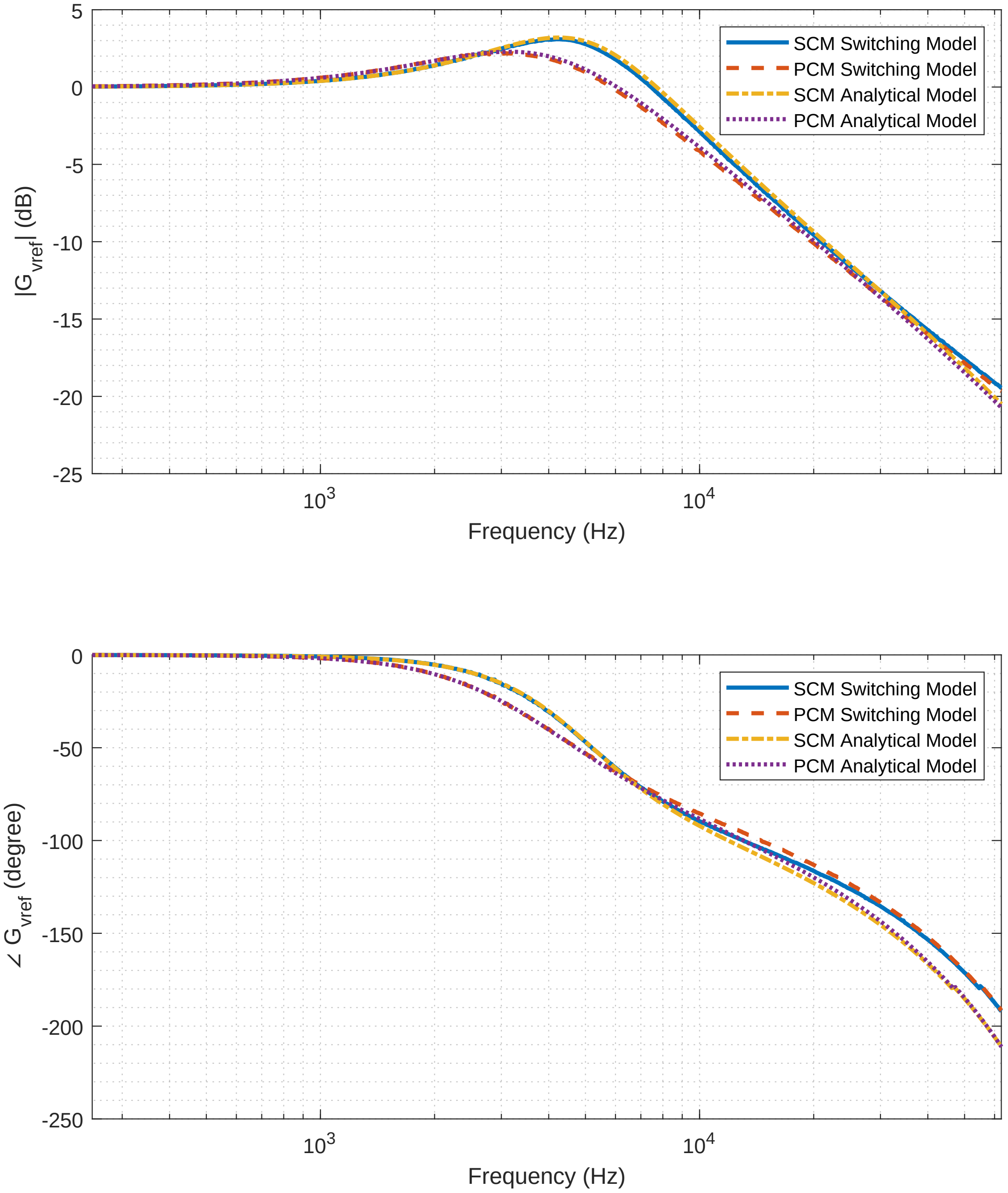


Figure 3.7: Comparison of peak and sensorless current mode controllers in closed loop, analytical model and switching model, reference tracking.

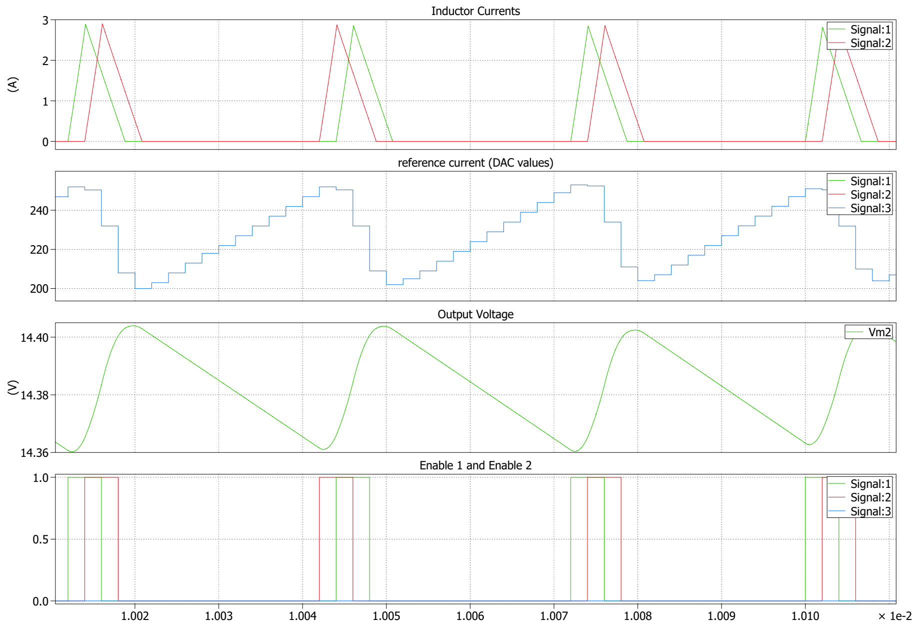


Figure 3.8: Light-load operation at 500 mA load (PLECS simulation).

skipping control is implemented for light loads. If the reference current evaluated after each sampling operation is below a light-load threshold, the set pulse to next phase is suppressed for the next cycle. This helps to reduce phase adding delay during load transients. PLECS simulations for light-load operation and transients from light load to heavy load are shown in Fig 3.8, Fig 3.9 and Fig 3.10.

3.4 Hardware prototype

The outer voltage loop controller implemented is a PI controller similar to the one described before, designed to offer a closed loop bandwidth of 25 kHz. The controller, implemented in a C2000 TMS320F28379 launchpad evaluation board, samples the output voltage error at both the set pulses of the two phases (samples twice in a period). The sample taken during the set pulse of one phase is responsible for setting the inductor current reference point for the other phase. This implementation provides a constant control loop delay of half a switching period which is higher than the 500 ns delay of the interrupt service routine that performs the PI control computations. However, since the write operations to the comparator DAC (for peak current mode) of the TI DSP can be performed when the PWM set or reset actions occur, this rotating DAC update process offers the least overall control

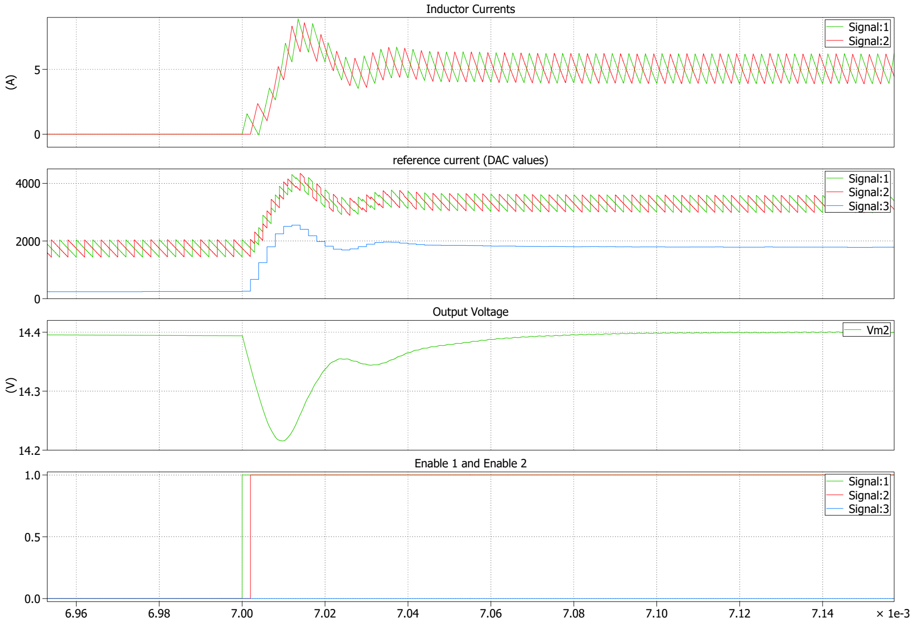


Figure 3.9: Transient from light load to heavy load (PLECS simulation).

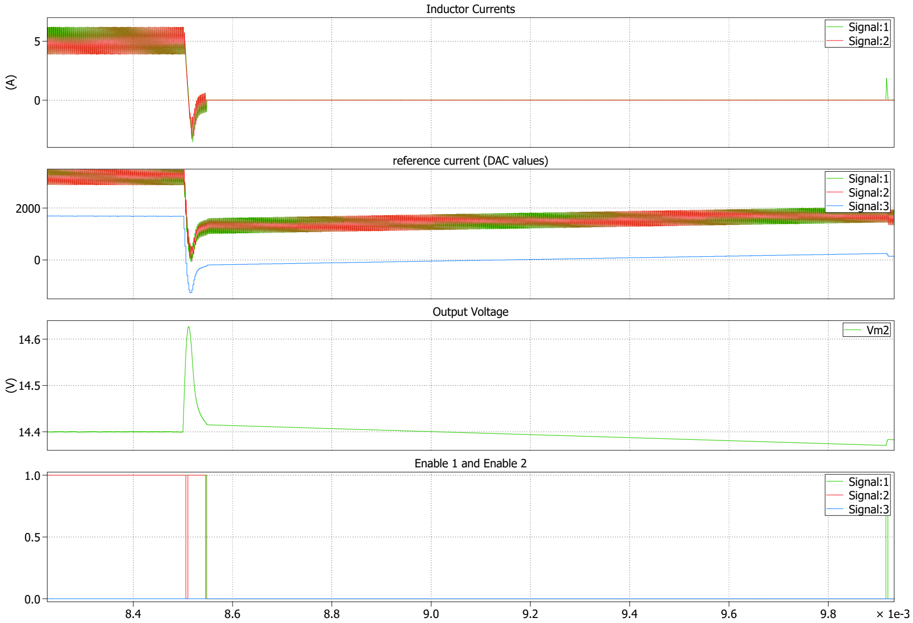


Figure 3.10: Transient from heavy load to light load (PLECS simulation).

Table 3.1: Stack converter components

Component	Part Number	Specifications
Phase 1/2 Switch	BSC340N08NS3	80 V, $r_{DS,on} = 34$ mΩ, $Q_g = 6.8$ nC
Phase 1/2 Inductor	IHLP-6767GZ-11	22 μH, $r_L = 20$ mΩ, $I_{sat} = 9.5$ A
Phase 1/2 Gate Driver	LM5106	1 A source/1 A sink, 12 V supply
C_{out}	GRM21BR61E226ME44K	10×22 μF, $R_{esr} = 3$ mΩ, 25 V, 0805
C_{in}	GRM32EC72A106KE05L	7×10 μF, $R_{esr} = 3$ $m\Omega$, 100 V, 1210

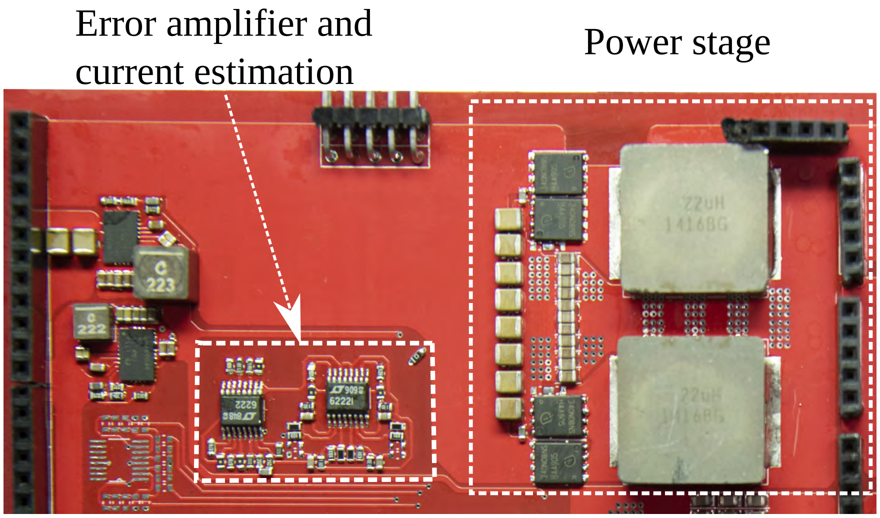
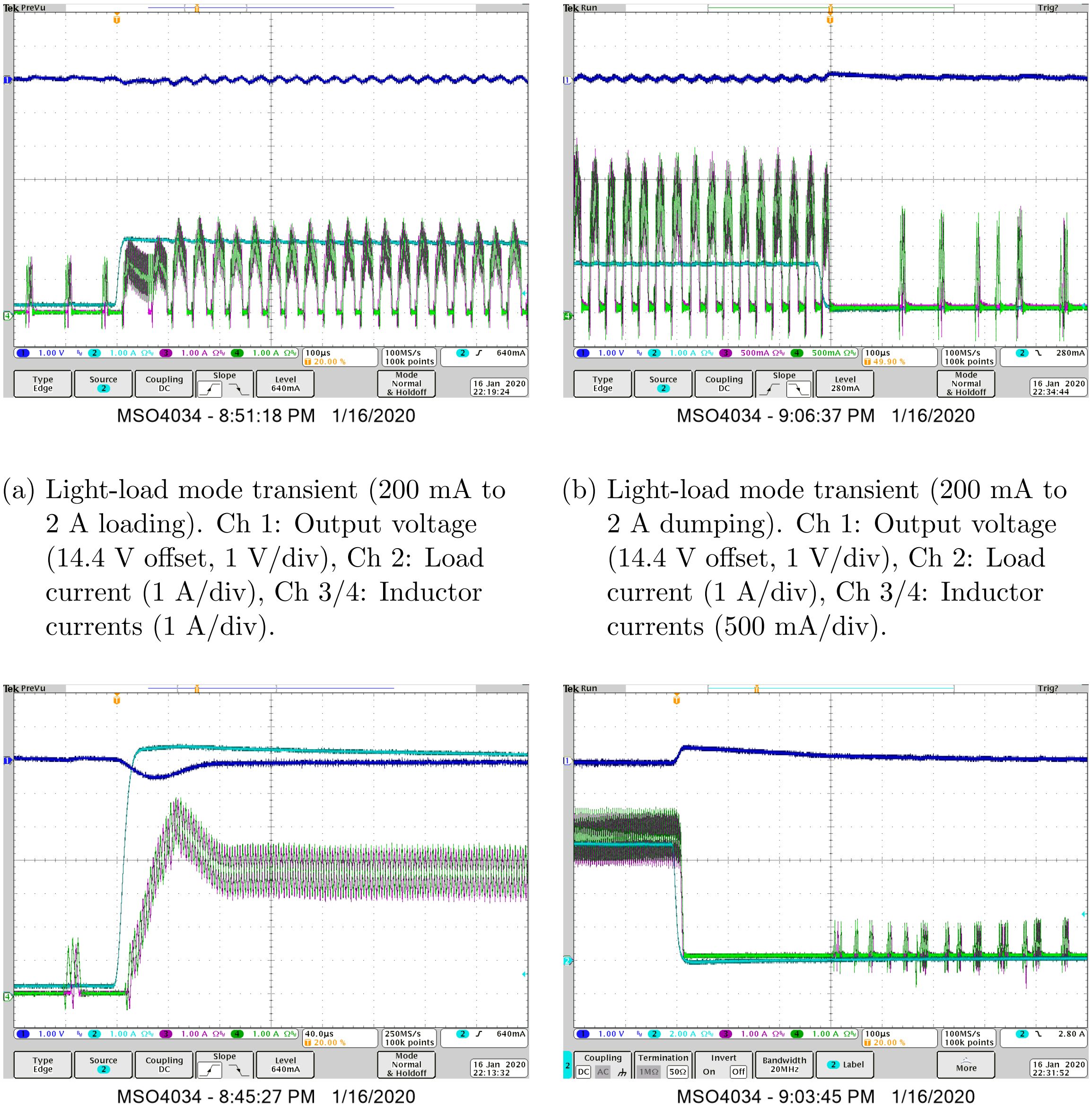


Figure 3.11: Hardware prototype of the stack converter.

loop delay.

The components used for the hardware prototype are listed in Table 3.1. A photograph of the stack converter is provided in Fig 3.11. The output voltage was sensed remotely by means of a difference amplifier, and an error amplifier drives the ADCs of the TMS320F28379D DSP. The inductor current estimator is built as in Fig 3.2. An additional amplification stage provides the estimated inductor current inputs to the comparators of the DSP. Figs 3.12 and 3.13 show transient response of the converter to different load transients. It can be seen that the converter settles within 60 μs and very good current sharing is achieved. Efficiency of the stack converter along with all DPP converters operating at no load is plotted in Fig 3.14. In this case the electronic load is directly connected to the stack voltage rails. The DPP converters process only the power necessary to regulate all intermediate voltage domains at 1.8 V. The input capacitors of the DPP converters provide significant load capacitance to the stack converter and were necessary for stable operation of the stack converter. The measured efficiency shown in Fig 3.14 can be considered an upper limit to achievable system level efficiencies with this setup.



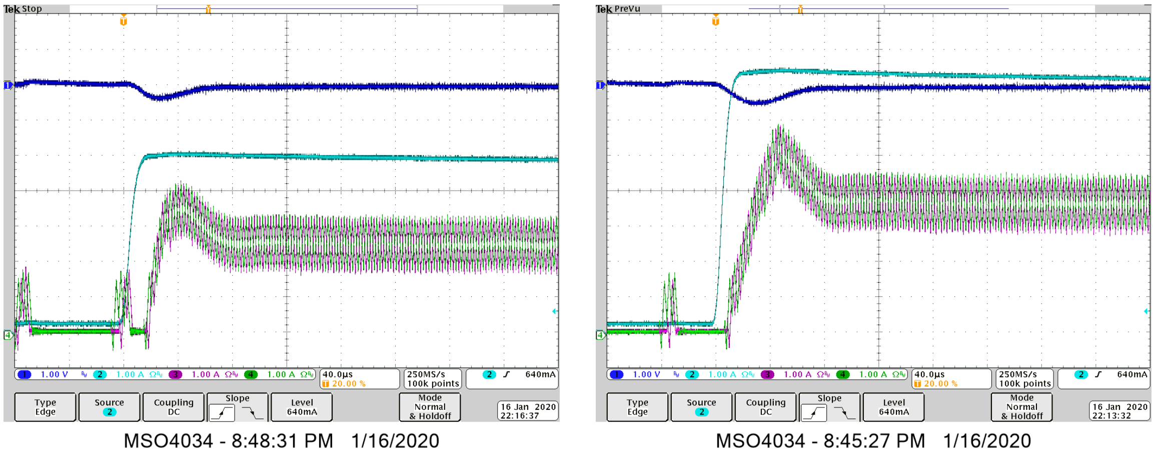
(a) Light-load mode transient (200 mA to 2 A loading). Ch 1: Output voltage (14.4 V offset, 1 V/div), Ch 2: Load current (1 A/div), Ch 3/4: Inductor currents (1 A/div).

(b) Light-load mode transient (200 mA to 2 A dumping). Ch 1: Output voltage (14.4 V offset, 1 V/div), Ch 2: Load current (1 A/div), Ch 3/4: Inductor currents (500 mA/div).

(c) Light-load mode to heavy loading transient (200 mA to 7 A loading). Ch 1: Output voltage (14.4 V offset, 1 V/div), Ch 2: Load current (1 A/div), Ch 3/4: Inductor currents (1 A/div).

(d) Light-load mode to heavy loading transient (200 mA to 7 A dumping). Ch 1: Output voltage (14.4 V offset, 1 V/div), Ch 2: Load current (2 A/div), Ch 3/4: Inductor currents (1 A/div)

Figure 3.12: Stack converter load transients. Channel 1 shows output voltage, Channel 2 shows load current, Channel 3 and 4 show inductor currents of phases 1 and 2 respectively. Horizontal time scale for (a), (b) and (d) = 100 μs/div, for (c) = 40 μs/div.



(a) Load transient (200 mA to 5 A loading). (b) Load transient (200 mA to 7 A loading).

Figure 3.13: Additional stack converter load transients. Channel 1: Output voltage (14.4 V offset, 1 V/div), Channel 2: Load current (1 A/div), Channel 3/4: Inductor currents (1 A/div). Horizontal time scale = 40 μs/div.

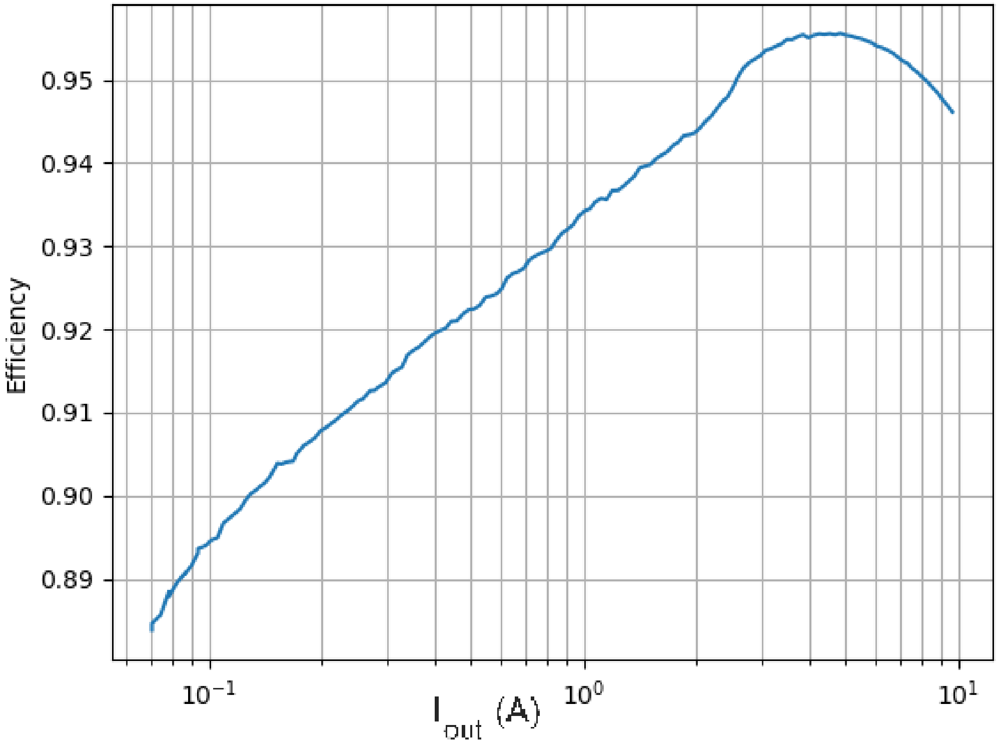


Figure 3.14: Stack converter efficiency plot. The efficiency plot includes all power train losses from the stack converter and the DPP converters regulating individual low voltage domains (under zero mismatch).

CHAPTER 4

VOLTAGE REGULATION OF A SERIES STACK OF LOW VOLTAGE LOADS

4.1 Distributed control in the cascaded/hierarchical DPP topology

The DPP converter control scheme from Chapter 2 has been designed such that interaction between different DPP converters for voltage regulation of the stack is not necessary. In this Chapter we analyze the stability of the stack voltages in the hierarchical DPP architecture (Fig 4.1) under the distributed current mode droop control that is used in the DPP converters.

4.1.1 Large signal model under distributed current mode control

As has been discussed before in Chapter 2, regulation of the voltage difference in case of the buck/boost DPP converters is similar to regulation of the output voltage of a conventional buck converter. So our target is to regulate the differences between the voltages of the domains that the DPP converters are connected to. Instead of directly regulating the eight voltages of the individual domains $[v_1, v_2, v_3, ..., v_8]$, we choose a transformation of variables:

$$\begin{aligned}
v_{d1} &= v_1 - v_2 \\
v_{d2} &= v_1 + v_2 - v_3 - v_4 \\
v_{d3} &= v_3 - v_4 \\
v_{d4} &= v_1 + v_2 + v_3 + v_4 - v_5 - v_6 - v_7 - v_8 \\
v_{d5} &= v_5 - v_6 \\
v_{d6} &= v_5 + v_6 - v_7 - v_8 \\
v_{d7} &= v_7 - v_8 \\
v_s &= v_1 + v_2 + v_3 + v_4 + v_5 + v_6 + v_7 + v_8
\end{aligned} \tag{4.1}$$

For simplifying the formulation of the state variable equations, a similar transformation

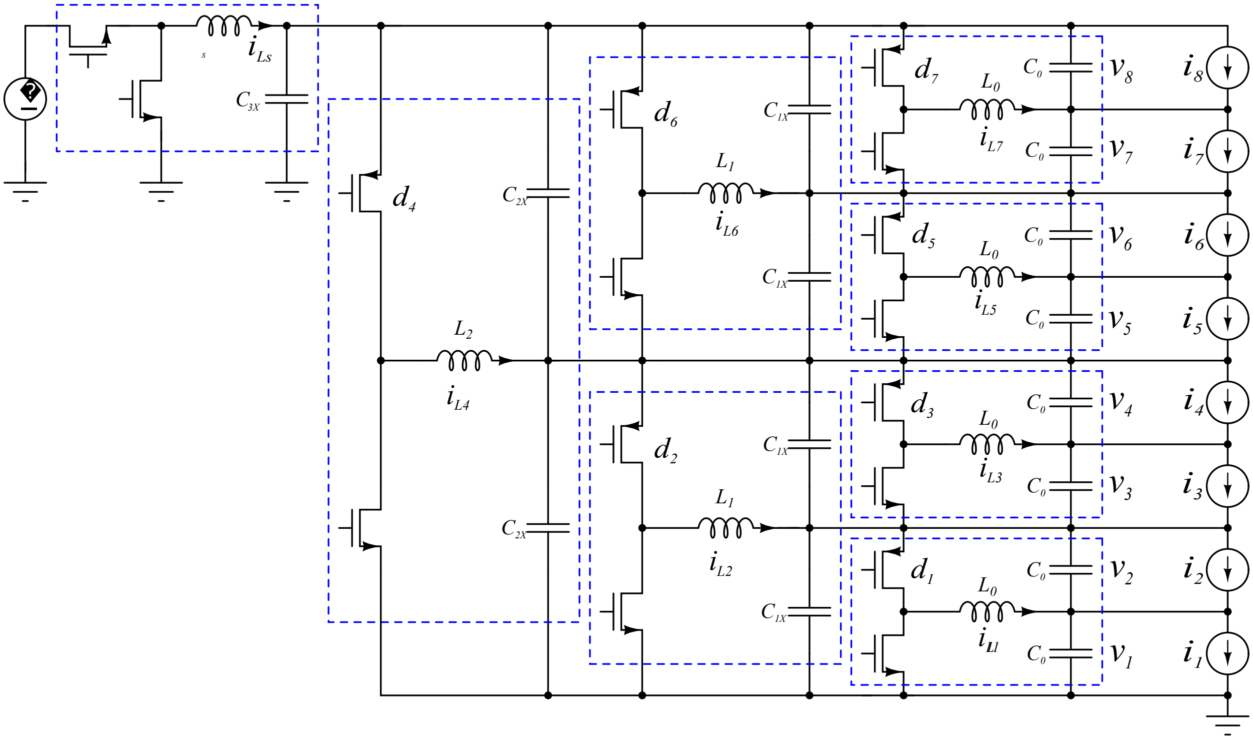


Figure 4.1: The hierarchical DPP topology.

is used for the load currents,

$$\begin{aligned}
i_{d1} &= i_1 - i_2 \\
i_{d2} &= i_1 + i_2 - i_3 - i_4 \\
i_{d3} &= i_3 - i_4 \\
i_{d4} &= i_1 + i_2 + i_3 + i_4 - i_5 - i_6 - i_7 - i_8 \\
i_{d5} &= i_5 - i_6 \\
i_{d6} &= i_5 + i_6 - i_7 - i_8 \\
i_{d7} &= i_7 - i_8 \\
i_s &= i_1 + i_2 + i_3 + i_4 + i_5 + i_6 + i_7 + i_8
\end{aligned} \tag{4.2}$$

Under this transformation, DPP$_k$ is assumed to be responsible for regulating v_{dk} and the stack converter regulates v_s. The eight voltage state variables in the system remain

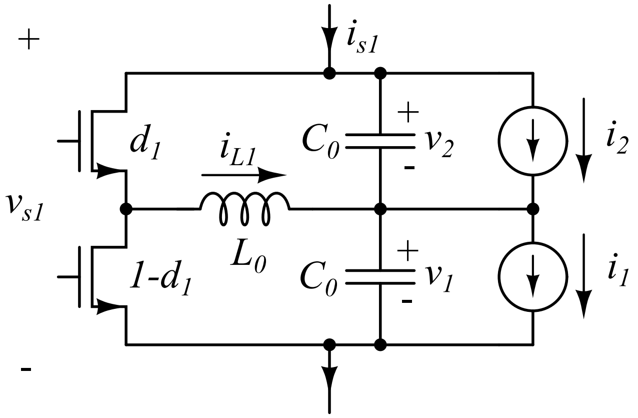


Figure 4.2: A single DPP converter in the outer hierarchical loop

preserved. For simplicity, we also introduce variables:

$$\begin{aligned}
v_{s1} &= v_1 + v_2 = \frac{v_s}{4} + \frac{v_{d4}}{4} + \frac{v_{d2}}{2} \\
v_{s2} &= v_1 + v_2 + v_3 + v_4 = \frac{v_s}{2} + \frac{v_{d4}}{2} \\
v_{s3} &= v_3 + v_4 = \frac{v_s}{4} + \frac{v_{d4}}{4} - \frac{v_{d2}}{2} \\
v_{s4} &= v_1 + v_2 + v_3 + v_4 + v_5 + v_6 + v_7 + v_8 = v_s \\
v_{s5} &= v_5 + v_6 = \frac{v_s}{4} - \frac{v_{d4}}{4} + \frac{v_{d6}}{2} \\
v_{s6} &= v_5 + v_6 + v_7 + v_8 = \frac{v_s}{2} - \frac{v_{d4}}{2} \\
v_{s7} &= v_7 + v_8 = \frac{v_s}{4} - \frac{v_{d4}}{4} - \frac{v_{d6}}{2}
\end{aligned} \tag{4.3}$$

which are the input voltages of the seven DPP converters. These variables can be expressed as a linear combination of v_{dk}'s and v_s.

Let us start analyzing the dynamics with the innermost DPP converters. DPP$_1$ is shown in Fig 4.2. The large signal dynamic equations of the converters in the inner hierarchy are represented by the following equations:

$$L_0 \frac{d\langle i_{Lk}\rangle}{dt} = d_k\left(v_k + v_{k+1}\right) - v_k \tag{4.4}$$

$$C_0 \frac{d}{dt}\left(v_{k+1} - v_k\right) = -\langle i_{Lk}\rangle - \left(i_{k+1} - i_k\right) \tag{4.5}$$

for $k = 1, 3, 5$ and 7. Referring to Fig 4.2, the large signal averaged input currents of these

DPP units can be described by the following equation:

$$\begin{aligned}\langle i_{sk} \rangle &= d_k \langle i_{Lk} \rangle + C_0 \frac{dv_{k+1}}{dt} + i_{k+1} \\ &= -(1-d_k) \langle i_{Lk} \rangle + C_0 \frac{dv_k}{dt} + i_k\end{aligned}$$

for $k = 1, 3, 5$ and 7. With the help of Equation 4.4 we can eliminate the duty ratio d_k from the above equations and arrive at the following equation:

$$v_{sk} \langle i_{sk} \rangle = v_k i_k + v_{k+1} i_{k+1} + \frac{d}{dt} \left[\frac{L_0 \langle i_{Lk} \rangle^2}{2} + \frac{C_0 v_k^2}{2} + \frac{C_0 v_{k+1}^2}{2} \right] \tag{4.6}$$

$$= v_{sk} \left[\frac{i_k + i_{k+1}}{2} \right] + \frac{v_{dk} i_{dk}}{2} + \frac{d}{dt} \left[\frac{L_0 \langle i_{Lk} \rangle^2}{2} + \frac{C_0 v_{sk}^2}{4} + \frac{C_0 v_{dk}^2}{4} \right] \tag{4.7}$$

Elimination of the duty ratio from the equations was necessary since we are using current mode control for controlling the DPP converters and the inductor current can be directly considered a control input instead of another state variable. Equation 4.6 is intuitive, as it claims that the power going into the DPP-load unit is equal to the power dissipated in the loads and the rate of change of energy stored in the inductor and the capacitors. Although the equation refers to the averaged input and inductor currents, it should be noted that 4.6 is valid for instantaneous input and inductor currents as well (irrespective of operation in CCM or DCM). The following can be written without any loss of accuracy:

$$v_{sk} i_{sk} = v_{sk} \left[\frac{i_k + i_{k+1}}{2} \right] + \frac{v_{dk} i_{dk}}{2} + \frac{d}{dt} \left[\frac{L_0 i_{Lk}^2}{2} + \frac{C_0 v_{sk}^2}{4} + \frac{C_0 v_{dk}^2}{4} \right] \tag{4.8}$$

Considering DPP units in the next level of the hierarchy (DPP$_2$ and DPP$_6$ for reference in Fig 4.3) equations similar to Equation 4.6 can be derived.

$$v_{s2} i_{s2} = v_{s1} i_{s1} + v_{s3} i_{s3} + \frac{d}{dt} \left[\frac{L_1 i_{L2}^2}{2} + \frac{C_{1X} v_{s1}^2}{2} + \frac{C_{1X} v_{s3}^2}{2} \right] \tag{4.9}$$

$$v_{s6} i_{s6} = v_{s5} i_{s5} + v_{s7} i_{s7} + \frac{d}{dt} \left[\frac{L_1 i_{L6}^2}{2} + \frac{C_{1X} v_{s5}^2}{2} + \frac{C_{1X} v_{s7}^2}{2} \right] \tag{4.10}$$

With the simplifying assumption that $C_1 = C_{1X} + {}^{C_0}/_2$ and using Equation 4.6 from before,

$$\begin{aligned} v_{s2}i_{s2} =& v_{s2}\left[\frac{i_1+i_2+i_3+i_4}{4}\right] + \frac{v_{d1}i_{d1}}{2} + \frac{v_{d2}i_{d2}}{4} + \frac{v_{d3}i_{d3}}{2} \\ &+ \frac{d}{dt}\left[\frac{C_1v_{s2}^2}{4} + \frac{C_0v_{d1}^2}{4} + \frac{C_1v_{d2}^2}{4} + \frac{C_0v_{d_3}^2}{4} + \frac{L_0i_{L1}^2}{2} + \frac{L_1i_{L2}^2}{2} + \frac{L_0i_{L3}^2}{2}\right] \qquad (4.11) \\ v_{s6}i_{s6} =& v_{s6}\left[\frac{i_5+i_6+i_7+i_8}{4}\right] + \frac{v_{d5}i_{d5}}{2} + \frac{v_{d6}i_{d6}}{4} + \frac{v_{d7}i_{d7}}{2} \\ &+ \frac{d}{dt}\left[\frac{C_1v_{s6}^2}{4} + \frac{C_0v_{d5}^2}{4} + \frac{C_1v_{d6}^2}{4} + \frac{C_0v_{d_7}^2}{4} + \frac{L_0i_{L5}^2}{2} + \frac{L_1i_{L6}^2}{2} + \frac{L_0i_{L7}^2}{2}\right] \qquad (4.12) \end{aligned}$$

Finally considering the last DPP converter in the hierarchy, DPP$_4$ (shown in Fig 4.3), the following equation can be written:

$$v_si_s = v_{s2}i_{s2} + v_{s6}i_{s6} + \frac{d}{dt}\left[\frac{L_2i_{L4}^2}{2} + \frac{C_{2X}v_{s2}^2}{2} + \frac{C_{2X}v_{s6}^2}{2}\right]$$

With the substitution $C_2 = C_{2X} + {}^{C_1}/_2$ and substitutions from the expressions of input power of DPP$_2$ and DPP$_6$:

$$\begin{aligned} v_si_{stack} =& \frac{v_si_s}{8} + \frac{v_{d1}i_{d1}}{2} + \frac{v_{d2}i_{d2}}{4} + \frac{v_{d3}i_{d3}}{2} + \frac{v_{d4}i_{d4}}{8} + \frac{v_{d5}i_{d5}}{2} + \frac{v_{d6}i_{d6}}{4} + \frac{v_{d7}i_{d7}}{2} \\ &+ \frac{d}{dt}\left[\frac{C_2v_s^2}{4} + \frac{C_0v_{d_1}^2}{4} + \frac{C_1v_{d_2}^2}{4} + \frac{C_0v_{d_3}^2}{4} + \frac{C_2v_{d_4}^2}{4} + \frac{C_0v_{d_5}^2}{4} + \frac{C_1v_{d_6}^2}{4} + \frac{C_0v_{d_7}^2}{4}\right. \\ &\left.+ \frac{L_0i_{L1}^2}{2} + \frac{L_1i_{L2}^2}{2} + \frac{L_0i_{L3}^2}{2} + \frac{L_2i_{L4}^2}{2} + \frac{L_0i_{L5}^2}{2} + \frac{L_1i_{L6}^2}{2} + \frac{L_0i_{L7}^2}{2}\right] \qquad (4.13) \end{aligned}$$

With the expressions for input currents of the DPPs formulated, it is now possible to formulate the differential equations governing the state variables. The differential equations

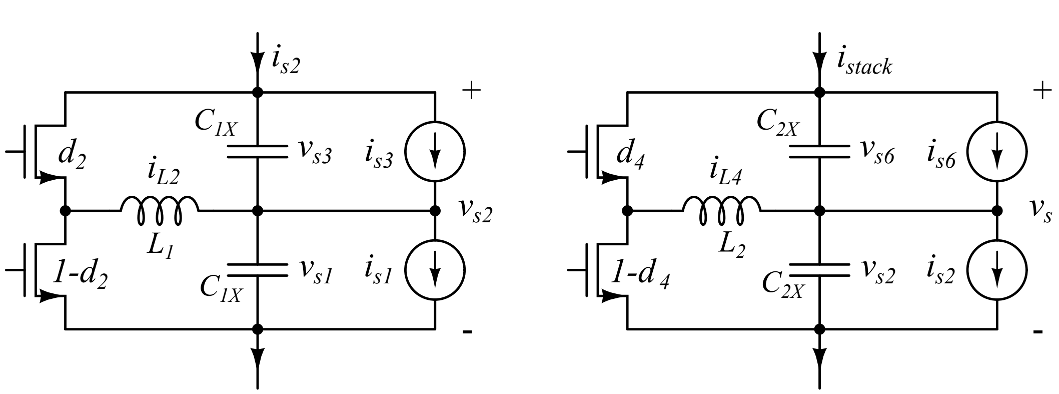


Figure 4.3: DPP$_2$ with DPP$_1$ and DPP$_3$ as loads. DPP$_4$ with DPP$_2$ and DPP$_6$ as loads.

governing the state voltages are:

$$C_0\frac{dv_{d1}}{dt} = i_{L1} - i_{d1} \tag{4.14}$$

$$C_0\frac{dv_{d3}}{dt} = i_{L3} - i_{d3} \tag{4.15}$$

$$C_0\frac{dv_{d5}}{dt} = i_{L5} - i_{d5} \tag{4.16}$$

$$C_0\frac{dv_{d7}}{dt} = i_{L7} - i_{d7} \tag{4.17}$$

$$C_1\frac{dv_{d2}}{dt} = i_{L2} - \frac{i_{d2}}{2} - \frac{v_{d1}i_{d1}}{2v_{s1}} + \frac{v_{d3}i_{d3}}{2v_{s3}} - \frac{1}{v_{s1}}\frac{d}{dt}\left[\frac{C_0v_{d1}^2}{4} + \frac{L_0i_{L1}^2}{2}\right] + \frac{1}{v_{s3}}\frac{d}{dt}\left[\frac{C_0v_{d3}^2}{4} + \frac{L_0i_{L3}^2}{2}\right] \tag{4.18}$$

$$C_1\frac{dv_{d6}}{dt} = i_{L6} - \frac{i_{d6}}{2} - \frac{v_{d5}i_{d5}}{2v_{s5}} + \frac{v_{d7}i_{d7}}{2v_{s7}} - \frac{1}{v_{s5}}\frac{d}{dt}\left[\frac{C_0v_{d5}^2}{4} + \frac{L_0i_{L5}^2}{2}\right] + \frac{1}{v_{s7}}\frac{d}{dt}\left[\frac{C_0v_{d7}^2}{4} + \frac{L_0i_{L7}^2}{2}\right] \tag{4.19}$$

$$\begin{aligned} C_2\frac{dv_{d4}}{dt} =& i_{L4} - \frac{i_{d4}}{4} - \frac{2v_{d1}i_{d1} + v_{d2}i_{d2} + 2v_{d3}i_{d3}}{4v_{s2}} + \frac{2v_{d5}i_{d5} + v_{d6}i_{d6} + 2v_{d7}i_{d7}}{4v_{s6}} \\ &- \frac{1}{v_{s2}}\frac{d}{dt}\left[\left(\frac{C_0v_{d1}^2}{4} + \frac{L_0i_{L1}^2}{2}\right) + \left(\frac{C_1v_{d2}^2}{4} + \frac{L_1i_{L2}^2}{2}\right) + \left(\frac{C_0v_{d3}^2}{4} + \frac{L_0i_{L3}^2}{2}\right)\right] \\ &+ \frac{1}{v_{s6}}\frac{d}{dt}\left[\left(\frac{C_0v_{d5}^2}{4} + \frac{L_0i_{L5}^2}{2}\right) + \left(\frac{C_1v_{d6}^2}{4} + \frac{L_1i_{L6}^2}{2}\right) + \left(\frac{C_0v_{d7}^2}{4} + \frac{L_0i_{L7}^2}{2}\right)\right] \end{aligned} \tag{4.20}$$

$$\begin{aligned} C_3\frac{dv_s}{dt} =& i_{Ls} - \frac{i_s}{8} - \frac{4v_{d1}i_{d1} + 2v_{d2}i_{d2} + 4v_{d3}i_{d3} + v_{d4}i_{d4} + 4v_{d5}i_{d5} + 2v_{d6}i_{d6} + 4v_{d7}i_{d7}}{8v_s} \\ &- \frac{1}{v_s}\frac{d}{dt}\left[\left(\frac{C_0v_{d1}^2}{4} + \frac{L_0i_{L1}^2}{2}\right) + \left(\frac{C_1v_{d2}^2}{4} + \frac{L_1i_{L2}^2}{2}\right) + \left(\frac{C_0v_{d3}^2}{4} + \frac{L_0i_{L3}^2}{2}\right) + \left(\frac{C_2v_{d4}^2}{4} + \frac{L_2i_{L4}^2}{2}\right)\right. \\ &\left. + \left(\frac{C_0v_{d5}^2}{4} + \frac{L_0i_{L5}^2}{2}\right) + \left(\frac{C_1v_{d6}^2}{4} + \frac{L_1i_{L6}^2}{2}\right) + \left(\frac{C_0v_{d7}^2}{4} + \frac{L_0i_{L7}^2}{2}\right)\right] \end{aligned} \tag{4.21}$$

where $C_3 = C_{3X} + \frac{C_2}{2}$. Equations 4.14 through 4.21 are valid even when the instantaneous inductor currents i_{Lk} are replaced with their averaged values $\langle i_{Lk}\rangle$. As discussed in Chapter 2, under current hysteretic control, a reference current is generated based on the output voltage error of the converter. Our target here is equalization of the voltages of the two domains to which the respective DPPs are connected. For that purpose the following droop control is proposed for the balancing and stack regulators:

$$\begin{aligned} &i_{L1,ref} = -g_0v_{d1}, \quad i_{L3,ref} = -g_0v_{d3}, \quad i_{L5,ref} = -g_0v_{d5}, \quad i_{L7,ref} = -g_0v_{d7}, \\ &i_{L2,ref} = -g_1v_{d2}, \quad i_{L6,ref} = -g_1v_{d6}, \quad i_{L4,ref} = -g_2v_{d4}, \quad i_{Ls,ref} = g_s\left(v_{ref} - v_s\right) \end{aligned}$$

It is a common assumption that under current hysteretic control, the average inductor current $\langle i_L\rangle = i_{L,ref}$, and is a valid approximation even in a large signal sense as long as the slew rate of the reference current does not exceed the maximum slew rate of the inductor current. This assumption loses its validity under discontinuous conduction mode; however, in some manner of droop control, $\langle i_{L1}\rangle = g\left(v_2 - v_1\right)$ still remains valid (where g and g_0 might not be the same gains). For simplicity, we assume that the droop control gains under CCM and DCM operation remains the same. With this assumption, we are essentially converting the inductor dynamics from Equations 4.4 to algebraic equations.

Furthermore, for simplicity, we assume that the dynamics of the stack converter are also similar. Even though the assumption $\langle i_L \rangle = i_{L,ref}$ has been proven to be inadequate for high performance peak current mode control loops (loses accuracy at high frequencies), we can still derive some insights into the stability of the stack by using an approximate control equation: $i_{Ls} = g_s \left(v_{ref} - v_s\right)$. The resulting dynamic equations of the differential and the stack voltages are given as

$$C_0 \frac{dv_{d1}}{dt} = - g_0 v_{d1} - i_{d1} \tag{4.22}$$

$$C_0 \frac{dv_{d3}}{dt} = - g_0 v_{d3} - i_{d3} \tag{4.23}$$

$$C_0 \frac{dv_{d5}}{dt} = - g_0 v_{d5} - i_{d5} \tag{4.24}$$

$$C_0 \frac{dv_{d7}}{dt} = - g_0 v_{d7} - i_{d7} \tag{4.25}$$

$$C_1 \frac{dv_{d2}}{dt} = - g_1 v_{d2} - \frac{i_{d2}}{2} - \frac{v_{d1} i_{d1}}{2v_{s1}} + \frac{v_{d3} i_{d3}}{2v_{s3}} - \frac{1}{v_{s1}} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d1}^2}{4} \right] + \frac{1}{v_{s3}} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d3}^2}{4} \right] \tag{4.26}$$

$$C_1 \frac{dv_{d6}}{dt} = - g_1 v_{d6} - \frac{i_{d6}}{2} - \frac{v_{d5} i_{d5}}{2v_{s5}} + \frac{v_{d7} i_{d7}}{2v_{s7}} - \frac{1}{v_{s5}} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d5}^2}{4} \right] + \frac{1}{v_{s7}} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d7}^2}{4} \right] \tag{4.27}$$

$$\begin{aligned} C_2 \frac{dv_{d4}}{dt} =& - g_2 v_{d4} - \frac{i_{d4}}{4} - \frac{2v_{d1} i_{d1} + v_{d2} i_{d2} + 2v_{d3} i_{d3}}{4v_{s2}} + \frac{2v_{d5} i_{d5} + v_{d6} i_{d6} + 2v_{d7} i_{d7}}{4v_{s6}} \\ & - \frac{1}{v_{s2}} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d1}^2}{4} + \frac{C_1 k_1 v_{d2}^2}{4} + \frac{C_0 k_0 v_{d3}^2}{4} \right] + \frac{1}{v_{s6}} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d5}^2}{4} + \frac{C_1 k_1 v_{d6}^2}{4} + \frac{C_0 k_0 v_{d7}^2}{4} \right] \end{aligned} \tag{4.28}$$

$$\begin{aligned} C_3 \frac{dv_s}{dt} =& g_s \left(v_{ref} - v_s\right) - \frac{i_s}{8} - \frac{4v_{d1} i_{d1} + 2v_{d2} i_{d2} + 4v_{d3} i_{d3} + v_{d4} i_{d4} + 4v_{d5} i_{d5} + 2v_{d6} i_{d6} + 4v_{d7} i_{d7}}{8v_s} \\ & - \frac{1}{v_s} \frac{d}{dt} \left[\frac{C_0 k_0 v_{d1}^2}{4} + \frac{C_1 k_1 v_{d2}^2}{4} + \frac{C_0 k_0 v_{d3}^2}{4} + \frac{C_2 k_2 v_{d4}^2}{4} + \frac{C_0 k_0 v_{d5}^2}{4} + \frac{C_1 k_1 v_{d6}^2}{4} + \frac{C_0 k_0 v_{d7}^2}{4} \right] \end{aligned} \tag{4.29}$$

where the factors k_0, k_1 and k_2 are given as

$$k_0 = 1 + \frac{2L_0 g_0^2}{C_0}, \quad k_1 = 1 + \frac{2L_1 g_1^2}{C_1}, \quad k_2 = 1 + \frac{2L_2 g_2^2}{C_2}$$

4.1.2 Stability under distributed droop control - small signal

From the nonlinear differential equations it can be observed that, v_{d1}, v_{d3}, v_{d5} and v_{d7} are inherently bounded and stable due to the control. Assuming v_{s1}, v_{s3}, v_{s5} and v_{s7} are stable as well (do not converge to zero), the disturbance terms in Equations 4.26 and 4.27 remain bounded as well. Due to the control, the differential Equations 4.26 and 4.27 are also bounded input stable, ensuring stability of v_{d2} and v_{d6} (which in turn validates the assumption that v_{s1}, v_{s3}, v_{s5} and v_{s7} are bounded and don't converge to zero). Similarly, the stability of v_{d4} can be intuitively established under the assumption that the stack converter (v_s) is stable.

To formally establish stability with droop control, a small signal analysis is performed.

Firstly we ignore perturbations in the load currents (assume they are constant current type loads without any perturbations or voltage dependence). This leads to: $i_{dk} = I_{Dk}$, for $k = 1, ..., 7$ and $i_s = I_s$. Then we separate the DC and perturbation terms of the state voltages: $v_{dk} = V_{Dk} + v_{\hat{dk}}$ for $k = 1, ..., 7$ and $v_s = V_s + \hat{v_s}$. Corresponding DC and perturbation term separations are also done for the input voltages $v_{sk} = V_{Sk} + v_{\hat{sk}}$. The perturbation terms v_{sk} can then be represented in terms of the state voltages according to equations 4.2. Proceeding with the linearization the following state equations are obtained:

$$
\begin{align}
C_0 \frac{dv_{\hat{d1}}}{dt} &= - g_0 v_{\hat{d1}} = g_{11} v_{\hat{d1}} \tag{4.30} \\
C_0 \frac{dv_{\hat{d3}}}{dt} &= - g_0 v_{\hat{d3}} = g_{33} v_{\hat{d3}} \tag{4.31} \\
C_0 \frac{dv_{\hat{d5}}}{dt} &= - g_0 v_{\hat{d5}} = g_{55} v_{\hat{d5}} \tag{4.32} \\
C_0 \frac{dv_{\hat{d7}}}{dt} &= - g_0 v_{\hat{d7}} = g_{77} v_{\hat{d7}} \tag{4.33} \\
C_1 \frac{dv_{\hat{d2}}}{dt} &= - \left[\frac{g_{11} V_{D1}}{2V_{S1}} (1 + k_0) \right] v_{\hat{d1}} - \left[g_1 - \frac{g_{11} V_{D1}^2}{4V_{S1}^2} - \frac{g_{33} V_{D3}^2}{4V_{S3}^2} \right] v_{\hat{d2}} + \left[\frac{g_{11} V_{D3}}{2V_{S3}} (1 + k_0) \right] v_{\hat{d3}} \nonumber \\
&\quad + \left[\frac{g_{11} V_{D1}^2}{8V_{S1}^2} - \frac{g_{33} V_{D3}^2}{8V_{S3}^2} \right] v_{\hat{d4}} + \left[\frac{g_{11} V_{D1}^2}{8V_{S1}^2} - \frac{g_{33} V_{D3}^2}{8V_{S3}^2} \right] \hat{v_s} \tag{4.34} \\
&= g_{21} v_{\hat{d1}} + g_{22} v_{\hat{d2}} + g_{23} v_{\hat{d3}} + g_{24} v_{\hat{d4}} + g_{28} \hat{v_s} \tag{4.35} \\
C_1 \frac{dv_{\hat{d6}}}{dt} &= - \left[\frac{g_{55} V_{D5}^2}{8V_{S5}^2} - \frac{g_{77} V_{D7}^2}{8V_{S7}^2} \right] v_{\hat{d4}} - \left[\frac{g_{55} V_{D5}}{2V_{S5}} (1 + k_0) \right] v_{\hat{d5}} - \left[g_1 - \frac{g_{55} V_{D5}^2}{4V_{S5}^2} - \frac{g_{77} V_{D7}^2}{4V_{S7}^2} \right] v_{\hat{d6}} \nonumber \\
&\quad + \left[\frac{g_{77} V_{D7}}{2V_{S7}} (1 + k_0) \right] v_{\hat{d7}} + \left[\frac{g_{55} V_{D5}^2}{8V_{S5}^2} - \frac{g_{77} V_{D7}^2}{8V_{S7}^2} \right] \hat{v_s} \tag{4.36} \\
&= g_{64} v_{\hat{d4}} + g_{65} v_{\hat{d5}} + g_{66} v_{\hat{d6}} + g_{67} v_{\hat{d7}} + g_{68} \hat{v_s} \tag{4.37} \\
C_2 \frac{dv_{\hat{d4}}}{dt} &= - \left[\frac{I_{D1} + k_0 g_{11} V_{D1} + k_1 g_{21} V_{D2}}{2V_{S2}} \right] v_{\hat{d1}} - \left[\frac{I_{D2} + 2k_1 g_{22} V_{D2}}{4V_{S2}} \right] v_{\hat{d2}} \nonumber \\
&\quad - \left[\frac{I_{D3} + k_0 g_{33} V_{D3} + k_1 g_{23} V_{D2}}{2V_{S2}} \right] v_{\hat{d3}} - \left[g_2 + \frac{P_{D1}}{4V_{S2}^2} + \frac{P_{D2}}{4V_{S6}^2} + \frac{k_1 g_{24} V_{D2}}{2V_{S2}} - \frac{k_1 g_{64} V_{D6}}{2V_{S6}} \right] v_{\hat{d4}} \nonumber \\
&\quad + \left[\frac{I_{D5} + k_0 g_{55} V_{D5} + k_1 g_{65} V_{D6}}{2V_{S6}} \right] v_{\hat{d5}} + \left[\frac{I_{D6} + 2k_1 g_{66} V_{D6}}{2V_{S6}} \right] v_{\hat{d6}} \nonumber \\
&\quad + \left[\frac{I_{D7} + k_0 g_{77} V_{D7} + k_1 g_{67} V_{D6}}{2V_{S6}} \right] v_{\hat{d7}} + \left[\frac{P_{D1}}{4V_{S2}^2} - \frac{P_{D2}}{4V_{S6}^2} - \frac{k_1 g_{28} V_{D2}}{2V_{S2}} + \frac{k_1 g_{68} V_{D6}}{2V_{S6}} \right] \hat{v_s} \tag{4.38} \\
&= g_{41} v_{\hat{d1}} + g_{42} v_{\hat{d2}} + g_{43} v_{\hat{d3}} + g_{44} v_{\hat{d4}} + g_{45} v_{\hat{d5}} + g_{46} v_{\hat{d6}} + g_{47} v_{\hat{d7}} + g_{48} \hat{v_s} \tag{4.39} \\
C_3 \frac{d\hat{v_s}}{dt} &= - \left[\frac{I_{D1} + k_0 g_{11} V_{D1} + k_1 g_{21} V_{D2} + k_2 g_{41} V_{D4}}{2V_s} \right] v_{\hat{d1}} - \left[\frac{I_{D2} + 2k_1 g_{22} V_{D2} + 2k_2 g_{42} V_{D4}}{4V_s} \right] v_{\hat{d2}} \nonumber \\
&\quad - \left[\frac{I_{D3} + k_1 g_{23} V_{D2} + k_0 g_{33} V_{D3} + k_2 g_{43} V_{D4}}{2V_s} \right] v_{\hat{d3}} - \left[\frac{I_{D4} + 4k_1 g_{24} V_{D2} + 4k_2 g_{44} V_{D4} + 4k_1 g_{64} V_{D6}}{8V_s} \right] v_{\hat{d4}} \nonumber \\
&\quad - \left[\frac{I_{D5} + k_2 g_{45} V_{D4} + k_0 g_{55} V_{D5} + k_1 g_{65} V_{D6}}{2V_s} \right] v_{\hat{d5}} - \left[\frac{I_{D6} + 2k_2 g_{46} V_{D4} + 2k_1 g_{66} V_{D6}}{4V_s} \right] v_{\hat{d6}} \nonumber \\
&\quad - \left[\frac{I_{D7} + k_2 g_{47} V_{D4} + k_1 g_{67} V_{D6} + k_0 g_{77} V_{D7}}{2V_s} \right] v_{\hat{d7}} - \left[g_s - \frac{P_D}{8V_s^2} + \frac{k_1 g_{28} V_{D2} + k_2 g_{48} V_{D4} + k_1 g_{68} V_{D6}}{2V_s} \right] \hat{v_s} \tag{4.40} \\
&= g_{81} v_{\hat{d1}} + g_{82} v_{\hat{d2}} + g_{83} v_{\hat{d3}} + g_{84} v_{\hat{d4}} + g_{85} v_{\hat{d5}} + g_{86} v_{\hat{d6}} + g_{87} v_{\hat{d7}} + g_{88} \hat{v_s} \tag{4.41}
\end{align}
$$

where the differential power terms P_{D1}, P_{D2} and P_D are

$$P_{D1} = 2V_{D1}I_{D1} + V_{D2}I_{D2} + 2V_{D3}I_{D3} \tag{4.42}$$

$$P_{D2} = 2V_{D5}I_{D5} + V_{D6}I_{D6} + 2V_{D7}I_{D7} \tag{4.43}$$

$$P_D = 4V_{D1}I_{D1} + 2V_{D2}I_{D2} + 4V_{D3}I_{D3} + V_{D4}I_{D4} + 4V_{D5}I_{D5} + 2V_{D6}I_{D6} + 4V_{D7}I_{D7} \tag{4.44}$$

The linearized equations can be represented in the form of a state transition matrix (without inputs, as we have ignored perturbations in load currents),

$$\begin{bmatrix} C_0\frac{d\hat{v_{d1}}}{dt} \\ C_1\frac{d\hat{v_{d2}}}{dt} \\ C_0\frac{d\hat{v_{d3}}}{dt} \\ C_2\frac{d\hat{v_{d4}}}{dt} \\ C_0\frac{d\hat{v_{d5}}}{dt} \\ C_1\frac{d\hat{v_{d6}}}{dt} \\ C_0\frac{d\hat{v_{d7}}}{dt} \\ C_3\frac{d\hat{v_s}}{dt} \end{bmatrix} = \begin{bmatrix} g_{11} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ g_{21} & g_{22} & g_{23} & g_{24} & 0 & 0 & 0 & g_{28} \\ 0 & g_{33} & 0 & 0 & 0 & 0 & 0 & 0 \\ g_{41} & g_{42} & g_{43} & g_{44} & g_{45} & g_{46} & g_{47} & g_{48} \\ 0 & 0 & 0 & 0 & g_{55} & 0 & 0 & 0 \\ 0 & 0 & 0 & g_{64} & g_{65} & g_{66} & g_{67} & g_{68} \\ 0 & 0 & 0 & 0 & 0 & 0 & g_{77} & 0 \\ g_{81} & g_{82} & g_{83} & g_{84} & g_{85} & g_{86} & g_{87} & g_{88} \end{bmatrix} \begin{bmatrix} \hat{v_{d1}} \\ \hat{v_{d2}} \\ \hat{v_{d3}} \\ \hat{v_{d4}} \\ \hat{v_{d5}} \\ \hat{v_{d6}} \\ \hat{v_{d7}} \\ \hat{v_s} \end{bmatrix} \tag{4.45}$$

The state matrix of this linearized system has all negative diagonal components of the form $-g_{xx} + \sum g\frac{V_D^n}{V_S^n}$ and the non-zero off diagonal components are all of the form $\sum g\frac{V_D^n}{V_S^n}$. By design, under any steady state, the differential voltages (V_D's) are expected to be much lower than the input voltages (V_S's) since our goal is voltage equalization. So it is relatively easy to construct the gains g_0, g_1, g_2 and g_s so that the state matrix is diagonal dominant, with all negative diagonal components. The eigenvalues of such a matrix are always negative and leads to a stable system.

At this point, it should be noted that the system can be stabilized more easily (with lower control gains) if the loads are resistive. Resistive loads would add an additional stabilizing component to the diagonal components of the state transition matrix. For example, with resistances r_k connected at each voltage domain v_k, Equation 4.22 can be denoted as,

$$\begin{aligned} C_0\frac{dv_{d1}}{dt} &= -\, g_0 v_{d1} - i_{d1} = -g_0 v_{d1} - \frac{v_1}{r_1} + \frac{v_2}{r_2} \\ &= -\left(g_0 + \frac{1}{2r_1} + \frac{1}{2r_1}\right) v_{d1} - \left(\frac{1}{2r_1} - \frac{1}{2r_2}\right)\left(\frac{v_s}{4} + \frac{v_{d4}}{4} + \frac{v_{d2}}{2}\right) \end{aligned} \tag{4.46}$$

However, the complexity in formulating the state transition matrix increases as the number of off-diagonal components increases in state transition matrix.

4.2 Stacking of the DPP converters - Hardware

In order to find a low inductance layout for the DPP converters which have been designed to operate in a modular fashion, the inner DPP converters, DPP$_1$, DPP$_3$, DPP$_5$ and DPP$_7$ have been laid out on one PCB shown in Fig 4.4. DPP$_2$ and DPP$_6$ are laid out on a second board. A third board contains layouts of the stack converter and DPP$_4$. Converters for auxiliary power (48 V - 12 V for stack converter gate drive, and 12 V - 5 V for control), voltage and current sensing circuits for the loads are also placed on the same board as the stack converter. Figs 4.4, 4.5 and 4.6 show the three populated PCBs.

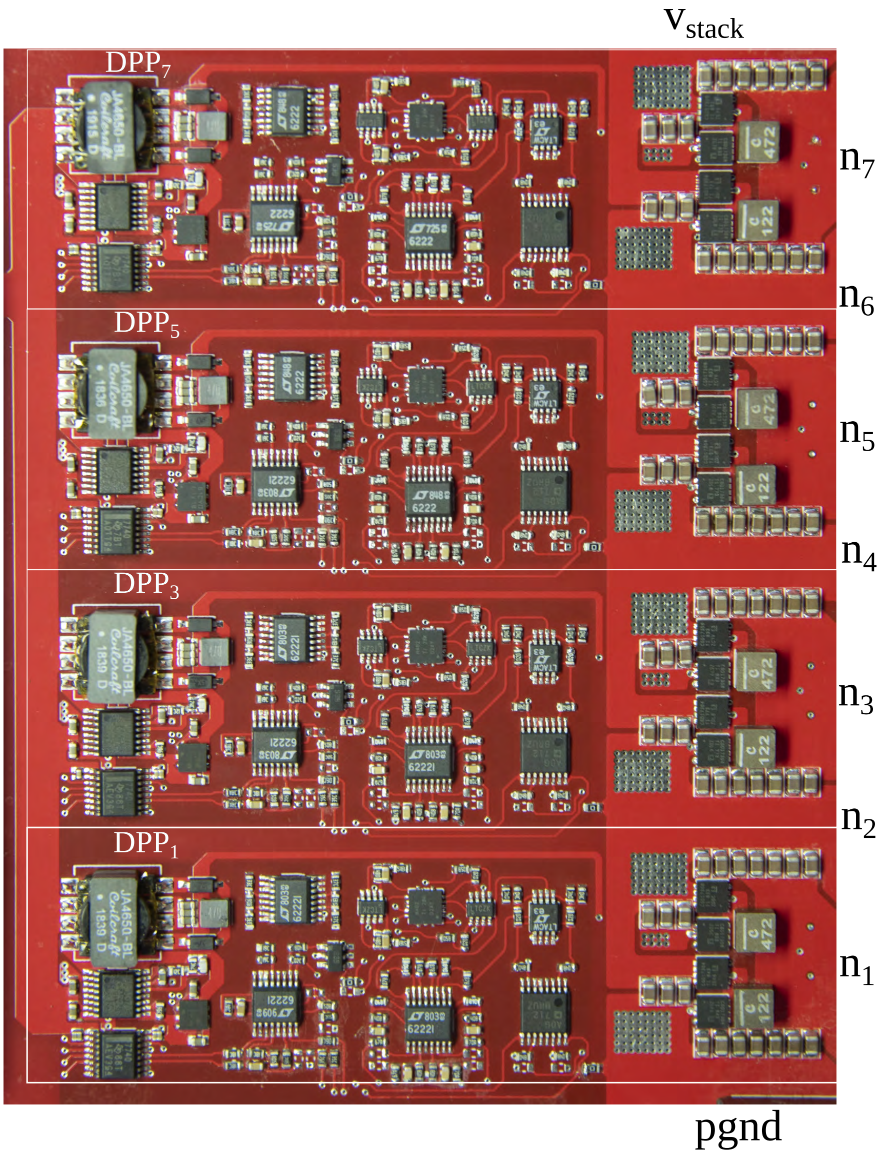


Figure 4.4: PCB with inner DPP converters.

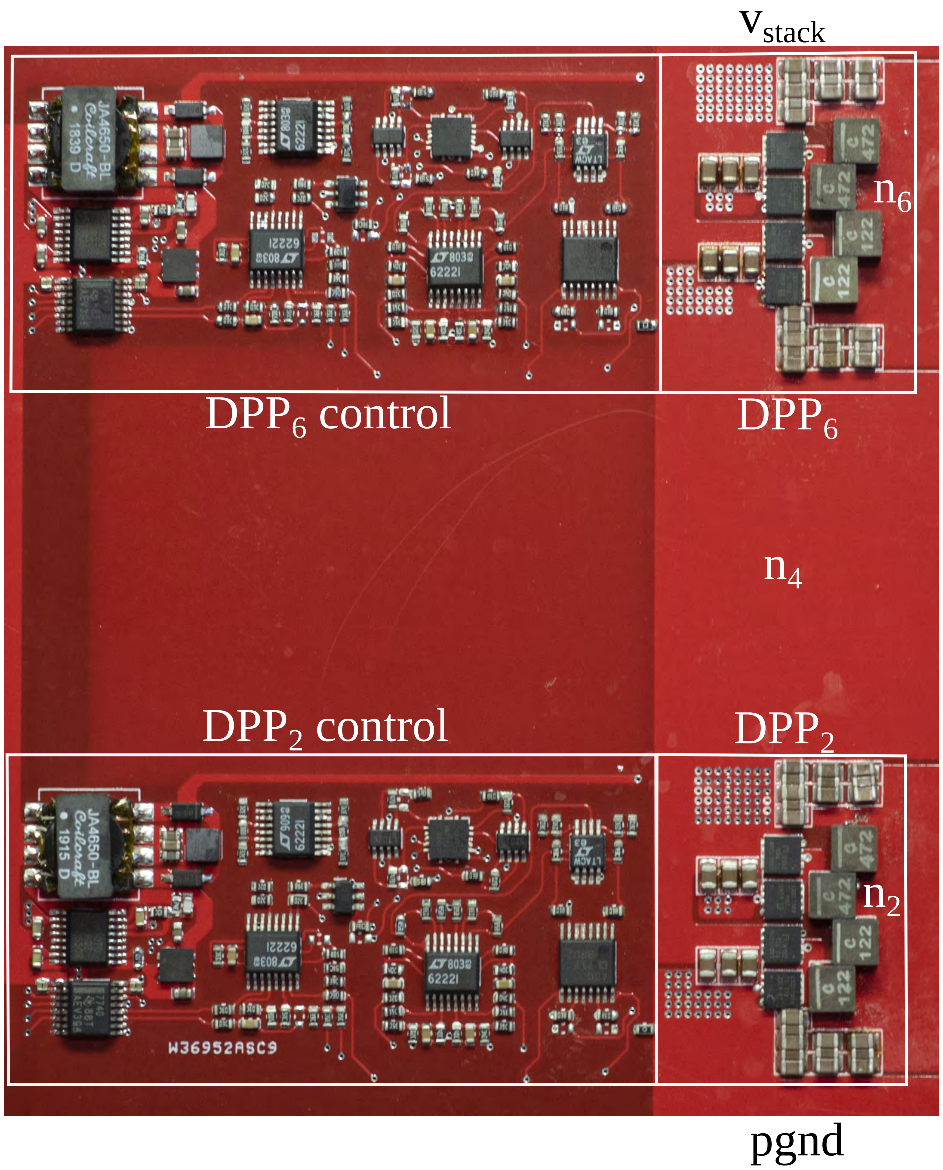


Figure 4.5: PCB with DPP converters in the middle of the hierarchy.

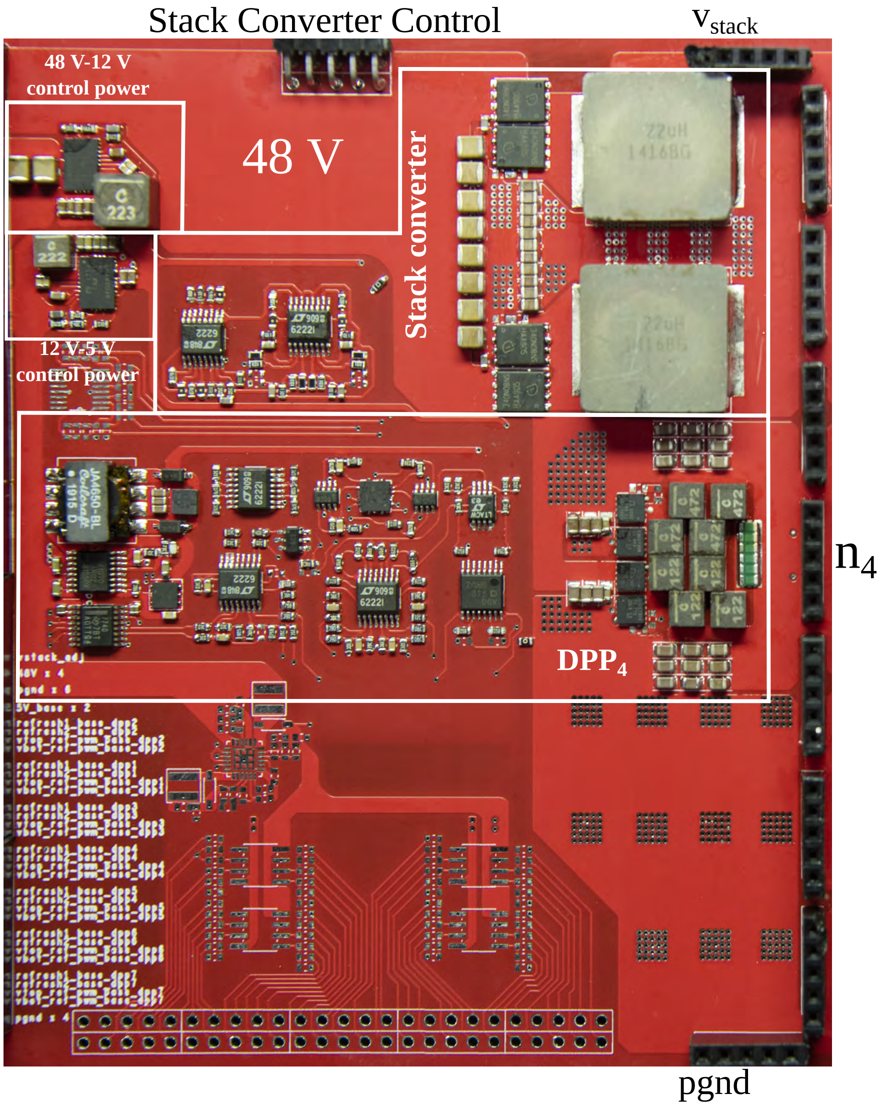


Figure 4.6: PCB with stack converter and outer DPP converter.

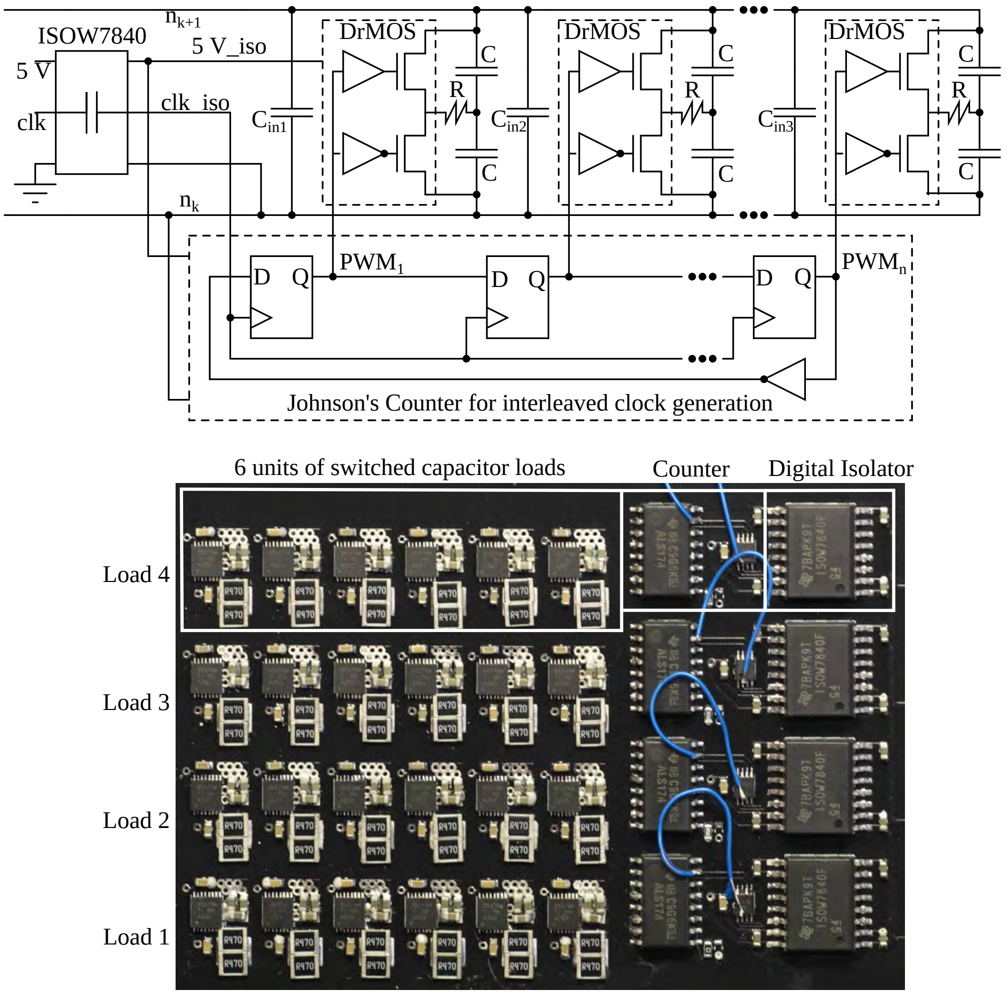


Figure 4.7: Series stacked low voltage loads with switched capacitor units.

4.3 Design of the load stack

The nominal input voltage for each load element is 1.8 V. The loads have to be designed so that they can sink 10 A of current when supplied with 1.8 V including droops due to load lines and current sense resistors. The loads can be realized with switched capacitor circuits. The proposed design is shown in Fig 4.7. Each load is designed as a parallel stack of inverters to be controlled with a variable frequency square wave. The inverters in each load are to be switched in an interleaved pattern to reduce the ripple on the sinked load current. The power dissipation of each load is supposed to emulate a digital circuit load and can be derived as $P = kf_{sw}CV^2$, where f_{sw} is the frequency of the square wave pulses to each inverter. Controlling f_{sw} allows us to change the load current at a fixed supply voltage.

To estimate the number of inverter units needed to achieve a reasonable current ripple ratio we consider a load with n interleaved inverter units as shown in Fig 4.8. Ignoring the

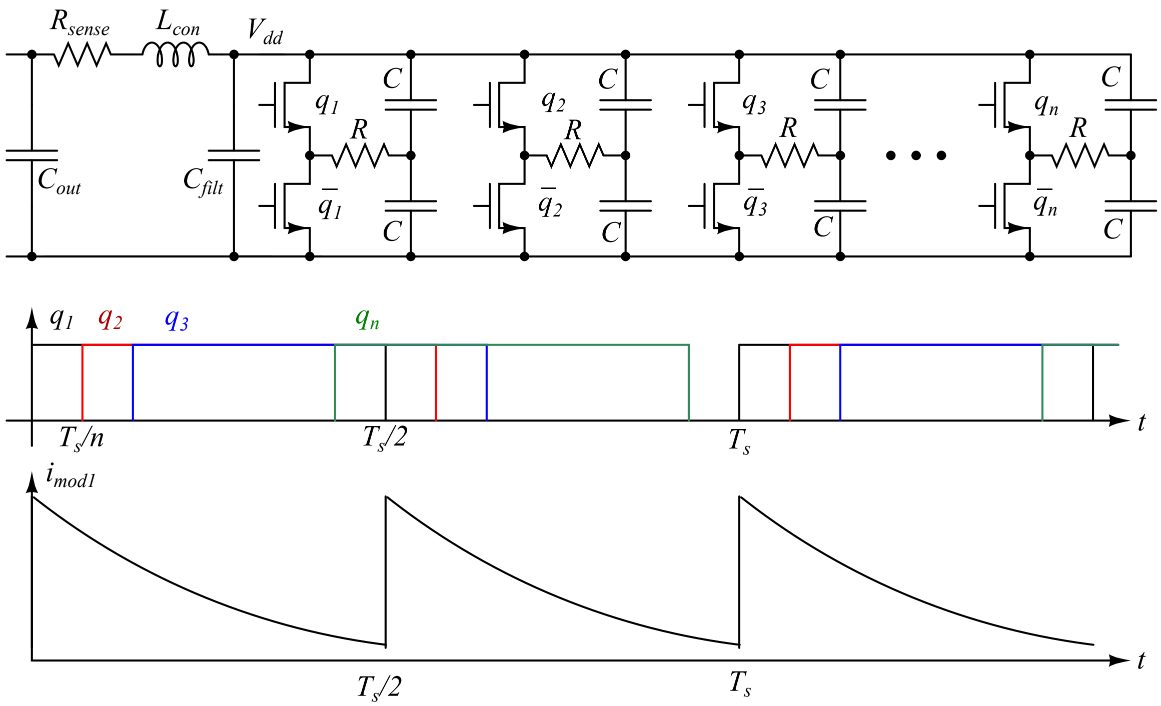


Figure 4.8: Load unit with n interleaved inverter loads.

drop across the input impedance formed of L_{con} and R_{sense}, the currents drawn from the units at $t = 0^+$ are

$$
\begin{aligned}
i_{in1}\left(t=0^+\right) &= \frac{V_{dd}}{2R\left(1+e^{-\frac{T_{sw}}{4RC}}\right)} \\
i_{in2}\left(t=0^+\right) &= \frac{V_{dd}}{2R\left(1+e^{-\frac{T_{sw}}{4RC}}\right)}e^{-\frac{(n-1)T_{sw}}{2nRC}} \\
i_{in3}\left(t=0^+\right) &= \frac{V_{dd}}{2R\left(1+e^{-\frac{T_{sw}}{4RC}}\right)}e^{-\frac{(n-2)T_{sw}}{2nRC}} \\
&\ldots \\
i_{inn}\left(t=0^+\right) &= \frac{V_{dd}}{2R\left(1+e^{-\frac{T_{sw}}{4RC}}\right)}e^{-\frac{T_{sw}}{2nRC}}
\end{aligned}
$$

The total current drawn by the load at $t = 0^+$ is

$$
i_{in}\left(t=0^+\right) = \frac{V_{dd}}{2R\left(1+e^{-\frac{T_{sw}}{4RC}}\right)}\left(\frac{1-e^{-\frac{T_{sw}}{2RC}}}{1-e^{-\frac{T_{sw}}{2nRC}}}\right) \tag{4.47}
$$

and at $t = 0^-$ is

$$i_{in}\left(t = 0^-\right) = \frac{V_{dd}}{2R\left(1 + e^{-\frac{T_{sw}}{4RC}}\right)}\left(\frac{1 - e^{-\frac{T_{sw}}{2RC}}}{1 - e^{-\frac{T_{sw}}{2nRC}}}\right)e^{-\frac{T_{sw}}{2nRC}} \tag{4.48}$$

The ripple current Δi_{in} is

$$\Delta i_{in} = \frac{V_{dd}}{2R\left(1 + e^{-\frac{T_{sw}}{4RC}}\right)}\left(1 - e^{-\frac{T_{sw}}{2RC}}\right) = \frac{V_{dd}}{2R}\left(1 - e^{-\frac{T_{sw}}{4RC}}\right) \tag{4.49}$$

The input current during $0 < t < {}^{T_{sw}}\!/_{n}$ is

$$i_{in}\left(t = 0^+\right) = \frac{V_{dd}}{2R}\left(\frac{1 - e^{-\frac{T_{sw}}{4RC}}}{1 - e^{-\frac{T_{sw}}{2nRC}}}\right)e^{-\frac{t}{2RC}} \tag{4.50}$$

The average input current $\langle i_{in}\rangle$ can be evaluated as

$$\langle i_{in}\rangle = \frac{nCV_{dd}}{T_{sw}}\left(1 - e^{-\frac{T_{sw}}{4RC}}\right) \tag{4.51}$$

The expression for average input current shows that for clock frequencies significantly below the RC time constant of the circuit, the load behaves like the resistive model for digital loads as expected. For higher frequencies the load tends to saturate. The ripple current to average current ratio is $\frac{T_{sw}}{2nCR}$. It can be inferred that increasing the number of paralleled inverters will serve to improve both the linearity of the load and the ripple to average current ratio. However, generating interleaved clock signals for the inverter units becomes a problem as we increase the number of paralleled loads. To accurately generate n interleaved clock signals of frequency f_{sw} we need a master clock signal whose frequency is at least nf_{sw}. In our design we use a Johnson's counter to generate n interleaved clock signals from a higher frequency clock signal of frequency $f_{clk} = nf_{sw}$. The load current and ripple current expressions can be modified as

$$\langle i_{in}\rangle = CV_{dd}f_{clk}\left(1 - e^{-\frac{n}{4RCf_{clk}}}\right) \tag{4.52}$$

$$\Delta i_{in} = \frac{V_{dd}}{2R}\left(1 - e^{-\frac{n}{4RCf_{clk}}}\right) \tag{4.53}$$

Load units with 220 mΩ resistance and 4.7 μF capacitance were built. With six modules in parallel and a load current sense resistance of 25 mΩ, a maximum current of 6.7 A could be drawn by the loads at $f_{clk} = 2$ MHz, as can be verified from the plots in Fig 4.9. This

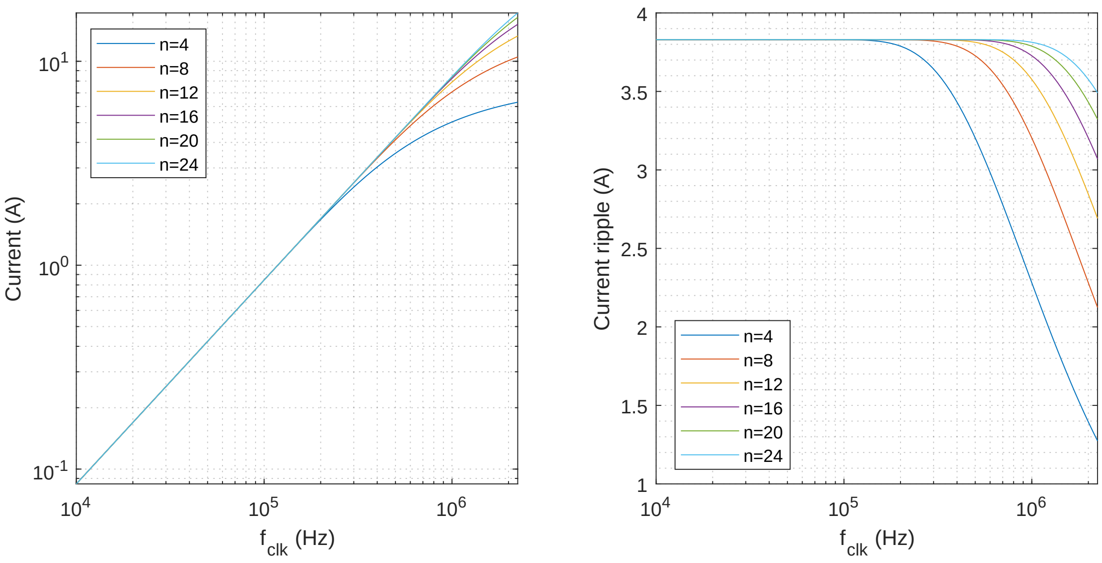


Figure 4.9: Loads without input impedance, behavior with respect to master clock frequency with varying number of units.

frequency was the upper limit of what could be achieved with the setup. The gate drive of the DrMOS used for building the loads was supplied by isolated 5 V power supplies (ISOW7840F) which were limited to a 650 mW power output. Increasing f_{clk} beyond 2 MHz caused the isolated supplies to start throttling and shut down (the isolated 5 V supplies the integrated gate drivers and the interleaved clock generation logic circuit, both of which draw increasing power with increasing frequency). A second load board could be populated and paralleled with the first load board, and this would allow us to draw up to the targeted 10 A load from the 1.8 V domains (taking into account the droop of the balancing regulators and the drop in the sense resistors). However, this would only be necessary if we intended to test the voltage regulation of the stack up to 100% mismatch. Instead, we used an electronic load to provide an offset load current for efficiency measurements in the higher current range, as shown in Fig 4.10.

Different sense resistor and passive components were used to build the loads for testing at light loads and lighter loads. Increasing the sense resistor value for measurements at light loads allowed for reducing the current ripple at light loads and as well as in improving measurement accuracy. The values of the components used for building the loads are shown in Table 4.1. This allowed satisfactory measurement of experimental data presented in the next section.

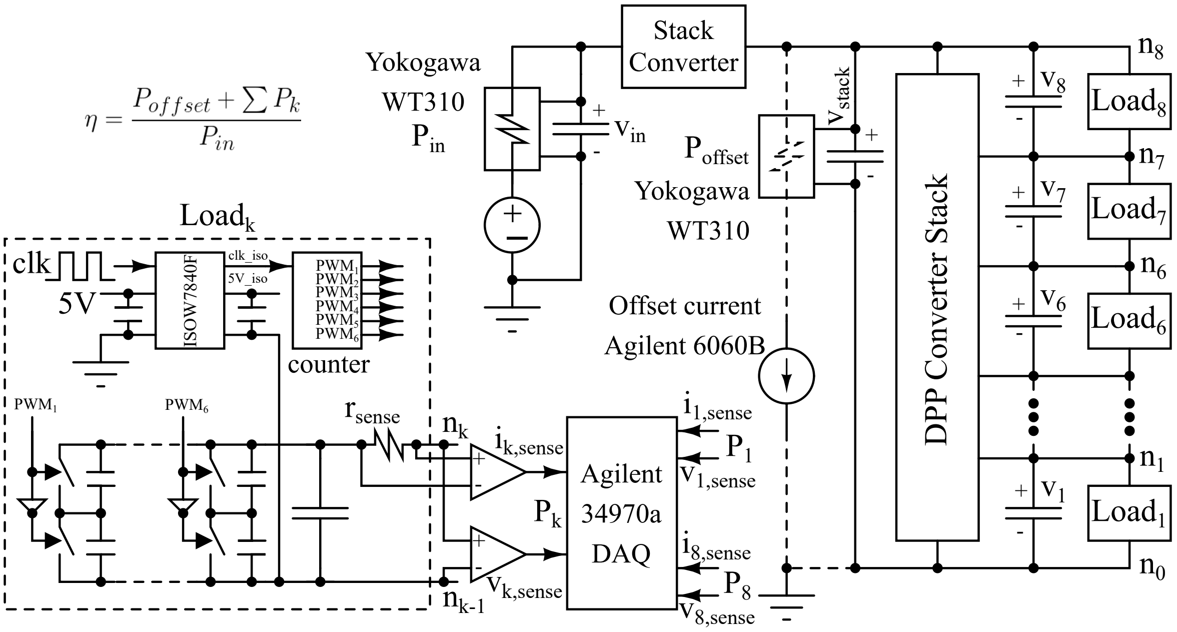


Figure 4.10: Measurement setup for system level efficiency datalogging.

Table 4.1: Load board components.

Component	Part Number	Specifications
DrMOS	CSD95379Q3M	20 V, 20 A
R (light load)	RL1632R-R750-F	0.75 Ω
C (light load)	06035C333JAT2A	0.33 μF, 25 V, 0603
R_{sense} (light load)		0.5 Ω (2 × 1 Ω parallel)
R (int-light load)	RL1632R-R750-F	0.75 Ω
C (int-light load)	CL10F334ZA8NNNC	1 μF, 25 V, 0603
R_{sense} (int-light load)	RL1632R-R750-F	0.075 Ω
R (heavy-int load)	RCWE1210R470FKEA	2 × 0.47 Ω (parallel), 1 W
C (heavy-int load)	LMK107BJ475KA-T	4.7 μF, 10 V, 0603
R_{sense} (heavy-int load)	FCSL110R025FER	0.025 Ω, 4320 wide
C_{filt}	CC0603ZRY5V6BB225	6 × 2.2 μF, 10 V, 0603
Digital Isolator	ISOW7840F	4 channel isolator, integrated power
D flip-flop (Counter)	SN74ALS174NSR	Hex D-type flip-flop with clear
Current sense amplifier	AD8218BRMZ	Current monitor (g = 20)
Voltage sense amplifier	INA149AID	Differential voltage sense (g = 1)

4.4 System level efficiency measurements

For measurement of system level efficiencies at light loads, the load board was populated with components from Table 4.1 labeled “light load”. Varying clock frequency between 250 kHz and 2.5 MHz allowed for varying the average current of each load between 50 mA and 500 mA. The 0.5 Ω current sensing resistance, and six paralleled 2.2 μF filter capacitances placed at the input of the DrMOS half bridges, helped in maintaining low current ripple for satisfactory measurement accuracy. For measurement of system level efficiencies at intermediate-light loads, the load board was populated with components from Table 4.1 labeled “int-light load”. Varying clock frequency between 250 kHz and 2.5 MHz allowed for varying the average current of each load between 200 mA and 2.5 A. At intermediate-heavy and heavy loads, the load boards were populated with the components labeled “heavy-int load”. These values allowed the load to be varied up to 7 A (for a clock frequency of 2 MHz). For capturing system level efficiencies beyond $i_{stack} = 7$ A, an Agilent 6060B electronic load was used to provide an offset load current. Under an offset current of 3 A, if the load currents of the switched capacitor loads are varied between 2 A and 7 A, system level efficiencies for i_{stack} upto 10 A can be captured (limiting mismatches up to 50%). Yokogawa WT310 power meters were used to capture the input and offset powers. An Agilent 34970a Data Acquisition Card was used to capture power dissipated in the switched capacitor loads. The setup for efficiency measurements has been shown in detail in Fig 4.10.

The loads were ramped up in small steps by stepping the clock frequencies of each load. The step size of each frequency change determines the percentage mismatch at which the system-level efficiencies are being measured. An example of the ramping of the loads is shown in Fig 4.21. System level efficiency measurements were performed for different load step sizes (allowing for measurements at 5%, 10%, 20% and 40% mismatches).

The order in which the loads are stepped up has an influence on the differential power processed by the DPP converters. For example, stepping up the loads in the order [1, 2, 3, 4, 5, 6, 7, 8] would ensure that all of the DPP converters process the maximum mismatch currents for some instances. While, following the order [1, 8, 2, 7, 3, 6, 4, 5] limits the mismatch current processed by DPP_4 to 25%, and mismatch currents processed by DPP_2 and DPP_6 to 50% of the maximum mismatch current during the course of the entire profile. System-level efficiency data under a few different stepping orders was captured. The efficiency of the DPP stack regulator was estimated by subtracting interpolated losses of the stack converter from the system losses and shown in Fig 4.11. The captured data was mapped with respect to total output power and differential power processed and the corresponding efficiency and loss distribution are shown as the contour plots in Figs 4.12 and 4.13.

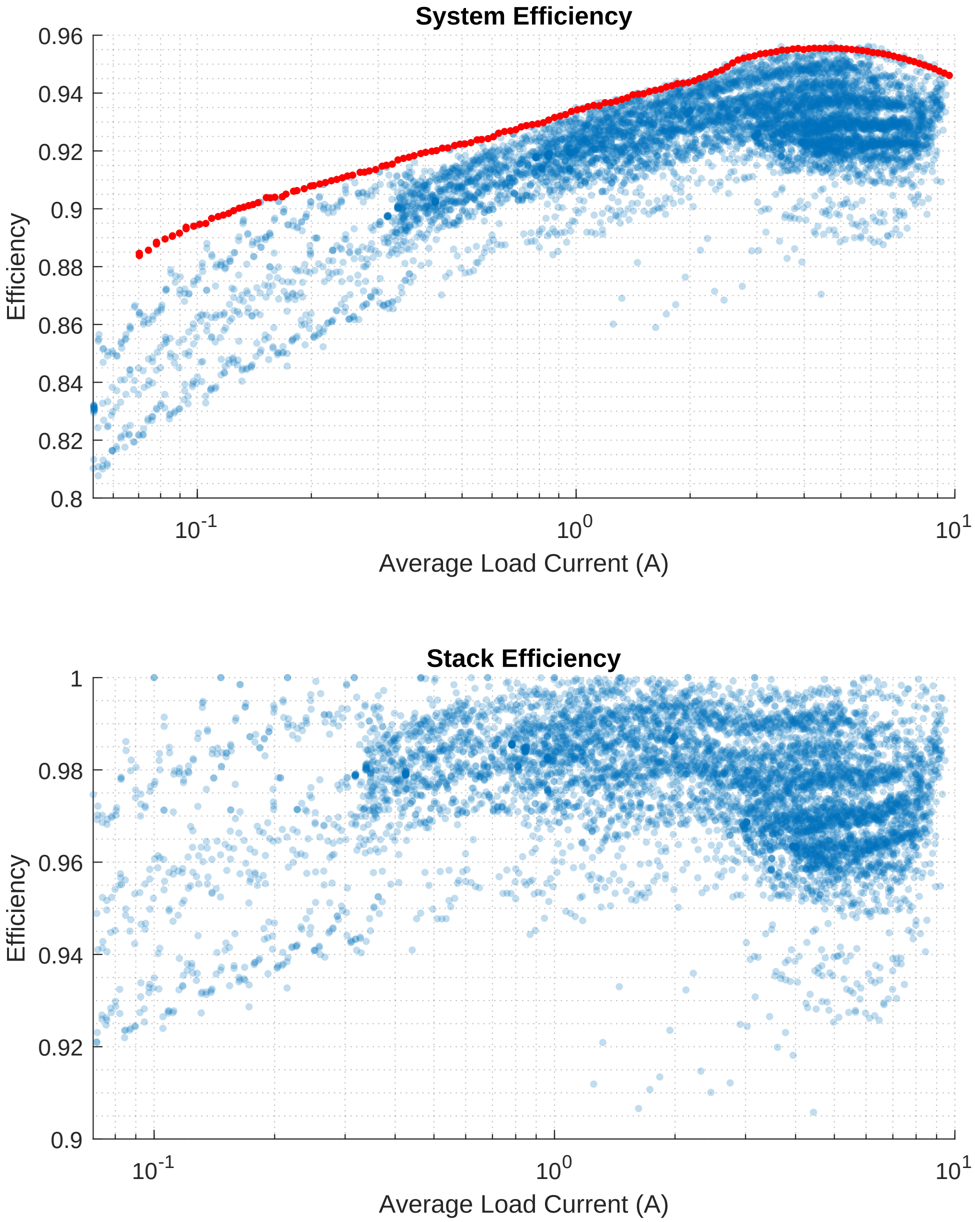


Figure 4.11: Efficiency of the system under mismatch power processed limited to 40%. Red: Efficiencies under zero mismatch with electronic load attached to the v_{stack} rail and none of the switched capacitor loads operational.

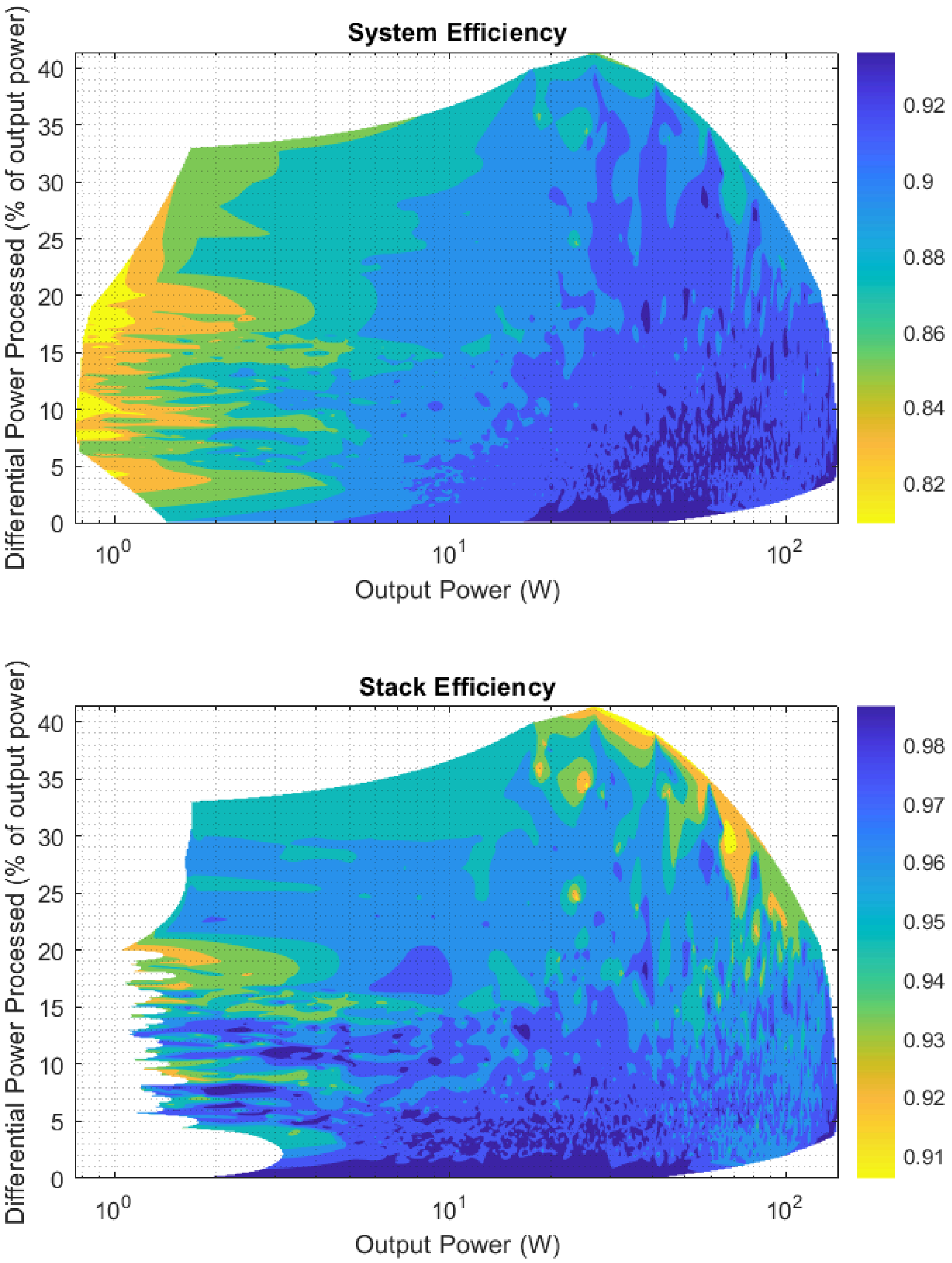


Figure 4.12: Efficiency map of the system with respect to output power and processed differential power. Differential power processed limited to 40%.

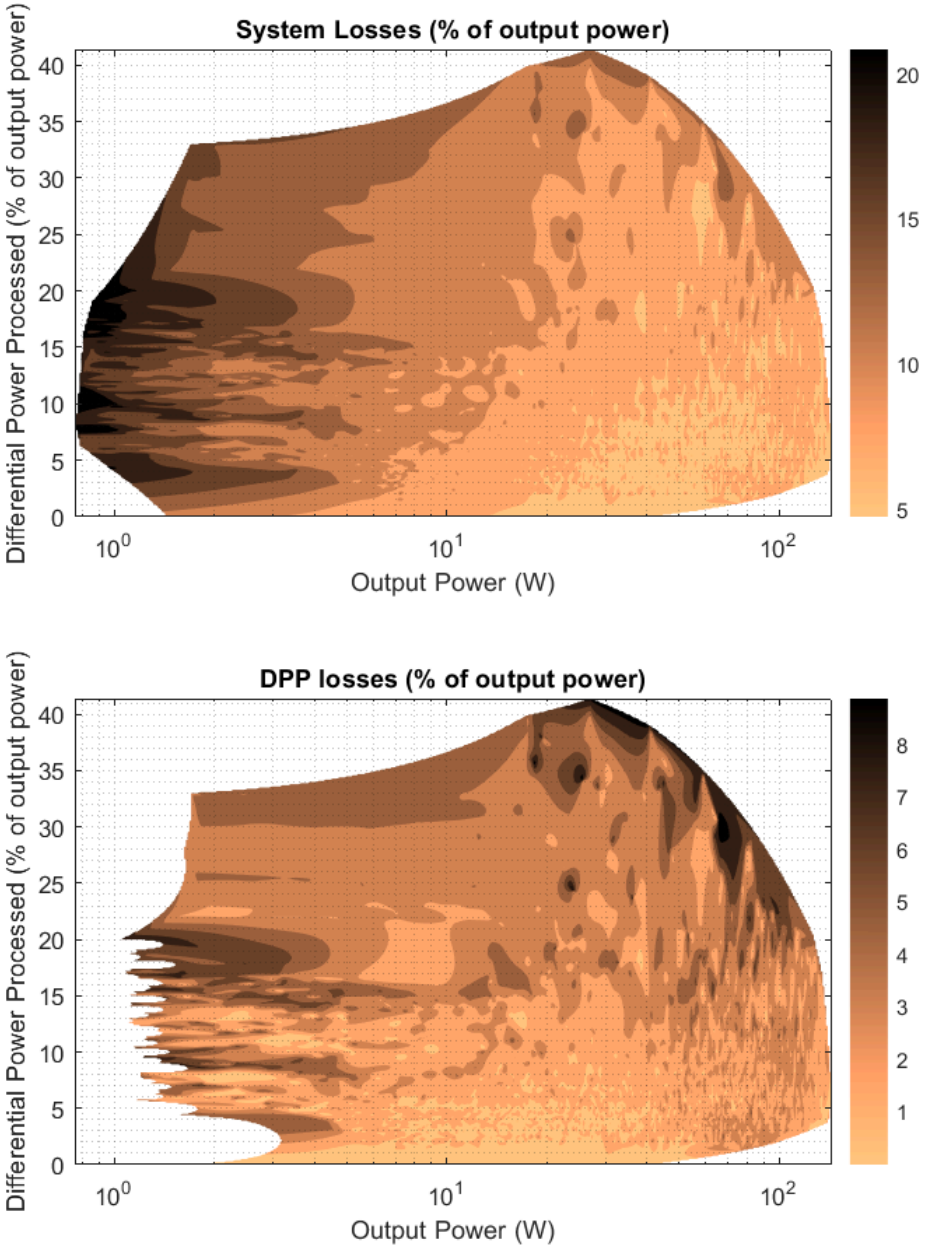


Figure 4.13: System and DPP stack losses with respect to output power and processed differential power. Differential power processed limited to 40%.

4.5 Load transients

Some transient load profiles are used to test stability and voltage regulation of the hierarchical DPP regulator. An Agilent 6060B electronic load was used to emulate load transients at different points in the series stack. The load transients shown in Figs 4.14 through 4.20 show load transients and the DPP currents that change in order to maintain voltage regulation. The achievable load current slew rates with the Agilent 6060B electronic load were considerably slower (slightly lower than 0.5 A/μs) than that typically encountered while powering microprocessor loads. However, testing load transients with multiple voltage domains enables us to emulate a situation where multiple cores are stepping up their power dissipation at the same time. For example, the load transient scenario depicted in Fig 4.15 emulates a scenario where three of the cores step up the load from up to 5 A at the same time. The equivalent load current slew rate for the parallel power delivery system would be three times of what we have tested here. For each of these load transients, we note that the DPP converters respond much faster than the stack converter (the DPP inductor currents settle much faster than the node voltages monitored).

Improving the load transient responses would be possible by improving the settling time of stack converter itself (either by switching faster, or by improved control methods). These load transients represent some heavily mismatched conditions, verifying stability and voltage regulation well within 10% limits. Also to be noted is that the delayed phase shedding/adding operations of the DPP converters themselves propagate and add to the response time with respect to the load transients. For example, in the load transient scenario of Fig 4.15, the second phase of DPP$_3$ is enabled with minimal delay (10 μs). But the second phases of DPP$_2$ and DPP$_4$ are enabled after another 20 μs (seen as the voltage of the node monitored on Channel 1 starts to rise up to 5.4 V). These additional delays can be minimized by lowering the values additional capacitances at the outputs of the inner DPP converters.

Some load profiles are tested under lower mismatched conditions. Similar to the efficiency measurement setup, the variable switching frequency loads were used. The loads are ramped up in 20%steps from light load to intermediate load (4 A). The eight load currents and eight domain voltages are captured with a 16 channel 125 kHz sampling rate ADC evaluation board (AD7616P). These load profiles captures are shown in Fig 4.21 and Fig 4.22. The steady state voltages are verified to be well within 10% regulation limits for these lightly mismatched conditions.

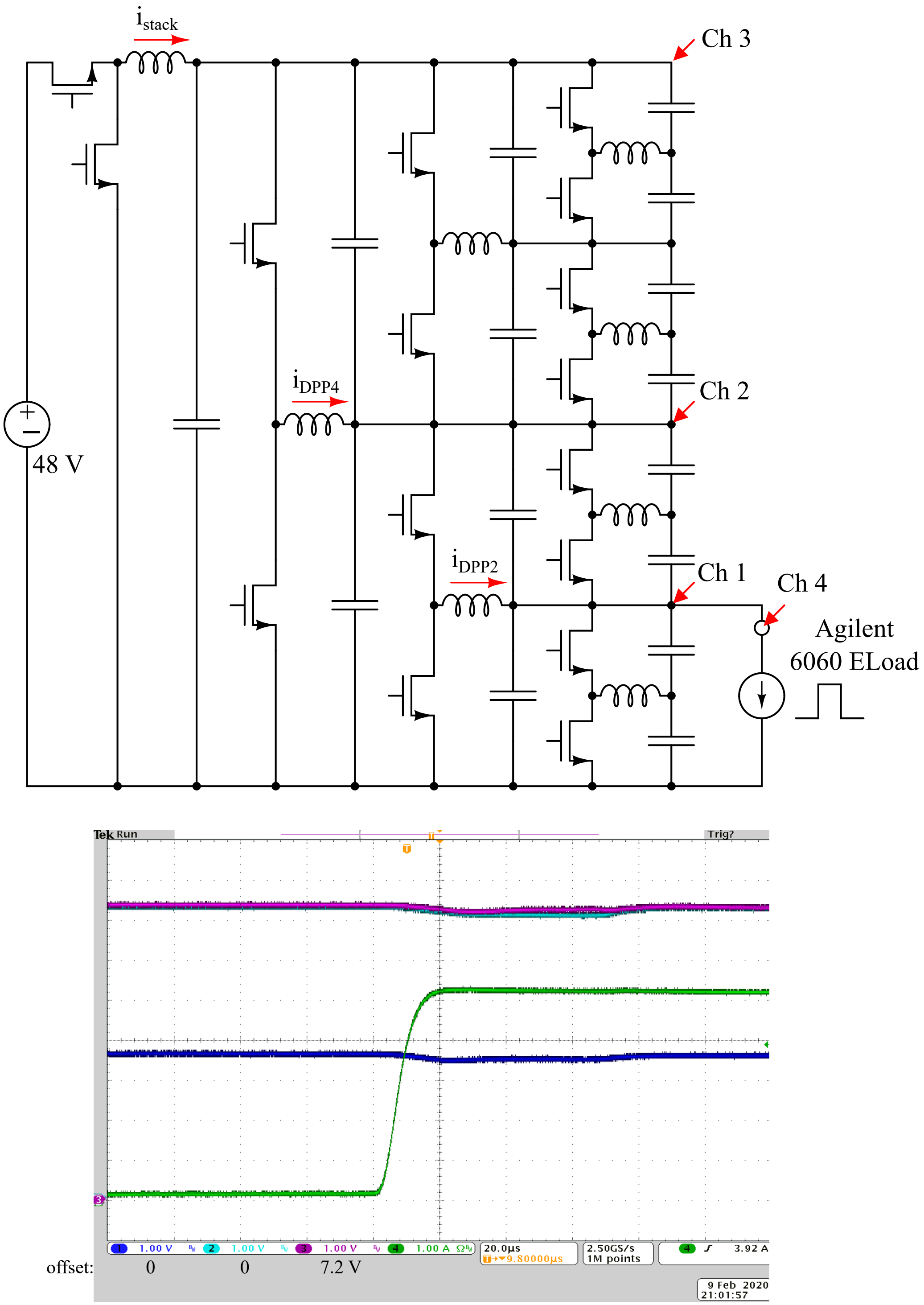


Figure 4.14: Load transient response 1: A 5 A load transient at the node n_2 causes DPP_2 to enable both its phases to deliver 5 A of differential current. DPP_4 also has to enable both its phases to deliver 2.5 A of differential current. The stack converter delivers 1.25 A and remains in light-load operation. The droop at node n_2 is approximately 100 mV. Horizontal time scale: 20 μs/div.

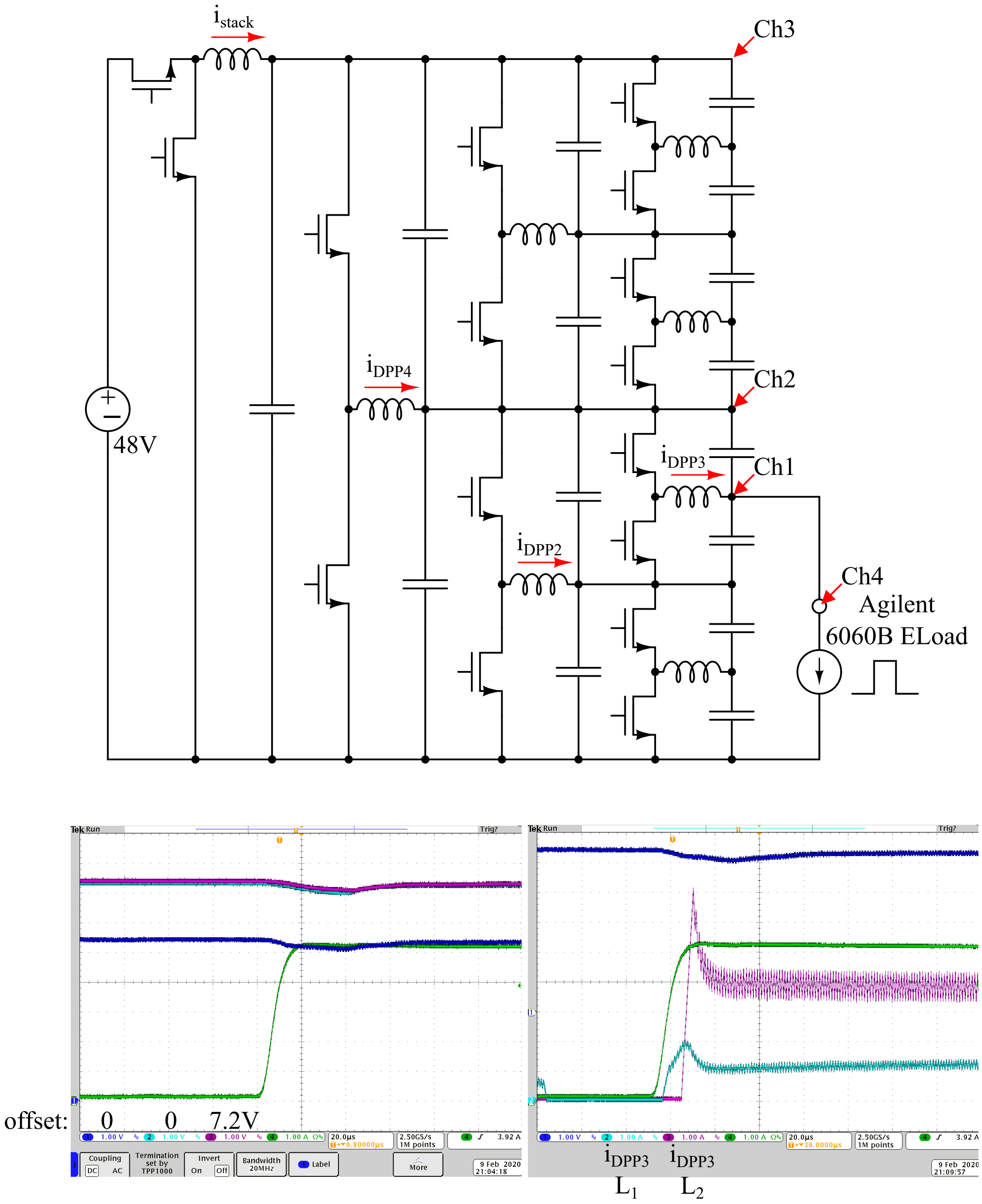


Figure 4.15: Load transient response 2: A 5 A load transient at the node n_3 causes DPP_3 to enable both its phases to deliver 5 A of differential current. DPP_2 also has to enable both its phases to deliver 2.5 A of differential current. DPP_4 delivers 3.75 A of differential current. The stack converter delivers 1.9 A and remains in light-load operation. The droop at node n_3 is approximately 400 mV (7.4%), which would be the worst percentage droop of all the nodes in the stack. Horizontal time scale: 20 μs/div.

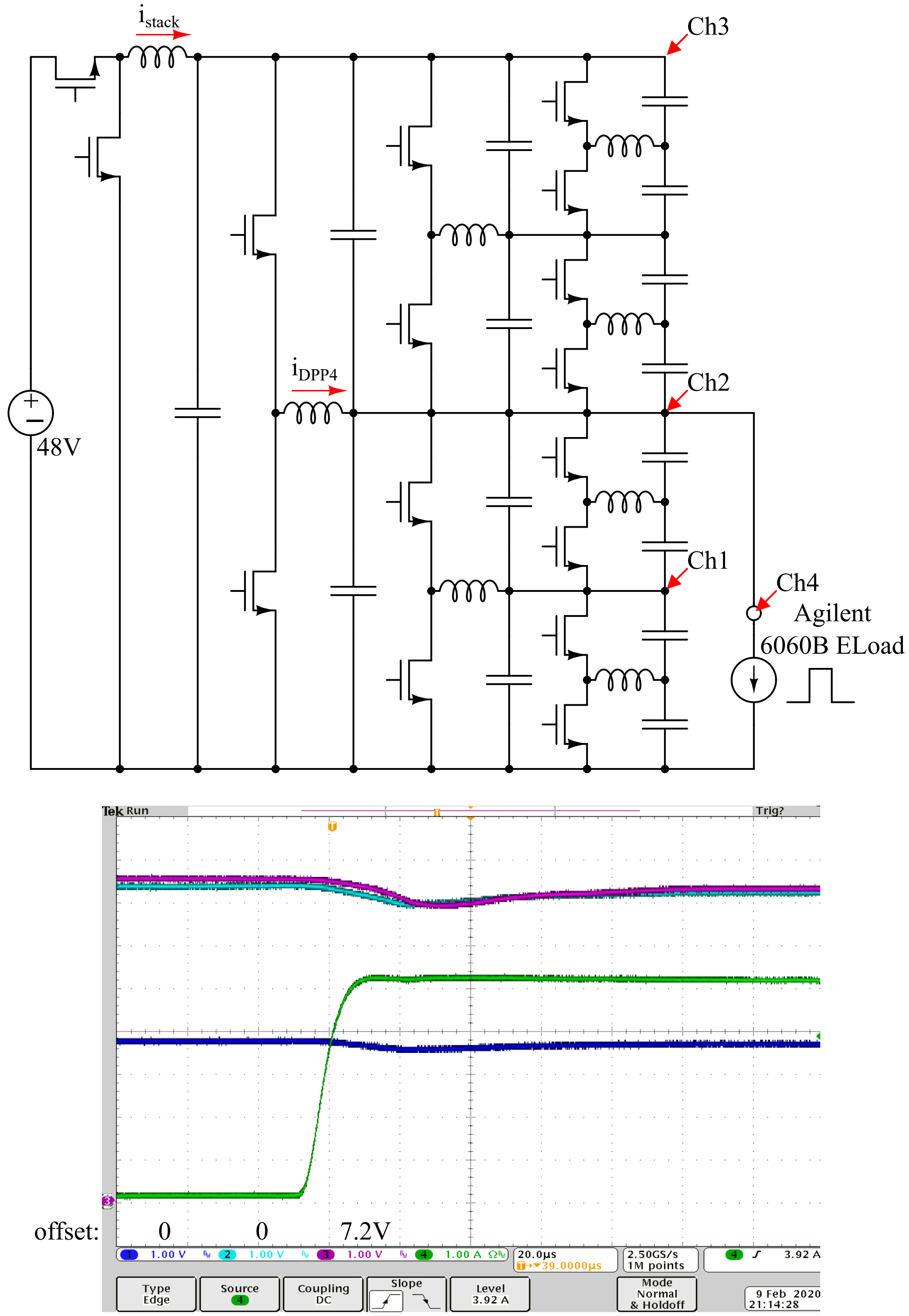


Figure 4.16: Load transient response 3: A 5 A load transient at the node n_4 causes only DPP_4 to enable both its phases to deliver 5 A of differential current. The stack converter delivers 2.5 A and remains in light-load operation. The droop at node n_4 is approximately 600 mV (8.3%), which would be the worst percentage droop of all the nodes in the stack. Horizontal time scale: 20 μs/div.

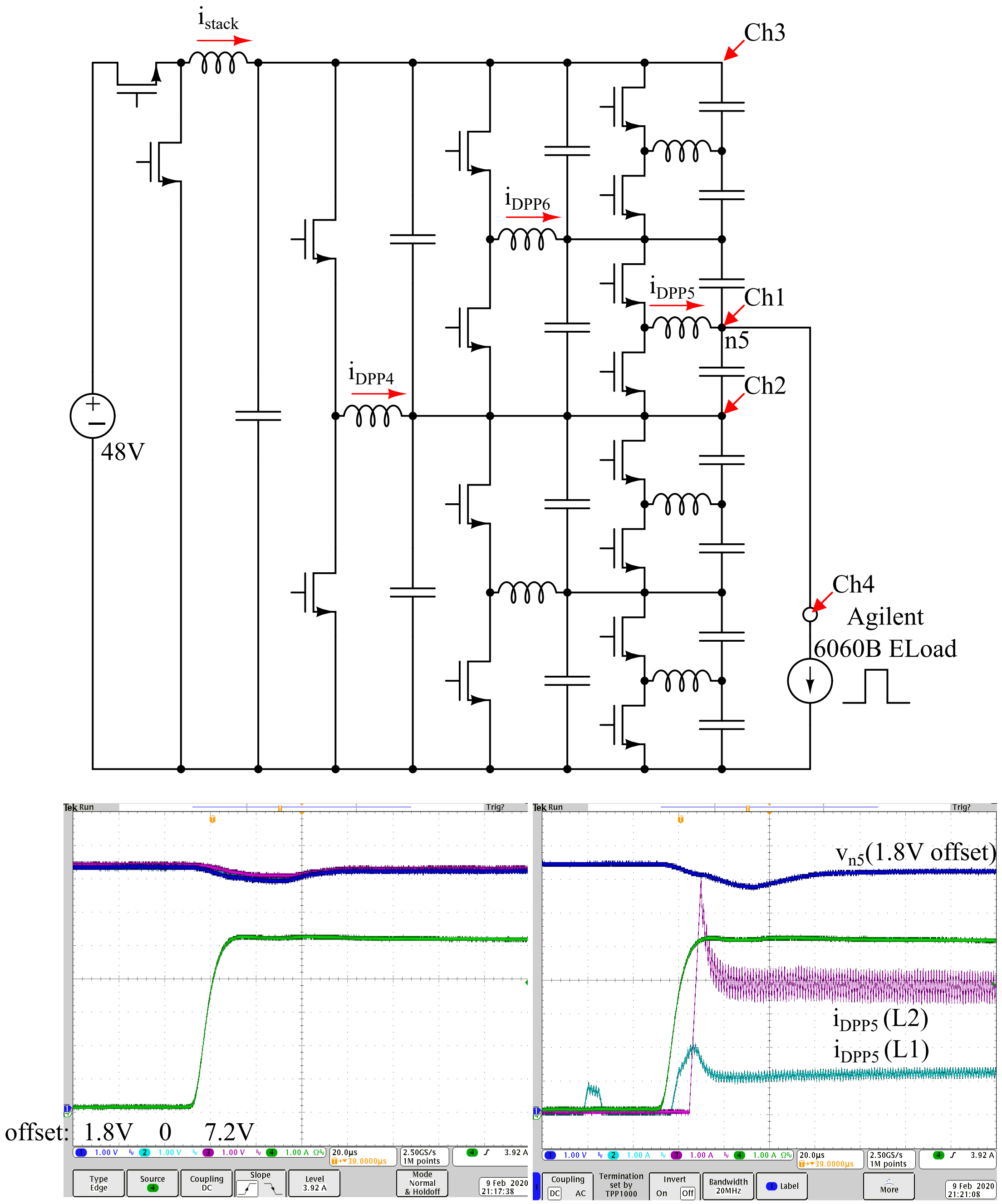


Figure 4.17: Load transient response 4: A 5 A load transient at the node n_5 causes DPP_5 to enable both its phases to deliver 5 A of differential current. DPP_6 also has to enable both its phases to deliver 2.5 A of differential current. DPP_4 delivers 3.75 A of differential current. The stack converter delivers 3.2 A and operates in CCM. The droop at node n_5 is approximately 800 mV (8.8%), which would be the worst percentage droop of all the nodes in the stack. Horizontal time scale: 20 μs/div.

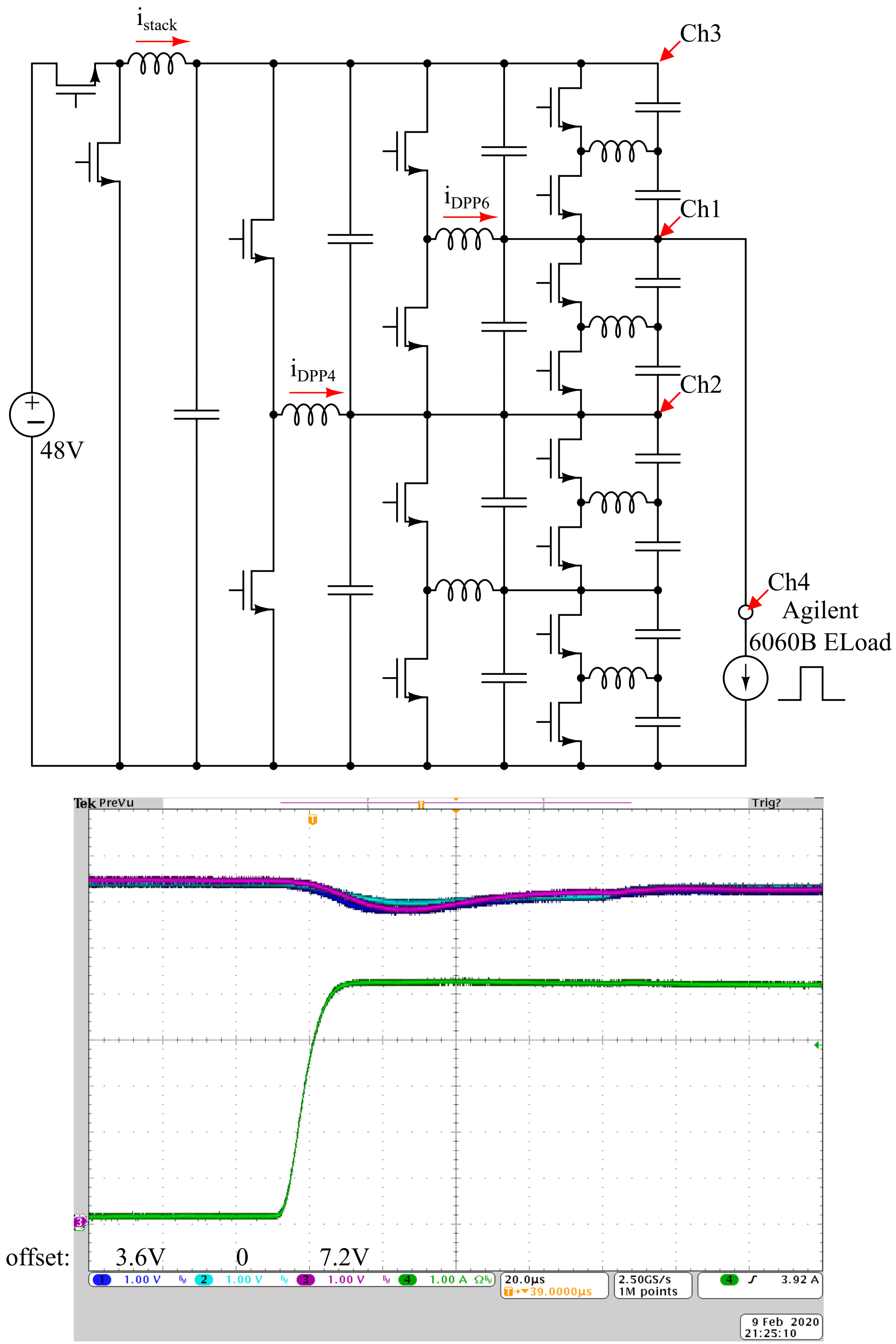


Figure 4.18: Load transient response 5: A 5 A load transient at the node n_6 causes DPP_6 to enable both its phases to deliver 5 A of differential current. DPP_4 also has to enable both its phases to deliver 2.5 A of differential current. The stack converter delivers 3.75 A and operates in CCM. The droop at node n_6 is approximately 600 mV (5.5%), which would be the worst percentage droop of all the nodes in the stack. Horizontal time scale: 20 μs/div.

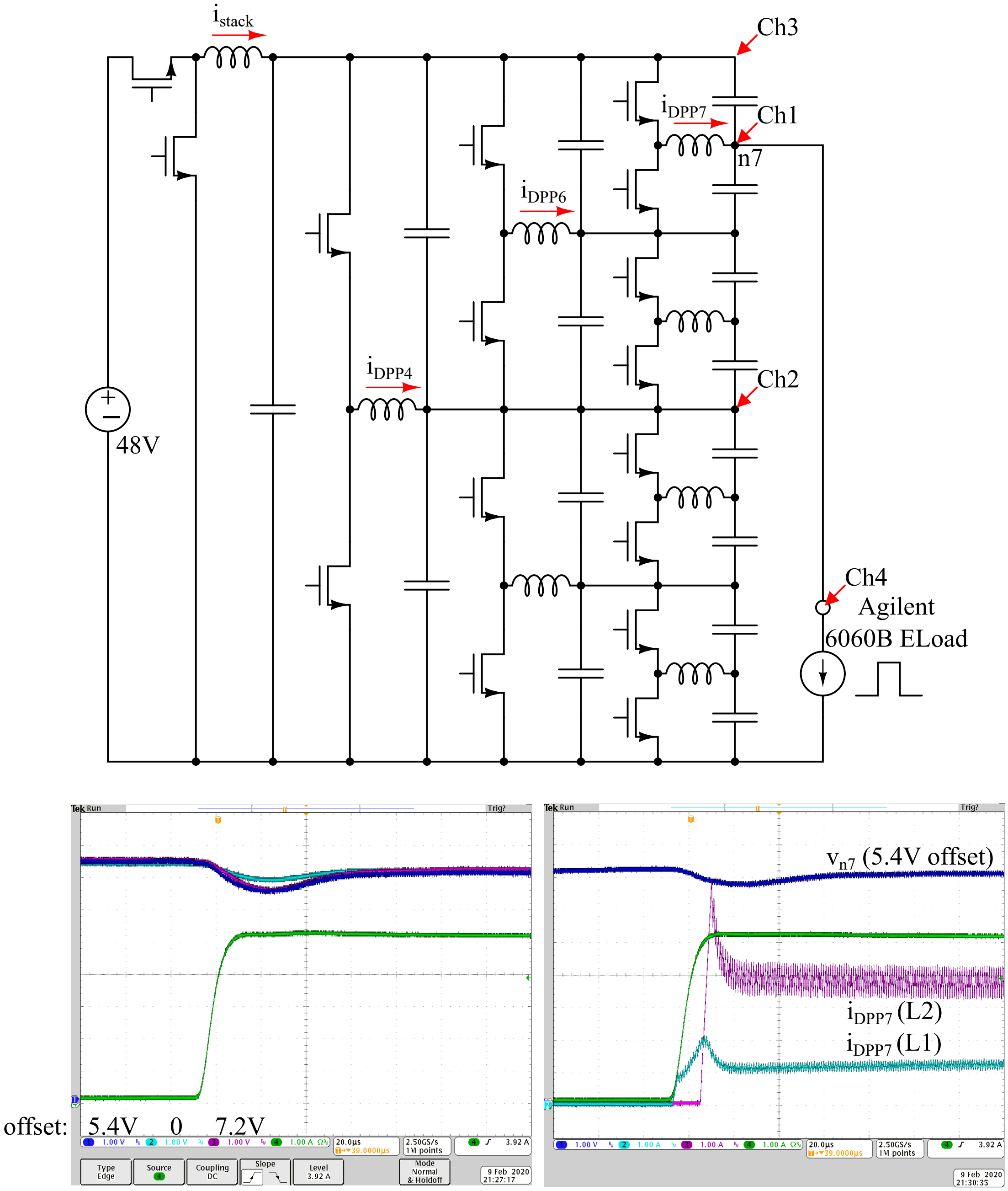


Figure 4.19: Load transient response 6: A 5 A load transient at the node n_7 causes DPP_7 to enable both its phases to deliver 5 A of differential current. DPP_6 also has to enable both its phases to deliver 2.5 A of differential current. DPP_4 delivers 1.25 A of differential current with its low current phase in CCM. The stack converter delivers 4.4 A and operates in CCM. The droop at node n_7 is approximately 1 V (7.9%), which would be the worst percentage droop of all the nodes in the stack. Horizontal time scale: 20 μs/div.

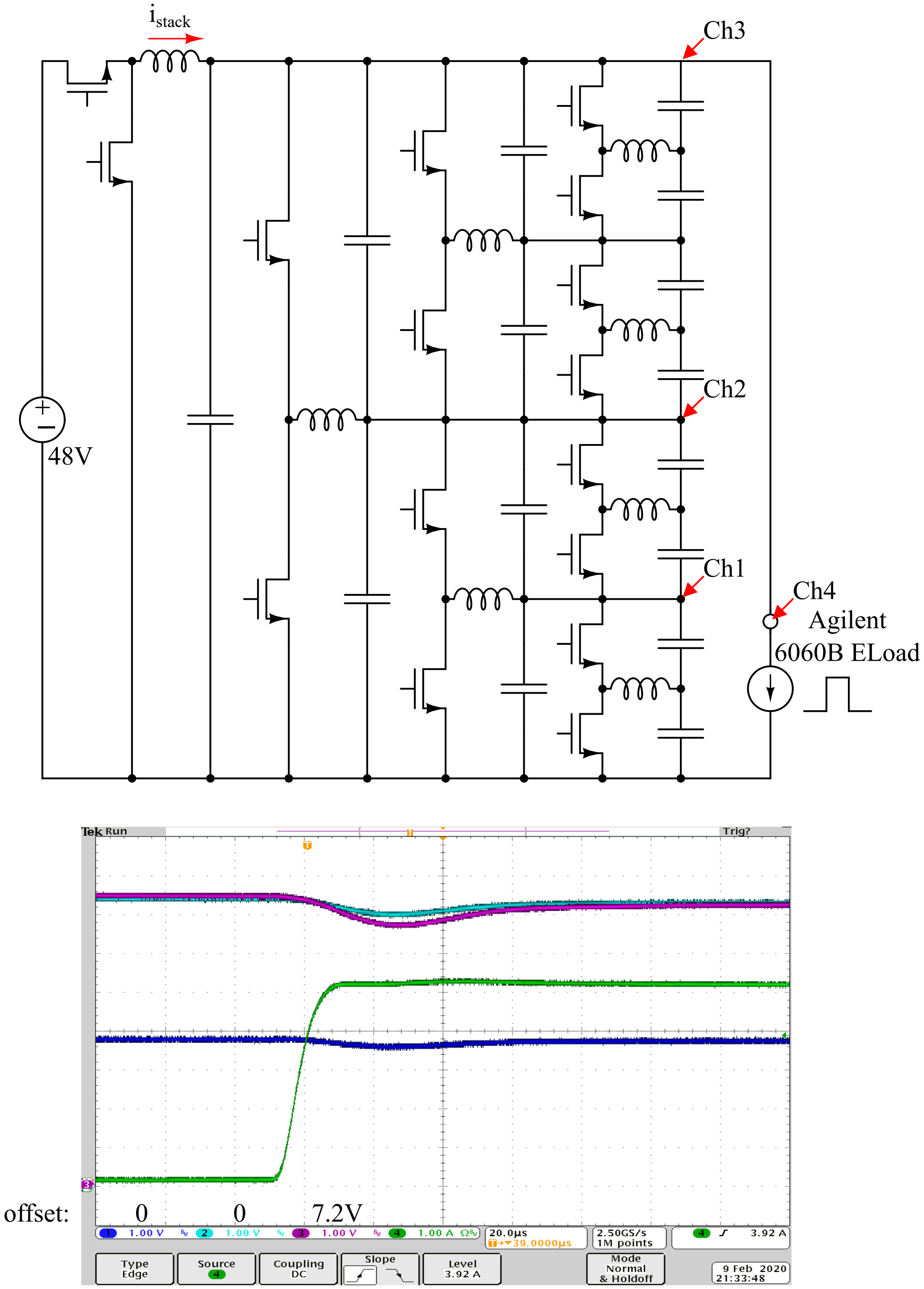


Figure 4.20: Load transient response 7: Load transient at the input of the stack only engages the stack converter. The stack voltage droop is approximately 0.75 V (5.2%). The stack converter's voltage droop propagates through the stack to all the domain voltages and gets distributed proportionally. Horizontal time scale: 20 μs/div.

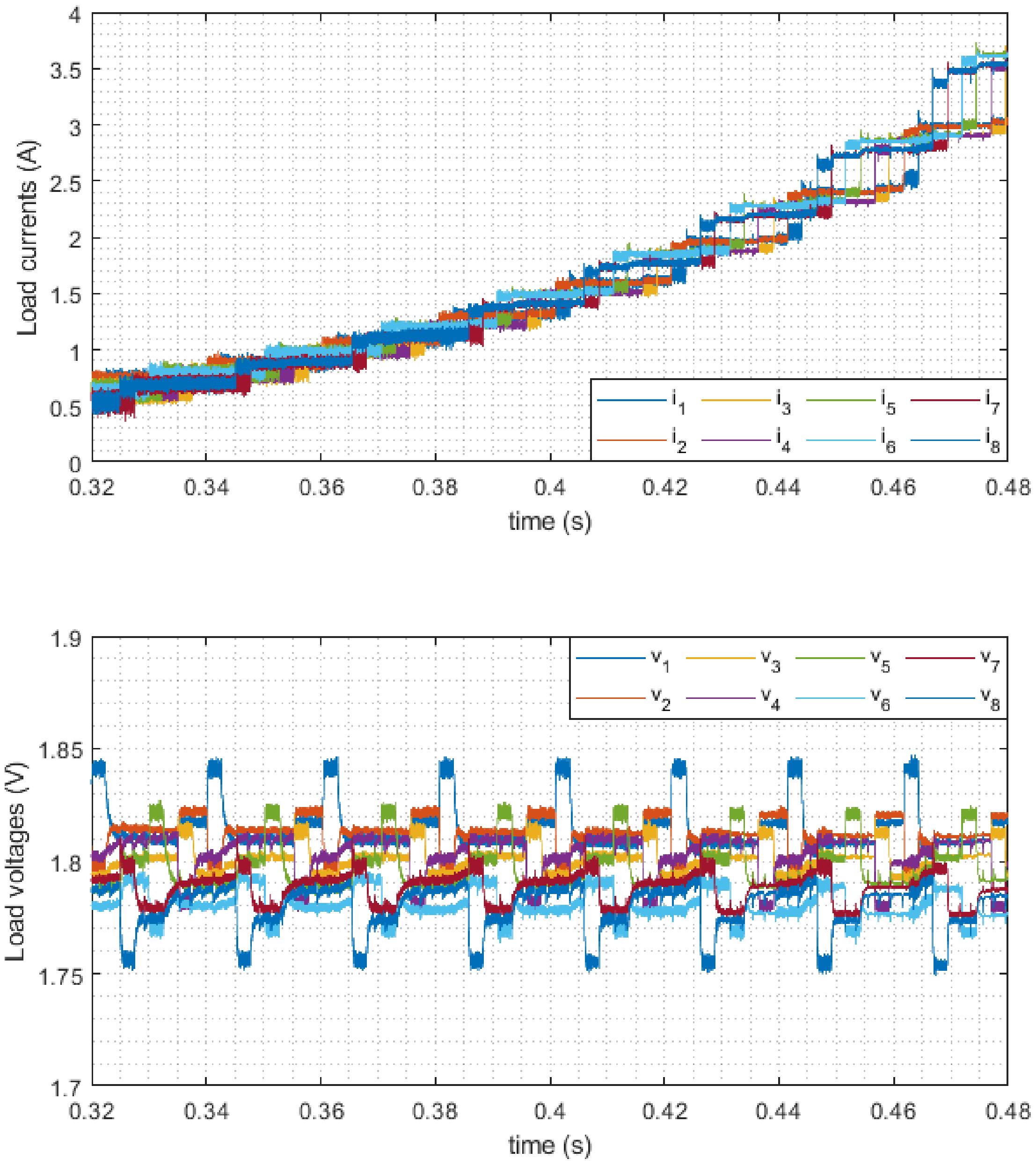


Figure 4.21: Voltage regulation of the eight 1.8 V domains under transients within 20% of average current. Load currents ramping up in 20% steps every 2.5 ms.

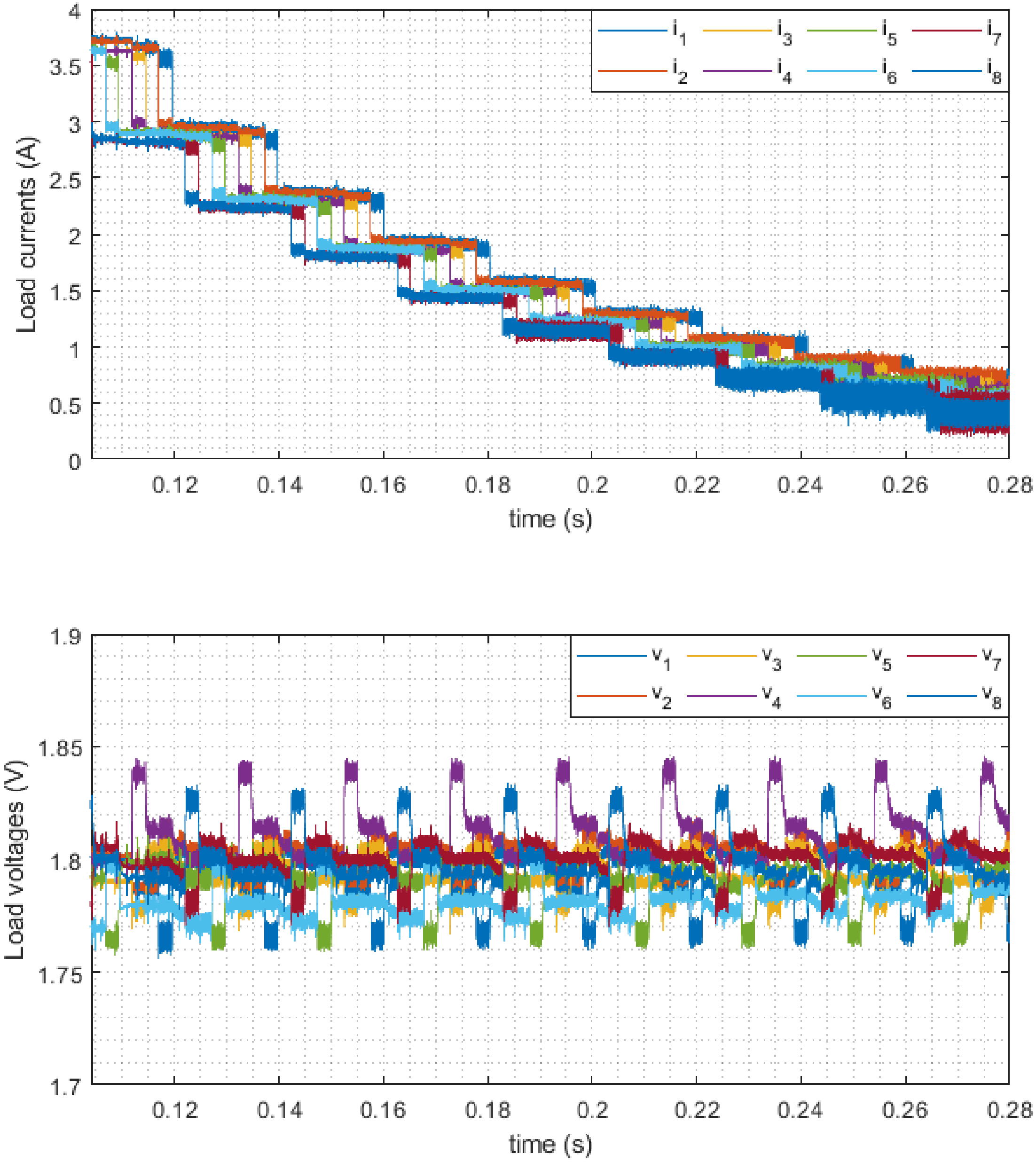


Figure 4.22: Voltage regulation of the eight 1.8 V domains under transients within 20% of average current. Load currents ramping down in 20% steps every 2.5 ms.

CHAPTER 5

CONCLUSION

The advantages of series stacked power delivery for low voltage loads compared to the conventional parallel connected power delivery system were discussed, and a differential power processing based architecture was proposed for power delivery for a series stack of eight low voltage high current domains. The series stacked architecture enables more efficient power delivery due to lower current requirements. For maintaining high efficiency over a wide load range, a light load control scheme suitable for bidirectional converters was proposed and demonstrated in Chapter 2 of this thesis. A single phase bidirectional converter was capable of achieving near 100x load range, while maintaining good transient response and voltage droop characteristics. For improving load range, a bidirectional two phase converter with asymmetric current sharing was proposed and demonstrated in Chapter 2. This converter employs the light-load control developed previously at light loads and also uses phase shedding to maintain over 90% efficiency over more than a 100x load range.

Bulk power for the series stacked loads needs to be supplied from a 48 V bus through a step-down converter. Step-down conversion of 48 V to 14.4 V (eight series stacked 1.8 V domains) was achieved with a two-phase interleaved buck converter, demonstrated in Chapter 3. With relaxed output impedance requirements due to series stacking of the low voltage domains, a two-phase converter was sufficient to meet 10% transient regulation limits. The designed two-phase converter employs a sensorless current mode control. Small signal analytical models for the sensorless current-mode-controlled two-phase buck converter were developed and verified against switching models in simulations. The sensorless current mode control also achieves excellent current sharing, on a par with that of conventional peak current mode controllers which are common for power delivery to microprocessor loads. Further, the controller is also augmented for operation in burst mode at light loads, which suited our target for achieving high system level efficiency over a wide load range.

Stability of the series stacked domain voltages with a distributed droop current mode control was discussed in Chapter 4. A frequency dependent switched capacitor load was designed for emulating digital circuit loads and system-level efficiency measurements were performed, for a wide range of mismatched conditions. Better than 85% system-level efficiency (averaged over mismatched conditions up to 40%) was demonstrated over an output power range of 1.44 W to 144 W. The power delivery system also achieved satisfactory transient performance, although transient performance at extreme load current slew rates was not tested. However, the tested load current slew rates were significantly higher than the response times of the regulating converters. It was demonstrated that even under heavily mismatched conditions, it is possible to maintain excellent voltage regulation for all stacked voltage domains with droop controlled balancing converters and a bulk power converter with reasonable output impedance.

5.1 Future work

Equalization of voltages of series connected domains with fast varying loads has been demonstrated in the research presented in this thesis. One of the initial motivations for using a switched inductor topology in this research was that voltage regulation is possible by operating the converters at different duty ratios. While the hierarchical topology is capable of driving each domain voltage to a particular desired reference value, dynamic voltage scaling (and related analysis of inrush currents associated with voltage reference tracking) has not been demonstrated, and would be a valuable addition for completeness of this research.

The general idea of nested or hierarchical DPP is very suitable and would be preferred for applications where a large number of series stacked domains are needed - such as battery packs in electric vehicles or grid level energy storage systems. It seems to have an advantage over the more generally accepted switched inductor ladder in terms of distributed control and amount of differential power processed, at the cost of modularity. The current mode control approach developed in this thesis is easily adapted to a battery management system where regulation of charging current to each battery is the end goal.

APPENDIX A

LOSS-MODELING OF DIFFERENT CURRENT SHARING RATIOS

The switch power losses are calculated as described in [62]. The loss models provide a good estimate of power losses in on board synchronous buck converters. However, they do not include the effects of inductor current saturation (increased ripple at higher loads). The inductor losses are generated from Coilcraft's inductor loss data available at [48]. This loss data also does not accommodate for saturation effects at higher currents, so the converter losses evaluated in the following code are inaccurate as the loads get closer to the saturation current limits of the inductors. Moreover, switching frequency is assumed to be held constant, which is generally not true for hysteretic current mode control. However, these models provide a good estimate of losses at light loads, in which we are more interested. The MATLAB script for optimizing converter switch sizes for different current sharing ratios is provided.

```
% XEL4030 inductor loss data
f_sw    =  [1500,1000, 900, 800, 700, 600, 500, 400, 350, 300, 250, 200, 150]'*1e3;
L       =  [0.64, 0.9, 1.2, 1.5, 2.2, 3.3, 4.7, 6.8]*1e-6;
Co      =  100e-6;

p_ac    =  [ 28   20   18   15   10    5    4    2;
             56   38   32   24   17    9    7    4;
             66   44   37   28   20   10    8    4;
             79   53   42   32   23   12    8    5;
             96   63   50   38   26   14   10    6;
            121   78   60   46   32   16   11    8;
            158  100   74   57   39   20   14    9;
            217  134   95   74   49   26   18   12;
            264  159  111   86   55   29   21   14;
            330  191  131  103   64   33   24   16;
            429  236  158  124   74   38   28   20;
            590  296  195  156   85   43   32   24;
            880  371  243  200   91   43   35   31]*1e-3;

r_dcr   =  [5.90 8.80 9.78 11.5 16.6 22.1 28.6 44.1 74.1]*1e-3;

ipk     =  10;
npk     =  1;
iout    =  logspace(-3,0,1000)*ipk;
```

```
ripv     =  zeros(1000,1);

% parameters for CSD17484F4
Qgs      = 0.28e-9;
Qgd      = 0.075e-9;
Rdson    = 107e-3;
Qg       = 0.9e-9;
Qrr      = 0.45e-9;
Coss     = 45e-12;
Vsd      = 0.73;
Rg       = 8;
tdead    = 20e-9;
Rdrv     = 1.2;
Vdrv     = 7;
Vin      = 7.2;
vout     = 3.6;
csi      = 1e-9;
Vpl      = 2.2;
pstatic  = 0.001*3.6;
rcin     = 0.001;
xp       = 0.1;


%% light load phase frequency optimization
Lcsi = .01e-9;
fq = linspace(1.5e5, 1.5e6, 10000);
figure(1)
clf
for j = 1:1:length(L)
    pac = interp1(f_sw, p_ac(:,j), fq, 'cubic');
    for i = 1:1:length(fq)
        fsw = fq(i);
        dil = 2.5/L(j)*1/(2*fsw);
        i_crit(i) = dil/2;
        loss_L = pac(i)+r_dcr(j)*i_crit(i)^2;
        io = i_crit(i);

        a = Lcsi*Coss*Vin/Qgd^2;
        b = Rg+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg+Rdrv+Lcsi*(io-dil/2)/Qgs);
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = 0.5*Vin*(io-dil/2)*fsw*(Qgs/Ig1on+Qgd/Ig2on);

        a = Lcsi*Coss*Vin/Qgd^2;
        b = Rg+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg+Rdrv+Lcsi*(io+dil/2)/Qgs);
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = 0.5*Vin*(io+dil/2)*fsw*(Qgs/Ig1off+Qgd/Ig2off);

        Pcond = (io^2+dil^2/12)*Rdson;
        Pgate = 2*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
```

```matlab
        Prr = Qrr*Vin*fsw;
        Poss = 0.5*Coss*Vin^2*fsw;
        loss_sw = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);
        loss_net = loss_L+loss_sw;
        n_crit(i) = i_crit(i)*2.5/(i_crit(i)*2.5+loss_net);
    end

    subplot(2,1,1)
    h1x(j) = semilogx(i_crit , n_crit);
    hold on

    subplot(2,1,2)
    h2x(j) = semilogx(fq/1000, n_crit);
    hold on

    lx{j} = sprintf('%s \\muH',num2str(L(j)*1e6));
    [M, I] = max(n_crit);
    fopt(j) = fq(I);
end

subplot(2,1,1)
xticks([0.1 0.2 0.3 0.5 0.7 1 2 3 4 5 7 10 20])
xlabel('Critical current (A)')
ylabel('Efficiency at critical current')
grid minor
legend(h1x, lx);

subplot(2,1,2)
xticks([1.5e2 2e2 3e2 5e2 1e3 1.5e3])
xlabel('Switching frequency (kHz)')
ylabel('Efficiency at critical current')
grid minor
legend(h2x, lx);

figure(2)
scatter(L*1e6, fopt, 'k')
xticks(L*1e6);
grid minor
title({'Switching frequency for low current phase', 'Optimized for highest ...
    efficiency at critical current'})
xlabel('Inductance \muH');
ylabel('Switching frequency')

figure(3)
clf
figure(4)
clf
k = 1;

Lcsi = csi;
%% 1:1 sharing ratio
L1     = 2*L(5);
L2     = 2*L(5);
fsw1   = 1e6*sqrt(2e-6/L1);
```

```
fsw2    = 1e6*sqrt(2e-6/L2);
I_crit  = 1.8/(fsw1*L1);
loss_L1 = zeros(1000,0);
loss_L2 = zeros(1000,0);

r       = round(L1/L2);
isw     = 2;
flag    = 0;
rsw     = 0.5;
m1      = 1;
m1p     = m1;
m2      = 1;
eff     = zeros(1000,1);

for i = 1:1:1000
    if iout(i) < isw
        iL1(i) = iout(i);
        iL2(i) = 0;
        en1(i) = 1;
        en2(i) = 0;
        nsw    = i;
    else
        iL1(i) = iout(i)*1/(r+1);
        iL2(i) = iout(i)*r/(r+1);
        en1(i) = 1;
        en2(i) = 1;
    end
    loss_L1(i) = 2*interp1(f_sw, p_ac(:,5), fsw1, 'cubic')*(Vin/5)^2+iL1(i)^2*r_dcr(5);
    loss_L2(i) = 2*interp1(f_sw, p_ac(:,5), fsw2, 'cubic')*(Vin/5)^2+iL2(i)^2*r_dcr(5);
    if(iout(i) < I_crit)
        ncrit  = i;
    end
end

for i=1:1:ncrit
    ripv(i)    = 1/(Co*fsw1)*(I_crit-iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

figure(5)
clf
semilogx(iout(1:ncrit), ripv(1:ncrit)/ripv(ncrit))
xlabel('I_{out}')
ylabel('Light Load Ripple (multiple of ripple at critical current)')
grid minor
hold on

count = 0
while(flag==0 && count<10000)
    count = count+1;
    loss_sw1 = zeros(1000,0);
    loss_sw2 = zeros(1000,0);
    m2 = m1;
    for i=1:1:1000
        io = iL1(i);
        fsw = fsw1;
        dil = 2.5/L1/(2*fsw);

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m1+Rdrv+Lcsi/m1*(io-dil/2)/(m1*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m1*Qgs)/Ig1on+(m1*Qgd)/Ig2on)/2;

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m1+Rdrv+Lcsi/m1*(io+dil/2)/(m1*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m1*Qgs)/Ig1off+(m1*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m1;
        Pgate = 2*m1*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m1*Qrr*Vin*fsw;
        Poss = 0.5*m1*Coss*Vin^2*fsw;
        loss_sw1(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);

        io = iL2(i);
        fsw = fsw2;
        dil = vout/L2/(2*fsw);

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m2+Rdrv+Lcsi/m2*(io-dil/2)/(m2*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m2*Qgs)/Ig1on+(m2*Qgd)/Ig2on)/2;

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m2+Rdrv+Lcsi/m2*(io+dil/2)/(m2*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m2*Qgs)/Ig1off+(m2*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m2;
        Pgate = 2*m2*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m2*Qrr*Vin*fsw;
        Poss = 0.5*m2*Coss*Vin^2*fsw;
        loss_sw2(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);
    end
    loss = (loss_L1+loss_sw1).*en1+(loss_L2+loss_sw2).*en2 + rcin*0.5*(iout.*iout);
    for j=1:1:ncrit
        loss(j) = loss(ncrit)*iout(j)/iout(ncrit);
    end
    loss = pstatic + loss;
    pout = iout*vout;
    eff  = pout./(pout+loss);

    crit_eff = eff(ncrit)
    if(count==1)
        crit_eff_d = crit_eff-0.01;
    end

    if(abs(crit_eff-npk)<0.001)
        flag==1;
    elseif(abs(crit_eff-npk)>abs(crit_eff_d-npk))
        if(m1p≤m1) %m1 was increased
            m1  = m1-0.001
        else
            m1  = m1+0.001
        end
    else
        if(m1p≤m1) %m1 was increased
            m1  = m1+0.001
        else
            m1  = m1-0.001
        end
    end
    crit_eff_d = eff(ncrit)
    m1p = m1;
    clc
end

m=m1+m2;

loss_11 = [pstatic loss];

l{k} = sprintf('1:%s , L_1 = %s uH, f_{sw1}=%s kHz, L_2 = %s uH, f_{sw2}=%s kHz, ...
    m1=%s, m2=%s', ...
       num2str(r), num2str(L1*1e6), num2str(round(fsw1/1000)), ...
                   num2str(L2*1e6), num2str(round(fsw2/1000)), ...
                   num2str(m1),     num2str(m2));

for i=1:1:ncrit
    ripv(i)    = 1/(Co*fsw1)*(I_crit-iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

for i=ncrit+1:1:nsw
    ripv(i)    = ripv(ncrit);
end

for i=nsw+1:1:1000
    ripv(i)    = 0.1584/0.125*ripv(ncrit);
end

figure(5)
clf
h5(k) = semilogx(iout(1:nsw), ripv(1:nsw)/ripv(ncrit))
xlabel('I_{out}')
```

```
ylabel('Output Voltage Ripple (multiple of ripple at critical current)')
grid minor
hold on

figure(3)
subplot(2,1,1)
h1(k) = plot(iout(1:1000), eff(1:1000));
hold on
subplot(2,1,2)
h2(k) = plot(iout(1:1000), loss(1:1000));
hold on

figure(4)
subplot(2,1,1)
h3(k) = semilogx(iout(1:1000), eff(1:1000));
hold on
subplot(2,1,2)
h4(k) = loglog(iout(1:1000), loss(1:1000));
hold on

loss11  = loss;
ncrit11 = ncrit;

k = k+1;
L1      = 2*L(6);
L2      = 2*L(4);
fsw1    = 1e6*sqrt(2e-6/L1);
fsw2    = 1e6*sqrt(2e-6/L2);
I_crit  = 1.8/(fsw1*L1);
loss_L1 = zeros(1000,0);
loss_L2 = zeros(1000,0);

r       = round(L1/L2);
isw     = 2;
flag    = 0;
rsw     = 0.5;
m1      = 1;
m1p     = m1;
eff     = zeros(1000,1);

for i = 1:1:1000
    if iout(i) < isw
        iL1(i) = iout(i);
        iL2(i) = 0;
        en1(i) = 1;
        en2(i) = 0;
        nsw    = i;
    else
        iL1(i) = iout(i)*1/(r+1);
        iL2(i) = iout(i)*r/(r+1);
        en1(i) = 1;
        en2(i) = 1;
    end
    loss_L1(i) = 2*interp1(f_sw, p_ac(:,6), fsw1, 'cubic')*(Vin/5)^2+iL1(i)^2*r_dcr(6);
    loss_L2(i) = 2*interp1(f_sw, p_ac(:,4), fsw2, 'cubic')*(Vin/5)^2+iL2(i)^2*r_dcr(4);
    if(iout(i) < I_crit)
        ncrit  = i;
    end
end

count = 0
while(flag==0 && count<10000)
    count = count+1;
    loss_sw1 = zeros(1000,0);
    loss_sw2 = zeros(1000,0);
    m2 = m-m1;
    for i=1:1:1000
        io = iL1(i);
        fsw = fsw1;
        dil = 2.5/L1/(2*fsw);

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m1+Rdrv+Lcsi/m1*(io-dil/2)/(m1*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m1*Qgs)/Ig1on+(m1*Qgd)/Ig2on)/2;

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m1+Rdrv+Lcsi/m1*(io+dil/2)/(m1*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m1*Qgs)/Ig1off+(m1*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m1;
        Pgate = 2*m1*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m1*Qrr*Vin*fsw;
        Poss = 0.5*m1*Coss*Vin^2*fsw;
        loss_sw1(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);

        io = iL2(i);
        fsw = fsw2;
        dil = vout/L2/(2*fsw);

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m2+Rdrv+Lcsi/m2*(io-dil/2)/(m2*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m2*Qgs)/Ig1on+(m2*Qgd)/Ig2on)/2;

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m2+Rdrv+Lcsi/m2*(io+dil/2)/(m2*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m2*Qgs)/Ig1off+(m2*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m2;
        Pgate = 2*m2*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m2*Qrr*Vin*fsw;
        Poss = 0.5*m2*Coss*Vin^2*fsw;
        loss_sw2(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);
    end
    loss = (loss_L1+loss_sw1).*en1+(loss_L2+loss_sw2).*en2 + rcin*0.5*(iout.*iout);
    for j=1:1:ncrit
        loss(j) = loss(ncrit)*iout(j)/iout(ncrit);
    end
    loss = pstatic + loss;
    pout = iout*vout;
    eff  = pout./(pout+loss);

    crit_eff = eff(ncrit)
    if(count==1)
        crit_eff_d = crit_eff-0.01;
    end

    if(abs(crit_eff-npk)<0.001)
        flag==1;
    elseif(abs(crit_eff-npk)>abs(crit_eff_d-npk))
        if(m1p≤m1) %m1 was increased
            m1  = m1-0.001
        else
            m1  = m1+0.001
        end
    else
        if(m1p≤m1) %m1 was increased
            m1  = m1+0.001
        else
            m1  = m1-0.001
        end
    end
    crit_eff_d = eff(ncrit)
    m1p = m1;
    clc
end

clc
loss_12 = [pstatic loss];

l{k} = sprintf('1:%s , L_1 = %s uH, f_{sw1}=%s kHz, L_2 = %s uH, f_{sw2}=%s kHz, ... m1=%s, m2=%s', ...
       num2str(r), num2str(L1*1e6), num2str(round(fsw1/1000)), ...
                   num2str(L2*1e6), num2str(round(fsw2/1000)), ...
                   num2str(m1),     num2str(m2));
for i=1:1:ncrit
    ripv(i)    = 1/(Co*fsw1)*(I_crit-iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

```

```
for i=ncrit+1:1:nsw
    ripv(i)    = ripv(ncrit);
end

for i=nsw+1:1:1000
    ripv(i)    = 0.1584/0.125*ripv(ncrit);
end

figure(5)
h5(k) = semilogx(iout(1:nsw), ripv(1:nsw)/ripv(ncrit))

figure(3)
subplot(2,1,1)
h1(k) = plot(iout(1:1000), eff(1:1000));
hold on
subplot(2,1,2)
h2(k) = plot(iout(1:1000), loss(1:1000));
hold on

figure(4)
subplot(2,1,1)
h3(k) = semilogx(iout(1:1000), eff(1:1000));
hold on
subplot(2,1,2)
h4(k) = loglog(iout(1:1000), loss(1:1000));
hold on

loss12  = loss;
ncrit12 = ncrit;

k = k+1;

%% 1:4 sharing ratio
% inductor losses 0.64uH high current phase and 3.3uH low current phase
L1      = 2*L(7);
L2      = 2*L(3);
fsw1    = 1e6*sqrt(2e-6/L1);
fsw2    = 1e6*sqrt(2e-6/L2);
I_crit  = 1.8/(fsw1*L1);
loss_L1 = zeros(1000,0);
loss_L2 = zeros(1000,0);

r       = round(L1/L2);
isw     = 2;
flag    = 0;
rsw     = 0.5;
m1      = 1;
m1p     = m1;
eff     = zeros(1000,1);

for i = 1:1:1000
    if iout(i) < isw
        iL1(i) = iout(i);
        iL2(i) = 0;
        en1(i) = 1;
        en2(i) = 0;
        nsw    = i;
    else
        iL1(i) = iout(i)*1/(r+1);
        iL2(i) = iout(i)*r/(r+1);
        en1(i) = 1;
        en2(i) = 1;
    end
    loss_L1(i) = 2*interp1(f_sw, p_ac(:,7), fsw1, 'cubic')*(Vin/5)^2+iL1(i)^2*r_dcr(7);
    loss_L2(i) = 2*interp1(f_sw, p_ac(:,3), fsw2, 'cubic')*(Vin/5)^2+iL2(i)^2*r_dcr(3);
    if(iout(i) < I_crit)
        ncrit  = i;
    end
end

for i=1:1:ncrit
    ripv(i)    = 1/(Co*fsw1)*(I_crit-iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

figure(5)
semilogx(iout(1:ncrit), ripv(1:ncrit)/ripv(ncrit))

count = 0
while(flag==0 && count<10000)
    count = count+1;
    loss_sw1 = zeros(1000,0);
    loss_sw2 = zeros(1000,0);
    m2 = m-m1;
    for i=1:1:1000
        io = iL1(i);
        fsw = fsw1;
        dil = 2.5/L1/(2*fsw);

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m1+Rdrv+Lcsi/m1*(io-dil/2)/(m1*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m1*Qgs)/Ig1on+(m1*Qgd)/Ig2on)/2;

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m1+Rdrv+Lcsi/m1*(io+dil/2)/(m1*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m1*Qgs)/Ig1off+(m1*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m1;
        Pgate = 2*m1*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m1*Qrr*Vin*fsw;
        Poss = 0.5*m1*Coss*Vin^2*fsw;
        loss_sw1(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);

        io = iL2(i);
        fsw = fsw2;
        dil = vout/L2/(2*fsw);

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m2+Rdrv+Lcsi/m2*(io-dil/2)/(m2*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m2*Qgs)/Ig1on+(m2*Qgd)/Ig2on)/2;

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m2+Rdrv+Lcsi/m2*(io+dil/2)/(m2*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m2*Qgs)/Ig1off+(m2*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m2;
        Pgate = 2*m2*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m2*Qrr*Vin*fsw;
        Poss = 0.5*m2*Coss*Vin^2*fsw;
        loss_sw2(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);
    end
    loss = (loss_L1+loss_sw1).*en1+(loss_L2+loss_sw2).*en2 + rcin*0.5*(iout.*iout);
    for j=1:1:ncrit
        loss(j) = loss(ncrit)*iout(j)/iout(ncrit);
    end
    loss = pstatic + loss;
    pout = iout*vout;
    eff  = pout./(pout+loss);

    crit_eff = eff(ncrit)
    if(count==1)
        crit_eff_d = crit_eff-0.01;
    end

    if(abs(crit_eff-npk)<0.001)
        flag==1;
    elseif(abs(crit_eff-npk)>abs(crit_eff_d-npk))
        if(m1p≤m1) %m1 was increased
            m1  = m1-0.001
        else
            m1  = m1+0.001
        end
    else
        if(m1p≤m1) %m1 was increased
            m1  = m1+0.001
        else
            m1  = m1-0.001
        end
    end
    crit_eff_d = eff(ncrit)
    m1p = m1;
    clc
end

clc
loss_14 = [pstatic loss];

l{k} = sprintf('1:%s , L_1 = %s uH, f_{sw1}=%s kHz, L_2 = %s uH, f_{sw2}=%s kHz, ... m1=%s, m2=%s', ...
       num2str(r), num2str(L1*1e6), num2str(round(fsw1/1000)), ...
                   num2str(L2*1e6), num2str(round(fsw2/1000)), ...
                   num2str(m1),     num2str(m2));
for i=1:1:ncrit
    ripv(i)     = 1/(Co*fsw1)*(I_crit-iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

for i=ncrit+1:1:nsw
    ripv(i)     = ripv(ncrit);
end

for i=nsw+1:1:1000
    ripv(i)     = 0.1584/0.125*ripv(ncrit);
end

figure(5)
h5(k) = semilogx(iout(1:nsw), ripv(1:nsw)/ripv(ncrit))

figure(3)
subplot(2,1,1)
h1(k) = plot(iout(1:1000), eff(1:1000));
hold on
subplot(2,1,2)
h2(k) = plot(iout(1:1000), loss(1:1000));
hold on

figure(4)
subplot(2,1,1)
h3(k) = semilogx(iout(1:1000), eff(1:1000));
hold on
subplot(2,1,2)
h4(k) = loglog(iout(1:1000), loss(1:1000));
hold on

loss14  = loss;
ncrit14 = ncrit;

k = k+1;

%% 1:8 sharing ratio
% inductor losses 0.64uH high current phase and 3.3uH low current phase
L1      = 2*L(8);
L2      = 2*L(2);
fsw1    = 1e6*sqrt(2e-6/L1);
```

```
fsw2     = 1e6*sqrt(2e-6/L2);
I_crit   = 1.8/(fsw1*L1);
loss_L1  = zeros(1000,0);
loss_L2  = zeros(1000,0);

r        = round(L1/L2);
isw      = 2;
flag     = 0;
rsw      = 0.5;
m1       = 1;
m1p      = m1;
eff      = zeros(1000,1);

for i = 1:1:1000
    if iout(i) < isw
        iL1(i) = iout(i);
        iL2(i) = 0;
        en1(i) = 1;
        en2(i) = 0;
        nsw    = i;
    else
        iL1(i) = iout(i)*1/(r+1);
        iL2(i) = iout(i)*r/(r+1);
        en1(i) = 1;
        en2(i) = 1;
    end
    loss_L1(i) = 2*interp1(f_sw, p_ac(:,8), fsw1, 'cubic')*(Vin/5)^2+iL1(i)^2*r_dcr(8);
    loss_L2(i) = 2*interp1(f_sw, p_ac(:,2), fsw2, 'cubic')*(Vin/5)^2+iL2(i)^2*r_dcr(2);
    if(iout(i) < I_crit)
        ncrit  = i;
    end
end

for i=1:1:ncrit
    ripv(i)    = 1/(Co*fsw1)*(I_crit -iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

figure(5)
semilogx(iout(1:ncrit), ripv(1:ncrit)/ripv(ncrit))

count = 0
while(flag==0 && count<10000)
    count = count+1;
    loss_sw1 = zeros(1000,0);
    loss_sw2 = zeros(1000,0);
    m2 = m-m1;
    for i=1:1:1000
        io = iL1(i);
        fsw = fsw1;
        dil = 2.5/L1/(2*fsw);

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m1+Rdrv+Lcsi/m1*(io-dil/2)/(m1*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m1*Qgs)/Ig1on+(m1*Qgd)/Ig2on)/2;

        a = Lcsi/m1*(m1*Coss)*Vin/(m1*Qgd)^2;
        b = Rg/m1+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m1+Rdrv+Lcsi/m1*(io+dil/2)/(m1*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m1*Qgs)/Ig1off+(m1*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m1;
        Pgate = 2*m1*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m1*Qrr*Vin*fsw;
        Poss = 0.5*m1*Coss*Vin^2*fsw;
        loss_sw1(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);

        io = iL2(i);
        fsw = fsw2;
        dil = vout/L2/(2*fsw);

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vdrv - Vpl;
        Ig1on = c/(Rg/m2+Rdrv+Lcsi/m2*(io-dil/2)/(m2*Qgs));
        Ig2on = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswon = Vin*(io-dil/2)*fsw*((m2*Qgs)/Ig1on+(m2*Qgd)/Ig2on)/2;

        a = Lcsi/m2*(m2*Coss)*Vin/(m2*Qgd)^2;
        b = Rg/m2+Rdrv;
        c = Vpl;
        Ig1off = c/(Rg/m2+Rdrv+Lcsi/m2*(io+dil/2)/(m2*Qgs));
        Ig2off = (-b+sqrt(b^2+4*a*c))/(2*a);
        Pswoff = Vin*(io+dil/2)*fsw*((m2*Qgs)/Ig1off+(m2*Qgd)/Ig2off)/2;

        Pcond = (io^2+dil^2/12)*Rdson/m2;
        Pgate = 2*m2*Qg*Vdrv*fsw;
        Pdt = 2*Vsd*io*fsw*tdead;
        Prr = m2*Qrr*Vin*fsw;
        Poss = 0.5*m2*Coss*Vin^2*fsw;
        loss_sw2(i) = (Pswon+Pswoff+Pcond+Pgate+Pdt+Prr+Poss);
    end
    loss = (loss_L1+loss_sw1).*en1+(loss_L2+loss_sw2).*en2 + rcin*0.5*(iout.*iout);
    for j=1:1:ncrit
        loss(j) = loss(ncrit)*iout(j)/iout(ncrit);
    end
    loss = pstatic + loss;
    pout = iout*vout;
    eff  = pout./(pout+loss);

    crit_eff = eff(ncrit)
    if(count==1)
        crit_eff_d = crit_eff-0.01;
        end

    if(abs(crit_eff-npk)<0.001)
        flag==1;
    elseif(abs(crit_eff-npk)>abs(crit_eff_d-npk))
        if(m1p≤m1) %m1 was increased
            m1  = m1-0.001
        else
            m1  = m1+0.001
        end
    else
        if(m1p≤m1) %m1 was increased
            m1  = m1+0.001
        else
            m1  = m1-0.001
        end
    end
    crit_eff_d = eff(ncrit)
    m1p = m1;
    clc
end

clc
loss_18 = [pstatic loss];

l{k} = sprintf('1:%s , L_1 = %s uH, f_{sw1}=%s kHz, L_2 = %s uH, f_{sw2}=%s kHz, ...
    m1=%s, m2=%s', ...
       num2str(r), num2str(L1*1e6), num2str(round(fsw1/1000)), ...
                   num2str(L2*1e6), num2str(round(fsw2/1000)), ...
                   num2str(m1),     num2str(m2));
for i=1:1:ncrit
    ripv(i)    = 1/(Co*fsw1)*(I_crit-iout(i)+iout(i)*iout(i)/(2*I_crit))/vout;
end

for i=ncrit+1:1:nsw
    ripv(i)    = ripv(ncrit);
end

for i=nsw+1:1:1000
    ripv(i)    = 0.1584/0.125*ripv(ncrit);
end

figure(5)
h5(k) = semilogx(iout(1:nsw), ripv(1:nsw)/ripv(ncrit))
legend(h5, l)

figure(3)
subplot(2,1,1)
h1(k) = plot(iout(1:1000), eff(1:1000));
hold off
grid minor
legend(h1, l)
subplot(2,1,2)
h2(k) = plot(iout(1:1000), loss(1:1000));
```

```
hold off
grid minor
legend(h2, l)

figure(4)
subplot(2,1,1)
h3(k) = semilogx(iout(1:1000), eff(1:1000));
hold off
grid minor
legend(h3, l)
subplot(2,1,2)
h4(k) = loglog(iout(1:1000), loss(1:1000));
hold off
grid minor
legend(h4, l)

loss18  = loss;
ncrit18 = ncrit;
i_out = [0 iout];
```

The loss data generated for different current sharing ratios was used to perform Monte Carlo simulations to obtain averaged system level efficiencies for the DPP converter stack. Uniform distribution with unlimited mismatch, 50% mismatch and 25% mismatch are simulated. The script for plotting averaged system level efficiencies is provided below.

```
iload = logspace(-2,1,100);
npts = 1000;
eff11 = zeros(npts,1);
eff12 = zeros(npts,1);
eff14 = zeros(npts,1);
eff18 = zeros(npts,1);
istack = zeros(npts,1);
avg_eff11 = zeros(length(iload),1);
avg_eff12 = zeros(length(iload),1);
avg_eff14 = zeros(length(iload),1);
avg_eff18 = zeros(length(iload),1);

x = 0.25;

for k=1:1:length(iload);
    k
    for j=1:1:npts
        i   = max(0, min(10, iload(k)*(1-x/2+x*rand(8,1))));
        il1=i(1)-i(2);
        il3=i(3)-i(4);
        il5=i(5)-i(6);
        il7=i(7)-i(8);
        il2=1/2*(i(1)+i(2)-i(3)-i(4));
        il6=1/2*(i(5)+i(6)-i(7)-i(8));
        il4=1/4*(i(1)+i(2)+i(3)+i(4)-i(5)-i(6)-i(7)-i(8));

        loss11 = 1/2*interp1(i_out, loss_11, abs(il1), 'pchip')...
               + 1/2*interp1(i_out, loss_11, abs(il3), 'pchip')...
               + 1/2*interp1(i_out, loss_11, abs(il5), 'pchip')...
               + 1/2*interp1(i_out, loss_11, abs(il7), 'pchip')...
               +     interp1(i_out, loss_11, abs(il2), 'pchip')...
               +     interp1(i_out, loss_11, abs(il6), 'pchip')...
               +   2*interp1(i_out, loss_11, abs(il4), 'pchip');

        loss12 = 1/2*interp1(i_out, loss_12, abs(il1), 'pchip')...
               + 1/2*interp1(i_out, loss_12, abs(il3), 'pchip')...
               + 1/2*interp1(i_out, loss_12, abs(il5), 'pchip')...
               + 1/2*interp1(i_out, loss_12, abs(il7), 'pchip')...
               +     interp1(i_out, loss_12, abs(il2), 'pchip')...
               +     interp1(i_out, loss_12, abs(il6), 'pchip')...
               +   2*interp1(i_out, loss_12, abs(il4), 'pchip');

        loss14 = 1/2*interp1(i_out, loss_14, abs(il1), 'pchip')...
               + 1/2*interp1(i_out, loss_14, abs(il3), 'pchip')...
               + 1/2*interp1(i_out, loss_14, abs(il5), 'pchip')...
               + 1/2*interp1(i_out, loss_14, abs(il7), 'pchip')...
               +     interp1(i_out, loss_14, abs(il2), 'pchip')...
               +     interp1(i_out, loss_14, abs(il6), 'pchip')...
               +   2*interp1(i_out, loss_14, abs(il4), 'pchip');

        loss18 = 1/2*interp1(i_out, loss_18, abs(il1), 'pchip')...
               + 1/2*interp1(i_out, loss_18, abs(il3), 'pchip')...
               + 1/2*interp1(i_out, loss_18, abs(il5), 'pchip')...
               + 1/2*interp1(i_out, loss_18, abs(il7), 'pchip')...
               +     interp1(i_out, loss_18, abs(il2), 'pchip')...
               +     interp1(i_out, loss_18, abs(il6), 'pchip')...
               +   2*interp1(i_out, loss_18, abs(il4), 'pchip');

        pout      = 1.8*sum(i);
        eff11(j)  = pout/(pout+loss11);
        eff12(j)  = pout/(pout+loss12);
        eff14(j)  = pout/(pout+loss14);
        eff18(j)  = pout/(pout+loss18);
        istack(j) = sum(i)/8;
    end
    avg_eff11(k)  = sum(eff11)/length(eff11);
    avg_eff12(k)  = sum(eff12)/length(eff12);
    avg_eff14(k)  = sum(eff14)/length(eff14);
    avg_eff18(k)  = sum(eff18)/length(eff18);
    avg_iload(k)  = sum(istack)/length(istack);

    clc
end

figure(1)
clf
h(1) = semilogx(avg_iload, avg_eff11)
l{1} = sprintf('DPP converters with 1:1 sharing ratio');
hold on
h(2) = semilogx(avg_iload, avg_eff12)
```

```
l{2} = sprintf('DPP converters with 1:2 sharing ratio');
h(3) = semilogx(avg_iload, avg_eff14)
l{3} = sprintf('DPP converters with 1:4 sharing ratio');
h(4) = semilogx(avg_iload, avg_eff18)
l{4} = sprintf('DPP converters with 1:8 sharing ratio');
legend(h, l)
xlabel('I_{stack} (A)')
ylabel('\eta_{stack}')
grid minor
```

APPENDIX B

ANALYTICAL AND SWITCHING MODELS FOR SENSORLESS CURRENT MODE CONTROL

The following MATLAB script was used to perform frequency response of switching models of the two phase stack converter under peak and sensorless current mode control.

```
clear
tsim = 4.01e-2;
dt   = 1e-8;
nw  = 1000;
npts = round(tsim/dt);
t    = linspace(0,tsim,npts);
dt   = t(2)-t(1);

%parameters
L    = 22e-6;
rl   = 20e-3;
C    = 100e-6;
rc   = 0.001;
kp   = 10;
ki   = 150000;
Ts   = 4e-6;
fs   = 1/Ts;
Ri   = 1;
M2   = 14.4/L;
Ma   = M2/4;
s    = tf([1 0],[1]);
Vin  = 48;
Vout = 14.4;
sn   = Ri*(Vin-Vout)/L;
sf   = Ri*(Vout)/L;
se   = sf/4;
D    = Vout/Vin;
zc   = rc+1/s/C;
zl   = rl+s*L;

%initialization
vin      = 48*ones(1,npts);
vref     = 14.4*ones(1,npts);
io       = zeros(1,npts);
iL1      = zeros(1,npts);
iL2      = zeros(1,npts);
vc       = ones(1,npts)*vref(1);
```

```
vo      = ones(1,npts)*vref(1);
iLe1    = zeros(1,npts);
iLe2    = zeros(1,npts);
u1      = 1;
u2      = 0;
int_err = 0;
s1      = zeros(1,npts);
s1(1)   = 1;
s2      = zeros(1,npts);
r1      = zeros(1,npts);
r2      = zeros(1,npts);
ramp1   = 0.5*ones(1,npts);
ramp2   = 0.5*zeros(1,npts);
ns      = round(Ts/dt);
ncyc    = round(npts/ns);
iLref1  = 0;
iLref2  = 0;
for k = 1:1:npts-1
    if(floor((k+1)/ns)>floor(k/ns))
        s1(k+1)     = 1;
        ramp1(k+1) = 0.5;
    else
        ramp1(k+1) = ramp1(k)-1/ns;
    end
    if(floor((k+1)/ns+0.5)>floor(k/ns+0.5))
        s2(k+1)=1;
        ramp2(k+1) = 0.5;
    else
        ramp2(k+1) = ramp2(k)-1/ns;
    end
end
ramp1 = Ma*ramp1*Ts;
ramp2 = Ma*ramp2*Ts;

figure(4)
clf

for k=1:1:10
    se      = sf/k;
    gvc     = fs/Ri/s*(1-exp(-s*Ts))/((sn+se)/(sn+sf)+(sf-se)/(sn+sf)*exp(-s*Ts));
    gvg     = ...
        (D-fs/s*(1-exp(-s*D*Ts))/((sn+se)/(sn+sf)+(sf-se)/(sn+sf)*exp(-s*Ts)))/(L*s);
    gvref   = ((1-exp(-s*Ts))/((sn+se)/(sn+sf)+(sf-se)/(sn+sf)*exp(-s*Ts))*fs/s-1)/(L*s);
    gc      = (exp(-s*Ts/2))*(kp+ki/s)*(1-exp(-s*Ts/2))/(s*Ts/2);
    f       = 2;

    LG_pcm = gc*gvc*(f*zc)/(1-f*zc*gvref);
    LG_scm = gc*gvc*(f*zc)/(1+f*zc/zl);
    f_i = 2.5*logspace(0,4.69897,nw);
    w_i = 2*pi*f_i;
    ana_LG_pcm = freqresp(LG_pcm, w_i);
    ana_LG_scm = freqresp(LG_scm, w_i);

    subplot(2,1,1)
    semilogx(f_i, 20*log(abs(squeeze(ana_LG_scm))), 'b')
    hold on
    semilogx(f_i, 20*log(abs(squeeze(ana_LG_pcm))), 'r')

    subplot(2,1,2)
    semilogx(f_i, unwrap(angle(squeeze(ana_LG_scm)))*180/pi, 'b')
    hold on
    semilogx(f_i, unwrap(angle(squeeze(ana_LG_pcm)))*180/pi, 'r')
end

subplot(2,1,1)
plot(f_i, zeros(1,nw))
grid minor
xlabel('Frequency (Hz)')
ylabel('|Loop Gain|')
xlim([min(f_i), max(f_i)])

subplot(2,1,2)
plot(f_i, -180*ones(1,nw))
xlabel('Frequency (Hz)')
ylabel('Loop Gain (phase) (degree)')
grid minor
xlim([min(f_i), max(f_i)])

se     = sf/4;
gvc    = fs/Ri/s*(1-exp(-s*Ts))/((sn+se)/(sn+sf)+(sf-se)/(sn+sf)*exp(-s*Ts));
gvg    = (D-fs/s*(1-exp(-s*D*Ts))/((sn+se)/(sn+sf)+(sf-se)/(sn+sf)*exp(-s*Ts)))/(s*L);
gvref  = ((1-exp(-s*Ts))/((sn+se)/(sn+sf)+(sf-se)/(sn+sf)*exp(-s*Ts))*fs/s-1)/(s*L);
gc     = (exp(-s*Ts/2))*(kp+ki/s)*(1-exp(-s*Ts))/(1-exp(-s*Ts/2))/2;
f      = 2;

%% load transient
% ttran = tsim/2;
% itran = 10;
% ntran = round(ttran/tsim*npts);
% for k=ntran:1:npts
%     io(k) = itran;
% end
%
% for k=2:1:npts
%     iL1(k)   = iL1(k-1)  + ...
    1/L*(vin(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
%     iL2(k)   = iL2(k-1)  + 1/L*(vin(k)*u2-rc*iL1(k)  ...
    -(rl+rc)*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
%     vc(k)    = vc(k-1)   + 1/C*(iL1(k)+iL2(k)-io(k))*dt;
%     vo(k)    = vc(k)     + rc*(iL1(k)+iL2(k)-io(k));
%     iLe1(k)  = iLe1(k-1) + 1/L*(vin(k)*u1-rl*iLe1(k-1)-vref(k))*dt;
%     iLe2(k)  = iLe2(k-1) + 1/L*(vin(k)*u2-rl*iLe2(k-1)-vref(k))*dt;
%     if(s1(k)==1)
%         err  = vref(k) - vo(k);
%         int_err = int_err + err*Ts/2;
%         iLref1 = kp*err + ki*int_err;
%     elseif(s2(k)==1)
%         err  = vref(k) - vo(k);
%         int_err = int_err + err*Ts/2;
%         iLref2 = kp*err + ki*int_err;
%     end
%     ic1      = iLref1 + ramp1(k);
%     ic2      = iLref2 + ramp2(k);
%
%     if(iLe1(k)>ic1)
%         r1(k) = 1;
%     else
%         r1(k) = 0;
%     end
%
%     if(iLe2(k)>ic2)
%         r2(k) = 1;
%     else
%         r2(k) = 0;
%     end
%
%     if(u1==0 && s1(k)==1)
%         u1 = 1;
%     elseif(u1==1 && r1(k)==1)
%         u1 = 0;
%     end
%
%     if(u2==0 && s2(k)==1)
%         u2 = 1;
%     elseif(u2==1 && r2(k)==1)
%         u2 = 0;
%     end
% end

%% output impedance test

f_i = 2.5*logspace(1,5,nw);
T_i = round((1./f_i)*round(1/dt))*dt;

% analytical model
zo_pcm   = -zc/(1+f*zc*(gc*gvc-gvref));
zo_scm   = -zc/(1+f*zc/zl+f*zc*gvc*gc);

w_i = 2*pi./T_i;
ana_Z_pcm   = freqresp(zo_pcm, w_i);
ana_Z_scm   = freqresp(zo_scm, w_i);
% switching model
for j=1:1:nw
    j
    iop  = io+0.1*sin(2*pi*t/T_i(j));
    ioq  = io+0.1*cos(2*pi*t/T_i(j));
    if(T_i(j)≥4e-3)
        n_cyc_fourier = 1;
    elseif(T_i(j)≥4e-4)
        n_cyc_fourier = 10;
    elseif(T_i(j)≥4e-5)
        n_cyc_fourier = 100;
    else
        n_cyc_fourier = 1000;
    end
    t_cyc_fourier = n_cyc_fourier*T_i(j);
    n_win_fourier = round(t_cyc_fourier/dt);

    %numerical integration SCM
    for k=2:1:npts

        iL1(k)    = iL1(k-1)  + ...
            1/L*(vin(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*iop(k))*dt;
        iL2(k)    = iL2(k-1)  + 1/L*(vin(k)*u2-rc*iL1(k)   ...
            -(rl+rc)*iL2(k-1)-vc(k-1)+rc*iop(k))*dt;
        vc(k)     = vc(k-1)   + 1/C*(iL1(k)+iL2(k)-iop(k))*dt;
        vo(k)     = vc(k)     + rc*(iL1(k)+iL2(k)-iop(k));
        iLe1(k)   = iLe1(k-1) + 1/L*(vin(k)*u1-rl*iLe1(k-1)-vref(k))*dt;
        iLe2(k)   = iLe2(k-1) + 1/L*(vin(k)*u2-rl*iLe2(k-1)-vref(k))*dt;
        err       = vref(max(1,k-round(ns/2))) - vo(max(1,k-round(ns/2)));
        int_err   = int_err + err*dt;

        if(s1(k)==1)
            iLref1 = kp*err+ki*int_err;
        elseif(s2(k)==1)
            iLref2 = kp*err+ki*int_err;
        end


        ic1       = iLref1 + ramp1(k);
        ic2       = iLref2 + ramp2(k);

        if(iLe1(k)>ic1)
            r1(k) = 1;
        else
            r1(k) = 0;
        end

        if(iLe2(k)>ic2)
            r2(k) = 1;
        else
            r2(k) = 0;
        end

        if(u1==0 && s1(k)==1)
            u1 = 1;
        elseif(u1==1 && r1(k)==1)
            u1 = 0;
        end

        if(u2==0 && s2(k)==1)
            u2 = 1;
        elseif(u2==1 && r2(k)==1)
            u2 = 0;
        end

    end

    int_ip_win   = sum(iop(npts-n_win_fourier:npts).*(vo(npts-n_win_fourier:npts)-...
                   sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_op_win   = sum(ioq(npts-n_win_fourier:npts).*(vo(npts-n_win_fourier:npts)-...
                   sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_ip2_win  = sum(iop(npts-n_win_fourier:npts).*iop(npts-n_win_fourier:npts));
    int_iq2_win  = sum(ioq(npts-n_win_fourier:npts).*ioq(npts-n_win_fourier:npts));
    Zip          = int_ip_win/int_ip2_win;
    Ziq          = int_op_win/int_iq2_win;
    cmp_Z_scm(j) = Zip+Ziq*i;

    %numerical integration PCM
    for k=2:1:npts

        iL1(k)  = iL1(k-1) + ...
            1/L*(vin(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*iop(k))*dt;
        iL2(k)  = iL2(k-1) + 1/L*(vin(k)*u2-rc*iL1(k)  ...
            -(rl+rc)*iL2(k-1)-vc(k-1)+rc*iop(k))*dt;
        vc(k)   = vc(k-1)  + 1/C*(iL1(k)+iL2(k)-iop(k))*dt;
        vo(k)   = vc(k)    + rc*(iL1(k)+iL2(k)-iop(k));
        err     = vref(max(1,k-round(ns/2))) - vo(max(1,k-round(ns/2)));
        int_err = int_err + err*dt;

        if(s1(k)==1)
            iLref1 = kp*err+ki*int_err;
        elseif(s2(k)==1)
            iLref2 = kp*err+ki*int_err;
        end

        ic1      = iLref1 + ramp1(k);
        ic2      = iLref2 + ramp2(k);

        if(iL1(k)>ic1)
            r1(k) = 1;
        else
            r1(k) = 0;
        end

        if(iL2(k)>ic2)
            r2(k) = 1;
        else
            r2(k) = 0;
        end

        if(u1==0 && s1(k)==1)
            u1 = 1;
        elseif(u1==1 && r1(k)==1)
            u1 = 0;
        end

        if(u2==0 && s2(k)==1)
            u2 = 1;
        elseif(u2==1 && r2(k)==1)
```

```
            u2 = 0;
        end

    end

    int_ip_win  = sum(iop(npts-n_win_fourier:npts).*(vo(npts-n_win_fourier:npts)-...
                sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_op_win  = sum(ioq(npts-n_win_fourier:npts).*(vo(npts-n_win_fourier:npts)-...
                sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_ip2_win  = sum(iop(npts-n_win_fourier:npts).*iop(npts-n_win_fourier:npts));
    int_iq2_win  = sum(ioq(npts-n_win_fourier:npts).*ioq(npts-n_win_fourier:npts));
    Zip          = int_ip_win/int_ip2_win;
    Ziq          = int_op_win/int_iq2_win;
    cmp_Z_pcm(j) = Zip+Ziq*i;

    clc
end

figure(1)
clf

subplot(2,1,1)
loglog(1./T_i, abs(cmp_Z_scm))
hold on
loglog(1./T_i, abs(cmp_Z_pcm))
loglog(1./T_i, abs(squeeze(ana_Z_scm)))
loglog(1./T_i, abs(squeeze(ana_Z_pcm)))
grid minor
xlabel('Frequency (Hz)')
ylabel('|Z_{out}| (\Omega)')
xlim([min(1./T_i), max(1./T_i)])

subplot(2,1,2)
semilogx(1./T_i, unwrap(angle(cmp_Z_scm))*180/pi)
hold on
semilogx(1./T_i, unwrap(angle(cmp_Z_pcm))*180/pi)
plot(1./T_i, unwrap(angle(squeeze(ana_Z_scm)))*180/pi)
plot(1./T_i, unwrap(angle(squeeze(ana_Z_pcm)))*180/pi)
xlabel('Frequency (Hz)')
ylabel('Z_{out} (phase) (degree)')
grid minor
xlim([min(1./T_i), max(1./T_i)])

%% audio susceptibility test
f_i = 2.5*logspace(2,5,nw);
T_i = round((1./f_i)*round(1/dt))*dt;

% analytical model
audio_pcm = f*gvg/(1/zc+f*(gc*gvc-gvref));
audio_scm = f*gvg/(1/zc+f/zl+f*gc*gvc);

w_i = 2*pi./T_i;
ana_audio_pcm   = freqresp(audio_pcm, w_i);
ana_audio_scm   = freqresp(audio_scm, w_i);
```

```

for j=1:1:nw
    j
    vgp  = vin+0.5*sin(2*pi*t/T_i(j));
    vgq  = vin+0.5*cos(2*pi*t/T_i(j));
    if(T_i(j)≥4e-3)
        n_cyc_fourier = 1;
    elseif(T_i(j)≥4e-4)
        n_cyc_fourier = 10;
    elseif(T_i(j)≥4e-5)
        n_cyc_fourier = 100;
    else
        n_cyc_fourier = 1000;
    end
    t_cyc_fourier = n_cyc_fourier*T_i(j);
    n_win_fourier = round(t_cyc_fourier/dt);

    %numerical integration SCM
    for k=2:1:npts

        iL1(k) = iL1(k-1) + ...
            1/L*(vgp(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        iL2(k) = iL2(k-1) + 1/L*(vgp(k)*u2-rc*iL1(k)  ...
            -(rl+rc)*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        vc(k)  = vc(k-1)  + 1/C*(iL1(k)+iL2(k)-io(k))*dt;
        vo(k)  = vc(k)    + rc*(iL1(k)+iL2(k)-io(k));
        iLe1(k) = iLe1(k-1) + 1/L*(vgp(k)*u1-rl*iLe1(k-1)-vref(k))*dt;
        iLe2(k) = iLe2(k-1) + 1/L*(vgp(k)*u2-rl*iLe2(k-1)-vref(k))*dt;
        err = vref(max(1,k-round(ns/2))) - vo(max(1,k-round(ns/2)));
        int_err = int_err + err*dt;

        if(s1(k)==1)
            iLref1 = kp*err+ki*int_err;
        elseif(s2(k)==1)
            iLref2 = kp*err+ki*int_err;
        end

        ic1      = iLref1 + ramp1(k);
        ic2      = iLref2 + ramp2(k);


        if(iLe1(k)>ic1)
            r1(k) = 1;
        else
            r1(k) = 0;
        end

        if(iLe2(k)>ic2)
            r2(k) = 1;
        else
            r2(k) = 0;
        end

        if(u1==0 && s1(k)==1)
```

```
            u1 = 1;
        elseif(u1==1 && r1(k)==1)
            u1 = 0;
        end

        if(u2==0 && s2(k)==1)
            u2 = 1;
        elseif(u2==1 && r2(k)==1)
            u2 = 0;
        end

    end

    int_vgip_win = ...
        sum((vgp(npts-n_win_fourier:npts)-48).*(vo(npts-n_win_fourier:npts)-...
                 sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vgop_win = ...
        sum((vgq(npts-n_win_fourier:npts)-48).*(vo(npts-n_win_fourier:npts)-...
                 sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vgp2_win = ...
        sum((vgp(npts-n_win_fourier:npts)-48).*(vgp(npts-n_win_fourier:npts)-48));
    int_vgq2_win = ...
        sum((vgq(npts-n_win_fourier:npts)-48).*(vgq(npts-n_win_fourier:npts)-48));
    gvgp          = int_vgip_win/int_vgp2_win;
    gvgq          = int_vgop_win/int_vgq2_win;
    audio_sw_scm(j)    = gvgp+i*gvgq;

    %numerical integration PCM
    for k=2:1:npts

        iL1(k) = iL1(k-1) + ...
            1/L*(vgp(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        iL2(k) = iL2(k-1) + 1/L*(vgp(k)*u2-rc*iL1(k)   ...
            -(rl+rc)*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        vc(k)  = vc(k-1)  + 1/C*(iL1(k)+iL2(k)-io(k))*dt;
        vo(k)  = vc(k)    + rc*(iL1(k)+iL2(k)-io(k));
        err    = vref(max(1,k-round(ns/2))) - vo(max(1,k-round(ns/2)));
        int_err = int_err + err*dt;

        if(s1(k)==1)
            iLref1  = kp*err+ki*int_err;
        elseif(s2(k)==1)
            iLref2  = kp*err+ki*int_err;
        end

        ic1      = iLref1 + ramp1(k);
        ic2      = iLref2 + ramp2(k);


        if(iL1(k)>ic1)
            r1(k) = 1;
        else
            r1(k) = 0;
        end

        if(iL2(k)>ic2)
            r2(k) = 1;
        else
            r2(k) = 0;
        end

        if(u1==0 && s1(k)==1)
            u1 = 1;
        elseif(u1==1 && r1(k)==1)
            u1 = 0;
        end

        if(u2==0 && s2(k)==1)
            u2 = 1;
        elseif(u2==1 && r2(k)==1)
            u2 = 0;
        end

    end

    int_vgip_win = ...
        sum((vgp(npts-n_win_fourier:npts)-48).*(vo(npts-n_win_fourier:npts)-...
                 sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vgop_win = ...
        sum((vgq(npts-n_win_fourier:npts)-48).*(vo(npts-n_win_fourier:npts)-...
                 sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vgp2_win = ...
        sum((vgp(npts-n_win_fourier:npts)-48).*(vgp(npts-n_win_fourier:npts)-48));
    int_vgq2_win = ...
        sum((vgq(npts-n_win_fourier:npts)-48).*(vgq(npts-n_win_fourier:npts)-48));
    gvgp         = int_vgip_win/int_vgp2_win;
    gvgq         = int_vgop_win/int_vgq2_win;
    audio_sw_pcm(j) = gvgp+i*gvgq;

    clc
end

figure(2)
clf

subplot(2,1,1)
loglog(1./T_i, abs(audio_sw_scm))
hold on
loglog(1./T_i, abs(audio_sw_pcm))
loglog(1./T_i, abs(squeeze(ana_audio_scm)))
loglog(1./T_i, abs(squeeze(ana_audio_pcm)))
grid minor
xlabel('Frequency (Hz)')
ylabel('|G_{vg}|')
xlim([min(1./T_i), max(1./T_i)])

subplot(2,1,2)
semilogx(1./T_i, unwrap(angle(audio_sw_scm))*180/pi)
```

```
hold on
semilogx(1./T_i, unwrap(angle(audio_sw_pcm))*180/pi)
semilogx(1./T_i, unwrap(angle(squeeze(ana_audio_scm)))*180/pi)
semilogx(1./T_i, unwrap(angle(squeeze(ana_audio_pcm)))*180/pi)
xlabel('Frequency (Hz)')
ylabel('G_{vg} (phase) (degree)')
grid minor
xlim([min(1./T_i), max(1./T_i)])

%% reference tracking test
f_i = 2.5*logspace(2,4.69897,nw);
T_i = round((1./f_i)*round(1/dt))*dt;

% analytical model
reft_pcm = (f*zc*gc*gvc)/(1-f*zc*gvref+f*zc*gc*gvc);
reft_scm = (f*zc*gc*gvc+f*zc*gvref+f*zc/zl)/(1+f*zc/zl+f*zc*gvc*gc);

w_i = 2*pi./T_i;
ana_reft_pcm   = freqresp(reft_pcm, w_i);
ana_reft_scm   = freqresp(reft_scm, w_i);

for j=1:1:nw
    j
    vrefp  = vref+0.01*sin(2*pi*t/T_i(j));
    vrefq  = vref+0.01*cos(2*pi*t/T_i(j));
    if(T_i(j)≥4e-3)
        n_cyc_fourier = 1;
    elseif(T_i(j)≥4e-4)
        n_cyc_fourier = 10;
    elseif(T_i(j)≥4e-5)
        n_cyc_fourier = 100;
    else
        n_cyc_fourier = 1000;
    end
    t_cyc_fourier = n_cyc_fourier*T_i(j);
    n_win_fourier = round(t_cyc_fourier/dt);

    %numerical integration SCM
    for k=2:1:npts

        iL1(k) = iL1(k-1) + ...
            1/L*(vin(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        iL2(k) = iL2(k-1) + 1/L*(vin(k)*u2-rc*iL1(k)  ...
            -(rl+rc)*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        vc(k)  = vc(k-1)  + 1/C*(iL1(k)+iL2(k)-io(k))*dt;
        vo(k)  = vc(k)    + rc*(iL1(k)+iL2(k)-io(k));
        iLe1(k) = iLe1(k-1) + 1/L*(vin(k)*u1-rl*iLe1(k-1)-vrefp(k))*dt;
        iLe2(k) = iLe2(k-1) + 1/L*(vin(k)*u2-rl*iLe2(k-1)-vrefp(k))*dt;
        err     = vrefp(max(1,k-round(ns/2))) - vo(max(1,k-round(ns/2)));
        int_err = int_err + err*dt;

        if(s1(k)==1)
            iLref1 = kp*err+ki*int_err;
        elseif(s2(k)==1)
```

```
            iLref2 = kp*err+ki*int_err;
        end

        ic1      = iLref1 + ramp1(k);
        ic2      = iLref2 + ramp2(k);


        if(iLe1(k)>ic1)
            r1(k) = 1;
        else
            r1(k) = 0;
        end

        if(iLe2(k)>ic2)
            r2(k) = 1;
        else
            r2(k) = 0;
        end

        if(u1==0 && s1(k)==1)
            u1 = 1;
        elseif(u1==1 && r1(k)==1)
            u1 = 0;
        end

        if(u2==0 && s2(k)==1)
            u2 = 1;
        elseif(u2==1 && r2(k)==1)
            u2 = 0;
        end

    end

    int_vrip_win = ...
        sum((vrefp(npts-n_win_fourier:npts)-14.4).*(vo(npts-n_win_fourier:npts)-...
                 sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vrop_win = ...
        sum((vrefq(npts-n_win_fourier:npts)-14.4).*(vo(npts-n_win_fourier:npts)-...
                 sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vrp2_win = ...
    sum((vrefp(npts-n_win_fourier:npts)-14.4).*(vrefp(npts-n_win_fourier:npts)-14.4));
    int_vrq2_win = ...
    sum((vrefq(npts-n_win_fourier:npts)-14.4).*(vrefq(npts-n_win_fourier:npts)-14.4));
    grefp        = int_vrip_win/int_vrp2_win;
    grefq        = int_vrop_win/int_vrq2_win;
    reft_sw_scm(j) = grefp+i*grefq;

    %numerical integration PCM
    for k=2:1:npts

        iL1(k) = iL1(k-1) + ...
            1/L*(vin(k)*u1-(rl+rc)*iL1(k-1)-rc*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        iL2(k) = iL2(k-1) + 1/L*(vin(k)*u2-rc*iL1(k)  ...
            -(rl+rc)*iL2(k-1)-vc(k-1)+rc*io(k))*dt;
        vc(k)  = vc(k-1)  + 1/C*(iL1(k)+iL2(k)-io(k))*dt;
        vo(k)  = vc(k)    + rc*(iL1(k)+iL2(k)-io(k));
        err    = vrefp(max(1,k-round(ns/2))) - vo(max(1,k-round(ns/2)));
        int_err = int_err + err*dt;

        if(s1(k)==1)
            iLref1 = kp*err+ki*int_err;
        elseif(s2(k)==1)
            iLref2 = kp*err+ki*int_err;
        end

        ic1      = iLref1 + ramp1(k);
        ic2      = iLref2 + ramp2(k);


        if(iL1(k)>ic1)
            r1(k) = 1;
        else
            r1(k) = 0;
        end

        if(iL2(k)>ic2)
            r2(k) = 1;
        else
            r2(k) = 0;
        end

        if(u1==0 && s1(k)==1)
            u1 = 1;
        elseif(u1==1 && r1(k)==1)
            u1 = 0;
        end

        if(u2==0 && s2(k)==1)
            u2 = 1;
        elseif(u2==1 && r2(k)==1)
            u2 = 0;
        end

    end

    int_vrip_win = ...
        sum((vrefp(npts-n_win_fourier:npts)-14.4).*(vo(npts-n_win_fourier:npts)-...
                  sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vrop_win = ...
        sum((vrefq(npts-n_win_fourier:npts)-14.4).*(vo(npts-n_win_fourier:npts)-...
                  sum(vo(npts-n_win_fourier:npts))/length(vo(npts-n_win_fourier:npts))));
    int_vrp2_win = ...
    sum((vrefp(npts-n_win_fourier:npts)-14.4).*(vrefp(npts-n_win_fourier:npts)-14.4));
    int_vrq2_win = ...
    sum((vrefq(npts-n_win_fourier:npts)-14.4).*(vrefq(npts-n_win_fourier:npts)-14.4));
    grefp        = int_vrip_win/int_vrp2_win;
    grefq        = int_vrop_win/int_vrq2_win;
    reft_sw_pcm(j) = grefp+i*grefq;

    clc
end

figure(3)
clf

subplot(2,1,1)
loglog(1./T_i, abs(reft_sw_scm))
hold on
loglog(1./T_i, abs(reft_sw_pcm))
loglog(1./T_i, abs(squeeze(ana_reft_scm)))
loglog(1./T_i, abs(squeeze(ana_reft_pcm)))
grid minor
xlabel('Frequency (Hz)')
ylabel('|G_{vref}|')
xlim([min(1./T_i), max(1./T_i)])

subplot(2,1,2)
semilogx(1./T_i, unwrap(angle(reft_sw_scm)*180/pi))
hold on
semilogx(1./T_i, unwrap(angle(reft_sw_pcm)*180/pi))
semilogx(1./T_i, unwrap(angle(squeeze(ana_reft_scm))*180/pi))
semilogx(1./T_i, unwrap(angle(squeeze(ana_reft_pcm))*180/pi))
xlabel('Frequency (Hz)')
ylabel('G_{vref} (phase) (degree)')
grid minor
xlim([min(1./T_i), max(1./T_i)])
```

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