NANOSCALE ELECTRONIC DEVICES BASED ON THE HYBRID STACKS OF TWO-DIMENSIONAL MATERIALS AND FERROELECTRIC METAL OXIDES

BY

JIALUN LIU

DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2020

Urbana, Illinois

Doctoral Committee:

Professor Joseph W. Lyding, Chair
Assistant Professor Wenjuan Zhu, Director of Research
Professor Xiuling Li
Associate Professor Qing Cao

Abstract

Further scaling of complementary metal-oxide-semiconductor (CMOS) dimensions will soon lead to a tremendous rise in power consumption while limited gain in the performance of integrated circuits. “Beyond-CMOS” devices, based on two-dimensional (2D) materials, can potentially overcome these limitations and further improve the performance, reduce energy consumption, and add novel functionalities to the CMOS platform. In this Ph.D. dissertation, we investigated energy efficient electronic devices based on a new hybrid material platform consisting of two-dimensional materials and ferroelectric metal oxides. The ferroelectric metal oxides provide programmable and non-volatile doping in the 2D materials, while the atomically thin body in 2D materials enables strong electrostatic control over the channel by the polarized ferroelectric metal oxides.

We design and demonstrate a new type of classifier using ferroelectric graphene transistors, which can perform the “comparison” function in the analog domain instead of the traditional digital domain. This new type of classifier utilizes the ambipolar transport and zero bandgap of the graphene to perform the absolute difference function, |A-B|, directly. Unlike the image classifier based on silicon CMOS, the classifier based on ferroelectric graphene transistors only needs ONE transistor per pixel, which will significantly reduce chip area and energy consumption. More importantly, the embedded ferroelectric layer in the graphene transistor enables the non-volatile storage of the target image inside the analog device. Therefore, a single graphene transistor can perform both image storage and comparison functions concurrently. This in-memory computing will eliminate the need for frequent image loading/unloading, which will further reduce the power consumption related to the data transfer.

We also explored non-volatile reconfigurable devices based on the hybrid stacks of ferroelectric materials and 2D materials. In traditional silicon CMOS, once the device is fabricated, its function is fixed as either an n-type or a p-type transistor. In this work, we show that functionality of this new type of device can be dynamically reconfigured during operation and the reconfiguration is non-volatile and reprogrammable. We have successfully demonstrated the electrostatic controlled reconfigurable devices based on black phosphorus and non-volatile reconfigurable devices based on molybdenum telluride and ferroelectric hafnium zirconium oxides. These reconfigurable devices will enable the logic circuits to evolve their functions on-demand. The 3D monolithic integration of these reconfigurable devices/circuits and memory blocks will enable in-memory computing and reduce the energy consumption and latency related to the transportation of "Big Data".

This work will open a new path toward the design of novel nano-function circuits based on unique material properties that are absent in traditional circuits based on CMOS logic transistors and Von Neumann architectures. These new devices will also enable a new computing paradigm, where the process latency and energy consumption will no longer be limited by the memory bottleneck.

Acknowledgments

Firstly, I would like to deliver my most sincere gratitude to my graduate research adviser, Prof. Wenjuan Zhu, for letting me join her research group to pursue my Ph.D. degree. Her tireless guidance and encouragement have undoubtedly been the greatest support to my academic life in the University of Illinois. I would like to express my appreciation to my teammates, Dr. Kai Xu and Hojoon Ryu, for their kind and constructive suggestions during my projects. I also appreciate the help from my doctoral committee, for their suggestions and approval for my research progress throughout the preliminary exam and final defense. I would also like to thank the ECE Department advising and editorial service staff for their professional advice and service during my completion of this work. Finally, thanks to my family, my love, and my friends for their care and support.

We would like to acknowledge the support from the National Science Foundation (NSF) under Grants ECCS 16-11279 and ECCS 16-53241 CAR, from the Office of Naval Research (ONR) under grant NAVY N00014-17-1-2973.

Table of Contents

Chapter 1 Introduction

The art of field-effect semiconductor devices is to use the electric field as a "switch" to control the current's on/off state. Following Moore's law [1], since the 1960s the semiconductor industry has been scaling down semiconductor devices and lowering their cost while improving the electrical performance and increasing the integrated circuit (IC) density. Various structural/material innovations (SOI, FINFET, high-K gate dielectrics, strained silicon, etc.) and lithography techniques (DUV/EUV, immersion lithography, double patterning, etc.) have been invented and they successfully maintain this trend of scaling down semiconductors. From 1971 to 2014, the typical semiconductor manufacturing process was driven from 10μm to 14nm node for metal-oxide-semiconductor field-effect transistors (MOSFETs) [2], the building blocks for most of today's consumer electronics. Nevertheless, a further device miniaturization/speed-up is exceptionally challenging given nanoscale physical limitations and high development cost. Specifically, shrunken channel length with higher doping undermines the control of the top gate of the channel over the source/drain [3]. Typically these short-channel effects (SCEs) lead to drain-induced barrier lowering (DIBL), carrier surface scattering, hot electron effects and other undesired side-effects [4]. Electron mobility in silicon, severely degraded by surface roughness, is also inevitably affected by heavy doping in short-channel cases. Innovations in materials and structures are required to extend Moore's law, as many have suggested. Further scaling of complementary metal-oxide-semiconductor (CMOS) dimensions will soon lead to a tremendous rise in power consumption while limited gain in the performance of integrated circuits. "Beyond-CMOS" devices, based on nanowires, nanorods, and two-dimensional (2D)

materials, can potentially overcome these limitations and further improve the performance, reduce energy consumption, and add novel functionalities to the CMOS platform. In this project, we investigated energy efficient electronic devices based on a new hybrid material platform consisting of 2D materials and ferroelectric metal oxides. The ferroelectric metal oxides provide programmable and non-volatile doping in the 2D materials, while the atomically thin body in 2D materials enables strong electrostatic control over the channel by the polarized ferroelectric metal oxides. In this chapter, we will review the background in 2D and ferroelectric material fields.

1.1 2D Materials

2D materials are layered materials with strong covalent bonds in the layer while weak van der Waals bonds in between layers. There are several hundreds of 2D materials, which have been predicted or experimentally demonstrated. Among those 2D materials, graphene, transitional dichalcogenides, and black phosphorus are the most intensely studied materials. Graphene has exceptionally high mobility ($\sim$ 200,000 $cm^2/$ ($V{\cdot}s$) [5], but zero bandgap, which makes it difficult to be used in logic devices. Graphene based radio frequency (RF) devices have very high cut-off frequencies (up to 427 GHz) [6], but limited power gain, again due to the lack of a bandgap. After graphene as an atomic layer was discovered, transistors made from it showed extraordinary mobility among other merits [7]. Although graphene's zero semi-metallic behavior brings about low switchability for transistors, this group of materials is recognized as important for potential applications in novel devices. For this reason, graphene and other 2D materials developed later with similar structure have

aroused interest. In addition to digital logic devices, 2D materials with a high surface-to-bulk ratio are naturally ideal for sensors with high sensitivity (e.g. biomedical sensors, piezoelectric sensors). Their sheet-like property suggests their suitability in flexible electronic applications beyond organic flexible electronics [8]. 2D materials are a relatively new and rapidly growing field of study, with new material findings and device breakthroughs emerging rapidly. Still, issues like large-scale production and doping remain challenging in the exploration.

Beyond graphene, transition metal dichalcogenides (TMDs) are another type of 2D material. TMDs have a general formula of MX_2, where M is a transition metal atom (such as Ti, Zr, Hf, V, Nb, Ta, Re, etc.) and X is a chalcogen atom (such as S, Se, Te). There are over 30 different TMDs with diverse properties, ranging from semiconductors (MoS_2, WSe_2) to semimetals (1T' phase WTe_2 and $TiSe_2$), metals (VSe_2, NbS_2), and superconductors ($PbTe_2$, $NbSe_2$) [9-24]. Among various TMDs, $MoTe_2$ is a promising material with small bandgap (0.88 eV in bulk, 1.02 eV in monolayer). This small bandgap makes it possible to fabricate ambipolar transistors and reconfigurable logic devices. In addition to MoTe2, black phosphorus is also a promising material for reconfigurable device due to its small bandgap ($\sim$ 0.3 eV in bulk).

For our main research focus in electronic devices, several kinds of 2D materials of interest are briefly reviewed in this section.

1.1.1 Graphene

Graphene was the very first two-dimensional atomic crystal discovered [7] and its 2D structure gives it properties very different from those of other allotropes of carbon (graphite, Fullerene, carbon nanotube, etc.) [25]. A scanning tunneling microscope (STM) image for graphene atomic structure is shown in Fig. 1-1 [26]. Its advantages include superior mechanical strength, high electronic and thermal conductivity, and impermeability to gases, which attracts a lot of attention for potential applications. Since researchers successfully exfoliated single-layer graphene from its bulk counterpart (graphite) with its main contributor winning the Nobel Prize later in 2010, its enticing electrical properties have encouraged extensive research into making electronic devices beyond the current complementary metal oxide semiconductor (CMOS) technology. Graphene, a semi-metallic carbon layer with one atom thickness, has superior carrier density and mobility ~ 10,000 $cm^2/(V \cdot s)$ and therefore is promising for lower energy dissipation and faster operating speed in electronics. Unfortunately, besides large-scale growth issues, the inherent gapless nature

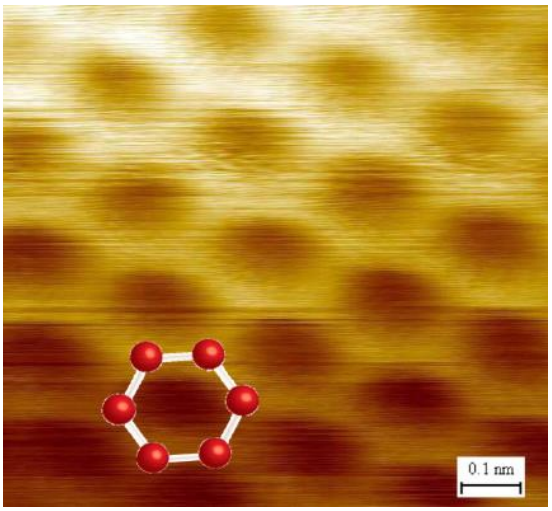

Figure 1-1. Graphene's honeycomb structure shown in STM topographic image.

in graphene restricts the energy states variety and brings about great challenges for people to switch graphene on/off for digital device applications [8]. Cutting graphene into nanoribbons or depositing graphene onto certain substrates is done to show the structure change, hence non-zero bandgap, in graphene. But these changes are overall insignificant and damage graphene's appealing carrier transport properties, or turn out to need further investigation [27-30].

Despite this drawback for digital applications, graphene shows exciting prospects for conductive coating for flexible electronics due to its transparency, flexibility, low sheet resistance and high transmittance, provided contact resistance issues can be appropriately addressed. In addition, graphene-based transistors have proved promising for RF devices with high cut-off frequencies [31]. On the other hand, graphene's transparency in one or a few layers and its wavelength-independent absorption rate in a large range of light spectra make it a suitable candidate for a number of photonic devices. These include photodetectors, various kinds of laser devices, and optical modulators [8].

As an important factor to be considered for industrial products incorporation, production methods (Fig. 1-2 [8]) for large-scale and uniform graphene are great challenges in current development. For research purposes, mechanical exfoliation from bulk graphite is used frequently for graphene and other 2D materials for its convenience and high-quality flakes. An alternative common way to yield graphene is to grow it on copper or nickel with a mixture of methane and hydrogen at as high as 1000 ˚C [32, 33]. Another method includes precipitation of graphene layer on SiC wafer but is very costly [34].

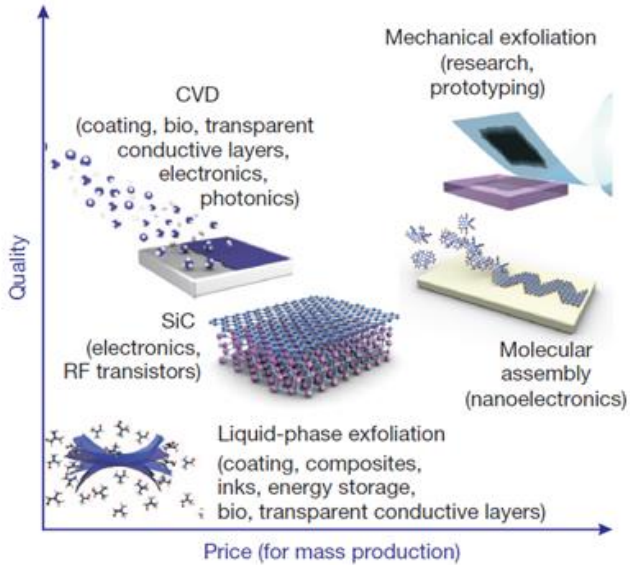

Figure 1-2. Different methods for mass synthesis/production of graphene.

1.1.2 2D Transition Metal Dichalcogenides

Two-dimensional transition metal dichalcogenides (TMDC) have chemical formula MX_2 with transition element M and chalcogen X [35]. Among this group of materials MoS_2, WS_2, and WSe_2 have been studied in recent years for their high quality and stability in the isolation process. Like graphene, these materials can be readily exfoliated into one or a few layers by breaking the interlayer weak van der Waals force without damaging intralayer covalent bonds (mechanical cleavage), or they can be grown by chemical vaporization deposition (CVD). As a representative example, a large area of atomic layer MoS_2 is often synthesized on a silicon wafer by CVD using MoO_3 and S powder with the help of PTAS as seeding material for nucleation. Figure 1-3 [36, 37] demonstrates the structure of MoS_2 layers.

As the thickness decreases to a single layer, the band structure of TMDCs is changed by quantum confinement effects. A transition from indirect bandgap (1.2 eV) at Γ point to direct bandgap (1.9 eV) at K-point in the Brillouin zone is predicted and confirmed for MoS_2. This suggests its appealing properties in possible logic devices and optoelectronics. A top-gated single-layer MoS_2 FET was successfully fabricated in 2011 by Radisavljevic et al. [37] with appreciable mobility ($\sim 70\ cm^2/(V{\cdot}s)$), large on/off current ratio ($\sim 10^8$) and satisfactory subthreshold swing ($\sim$ 74 mV/decade) at room temperature (Fig. 1-4 [37]).

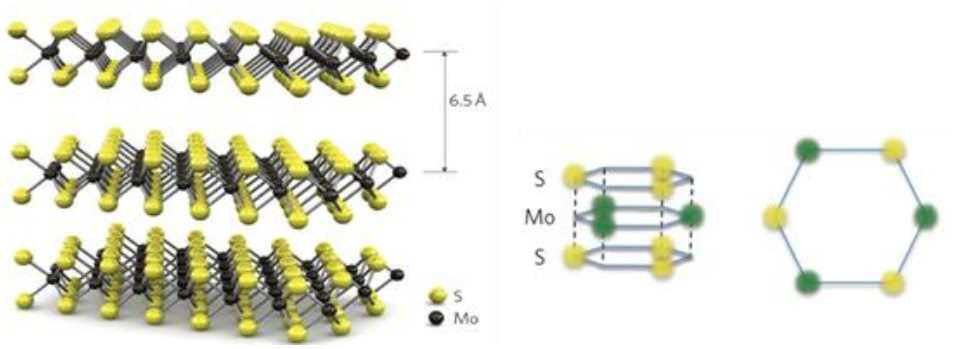

Figure 1-3. Honeycomb MoS_2 structures with alternating Mo and S atoms.

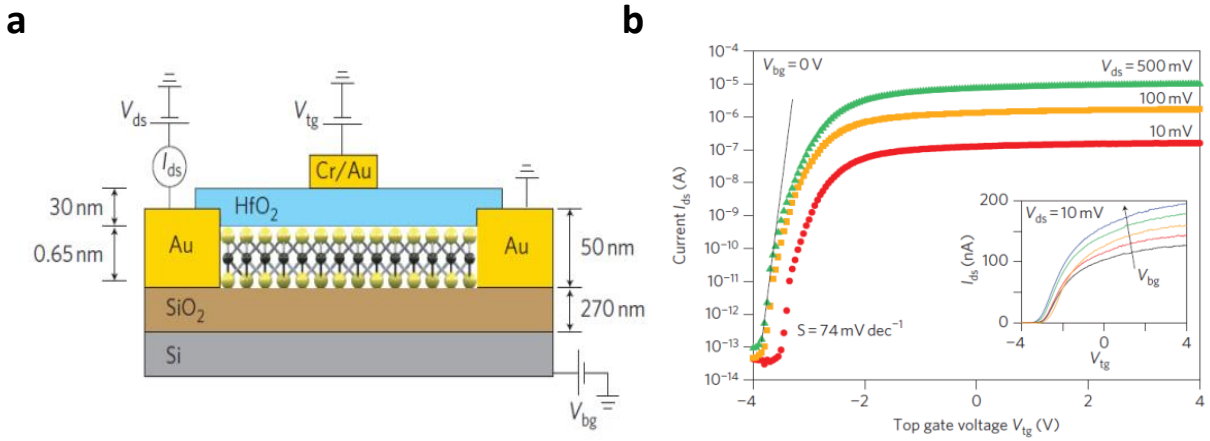

Figure 1-4. A single-layer MoS_2 top-gated FET. (a) Device structure. (b) I-V characteristics.

Despite the inherent p or n type body by impurity charges, progress toward doping the TMDCs in a controllable way was made by several groups utilizing chemical treatment during/after crystal growth, for electronics fabrication with reliability and repeatability [38].

The various bandgap range of the TMDC family and its layer structure free of surface dangling bonds also provide exciting possibilities for applications based on epitaxy and heterostructure/junctions. The various direct bandgap values and tunable features with layer numbers in visible light range also make TMDC optoelectronics attractive [39]. A phototransistor was made by single-layer (SL) MoS_2 to show its potential as a photodetector with photo responsivity of 880 A/W at 561 nm wavelength light [40]. Finally, due to TMDC's M-X composition, the piezoelectric effect was examined in SL MoS_2 thin films, with the finding that no net piezoelectric effect is present within even number of layers or bulk counterparts due to the opposite orientation of alternating layers [41].

Within MoS_2, a strong Fermi-level pinning effect is present, and it mostly demonstrates n-type unipolar characteristics around the conduction band [42, 43]. Tungsten diselenide (WSe_2), with two layers of Se atoms sandwiching a single layer of W atoms is another addition to the TMDC family studied in these years. Unlike MoS_2, WSe_2 could exhibit ambipolar carrier conduction from the effective Fermi level tuning relative to conduction and valence band edge [44-46]. A technique to facilitate the ambipolar transport is to utilize the contact metal engineering, where the source and drain of the FET device are deposited with different metals, each aligned closer to either conduction or valence band and favored for one of the carriers. An example ambipolar WSe_2 device with different contact electrodes is made by S. Das and J. Appenzeller (Fig. 1-5 and Fig. 1-6 [47]).

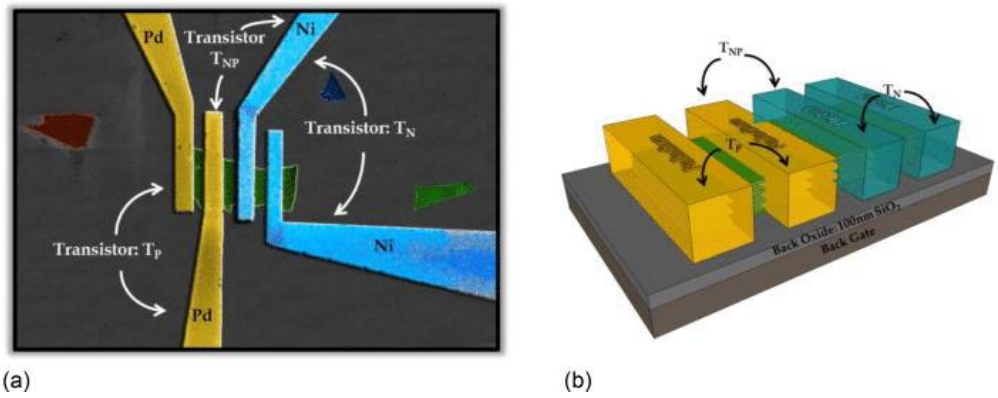

Figure 1-5. (a) SEM and (b) 3D structure of multilayer WSe_2 hetero-contact transistors. T_N:Ni is used for both the source and the drain contact electrode; T_P:Pd is used for both the source and the drain contact electrode; and T_{NP}:Ni is used as the source, and Pd is used as the drain contact electrode.

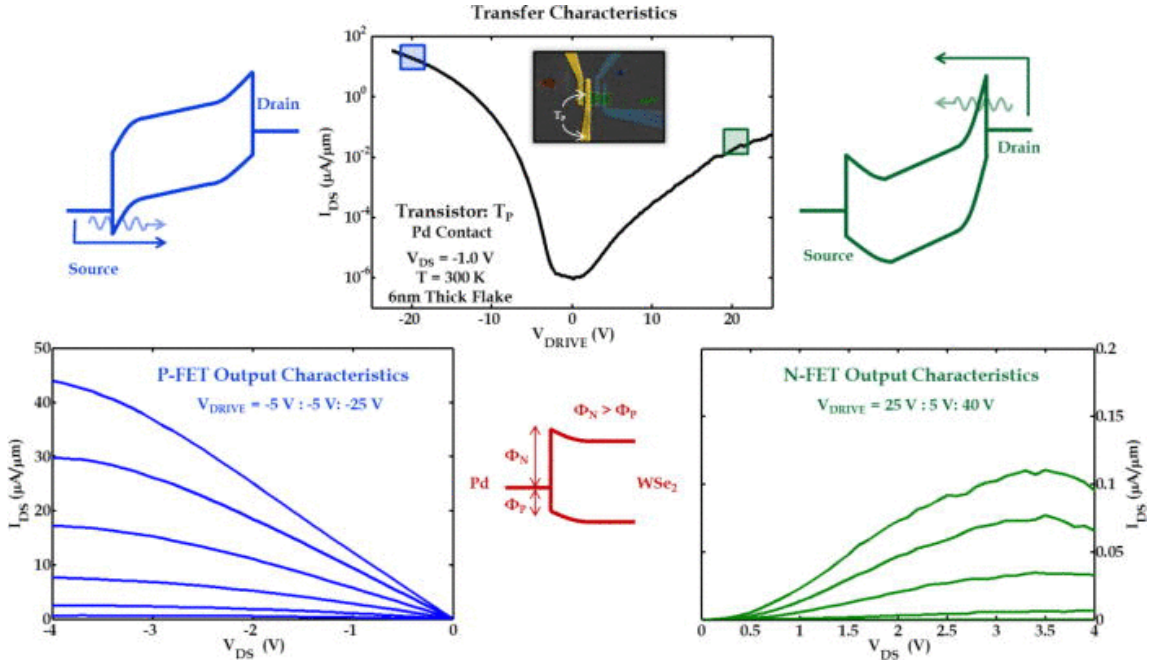

Figure 1-6. Transfer and output characteristics of the transistor T_P and the associated energy band diagram for the electron (green) and the hole (blue) injection. The energy band diagram in red shows the relative Schottky barrier heights for the electron and the hole injection from Pd contact to WSe_2.

Another TMDC, molybdenum ditelluride ($MoTe_2$), has a direct bandgap at ~ 1.1 eV at the single-layer limit, smaller than the corresponding value ~ 1.6 eV of WSe_2 [48, 49]. This suggests a potential higher barriers to suppress carrier injection in WSe_2 [50] and a

facilitated ambipolar transport in $MoTe_2$ [51]. Without the impeding fermi-level pinning effect, these two materials have adjustable barrier heights for n or p carriers depending on flake thickness, contact metal and other factors.

1.1.3 Black Phosphorus

Compared to its allotropes (yellow/red/fibrous phosphorus), black phosphorus is most dense and least reactive due to its interlinked six-membered ring. This unique puckered hexagonal structure (Fig. 1-7 [52]) leads to anisotropic in-plane electrical and optical properties, which may offer special benefits in novel fields such as plasmonic devices [52]. Bulk black phosphorus has a direct bandgap around 0.3 eV, while single-layer black phosphorus is predicted to have a much larger bandgap from 1 eV to 2 eV, depending on the theory model. This large variation indicates black phosphorus might be an ideal candidate for purposes requiring tunable bandgap. Another notable point is this bandgap range corresponds to the infrared range in the optical spectrum. Combined with other 2D materials' optical range from the bandgap, heterostructures could be made for optoelectronics like high-efficiency solar cells. Black phosphorus used in devices is usually exfoliated from bulk crystal which could be made from red phosphorus under high temperature and/or high pressure although some innovative methods (including CVD) also exist [53-55].

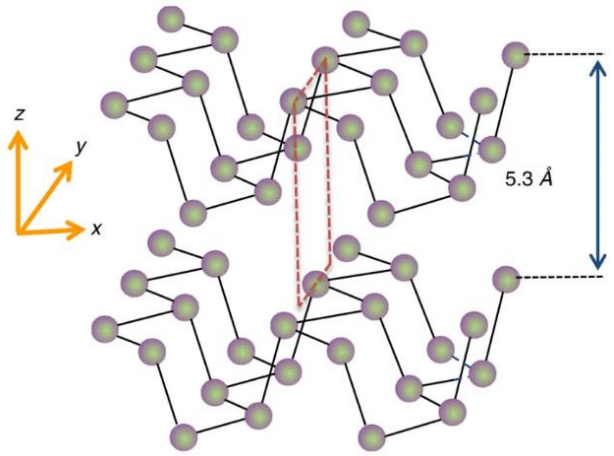

Figure 1-7. Puckered sheets of linked phosphorus atoms. Layer-to-layer space is ~ 0.5nm.

Back-gated FETs were fabricated by several independent groups [52, 56, 57]. In Figure 1-8 [57], experimental data from the Zhang group shows that a p-type FET device with 5nm thick BP channel is fabricated with ~ 200 $cm^2/(V \cdot s)$ mobility with good on/off ratio at 10^5. As a comparison, the data here suggests the black phosphorus FET has higher

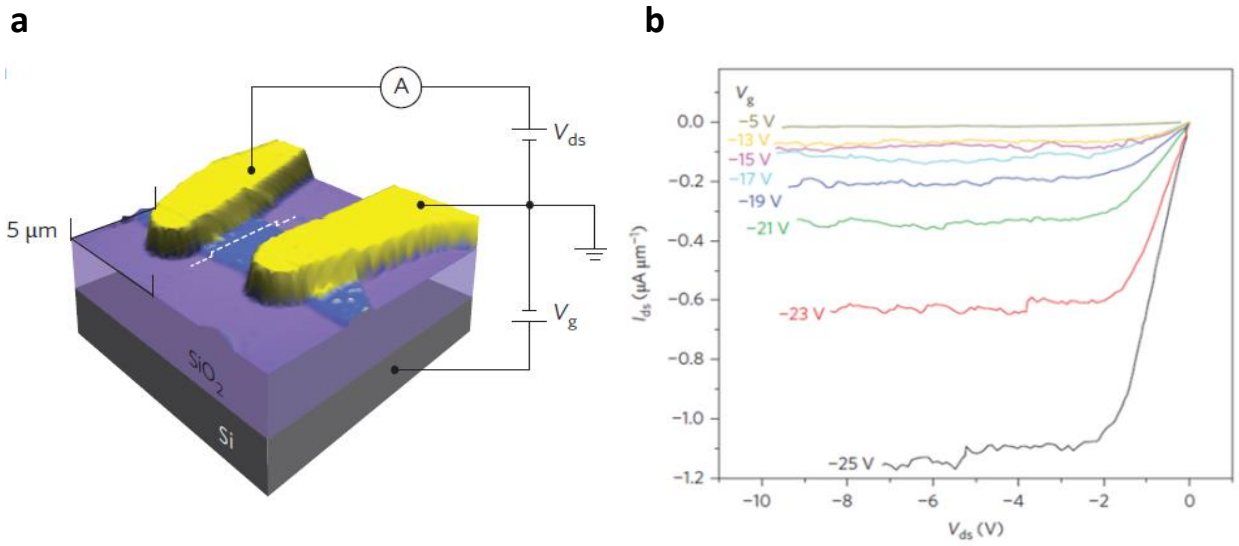

Figure 1-8. (a) A BP back gated transistor. (b) I_d-V_d curves under different gate bias.

mobility than that of a typical TMDC transistor while having a moderate (lower) on/off ratio.

However, instability might be an issue for making black phosphorus thin film devices since a few layers of black phosphorus gradually react with water and oxygen (Fig. 1-9 [58]). Some recent experiments have assessed its surface reaction with the ambient environment and further work is expected to reveal this unstable nature of the material [59].

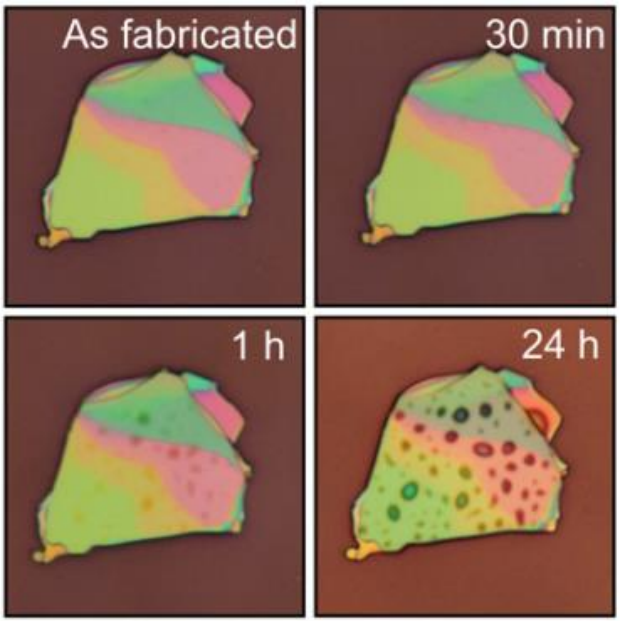

Figure 1-9. Optical images for mechanically exfoliated black phosphorus as time elapses.

1.1.4 Hexagonal Boron Nitride

Hexagonal boron nitride (hBN) is a III-V compound insulator with a wide indirect bandgap around 6 eV [60]. It has a similar honeycomb structure to graphene except it is composed of alternating boron and nitrogen atoms. The hBN also has good mechanical strength and thermal/chemical stability. More importantly, it is experimentally suggested that graphene and other 2D semiconductors demonstrate remarkable mobility with hBN compared to other dielectrics due to their flat and low-impurity surfaces [61]. For these

reasons, hBN is widely used as dielectric material or physical protection coating in 2D material transistors and heterostructures [62-65].

The first CVD growth of monolayer hBN was developed by Kong's group in 2012, using ammonia borane as precursor under LPCVD on copper foil [66]. Other CVD growth methods for hBN also exist using precursors such as borazine [67]. Figure 1-10 consists of an AFM image of hBN [62] and a graphene-hBN transistor device demonstration [63].

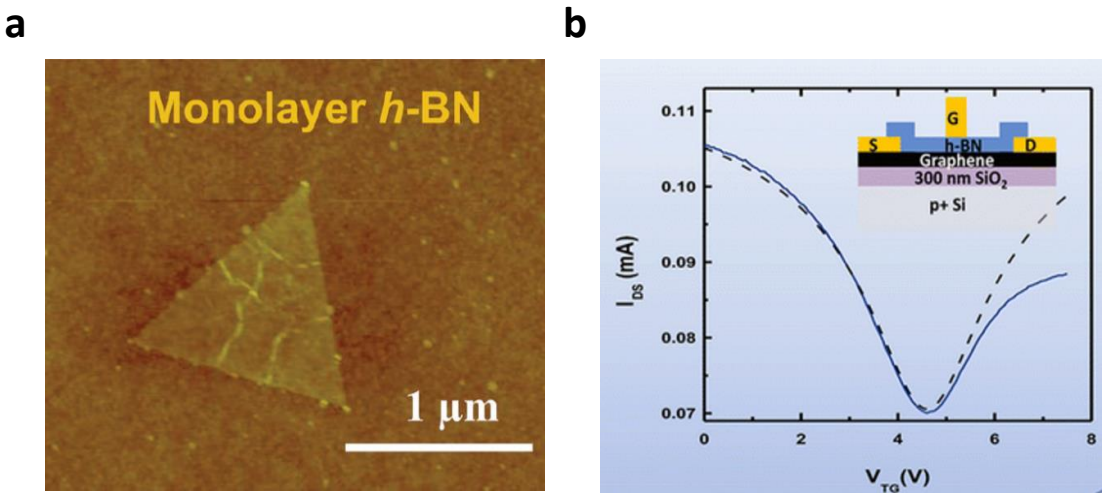

Figure 1-10. (a) CVD-grown hBN under AFM scanning. (b) Graphene transistor structure and transfer characteristics with hBN as top gate dielectric.

1.2 Ferroelectric Materials

1.2.1 Polarization in Ferroelectric Materials

As an important feature of ferroelectric material, the spontaneous polarization in ferroelectric (FE) material is a non-volatile property. The polarization value could be used to represent different states in the layer and the distributed charge could electrically interact

with the nearby material. In this section, a brief explanation for the origin of ferroelectricity is presented.

Material's electrical polarity is reflected by the separation of the positive and negative charges within, called electrical dipole moment. A pair of positive and negative charge (+q and -q) separated by distance d has polarization pointing from negative charge to positive charge with amplitude P = qd (Fig. 1-11a). Polarization introduces an electric field. For a capacitor with dielectric between two metal plates, if external electric field E_0 is applied between the two plates, uniform polarization $P = \chi\varepsilon_0 E$ would be induced, where χ is the material's dielectric susceptibility. Within the dielectric, depolarization field E_1 is generated against the external field due to the induced polarization (Fig. 1-11b). The polarizability of material could be attributed to different factors: electronic polarization (displacements between nucleus and electronic shell), ionic polarization (displacements between ions), dipolar polarization (change of molecules with permanent dipole moment in electric field), and interfacial polarization (accumulation of charge at interface between materials or regions) [68-70].

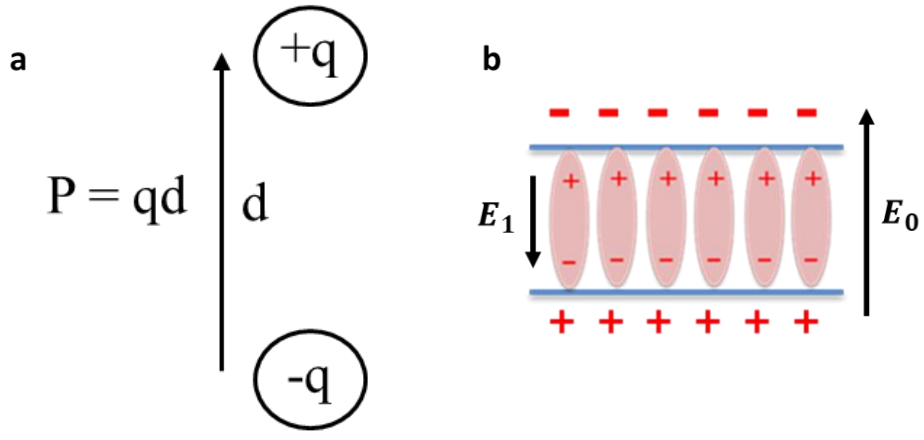

Figure 1-11. (a) Demonstration of electric polarization's magnitude and direction. (b) Polarization induced in capacitor.

Ferroelectric materials are characterized as materials which exhibit robust and reversible spontaneous electrical polarization. The word “spontaneous” may mean that the polarization has a nonzero value in the absence of an applied electric field [68], which distinguish it from normal dielectric material. Ferroelectricity is a subset of pyroelectricity which describes spontaneous dielectric polarization from change of temperature [71]. If the dielectric material in external electrical field is normal dielectric, polarization within will disappear upon removal of the external field. However, if the dielectric is ferroelectric, partial polarization would remain even after the removal of external field if the field was large enough to orient the domains within it, and its amplitude and direction could depend both current external field and its previous state. Figure 1-12 exhibits a P – E diagram with double sweep of external electric field, which would indicate hysteresis if the dielectric material is ferroelectric, while a simple linear relationship is found if the dielectric material is non-ferroelectric.

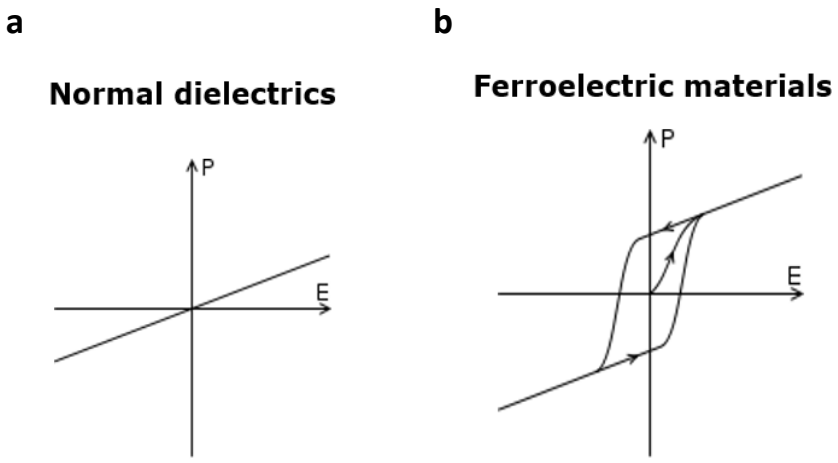

Figure 1-12. P-E diagram for (a) normal and (b) ferroelectric material with direction of hysteresis labeled.

Ferroelectric materials have three important metrics, which are discussed as follows [68, 72]:

1. Remanent polarization (P_r): As we introduced, the polarization's direction and amplitude within ferroelectric material domains could be switched or changed by the external field. When the external field drops to zero, ferroelectric material remains polarized and this remaining polarization is called remanent polarization (P_r) [73]. Remanent polarization depends on the polarization states prior to external field application, and the applied external field's shape, amplitude, width, etc. A field with an amplitude higher than coercive field is required to "flip" and switch part or all of the domains' polarization in ferroelectric material. An external field lower than coercive voltage would not change the remanent polarization since only field-induced polarization is present and it disappears after field removal (like in normal dielectric layer).

2. Retention: The dipoles within ferroelectric layer tends to relax and depolarize as time elapses and remanent polarization decreases. Retention describes the ability of ferroelectric layer to retain the sign and magnitude of remanent polarization after writing with external field [74]. Retention time describes the duration a ferroelectric layer could maintain its remanent polarization until it drops to zero. The retention of a ferroelectric layer in a capacitor structure not only depends on the composition of the ferroelectric material and working environment (e.g. temperature), but also on the adjacent materials.

3. Endurance: For storage purposes, a ferroelectric layer needs to be written into different states (represented by the direction and amount of polarization). After repetitive writing pulses, ferroelectric material is subject to potential "fatigue effect" (a lowered

remanent polarization after repetitive writing pulses) and may even break down, losing its ferroelectric properties. Endurance measures the number of cycles of consecutive opposite writing with pulses above coercive voltage that the ferroelectric layer could sustain before breaking down.

Ferroelectric materials were discovered in 1920 in the form of bulk single crystals of Rochelle salt. Traditional oxide ferroelectric materials include $NH_4H_2PO_4$ (ADP), KH_2PO_4 (KDP), $LiNbO_3$ (LN), $LiTaO_3$ (LT), $BaTiO_3$ (BT), $PbTiO_3$ (PT), Pb (Zr,Ti) O_3 (PZT), (Pb,La)TiO_3 (PLT), $SrBi_2Ta_2O_9$ (SBT) and (Pb,La)(Zr,Ti)O_3 (PLZT)), etc., developed in the form of bulk single-crystal and bulk polycrystalline ceramics. Various techniques (MBE, PVD, CVD) could be used for ferroelectric thin film deposition [75]. In addition to complex oxides, ferroelectric materials are also found in other material classes, like polymer (Polyvinylidene fluoride, or PVDF) and 2D materials ($CuInP_2S_6$ and In_2Se_3). Ferroelectric materials usually only demonstrated their ferroelectric properties below certain temperature (Curie temperature) [68]. Nowadays, traditional ferroelectric materials mainly refer to complex perovskites, such as lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), and lead magnesium niobate-lead titanate (PMN-PT). They have been widely used in ferroelectric devices [76, 77]. However, these traditional ferroelectric materials have a limitation in thickness scaling and are not compatible with CMOS processes. In the last few years, doped metal oxides, including hafnium oxide (HfO_2) and zirconium oxide (ZrO_2), were found to have ferroelectric phase [78-84]. Ferroelectric HfO_2 has the advantages of a high coercive field, excellent scalability (down to 2.5nm), and good compatibility with CMOS processing [84-87].

1.2.2 PUND Measurement

The polarization of the ferroelectric capacitors is commonly measured using the positive-up–negative-down (PUND) method. The capacitors are subjected to a series of five pulses consisting of a preset pulse, positive switching pulse, positive non-switching pulse, negative switching pulse and a negative non-switching pulse, illustrated in Fig. 1-13a. The preset pulse set the ferroelectric HfO_2 in negative spontaneous polarization $-P_s$ state. The first positive pulse applied (P) will switch the polarization vector to $+P_s$ state and the displacement current for this "switching" pulse will be [88]:

$$i_s(t) = \frac{\partial D}{\partial t} = \frac{\partial(\epsilon E + P)}{\partial t} \tag{1-1}$$

where P is the polarization due to the ferroelectric dipoles, E is the electric field, and ϵ is the dielectric constant of the dielectric. Since the film already polarized positively $+P_s$, applying the second positive pulse (U) will not switch the polarization, and displacement current for this "non-switching" pulse will be:

$$i_{ns}(t) = \frac{\partial(\epsilon E)}{\partial t} \tag{1-2}$$

The difference between the two currents will be given by:

$$\Delta i(t) = i_s(t) - i_{ns}(t) = \frac{\partial P(t)}{\partial t} \tag{1-3}$$

Then the positive polarization ($+P_r$) can be extracted from $P(t) = \int_0^t \Delta i(t)dt$ (Fig. 1-13 b [89]). Negative polarization ($-P_r$) is measured with same logic from N and D pulses. An example pulse diagram and P – E diagram are shown below (Fig. 4-13c [74]), where $+P_r$ and $-P_r$ indicates positive and negative remanent polarization, respectively, P_s refers to saturation polarization (when all the domains are polarized in one direction and no more

ferroelectric polarizarion could be added), and $+E_c$ and $-E_c$ means positive and negative coercive voltage.

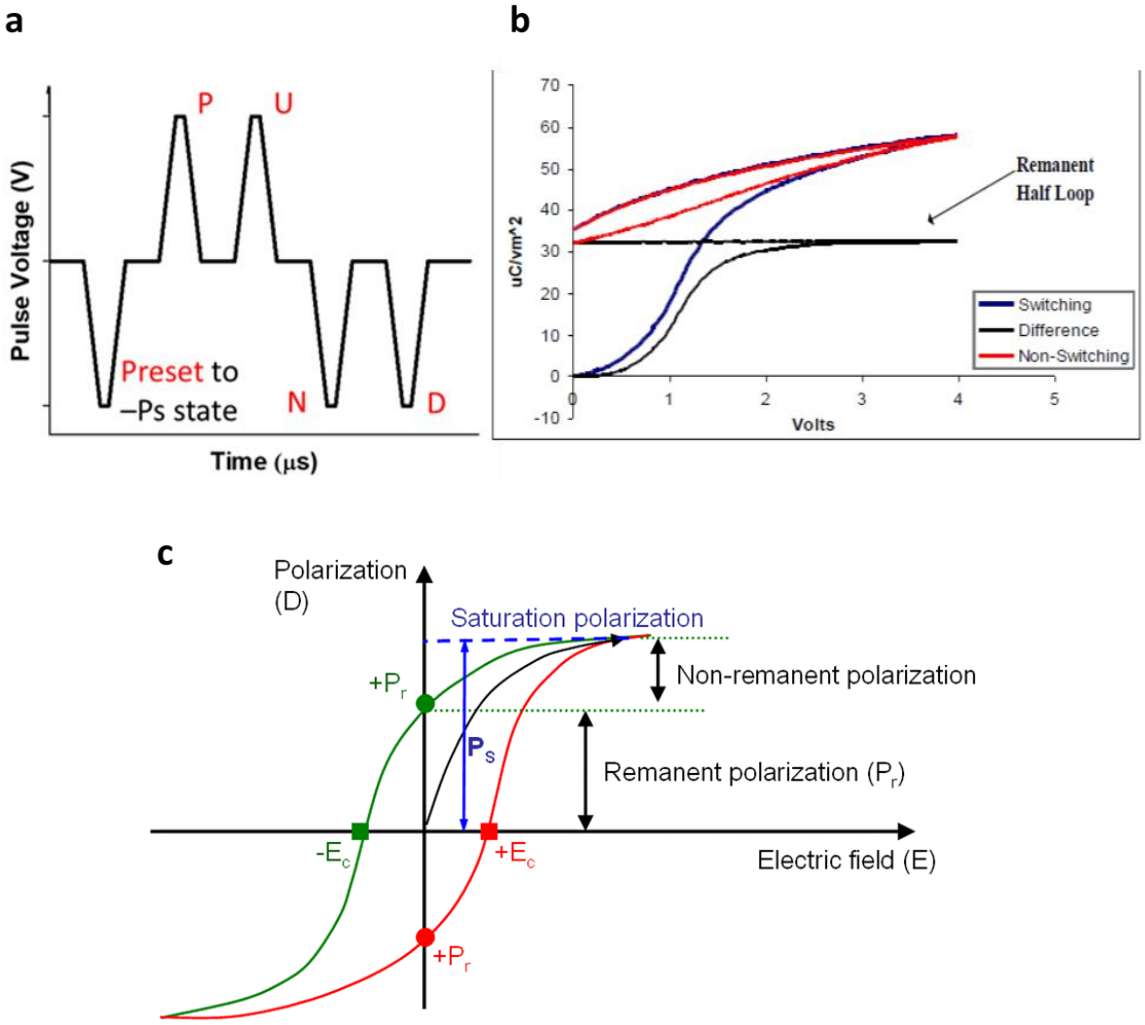

Figure 1-13. (a) Pulse schematics during a PUND measurement. (b) The two polarization half-loops calculated from the integration of current and positive remanent polarization calculated from the difference. (c) An example P-E loop with the important parameters labeled.

1.2.3 Ferroelectric Memory

Ferroelectric material is widely studied for application in ferroelectric random-access memory (FRAM) based on polarization reversal with applied electric field across the

ferroelectric thin film. The non-volatile ferroelectric film stores negative or positive remanent polarization even after field is revoked and therefore stores computational “0” and “1” states [72]. Two typical FRAM structures and their working principles are shown in Fig. 1-14 (taken with permission from website of program “feram” [90]).

In 1T1C (one-transistor-one-capacitor) FRAM (Fig. 1-14a), memory states are stored in the ferroelectric capacitor where ferroelectric layer’s polarization orientation is written by electric field pulse across the plate. During reading, word line turns on the transistor and force the plate to reach the potential from the bit line. For example, in Fig. 1-14c, if the capacitor upper plate charge induced from ferroelectric polarization is positive, a brief current pulse could be sensed when the transistor turns on and force the plate to reach a low potential from bit line, hence a “1” state read from the capacitor. Since this read process overwrites the original state from capacitor when the current pulse is captured, the cell needs to be reprogramed after the reading.

1T (one-transistor) FRAM (Fig. 1-14b) structure is similar to conventional MOSFET except the dielectric layer is replace with a ferroelectric layer. During write operation, gate (word line) provides voltage pulse exceeding coercive voltage for the ferroelectric layer and program it into either an “up” or a “down” state depending on the remanent polarization orientation. The induced doping in channel therefore determined either the transistor would be on or off states with zero gate voltage. In this process, the read operation by sensing current in the channel is non-destructive and no reprogramming is required, while its main disadvantage is that the achievable retention time in current devices is very limited [91].

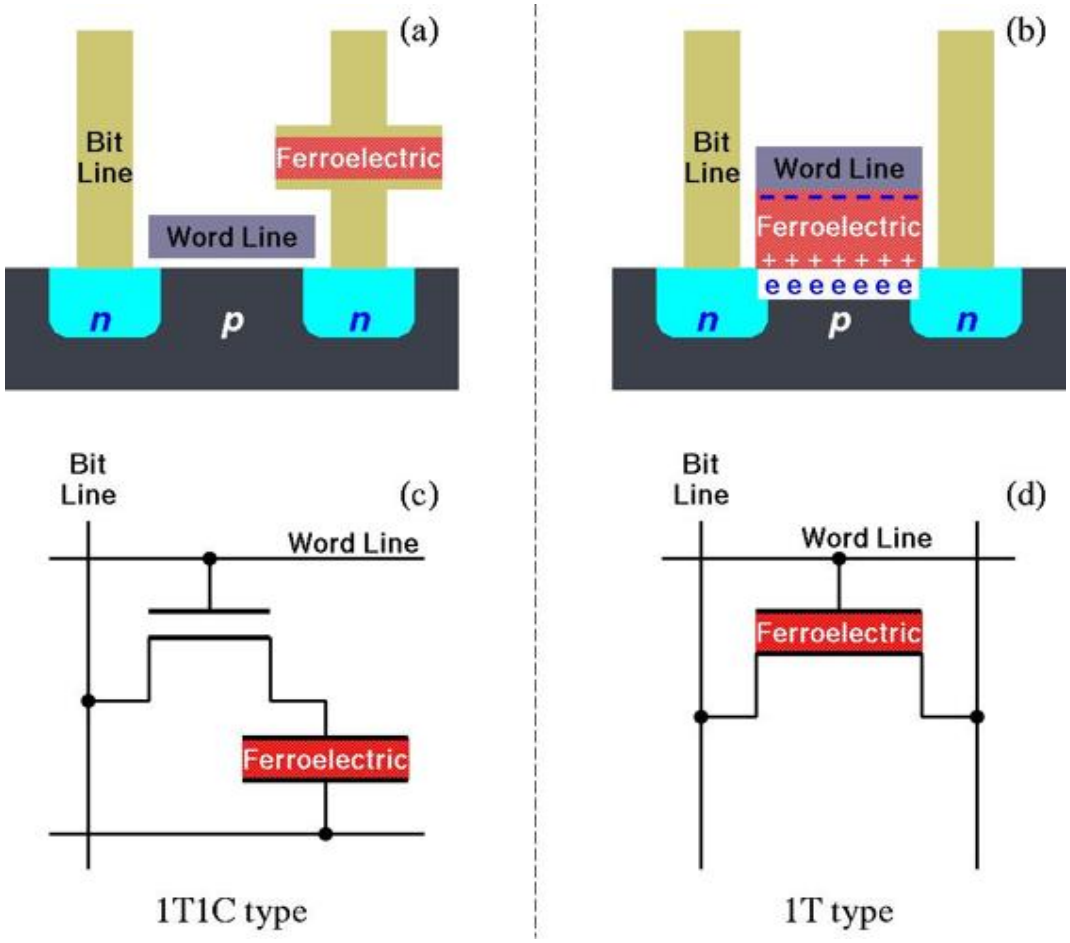

Figure 1-14. (a) FRAM with 1T1C structure. (b) FRAM with 1T structure. (c) Circuit diagram for 1T1C FRAM. (d) Circuit diagram for 1T FRAM.

1.2.4 2D Material Electronic Devices with Ferroelectric Dielectrics

2D materials have been combined with ferroelectric materials to make electronic devices in recent years. The non-volatile ferroelectric polarization is utilized for doping the 2D materials through electrostatic force. The doping level is determined by the remanent polarization, which could be adjusted to different levels by programming pulse conditions.

Beaumer et al. studied the bidirectional interdependency between graphene doping level and ferroelectric polarization in their graphene/$PbZr_{0.2}Ti_{0.8}O_3$ hybrid structure [92]. In

their work, single-layer CVD graphene was transferred onto laser deposition grown 140 nm $PbZr_{0.2}Ti_{0.8}O_3$ (FE layer)/60 nm $SrRuO_3/SrTiO_3$ (bottom electrode) substrate and Pd contacts are used (Fig. 1-15a inset [92]). The control FE capacitor sample with graphene between top electrode and FE layer indicates a $2P_r$ remanent polarization ~ 23 $\mu C/cm^2$ with ~ 2.44 V coercive voltage and ~ 0.5 ms pulse duration.

Due to the interfacial traps induced by H_2O or other absorbates between 2D material and dielectric interface, a clockwise hysteresis in I_d-V_g double-sweep curve is usually observed due to the trapped charges at interface [93]. In ferroelectric FET, this phenomenon is competing with the signature counterclockwise hysteresis in the I_d-V_g curve due to induced polarization switching if sweeping V_g exceeds coercive voltage of the ferroelectric layer. With a slow gate sweeping, the authors found an I_d drop deviating from traditional "V-shape" curve in non-ferroelectric graphene FET at around coercive voltage (Fig. 1-15a) and suggest it is due to the ferroelectric polarization switching, which is also observed in the gate

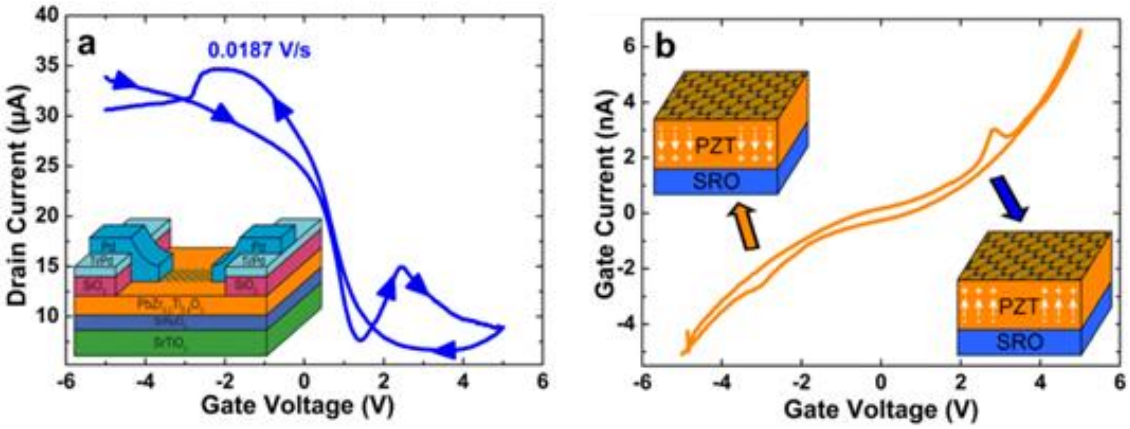

Figure 1-15. (a) Complex I_D–V_G characteristic for large gate voltages with a drain voltage of 50 mV and a gate voltage sweep rate of 0.0187 V/s. Inset: Schematic of a graphene transistor on PbZr0.2Ti0.8O3. (b) Gate current measured simultaneously to (a). Insets: Schematics of the ferroelectric polarization for different gate voltage regimes.

current peak at around same location (Fig. 1-15b). The Dirac point shift indicates an overall p-doping from gate-induced traps.

With increasing speed of gate sweeping, the influence from slow interfacial traps is reduced, a gradually diminishing p-doping is observed from the Dirac voltage shift until n-doping and a counterclockwise hysteresis loop is found, which could only be explained by ferroelectric polarization switching in PZT (Fig. 1-16 [92]).

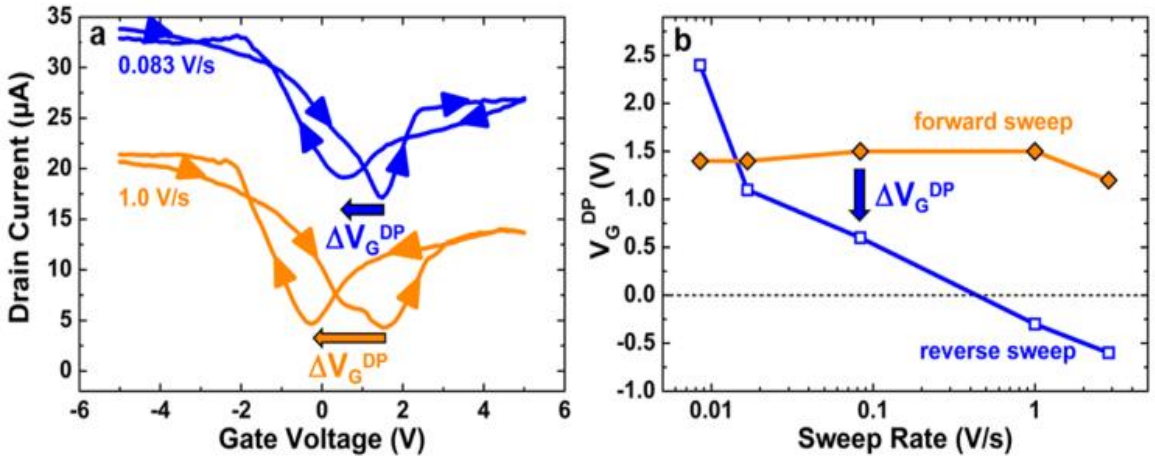

Figure 1-16. (a) Complex I_D–V_G characteristics of another graphene/PZT transistor for two representative sweep rates as indicated and offset for clarity. (b) Sweep-rate dependent position of the current minima defined as the Dirac point voltage in the forward (orange, filled diamonds) and reverse sweep (blue, open squares). The dotted line represents zero gate voltage and separates the regimes of n- and p-doping.

At last, the author demonstrated that, by managing the interfacial trap level (through high temperature annealing for hours) and ferroelectric polarization in the same device, their FE FET could demonstrate an I_d-V_g curve with different polarity through the channel carrier modulation, shown and explained in Fig. 1-17a [92]. In addition, with a constant drain voltage on and gate pulse schematics in Fig. 1-17b [92], the repetitive and consistent intrinsic/n-type device switching, and programming is realized, as a combined effect from ferroelectric layer polarization and reduced interfacial absorbates level.

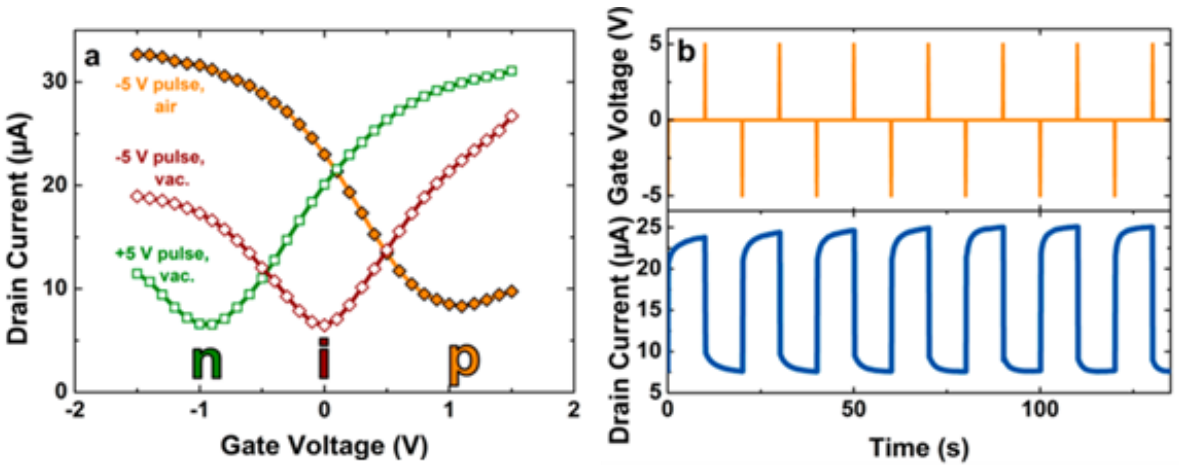

Figure 1-17. (a) Small gate voltage sweeps not exceeding the coercive voltage measured after 1 ms gate voltage pulses. p-type, nearly intrinsic, and n-type behavior can be observed after a −5 V pulse in air (orange, filled diamonds), a −5 V pulse in vacuum (red, open diamonds), and a +5 V pulse in vacuum (green, open squares), respectively. (b) Multiple gate voltage pulses applied to a similar device in air (upper panel) and resulting reversible and reproducible switching between a highly p-doped state for the down-polarized state and a nearly intrinsic level for the up-polarized case.

Another notable ferroelectric FET study is done by Lipatov et al. [94]. In their MoS_2-PZT FET structure (Fig. 1-18 [94]), mechanically exfoliated few-layer MoS_2 was transferred with PMMA on to 100 nm polycrystalline (001) oriented tetragonal $PbZt_{0.4}Ti_{0.6}O_3$ grown by metal-organic chemical vapor deposition covered by conductive TiO_2/Ir layer used as back gate. With a moderate bandgap channel material, their device shows large hysteresis of electronic transport with high on/off ratios, nondestructive data readout, low operation voltage, and wide memory window. Besides, their device exhibits possibility to write and erase the ferroelectric states both electrically and optically and therefor provides instant optical erase of large data arrays that is unavailable for many conventional memories.

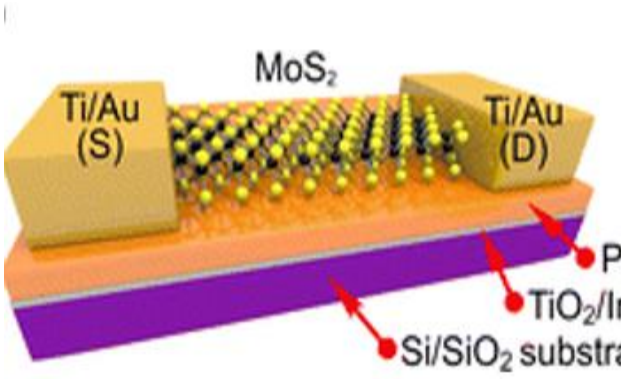

Figure 1-18. MoS_2 – PZT FEFET structure.

From a direct I_d-V_g sweep at different speed, while the author confirmed I_d and I_g local peaks from ferroelectric polarization switching (Fig. 1-19a and b [94]), the clockwise hysteresis from interfacial trap in this work overcomes the counterclockwise hysteresis from ferroelectric polarization (Fig. 1-19a [94]). As a result, a set of current measurements for the device at zero gate voltage 5 mins after different gate pulse values (Fig. 1-19c [94]) from -6V to 6V is designed to eliminate the major influence from the trap charges after their dissipation. The result current after different level of gate pulses clearly indicates the different levels of current level and channel doping from polarization switching (Fig. 1-19d [94]). The hysteresis suggests a wide memory window for zero-gate current measurement. While this dissipation time limits the operation frequency between write/read in the memory and leads to unstable device performance depending on the trap charge dissipation, the authors obtained a long-term on/off ratio for zero-gate current around 22 and endurance ~ 500 cycles between 1ms +6V and -6V write/erase gate pulses.

The moderate bandgap of MoS_2 enables a new approach to alter the polarization in ferroelectric layer due to its optoelectronic property. When the structure is illuminated with

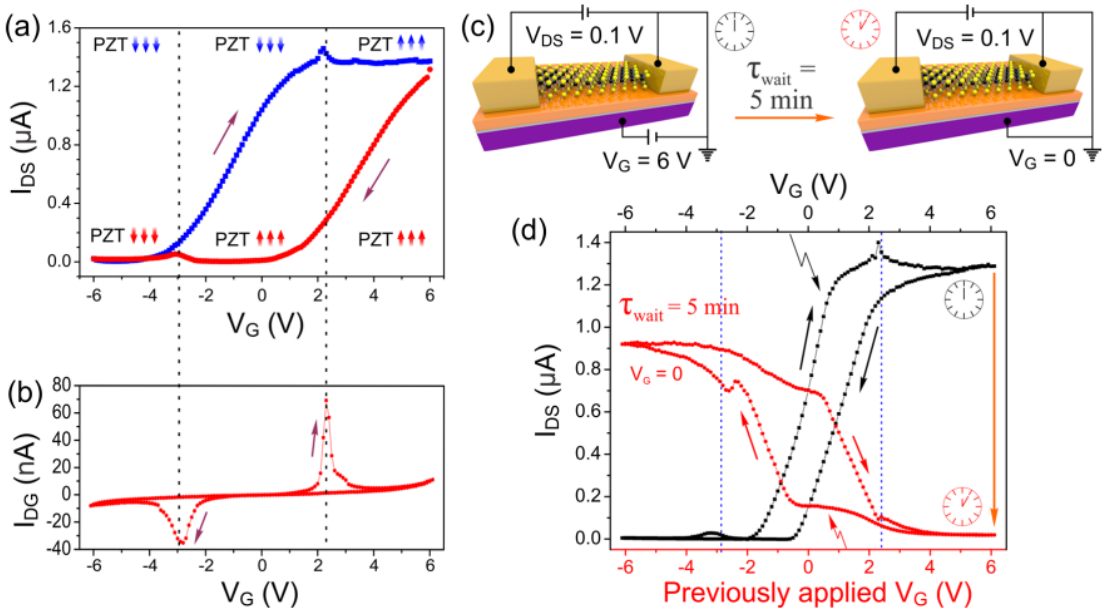

Figure 1-19. Electronic properties of a MoS2-PZT FEFET with V_{DS} = 0.1 V. (a) I_{DS}-V_G characteristics. The arrows in the insets show the polarization directions of PZT at different VG, which were determined from PFM control sample measurements. (b) V_G dependence of the drain-gate (leakage) current (I_{DG}-V_G measurements) for the same device. (c) Scheme of the electrical measurements revealing the polarization-dependent hysteresis of electronic transport in MoS2-PZT FEFETs (d) I_{DS}-V_G characteristics for the same device measured using the method shown in (c). Black data points show I_{DS} values while VG was applied. Red data points show I_{DS} values measured at grounded gate voltage (VG = 0) 5 min after the corresponding gate voltages were applied. Arrows indicate the directions of hysteresis.

visible light, the photo-generated charge carriers in MoS_2 channel could affect the polarization of the PZT beneath. Figure 1-20 [94] shows that the stabilized zero-gate current level after 1 ms +6 V (erase) and -6 V (write) in dark environment would be degraded into an intermediate level that is indistinguishable after 5 mins of 150 W halogen bulb illumination. This intermediate state is close to the original "on" state and thus illumination could be used to "write" the device to "on" state, in addition to the electric pulse write option.

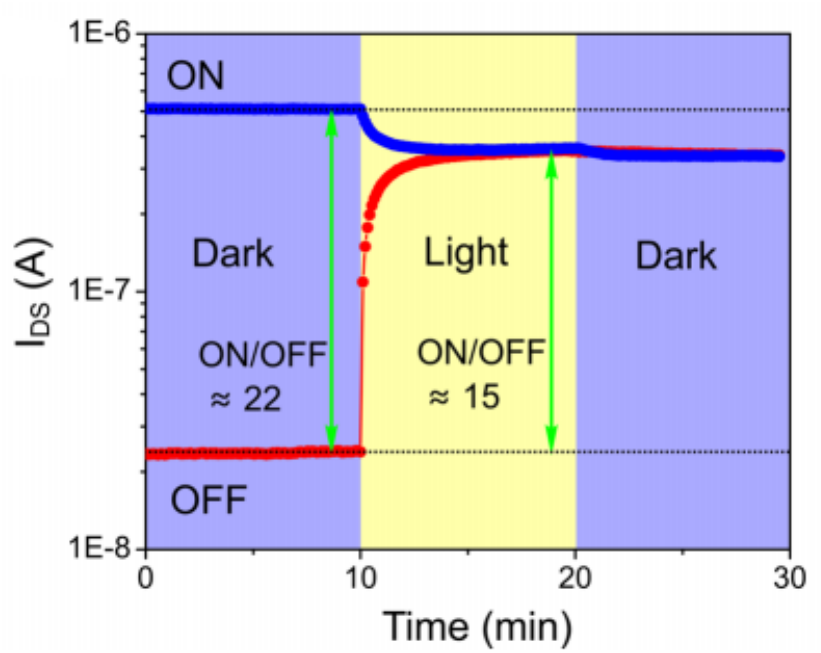

Figure 1-20. Effect of visible light illumination on the data retention characteristics of a MoS2-PZT FEFET.

Other than graphene and MoS_2 on PZT, ferroelectric memory device with memory window from polarization-induced threshold voltage shift has also been fabricated with graphene and black phosphorus with PVDF ferroelectric polymer, which has comparable thickness to PZT layer but with smaller remanent polarization value [95, 96]. Other than back gate FET structure, 2D van der Waals heterostructure stack based on 2D ferroelectric material $CuInP_2S_6$ and MoS_2 could also exhibit different traces for signature in transfer characteristics of FRAM [97]. A previous study done by our research group [98] demonstrated that Al-doped HfO_2 ferroelectric floating gate FET structure (Fig. 1-21) could successfully modulate the doping level in MoS_2 channel with the help of Ti intermediate gate (Fig. 1-22). These works provide valuable references toward our image classifier based on ferroelectric layer modulation.

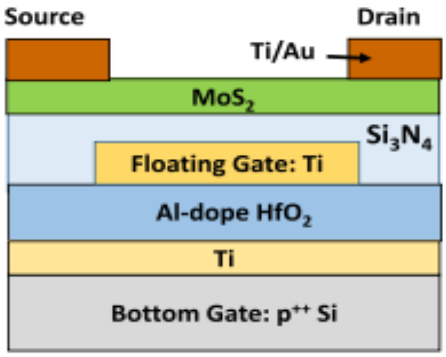

Figure 1-21. structure of MoS_2 Al-doped HfO_2 ferroelectric floating gate FET.

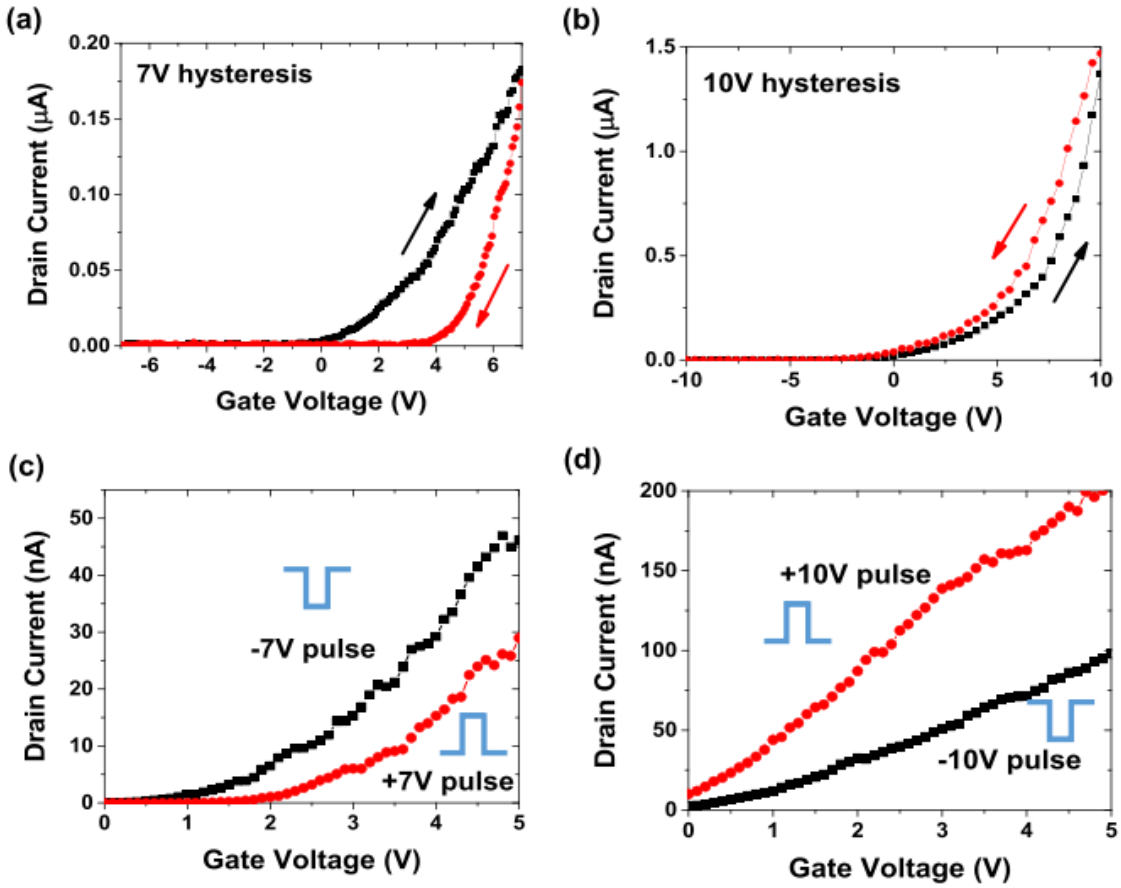

Figure 1-22. (a)(b) A sweep gate voltage below (7V) and above (10V) coercive voltage generates clockwise/counterclockwise transfer characteristic hysteresis, indicating the interfacial trap/ferroelectric switching dominant processes. (c)(d) A gate pulse amplitude below (±7V) and above (±10V) coercive voltage generates opposite doping in channel, indicating the interfacial trap/ferroelectric switching dominant processes.

Chapter 2 Experimental Details

In this chapter, we discuss the experimental details including synthesis/characterization of 2D materials and fabrication of 2D material-based electronic devices. These processes include material yielding (CVD growth/mechanical exfoliation), identification, and transfer (bulk mass transfer or target transfer), along with device fabrication techniques (lithography, metal deposition and/or dielectric growth).

Compared to mature III-V material, Ge or Si growth techniques used in wafer-scale substrates, 2D material used in electronic devices for research nowadays is usually cleaved from bulk crystal (mechanical transfer) or taken as a membrane from corresponding CVD substrate (wet transfer). In general, mechanically transferred 2D material flakes are relatively intact but their shapes and thickness are more random and uncontrollable due to the irreproducible process while splitting the bulk material into fragmented pieces. Sizes of these 2D material flakes are hence typically small. On the other hand, CVD-grown material provides the possibility for a larger (even wafer-scale) area of continuous material and the thickness of the flakes is more consistent through growth parameters (growth seeds, gas flow, temperature, time, etc.). But the material is likely to suffer from quality issues from the growth process and following transfer process with chemical etchant involved. Typically, for both material sources, they need to be transferred (from either bulk material or growth substrate) to dielectric substrates (SiO_2, quartz) to be further utilized in devices.

2.1 Exfoliation and Mechanical Transfer

The method to yield "Scotch-tape graphene" used in the very first graphene transistor is widely known and forms the basis for the mechanical transfer method. For mass printing, magic tape or thermal-release tape is commonly used in labs. The following process describes typical steps for mechanical cleavage and transfer of 2D material from bulk crystal onto SiO_2 wafer or other substrates [99].

A wafer with 90 nm or around 280 ~ 300 nm SiO_2 thickness is preferred for visible contrast between substrate and transferred 2D material flakes [100]. Acetone/IPA cleaning followed by N_2 air gun blow-dry is often applied, preferably with sonication treatment. In many cases, Piranha solution (sulfuric acid to 30% hydrogen peroxide with 3:1 ratio in volume) cleaning and oxygen plasma etching are also applied to clean the wafer and promote adhesion between flakes and substrate [101]. The process should be finished within ~1 hour after substrate pre-treatment for enhanced transfer rate. In some special applications, quartz wafer or flexible polyimide substrates may be used to eliminate potential parasitic effects, depending on the device specification and requirements.

Then, a small piece of 2D material crystal is placed gently on the adhesive side of a piece of Scotch-tape/thermal release tape. Lay another piece of tape smoothly on previous tape to enclose the crystal piece in both tapes. Adhere tapes completely and uniformly. Split the tapes slowly from each other to exfoliate the flakes in the middle. During the exfoliation, maintain steady and slow speed ~ 1 mm per second. A small angle should be kept between the two tapes during the process and tension should be applied along the tape. This splitting process should be repeated several times to split the original crystal into thinner parts, either

between the same two original tapes, or with the help of new tapes. After crystals become sufficiently thin and cover a moderate area of the tape after several times of splitting, print the tape with thinnest flakes gently on the prepared substrate. Apply tension along the tape to make the contact between substrate and tape flat and uniform. Press gently to ensure sufficient contact.

Tape is the peeled away from the substrate after ~ 30 s of contact. Similarly, exfoliation speed should be slow (~ 1 mm/sec) and tension should be exerted along the tape as well. A small angle between tape and substrate is important to a high yield of thin flakes on the target substrate. If thermal release tape is used, substrate with tape is placed on a hot plate, where a typical ~ 120 °C temperature heats up the thermal release tape and curl it up to separate the tape from the substrate. This whole series of steps should be done with gloves on to minimized potential contamination. A glovebox could also help to reduce the degradation for air-sensitive 2D materials. Since the crystal shape is random at the beginning and the exfoliation process is arbitrary, it is very hard to precisely control the size and shape of the resulting 2D material flake. However, this method or many other recipes tend to yield large amount of atomically thin flakes of interest among thick crystal fragments. In order to better understand the unique two-dimensional properties of the material, various inspection techniques are required to locate appropriate flakes (for characterization or device fabrication) on the substrate. Since many flakes of varying size, thickness and shape are distributed on the substrate at the same time and we need to inspect the whole area in search of a target flake of interest (usually one or a few layers), this is an example of a bottom-up procedure.

Although the method above provides a standard way to produce large amount of thinned down flakes, in many cases, we require our 2D material flake to be at specific sites on the substrate instead of random locations. For example, if a heterostructure stacking different 2D material flakes is proposed, we need to transfer the second layer of material exactly on the first target flake layer. While the first layer of material could be mass printed on the substrate using the method described in last section, a targeting transfer is required to place the second layer on top of the first layer.

The key to accomplish such a goal is an appropriate transfer medium (usually some sacrificial adhesive solid/liquid chemical compound) which picks up the 2D material flakes from the tape or growth substrate. Then with help of the mechanical stage, the medium with flakes could be moved precisely and printed onto the target transfer area. Microscopes are often used to ensure accurate alignment before the contact between flakes on the medium and the target area on the substrate. The medium is then removed, leaving the transferred flake on the substrate.

In the past, the wedging method, polyvinylalcohol (PVA) method and Evalcite method have been used to place 2D material flakes on the target position [61, 102, 103]. The wedging method uses water as the transfer-active agent to lift off the spin-coated hydrophobic polymer layer on hydrophilic substrate. If 2D material flakes on the hydrophilic surface are partially taken away by the hydrophobic layer, they can then be transferred elsewhere. The sacrificial layer needs to be removed by solvent after transfer. In the PVA method, flakes are transferred onto polymer sacrificial layer from substrate after the water soluble PVA polymer layer is dissolved in water. The sacrificial layer is then scooped up and mounted

onto the manipulator for transfer. It also needs to be removed after transfer is done. The Evalcite method makes use of low glass temperature polymer, which is applied between the glass slide and picked-up flakes. After flakes on the glass slide are moved to the desired location, heat is applied and the polymer melts, leaving flakes to drop easily on the acceptor substrate. In all these methods, chemicals from the sacrificial layer are involved and might degrade the crystal quality and give a rise to capillary force.

Compared to these wet agent transfer methods, dry transfer methods use solidated viscoelastic material as the transfer medium ("stamp") to carry the 2D material flakes without sacrificial layer dissolutions and they are low-cost, efficient and wet-chemical-free. Most dry transfer stamps are made of elastomer-based materials (polydimethylsiloxane, or PDMS, for example). For the dry transfer procedures used in our device fabrication based on *Gelfilm* (a polysiloxane based material similar to PDMS film) [104], the small piece of 2D material is first split into thinner flakes using methods described earlier. The flakes are then printed on the *Gelfilm* instead of SiO_2 substrates. *Gelfilm* is then observed under optical microscope so that flake with ideal size/thickness is located. The area of interest is then cut out and mounted on glass slide. A micromanipulator is then used to align the glass slide with target flake onto target area on the substrate. After the *Gelfilm* is brought into proximity with the substrate, continuous X-Y adjustment of the manipulator aligns the target flake on the *Gelfilm* to the target area on the substrate until flakes approach substrates in Z direction. Focus on the substrate and observe the alignment of target flake and target area while film starts to from contacts with substrate. The contrast between contacting and non-contacting regions during stamping could be easily differentiated by the contrast due to air gap. After complete adhesion is maintained for ~ 30 s, apply heat on the substrate to soften and lower

the viscosity of the *Gelfilm* to facilitate dropping the 2D material onto the substrate. Lift and remove the glass slide quickly afterwards and inspect the substrate.

After 2D material flakes are transferred onto acceptor substrates, it is necessary to confirm their shape, size, thickness, and contact with substrate to ensure that proposed structures would be appropriately fabricated. In our work here, we mostly use optical microscope with camera and AFM to fulfill such tasks.

2.2 CVD Graphene and Wet Transfer

The previous section demonstrates how to extract 2D material flakes from bulk crystal. Instead of bulk synthesis, 2D material could also be grown with few layers on specific substrates (such as CVD graphene on copper/nickel films) and requires "peeling off" to be transferred onto other substrates for further characterization or device fabrication. Taking single-layer graphene grown on copper foil as an example, the following wet transfer steps provides a way to obtain CVD grown few layer 2D material on desired substrate. Note that the chemical (PMMA and copper etchant) may damage the grown layer's quality.

After transparent single-layer graphene is grown on both sides of the copper foil [33], PMMA is spun on top of graphene on one side, usually the outer surface during CVD process. A piece of PMMA/graphene/Cu/graphene stack is then put to float on copper etchant ($FeCl_3$) in a beaker. After ~ 2 mins of floating, the graphene on back side (not protected by PMMA) are disappearing due to the partial copper removal. Repetitive rinsing between DI water beaker and copper etchant beaker should remove the copper and graphene on one side completely after ~ 10 mins etching. A silicon wafer piece is used to scoop and transfer the

PMMA/graphene stack between beakers. Then the graphene/PMMA membrane is rinsed thoroughly in DI water before the desired substrate is used to scoop it up, leaving conformal single layer of graphene on substrate surface after gentle nitrogen gun blow and water evaporation. Acetone is then used to remove the PMMA sacrificial layer. Note that the chemical residue (PMMA and copper etchant) may degrade the material layer's quality. The cross section for the structure during this series of operation is shown in Fig. 2-1.

Compared to the mechanical exfoliation, the CVD layer wet transfer brings the possibility for large-scale and uniform 2D material coverage. Oxygen plasma against a photoresist layer could then selectively etch the graphene layer for device patterns.

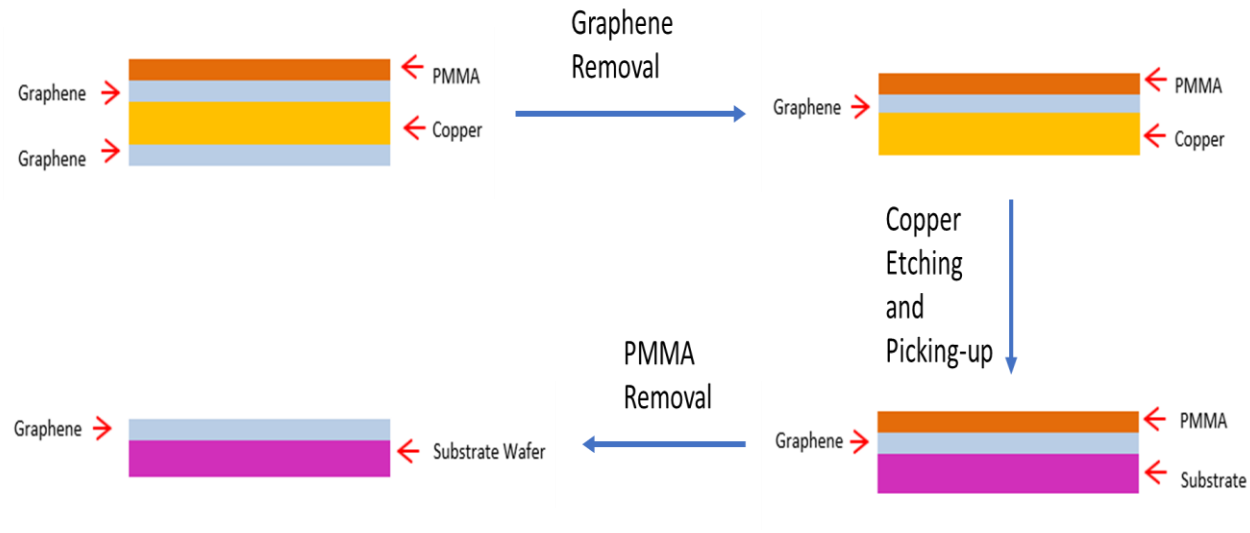

Figure 2-1. CVD graphene cross section during procedures described in Section 2.2.

2.3 Identifying the Transferred 2D Materials

After 2D material flakes are transferred onto acceptor substrates, it is necessary to confirm their shape, size, thickness, and contact with substrate to ensure that proposed structures would be appropriately fabricated. An optical microscope is the most accessible

and low-cost tool for rough inspection. Color contrast between the substrate and flakes transferred reveals the thickness. For atomic layers of 2D material, the color difference is barely visible. It generally holds that the thinner the layer, the lighter the contrast. For thick crystals among all the flakes transferred, their color ranged from green, to purple, to red, and to yellow, depending on specific material and thickness. An image process tool such as *ImageJ* could be used to numerically calculate the contrast between material body and substrate, providing a more reliable tool to determine material thickness [100]. Two example graphene optical images are shown below in Fig. 2-2.

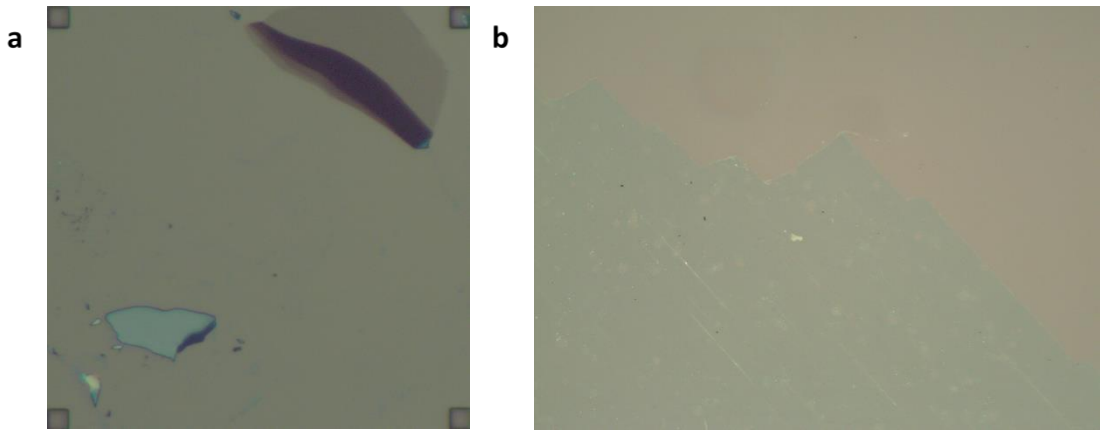

Figure 2-2. (a) Mechanically exfoliated single-layer graphene (upright corner). Flake area with deeper color is multi-layer graphite. (b) Wet transferred CVD grown single-layer graphene (green area). Stripes on CVD-grown graphene are likely results from wet chemical etching and PMMA residue.

Raman spectroscopy and atomic-force microscopy (AFM) are widely used to determine the precise thickness of material. Specifically, the peak location and height of the Raman signal (with an example in Fig. 2-3 [41]) are signatures of the material since it reflects the unique vibration mode within the material and hence the interaction with incoming photons. Even for identical 2D material, samples with different thickness will slightly affect the peaks' relative location and height [41, 105]. AFM is commonly used to measure the thickness of the 2D flakes. Two-dimensional material has typical layer thickness from 0.4

nm to 1 nm [7, 37]. Figure 2-4 demonstrates a set of AFM data for a ~ 5-layer hexagonal boron nitride. Other identification methods include scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-ray diffraction (XRD), etc., and are applied in various cases with different strengths and limitations [106].

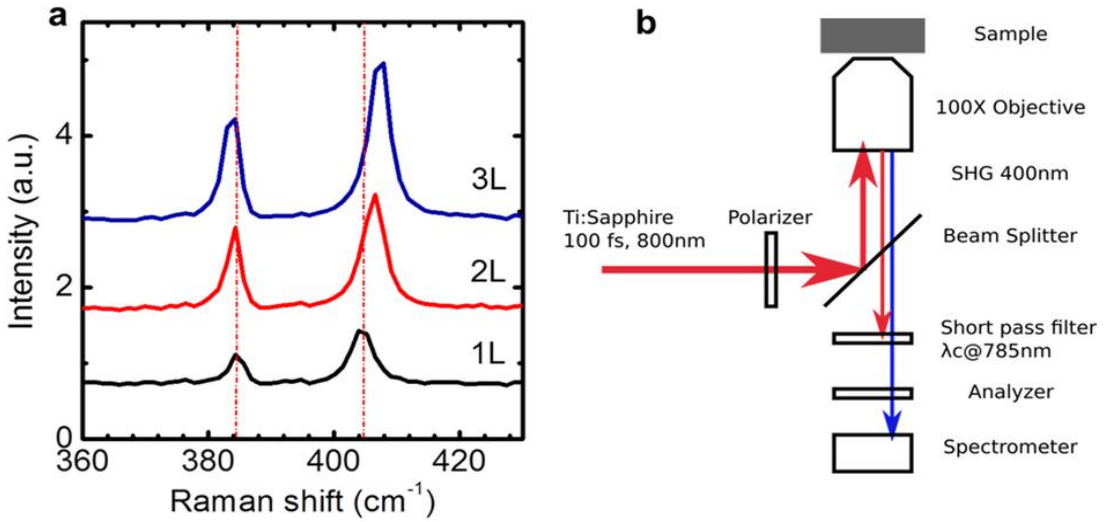

Figure 2-3. (a) Raman signals from different thickness of MoS_2 and (b) tool setup.

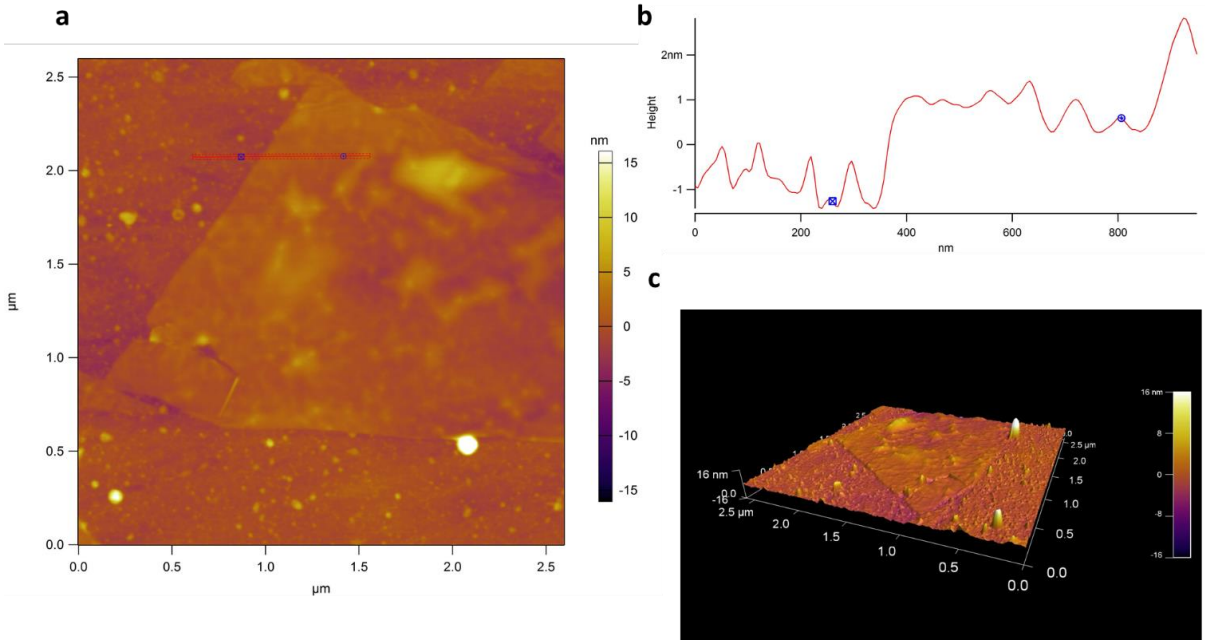

Figure 2-4. AFM data for a 5-layer hBN. (a) Top view with color depth representing thickness in each region. (b) Line scan indicating the thickness along the red scan line in (a). (c) 3D rendered view.

2.4 Device Fabrication

As in other traditional semiconductor devices, optical and/or e-beam lithography can be used to pattern the structure layer with corresponding etching or metal deposition/lift-off. For example, if we need to form a specific dimension for the graphene channel in our FET or capacitor devices, an AZ photoresist pattern by regular optical lithography could be used as a mask to protect the channel beneath it while oxygen plasma could etch away the excessive part from our transferred 2D material flake or CVD layer. With the help of alignment marks on the wafer substrate, we could also align the physical location of the 2D material on a wafer with the mask designed by computer for e-beam lithography. Metal contacts are often designed this way prior to e-beam evaporation with lift-off due to the random position, size and shape of the 2D material flakes on the substrate.

Another common step involved in the construction of electronic devices is deposition of dielectrics. For 2D material devices, this could be done with a conventional dielectric growth method (atomic layer deposition of aluminum oxide/hafnium oxide, low pressure chemical vapor deposition of silicon nitride, etc.) or targeting transfer of a 2D insulator. Some channel materials, such as black phosphorus, are sensitive to high temperature and special treatment or an alternative path needs to be considered.

Chapter 3 Electrical Characterization of 2D Materials

Electrical characterization of capacitors and transistors based on 2D materials can provide important information on the material properties. In the past, most of the electrical characterization of 2D electronic devices is based on direct-current (DC) measurements. In this chapter we show that alternating-current (AC) measurements can provide unique insights on the properties of 2D crystals. More specifically, we show that the bandgap and the gap states of 2D materials can be extracted from capacitance and AC conductance measured at various temperatures. This information is critical for designing and optimizing electronic devices such as transistors, tunneling field-effect transistors (TFETs) and resonant tunneling diodes (RTDs) based on 2D materials. (Contents of this chapter was previously published in *Applied Physics Letters* [107] and is used here with permission)

3.1 Characterization of the Bandgap of Black Phosphorus

The bandgap of black phosphorus (BP) is widely tunable, depending on the number of layers, external electric field and strain. Since the bandgap of black phosphorus is very narrow, it is difficult to measure using the standard photoluminescence and absorption spectroscopy in visible range. In this work, we propose a new approach to extract the bandgap of black phosphorus, using capacitance measured at various temperatures and frequencies. From the transition frequency or transition temperature, where the C-V changes from high-frequency to low-frequency behavior, we can extract the bandgap information. Using this method, we extracted the bandgap of the black phosphorus with 50

nm thickness as 0.30 eV. For comparison, we also extracted the bandgap of the black phosphorus using minimum conductance and threshold voltage methods, and the results are consistent with those of the C-V method. This C-V method can overcome the wavelength limitation of the photoluminescence measurement and spatial resolution limitation of Fourier transform infrared spectroscopy (FTIR). Another advantage of this C-V method is that the extracted bandgap is unaffected by the contact resistance and device area, making it reliable and convenient in determining the bandgap of narrow bandgap materials.

Black phosphorus has direct and tunable bandgap from 0.3 eV (bulk) to 1.4 eV (monolayer), corresponding to a broad energy spectrum from infrared to visible frequency range, which opens up a wide range of applications in photonics [56, 108-112]. The bandgap of the black phosphorus with layer number larger than five is less than 0.7 eV based on the density function theory (DFT) calculation [109, 113]. This narrow bandgap is beyond the wavelength range for most of the spectrometers in the photoluminescence (PL) measurements. In addition, the bandgap measured using PL is the optical gap, which is lower than the electronic bandgap due to the exciton binding energy. Recently, bandgap extractions based on current voltage (I-V) measurements using a Schottky metal-oxide field-effect-transistor (MOSFET) model were demonstrated, which can measure the transport gap directly [111, 112]. However, the accuracy of this method is highly dependent on the quality and the geometry of the devices, where the trap-assisted tunneling current and non-negligible resistance along the channel can cause errors in the extracted bandgap values. In this chapter, we propose a new method to extract the bandgap of the black phosphorus using the C-V method and compare it with the bandgap extracted using minimum conductance and threshold voltage methods.

3.1.1 Experiments

The black phosphorus capacitors were fabricated on quartz substrates to eliminate the potential parasitic capacitance between the probe pads and substrates. The black phosphorus flakes were exfoliated from bulk crystal and stacked onto the bottom metal electrodes using aligned dry transfer [104]. Hexagonal boron nitride (BN) was exfoliated from bulk crystal and used as the dielectric in the capacitor. C-V measurements were performed in vacuum at frequencies ranging from 10 kHz to 4 MHz and at temperatures ranging from 6 K to 300 K. Ti/Au (5nm/25nm) was deposited to form source and drain contacts in the BP transistors. The top gate dielectric is ~ 30 nm HfO2 deposited by atomic layer deposition (ALD).

3.1.2 Results and Discussion

The device structure of a black phosphorus capacitor is illustrated in Fig. 3-1a. The BN thickness is ~ 32 nm and the black phosphorus thickness is ~ 50 nm. The multi-frequency C-Vs of the BP/BN capacitor measured at 300 K are shown in Fig. 3-1b. Here, the capacitance of the device, C, is normalized with respect to the gate dielectric capacitance, C_{ox}. At 63 kHz measurement frequency, the C-V shows a typical low-frequency C-V behavior, where a local minimum is exhibited near the threshold voltage. As the frequency increases, the inversion capacitance decreases because the minority carriers in the inversion layer have more difficulty following the fast AC signal. At 4 MHz, the semiconductor capacitance shows high-frequency C-V behavior, where the inversion capacitance remains at minimum capacitance even beyond threshold voltage.

This transition from high- to low-frequency behavior is also observed in the temperature dependence of the capacitances. Figure 3-1c shows the C-Vs for BP/BN capacitors measured at 1 MHz from 8 K to 300 K. We can see that there is large temperature dispersion in the inversion over this temperature range. At low temperature (8 K), the minority carriers could not follow the 1 MHz signal; thus, a high-frequency behavior is observed. However, as temperature increases, minority carriers begin to follow because the generation and recombination rates (G_{gr}) increase with temperature, so that the carrier response time ($\tau_R = C_D/G_{gr}$) decreases. Here C_D is the depletion capacitance of the black phosphorus. As a result, the C-V curves change from high- to low-frequency behavior as the temperature increases from 8 K to 300 K. Here we define the transition frequency or transition temperature as the frequency or temperature where the C-V changes from a high-frequency to low-frequency behavior [114]. At 1 MHz frequency, the transition temperature is ~ 200 K for this BP capacitor, as shown in Fig. 3-1c.

By measuring the C-Vs at various temperatures and frequencies, the temperature dependence of the transition frequency can be determined. The inset of Fig. 3-1d shows the transition frequency as a function of temperature. Assuming the minority carrier response is dominated by the trap assistant process, the response time (τ_R) is inversely proportional to the intrinsic carrier density (n_i): $\tau_R \propto \frac{1}{n_i}$ [114]. Here the intrinsic carrier density can be expressed as: $n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{3/2}\left(m_n^* m_p^*\right)^{3/4} e^{-E_g/2kT}$, where m_n^* and m_p^* are the effective masses of electrons and holes respectively, E_g is the bandgap, h is Planck's constant, k is Boltzmann's constant, and T is the temperature. The transition frequency can be expressed as $f_{tr} \approx 1/\tau_R$. From these equations, we can see that the transition frequency follows:

$$f_{tr} \propto T^{3/2} e^{-E_g/2kT} \quad (3\text{-}1)$$

By plotting $\log (f_{tr}/T^{3/2})$ versus $1000/T$, we can extract the bandgap from the slope, shown in Fig. 3-1d. The extracted bandgap is ~ 0.30 eV for this BP flake, which is consistent with the DFT calculation and the bandgaps extracted from Schottky barriers [109, 112].

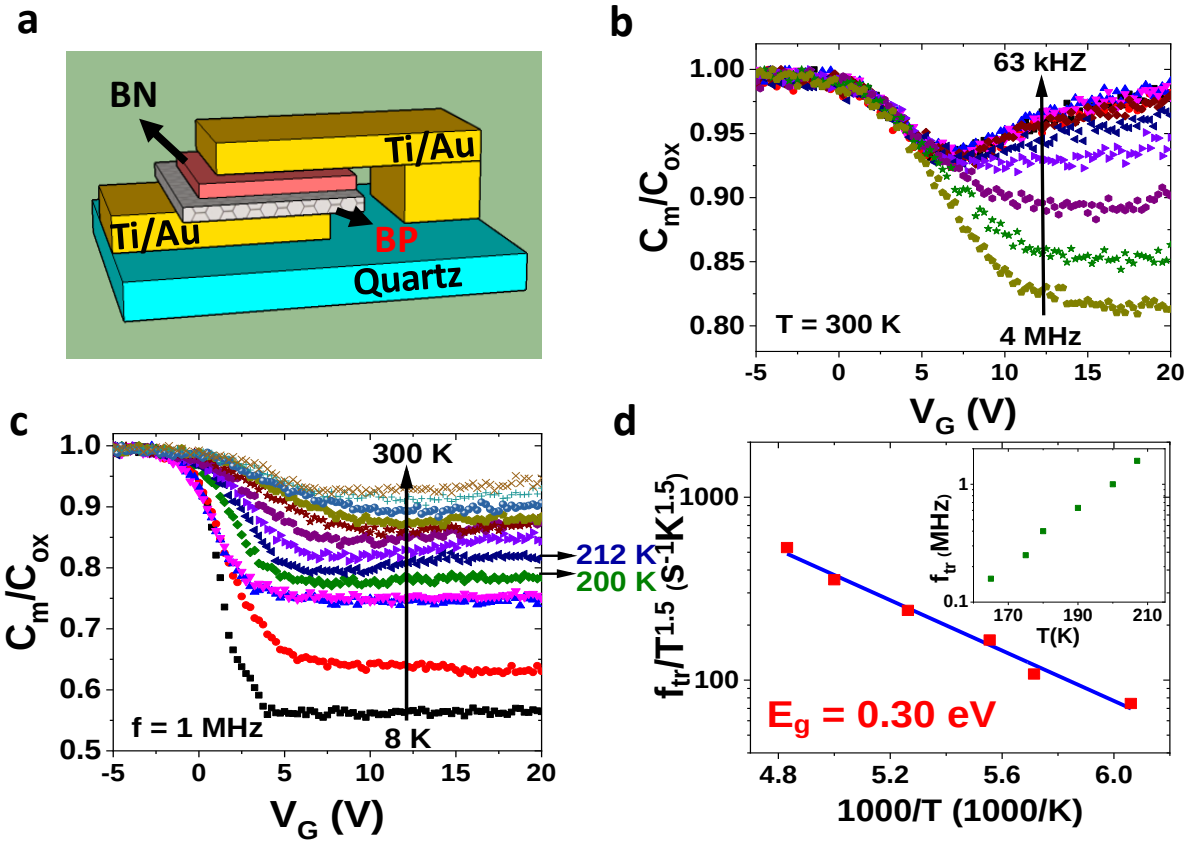

Figure 3-1. Bandgap extracted using C-V method. (a) Illustration of the BP/BN capacitors on quartz substrate. (b) C-Vs of the BP/BN capacitor measured at 300 K with various frequencies. (c) C-Vs of the BP/BN capacitor measured at 1 MHz with various temperatures. (d) Transition frequency divided by $T^{1.5}$ as a function of 1000/T. From the slope, we extracted the bandgap of the black phosphorus to be 0.30 eV. The inset shows the transition frequency as a function of measurement temperature.

This transition frequency method provides a unique technique to extract the bandgap for narrow bandgap materials, such as black phosphorus. This C-V transition frequency technique can overcome the wavelength limit of the photoluminescence measurement and spatial resolution limit in Fourier transform infrared spectroscopy (FTIR). For indirect

bandgap materials, since the photoluminescence signal is very weak, this electrical method to determine the bandgap will be very useful as well.

It has been reported previously that the bandgap of black phosphorus can be determined by minimum conductance. To compare the bandgaps extracted using these two methods, we fabricated BP transistors (with Al_2O_3 dielectric) by same transfer and fabrications techniques and measured the temperature dependence of the transfer characteristics. Since the thickness of the BP flakes is typically above 30 nm and the flakes are exfoliated from the same crystal, we expect that they will have similar bandgaps [115]. The transfer characteristics of the BP transistors are shown in Fig. 3-2a. The motilities for holes and electrons are extracted from the linear regions of the transfer curves at the hole and electron branches respectively. The hole and electron mobilities are plotted as a function of temperature shown in Fig. 3-2b and the inset of Fig. 3-2b respectively. By fitting the temperature dependence of the mobility using the equation $\mu \propto T^{-r}$ [116], we determine the r factor of this sample as 0.56 for hole mobility and 2.44 for electron mobility. The minimum conductance as a function of temperature is shown in Fig. 3-2c. The conductance (σ) can be expressed as: $\sigma = q(n\mu_e + p\mu_h)$, where n and p are the carrier concentrations for electrons and holes, μ_e and μ_h are the mobilities for electrons and holes, respectively. When the conductance reaches minimum, we have $\frac{\partial \sigma}{\partial p} = 0$. Considering $np = n_i^2$, we can derive that the minimum conductance:

$$\sigma_{min} = 2qn_i\sqrt{\mu_e\mu_h} \tag{3-2}$$

Since the intrinsic carrier concentration $n_i \propto T^{3/2} e^{-E_g/2kT}$ and $\sqrt{\mu_e \mu_h} \propto T^{-3/2}$ based on the r factors extracted in our sample, the minimum conductance follows $\sigma_{min} \propto e^{-E_g/2kT}$. The BP bandgap could then be extracted from the plot of ln (σ_{min}) versus ($1/T$), as shown in Fig. 3-2d. The extracted bandgap of the BP flake is ~ 0.30 eV, which is consistent with the result extracted from the C-V methods.

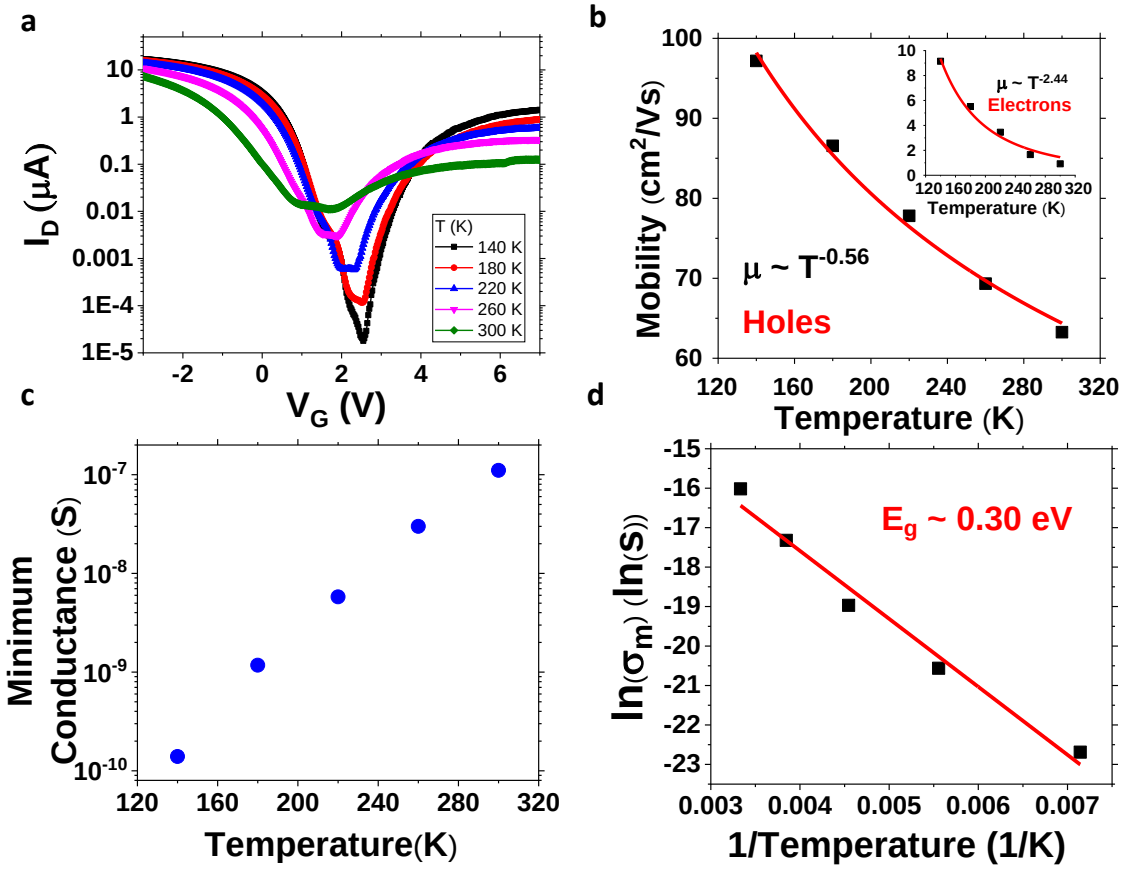

Figure 3-2. Bandgap extracted using minimum conductance method. (a) Ambipolar transfer characteristics of the BP transistor measured from 140 K to 300 K. (b) Effective hole mobility as a function of temperature. The inset shows the effective electron mobility as a function of temperature. (c) Minimum conductance as a function of temperature. (d) The bandgap of the black phosphorus extracted from the ln (σ_{min}) versus ($1/T$) plot is ~ 0.30 eV.

Another reported method to extract bandgap using IV measurement is based on the threshold voltages and subthreshold swing [117-119]. A transfer curve in semi-log scale is drawn in Fig. 3-3a and the band diagrams at the threshold voltages for the electron and hole

branches are illustrated in the insets of Fig. 3-3a. When the Fermi level in the source electrode is lined up with the conduction band edge of the semiconductor channel, the gate voltage applied on the channel is defined as threshold voltage for the electron branch, V_{th-n}. When the Fermi level in the drain electrode is lined up with the valence band edge of the semiconductor channel, the gate voltage applied on the channel is defined as threshold voltage for the hole branch, V_{th-p} The subthreshold swing is $SS \equiv \ln(10)\frac{\partial V_G}{\partial \ln(I_D)} = \frac{kT}{q}\ln(10)\frac{\partial V_G}{\partial \psi_s} = SS_{ideal}\frac{\partial V_G}{\partial \psi_s}$, where ψ_s is the surface band bending in semiconductor and $SS_{ideal} = \frac{kT}{q}\ln(10)$ is the thermodynamically limited subthreshold slope. Therefore, the bandgap of a semiconductor can be expressed as [117, 118, 120]:

$$E_g = q[\frac{\Delta V_{th}}{(SS_p+SS_n)/2/SS_{ideal}}] \quad (3\text{-}3)$$

where q is the electron charge, $\Delta V_{th} = V_{th-n} - V_{th-p}$ is the difference between the threshold voltages for electron and hole branches, and SS_p and SS_n are the subthreshold swings in p and n branches respectively. An example transfer curve measured at 300 K and the extracted threshold voltages are shown in Fig. 3-3b. The bandgap extracted is 0.30 eV, which is consistent with that extracted using C-V and minimum conductance methods discussed previously.

Among these three methods of extracting bandgap using electrical measurements, the C-V method uses the simplest device structure (two-terminal capacitor) and is least sensitive to the contact resistance. However, the C-V method is not practical for wide bandgap materials, since the transition temperature at the standard frequency range (1 kHz ~ 5 MHz) can reach > 500 ^{o}C, which exceeds the temperature range for many probe stations. The threshold voltage method is the easiest and fastest method; however, its

accuracy is undermined by the ambiguity in determining the threshold voltage in real devices' transfer curves. The minimum conductance method has moderate accuracy and complexity for narrow bandgap materials but has very limited application in medium or wide bandgap materials, since the current at minimum conductance is below the detection level of the instrument if the bandgap is too large.

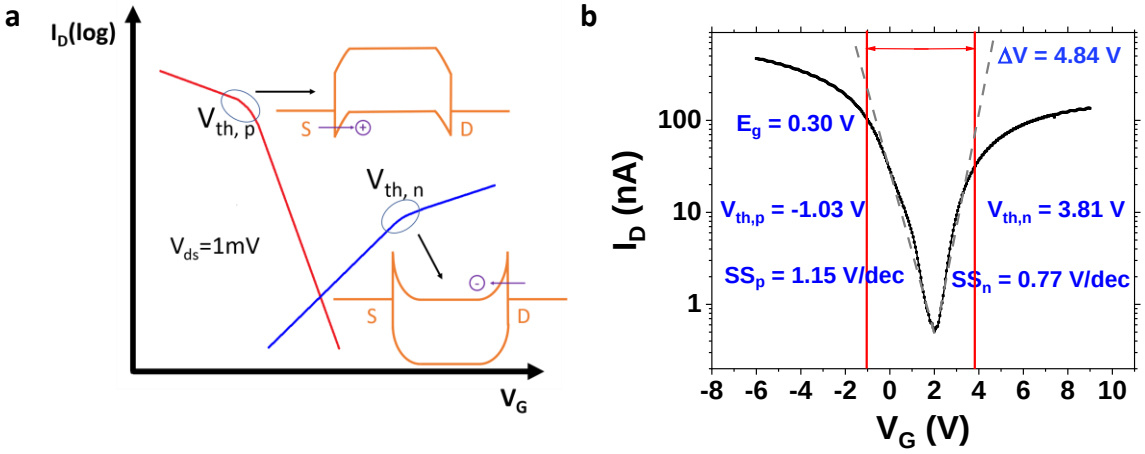

Fig. 3-3. (a) Expected Schottky-Barrier FET I_d-V_g curve for small bandgap semiconductor and low work-function contact metal, with threshold voltages for both the electron and the hole branches labeled. When drain voltage applied is very small, band diagram is almost symmetric about source and drain sides. (b) I-V curve in log scale at 300K with extracted bandgap ~ 0.30 eV from threshold voltage difference and subthreshold swings (with v_{ds} = 1mV).

3.1.3 Summary

In conclusion, we proposed and demonstrated a new method to determine the bandgap of black phosphorus using C-V measurements. Based on the transition frequency, at which the C-V characteristics changes from high- to low-frequency behavior, we can extract the bandgap of the semiconductor. A 0.30 eV bandgap is determined for thick black phosphorus flakes (50 nm). For comparison, we also extracted the bandgaps using minimum conductance and threshold voltage methods. The bandgaps extracted from the three

methods are consistent with each other. This new method is especially useful for narrow and/or indirect bandgap materials, where photoluminescence measurements are beyond the spectrum range or detecting limit. The bandgap extracted using the C-V method is not affected by the contact resistance and device area, making it a convenient and accurate tool for charactering the bandgaps of narrow bandgap materials.

3.2 Characterization of the Interface States in Black Phosphorus

Interface traps are electrically active defects located at the interface between gate dielectric and semiconductors. Interface traps have energy levels within the forbidden gaps of the semiconductors. They are distributed with interface trap density, $D_{it} \equiv \partial N_{it}/\partial E$, in units of $cm^{-2}eV^{-1}$, where N_{it} is the number of interface traps per unit area and E is energy. Interface states are capable of trapping and de-trapping charge carriers and can have an adverse effect on device performance. In metal oxide field-effect transistors (MOSFETs), the charged interface traps can reduce the carrier mobility by Coulomb scattering and thus reduce the drain current. The interface trap capacitance can degrade the subthreshold swing and reduce the on/off current ratio for a given supply voltage. In tunneling field-effect transistors (TFETs), the interface states can induce trap-assistant tunneling in the "off" states, which will increase the off-current and degrade the subthreshold swing. In Esaki diodes and resonant tunneling diodes (RTDs), the interface states can introduce additional valley currents, which will reduce the peak-to-valley current ratio and make it difficult to observe negative-differential resistance (NDR) effect at room temperature [121].

For electronic devices based on 2D materials, their performance and reliability are even more sensitive to the interface quality, since 2D materials have atomically thin bodies

and extremely large surface-to-body ratio. To ensure the technologies based on 2D materials are predictable, reliable and stable, it is very important to characterize and monitor the quality of the interface between 2D materials and gate dielectric/substrate. Among the large variety of 2D materials, black phosphorus and WSe_2 are two promising candidates for electronic and photonic devices. Black phosphorus has a puckered hexagonal structure and anisotropic in-plane electrical and optical properties [56, 57, 122-124]. The bandgap of black phosphorus is direct and tunable from 0.3 eV (bulk) to 1.4 eV (monolayer) [56, 108-112]. The transistors based on black phosphorus show high carrier mobility (up to 5200 cm^2/V-s at room temperature and ~ 45000 cm^2/V-s at 2 K) and good on/off ratio (~ 10^5) [57, 96, 118, 125-135]. WSe_2 is an important member of the transition metal dichalcogenide (TMD) family due to its smaller effective electron and hole masses compared to most of the other TMDs [47, 136]. The small effective mass implies high carrier mobilities. The hole mobility of WSe_2 is reported to reach 500 cm^2/V-s at room temperature and 2.1 × 10^3 cm^2/V-s at 5 K [137, 138]. Various electronic and photonic devices based on black phosphorus and WSe_2 — including metal-oxide field-effect transistors (MOSFETs), tunneling devices, bipolar transistors, photodetectors, light emitting diodes, and solar cells—have been demonstrated [47, 96, 118, 125, 127-134, 137, 139-152]. However, there is very limited research on the interface properties between these 2D materials and gate dielectrics/substrates. In this section, we systematically study the interface states of black phosphorus and WSe_2 using capacitance and conductance methods. We found that the C-V characteristics of black phosphorus and WSe_2 capacitors are dramatically different due to the different sizes of the bandgaps. In addition, we found the interface-state density increases exponentially with gate voltage, when the capacitor is biased from midgap toward band edge. As the temperature

increases, the interface-state time constant reduces dramatically due to the increasing carrier thermal velocity.

3.2.1 Experiments

The metal-insulator-semiconductor-metal (MISM) capacitors based on black phosphorus and WSe_2 were fabricated on quartz substrates to eliminate the potential parasitic capacitances between the probe pads and the substrates. Embedded metal electrodes (30 nm Ti / 20 nm Au) were formed by photolithography, e-beam metal evaporation and lift-off. The black phosphorus and WSe_2 flakes were exfoliated from bulk crystals and stacked onto the bottom metal electrodes by aligned dry transfer [104]. Al_2O_3 was deposited as gate dielectric using atomic layer deposition (ALD) at 200 °C [153]. The top electrodes were formed by photolithography, metal deposition and lift-off. The Al_2O_3 at the pad area of the bottom electrodes was removed using hot phosphoric acid in order to ensure good contacts. The structure of the MISM capacitor is illustrated in Fig. 3-4a. Al_2O_3 thickness is ~ 30 nm measured by profilometer on a control structure. The capacitors were measured in vacuum at various temperatures using a Lakeshore cryogenic probe-station. The capacitance and conductance of the capacitors were measured at various frequencies using a Keysight parameter analyzer. The equivalent circuit model of the device, simplified parallel model of the device and measurement model in parallel mode are illustrated in Fig. 3-4b.

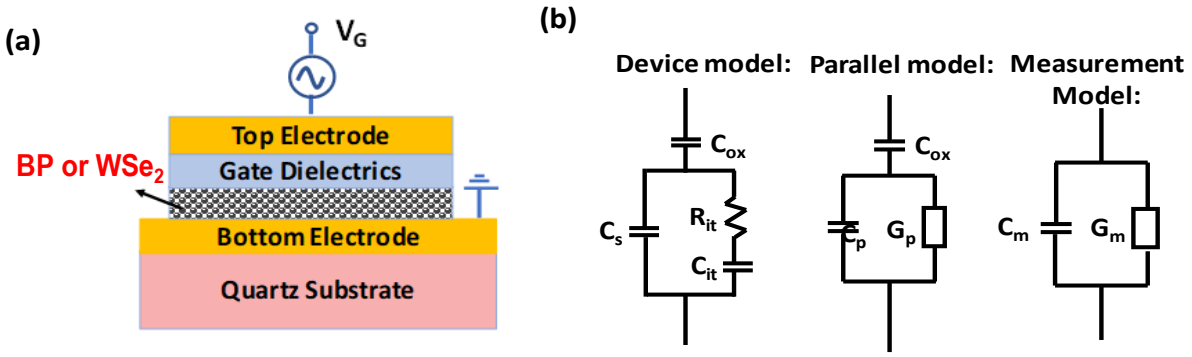

Figure 3-4. (a) Illustration of the MISM capacitor structure on quartz substrate. (b) The equivalent circuit model of the device, simplified parallel model of the device, and the measurement model in parallel mode. C_{ox} is the gate dielectric capacitance, C_s is the semiconductor capacitance, C_{it} is the interface trap capacitance, and R_{it} is the resistance due to interface traps. C_p and G_p are the extracted parallel capacitance and conductance, respectively. C_m and G_m are the measured capacitance and conductance in parallel mode, respectively.

3.2.2 Results and Discussion

The capacitances of the WSe_2 and black phosphorus capacitors were measured as a function of gate voltage at various frequencies, shown in Fig. 3-5a and 3-5b, respectively. Here, the capacitance of the device, C_m, is normalized with respect to the gate dielectric capacitance, C_{ox}. The thickness of the black phosphorus is ~ 55 nm and the thickness of the WSe_2 is ~ 30 nm. The gate dielectrics in both capacitors are Al_2O_3 grown by ALD with thickness of ~ 30 nm. These two sets of C-Vs are drastically different. The C-Vs of the WSe_2 capacitor are unipolar and high-frequency-like, while the C-Vs of the black phosphorus capacitor are ambipolar and low-frequency-like. The C-V curves of black phosphorus capacitor are nearly symmetric about the minimum capacitance point at gate voltage of around 0.4 V. Even at a very high frequency (2.5 MHz), the C-V shows low-frequency behavior, i.e., the capacitance at inversion is nearly as high as the capacitance at accumulation. These phenomena can be attributed to the narrow bandgap and low doping of the black phosphorus flake. The thickness of this black phosphorus flake is ~ 55 nm, which

corresponds to a ~ 0.3 eV bandgap. The narrow bandgap of black phosphorus leads to a large number of minority carriers generated thermally at room temperature, which can effectively reduce the generation/recombination resistance of the minority carriers, R_{gr}, and consequently reduce the minority carrier time constant, $\tau_R = R_{gr}C_D$, where C_D is depletion capacitance. Therefore, at room temperature, the minority carriers can still follow the ac signal and the C-Vs show low-frequency behavior, even when the testing frequency is in MHz regime. The very low doping in black phosphorus flakes yields symmetric C-Vs about the midgap. These two factors result in the nearly V-shaped C-Vs. For WSe_2, however, the bandgap is much larger (~ 1.21 eV), there are very few minority carriers generated at room temperature and the minority carrier time constant is very long. Therefore, the minority carriers cannot follow the ac signal and the C-Vs show high-frequency behavior, even when the measurement frequency is as low as 1 kHz. In addition, the exfoliated WSe_2 flake is naturally p-type doped, which gives the unipolar C-Vs, similar to p-type silicon. These results indicate that we can use the C-V characteristics to evaluate the bandgap of the 2D materials. At a given temperature and testing frequency, the wider the bandgap of the semiconductor, the stronger the high-frequency behavior in the C-V characteristics.

To evaluate the interface-state density quantitatively, we extracted the parallel conductance from the capacitance and conductance measurements. As shown in Fig. 3-4b, the parallel conductance, G_p, can be extracted from the measured capacitance, C_m, and conductance, G_m, by the following equation [114]:

$$G_p = \frac{\omega^2 G_m C_{ox}^{\ 2}}{G_m^{\ 2} + \omega^2 (C_{ox} - C_m)^2} \tag{3-4}$$

where ω is the measurement frequency and C_{ox} is the oxide capacitance. Figures 3-5c and 3-5d show the G_p/ω plot at various gate voltages for black phosphorus and WSe_2 capacitors, respectively.

The relation between G_p/ω and the interface-state density D_{it} is given by [114]:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega_{it}} \ln\left[1 + (\omega_{it})\right]^2 \tag{3-5}$$

from which one can deduce the interface-state density, D_{it}, and the respective time constant, τ_{it}, from the following relations [114]:

$$D_{it} = \frac{2.5}{e}\left(\frac{G_p}{\omega}\right)_{peak} \tag{3-6}$$

$$\tau_{it} = \frac{1.98}{2\pi f_0} \tag{3-7}$$

Here, $\left(G_p/\omega\right)_{peak}$ is the maximum G_p/ω value and f_0 is the frequency at which this maximum G_p/ω is obtained. The extracted interface-state densities, D_{it}, are plotted as a function of gate voltages for WSe_2 and black phosphorus, shown in Fig. 3-5e and 3-5f, respectively. We can see that the interface-state densities decrease exponentially with increasing gate voltage toward the midgap for the WSe_2 capacitor. This exponential dependence of the interface-state density on gate voltage is similar to what has been observed in silicon. In silicon, the D_{it} distribution is typically modeled using this equation: $D_{it} = D_{it0}e^{\phi_s/\phi_{s0}}$, where D_{it0} is the interface trap density at the midgap, ϕ_s is the surface potential measured from the intrinsic Fermi level, and ϕ_{s0} is a characteristic potential, which describes the slope of D_{it} near the band edges. Note that $\phi_s = E_{Fs} - E_i$, where E_{Fs} is the Fermi level at the interface between the semiconductor and gate dielectrics and E_i is the

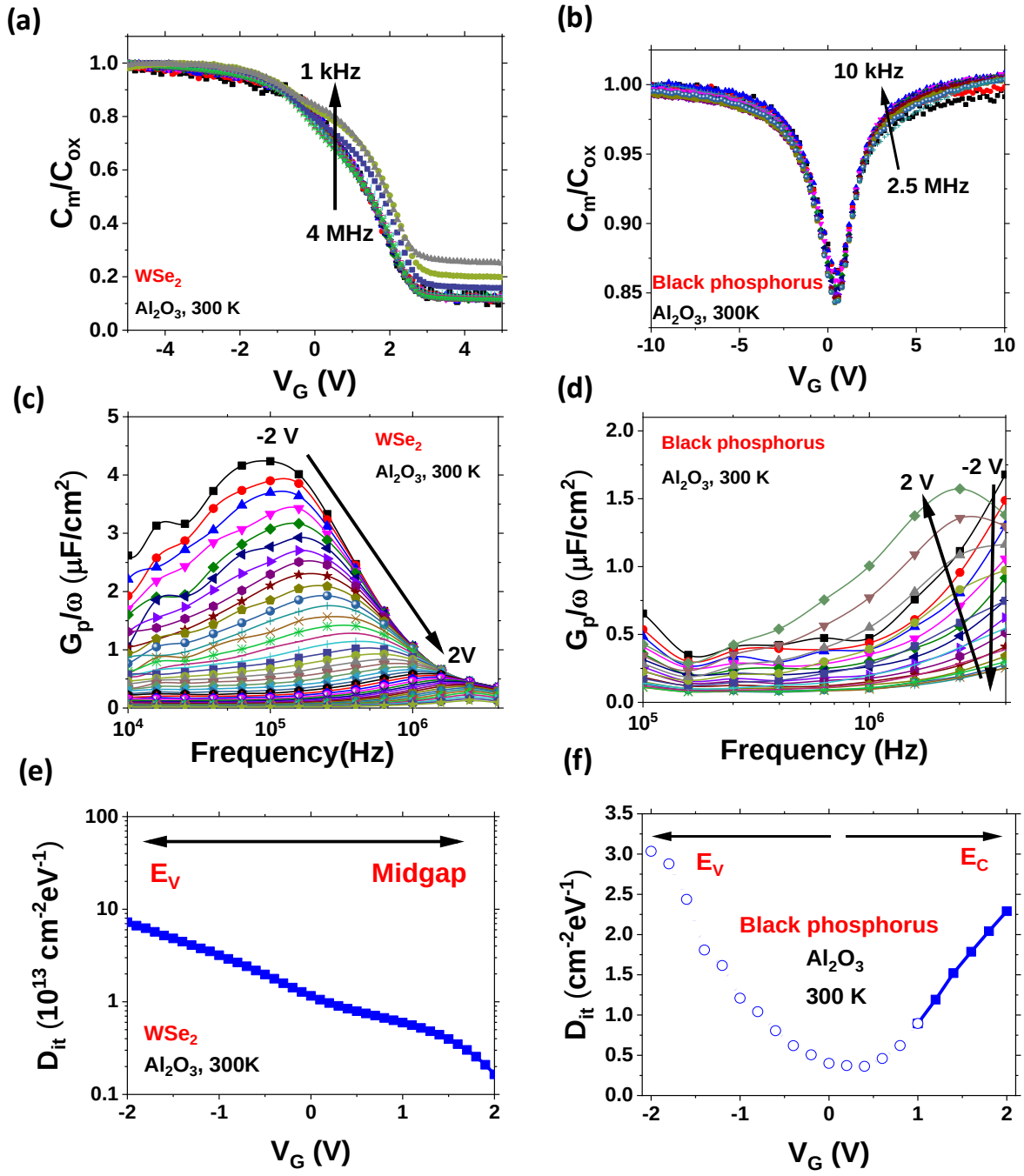

Figure 3-5. The interface states of WSe_2 and black phosphorus capacitors with Al_2O_3 gate dielectrics at 300 K. (a) Capacitance as function of gate voltage of a WSe_2 capacitor measured at various frequencies. (b) Capacitance as function of gate voltage of a black phosphorus capacitor measured at various frequencies. (c) G_p/ω as a function of frequency of the WSe_2 capacitor measured at various gate voltages. (d) G_p/ω as a function of frequency of the black phosphorus capacitor measured at various gate voltages. (e) Interface-state density, D_{it}, as function of gate voltage extracted from the G_p/ω plot for the WSe_2 capacitor. (f) Interface-state density, D_{it}, as function of gate voltage extracted from the G_p/ω plot for the black phosphorus capacitor.

intrinsic Fermi level of the semiconductor. As the surface Fermi level, E_{Fs}, is moving from the midgap toward the band edge, the interface-state density increases exponentially, as we observed in the WSe_2 capacitor. For the black phosphorus capacitor, the interface-state density first decreases, then increases, with the increasing gate voltage. The interface-state density reaches minimum, when the gate voltage is $\sim$ 0.4 V, which corresponds to the minimum capacitance in the C-Vs, shown in Fig. 3-5b. At this gate voltage, the surface Fermi level reaches midgap. As the surface Fermi level is swept from midgap to the conduction/valence band edges, the interface-state density increases exponentially. The very low doping and the narrow bandgap of the black phosphorus make it possible to observe the interface states in both the upper and lower half of the bandgap.

The temperature dependence of the capacitance and the interface states were also studied. Figure 3-6a shows the C-Vs of a black phosphorus capacitor measured at various temperatures from 6 K to 300 K. The testing frequency is 2.5 MHz. As the temperature decreases, the inversion capacitance of the black phosphorus capacitor decreases, and the C-V characteristics migrate from low-frequency to intermediate-frequency behavior. The reason for this is that, as the temperature decreases, the generation-recombination rate in black phosphorus decreases, and as a result the generation-recombination resistance, R_{gr}, increases and the minority carrier response time, τ_R , increases. Therefore, as the temperature decreases, the minority carriers follow the ac signal less readily, and the C-Vs gradually change from low-frequency to high-frequency behavior for a given testing frequency.

From the measured capacitance and conductance, we can extract the G_p/ω as a function of frequency at various gate voltages (Fig. 3-6b) and at various temperatures (Fig. 3-6c). As the temperature increases, the G_p/ω peak shifts to higher frequencies. The extracted interface-state density, D_{it}, was plotted as a function of temperature, shown in Fig. 3-6d. We can see that the interface-state density is nearly independent of temperature.

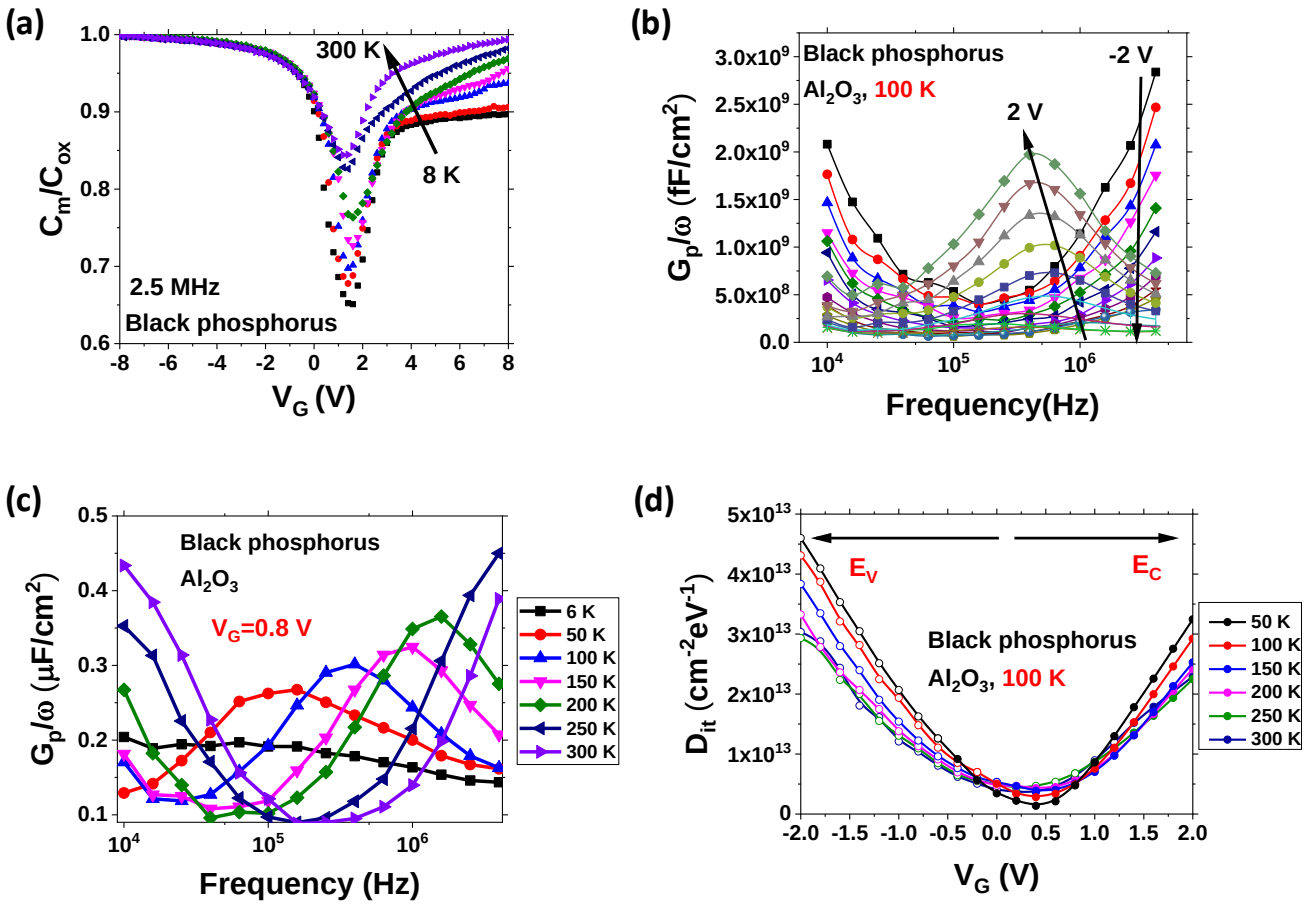

Figure 3-6. Temperature dependence of interface states in black phosphorus capacitors with Al_2O_3 gate dielectrics. (a) Capacitance as a function of gate voltages measured at various temperatures. The measurement frequency is 2.5 MHz. (b) G_p/ω as a function of frequency measured with various gate biases at 100 K. (c) G_p/ω as a function of frequency at various temperatures. The gate bias is 0.8V. (d) Interface-state density, D_{it}, as function of gate voltage extracted from the G_p/ω plots.

The interface states are not only dependent on the 2D materials, but also influenced by the gate dielectrics, which are in intimate contact with the 2D materials. Figure 3-7a and

3-7b show G_p/ω plots for black phosphorus capacitors with Al_2O_3 and hexagonal boron nitride (hBN) as gate dielectrics, respectively. The peak height of the G_p/ω plots for the capacitor with Al_2O_3 are much higher than that with hBN. Consequently, the extracted interface-state densities, D_{it}, for capacitor with Al_2O_3 are much higher than that with hBN, shown in Fig. 3-7c and 3-7d. Previously it has been reported that the surface roughness in

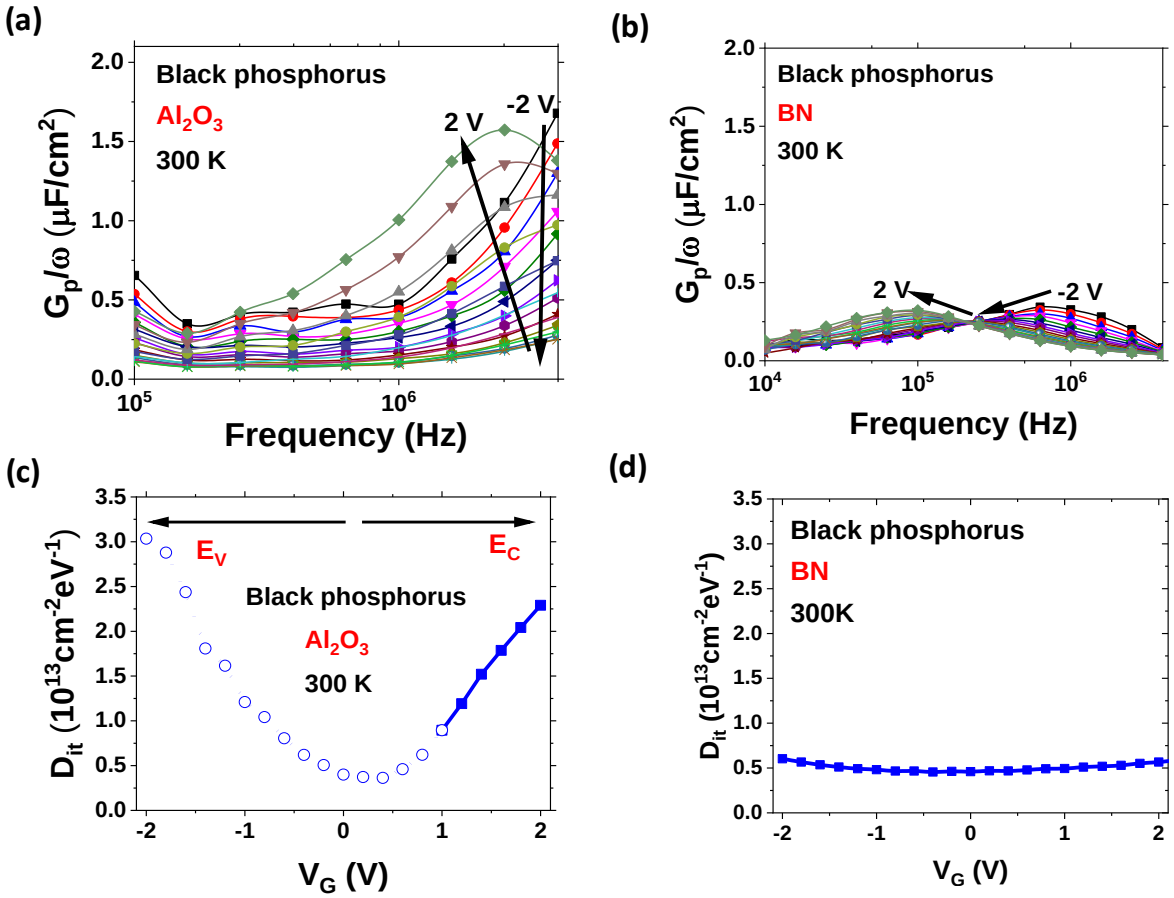

Figure 3-7. Impact of gate dielectric on the interface-state density. (a) G_p/ω as a function of frequency at various gate voltages measured on black phosphorus with Al_2O_3 gate dielectrics. (b) G_p/ω as a function of frequency at various gate voltages measured on black phosphorus with hBN as gate dielectrics. (c) Extracted interface-state density, D_{it}, as a function of temperature at various gate voltages for the black phosphorus capacitor with Al_2O_3 gate dielectric. (d) Extracted interface-state density, D_{it}, as a function of temperature at various gate voltages for the black phosphorus capacitor with hBN as gate dielectric.

crystalline hBN is much smaller than that in SiO_2, and this low interface-state density in hBN provides another advantage to using hBN as gate dielectrics.

3.2.3 Summary

In this section, we have systematically studied the capacitance and interface states of black phosphorus and WSe_2 capacitors with Al_2O_3 gate dielectrics. We found that the C-Vs in black phosphorus capacitors are ambipolar (symmetric about the minimum capacitance) and show low-frequency behavior even when the testing frequency is as high as 2.5 MHz, while the C-Vs in WSe_2 capacitors are unipolar (p-type) with high-frequency behavior even when the frequency is as low as 1 kHz. These dramatic differences in C-V characteristics can be explained by the difference in bandgap sizes and doping concentrations in these two materials. The narrow bandgap of the black phosphorus flake (~ 0.3 eV) results in ample minority carriers at room temperature, which gives low-frequency C-Vs in black phosphorus capacitors, while the large bandgap (1.21 eV) of WSe_2 results in the high-frequency C-Vs. The natural p-type doping in WSe_2 leads to unipolar C-Vs while the very low doping in black phosphorus yields ambipolar C-V characteristics. Although 2D materials are free of dangling bonds, the intimate contact of these 2D materials with high-k dielectrics can still generate a large number of interface traps. In this case, ALD Al_2O_3 is used as gate dielectric and the interface states can be as high as 10^{13} cm^{-2}/eV. These interface states can significantly degrade the performance of electronic devices based on 2D materials. The interface-state density in WSe_2 and black phosphorus shows strong voltage dependence. As the surface Fermi level shifts from midgap to the band edges, the interface-state density increases

exponentially. In addition, the interface trap density in BP/Al_2O_3 capacitors is several times higher than that in the BP/BN capacitors. This work provides valuable information on the interface states of black phosphorus and WSe_2. These characterization and analysis methods can be broadly applied to any 2D materials and serve as important tools for material selection, process optimization, and device design for 2D electronics and optoelectronics.

Chapter 4 Ferroelectric Hafnium Zirconium Oxide

In order to realize energy efficient electronic devices based on the hybrid stacks of ferroelectric metal oxides and 2D materials, we need to develop high-quality ferroelectric materials. In this project, we demonstrate ferroelectric hafnium zirconium oxide (HZO) with very high remanent polarization ($2P_r$ up to ~ 70 $\mu C/cm^2$), which serve as an important foundation for the graphene classifiers and reconfigurable devices to be discussed in Chapters 5 and 6.

4.1 Background of Ferroelectric Hafnium Oxide

Traditional ferroelectric materials like perovskite material ($PbZrO_3$, $BaTiO_3$, $PbTiO_3$)) are usually thick due to the size limits. Currently, this group of materials are usually prepared by complex sol-gel methods. On the other hand, polymer-based ferroelectric material like PVDF could be readily deposited by electrospun method, which has good processability but still has similar thickness limitation (~ typically several hundred nanometers). In a word, these materials based on current research progress are not ideal for the CMOS-compatible process [154].

HfO_2 is a dielectric with ε_r ~ 20 depending on the phase composition and large bandgap larger than 5eV. Thanks to its stable and inert property and high dielectric constants, it has been used as high-k gate dielectric in semiconductor industry since the gate dielectric scaling has been down to several nanometers [71]. It is found in the last decade that various dopants, such as Si, Zr, Al, Y, Gd, Sr, and La can induce ferroelectricity or

antiferroelectricity in thin HfO_2 films. The origin of the ferroelectricity of the doped HfO_2 films is attributed to formation of several kinds of polymorphs in the bulk phase based on the temperature and pressure. Among the 11 possible phases within the crystal (m-phase, t-phase, c-phase, different o phases, etc.), o-III and o-IV phases are verified to be accounting for the ferroelectricity in the layer. These phases are usually transformed from the non-ferroelectric m-phase with application of high temperature (annealing) and/or high pressure. The FE properties are highly related to the size and spatial distribution of the grain formation for different polymorphs, which is determined by the film thickness and annealing condition. It is found that the P_r value of the film could be highly affected by the thickness of the film since either too thin or too thick films could inhibit the formation of the ferroelectric o phases [155]. Also, a capping layer, for example, TiN, covering the doped-HfO_2 layer during annealing is reported to help the boost of P_r value. Researches pointed out this could be explained by the top capping layer's protection role to avoid shearing and volume expansion of the unit cells during the ferroelectric phase crystallization [78]. These TiN capping layer could also be used as electrodes afterwards.

Among the different dopants, Zirconium has been of great interest in the past years due to its low thermal budget requirement (~ 500 °C compared to ~ 1000 °C for aluminum dopant case) and high ratio tunability since $Hf_{0.5}Zr_{0.5}O_2$ has been demonstrated appealing FE properties, which could be just synthesized by 1:1 alternative HfO_2:ZrO_2 ALD growth [154]. For these merits, we are using Zr-doped HfO_2 as our ferroelectric material as the candidate for polarization storage purpose in our electronic device design.

4.2 Synthesis of Ferroelectric Hafnium Zirconium Oxide

We synthesized ferroelectric hafnium zirconium oxide using atomic layer deposition (ALD). HfO_2 and ZrO_2 layers were deposited alternatively by using the Hf precursor [tetrakis(dimethylamido)hafnium] and Zr precursor [tetrakis(dimethylamido)zirconium]. Then, we deposited Al_2O_3 by using Al precursor (trimethylaluminium). The encapsulated Zr-doped HfO_2 films were then annealed in a rapid thermal annealing (RTA) system. To characterize the film quality, we use Ti/Au as the top electrode (Fig. 4-1).

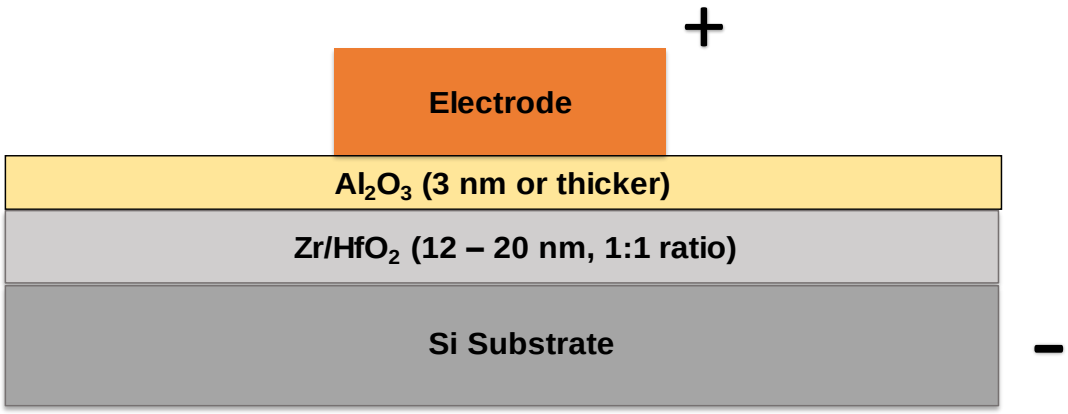

Figure 4-1. HZO film grown with Al_2O_3 capping layer and gold electrode.

4.3 Remanent Polarization of Ferroelectric Hafnium Zirconium Oxide

The polarization of the capacitors with ferroelectric hafnium zirconium oxide was measured using the positive-up-negative-down (PUND) method. The current is measured as a function of time using a Keithley semiconductor parameter analyzer (model 4200-SCS) equipped with a 4225-PMU ultra-fast I-V module. Figure 4-2 shows the extracted polarization as a function of electric field in various voltage ranges for a hafnium zirconium

oxide capacitor. A clear hysteresis loop is observed, indicating the successful formation of the ferroelectric phase in this hafnium zirconium oxide. We can see the remnant polarization increases monotonically with the program/erase voltage. At 10 V program/erase voltage, the $2P_r$ remnant polarization reaches ~ 45 μC/cm^2, indicating strong ferroelectricity in these hafnium zirconium oxide films.

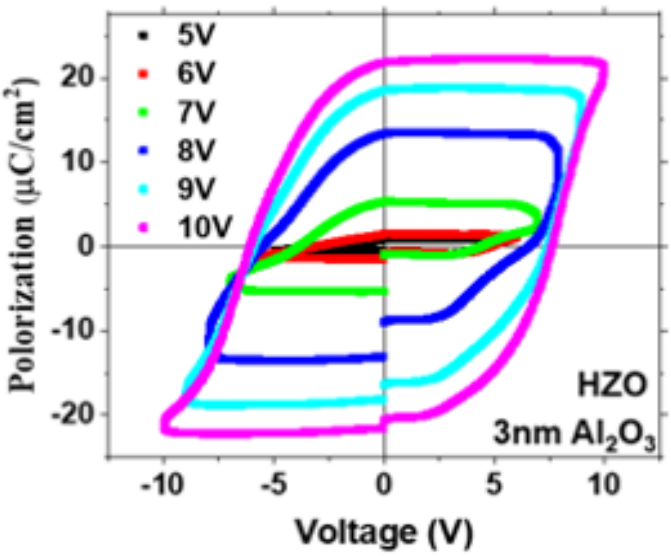

Figure 4-2. P-V loop for ferroelectric capacitor structure built in Fig. 4-1.

4.3.1 Influence of the Capping Layer on the Ferroelectricity of Hafnium Zirconium Oxide

In the ferroelectric phase transition, capping electrodes and bottom substrates play important roles [157-161]. It has been found that, with a TiN capping layer, the silicon doped HfO2 transformed into the orthorhombic ferroelectric phase after annealing, while without TiN capping layer confinement, a monoclinic/tetragonal phase mixture was formed [162]. For our devices (graphene classifiers and reconfigurable devices), we need the 2D materials to be in direct contact with the ferroelectric materials. These metal capping layer will short

the 2D channel. We found that Al_2O_3 can also serve as a capping layer. Figure 4-3 shows the P-V loops of the HZO capacitor annealed with and without Al_2O_3 capping layer. The HZO layer annealed with Al_2O_3 capping layer demonstrates much higher remnant polarization than that from HZO layer without capping layer. Adding thick Al_2O_3 layer can also help to reduce the leakage current between the probe pad and silicon substrate in the transistor structures.

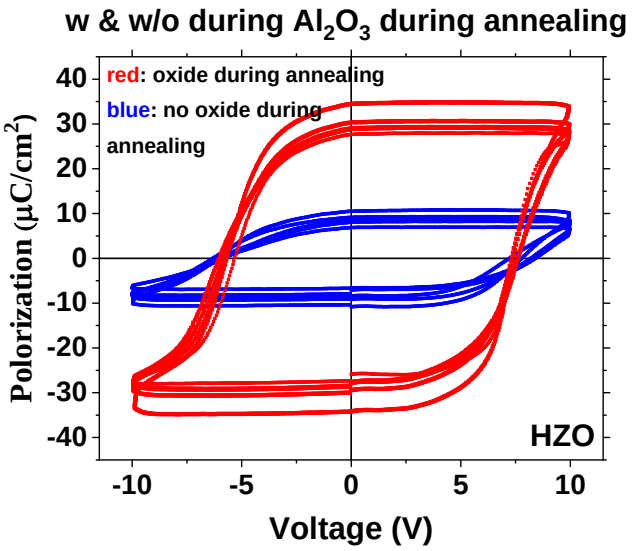

Figure 4-3. Polarization - Voltage loops of the HZO capacitors on silicon. For the 5 devices with red curves, 12 nm HZO and 20 nm Al_2O_3 capping layer are deposited sequentially on the silicon substrate and annealed at 500 °C. Then capping layer is then etched with phosphoric acid. For the 5 devices with blue curves, 12 nm HZO is annealed at 500 °C directly without capping layer deposition.

However, since the maximum pulse amplitude is 10 V in our instrument, if the Al_2O_3 layer is too thick, the voltage dropped on HZO layer will not be able to reach coercive voltage. Hence, we propose to use thick Al_2O_3 during annealing and then form an access window in the active channel region. Al_2O_3 layer is selectively etched in the active region using hot phosphoric acid. Device channel (described in Chapters 5 and 6) would be in proximity with

the HZO layer while the majority of electrode area would be sitting on the remaining Al_2O_3 protection layer, as shown in Fig. 4-4.

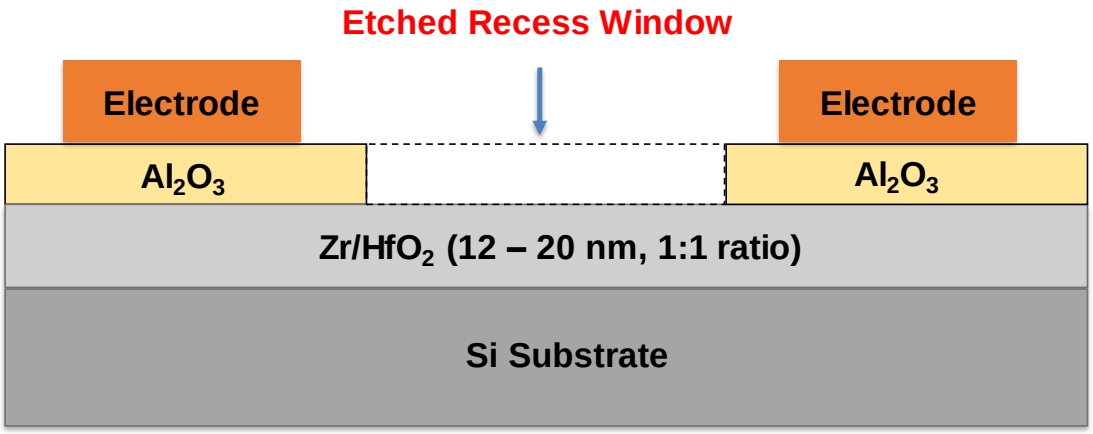

Figure 4-4. Demonstration of window-etching structure based on previously illustrated ferroelectric thin film.

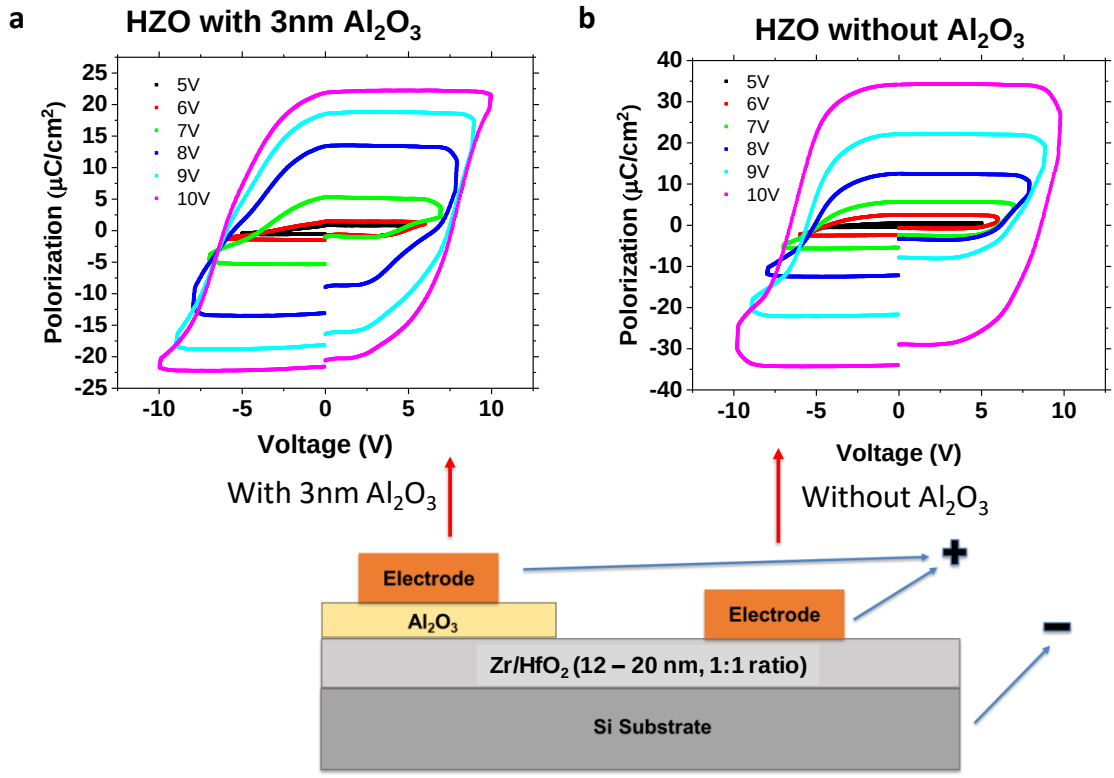

Figure 4-5. Polarization ~ voltage loops of the HZO capacitors on silicon. For both (a) and (b), 12 nm HZO and 3 nm Al_2O_3 are deposited on the silicon substrate and annealed at 500 °C. (a) Al_2O_3 is preserved before top gate electrode deposition. (b) Al_2O_3 layer is removed before metal deposition. The remnant polarization is larger for the capacitor with Al_2O_3 removal process at a given voltage.

We measure the remnant polarization in the etched region. As we see in Fig. 4-5, under 10V pulse, remanent polarization at 10V pulse amplitude increases from ~ 45 μC/cm^2 to ~ 70 μC/cm^2. Higher $2P_r$ value after Al_2O_3 etching can be attribute to the higher electric field across the FE layer. In addition, removing Al_2O_3 could reduce depolarization field from the top side, which in return enhances remanent polarization and retention.

4.3.2 Influence of 2D Material between HZO Layer and Electrode

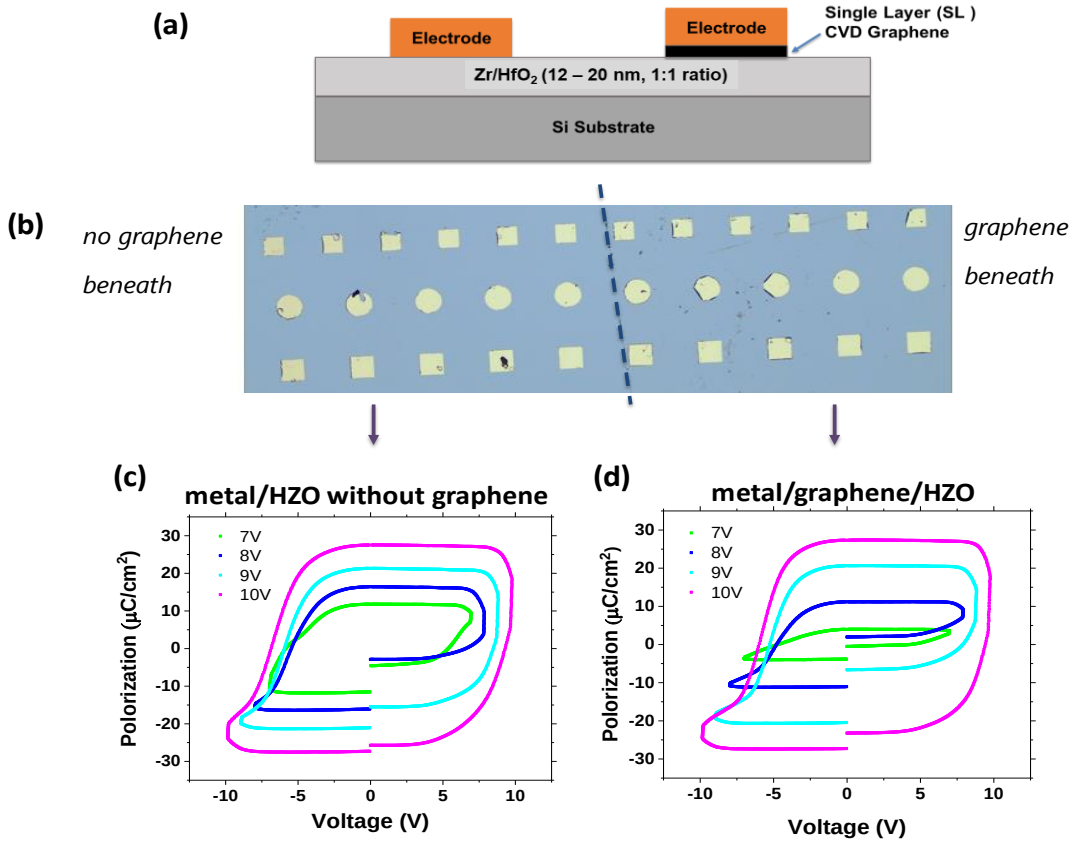

Figure 4-6. (a) Device cross section for FE capacitors with or without graphene beneath. (b) Optical image top view. (c) P-V loop measured on FE film with graphene beneath. (d) P-V loop measured on the same FE film without graphene beneath. We could see the single-layer graphene's influence is negligible.

For graphene classifier (Chapter 5) or other similar device structures, graphene needs to be integrated with HZO to utilize the induced polarization and electrodes are often

deposited on top. As shown in Fig. 4-6, we created two regions on HZO, with or without graphene covering on top. Our results show that the ferroelectricity can be preserved after inserting graphene layer due to the single-layer thickness of graphene.

4.4 Retention and Endurance of Ferroelectric Hafnium Zirconium Oxides

Retention and endurance are important metrics for the reliability of ferroelectric materials, especially for the memory applications. Figure 4-7a shows the retention of a ferroelectric HZO capacitor using Al_2O_3 etch-back process. The extrapolated lifetime is over 10 years at room temperature with ±9 V program pulses. The asymmetric retention curve is due to the asymmetric device structure: metal as top electrode and highly doped silicon as bottom electrode. The incomplete charge screening in semiconducting silicon can accelerate the depolarization of the dipoles within the ferroelectric film [156]. The endurance measurement of the HZO capacitor is shown in Fig. 4-7b. The rising polarization in the first several hundred of cycles can attribute "wake-up effect" [155]. These capacitors can endure ~ 4.9×10^4 cycles with ±8 V pulses before breakdown.

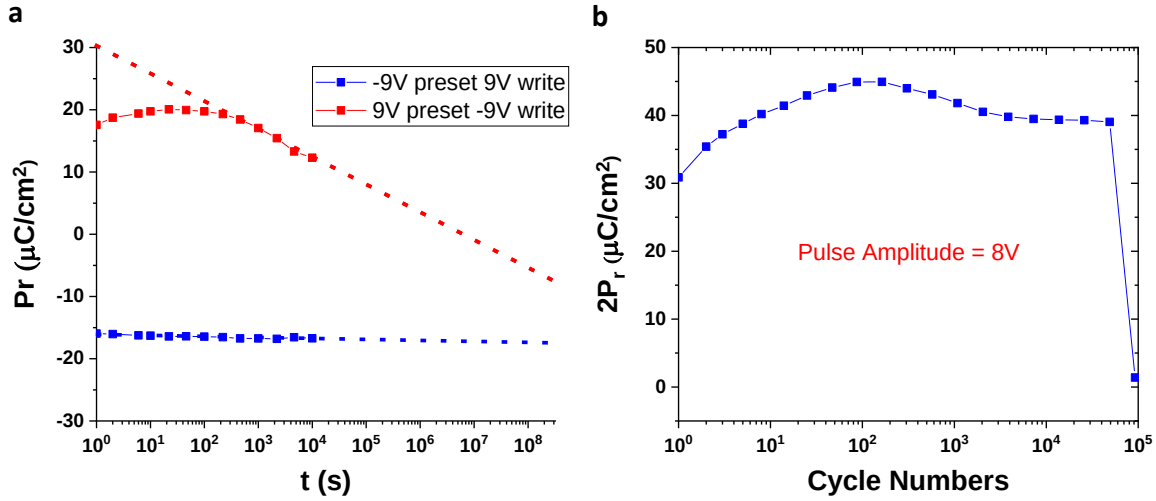

Figure 4-7. Retention and endurance measurements for HZO film grown.

Chapter 5 Non-Conventional Analog Classifiers Based on Ferroelectric Graphene Transistors

Image comparison is one of the essential building blocks for image processing and motion detection. In traditional classifiers based on CMOS logic transistors, each pixel needs 23 transistors, and the comparison function is carried out in four stages of calculation. In this chapter, we propose and demonstrate a new type of classifier incorporating 2D materials with ferroelectric material. Based on ferroelectric graphene transistors, our classifiers can perform the "comparison" function in the analog domain instead of the traditional digital domain. This new type of classifier utilizes the ambipolar transport and zero bandgap of the graphene to perform the |A-B| (absolute difference) function directly. Unlike the image classifier based on silicon CMOS, the classifier based on ferroelectric graphene transistors only needs ONE transistor per pixel, which will significantly reduce chip area and energy consumption. In addition, the operation frequency for the graphene classifier can exceed 100 GHz, which is several orders of magnitudes higher than that for silicon CMOS classifiers. More importantly, the embedded ferroelectric layer in the graphene transistor enables the non-volatile storage of the target image inside the analog device. Therefore, a single graphene transistor can perform both image storage and comparison functions concurrently. This in-memory computing will eliminate the need for frequent image loading/unloading, which will further reduce the power consumption related to the data transfer. This work opens a new path toward the design of novel nano-function circuits based on unique material properties that are absent in traditional circuits based on CMOS logic transistors and Von Neumann architectures.

5.1 Motivation and Background

Comparison between two signals is the basic function in signal processing and image recognition. This comparison function transitionally is implemented by CMOS logic devices. For current-mode classifiers based on CMOS, each pixel needs 23 transistors for the subtractor, absoluter, and squarer/divider blocks [157]. Consequently, this comparison function requires a significant amount of chip area and consumes a large amount of power. In addition, this type of circuit is very difficult to scale to large networks. Simulations have shown that using networks of interconnected nonlinear elements (such as SymFETs and BiSFETs) to process data coming from a large number of inputs in an analog fashion can dramatically reduce power consumption [158-160]. However, SymFETs and BiSFETs are based on negative differential resistance which has a very limited operating voltage range, and the two branches about the valley are usually not symmetrical, which can severely distort the output.

In this chapter, we propose and demonstrate a new type of classifier using embedded-gate ferroelectric graphene transistors, a stack of two-dimensional materials and ferroelectric metal oxides. These devices utilize graphene's unique ambipolar characteristics, symmetric mobility and zero bandgap to form analog devices to perform the "comparison" function, which can significantly reduce the number of transistors needed for each pixel in image recognition and signal processing circuits. The ferroelectric metal oxides (hafnium zirconium oxide) provide programmable and non-volatile doping in graphene, while the atomically thin body in 2D materials enables strong electrostatic control over the channel by the polarized ferroelectric metal oxides. As compared to traditional ferroelectric

materials such as perovskites, ferroelectric hafnium zirconium oxides have the advantages of excellent scalability, high coercive field, and full compatibility with CMOS [78, 79, 81-87].

5.2 Device Design and Operating Principle

We propose a novel device structure: embedded-gate ferroelectric graphene transistor, as a basic building block for a comparator, illustrated in Fig. 5-1a. The operating principle is as follows. The input voltage is applied to the top gate of the graphene transistor. A typical current voltage characteristic of a graphene transistor is illustrated in Fig. 5-1b. The channel current, I_{out}, increases linearly with the absolute distance between the input voltage and the target Dirac voltage: $|V_{in} - V_{Dirac}|$. Here the target Dirac voltage is determined by the polarization in the ferroelectric layer, which can be programmed by the pulses between the top and bottom gates, as illustrated in Fig. 5-1c. An array of these graphene transistors can be used as a classifier to recognize an image as illustrated in Fig. 5-1d to 5-1e. When the input image is the same as the target image, the total output current reaches a minimum. The value of the output current is a scalar indicator of the degree of matching between the input image and the target image. In this way, each pixel will only need one graphene transistor. As compared to the traditional CMOS based classifier, which needs 23 transistors per pixel, this graphene classifier circuit will consume a significantly smaller chip area and lower power. By using ferroelectric gate dielectrics in the graphene transistor, the information of the target image can be programed and stored as the level of polarization in the ferroelectric HfO_2. In this way, each graphene ferroelectric transistor will have both storage and analog

processing dual function. This local storage of the target image will significantly reduce the power consumption and operation latency related to the data transfer.

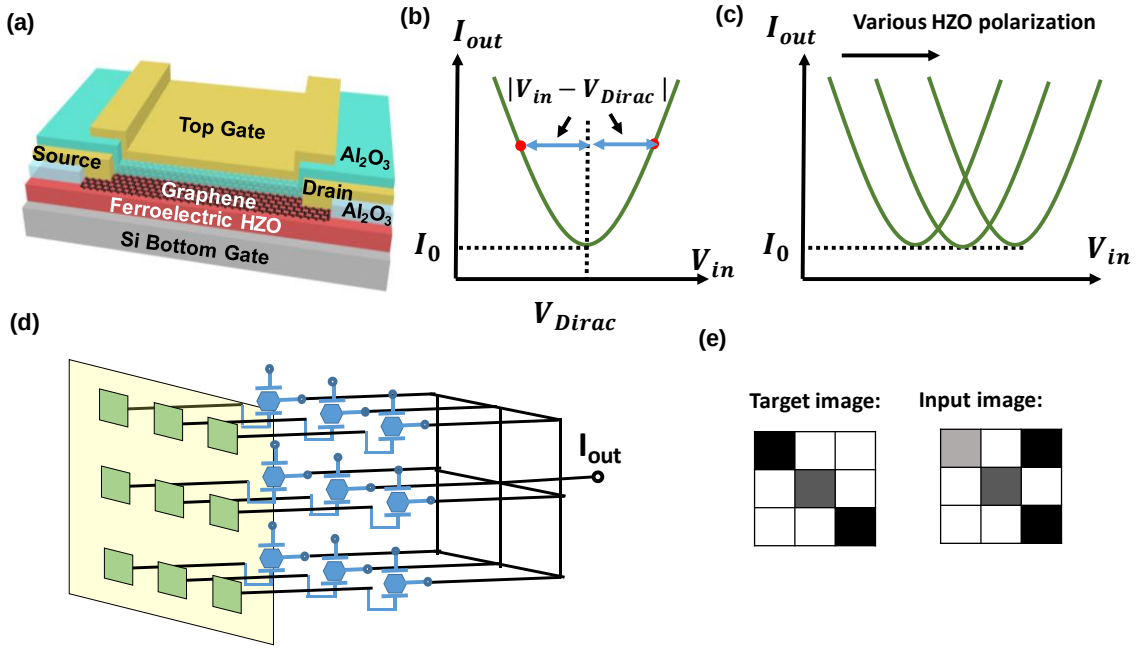

Figure 5-1. Device structure and operating principles of ferroelectric graphene transistor for analog comparison function. (a) Device structure. (b) I-V characteristics of graphene transistor illustrating that the output current I_{out} is determined by the distance between input voltage and Dirac voltage $|V_{in} - V_{Dirac}|$. (c) Illustration of the drain current as a function of input voltage on the top gate in the graphene transistor with various polarizations in the ferroelectric HZO layer. (d) Illustration of graphene transistor array as classifier for image recognition. (e) Illustration of a target image and an input image in grayscale.

5.3 Device Fabrication and Methods

Thin Zr-doped HfO_2 (12 nm) is deposited on highly doped silicon substrate followed by the deposition of 40 nm thick Al_2O_3 layer. RTA annealing at 500 °C is performed for 60 seconds to induce ferroelectric phase transformation. Our PUND measurement on calibration capacitor indicates a high remnant polarization ~ 35 μC/cm^2 with ±10 V pulses with Al_2O_3 removed (refer to Fig. 4-5b). A window is then patterned in the channel region and the Al_2O_3 layer is removed using hot phosphorus acid. Graphene is grown on copper using chemical vapor deposition method. After graphene formation, Poly(methylmethacrylate) (PMMA) is spin-coated on the top of the graphene layer. The Cu

foil is then dissolved in copper etchant. To minimize the damage of the graphene during the transfer, we use a one-touch wet-transfer method where the DI water is introduced into the container continuously [92]. Then graphene is patterned by lithography and O_2 plasma. Source/drain contacts (Cr/Au) are formed using photolithography and e-beam deposition. Next, 2 nm Al is deposited on the graphene and then re-oxidized to enhance the nucleation of the top gate dielectrics. Then 20 nm Al_2O_3 is deposited on top of the device using ALD. The top gate electrode (Cr/Au) is formed on the Al_2O_3 layer. All of the fast-sweep I-V measurements and pulse programming (with 4ms width) are done with Lakeshore cryo probe station and Keysight B-1500 analyzer. Our HZO PUND measurements are measured through Keithley 4225-PMU. The process flow is illustrated in Fig. 5-2.

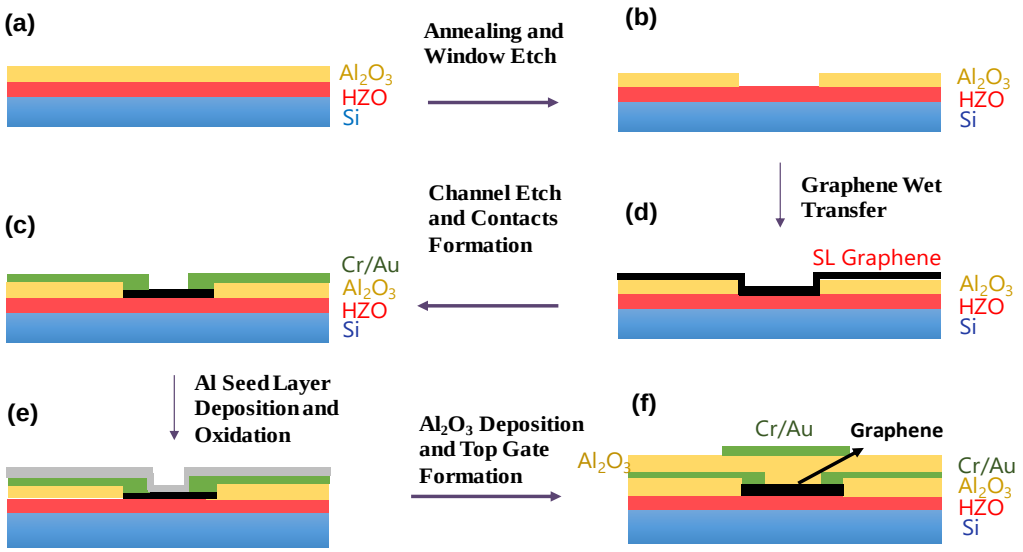

Figure 5-2. Process flow of the ferroelectric graphene transistor. (a) Zr-doped HfO_2 is deposited on highly doped silicon substrate followed by Al_2O_3 layer deposition. RTA annealing at 500 °C is performed to induce ferroelectric phase transformation. (b) A window is patterned in the channel region and the Al_2O_3 layer is removed using hot phosphorus acid. (c) CVD grown graphene is transferred onto the wafer using a one-touch transfer method. (d) Graphene is patterned by lithography and O_2 plasma. Source/drain contacts (Cr/Au) are formed using photolithography and e-beam deposition. (e) 2 nm Al is deposited on the graphene and then re-oxidized to enhance the nucleation of the top gate dielectrics. (f) 20 nm Al_2O_3 is deposited on top of the device using ALD. Top gate electrode (Cr/Au) is formed on the Al_2O_3 layer.

5.4 Tunable Polarization and Dirac Voltage in Ferroelectric Graphene FETs

Before ferroelectric layer programming, the transfer characteristics of the ferroelectric graphene transistor were measured. In order to eliminate the impact of the interface traps, the device was measured at low temperatures (80 K), as shown in Fig. 5-3. Notice that the Dirac voltage of the graphene transistor is close to zero, which is desired for the graphene classifier application, since both electron and hole branches are needed for the comparison function. The hysteresis is negligible, confirming that the interfacial trap effect is suppressed at this low temperature.

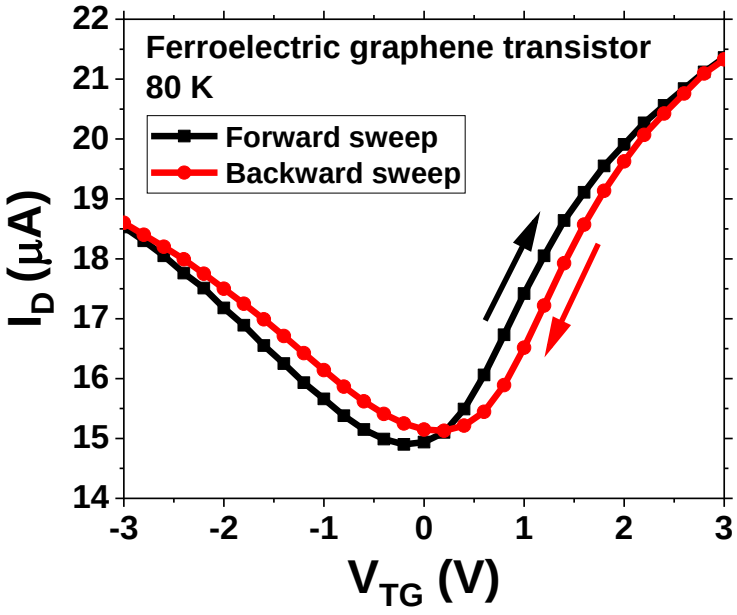

Figure 5-3. Double-sweep transfer curve of a fresh ferroelectric graphene transistor measured at 80 K. The hysteresis is negligible, indicating that the effect of the interfacial traps is suppressed at this low temperature.

The tunability of the polarization in HZO and its impact on the Dirac voltage of the ferroelectric graphene transistor were studied using two pulse schemes: opposite-polarity program pulses and preset-program pulses. In the opposite-polarity pulse scheme, a train of

program pulses with alternating polarities and incremental amplitudes are applied between the top gate and the silicon bottom gate on the fresh devices (Fig. 5-4a). The transfer curves of the graphene transistor before and after various program pulses are measured by sweeping the top gate voltage, shown in Fig. 5-4b. The extracted Dirac voltage is plotted as a function of program pulse amplitude (Fig. 5-4c). When the pulse amplitude is below the coercive voltage, there are negligible shifts in the Dirac voltage after program pulses. When the pulse amplitude exceeds the coercive voltage, the Dirac voltage shifts to the positive (negative) direction after positive (negative) program pulses are applied. The higher the pulse amplitude, the larger the shift in Dirac voltage.

The mechanism of the above phenomenon is illustrated in Fig. 5-4d. When a positive pulse is applied on the top gate, negative polarization charges are induced on the top surface of the HZO layer, which attract positive mobile charges in graphene. Therefore, the Dirac voltage shifts to the positive direction. When a negative pulse is applied on the top gate, positive polarization charges are induced on the top surface of the HZO layer, which attract negative mobile charges in graphene. Therefore, the Dirac voltage shifts to the negative direction. Note that in this pulse scheme, the polarization in HZO is a cumulative effect of all the pulses that have been applied on the device previously, since there is no reset or preset pulse in between the program pulses.

In order to quantify the effect of each individual program pulse on the polarization, a second pulse scheme is utilized, in which a preset pulse is applied before each program pulse, as illustrated in Fig. 5-5a and 5-5c. In this case, the polarization of HZO is reset to a constant level before each program pulse, which ensures a fair comparison of the polarization switching induced by various program pulses. Figure 5-5b shows the transfer curves of the

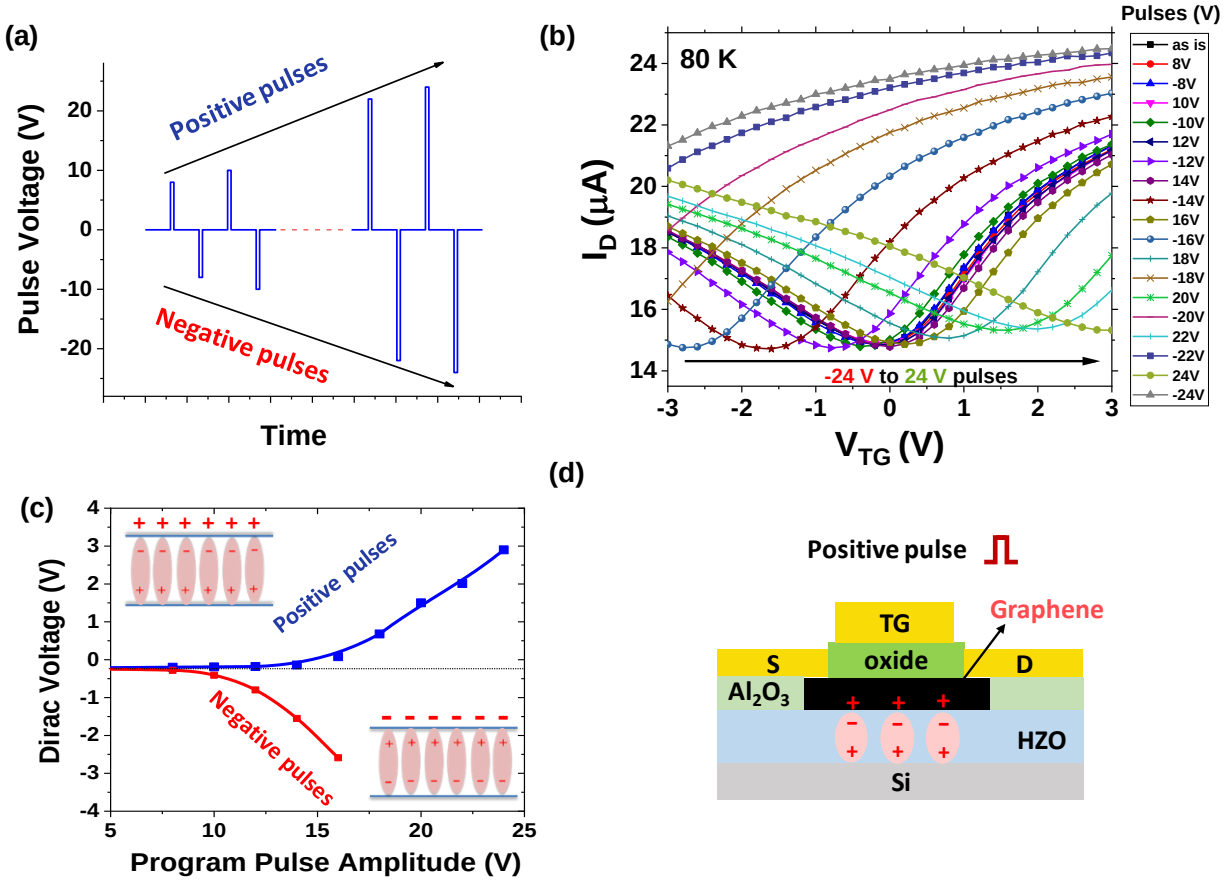

Figure 5-4. Polarization and Dirac voltage of a graphene transistor tested using opposite-polarity program pulses (the first pulse scheme) on a fresh device. (a) Waveform of the pulse train. Positive and negative program pulses are applied alternatively with progressively increasing pulse amplitudes. The pulse width is 4 ms and the pulse amplitude increases from 8 V to 24 V. A fast I_D–V_{TG} sweep is taken after each pulse to read the Dirac voltage. (b) Transfer characteristics of the graphene transistor before and after program pulses measured at 80 K. (c) Dirac voltage as a function of program pulse amplitude for both positive and negative pulses. The upper-left and lower-right insets illustrate the polarization charges in HZO and the induced screening charge in graphene after positive and negative pulses, respectively. (d) Illustration of the mechanism of the Dirac voltage shift induced by polarization. After a positive pulse is applied on the top gate, negative polarization charges are induced on the top surface of the HZO layer, which attract positive screening charges in graphene. As a result, the Dirac voltage shifts to the positive direction.

graphene transistor after preset and program pulses. After a -24 V preset pulse is applied, the graphene transistor shows strong electron transport and makes the Dirac voltage less than -3 V. After the positive program pulses with progressively increasing amplitude were applied on the gate, the Dirac voltage shifts monotonically to the positive direction, which is

consistent with the mechanism illustrated in Fig. 5-5d. The Dirac voltage is plotted as a function of pulse amplitude for both positive and negative program pulses, as shown in Fig. 5-5e. We can see that positive pulses induce positive shifts and negative pulses induce negative shifts in Dirac voltage. Approximately, the Dirac voltage and the program pulse amplitude follow a linear relationship for both positive and negative pulses. Based on this correlation, we can convert the target Dirac voltages to the program pulse voltages, which will be essential for realizing the image comparison function. Note that after each preset pulse (-24 V), the transfer curve shifts back to nearly the same location (Fig. 5-5b), which means that these preset pulses provide reliable and consistent reset of the polarization. In addition, minimum conductance at the charge neutrality point is nearly unchanged when we vary the program pulse amplitudes, which will be an important feature for image processing, so that the current from all pixels can be equally weighted, regardless of the target voltage value. These results indicate that ferroelectric graphene transistors can provide a promising hardware platform for image classification.

The transport of the ferroelectric graphene transistor is modeled using the following equation:

$$\sigma \approx \mu \sqrt{(en_{Dirac})^2 + {C_{TG}}^2 (V_{TG} - V_{Dirac})^2} \tag{5-1}$$

where σ is the conductivity of the graphene channel, n_{Dirac} is the carrier density at Dirac point, C_{TG} is the top gate capacitance, V_{Dirac} is the Dirac voltage, V_{TG} is the top gate voltage, and e is electron charge. The graphene channel resistance is $R_{ch} = \frac{l}{\sigma W}$, where l and W are the length and width of the graphene channel respectively. Considering the contact resistance R_c, the total resistance of the device can be expressed as $R_{total} = R_{ch} + R_c$. The

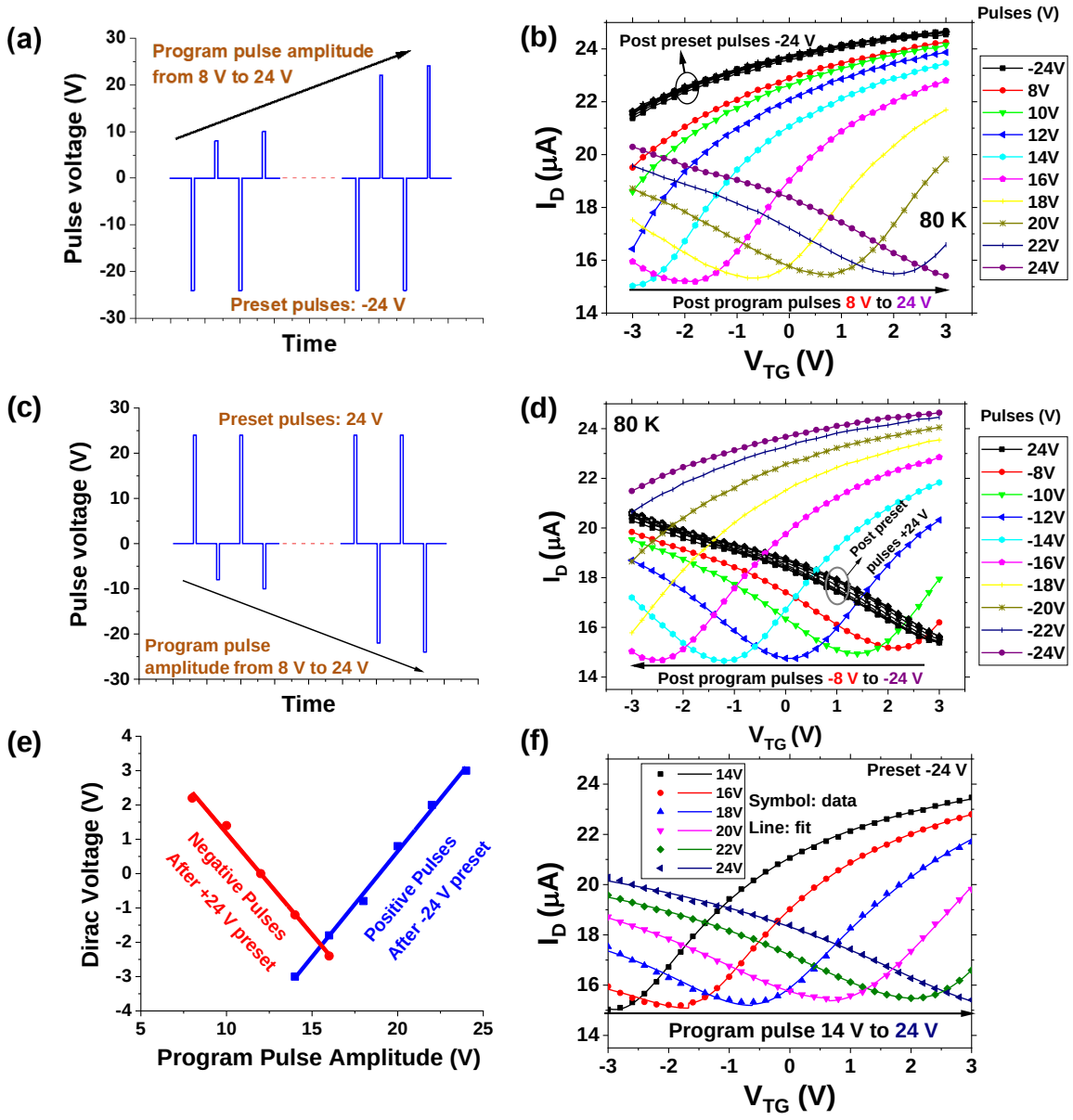

Figure 5-5. Polarization and Dirac voltage of graphene transistor tested using the preset-program pulses (the second pulse scheme). (a) and (c) Waveforms of the pulse train with positive and negative program pulses, respectively. A preset pulse is applied before each program pulse. The pulse width is 4 ms and the amplitude of the program pulse increases from 8 V to 24 V. A fast I_D–V_{TG} sweep is taken after each program pulse to read the Dirac voltage. (b) and (d) Transfer characteristics of the graphene transistor after positive and negative program pulses, respectively. The I_D–V_{TG} characteristics shift consistently with increasing pulse amplitude for both positive and negative pulses. (e) Extracted Dirac voltage as a function of program pulse amplitude for positive and negative program pulses. The Dirac voltages follow an approximate linear relationship with the pulse amplitude for both positive and negative program pulses. (f) Modeling of the transfer curves of the ferroelectric graphene transistor after positive program pulses. The symbols are measured data and the lines are fittings.

drain current can be calculated from $I_D = V_D/R_{total}$, where V_D is drain voltage. Figure 5-5f shows the measured data (symbols) versus the modeled result (solid lines). We can see that this model fits the experimental results very well. Based on this model, we can predict the drain current of the ferroelectric graphene transistor at any given input voltage V_{TG} for given Dirac voltage V_{Dirac}; i.e., we can predict the output current for a given pair of input and target images, discussed next.

5.5 Image Comparison Based on Graphene Classifier

The schematic of the graphene classifier array is illustrated in Fig. 5-6d. The graphene transistors are arranged into a 3 × 3 array, where the drain terminals are connected together, and the total drain current is monitored as the output current I_{out}. A photodetector array can be put on top of the graphene classifier. For each pixel, the output of the photodetector is linked to the top gate of the graphene classifier through a voltage amplifier. The Dirac voltage of each graphene transistor is programmed according to the target image. The drain current serves as a scalar indicator of the level of similarity between the input and target images. The detailed analysis follows.

The target image in grayscale (256 levels) is converted into a map of the Dirac voltages in the graphene transistor array, which is then converted into a map of program pulse voltages as shown in Fig. 5.6a - 5.6c. Based on the blue line in Fig. 5-6e, the image levels [0 to 255] correspond to the Dirac voltages [-3 V to 3 V] and program pulse voltage [14 V to 24 V]. The details of the conversion are approximated as:

The target image in grayscale is converted to the Dirac voltage (in volts) using the equation:

$$V_{Dirac} = -3 + \left(Graylevel\_target * \frac{6}{255}\right)$$

where Graylevel_target is the gray level in the target image.

Similarly, the input image in grayscale is converted to the top gate input voltage by:

$$V_{tg} = -3 + \left(Graylevel\_input * \frac{6}{255}\right)$$

where Graylevel_input is the gray level in the input image.

The program pulse amplitude is determined by the target Dirac voltage:

$$Amplitude = 14 + (V_{Dirac} + 3) * \frac{5}{3}$$

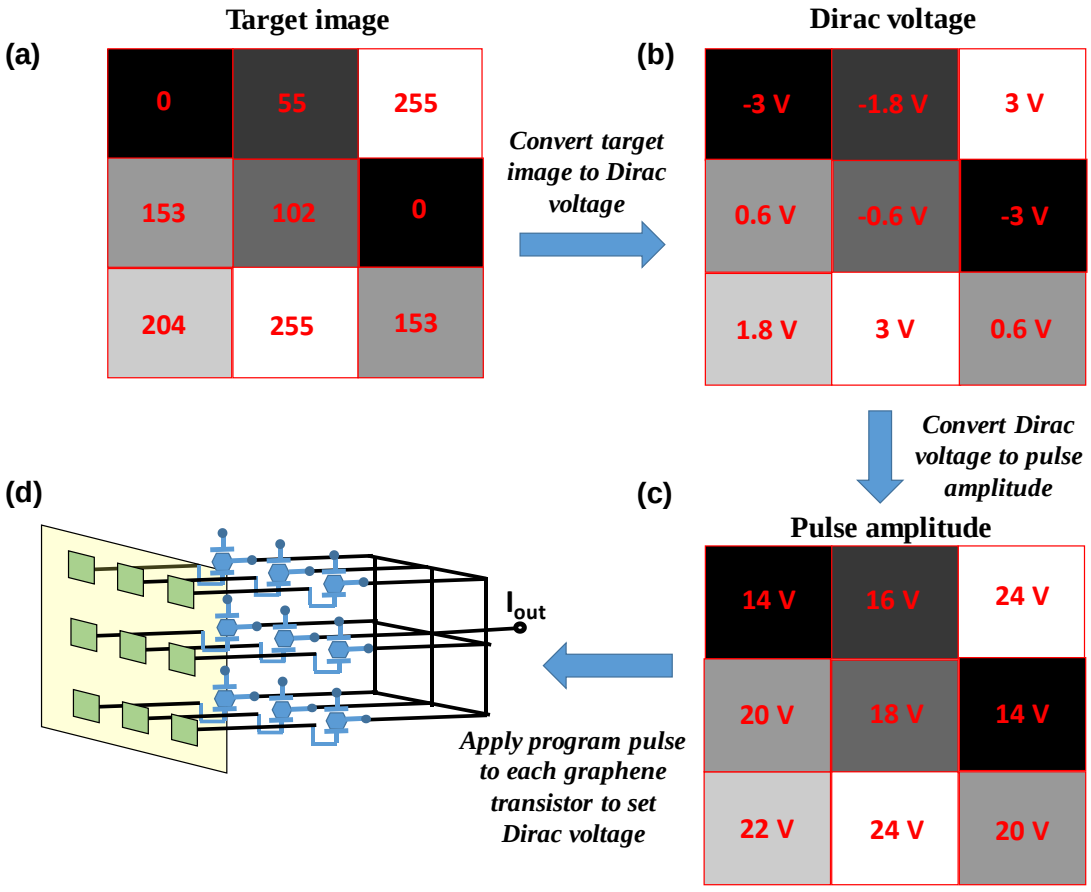

Figure 5-6. Programming graphene transistors according to a target image. (a) Target image with 3x3 pixels in grayscale (256-levels). (b) The target image is converted to a map of Dirac voltages in the graphene transistors. (c) The target Dirac voltages are translated into the program pulse voltages. (d) The program pulses are applied to the 3 x 3 array of ferroelectric graphene transistors to store the target image in the devices.

The input images in grayscale (256 levels) are translated to the map of the top gate voltages, as shown in Fig. 5-7. When the input image is the same as the target image (case 1), the top gate voltage is equal to the Dirac voltage at every graphene transistors in the array. The drain current reaches minimum at every transistor. As a result, the total output current reaches minimum $I_{out\_1} = 137.46$ μA. If the input image is similar, but not identical, to the target image (case 2), then the top gate voltage will be slightly different from the Dirac voltage in some graphene transistors. Thus the total output current will be slightly higher at $I_{out\_2} = 143.6$ μA. If the input image is very different from the target image (case 3), then the output current is significantly higher than that in case 1: $I_{out\_3} = 163.54$ μA. We can see that the total output current can serve as a scalar indicator of the similarity between the input and output images. The higher the similarity, the lower the total output current.

The comparison function in these classifiers is carried out in one step, which can be achieved at very high speed. In addition to the circuit simplicity, the extremely high mobility in graphene can further improve the operating speed. We have shown that the operating frequency of graphene transistors can be above 300 GHz [161], which means that the image comparison in graphene transistors can be completed within 10 ps. In contrast, the silicon CMOS based classifiers need four stages of calculation and the operating frequency is typically in MHz regime [157]. In addition, as compared to the 23 transistors required by the CMOS based classifier, the image classifier based on graphene transistor only needs one transistor per pixel, which can significantly reduce the chip area. More importantly, the target image is stored in the classifier array using a ferroelectric layer, which is non-volatile. This design can further reduce the energy consumption related to data storage and transportation. Furthermore, these graphene classifier arrays are especially suitable for

large networks, where the output current from each transistor can be directly summed up. Regardless of the number of units in the array, the operation time remains constant, which will be very important for sensor network applications.

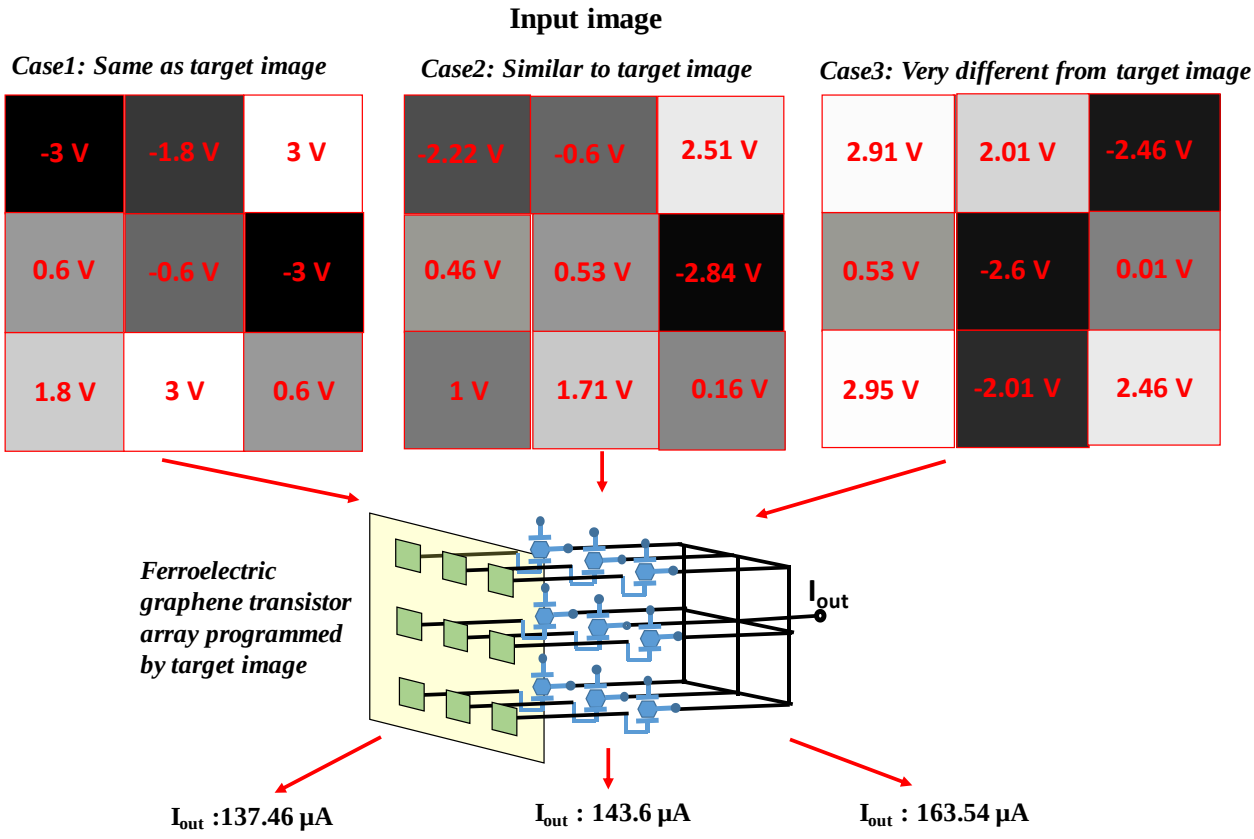

Figure 5-7. Comparison operation between the input and target images. Case 1: The input image is the same as the target image. Case 2: The input image is similar to the target image. Case 3: The input image is very different from the target image. These input images are converted to the maps of top gate voltages, labeled in red on each pixel. The corresponding total output currents for these three input images are 137.46 µA, 143.6 µA, and 163.54 µA respectively. The output current serves as a scalar indicator of the similarity level between the input and target images. Low output current represents high similarity between two images.

5.6 Future Directions for Improvements

As shown above in Fig. 5.3 – 5.5, our FET cell current transfer curve demonstrated "U" Valley instead of "V" shape, which makes it less sensitive to color change in close vicinity to

target depth level very close or are far away from target depth level. The asymmetry in I-V curve and shallower P-branch makes the outputs more sensitive for deeper color than target level. Improvements regarding to these aspects requires optimizing the graphene transfer and device fabrication process, which would reduce the non-ideal effects (such as doping from absorbates) for graphene's inherent properties. Besides, appropriate circuit design could potentially realize a transformation circuit to reshape the I-V curve to a more symmetric and linear output [162]. In addition, for a true classifier network circuit to work experimentally, it is desired to perform a statistical analysis for the variance of the devices' performance. If performance variance is considerable among devices, each single cell need an individual characterization and training.

Our demonstration above only has six levels, but we could characterize the device from measurements with more pulse levels. Alternatively, we could try a global fitting to predict the intermediate I-V shape between current levels.

5.7 Summary

In conclusion, we designed and demonstrated a new type of image classifier based on graphene ferroelectric transistors and highly optimized HZO ferroelectric layer. These devices utilize graphene's unique ambipolar characteristics and zero bandgap to form analog devices to perform the "comparison" function. The V-shaped transfer characteristics of the graphene transistor enable direct calculation of the absolute distance between two inputs. This graphene classifier only needs one graphene transistor per pixel as compared to 23 transistors per pixel in CMOS classifiers, significantly reducing the chip area of image recognition and signal processing circuits. More importantly, the operation frequency of the

graphene classifier can be over ~ 100 GHz, which is several orders of magnitude higher than that of a CMOS classifier. In addition, the non-volatile nature of ferroelectric hafnium oxide will eliminate the need for frequent image loading/unloading, which will further reduce the power consumption related to the data transfer. Its consistent and easy programmability enables dynamic operation flexibility. The analog classifiers based on graphene ferroelectric transistors will enable ultrahigh-speed image recognition and motion detection.

Chapter 6 Reconfigurable Logic Devices Based on Ferroelectric and 2D Materials

6.1 Motivation

A key limiting factor in current computing systems is the "memory bottleneck", the fact that more time and energy is spent transferring data between memory and computing than with the computation itself. In recent years, the processor-in-memory (PIM) architecture has been explored to address this problem, wherein a logic layer is 3D stacked with a DRAM layer, to reduce energy consumed in data transfer, while simultaneously increasing performance [158, 163]. However, 3D integration in these circuits was mainly achieved by stacking wafers/dies and interconnecting them vertically, using through-silicon vias (TSVs). This technique has drawbacks of high cost, long vertical distance between the wafers, and the very limited number of wafers that can be stacked. In addition, since the function of each logic blocks is fixed, the data still needs to be transferred between different logic blocks. In this project, we design and fabricate ferroelectric reconfigurable logic devices, which can be integrated with memory circuits monolithically and the function of the logic devices can be dynamically changed during operation. The logic circuits enabled by these reconfigurable devices can evolve with time based on the demand for the next operation or calculation. In this way, the "big data" is no longer needed to be transported from one logic block to another, instead one logic block on top or underneath the memory block can fulfill all the needed data analysis and processing operations. This technique will enable a new computing paradigm, where the process latency and energy consumption will no longer be limited by the memory bottleneck.

6.2 Background

In the past, the most common type of reconfigurable hardware is field-programmable gate array (FPGA). FPGAs contain an array of logic blocks, and a hierarchy of "reconfigurable interconnects" that allow the blocks to be "re-wired" in various configurations. In this design, a large amount of chip area is consumed by the networks of wires, memory arrays and logic control circuits for re-wiring the connections. Therefore, the circuits implemented by FPGA typically have low circuit density, low speed and high energy consumption. To overcome this limitation, reconfigurability at logic device level is needed.

In traditional silicon CMOS, the type of the transistor (nMOSFET or pMOSFET) is determined by the doping type at source/drain region, which is fixed once the fabrication is completed. N-type (p-type) doping at source/drain region leads to nMOSFET (pMOSFET). For 2D material-based transistors, however, the channel typically is not intentionally doped due to lacking of mature doping process. Therefore, most 2D transistors are Schottky barrier field-effect transistors (SB-FET), where the source and drain metal electrodes form Schottky contacts with 2D material channel. Depending on the metal work function, 2D material bandgap, electron affinity, and density/location of interface states, the 2D transistors can show n-type, p-type or ambipolar behavior [44-46, 51, 144, 164-166]. As a result, the device type is highly influenced by the thickness of 2D channel, metal contact materials, and process conditions.

Recently, it was demonstrated that the type of 2D transistors can be dynamically switched between nMOSFET and pMOSFET by electrostatic gating [50, 150, 167-170]. Figure 6-1 shows the optical image and schematic of a WSe_2 CMOS inverter implemented by

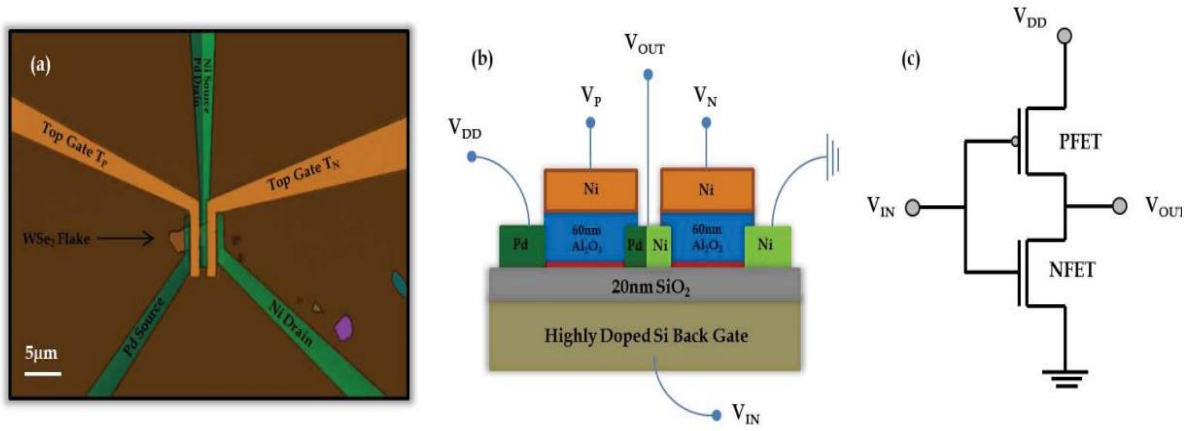

Figure 6-1. WSe2 CMOS inverter with (a) device false color optical image, (b) Schematic representation, and (c) circuit diagram of the inverter with electrostatic doping through top gate voltages V_P and V_N applied to T_P and T_N respectively. Pd is used as the contact electrode for the PFET and Ni is used as the contact electrode for the NFET. 60 nm Al_2O_3 is used as the top gate (program gate) dielectric and 20 nm SiO_2 is used as the back gate (control gate) dielectric.

electrostatic doping [167]. In addition to the global back gate, each transistor has a local program gate on the top of the channel. Figure 6-2a (2b) shows transfer characteristics of the PFET (NFET) with and without the program voltage -6V (6V) [167]. when a negative (positive) voltage is applied on the program gate of the PFET (NFET), the transfer curve shifts to the right (left), indicating that more hole (electron) is induced in the channel by the electrostatic gating. To further enhance the electron (hole) transport in the NFETs (PFETs), low work function metal Ni was used as the contacts for NFETs, while high work function metal Pd was used as the contacts for PFETs. Based on these complementary transistors, an inverter is demonstrated with a maximum gain of ~ 12 at V_{in} ~ 0.4 V and a noise margin of ~ 2 V. This device indicates that manipulating the types of the 2D transistors through electrostatic gating is feasible. However, these devices need continued voltage supply on the program gates to maintain the doping level, which will consume a large amount of power. In this project, we propose to develop ferroelectric reconfigurable devices, where the doping in

2D materials is determined by the non-volatile polarization in the ferroelectric materials, which will significantly reduce the energy consumption.

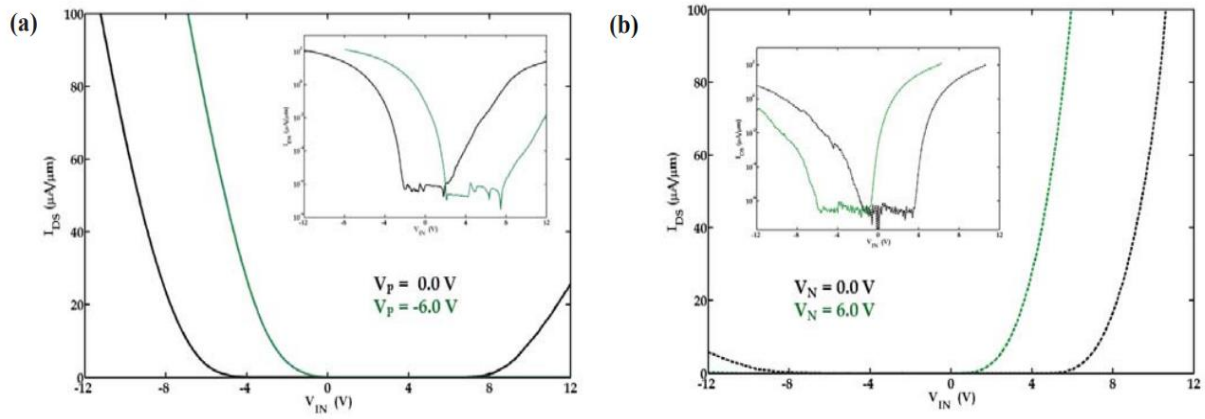

Figure 6-2. (a) Transfer characteristics of the PFET with top gate (polarity gate) biases V_P = 0.0 V and V_P = -6.0 V. (b) Transfer characteristics of the NFET with top gate biases V_P = 0.0 V and V_P = 6.0 V.

6.3 Device Structure and Operating Principle

The structure of the ferroelectric reconfigurable logic device we designed is illustrated in Fig. 6-3a. Two embedded gates are formed on the SiO2/Si substrates. A ferroelectric layer is deposited on the embedded gates. 2D material with narrow or moderate bandgap, such as black phosphorus and molybdenum ditelluride ($MoTe_2$), is transferred on the ferroelectric layer. Source/drain contacts are formed on the 2D channel. When program pulses are applied on the embedded gates, the direction and amplitude of the polarization in the ferroelectric layer can be modulated locally. These polarization charges will induce electrons or holes in the 2D materials under the source/drain contacts and dynamically change the transistor type from n to p or vice versa (Fig. 6-3b).

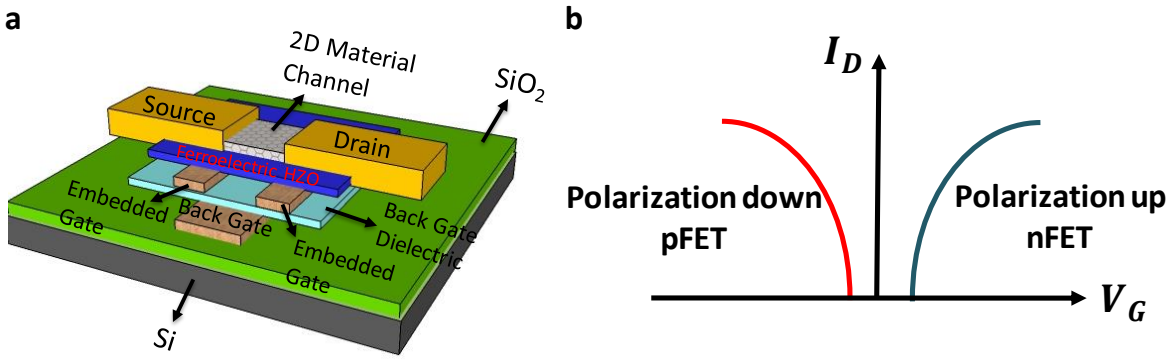

Figure 6-3. (a) An illustration for n/p reconfigurable device. (b) Its characteristics. The carrier polarity and modulation in 2D material is controlled through the dipoles switching in ferroelectric layer.

6.4 Device Fabrication

As a proof of concept on the electrostatically controlled reconfigurable device, we fabricated dual-gate black phosphorus MOSFETs (Fig. 6-4). A 12 nm ALD HZO is used as bottom dielectric while a 30 nm ALD Al_2O_3 by is used as top gate dielectric. Source/drain and top gate electrodes are deposited with 15 nm Cr/Au . The thickness of the black phosphorus flake is ~ 20nm.

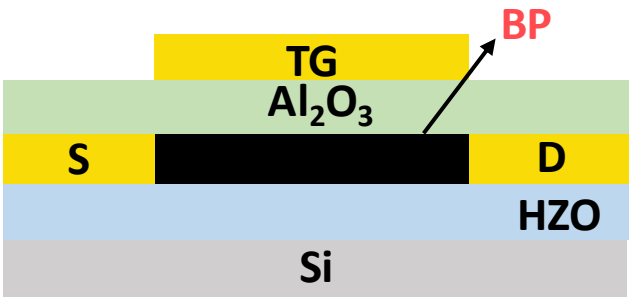

Figure 6-4. A double-gate black phosphorus FET fabricated. A positive back gate bias introduces n-doping.

For our prototype ferroelectric reconfigurable logic device (Fig. 6-5), we used $MoTe_2$ as the channel since it has moderate bandgap and ambipolar current transport. We first deposit ~ 15 nm HZO on highly doped silicon layer and then formed the recess window using the procedure described in Chapter 5. After a few-layers $MoTe_2$ flake is transferred into the window, a two-step optical lithography with two separate e-beam metal-deposition (~ 15 nm) is applied to deposit heterogeneous metal contacts at the drain and source sides to facilitate the transport for either electrons or holes (Explained in Section 6.5).

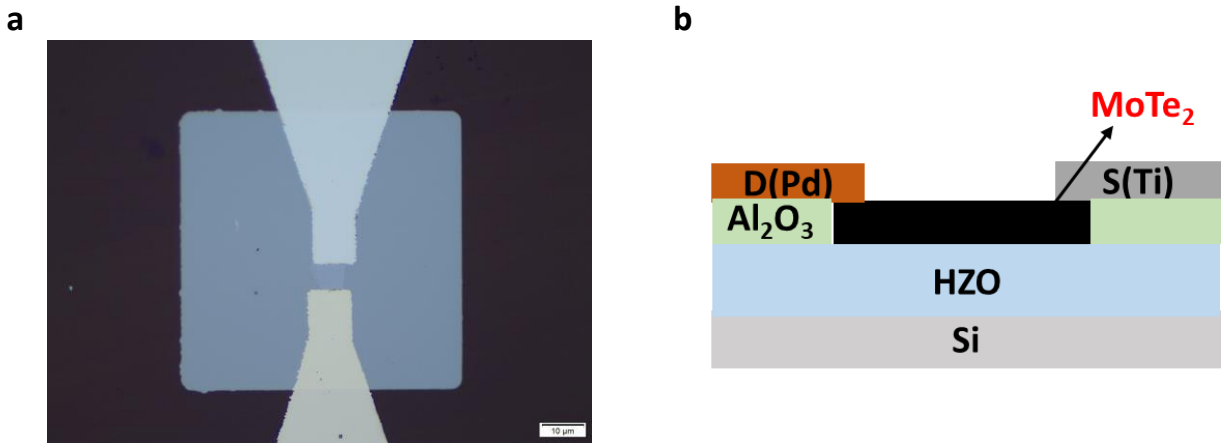

Figure 6-5. (a) Micrograph for our ferroelectric back gate $MoTe_2$ FET fabricated (top view). (b) Its structure shown from side view. A positive back gate pulse introduces n-doping.

6.5 Results and Analysis

Our dual-gate BP MOSFET shows dynamic switching between electron and hole transport. All three types of transport curves (p, ambipolar, and n) are observed with the program gate biased at 0 V, 1 V, 2V, respectively (Fig. 6-6). The effective tuning of the carrier polarity in these devices is attributed to the small bandgap of BP (E_g ~ 0.3 eV). These results

indicate the feasibility of dynamic reconfiguration of transport polarity by electrostatic gating.

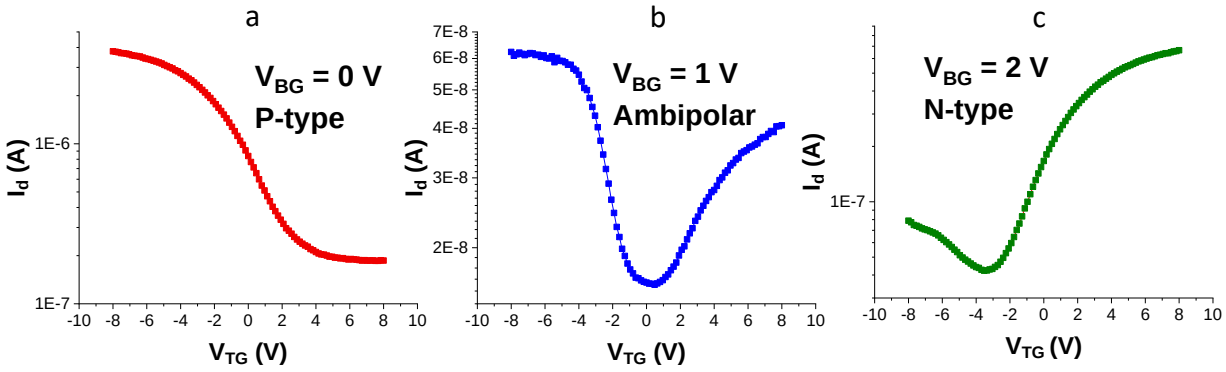

Figure 6-6. (a)-(c) A double-gate black phosphorus FET fabricated whose polarity could be switched by different back gate electrostatic doping.

Black phosphorus, however, is not thermodynamically stable in air. To further enhance the stability of the devices, we investigated ferroelectric reconfigurable devices based on $MoTe_2$. The bandgap of $MoTe_2$ is ~ 1eV, which is much larger than that of black phosphorus. To facilitate the electron and hole injection into the channel, we evaluated various contact metals. We found that low work function metals, such as Ti, facilitates electron injection, while high work function metal, such as Pd, enhances hole injection. In order to allow both electron and holes to participate the conduction, we fabricated asymmetric contact with Ti on the source and Pd on the drain side, shown in Fig. 6-5.

As illustrated in the energy diagram in Fig. 6-7a, when the $MoTe_2$ transistor has Ti contacts (low work function ~ 4.3 eV), the electron barrier at the metal/2D interface is small in favoring electron transport. On the other hand, when Pt contacts (large work function ~ 5.2 eV) is used, the injection barrier for hole is smaller, hence favoring hole transport (Fig. 6-7b). When we deposit asymmetric contacts featuring drain with Pd and source with Ti,

ambipolar transport is observed. The transfer characteristics of a $MoTe_2$ transistor measured at 80 K with asymmetric contact is shown in Fig. 6-7c. We can see a clear ambipolar conduction in the device. Since the positive drain bias is applied on the Pd contact, the hole can easily inject from the drain to the channel due to the smaller hole barrier at the drain side. In the meantime, the electrons can be easily injected from the source side due to

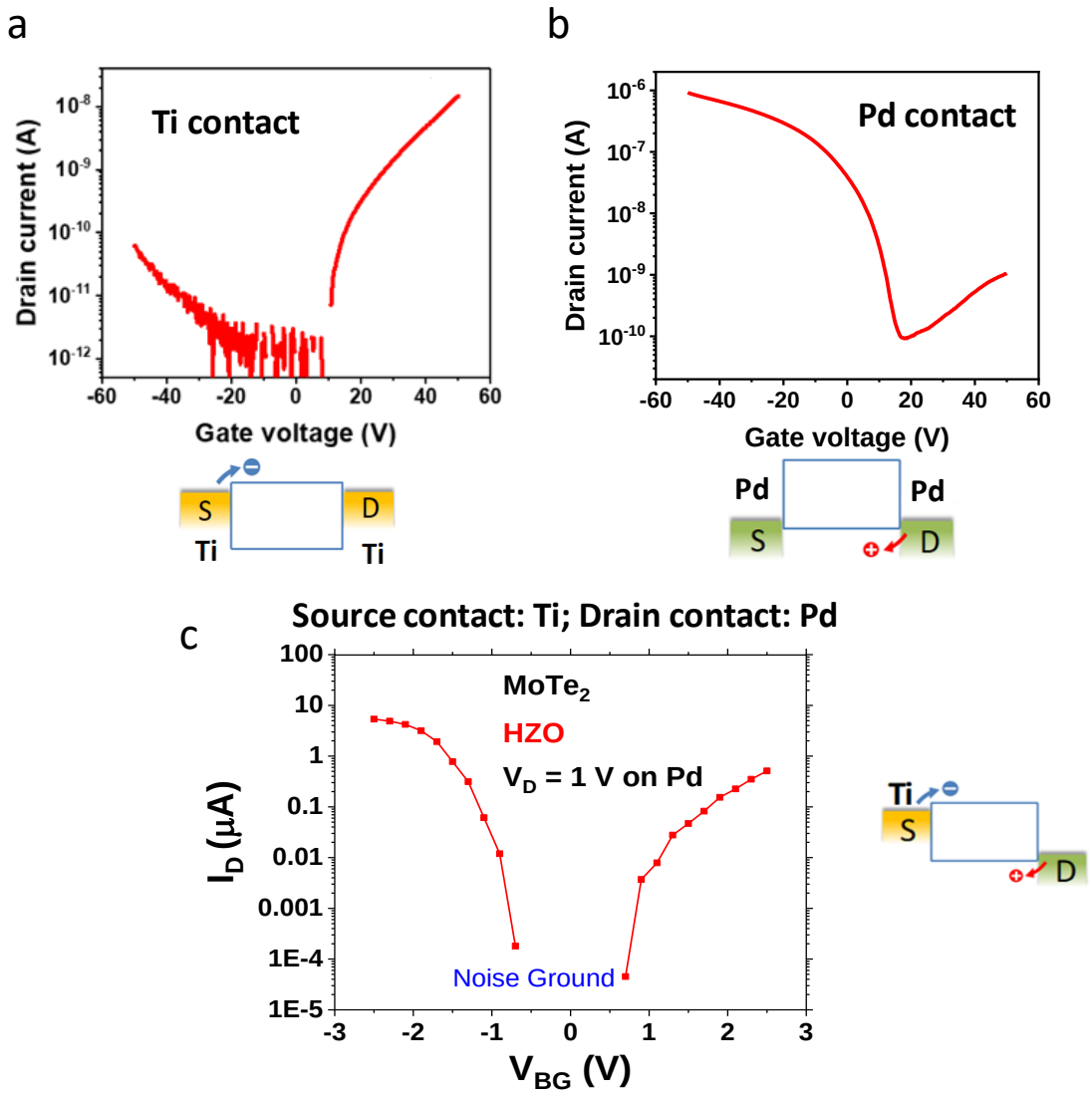

Figure 6-7. $MoTe_2$ MOSFET with different contact metal (a) n-branch dominant transfer characteristic facilitated by Ti contacts (b) p-branch dominant transfer characteristic facilitated by Pd contacts. (c) balanced p and n-branch transfer characteristic from asymmetric contacts. Data and figure in (a) and (b) with courtesy by group member Dr. Kai Xu.

the small electron barrier at the source side. Therefore, ambipolar transport is observed in this device.

Then we integrated ferroelectric hafnium zirconium oxide with the $MoTe_2$ transistors, aiming to achieve non-volatile switching of transistor polarity. In these devices, the carrier type and concentration of $MoTe_2$ channel can be modulated by the polarization of ferroelectric layer. Figure 6-8a shows the transfer curves of the $MoTe_2$ after +8V and -8V program pulses from the Si back gate. After positive program pulse is applied on the back gate while source and drain are grounded, the threshold voltage of the transistor shifts to the negative direction, which indicates n-doping in the channel. This is can be explained by the diagram in Fig. 6-8b. A positive back gate pulse will induce an upward polarization in the ferroelectric layer, which will attract electrons in the $MoTe_2$ channel. This result indicate that the threshold voltage can be modulated by the polarization in the ferroelectric film.

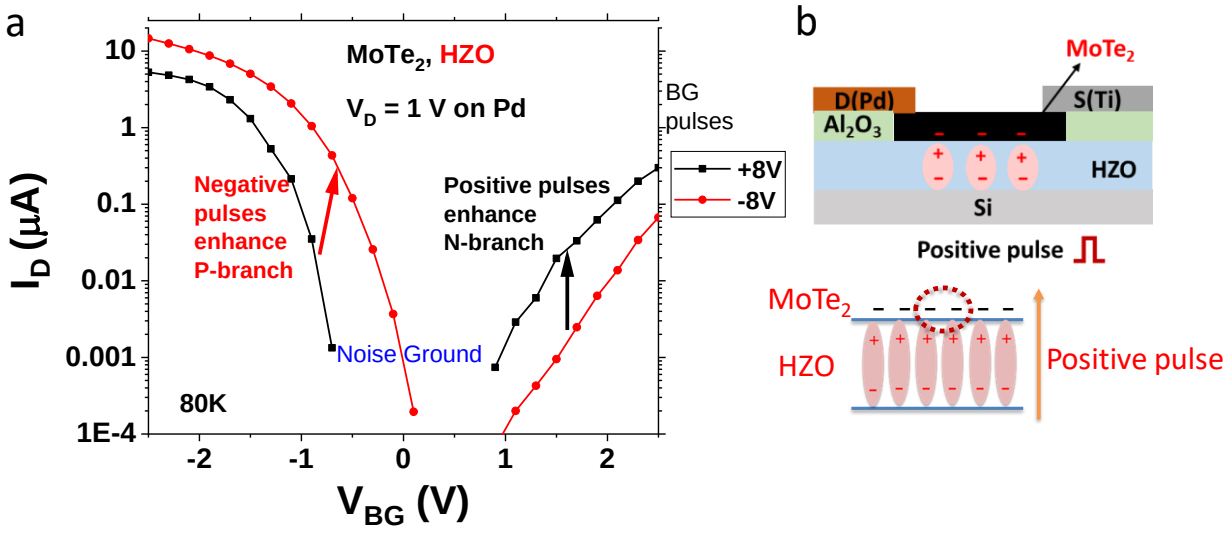

Figure 6-8. (a) Transfer curve shift with paired opposite pulse in agreement with ferroelectric polarization switching scheme. (b) Polarization orientation and the channel doping induced. The charge in circle dash line indicates the dipoles in the center channel region may not be fully polarized from the gate pulse due to an absence of top gate hence a potential lack of doping control in the $MoTe_2$ channel central region.

However, the I-V curves have not fully converted between n and p type. The possible reason is that, with the absence of the top gate, program pulses between the source/drain and bottom gate could not introduce sufficient electric field in the center channel region. In the future, we will further investigate the dual-gate structure and optimize the ferroelectric layers, aiming to further enhance the switching between n- and p-type characteristics.

Chapter 7. Conclusion and Future Work

7.1 Conclusion

In this thesis, we studied the electrical properties of 2D materials, developed ferroelectric hafnium zirconium oxide, and explored energy efficient analog and logic devices based on the hybrid stacks of ferroelectric dielectrics and 2D materials. The key results are summarized as follows.

We synthesized high-quality ferroelectric hafnium zirconium oxide with remanent polarization up to 35 $\mu C/cm^2$, endurance higher than 4.9×10^4 cycles, and retention over 10 years at room temperature. We found that Al_2O_3 capping layer and recess window process can effectively enhance the remanent polarization in hafnium zirconium oxide while reduce the leakage current under the source/drain contact pads in the transistors.

Based on these high-performance ferroelectric dielectrics, we successfully demonstrated ferroelectric graphene classifiers. These devices utilize graphene's unique ambipolar characteristics and zero bandgap to form analog devices to perform the "comparison" function. The V-shaped transfer characteristics of the graphene transistor enable direct calculation of the absolute distance between two inputs. This graphene classifier only needs one graphene transistor per pixel as compared to 23 transistors per pixel in CMOS classifiers, significantly reducing the chip area of image recognition and signal processing circuits. In addition, the non-volatile nature of ferroelectric hafnium oxide will eliminate the need for frequent image loading/unloading, which will further reduce the power consumption related to the data transfer. The analog classifiers based on graphene

ferroelectric transistors will enable ultrahigh-speed image recognition and motion detection.

Furthermore, we investigated ferroelectric reconfigurable logic devices. We found that black phosphorus transistors can be effectively switch from p-type, ambipolar to n-type by electrostatic gating. To make the reconfiguration non-volatile, we further investigated ferroelectric reconfigurable devices based on $MoTe_2$. We found that the threshold voltage of the $MoTe_2$ transistors can be modulated by the polarization in the ferroelectric film, which indicate the feasibility of these reconfigurable devices. These reconfigurable devices will enable the ultimate flexibility of circuit functionality and minimize the data transport, which will significantly increase energy efficiency in computing.

In addition, we studied the electrical properties of 2D materials. We proposed and demonstrated a new method to determine the bandgap of black phosphorus using C-V measurements. Based on the transition frequency, we can extract the bandgap of the semiconductor. A 0.30 eV bandgap is determined for thick black phosphorus flakes (50 nm). For comparison, we also extracted the bandgaps using minimum conductance and threshold voltage methods. The bandgaps extracted from the three methods are consistent with each other. This new method is especially useful for narrow and/or indirect bandgap materials, where photoluminescence measurements are beyond the spectrum range or detecting limit. We also systematically studied the interface states of black phosphorus and WSe_2 capacitors. Although 2D materials are free of dangling bonds, the intimate contact of these 2D materials with high-k dielectrics still generates a large number of interface traps. The interface states can be as high as 10^{13} $cm^{-2}eV^{-1}$ in BP/BN capacitors, while reduces to $\sim 5 \times 10^{12}$ $cm^{-2}eV^{-1}$ in

BP/BN capacitors. The interface state density in WSe_2 and black phosphorus shows strong voltage dependence. As the surface Fermi level shifts from midgap to the band edges, the interface-state density increases exponentially. These characterization and analysis methods can be broadly applied to other 2D semiconductors and serve as important tools for material selection, process optimization, and device design for 2D electronics and optoelectronics.

7.2 Future Work

In the future, we propose to further investigate the ferroelectric reconfigurable devices based on hafnium zirconium oxide and moderate bandgap 2D materials. We plan to investigate dual gate structure and optimize the top gate dielectrics to maintain the ambipolar characteristics of the $MoTe_2$ transistors against undesired interfacial doping. The dual-gate structure can further enhance the vertical electric field in the center channel region and facilitate the polarization switching. In addition, we will further optimize the synthesis of doped HfO_2 to enhance its ferroelectricity, aiming to demonstrate ferroelectric reconfigurable devices with prominent polarity switching. These new ferroelectric reconfigurable devices will help usher in a new computing paradigm that breaks the memory bottleneck of current computing systems. This new computing platform with high energy efficiency and high speed will have broad applications in computing and communication.

References

[1] R. R. Schaller, "Moore's law: past, present, and future," (in English), *IEEE Spectrum,* vol. 34, no. 6, pp. 52-59, Jun 1997.

[2] R. K. Cavin, P. Lugli, and V. V. Zhirnov, "Science and engineering beyond Moore's law," (in English), *Proceedings of the IEEE,* vol. 100, pp. 1720-1749, May 2012.

[3] B. V. Zeghbroeck, *Principles of Electronic Devices,* University of Colorado, CO, 2011. [Online]. Available: http://ecee.colorado.edu/~bart/book/

[4] F. D. Agostino and D. Querica, "Short Channel Effects in MOSFETs," project report for EECS 467, Department of Computer Science, University College London, 2000.

[5] X. Du, I. Skachko, A. Barker, and E. Y. Andrei, "Approaching ballistic transport in suspended graphene," *Nature Nanotechnology,* vol. 3, no. 8, pp. 491-495, 2008.

[6] R. Cheng *et al.*, "High-frequency self-aligned graphene transistors with transferred gate stacks," (in English), *Proceedings of the National Academy of Sciences of the United States of America,* vol. 109, no. 29, pp. 11588-11592, Jul 17 2012.

[7] K. S. Novoselov *et al.*, "Electric field effect in atomically thin carbon films," (in English), *Science,* vol. 306, no. 5696, pp. 666-669, Oct 22 2004.

[8] K. S. Novoselov, V. I. Fal'ko, L. Colombo, P. R. Gellert, M. G. Schwab, and K. Kim, "A roadmap for graphene," (in English), *Nature,* vol. 490, no. 7419, pp. 192-200, Oct 11 2012.

[9] M. Chhowalla, H. S. Shin, G. Eda, L.-J. Li, K. P. Loh, and H. Zhang, "The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets," *Nature Chemistry,* Review Article vol. 5, p. 263, Mar 20 2013.

[10] V. Fatemi *et al.*, "Electrically tunable low-density superconductivity in a monolayer topological insulator," (in English), *Science,* vol. 362, no. 6417, pp. 926-929, Nov 23 2018.

[11] E. Sajadi *et al.*, "Gate-induced superconductivity in a monolayer topological insulator," (in English), *Science,* vol. 362, no. 6417, pp. 922-925, Nov 23 2018.

[12] K. S. Novoselov, A. Mishchenko, A. Carvalho, and A. H. C. Neto, "2D materials and van der Waals heterostructures," (in English), *Science,* vol. 353, no. 6298, Jul 29 2016.

[13] E. J. Sie *et al.*, "An ultrafast symmetry switch in a Weyl semimetal," (in English), *Nature,* vol. 565, no. 7737, pp. 61-66, Jan 3 2019.

[14] Q. Ma *et al.*, "Observation of the nonlinear Hall effect under time-reversal-symmetric conditions," (in English), *Nature,* vol. 565, no. 7739, pp. 337-342, Jan 17 2019.

[15] B. Sipos, A. F. Kusmartseva, A. Akrap, H. Berger, L. Forro, and E. Tutis, "From Mott state to superconductivity in 1T-TaS($_2$)," (in English), *Nature Materials,* vol. 7, no. 12, pp. 960-965, Dec 2008.

[16] Y. J. Yu *et al.*, "Gate-tunable phase transitions in thin flakes of 1T-TaS_2," (in English), *Nature Nanotechnology,* vol. 10, no. 3, pp. 270-276, Mar 15 2015.

[17] X. X. Xi *et al.*, "Strongly enhanced charge-density-wave order in monolayer $NbSe_2$," (in English), *Nature Nanotechnology,* vol. 10, no. 9, pp. 765-769, Sep 2015.

[18] Y. I. Joe *et al.*, "Emergence of charge density wave domain walls above the superconducting dome in 1T-$TiSe_2$," (in English), *Nature Physics,* vol. 10, no. 6, pp. 421-425, Jun 2014.

[19] M. M. Ugeda *et al.*, "Characterization of collective ground states in single-layer NbSe2," (in English), *Nature Physics,* vol. 12, no. 1, pp. 92-U126, Jan 2016.

[20] X. X. Xi *et al.*, "Ising pairing in superconducting $NbSe_2$ atomic layers," (in English), *Nature Physics,* vol. 12, no. 2, pp. 139-143, Feb 2016.

[21] P. K. Das *et al.*, "Layer-dependent quantum cooperation of electron and hole states in the anomalous semimetal WTe_2," (in English), *Nature Communications,* vol. 7, Feb 2016.
[22] L. G. Ma *et al.*, "A metallic mosaic phase and the origin of Mott-insulating state in 1T-TaS_2," (in English), *Nature Communications,* vol. 7, Mar 2016.
[23] E. Navarro-Moratalla *et al.*, "Enhanced superconductivity in atomically thin TaS_2," (in English), *Nature Communications,* vol. 7, Mar 2016.
[24] M. Z. Yan *et al.*, "Lorentz-violating type-II Dirac fermions in transition metal dichalcogenide PtTe2," (in English), *Nature Communications,* vol. 8, Aug 15 2017.
[25] M. J. Allen, V. C. Tung, and R. B. Kaner, "Honeycomb carbon: A review of graphene," (in English), *Chemical Reviews,* vol. 110, no. 1, pp. 132-145, Jan 2010.
[26] E. Stolyarova *et al.*, "High-resolution scanning tunneling microscopy imaging of mesoscopic graphene sheets on an insulating surface," (in English), *Proceedings of the National Academy of Sciences of the United States of America,* vol. 104, no. 22, pp. 9209-9212, May 29 2007.
[27] S. Y. Zhou *et al.*, "Substrate-induced bandgap opening in epitaxial graphene," (in English), *Nature Materials,* vol. 6, no. 10, pp. 770-775, Oct 2007.
[28] Y. W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," (in English), *Physical Review Letters,* vol. 97, no. 21, Nov 24 2006.
[29] M. Y. Han, B. Ozyilmaz, Y. B. Zhang, and P. Kim, "Energy band-gap engineering of graphene nanoribbons," (in English), *Physical Review Letters,* vol. 98, no. 20, May 18 2007.
[30] C. R. Woods *et al.*, "Commensurate–incommensurate transition in graphene on hexagonal boron nitride," *Nature Materials,* vol. 6, pp. 770-775, 2007.
[31] H. Wang *et al.*, "BN/graphene/BN transistors for RF applications," (in English), *IEEE Electron Device Letters,* vol. 32, no. 9, pp. 1209-1211, Sep 2011.
[32] M. O'Brien and B. Nichols, "CVD synthesis and characterization of graphene thin films," report for Army Research Laboratary. [Online]. Available: https://www.arl.army.mil/arlreports/2010/ARL-TR-5047.pdf
[33] X. S. Li *et al.*, "Large-area synthesis of high-quality and uniform graphene films on copper foils," (in English), *Science,* vol. 324, no. 5932, pp. 1312-1314, Jun 5 2009.
[34] C. Riedl, C. Coletti, and U. Starke, "Structural and electronic properties of epitaxial graphene on SiC(0 0 0 1): A review of growth, characterization, transfer doping and hydrogen intercalation," (in English), *Journal of Physics D-Applied Physics,* vol. 43, no. 37, Sep 2 2010.
[35] D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, and M. C. Hersam, "Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides," (in English), *ACS Nano,* vol. 8, no. 2, pp. 1102-1120, Feb 2014.
[36] K. F. Mak, K. L. He, J. Shan, and T. F. Heinz, "Control of valley polarization in monolayer MoS_2 by optical helicity," (in English), *Nature Nanotechnology,* vol. 7, no. 8, pp. 494-498, Aug 2012.
[37] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS2 transistors," (in English), *Nature Nanotechnology,* vol. 6, no. 3, pp. 147-150, Mar 2011.
[38] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-performance single layered WSe2 p-FETs with chemically doped contacts," (in English), *Nano Letters,* vol. 12, no. 7, pp. 3788-3792, Jul 2012.
[39] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, and M. S. Strano, "Electronics and optoelectronics of two-dimensional transition metal dichalcogenides," (in English), *Nature Nanotechnology,* vol. 7, no. 11, pp. 699-712, Nov 2012.
[40] O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, and A. Kis, "Ultrasensitive photodetectors based on monolayer MoS_2," (in English), *Nature Nanotechnology,* vol. 8, no. 7, pp. 497-501, Jul 2013.

[41] W. Z. Wu *et al.*, "Piezoelectricity of single-atomic-layer MoS_2 for energy conversion and piezotronics," (in English), *Nature,* vol. 514, no. 7523, pp. 470-474, Oct 23 2014.
[42] C. Kim *et al.*, "Fermi level pinning at electrical metal contacts of monolayer molybdenum dichalcogenides," (in English), *ACS Nano,* vol. 11, no. 2, pp. 1588-1596, Feb 2017.
[43] C. Gong, L. Colombo, R. M. Wallace, and K. Cho, "The unusual mechanism of partial Fermi level pinning at metal-MoS_2 interfaces," (in English), *Nano Letters,* vol. 14, no. 4, pp. 1714-1720, Apr 2014.
[44] A. Allain and A. Kis, "Electron and hole mobilities in single-layer WSe_2," (in English), *ACS Nano,* vol. 8, no. 7, pp. 7180-7185, Jul 2014.
[45] C. J. Zhou *et al.*, "Carrier type control of WSe_2 field-effect transistors by thickness modulation and MoO3 layer doping," (in English), *Advanced Functional Materials,* vol. 26, no. 23, pp. 4223-4230, Jun 20 2016.
[46] Z. G. Wang *et al.*, "The ambipolar transport behavior of WSe_2 transistors and its analogue circuits," (in English), *NPG Asia Materials,* vol. 10, pp. 703-712, Aug 1 2018.
[47] S. Das and J. Appenzeller, "WSe_2 field effect transistors with enhanced ambipolar characteristics," (in English), *Applied Physics Letters,* vol. 103, no. 10, Sep 2 2013.
[48] C. Ruppert, O. B. Aslan, and T. F. Heinz, "Optical properties and band gap of single- and few-layer $MoTe_2$ crystals," (in English), *Nano Letters,* vol. 14, no. 11, pp. 6231-6236, Nov 2014.
[49] W. J. Zhao *et al.*, "Evolution of electronic structure in atomically thin sheets of WS_2 and WSe_2," (in English), *ACS Nano,* vol. 7, no. 1, pp. 791-797, Jan 2013.
[50] S. Nakaharai, M. Yamamoto, K. Ueno, Y. F. Lin, S. L. Li, and K. Tsukagoshi, "Electrostatically reversible polarity of ambipolar alpha-$MoTe_2$ transistors," (in English), *ACS Nano,* vol. 9, no. 6, pp. 5976-5983, Jun 2015.
[51] Y. F. Lin *et al.*, "Ambipolar $MoTe_2$ transistors and their applications in logic circuits," (in English), *Advanced Materials,* vol. 26, no. 20, pp. 3263-3269, May 28 2014.
[52] F. N. Xia, H. Wang, and Y. C. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics," (in English), *Nature Communications,* vol. 5, Jul 2014.
[53] S. Endo, Y. Akahama, S. Terada, and S. Narita, "Growth of large single-crystals of black phosphorus under high-pressure," (in English), *Japanese Journal of Applied Physics Part 2-Letters,* vol. 21, no. 8, pp. L482-L484, 1982.
[54] T. Nilges, M. Kersting, and T. Pfeifer, "A fast low-pressure transport route to large black phosphorus single crystals," (in English), *Journal of Solid State Chemistry,* vol. 181, no. 8, pp. 1707-1711, Aug 2008.
[55] J. B. Smith, D. Hagaman, and H. F. Ji, "Growth of 2D black phosphorus film from chemical vapor deposition," (in English), *Nanotechnology,* vol. 27, no. 21, May 27 2016.
[56] H. Liu *et al.*, "Phosphorene: An unexplored 2D semiconductor with a high hole mobility," (in English), *ACS Nano,* vol. 8, no. 4, pp. 4033-4041, Apr 2014.
[57] L. K. Li *et al.*, "Black phosphorus field-effect transistors," (in English), *Nature Nanotechnology,* vol. 9, no. 5, pp. 372-377, May 2014.
[58] A. Castellanos-Gomez *et al.*, "Isolation and characterization of few-layer black phosphorus," (in English), *2D Materials,* vol. 1, no. 2, Sep 2014.
[59] E. S. Reich, "Phospherene excites material scientists," *Nature Communications,* vol. 506, no. 19, 2014.
[60] G. Cassabois, P. Valvin, and B. Gil, "Hexagonal boron nitride is an indirect bandgap semiconductor," (in English), *Nature Photonics,* vol. 10, no. 4, pp. 262-266, Apr 2016.
[61] C. R. Dean *et al.*, "Boron nitride substrates for high-quality graphene electronics," (in English), *Nature Nanotechnology,* vol. 5, no. 10, pp. 722-726, Oct 2010.

[62] K. K. Kim *et al.*, "Synthesis and characterization of hexagonal boron nitride film as a dielectric layer for graphene devices," (in English), *ACS Nano,* vol. 6, no. 10, pp. 8583-8590, Oct 2012.
[63] I. Meric *et al.*, "Graphene field-effect transistors based on boron-nitride dielectrics," (in English), *Proceedings of the IEEE,* vol. 101, no. 7, pp. 1609-1619, Jul 2013.
[64] N. Petrone, T. Cheri, I. Meric, L. Wang, K. L. Shepard, and J. Hone, "Flexible graphene field-effect transistors encapsulated in hexagonal boron nitride," (in English), *ACS Nano,* vol. 9, no. 9, pp. 8953-8959, Sep 2015.
[65] G. H. Lee *et al.*, "Flexible and transparent MoS_2 field-effect transistors on hexagonal boron nitride-graphene heterostructures," (in English), *ACS Nano,* vol. 7, no. 9, pp. 7931-7936, Sep 2013.
[66] K. K. Kim *et al.*, "Synthesis of monolayer hexagonal boron nitride on Cu foil using chemical vapor deposition," (in English), *Nano Letters,* vol. 12, no. 1, pp. 161-166, Jan 2012.
[67] S. M. Kim *et al.*, "Synthesis of large-area multilayer hexagonal boron nitride for high material performance," (in English), *Nature Communications,* vol. 6, Oct 2015.
[68] K.-C. Kao, *Dielectric Phenomena in Solids: With Emphasis on Physical Concepts of Electronic Processes*. Amsterdam; Boston: Academic Press, 2004.
[69] S. O. Kasap, *Principles of Electronic Materials and Devices*, 3rd ed. Boston: McGraw-Hill, 2006.
[70] I. Bunget and M. Popescu, *Physics of Solid Dielectrics*. Amsterdam: Elsevier, 1984.
[71] S. M. Said, M. F. M. Sabri, and F. S. Salleh, *Ferroelectrics and Their Applications Reference Module in Materials Science and Materials Engineering*. Amsterdam: Elsevier, 2017.
[72] N. Setter *et al.*, "Ferroelectric thin films: Review of materials, properties, and applications," (in English), *Journal of Applied Physics,* vol. 100, no. 5, Sep 1 2006.
[73] J. F. Scott, "Ferroelectric random access memories - Fundamental and applications - Overview," (in English), *Ferroelectric Random Access Memories Fundamentals and Applications,* vol. 93, pp. 3-16, 2004.
[74] Y. Liao. "Retention & retention loss in ferroelectrics," *Practical Electron Microscopy and Database.* [Online]. Available: https://www.globalsino.com/EM/
[75] E. Mount, "Thin film materials technology; sputtering of compound materials," *Sci-Tech News,* Book Review vol. 58, no. 4, p. 61, 2004.
[76] N. Setter *et al.*, "Ferroelectric thin films: Review of materials, properties, and applications (vol 100, art no 051606, 2006)," (in English), *Journal of Applied Physics,* vol. 100, no. 10, Nov 15 2006.
[77] Y. Xu, *Ferroelectric Materials and Their Applications*. Amsterdam: Elsevier, 1991, pp. 1-391.
[78] T. S. Boscke *et al.*, "Phase transitions in ferroelectric silicon doped hafnium oxide," (in English), *Applied Physics Letters,* vol. 99, no. 11, Sep 12 2011.
[79] X. S. N. Gong, H. Jiang, Q. Xia and T. P. Ma, "Ferroelectricity of Al-doped HfO_2: Fast polarization switching, long retention and robust endurance," presented at the 46th IEEE Semiconductor Interface Specialists Conference, Arlington, VA, 2015.
[80] J. Müller *et al.*, "Ferroelectricity in yttrium-doped hafnium oxide," *Journal of Applied Physics,* vol. 110, no. 11, p. 114113, 2011.
[81] S. Mueller *et al.*, "Incipient ferroelectricity in Al-doped HfO_2 thin films," *Advanced Functional Materials,* vol. 22, no. 11, pp. 2412-2417, 2012.
[82] S. Mueller, C. Adelmann, A. Singh, S. Van Elshocht, U. Schroeder, and T. Mikolajick, "Ferroelectricity in Gd-Doped HfO_2 thin films," *ECS Journal of Solid State Science and Technology,* vol. 1, no. 6, pp. N123-N126, January 1 2012.
[83] T. Schenk *et al.*, "Strontium doped hafnium oxide thin films: Wide process window for ferroelectric memories," in *Solid-State Device Research Conference (ESSDERC), 2013 Proceedings of the European*, 2013, pp. 260-263.

[84] J. Muller *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," (in English), *2013 IEEE International Electron Devices Meeting (IEDM),* 2013.
[85] E. Yurchuk *et al.*, "Impact of scaling on the performance of HfO_2-based ferroelectric field effect transistors," (in English), *IEEE Transactions on Electron Devices,* vol. 61, no. 11, pp. 3699-3706, Nov 2014.
[86] U. Schroeder *et al.*, "Hafnium oxide based CMOS compatible ferroelectric materials," (in English), *ECS Journal of Solid State Science and Technology,* vol. 2, no. 4, pp. N69-N72, 2013.
[87] A. Chernikova *et al.*, "Ultrathin $HfZr_{0.5}O_2$ ferroelectric films on Si," (in English), *ACS Applied Materials & Interfaces,* vol. 8, no. 11, pp. 7232-7237, Mar 23 2016.
[88] J. F. Scott, C. A. Araujo, H. B. Meadows, L. D. Mcmillan, and A. Shawabkeh, "Radiation effects on ferroelectric thin-film memories - Retention failure mechanisms," (in English), *Journal of Applied Physics,* vol. 66, no. 3, pp. 1444-1453, Aug 1 1989.
[89] J. T. Evans, "Charcterizing ferroelectric materials," Radiant Technologies, Inc, 2011. [Online]. Available: https://www.ferrodevices.com/1/297/files/Ferroelectric_Properties_and_Instrumentation.pdf
[90] T. Nishimatsu. *Program "feram"*. [Online]. Available: http://loto.sourceforge.net/feram/
[91] S. Lee and K. Kim, "Current development status and future challenges of ferroelectric random access memory technologies," (in English), *Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers,* vol. 45, no. 4b, pp. 3189-3193, Apr 2006.
[92] C. Baeumer, S. P. Rogers, R. Xu, L. W. Martin, and M. Shim, "Tunable carrier type and density in graphene/$PbZr_{0.2}Ti_{0.8}O_3$ hybrid structures through ferroelectric switching," *Nano Letters,* vol. 13, no. 4, pp. 1693-1698, Apr 10 2013.
[93] H. M. Wang, Y. H. Wu, C. X. Cong, J. Z. Shang, and T. Yu, "Hysteresis of electronic transport in graphene transistors," (in English), *ACS Nano,* vol. 4, no. 12, pp. 7221-7228, Dec 2010.
[94] A. Lipatov, P. Sharma, A. Gruverman, and A. Sinitskii, "Optoelectrical molybdenum disulfide (MoS_2)-ferroelectric memories," (in English), *ACS Nano,* vol. 9, no. 8, pp. 8089-8098, Aug 2015.
[95] Y. Zheng, G. X. Ni, C. T. Toh, C. Y. Tan, K. Yao, and B. Ozyilmaz, "Graphene field-effect transistors with ferroelectric gating," (in English), *Physical Review Letters,* vol. 105, no. 16, Oct 11 2010.
[96] Y. T. Lee *et al.*, "Nonvolatile ferroelectric memory circuit using black phosphorus nanosheet-based field-effect transistors with P(VDF-TrFE) polymer," (in English), *ACS Nano,* vol. 9, no. 10, pp. 10394-10401, Oct 2015.
[97] M. W. Si, P. Y. Liao, G. Qiu, Y. Q. Duan, and P. D. Ye, "Ferroelectric field-effect transistors based on MoS_2 and $CuInP_2S_6$ two-dimensional van der Waals heterostructure," (in English), *ACS Nano,* vol. 12, no. 7, pp. 6700-6705, Jul 2018.
[98] W. C. Yap, H. Jiang, J. L. Liu, Q. F. Xia, and W. J. Zhu, "Ferroelectric transistors with monolayer molybdenum disulfide and ultra-thin aluminum-doped hafnium oxide," (in English), *Applied Physics Letters,* vol. 111, no. 1, Jul 3 2017.
[99] M. Yi and Z. G. Shen, "A review on mechanical exfoliation for the scalable production of graphene," (in English), *Journal of Materials Chemistry A,* vol. 3, no. 22, pp. 11700-11715, 2015.
[100] I. Jung *et al.*, "Simple approach for high-contrast optical imaging and characterization of graphene-based sheets," (in English), *Nano Letters,* vol. 7, no. 12, pp. 3569-3575, Dec 2007.
[101] Q. H. Wang *et al.*, "Understanding and controlling the substrate effect on graphene electron-transfer chemistry via reactivity imprint lithography," (in English), *Nature Chemistry,* vol. 4, no. 9, pp. 724-732, Sep 2012.
[102] G. F. Schneider, V. E. Calado, H. Zandbergen, L. M. K. Vandersypen, and C. Dekker, "Wedging transfer of nanostructures," (in English), *Nano Letters,* vol. 10, no. 5, pp. 1912-1916, May 2010.

[103] P. J. Zomer, S. P. Dash, N. Tombros, and B. J. van Wees, "A transfer technique for high mobility graphene devices on commercially available hexagonal boron nitride," (in English), *Applied Physics Letters,* vol. 99, no. 23, Dec 5 2011.
[104] A. Castellanos-Gomez *et al.*, "Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping," (in English), *2D Materials,* vol. 1, no. 1, Jun 2014.
[105] L. M. Malard, M. A. Pimenta, G. Dresselhaus, and M. S. Dresselhaus, "Raman spectroscopy in graphene," (in English), *Physics Reports-Review Section of Physics Letters,* vol. 473, no. 5-6, pp. 51-87, Apr 2009.
[106] V. Loryuenyong, K. Totepvimarn, P. Eimburanapravat, W. Boonchompoo, and A. Buasri, "Preparation and characterization of reduced graphene Oxide sheets via water-based exfoliation and reduction methods," (in English), *Advances in Materials Science and Engineering,* 2013.
[107] J. L. Liu, Y. J. Zhou, and W. J. Zhu, "Dielectric-induced interface states in black phosphorus and tungsten diselenide capacitors," (in English), *Applied Physics Letters,* vol. 113, no. 1, Jul 2 2018.
[108] A. Castellanos-Gomez *et al.*, "Isolation and characterization of few-layer black phosphorus," (in English), *2D Materials,* vol. 1, no. 2, pp. 1-19, Sep 2014, Art. no. 025001.
[109] V. Tran, R. Soklaski, Y. F. Liang, and L. Yang, "Layer-controlled band gap and anisotropic excitons in few-layer black phosphorus," (in English), *Physical Review B,* vol. 89, no. 23, pp. 1-6, Jun 26 2014, Art. no. 235319.
[110] X. M. Wang *et al.*, "Highly anisotropic and robust excitons in monolayer black phosphorus," (in English), *Nature Nanotechnology,* vol. 10, no. 6, pp. 517-521, Jun 2015.
[111] S. Das, W. Zhang, M. Demarteau, A. Hoffmann, M. Dubey, and A. Roelofs, "Tunable transport gap in phosphorene," (in English), *Nano Letters,* vol. 14, no. 10, pp. 5733-5739, Oct 2014.
[112] A. V. Penumatcha, R. B. Salazar, and J. Appenzeller, "Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model," (in English), *Nature Communications,* vol. 6, pp. 1-8, Nov 2015, Art. no. 8948.
[113] Y. Cai, G. Zhang, and Y. W. Zhang, "Layer-dependent band alignment and work function of few-layer phosphorene," *Scientific Reports,* vol. 4, 2014, Art. no. 6677.
[114] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982, p. 906.
[115] S. J. Liu *et al.*, "Thickness-dependent Raman spectra, transport properties and infrared photoresponse of few-layer black phosphorus," (in English), *Journal of Materials Chemistry C,* vol. 3, no. 42, pp. 10974-10980, 2015.
[116] B. C. Deng *et al.*, "Efficient electrical control of thin-film black phosphorus bandgap," (in English), *Nature Communications,* vol. 8, Apr 19 2017.
[117] S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, and P. L. McEuen, "High performance electrolyte gated carbon nanotube transistors," (in English), *Nano Letters,* vol. 2, no. 8, pp. 869-872, Aug 2002.
[118] H. Tian *et al.*, "A dynamically reconfigurable ambipolar black phosphorus memory device," (in English), *ACS Nano,* vol. 10, no. 11, pp. 10428-10435, Nov 2016.
[119] H. L. Xu, S. Fathipour, E. W. Kinder, A. C. Seabaugh, and S. K. Fullerton-Shirey, "Reconfigurable ion gating of 2H-$MoTe_2$ field-effect transistors using poly(ethylene oxide)-$CsClO_4$ solid polymer electrolyte," (in English), *ACS Nano,* vol. 9, no. 5, pp. 4900-4910, May 2015.
[120] T. Chu, H. Ilatikhameneh, G. Klimeck, R. Rahman, and Z. H. Chen, "Electrically tunable bandgaps in bilayer MoS_2," (in English), *Nano Letters,* vol. 15, no. 12, pp. 8000-8007, Dec 2015.
[121] A. Seabaugh and R. Lake, "Tunnel diodes," *Encyclopedia of Applied Physics,* vol. 22, p. 335, 1998.
[122] J. S. Qiao, X. H. Kong, Z. X. Hu, F. Yang, and W. Ji, "High-mobility transport anisotropy and linear dichroism in few-layer black phosphorus," (in English), *Nature Communications,* vol. 5, pp. 1-7, Jul 2014, Art. no. 4475.

[123] Z. Luo *et al.*, "Anisotropic in-plane thermal conductivity observed in few-layer black phosphorus," (in English), *Nature Communications,* vol. 6, pp. 1-8, Oct 2015, Art. no. 8572.
[124] F. N. Xia, H. Wang, and Y. C. Jia, "Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics," (in English), *Nature Communications,* vol. 5, pp. 1-6, Jul 2014, Art. no. 4458.
[125] N. Haratipour and S. J. Koester, "Ambipolar black phosphorus MOSFETs with record n-channel transconductance," (in English), *IEEE Electron Device Letters,* vol. 37, no. 1, pp. 103-106, Jan 2016.
[126] G. Long *et al.*, "Achieving ultrahigh carrier mobility in two-dimensional hole gas of black phosphorus," (in English), *Nano Letters,* vol. 16, no. 12, pp. 7768-7773, Dec 2016.
[127] N. Haratipour, M. C. Robbins, and S. J. Koester, "black phosphorus p-MOSFETs With 7-nm HfO_2 gate dielectric and low contact resistance," (in English), *IEEE Electron Device Letters,* vol. 36, no. 4, pp. 411-413, Apr 2015.
[128] D. J. Perello, S. H. Chae, S. Song, and Y. H. Lee, "High-performance n-type black phosphorus transistors with type control via thickness and contact-metal engineering," (in English), *Nature Communications,* vol. 6, Jul 2015.
[129] L. Li, M. Engel, D. B. Farmer, S. J. Han, and H. S. P. Wong, "High-performance p-type black phosphorus transistor with scandium contact," (in English), *ACS Nano,* vol. 10, no. 4, pp. 4672-4677, Apr 2016.
[130] J. S. Miao, S. M. Zhang, L. Cai, M. Scherr, and C. Wang, "Ultrashort channel length black phosphorus field-effect transistors," (in English), *ACS Nano,* vol. 9, no. 9, pp. 9236-9243, Sep 2015.
[131] P. J. Jeon, Y. T. Lee, J. Y. Lim, J. S. Kim, D. K. Hwang, and S. Im, "Black phosphorus–zinc oxide nanomaterial heterojunction for p–n diode and junction field-effect transistor," *Nano Letters,* vol. 16, no. 2, pp. 1293-1298, Feb 10 2016.
[132] J. Xu, J. Y. Jia, S. Lai, J. Ju, and S. Lee, "Tunneling field effect transistor integrated with black phosphorus-MoS_2 junction and ion gel dielectric," (in English), *Applied Physics Letters,* vol. 110, no. 3, Jan 16 2017.
[133] Y. Li, S. X. Yang, and J. B. Li, "Modulation of the electronic properties of ultrathin black phosphorus by strain and electrical field," (in English), *Journal of Physical Chemistry C,* vol. 118, no. 41, pp. 23970-23976, Oct 16 2014.
[134] R. S. Yan *et al.*, "Esaki diodes in van der Waals heterojunctions with broken-gap energy band alignment," (in English), *Nano Letters,* vol. 15, no. 9, pp. 5791-5798, Sep 2015.
[135] L. K. Li *et al.*, "Quantum Hall effect in black phosphorus two-dimensional electron system," (in English), *Nature Nanotechnology,* vol. 11, no. 7, pp. 592-596, Jul 2016.
[136] Z. H. Jin, X. D. Li, J. T. Mullen, and K. W. Kim, "Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides," (in English), *Physical Review B,* vol. 90, no. 4, Jul 24 2014, Art. no. 045422
[137] H. J. Chuang *et al.*, "Low-resistance 2D/2D ohmic contacts: a universal approach to high-performance WSe_2, MoS_2, and $MoSe_2$ transistors," (in English), *Nano Letters,* vol. 16, no. 3, pp. 1896-1902, Mar 2016.
[138] V. Podzorov, M. E. Gershenson, C. Kloc, R. Zeis, and E. Bucher, "High-mobility field-effect transistors based on transition metal dichalcogenides," (in English), *Applied Physics Letters,* vol. 84, no. 17, pp. 3301-3303, Apr 26 2004.
[139] A. Prakash and J. Appenzeller, "Bandgap extraction and device analysis of ionic liquid gated WSe_2 Schottky barrier transistors," (in English), *ACS Nano,* vol. 11, no. 2, pp. 1626-1632, Feb 2017.

[140] P. Agnihotri, P. Dhakras, and J. U. Lee, "Bipolar junction transistors in two-dimensional WSe_2 with large current and photocurrent gains," (in English), *Nano Letters,* vol. 16, no. 7, pp. 4355-4360, Jul 2016.
[141] G. W. Burg *et al.*, "Coherent interlayer tunneling and negative differential resistance with high current density in double bilayer graphene–WSe_2 heterostructures," *Nano Letters,* vol. 17, no. 6, pp. 3919-3925, June 14 2017.
[142] J. J. Wang *et al.*, "Gate-modulated conductance of few-layer WSe_2 field-effect transistors in the subgap regime: Schottky barrier transistor and subgap impurity states," (in English), *Applied Physics Letters,* vol. 106, no. 15, Apr 13 2015.
[143] N. R. Pradhan *et al.*, "Hall and field-effect mobilities in few layered p-WSe_2 field-effect transistors," (in English), *Scientific Reports,* vol. 5, Mar 11 2015.
[144] S. Das, M. Dubey, and A. Roelofs, "High gain, low noise, fully complementary logic inverter based on bi-layer WSe_2 field effect transistors," (in English), *Applied Physics Letters,* vol. 105, no. 8, Aug 25 2014.
[145] H.-J. Chuang *et al.*, "High mobility WSe_2 p- and n-type field-effect transistors contacted by highly doped graphene for low-resistance contacts," *Nano Letters,* vol. 14, no. 6, pp. 3594-3601, June 11 2014.
[146] M. Tosun *et al.*, "High-gain inverters based on WSe_2 complementary field-effect transistors," *ACS Nano,* vol. 8, no. 5, pp. 4948-4953, May 27 2014.
[147] H. C. P. Movva *et al.*, "High-mobility holes in dual-gated WSe_2 field-effect transistors," *ACS Nano,* vol. 9, no. 10, pp. 10402-10410, Oct 27 2015.
[148] L. Yu *et al.*, "High-performance WSe_2 complementary metal oxide semiconductor technology and integrated circuits," *Nano Letters,* vol. 15, no. 8, pp. 4928-4934, Aug 12 2015.
[149] H. J. Kim, D. H. Kim, C. Y. Jeong, J. H. Lee, and H. I. Kwon, "Determination of interface and bulk trap densities in high-mobility p-type WSe_2 thin-film transistors," (in English), *IEEE Electron Device Letters,* vol. 38, no. 4, pp. 481-484, Apr 2017.
[150] G. V. Resta *et al.*, "Polarity control in WSe_2 double-gate transistors," (in English), *Scientific Reports,* vol. 6, Jul 8 2016.
[151] W. Liu, J. H. Kang, D. Sarkar, Y. Khatami, D. Jena, and K. Banerjee, "Role of metal contacts in designing high-performance monolayer n-Type WSe_2 field effect transistors," (in English), *Nano Letters,* vol. 13, no. 5, pp. 1983-1990, May 2013.
[152] S. G. Xu *et al.*, "Universal low-temperature ohmic contacts for quantum transport in transition metal dichalcogenides," (in English), *2D Materials,* vol. 3, no. 2, Jun 2016.
[153] J. D. Wood *et al.*, "Effective passivation of exfoliated black phosphorus transistors against ambient degradation," (in English), *Nano Letters,* vol. 14, no. 12, pp. 6964-6970, Dec 2014.
[154] L. Sang, "Ferroelectricity in nanocrystalline $Hf_{0.5}Zr_{0.5}O_2$ thin films," M.S. thesis*, Deoartment of Physics, LUND Univeristy,* 2018.
[155] M. H. Park *et al.*, "Ferroelectricity and Antiferroelectricity of Doped Thin HfO_2-Based Films," (in English), *Advanced Materials,* vol. 27, no. 11, pp. 1811-1831, Mar 18 2015.
[156] D. Zhao *et al.*, "Depolarization of multidomain ferroelectric materials," (in English), *Nature Communications,* vol. 10, Jun 11 2019.
[157] B. D. Liu, C. Y. Chen, and J. Y. Tsao, "A modular current-mode classifier circuit for template matching application," (in English), *IEEE Transactions on Circuits and Systems Ii-Analog and Digital Signal Processing,* vol. 47, no. 2, pp. 145-151, Feb 2000.
[158] B. Sedighi, X. S. Hu, J. J. Nahas, and M. Niemier, "Nontraditional computation using beyond-CMOS tunneling devices," (in English), *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* vol. 4, no. 4, pp. 438-449, Dec 2014.

[169] P. Zhao, R. M. Feenstra, G. Gu, and D. Jena, "SymFET: A proposed symmetric graphene tunneling field-effect transistor," (in English), *IEEE Transactions on Electron Devices,* vol. 60, no. 3, pp. 951-957, Mar 2013.
[160] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudoSpin field-effect transistor (BiSFET): A proposed new logic device," (in English), *IEEE Electron Device Letters,* vol. 30, no. 2, pp. 158-160, Feb 2009.
[161] Y. Q. Wu *et al.*, "State-of-the-art graphene high-frequency electronics," (in English), *Nano Letters,* vol. 12, no. 6, pp. 3062-3067, Jun 2012.
[162] L. Bin-Da, C. Chuen-Yau, and T. Ju-Ying, "A modular current-mode classifier circuit for template matching application," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 47, no. 2, pp. 145-151, 2000.
[163] R. G. Dreslinski *et al.*, "Centip3De: A 64-core, 3D stacked near-threshold system," *IEEE Micro,* vol. 33, no. 2, pp. 8-16, 2013.
[164] P. J. Jeon *et al.*, "Low power consumption complementary inverters with n-MoS_2 and p-WSe_2 dichalcogenide nanosheets on glass for logic and light-emitting diode circuits," (in English), *ACS Applied Materials & Interfaces,* vol. 7, no. 40, pp. 22333-22340, Oct 14 2015.
[165] M. Tosun *et al.*, "High-gain inverters based on WSe_2 complementary field-effect transistors," (in English), *ACS Nano,* vol. 8, no. 5, pp. 4948-4953, May 2014.
[166] L. L. Yu *et al.*, "High-performance WSe_2 complementary metal oxide semiconductor technology and integrated circuits," (in English), *Nano Letters,* vol. 15, no. 8, pp. 4928-4934, Aug 2015.
[167] Das, S., & Roelofs, A., "Electrostatically doped WSe_2 CMOS inverter," in *72nd Device Research Conference*, 2014, pp. 185-186.
[168] P. Dhakras, P. Agnihotri, and J. U. Lee, "Three fundamental devices in one: A reconfigurable multifunctional device in two-dimensional WSe_2," (in English), *Nanotechnology,* vol. 28, no. 26, Jun 30 2017.
[169] M. R. Muller *et al.*, "Gate-controlled WSe_2 transistors using a buried triple-gate structure," (in English), *Nanoscale Research Letters,* vol. 11, Nov 22 2016.
[170] C. S. Pang *et al.*, "WSe_2 homojunction devices: Electrostatically configurable as diodes, MOSFETs, and tunnel FETs for reconfigurable computing," (in English), *Small,* vol. 15, no. 41, Oct 2019.