Facile Route for Low-temperature Eco-friendly Solution Processed ZnSnO Thin-film Transistors

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***Abstract*—In this work, solution processed zinc tin oxide semiconductor films were investigated. Different from the widely reported high-temperature and toxic organic solvent-based fabrication process, a low temperature and eco-friendly aqueous solvent-based route was studied. The optimization of electrical performances on field effect mobility and reliability was proved. Moreover, a resistor-loaded inverter was constructed.**

***Index Terms*-- Semiconductor devices, Thin film transistors, Current-voltage characteristics, Threshold voltage, Inverters.**

I. INTRODUCTION

Recently, amorphous metal oxide (MO) semiconductors have attracted lots of attention in the research of thin-film transistors (TFT) as a result of their superior physical and device performance characteristics compared to traditional amorphous silicon and organic semiconductors [1]. Solution fabrication processes compared with conventional vacuum-based fabrication processes, offer lots of advantages, such as low cost, roll-to-roll capability, equipment convenience, and atmospheric processing [2]. Among the reported solution processed MO materials, indium (In), zinc (Zn) and tin (Sn) based oxidizing compounds have been shown to be a promising candidate for the n-type TFTs [3]. Since, the abundance of In in the earth is low (0.25 ppm), solution processed ZnSnO (ZTO) with excellent semiconductor characteristics are emerging as a replacement of In-based channel materials [3]. However, in previous reports related to solution processed ZTO TFTs, the high annealing temperature (>450 ℃) process as well as the toxic organic solvent such as 2-methoxyethanol (2-Me) are common drawbacks [4].

In this work, a low-temperature (300 ℃) process route to fabricate ZTO films with non-toxic eco-friendly aqueous solvent was studied. Compared with the 2-Me based control group, both physical and electrical characteristics were improved successfully. Gate bias tests were measured and analyzed in detail to investigate the reliability of these devices. The aqueous solvent based group is showed to have a more stable behavior. Resistor-loaded inverter circuits were built by connecting the ZTO TFT with an 8 MΩ resistor, indicating the potential for further circuits application research.

II. DEVICE AND STRESS PROCEDURE DESCRIPTION

The precursor solutions for the non-toxic eco-friendly ZTO solvent (A-ZTO) were prepared by dissolving 0.2 M tin chloride dihydrate ($SnCl_2 \cdot 2H_2O$, Aladdin) and 0.3 M zinc acetate dihydrate ($C_4H_6O_4Zn \cdot 2H_2O$, Aladdin) in deionized water (DI water). A control group (O-ZTO) was prepared using 2-Me as the solvent instead of the DI water. For TFT fabrication, the processes and structure of devices are displayed in Fig. 1. Both of the A-ZTO and the O-ZTO solution groups were stirred in atmosphere for 12 h and aged for 2 h before being filtered and spun coated on heavily doped n-type silicon substrate with 100 nm thermally grown silicon oxide (SiO_2). Films were then pre-annealed at 180 ℃ for 10 min and 300 ℃ for 2 h on a hotplate in air. An extra group of O-ZTO samples under 500 ℃ annealing process was also fabricated and acted as control group for physical characterization tests. Finally, aluminum (Al) source and drain electrodes were deposited onto the semiconductor layer through a shadow mask with a Width/Length of 150/10 μm. The threshold voltage (V_{th}) are extracted by the intersection point of $I_D^{1/2}$-V_G curve linear region extension line and x-axis. The mobility (μ_{sat}) of the devices was calculated by the following equations:

$$\mu_{sat} = \left(\frac{2L}{WC_i}\right)\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2 \qquad (1)$$

Where C_i is the capacitance per unit area of the SiO_2 dielectric layer in the transistor, the value of which is 26 nF/cm². W and L are the channel width and length, I_D is the drain current, and V_G is the gate voltage.

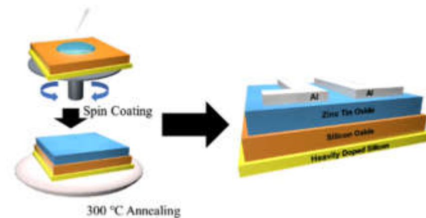

Figure 1. Schematic diagram fabrication flow of the low-temperature solution processed ZTO thin-film transistors

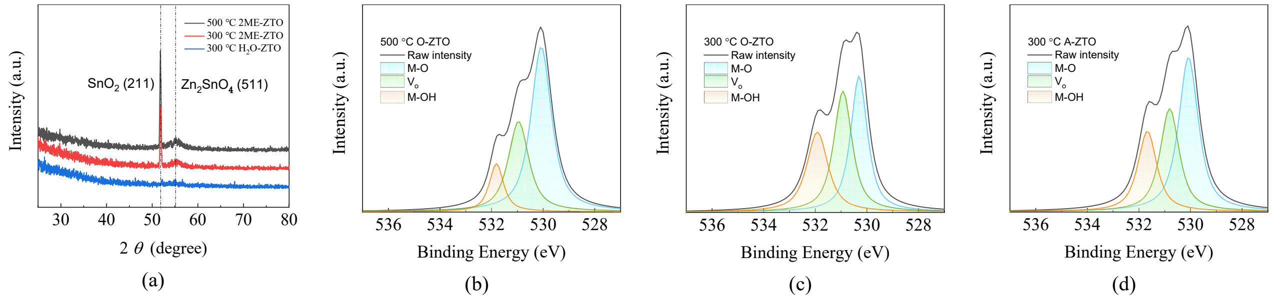

Figure 2. (a) XRD spectra of O-ZTO and A-ZTO thin film. XPS O 1s spectra of (b) 500 °C O-ZTO, (c) 300 °C O-ZTO and (d) 300 °C A-ZTO samples.

Table 1. Positions, areas, and area ratios of the O 1*s* peaks for ZTO films

	500°C 2-Me ZTO			300°C 2-Me ZTO			300°C H_2O ZTO		
Bind	Position(eV)	AREA(a.u.)	Ratio(%)	Position(eV)	AREA(a.u.)	Ratio(%)	Position(eV)	AREA(a.u.)	Ratio(%)
O_M	530.05	50060	57.23	530.28	28093	36.96	530.06	37661	50.34
O_V	530.93	27288	31.20	530.91	27109	35.66	530.79	23435	31.32
O_H	531.79	10126	11.58	531.90	20811	27.38	531.66	13723	18.34

III. Experimental Results and Discussion

A. Physical Characterization

The crystallization of ZTO under different fabricate conditions was investigated using x-ray diffraction (XRD) measurements on the 500 °C O-ZTO, 300 °C O-ZTO and 300°C A-ZTO samples. As shown in Fig. 2(a), the 500 °C O-ZTO and 300 °C O-ZTO samples display diffraction peaks due to the (211) and (511) crystallographic planes, which can be identified as crystalline tin dioxide (SnO_2) and zinc stannate (Zn_2SnO_4). For the 300°C A-ZTO samples an amorphous state is observed. It should be noted that the amorphous structure could lead to improved uniformity for TFT devices, beneficial for large-area mass production, since the grain boundaries may cause surface roughness [5-7].

Oxygen (O) bonds plays an important role in device performance. To investigate oxygen chemical bonding states and compositions of ZTO layers prepared through different methods, X-ray photoelectron spectra (XPS) were measured and is shown in Figs. 2(b) to (d). The O 1*s* XPS spectra can be divided into three sub-peaks through deconvolution. They are centered at approximately 530, 531, and 532 eV, which correspond to metal-oxygen bonds (O_M), O^{2-} ions near oxygen vacancies (O_V), and metal-hydroxyl bonds (O_H), respectively [8-10]. M-O bonds enable a stable conductive channel, while the V_o and M-OH bonds induce positive ions that act as donor-like traps under the application of gate bias [11]. As shown in Table 1 the area ratios of M-O peaks (centered at 529.8 eV) are 57.23 %, 36.96 % and 50.34 for 500 °C O-ZTO, 300 °C O-ZTO and 300 °C A-ZTO samples, respectively. Compared to the 300 °C O-ZTO samples, the group of 300°C A-ZTO samples exhibit larger area ratio of M-O peaks, which indicates a more complete conversion from solution to MO network. Although a little enhancement of M-O peak area ratio could be bound in the 500 °C O-ZTO samples, increasing the A-ZTO annealing temperature from 300 °C to 500 °C is not worth the small observed benefit.

Table 2. Electrical properties of solution processed ZTO TFTs

Solvent/temp.	Mobility ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	On/Off Ratio	Ref.
Ethanol/350℃	0.8	-	-	[12]
2-Me/500℃	0.5-3.7	1.75-7.05	10^5-10^6	[4]
2-Me/500℃	2.5	0.5	$2.4\cdot10^6$	[13]
2-Me/300℃	0.04	51.1	10^5	This work
DI water/300℃	2.00	17.6	10^6	

B. Electrical Characterization

Since this work is mainly focus on the low-temperature (<350 °C) annealed TFTs, TFT devices were fabricated among the 300 °C groups and tested. The results of typical transfer test for 300 °C O-ZTO and 300 °C A-ZTO devices are shown in Fig.3(a) and (b). All the devices exhibited a feature of enhanced mode n-channel transistor. Extracted from these results, the electrical performances of both groups and recent studies are summarized in Table 2. The performance of the devices in this work are superior or comparable to related reports [4, 12, 13]. Compared with the 300 °C O-ZTO TFTs, the aqueous solvent based A-ZTO TFTs shows a higher mobility of 2 $cm^2V^{-1}s^{-1}$ (50 times that of 300 °C O-ZTO TFTs) and a higher on/off current ratio of 10^6. This is mainly due to the less temperature requirement for the removal of solvent residues of DI water than 2-Me, which is also consistent with the XPS results mentioned above [2]. These kinds of residues may cause the defects in the films and block the charge transport. Therefore,

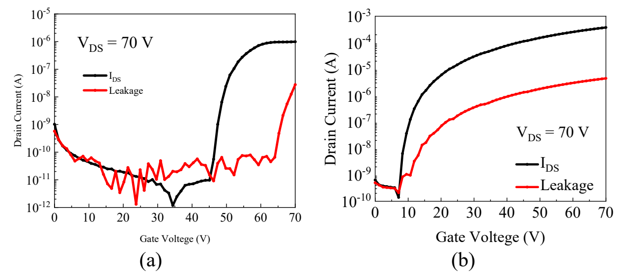

Figure 3. Transfer characteristics of (a) O-ZTO and (b) A-ZTO TFTs.

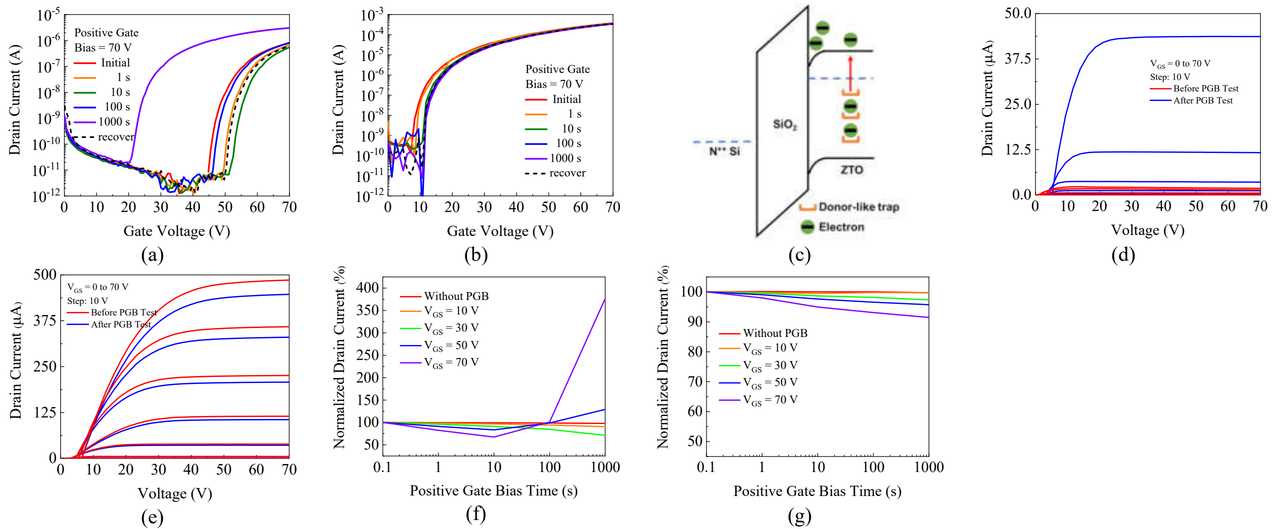

Figure 4. Transfer characteristics under 1000 s PGB test for the (a) O-ZTO (b) A-ZTO TFTs (a small distortion in the initial characterization data is present due device instabilities at the large voltages measured). (c) Schematic diagram of the threshold voltage reduction mechanism. Output characteristics before/after 1000 s PGB test of the (d) O-ZTO (e) A-ZTO TFTs. The normalized drain current of (f) O-ZTO (g) A-ZTO during the 1000 s PGB test

the channel layers of A-ZTO TFTs exhibited a higher carrier mobility as well as a higher operating current.

Moreover, to investigate the reliability of the devices, a 70 V positive gate bias (PGB) test was studied. The transfer curves' measurement may cause some recovery due to the interruption of the gate bias stress (about 1 ms). However, the overall trend of the V_{th} shifts can still indicate the difference of the two groups. As shown in Fig. 4(a), (b) and Table 3, after 1000 s measurement, compared with the O-TFT, the A-ZTO TFTs exhibited much less threshold voltage (V_{th}) shift (3.6 V). This indicates a much better PGB stress reliability of A-ZTO than O-ZTO. Different from the totally positive V_{th} shift of the A-ZTO TFTs, the O-ZTO TFTs showed a positive shift at first and then switched to an opposite direction. According to related reports, typically, MO TFTs show a positive V_{th} shift under the PGB condition due to the trapping of electrons at either the channel layer/dielectric interface or the backchannel [11, 14]. These trapping effects also degrade the transport of charge carriers leading to a decrease of the operating drain current, as displayed in Figs. 4(d) to (g). However, solvent residues and V_o may generate a large number of donor states, as shown in Fig. 4(c), that become positively charged when their electrons move to the conduction band during the PGB test [11, 14]. The

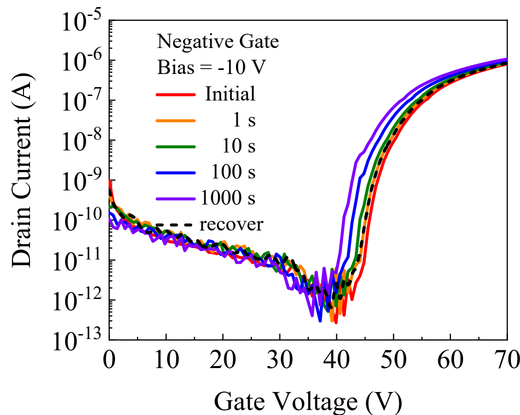

Figure 5. Transfer characteristics under 1000 s NGB test for the (a) O-ZTO (b) A-ZTO TFTs.

positively charged donor states lower the gate voltage (V_{th} shifts negatively) and increases the drain current at operating gate voltage, as displayed in Figs. 4(d) to (g) [11, 14, 15]. In addition, this negative V_{th} shift mechanism is largely recoverable due to gradual charge neutralization during the recovery process [14]. This helps explain the results that after 1000 s recover test, the negative V_{th} shift is mostly recovered while the positive V_{th} shift was not recovered as much as summarized in Table 3. Therefore, the much more unstable behavior of O-ZTO under the PGB test could be attributed to the larger amounts of solvent residues and the V_o, which is in great agreement with the XPS results above. Figs. 5(a) and (b) displays the -10 V negative gate bias (NGB) test performance of O-ZTO and A-ZTO. Under 1000 s measurement, the O-ZTO TFTs showed an unrecoverable negative V_{th} shift of -7.8 V while the A-ZTO TFTs showed a negligible V_{th} shift. This could be attributed to the more hole trapping at the channel/dielectric layer interface of the O-ZTO TFTs [14].

To further investigate the potential of the application of A-ZTO FETs in circuits, a resistor-loaded inverter was built by connecting the A-ZTO TFTs with an 8 MΩ resistor, as shown in Fig. 6(a). The logic performance and the gain of the inverters are displayed in Fig. 6(b) and (c). When the supply voltage (V_{DD}) was 10 V, the voltage gain is less than 1, and as the supply voltage (V_{DD}) increased to 60 V, the voltage gain increases to more than 4. It should be noted here that the voltage gain driving the logic circuit elements requires only 2.5, which proves that the TFTs in this study has a promising future for the circuits research[16].

IV. CONCLUSIONS

In this work, a low-temperature route of solution processed ZTO TFT was reported. Compared with widely reported toxic 2-Me solvent based groups, the eco-friendly aqueous based devices optimized significantly on the performance of mobility and reliability. Moreover, the as-mentioned ZTO TFTs were proved to be applied for a resistor-loaded inverter circuits with a gain of more than 4.

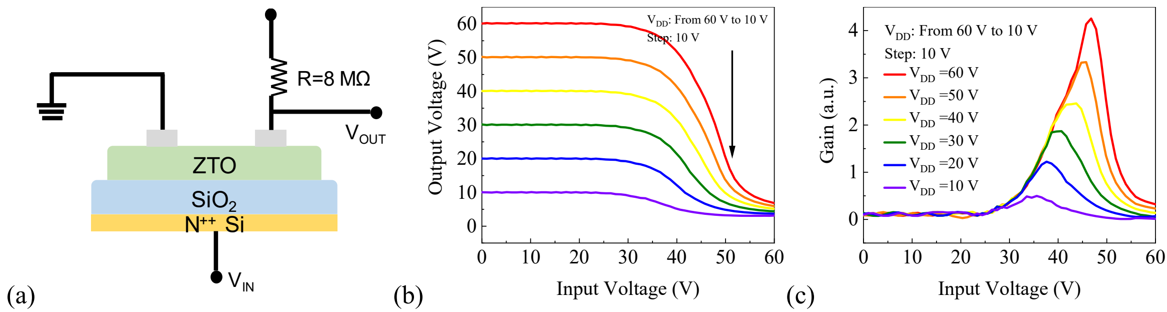

Figure 6. (a) Resistor-loaded inverter structure with A-ZTO TFTs. (b) Static logic test curves of the inverter with A-ZTO TFTs. (c) Voltage gain of the inverter at various V_{DD} values.

Table 3. V_{th} shifts under gate bias stress test of ZTO TFTs

	Device	1 s	10 s	100 s	1000 s	1000 s recovery
PGB	O-ZTO TFT	+ 4.9 V	+7.7 V	+2.1 V	-21.2 V	+8.7 V
	A-ZTO TFT	+ 0.4 V	+1.2 V	+2.2 V	+3.6 V	+3.4 V
NGB	O-ZTO TFT	-1.2 V	-2.5 V	-4.6 V	-7.8 V	-7.6 V
	A-ZTO TFT	Negligible				

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