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Electron Charge Transport in Non-Peripherally Substituted Copper Phthalocyanine

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Bottom-gate, bottom-contact organic thin film transistors (OTFTs) were fabricated using solvent soluble copper-1,4,8,11,15,18,22,25-octakis(hexyl)phthalocyanine as the active semiconductor layer. The compound was deposited as 70 nm thick spin-coated films onto gold source-drain electrodes supported on octadecyltrichlorosilane treated 250 nm thick SiO$_2$ gate insulator. The analysis of experimental results showed the n-type field effect behaviour. Devices annealed at 100 $^{\rm o}$C under vacuum were found to exhibit the field-effect mobility of 0.0989 cm^2 V^{-1} s^{-1}, with an on/off current modulation ratio of ∼10^6, a reduced threshold voltage of 0.7 V and a sub-threshold swing of 2.12 V decade^{-1}. The variations in surface morphology of the devices are found reflected considerably in the electrical measurements. The device contact resistance was found to be decreased as the gate bias increased and also with the annealing.

In recent years, organic field-effect transistors (OFETs) have been extensively used in designing complementary integrated circuits for flexible smart cards, low-cost radio frequency identification (RFID) tags, and organic active matrix displays and sensors.[1] Fullerene derivatives are found to be good materials for the formation of n-type conducting channels.[2] For example, a value of 0.34 cm^2 V^{-1} s^{-1} for electron mobility is reported for the Faux-hawk fullerenes (C$_{60}$FHF) channel.[3] Alternatively perylene diimides (PDIs) and naphthalene diimides (NDIs) are the most promising electron deficient building blocks for obtaining high performance electron transport materials with high mobilities of 6.2 cm^2 V^{-1} s^{-1} due to their relatively high electron affinities, and excellent chemical and thermal stability.[4]

Solution processable organic and polymeric semiconducting materials are attractive to realize low-cost, high-volume, large-area electronic circuits on flexible substrates. Several solution based processes, such as spin-coating, drop-casting, and inkjet printing can be used to form semiconducting thin films. Bottom-gate, top-contact OTFTs with NDI active layers were fabricated based on OTS-modified SiO$_2$ substrates and extremely high electron mobility up to 7.5 cm^2 V^{-1} s^{-1} was achieved.[5] Representative examples of PDI derivatives with thin film mobilities over 1.0 cm^2 V^{-1} s^{-1} are compounds with C$_8$H$_{17}$ and C$_{13}$H$_{27}$ alkyl chains substituted at the N-positions, respectively. The mobility of solution-processed perchlorinateddiperylenebisimide(C12-4CldiPBI) is found to be larger than 1.0 cm^2 V^{-1} s^{-1} with the largest value of 4.65 cm^2 V^{-1} s^{-1}.[6] Bottom-gate, top-contact OTFTs were fabricated with a NDI on OTS-modified SiO$_2$ substrates, and extremely high electron mobility up to 7.5 cm^{-2} V^{-1} s^{-1} was achieved when the devices were tested after 30 min equilibration in an argon atmosphere at low humidity.[7] Small molecules based on azulene derivatives, dicyanomethylene-terminated quinoidal oligothiophenes, and isoindigo derivatives (3E,7E)−3,7-bis(2-oxoindolin-3-ylidene)benzo[1,2-b:4,5-b′]difuran-2,6(3 H,7 H)-dione have been investigated for their uses as n-type active layers in OFETs, producing mobility in the order of 0.1 cm^2 V^{-1} s^{-1}.[8] When[6,6]-phenyl C61 butyric acid methyl ester is doped with (4-(1,3dimethyl-2,3-dihydro-1H-benzoimidazol-2-yl)phenyl)dimethylamine, the electron mobility is found to increase from 1.68 × 10^{-2} cm^2 V^{-1} s^{-1} to 0.124 cm^2 V^{-1} s^{-1} for undoped

and doped layers, respectively.[8] A high value of 3 cm^2 V^{-1} s^{-1} has recently been reported for electron mobility for phenylalkyl-substituted-benzo[de]isoquinolino[1,8-gh] quinolinetetracarboxylic diimide.[9]

Phthalocyanines, highly conjugated 18 π-electron planar aromatic systems with a central cavity of sufficient size capable of coordinating different metal ions, are thermally and chemically stable and show excellent semiconducting properties for their applications including the fabrication of OTFTs.[10] Thermally deposited fluorinated copper phthalocyanines (F$_8$CuPc) show n-channel OTFT characteristics under vacuum with the electron mobility of 7.9 × 10^{-4} cm^2 V^{-1} s^{-1} in vacuum of 10^2 Pa.[11] A value of 0.54 cm^2 V^{-1} s^{-1} is obtained for electron mobility of thermally deposited bis(pentafluorophenoxy) silicon phthalocyanine(F-10-SiPc) at 140 $^\circ$C.[12] Electron mobilities of OTFTs with a n-type polycrystalline channel of tin phthalocyanines (SnPcs) with tributylsilane and trihexylsilane axial functional groups is found to be higher than their silicon counterparts due to increased molecular interactions.[13] The introduction of substituents onto the phthalocyanine nucleus can confer new and useful properties upon the ring system.[14]

The present paper reports an investigation of n-type field-effect transistor characteristics of non-peripherally octakis(hexyl) substituted copper phthalocyanine (6CuPc) derivative in the bottom gate transistor configurations as shown in Fig. 1. As reported before, the solubility of these molecule in common organic solvents enabled it to be deposited readily as well-ordered films by the spin coating method, a methodology ideal for simple device fabrication at room temperature.[15] Hole transport in spin coated 6CuPc has been investigated in OTFTs of similar configurations, giving p-type characteristics in the accumulation mode. These molecules are liquid crystalline and the transistor parameters are reported to be dependent upon the annealing temperature. Devices heat treated at 100°C under vacuum (⩾10^{-7}mbar) were found to exhibit the highest field-effect mobility of 0.7 cm^2 V^{-1} s^{-1}, with an on-off current modulation ratio of 10^7, threshold voltage of 2.0 V and a sub-threshold swing of 1.11 V per decade.[16]

Experimental

The drift mobility $\mu_{\rm de}$ was determined from the time of flight (TOF) measurement for the electron transport in a 9.1 μm thick film
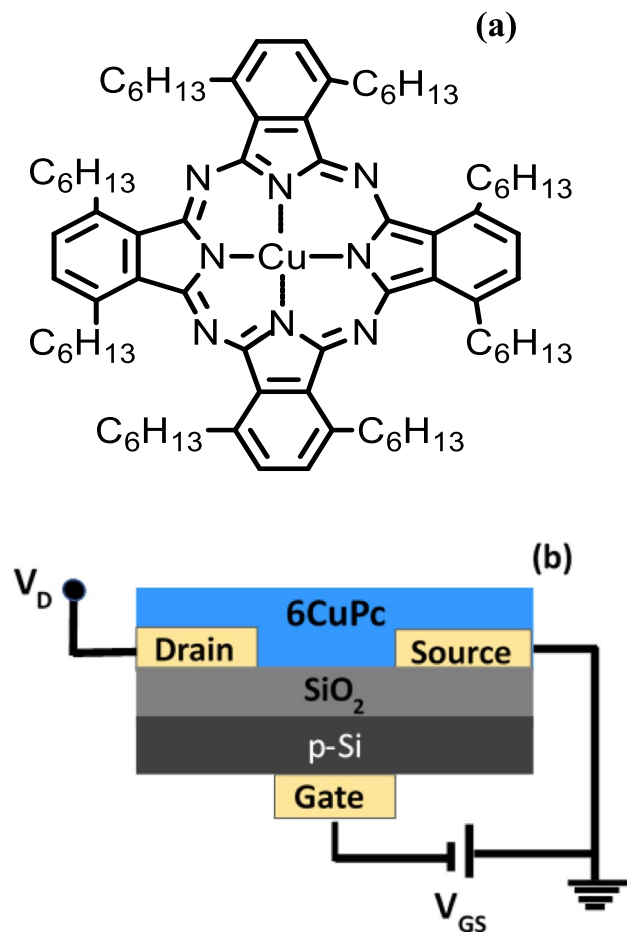
Figure 1. (a) Chemical structure of non-peripherally substituted 1,4,8,11,15,18,22,25-octakis(hexyl) copper phthalocyanine (6CuPc) and (b) bottom gate bottom contact organic field effect structure with channel length L and channel width W of 10 μm and 2 mm respectively. The thickness of active 6CuPc film layer is ~70 nm.

of 6CuPc sandwiched between two transparent indium tin oxide (ITO) coated glass substrates. The cell was formed by slow cooling of the organic layer at a rate of 2 °C min^{-1} to room temperature from the isotropic melt and a film of anti-parallel polyimide was used as the alignment layer. The photocurrents were produced using a 532 nm pulsed output of a double-frequency Nd:YAG laser to excite the sample. The bias between the ITO electrodes was provided by a DC power supply while the transient photocurrent was recorded by a voltage drop across the input resistor of a gain 11 amplifier circuit whose output was connected to an Agilent Infinium digitizing oscilloscope. Signal averaging was carried out on all signals in order to improve data quality.[17]

As shown in Fig. 1b, measurements of the n-type transistor characteristics have been performed under identical conditions on bottom gated organic field effect transistors using both as-prepared and annealed 70 nm (± 2 nm) thick spin-coated active layer 6CuPc films on the pre-patterned source and drain electrodes and 250 nm thick octaoctadecyltrichlorosilane (OTS) passivated SiO$_2$ gate dielectric layer on the highly doped silicon (110) gate electrode substrates. Two stage spin coater, Chemat Technology Inc., Model KW-4A was employed to prepare the uniform 6CuPc thin films initially at 1000 rpm for 30 s and subsequently 3000 rpm for 60 s. The devices were heated to 100 °C in a tubular furnace under vacuum of ~2 × 10^{-7} Torr and then gradually cooled down to room temperature at the rate of 1 °C min^{-1}. The electrical measurements were performed at room temperature in air under ambient conditions using a Keithley 4200 semiconductor parameter analyzer with three

source measure units (SMUs), which allows to measure the source, drain and gate currents simultaneously. All measurements were performed at a typical scan rate 50 m V s^{-1}. A custom-made probe station was used to obtain the source, drain and gate contacts. Prior to electrical measurement the devices were blew with N$_2$ gas and all equipments commonly grounded to probe station.[18] The surface morphology of the sample was investigated by the Digital Nanoscope III, Atomic Force Microscope (AFM) in non-conducting mode at ambient conditions using V-shaped silicon nitride cantilevers with force constant 2 N/m and resonance frequency 315 kHz.

Results and Discussion

The AFM micrographs o as-prepared and annealed 6CuPc spin coated film on Silicon substrate is shown in Figs. 2a and 2b, respectively. Both films illustrate significantly void free, densely packed compact good film adhesion to the 15 mm × 15 mm area of silicon substrate. Long grain like flat lying crystals of size ~0.1 μm can be seen in as-prepared sample. Randomly oriented short nanorods ~0.3 to 0.4 μm were observed upon annealing the devices at 100 °C in vacuum. The rod like morphology reduces apparent grain boundaries and may behave like a compound in the bulk material. Further, the rod like morphology is assumed to be supportive for charge transportation within the active semiconductor, which of course helps to improve the mobility of device. Root mean square values of 9 nm and 17 nm were measured for surface roughness of as-prepared and annealed 6CuPc films, respectively. The number of grain boundaries influences the electrical properties of devices. Rosenwaks and co-worker showed for the accumulation of charge carriers at the grain boundaries for pentacene films using Kelvin probe measurements leads to lower mobility of FETs.[19] Klauk and co-worker have reported that the grain boundaries are major source of degradation of charge carries mobility in C$_3$F$_7$CH$_2$−PTCDI-(CN)$_2$ based p-channel devices.[20] Larger grain size obtained for pentacene on poly-4-vinylphenol than polymethyl methacrylate gate dielectric measured higher mobility.[21]

The transit times t_0 of the photo-generated carriers traversing the 6CuPc layer at an applied bias, were determined by the inflection point on a double logarithmic plot. The resulting mobilities μ were then calculated using the relation,

$$\mu_{de} = \frac{d^2}{Vt_0}$$ [1]

where d is the cell thickness and V is the applied bias. Electron transport was measured in the sample at 0.40 μs and 0.26 μs for −6 V and −10V, respectively (Fig. 3a). Further analysis of the sample at higher fields for both electron transport, could not be carried out at room temperature as the inflexion point became engulfed in the initial peak of the photocurrent. The mobilities were calculated using Eq. 1 and plotted against the square root of the electric field (Fig. 3b). Electron mobility is found to be 0.4 cm^2 V^{-1} s^{-1}. This value is three orders of magnitude higher than one obtained for similar configured 2 μm thick 6ZnPc drop-cast films.[22] This relatively high mobility is attributed to the larger, well defined 6CuPc crystallites formed during slow cooling of the sample. For both bias voltages, the photo-current is found to have progressively decreased over time. However, the decrease is steeper for V$_a$ = 10 V than V$_a$ = 23 V, indicating the dominance of dispersive transport. The time of flight method gives a "long-range" mobility measured over relatively large distances (usually tens of microns) and on a milli-second or micro-second timescale. This dispersive behaviour is consistent for the multi-domain film structure, consisting of a large number of boundaries between domains with typically 300 nm to 400 nm cross-section as recorded under a polarizing microscope.

A typical set of output characteristics of drain-to-source current I$_{DS}$ vs drain-to-source voltage V$_{DS}$ for different values of the gate voltage V$_G$ of as-prepared and annealed devices are shown in Figs. 4a and 4b, respectively. The variations in surface morphology
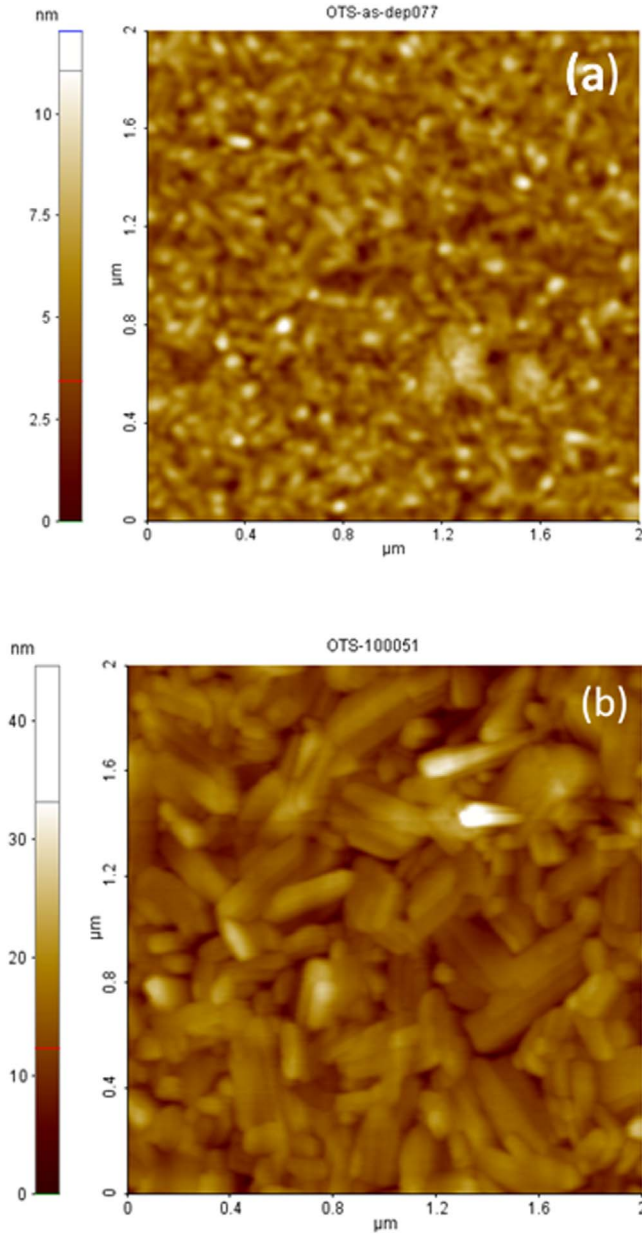
Figure 2. AFM images of OTS treated 6CuPc films on SiO$_2$ (a) as-prepared and (b) annealed at 100 °C.

Figure 3. (a) Electron photocurrent transients in a 9.1 μm thick cell of 6CuPc at -6 V and -10 V, scaling linearly with field, (b) electron mobility in 6CuPc calculated, parametric in electric field.

of the devices are found reflected considerably in the electrical measurements. Both devices demonstrated a typical n-type behaviour operating in accumulation mode with the increase in the drain current I$_{DS}$ with V$_G$.[23] A significant improvement in the performance of thermally annealed device at 100 °C is observed due to the coalescence of small grains having low surface energy leading to improve crystallinity and less grain boundaries. A clear transition from linear to saturation region was observed for annealed device due to pinch-off of the accumulation of charges. It was further observed that the I$_{DS}$ in annealed device saturated at lower I$_{DS}$ as compared to the corresponding value of as-prepared device. The annealing temperature was chosen based on the differential scanning calorimetry studies discussed in our earlier publication.[16]

The transfer characteristics, drain-to-source current, I$_{DS}$ and square root of drain current, (I$_{DS}$)$^{1/2}$ as a function of gate voltages, (V$_G$) with constant drain voltages in linear regime, V$_D$ = 5 V and saturated regime, V$_D$ = 40 V for as-prepared and annealed devices are shown in Figs. 5a and 5b, respectively. The performance
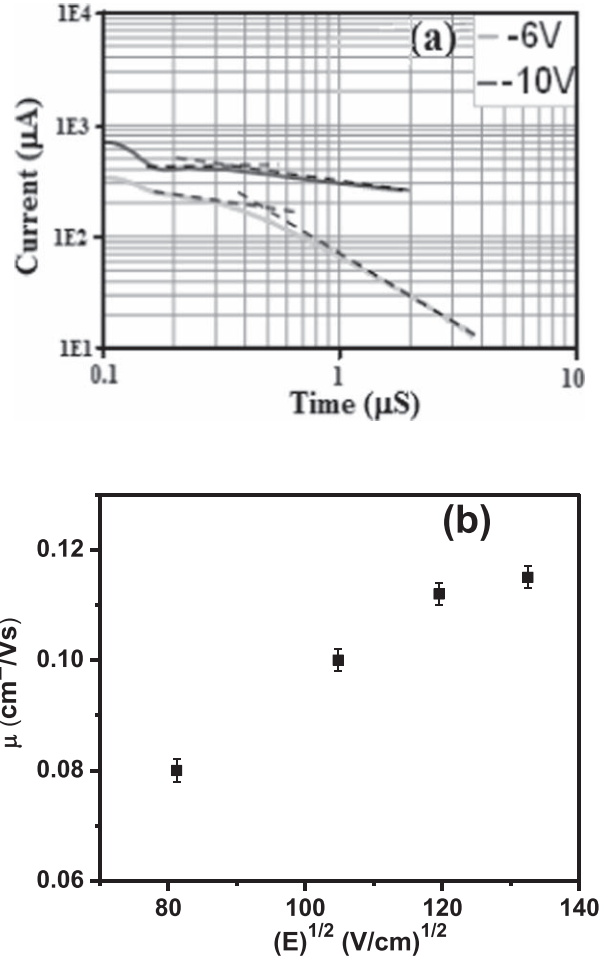
parameters of 6CuPc FET were extracted from the saturated and linear regimes by using the Eqs. 2 and 3.

$$I_{DS(sat)} = \frac{WC_i}{2L}\mu_{sat}(V_G - V_T)^2 \qquad [2]$$

$$\mu_{lin} = \left(\frac{L}{WC_iV_{DS}}\right)\frac{\partial I_{DS}}{\partial V_G} \qquad [3]$$

where L, W and C$_i$ are the channel length (10 μm), channel width (2 mm) and capacitance/unit area taken to be 1 $\times$ 10^{-4} F m^{-2} for the OTS treated SiO$_2$ gate dielectrics.[24] μ_{sat} and μ_{lin} are saturated and linear field effect mobility, V$_T$ is the threshold voltage of the device in both linear and saturated regime were determined from the graph of $\sqrt{I_{DS}}$ vs V$_G$ by extrapolating the straight line to I$_{DS}$ = 0. The values of linear and saturated field effect mobility, μ_{lin} and μ_{sat} were extracted from the trans-conductance plot shown in Figs. 5a and 5b. The values of mobilities of as-prepared and annealed devices are given in Table I. The value of μ_{lin} was comparatively lower than that of μ_{sat}. However, the value of μ_{lin} is found to be increased by one order of magnitude from 3.69 $\times$ 10^{-3} cm^{2}V^{-1} s^{-1} for OFFT with as-prepared channel to 4.87 $\times$ 10^{-2} cm^{2}V^{-1} s^{-1} for annealed OFETs. Values of μ_{sat} at V$_G$ = 40 V are found to be 3.67 $\times$ 10^{-2} cm^2 V^{-1} s^{-1} and 9.89 $\times$ 10^{-2} cm^2 V^{-1} s^{-1} for as-prepared and annealed 6CuPc OTFTs, respectively. The value of μ_{sat} measured for annealed device is more than doubled as compared to the as-
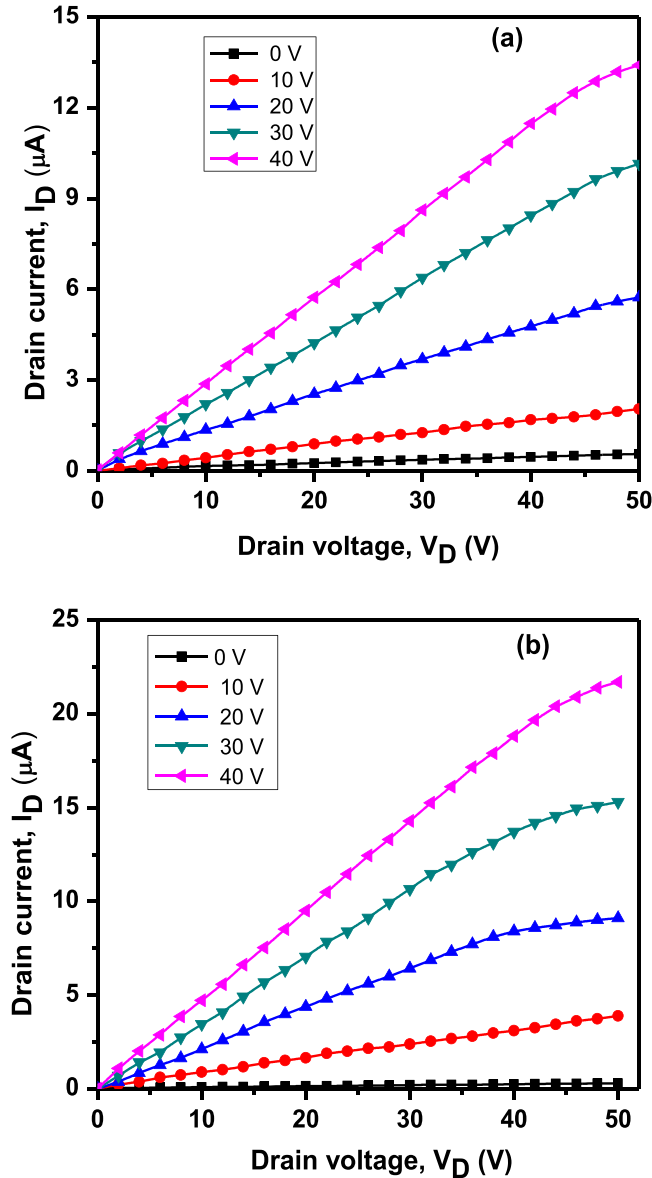
Figure 4. Output characteristics for an OTFT with the 6CuPc films in terms of the variation of the drain current I_D as a function of the drain voltage V_D, (a) as-deposited and (b) annealed for the gate voltage $V_G = 0$ V, 10 V, 20 V, 30 V and 40 V.

prepared device. These experimental results show the decrease of the resistance of the conducting channel with large grain boundaries leading to a performance improvement of the OTFTs.[25] The transistor characteristics of an n-type OTFT using physical vapour deposited N hexdecafluoro copper phthalocyanine (16-CuPc) films as active layer have recently reported. Values of saturation mobility μ_{sat} threshold voltage V_T and on-off ratio are found to be 2×10^{-2} cm^2 V^{-1} s^{-1}, -16 V and 3×10^3, respectively. In this context, 6CuPc OTFTs have produced the characteristics of improved performance.[26] Kraus et al., and de Boer et al., showed the ambiploar behaviour of CuPc OFETs prepared by thermal evaporation technique with electron mobility to 5.8×10^{-3} and 10^{-5}–10^{-3} cm^2 V^{-1} s^{-1},[27,28] which is considerably less than the electron mobility, 9.89×10^{-2} cm^2 V^{-1} s^{-1} measured for our devices.

The transfer characteristics exhibited good sub-threshold slopes. The sub-threshold voltage, S gives the information about the gate voltage required to increase the drain-to-source current by a factor of 10. The values of sub-threshold voltages, 3.65 V decade^{-1} and 2.12 V decade^{-1} were estimated using the following equation for as-
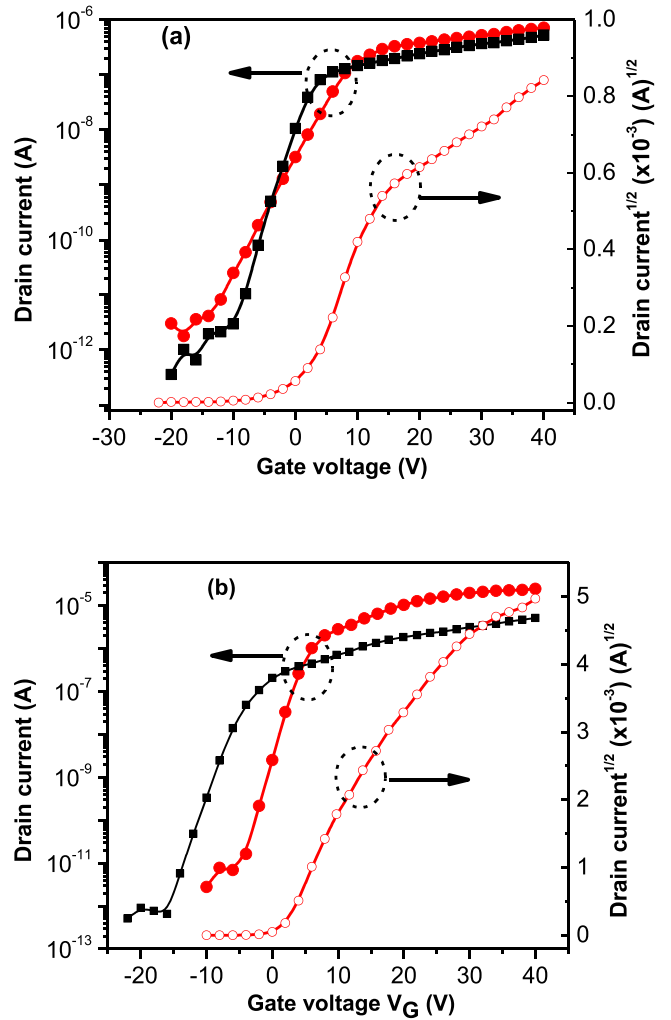

Figure 5. Transfer characteristics for 6CuPc (a) $V_D = 5$ V and (b) $V_D = 40$ V for as-deposited and annealed devices.

prepared and annealed 6CuPc transistors within saturated regimes, respectively.

$$S = \frac{dV_G}{d(\log_{10} I_{DS})} \qquad [4]$$

The performance parameters of the transistor also depend on the grain size, grain boundaries and the interface between the gate dielectric (SiO$_2$) layer and active semiconductor (6CuPc) thin film. The density of trapped charges (trap charge density (N_t)) can be determined by using the following relation related to sub-threshold voltages:

$$N_t = \left[\frac{S \log(e)}{\left(\frac{kT}{q} \right)} - 1 \right] \frac{C_i}{q} \qquad [5]$$

where k, T, q and S are the Boltzmann constant, the operating temperature, the electronic charge and the sub-threshold voltage swing, respectively. The values of density of trap, N_t were calculated to be 1.99×10^{12} cm^{-2} eV^{-1} and 2.23×10^{11} cm^{-2} eV^{-1} for as-prepared and annealed devices in the saturated regime. The decrease in value of N_t upon annealing is believed to be due to reduction in grain boundaries.[29]

Table I. A summary of transistor parameters measured for as-prepared and annealed 6CuPc devices.

6CuPctransistors	Mobility (cm^2 Vs^{-1})		On/off ratio	Threshold voltage, V_T (V)	Sub-threshold voltage, S (V/decade)	Interface trap density, N_t (cm^{-2} eV^{-1})	Grain-boundary trap density (cm^{-3})
	μ_{sat}	μ_{lin}					
As-prepared	0.0367	0.00369	10^5	1.0	3.65	1.99×10^{12}	6.56×10^{12}
Annealed	0.0989	0.0487	10^6	0.7	2.12	2.23×10^{11}	1.72×10^{12}

The relation between I_{DS} and the charges trapped at the grain boundaries of the material is described by Levinson model.[30] The Levinson plots of $\ln(I_D/V_G)$ vs $1/V_G$ at $V_D = 40$ V for as-prepared and annealed 6CuPc devices are shown in Fig. 6. The linear behaviour of the graph demonstrates the dependence of I_{DS} on the density of traps at the grain boundaries, N_g.

$$I_{DS} = \mu_0 V_{DS} \frac{W}{L} C_i V_G \exp\left(-\frac{q^3 N_g^2 t}{8\varepsilon_0 \varepsilon_{Pc} kTC_i V_G}\right) \quad [6]$$

The values of N_g and trap-free mobility, μ_0 can be extracted from the slope and intercept to x-axis at $1/V_G = 0$, respectively. The values of free space permittivity, $\varepsilon_o = 8.85 \times 10^{-12}$ F m^{-1}, electronic charge, $q = 1.6 \times 10^{-19}$ C, Boltzmann constant, $k = 8.62 \times 10^{-5}$ eV K^{-1}, temperature, T = 300 K and dielectric constant, $\varepsilon_{pc} = 3$ of 6CuPc were used to determine values of N_g. The values of 6.56×10^{12} cm^{-3} and 8.72×10^{11} cm^{-3} were estimated for N_g, from the slopes of best linear fits of Levinson plots. As shown in Fig. 7, the value of N_g obtained for annealed device is smaller than that of as-deposited film by nearly a one order of magnitude. This observation is associated with the less dense presence of grain boundaries upon thermal annealing. The values of trap-free mobilities, 0.882×10^{-2} and 2.26×10^{-2} cm^2 V^{-1} s^{-1} at $V_D = 40$ V were calculated for as-prepared and annealed 6CuPc devices. The grain boundary barrier $E_B = \frac{q^3 N_g^2 t}{8\varepsilon_0 \varepsilon_{Pc} C_i V_G}$ decreases while the grain boundary mobility μ_{GB} increases with V_G. E_B is found to undergo sharp decreases at low voltages and then the reduction tends to be steady. The density N_g is believed to contribute to the parasitic resistance of the device.

The contact resistance R_C can be expressed at each gate voltage in the following form[31]:

$$R_{total}\left(\frac{W}{L}\right) = \frac{1}{\mu_{lin} C_i (V_G - V_T)} + R_C\left(\frac{W}{L}\right) \quad [7]$$

The linear regions of the output curve can be used to determine the values of total resistance (R_{total}) for different gate voltages. The linear mobilities, 0.00369 and 0.0487 cm^2 V^{-1} s^{-1} computed with $V_D = 5$ V for as-prepared and annealed transistors, respectively along with corresponding V_G and V_T were used. The contact resistances as a function of gate biases shown in Fig. 8 revealed that the contact resistance decreases with increasing the gate bias. The decrease in contact resistance at higher gate biases could be due to the higher charge density in the conducting channel and in the vicinity of contacts. These results are consistent with the observations reported by Zhang et al.[32] Upon annealing the contact resistances obtained for each gate bias decreases substantially due to the coalescence of small grains, results the improvement in degree of crystallinity and less grain boundaries.

Concluding Remarks

6CuPc molecules are liquid crystalline and remain well aligned in the spin coated film with their columnar axis parallel to the substrate. This technique of thin film deposition may easily be adopted for the deposition over a large area for flexible electronics. The disordered film structure is evident from AFM images, following the annealing temperature dependent growth of crystallites in different shapes, sizes and orientations. The variations in surface morphology of the devices are found reflected considerably in the electrical measurements. The drain-source current is believed to be one dimensional electron transport via the overlap of π-π molecular orbitals through the accumulation layer. This investigation is interesting for the development of organic complementary metal oxide semiconductor (CMOS) circuits and organic light-emitting transistors.
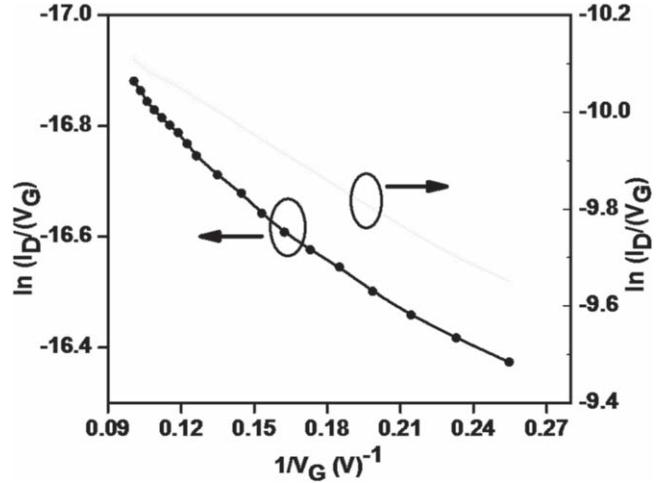

Figure 6. Levinson plots for as-prepared (open circles) and annealed (closed circles) of 6CuPc devices for $V_D = 40$ V.
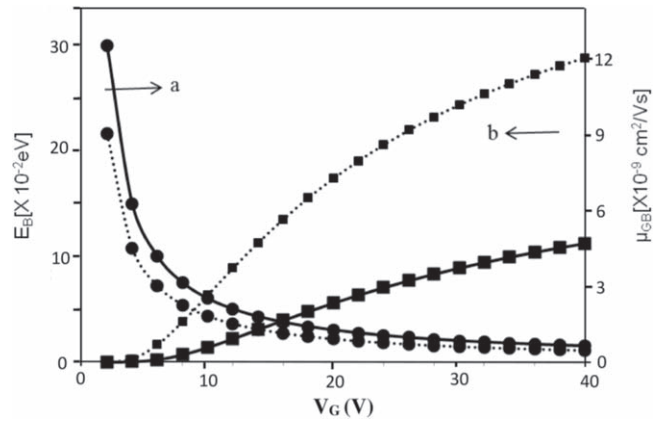

Figure 7. Dependence of (a) interfacial barrier E_B (curves with closed circles) and (b) the grain boundary mobility μ_{GB} (curve with solid rectangles) on gate voltage V_G for deposited (solid lines) and (broken lines) annealed 6CuPc films.
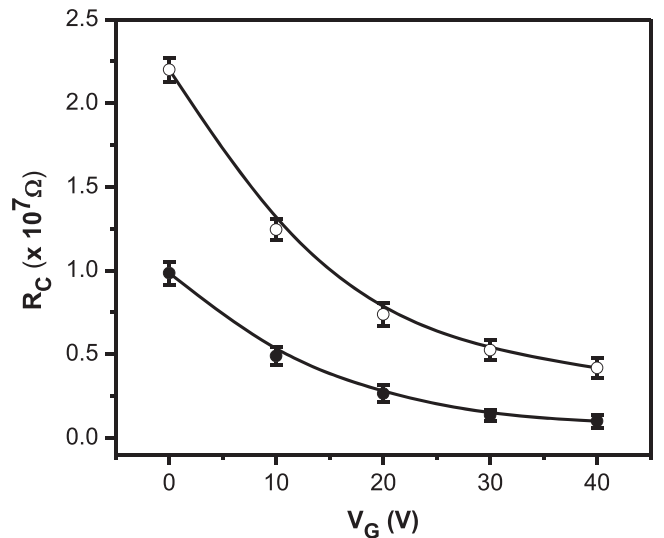

Figure 8. Dependence of the contact resistance R_C on the gate voltage V_G for as-deposited (open circles) and annealed (closed circles) 6CuPc films.

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References

1. B. Kumar, B. K. Kaushik, and Y. S. Negi, "Thin film transistors: structures, models, materials, fabrication, and applications: a review." *Polym. Rev.*, **54**, 33 (2014).
2. P. H. Wobkenberg, D. D. C. Bradley, D. Kronholm, J. C. Hummelen, D. M. de Leeuw, M. Colle, and T. D. Anthopoulos, "High mobility n-channel organic field-effect transistors based on soluble C-60 and C-70 fullerene derivatives." *Synth. Met.*, **158**, 468 (2008).
3. S. Y. Liu, N. J. DeWeerd, B. J. Reeves, L. K. San, D. Dahal, R. K. R. Krishnan, H. Strauss, O. V. Boltalina, and B. Lussem, "Doped N-type organic field-effect transistors based on faux-hawk fullerene." *Adv. Electron. Mater.*, **5**, 1900109 (2019).
4. A. Nowak-Krol, K. Shoyama, M. Stolte, and F. Wurthner, "Naphthalene and perylenediimides—better alternatives to fullerenes for organic electronics?" *Chem. Commun.*, **54**, 13763 (2018).
5. S. Kola, J. Sinha, and H. E. Katz, *J. Polym. Sci. Pt. B-Polym. Phys.*, **50**, 1090 (2012).
6. A. F. Lv et al., "High mobility, air stable, organic single crystal transistors of an n-type diperylenebisimide." *Adv. Mater.*, **24**, 2626 (2012).
7. K. Zhou, H. L. Dong, H. L. Zhang, and W. P. Hu, "High performance n-type and ambipolarsmallorganicsemiconductors for organicthin film transistors." *Phys. Chem. Chem. Phys*, **16**, 22448 (2014).
8. J. T. E. Quinn, J. X. Zhu, X. Li, J. L. Wang, and Y. N. Li, *J. Mater. Chem. C*, **5**, 8654 (2017).
9. T. Okamoto et al., *Sci. Adv.*, **6**, eaaz0632 (2020).
10. C. G. Claessens, U. Hahn, and T. Torres, "Phthalocyanines: from outstanding electronic properties to emerging applications." *Chem. Rec.*, **8**, 75 (2008).
11. A. Matumoto, N. Hoshino, T. Akutagawa, and M. Matsuda, "N-Type semiconducting behavior of copper octafluorophthalocyanine in an organic field-effect transistor." *Appl. Sci.-Basel*, **7**, 1111 (2017).
12. O. A. Melville, T. M. Grant, B. Mirka, N. T. Boileau, J. Park, and B. Lessard, "Ambipolarity and air stability of silicon phthalocyanine organic thin-film transistors." *Adv. Electron. Mater.*, **5**, 1900087 (2019).
13. T. M. Grant, N. A. Rice, L. Muccioli, F. Castet, and B. Lessard, "Solution-processable n-type tin phthalocyanines in organic thin film transistors and as ternary additives in organic photovoltaics." *ACS Appl. Electron. Mater.*, **1**, 494 (2019).
14. T. A. Turkmen et al., *Inorg. Chem.*, **57**, 6456 (2018).
15. S. Y. Wang, X. L. Zhao, Y. H. Tong, Q. X. Tang, and Y. C. Liu, *Adv. Mater. Interfaces*, **7**, 1901950 (2020).
16. N. B. Chaure, C. Pal, S. Barard, T. Kreouzis, A. K. Ray, A. N. Cammidge, I. Chambrier, M. J. Cook, C. E. Murphy, and M. G. Cain, *J. Mater. Chem.*, **22**, 19179 (2012).
17. S. Barard, T. Kreouzis, A. N. Cammidge, M. J. Cook, and A. K. Ray, *Semicond. Sci. Technol.*, **33**, 095010 (2018).
18. N. B. Chaure, J. L. Sosa-Sanchez, A. N. Cammidge, M. J. Cook, and A. K. Ray, *Org. Electron.*, **11**, 434 (2010).
19. S. Yogev, R. Matsubara, M. Nakamura, and Y. Rosenwaks, *Org. Electron.*, **11**, 1729 (2010).
20. R. T. Weitz, K. Amsharov, U. Zschieschang, M. Burghard, M. Jansen, M. Kelsch, B. Rhamati, P. A. van Aken, K. Kern, and H. Klauk, *Chem. Mater.*, **21**, 4949 (2009).
21. G.-W. Kang, K.-M. Park, J.-H. Song, C. H. Lee, and D. H. Hwang, *Curr. Appl Phys.*, **5**, 297 (2005).
22. N. B. Chaure, S. Barard, A. K. Ray, A. N. Cammidge, and M. J. Cook, *EPL*, **104**, 57005 (2013).
23. I. A. Grimaldi, M. Barra, A. Carella, F. V. Di Girolamo, F. Loffredo, C. Minarini, F. Villani, and A. Cassinese, *Synth. Met.*, **176**, 121 (2013).
24. N. B. Chaure, A. N. Cammidge, I. Chambrier, M. J. Cook, and A. K. Ray, *ECS J. Solid State Sci. Technol.*, **4**, P3086 (2015).
25. J. Xu, X. Q. Liu, L. WangH., W. L. Hou, L. L. Zhao, and H. Q. Zhang, *Solid-State Electron.*, **127**, 61 (2017).
26. N. T. Boileau, O. A. Melville, B. Mirka, R. Cranston, and B. H. Lessard, *RSC Adv.*, **9**, 2133 (2019).
27. M. Kraus, S. Richler, A. Opitz, W. Brütting, S. Haas, T. Hasegawa, A. Hinderhofer, and F. Schreiber, *J. Appl. Phys.*, **107**, 094503 (2010).
28. R. W. I. de Boer, A. F. Stassen, M. F. Craciun, C. L. Mulder, A. Molinari, S. Rogge, and A. F. Morpurgoa, *Appl. Phys. Lett.*, **86**, 262109 (2005).
29. G. H. Heilmeier and S. E. Harrison, *Phys. Rev.*, **132**, 2010 (1963).
30. J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. J. Rider, *Appl. Phys.*, **53**, 1193 (1982).
31. M. Waldrip, O. D. Jurchescu, D. J. Gundlach, and E. G. Bittle, *Adv. Funct. Mater.*, **30**, 1904576 (2020).
32. K. Zhang, N. B. Kotadiya, X. Y. Wang, G. J. A. H. Wetzelaer, T. Marszalek, PisulaW., and P. W. M. Blom, *Adv. Electron. Mater.*, **6**, 1901352 (2020).