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Design and Characterization of a Radiation Tolerant Triple Mode Redundant Sense Amplifier Flip-Flop for Space Applications

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THESIS

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AFIT/GE/ENG/06-39

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ABSTRACT

One of the more recently proposed flip-flop designs has been the sense amplifier flip-flop. It has gained acceptance in the commercial realm because of its power consumption, speed, setup time, clock line loading, and data line loading characteristics.

In this thesis, a recently designed RADHARD version of D sense amplifier flip-flop was taken and a triple mode redundant version for space and radiation environment use was created. The design was created with valuable options to increase radiation hardness and to give end users greater flexibility in realizing their own radiation hardened version of flip-flop. In addition, a methodology for using a traditional circuit simulation tool, SPICE, was developed to test the operation of the flip-flop design for both normal conditions and under the influence of radiation.

The prescribed level of radiation resilience was chosen to reflect the upper bound of radiation tolerant design which is equivalent to a 100MeV Fe ion interaction with Si.

This work provides the results of the design effort and the characteristics of the final triple mode redundant sense amplifier flip-flop design both as a device which did not utilize any of the options created for use with the design and with various combinations of options employed.

This work also provides information on a revolutionary technology coined by the author (S&IC Technology, Sensor and Integrated Circuit Technology) which when used in conjunction with the triple mode design of this work would realize a self-sensing, self-correcting, and self-repairing triple mode design which would be of immeasurable benefit to space applications, avionics, and terrestrial applications the world over.

DEDICATION

To God and Country

ACKNOWLEDGEMENTS

I would like to thank everyone who made this thesis possible.

Mark E. Martin

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List of Acronyms/Abbreviations

AMI	American Megatrends Incorporated.
B	Boron.
BJT	Bipolar Junction Transistor.
C	Carbon.
CMOS	Complementary Metal Oxide Semiconductor.
Cu	Copper.
DICE	Dual Interlocked Cell.
DRAM	Dynamic Random Access Memory.
E	Energy.
EDAC	Error Detecting And Correcting.
EHP	Electron-Hole Pair.
FDSOI	Fully Depleted Silicon on Insulator.
Fe	Iron.
FF	Flip-Flop.
FIT	Failures In Time.
GaAs	Gallium Arsenide.
Ge	Germanium.
He	Helium.
HSPICE	High Accuracy Simulation Program with Integrated Circuit Emphasis.
IC	Integrated Circuit.
L	Length.
LET	Linear Energy Transfer.
LSI	Large Scale Integration.
Mg	Magnesium.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
NAND	not-AND.
Ne	Neon.
Ni	Nickel.
NMOS	N-channel Metal Oxide Semiconductor.
NOR	not-OR.
NSREC	Nuclear and Space Radiation Effects Conference.
O	Oxygen.
P	Phosphorous.
PDSOI	Partially Depleted Silicon on Insulator.
PMOS	P-channel Metal Oxide Semiconductor.
RC	Resistor-Capacitor.
SAFF	Sense Amplifier Flip-Flop.
SEB	Single Event Burnout.

SEE	Single Event Effects.
SEGR	Single Event Gate Rupture.
SEL	Single Event Latch-up.
SER	Soft Error Rate.
SET	Single Event Transient.
SEU	Single Event Upset.
Si	Silicon.
SiO_2	Silicon Dioxide.
SOI	Silicon On Insulator.
SPICE	Simulation Program with Integrated Circuit Emphasis.
SR	Set-Reset.
SRAM	Static Random Access Memory.
TID	Total Ionizing Dose.
TMR	Triple Mode Redundant.
TMRSAFF	Triple Mode Redundant Sense Amplifier Flip-Flop.
TSMC	Taiwan Semiconductor Manufacturing Company.
α-particles	Alpha-particles.
β-particles	Beta-particles.
γ-ray	Gamma-ray.
Δ-rays	Delta-rays.
ρ	Density.

DESIGN AND CHARACTERIZATION OF A RADIATION TOLERANT TRIPLE MODE REDUNDANT SENSE AMPLIFIER FLIP-FLOP FOR SPACE APPLICATIONS

I. INTRODUCTION

1.1 OVERVIEW

This chapter will go over the following topics:

1) Motivation for pursuing the problem to be solved.

2) A basic problem statement.

3) A basic plan of attack.

4) Contributions this work will provide.

5) A simple sequence of presentation.

1.2 MOTIVATION

Flip-flops are used extensively in time driven digital devices. Flip-flops influence the power consumption, speed and reliability of time driven digital devices and as a result are the most important device type to focus in upon to improve device performance. Figure 1.2.1 illustrates the percentage of error attributable to static combinational logic, sequential elements (latches and flip-flops), and memory. Figure 1.2.1 shows how sequential elements despite being vastly outnumbered by combinational logic and memory is the prime source of error in systems.

Focusing in on flip-flops is especially important in space applications because of the need to conserve power and operate in an environment which is inherently detrimental to the reliable operation of semiconductor devices. Indeed, radiation interaction with semiconductor circuits is directly attributable to spacecraft losses every year which could represent a considerable loss of money. For example, from 1998 to

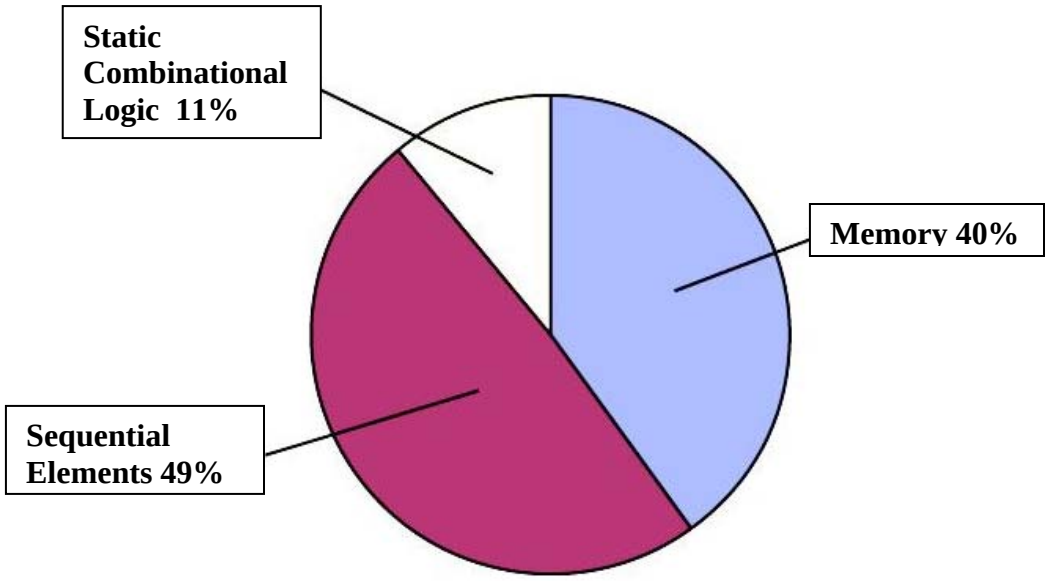

Figure 1.2.1: Pie chart depiction of the amount of soft-error attributable to static combinational logic, sequential elements and memory regardless of environment [1].

2004 twelve satellites were lost due to radiation interaction with the satellites circuitry which represented a total monetary loss of $500 million [2]. By 2005, there were 967 operating satellites in orbit around the Earth which represented a total of $190 billion in assets [3]. A sizeable portion of these satellites helped to support a $350 billion a year telecommunications industry [3]. Forecasts predict the launching of an additional 176 satellites worth $28.3 billion between 2006 and 2015 [4]. Radiation has been an issue in the past costing millions of dollars in losses and with so much money invested in space applications of all kinds it is imperative that better, more radiation resistant flip-flop designs be developed.

1.3 PROBLEM STATEMENT

The objective of this work will be to design and characterize a radiation tolerant triple mode redundant sense amplifier flip-flop (TMRSAFF) for use in space applications. The design will be created to provide:

1) Radiation tolerance up to the level of a 100MeV Iron (Fe) ion interaction.

2) Utilize a modified rail voltage to mitigate total ionizing dose (TID) effects.
3) Options to enhance radiation hardness against single event upsets (SEU's) and to provide designers greater flexibility in creating their own version of TMRSAFF.

1.4 PLAN OF ATTACK

The plan of attack for each component of the TMRSAFF design will be initially to assign values to items such as transistor sizes based on the authors initial desire to have a low power, high speed circuit. The plan of attack for the overall design will be to take the basic sense amplifier flip-flop (SAFF) design developed by Wang and Gong [5] and make three copies of the flip-flop. This triple mode redundant (TMR) flip-flop will then be enhanced and modified beyond traditional TMR design by incorporating several valuable options. After the design has been formulated, it will be simulated and tested for basic functionality. With a basically functioning TMRSAFF design, the next step will be to subject the design to simulated levels of cosmic ray ion interactions equivalent to that expected for a 100MeV Fe ion interaction. Adjustments to circuit parameters will be made as a result of empirical results achieved in simulation and simulations repeated until the circuit passes all radiation interaction simulation tests. Given that the circuit basically functions and delivers radiation tolerance results as specified then the circuit will be characterized for performance characteristics such as setup time, hold time, clock to Q delay and so on to establish it as a unique operating device.

1.5 CONTRIBUTIONS

The contributions of this work will include the following:

1) The successful design and characterization through simulation of the worlds first version of TMRSAFF.
2) Valuable options developed in the TMRSAFF design effort will serve as a list of potential options to incorporate in all TMR flip-flop designs to follow. As such, the options will serve as a precedent for follow on researchers to consider as they develop their own versions of radiation tolerant/hardened flip-flop circuits.
3) Development of testing methodologies using a conventional simulation tool for testing whether a given design meets radiation tolerance levels.

1.6 SEQUENCE OF PRESENTATION

This work is divided into five chapters and several supporting appendices. Chapter 1 provides motivation, a basic problem statement, a plan of attack, and contributions. Chapter 2 provides background information necessary to better understand why certain decisions were made in developing the TMRSAFF design. Chapter 3 will go over the methodology used to design and test the TMRSAFF proposed in this work. Chapter 4 provides the results of the characterization of the TMRSAFF design and Chapter 5 provides conclusions and some discussion on future work. The supporting appendices contain supporting information considered too lengthy to include in the main body of the text but which provide additional information for those interested parties.

II. BACKGROUND INFORMATION

2.1 OVERVIEW

Material that will be discussed in this chapter will be:

1) TID Effects on circuits.

2) Causes of single event upsets (SEU's) in circuits.

3) Choice of radiation tolerant design in the creation of the TMRSAFF design.

4) Definition of radiation tolerant design.

5) Definition of basic TMR design.

6) Justification for use of TMR in flip-flop design.

2.2 TID FFECTS ON CIRCUITS

When radiation traverses through a material it produces electron hole pairs (EHP's). When EHP's are generated in oxides a sizable portion of the negative and positive charge recombines but not all of the charge recombines. A certain portion of the generated negative and positive charge remains after a radiation event has occurred. The negative charge is generally drawn out of the oxide rapidly but positive charge is moved less rapidly. Consequently, there is a corresponding increase in the positive charge that exists in the oxide. Over time this positive charge migrates toward the silicon (Si)/silicon dioxide (SiO_2) interface. The application of positive voltages to conductors (typical in applications) encourages the migration of positive charge to the Si/SiO_2 interface because positive voltage repels positive charge. As charge builds up on the Si/SiO_2 interface of negative metal oxide semiconductor (NMOS) metal oxide semiconductor field effect transistors (MOSFET's), negative charge is drawn up to the Si/SiO_2 interface from within the substrate and shorting paths are formed in circuits. Figure 2.2.1 shows the formation

of a shorting path between the source and drain of an NMOS MOSFET as a result of positive charge build up on the Si/SiO_2 interface.

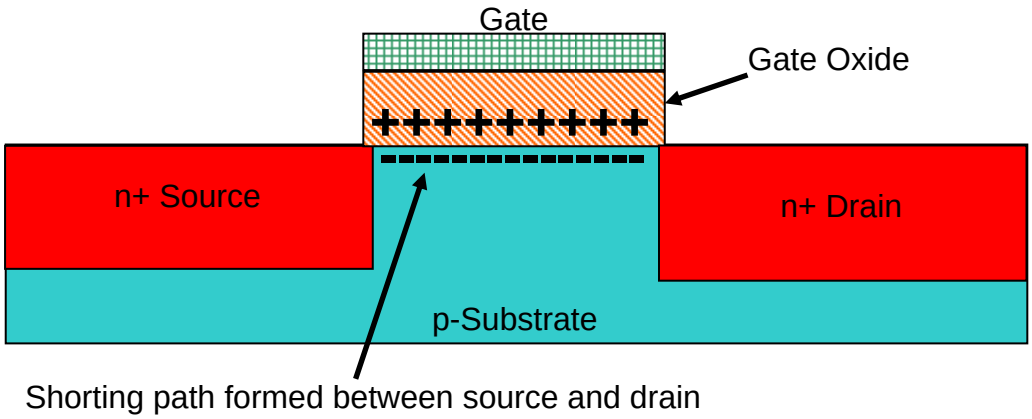

Figure 2.2.1: Formation of a shorting path between the source and drain of an NMOS device.

In instances where circuit conductors are routed over oxides which separate adjacent NMOS MOSFET's, a similar phenomenon as seen in the case of NMOS MOSFET gates produces a shorting path between what should be separated devices. This is illustrated in Figure 2.2.2 which shows the formation of a shorting path between the n+ regions of two adjacent NMOS MOSFET's. The accumulation of positive charge in the gate oxides of both NMOS and positive metal oxide semiconductor (PMOS) MOSFET's creates a phenomenon known as negative threshold voltage shift. The accumulation of positive charge and the subsequent attraction of negative charge to the Si/SiO_2 interface corresponds to an equivalent voltage source being applied to the gate of a transistor. The overall effect being that NMOS devices become more difficult to turn off while PMOS devices become more difficult to turn on. Figure 2.2.3 shows the effects of ionizing radiation dose absorbed by both NMOS (top graph) and PMOS (bottom graph) transistors and the corresponding shift of transistor threshold voltage.

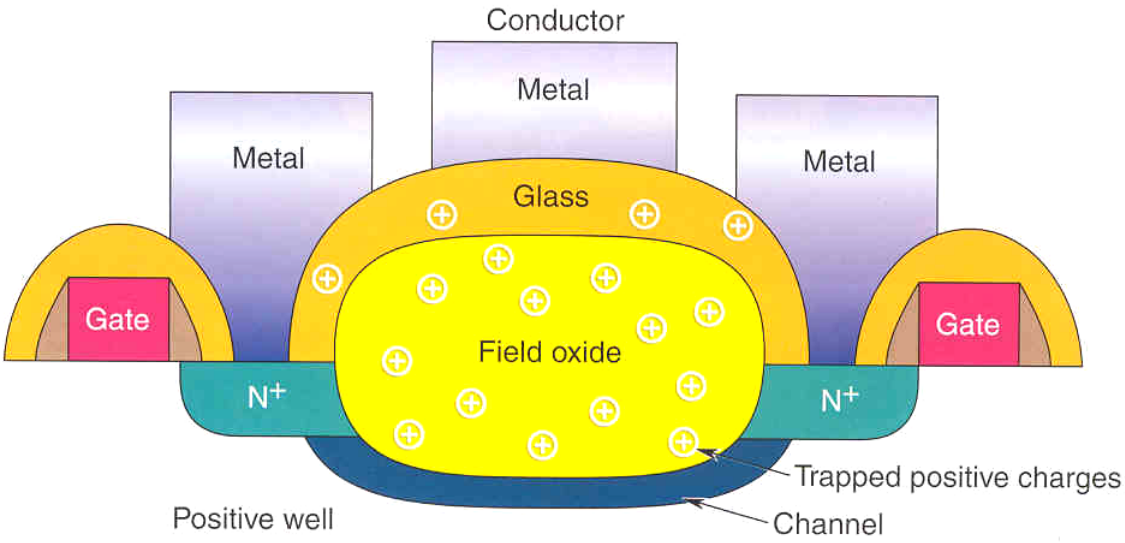

Figure 2.2.2: Formation of a shorting path between adjacent NMOS MOSFET's [23].

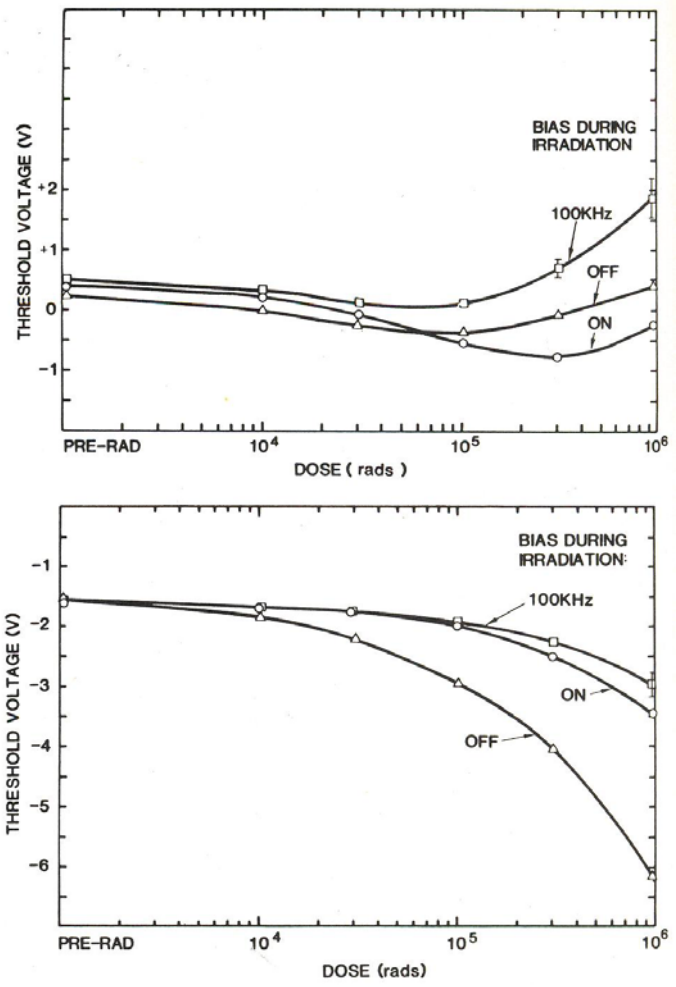

Figure 2.2.3: NMOS and PMOS transistor threshold voltage shift [6].

2.3 CAUSES OF SEU's IN CIRCUITS

Seu's are caused by one, a combination of two or potential all three of the following occurrences:

1) When a cosmic ray traverses through Si it generates what is referred to as a funnel which is shown in Figure 2.3.1. When this funnel collapses it collapses back toward the point of entry and as it does so, excess charge generated in the funnel (potentially as high as 10^{25} cm^{-3}) is drawn back toward the point of entry. If the point of entry was a node which was storing information, then the introduction of charge on to that node could cause an upset of the information (bit flip).

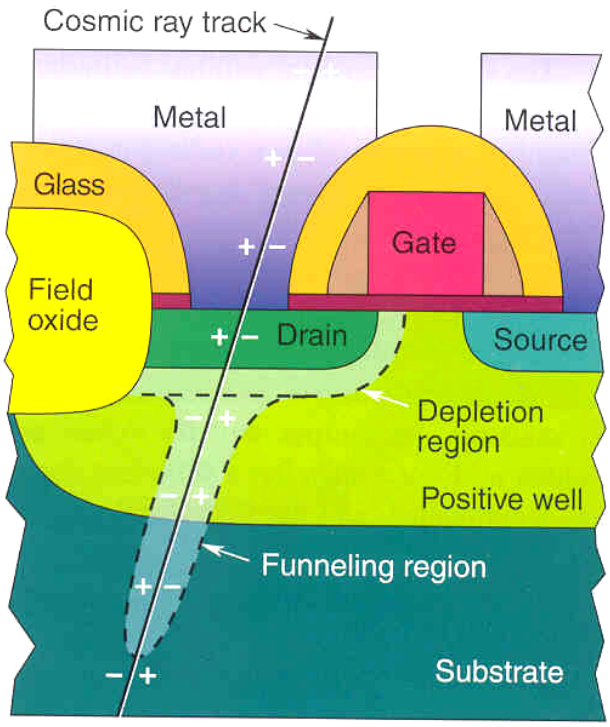

Figure 2.3.1: Funnel formation in Si [5].

2) If a cosmic ray traverses through the source or drain of a MOSFET, it creates an effect referred to as channel shortening where the physical length of the MOSFET channel is reduced. This reduction in channel length with applied biases

encourages the injection of charge across the channel of what should be a turned off transistor. This charge injection can cause upsets in information.

3) If a cosmic ray traverses through the source or drain of a MOSFET, it creates an effect in addition to that outlined in 2). It is referred to as a bipolar effect where charge concentration differences temporarily create a bipolar device which encourages the injection of charge in to the substrate of a MOSFET whereupon it can be collected by a node which is storing information. This also could cause information upsets.

Figure 2.3.2 shows an electron-micrograph of a charged particle going through the drain of an NMOS MOSFET. Dark regions in Figure 2.3.2 are indicative of regions which are predominantly made up of negative charge. Figure 2.3.2 shows the characteristic formation of a funnel, the shortening of the MOSFET channel, and charge injection toward the funnel due to bipolar effects.

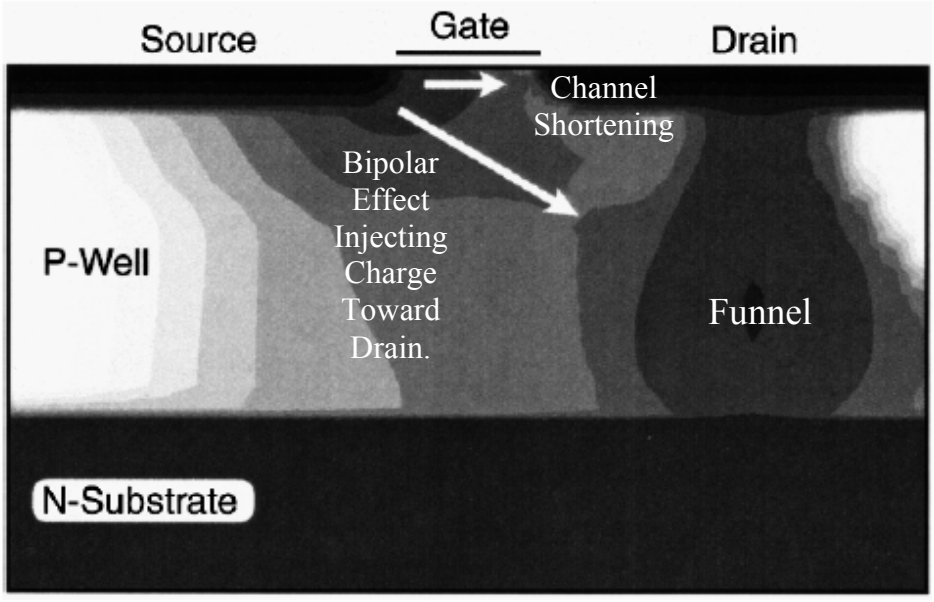

Figure 2.3.2: Electron-micrograph of charged particle interaction with NMOS transistor [7].

2.4 CHOICE OF RADIATION TOLERANT DESIGN

The reasoning behind pursuing radiation tolerant design as opposed to radiation hardened design of the TMRSAFF is mainly due to the fact that NASA currently has greater interest and need for radiation tolerant designs as opposed to radiation hardened designs [8]. This fact is conveyed in Figure 2.4.1 which shows the percentage of missions out of a representative group of 225 recent NASA missions and their requirements in the area of radiation design.

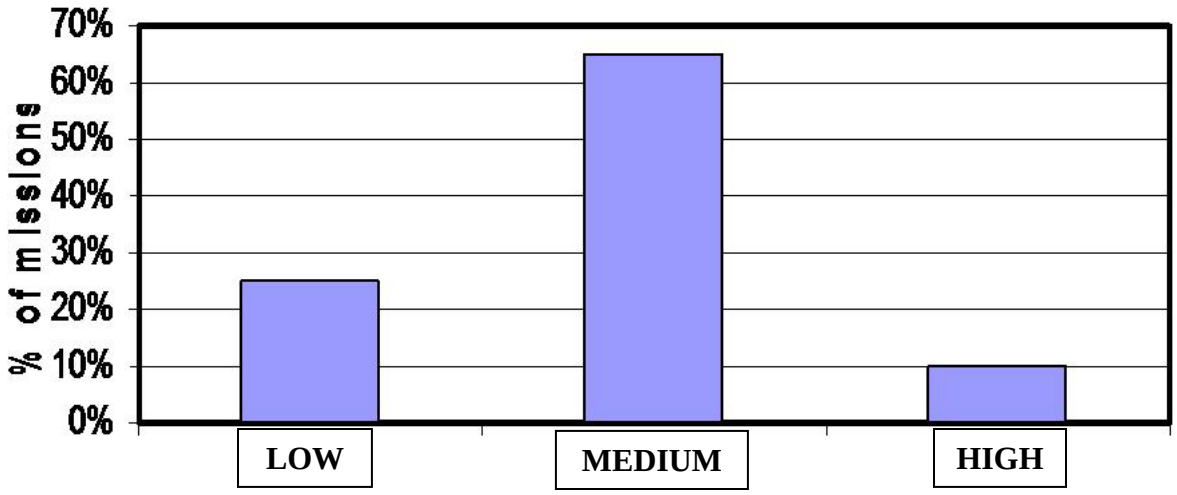

Figure 2.4.1: Bar graph representation of radiation design requirments of 225 recent NASA missions [8].

2.5 DEFINITION OF RADIATION TOLERANT DESIGN

The definition of radiation tolerant design as specified by NASA is as follows [9]:

1) Design assures radiation hardness up to a given level.
2) Hardness levels required are:
    a) Total Ioniziing Dose: 20-50krad minimum.
    b) SEU Threshold Linear Energy Transfer (LET): 20MeV-cm^2/mg minimum.
    c) Tested for functional fail only.

The LET of a 100MeV Fe ion in 27-30MeV-cm^2/mg [10]. It is for this reason and the fact that industry considers a 100MeV Fe ion to represent the upper bound of the typical natural radiation environment [10] that a radiation hardness level resilient up to the level required for a 100MeV Fe ion was chosen in the design of the TMRSAFF.

2.6 DEFINITION OF BASIC TMR DESIGN

The most fundamental realization of TMR design is shown in Figure 2.6.1. It shows TMR design in its most basic form. In this case, three identical copies of logic are routed into a majority logic gate, also known as a voter, which passes the value found on the majority of its inputs. Results of the majority logic determination then produce a single output.

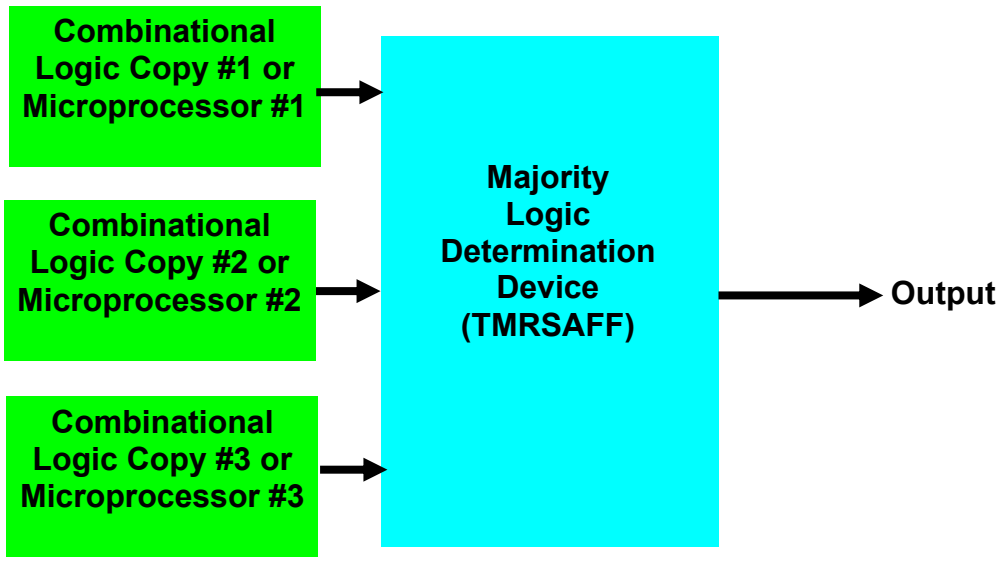

Figure 2.6.1: Basic TMR block diagram.

In the case of space applications, it is common for three identical copies of microprocessor to be routed to a majority logic gate which then passes the majority value found on its inputs to an overall system output. This arrangement generally requires that each processor be fabricated on its own chip and then be externally wired into a majority

logic chip which then votes on the results.

2.7 JUSTIFICATION FOR USE OF TMR IN FLIP-FLOP DESIGN

The main reason for utilizing TMR design in designing flip-flops is as follows:

1) If a single flip-flop is utilized, then the flip-flop has no means by which to either detect or correct for errors by itself.
2) If 2N flip-flops (an even number of flip-flops) are utilized then there is no ability to do basic tie breaking determinations. For example, if two flip-flops are utilized and one flip-flop outputs a high while the other flip-flop outputs a low then there is no way of knowing which flip-flop is correct.
3) If 2N+1 flip-flops (an odd number of flip-flops) are utilized then there exists the ability to do basic tie breaking. For example, if three flip-flops are utilized and one flip-flop outputs a high while the remaining two flip-flops output a low then routing into a majority logic gate will produce an ultimate low output for the group of three flip-flops.

The main reason for not utilizing more than three copies of any circuit to produce a more reliable device is because there is a point of diminishing return in reliability gained using more than three copies of a circuit while overall circuit performance can be detrimentally affected by utilizing more than three copies of a circuit. Table 2.7.1 lists a tabulation of reliability, transistor count, equivalent power consumption, and equivalent majority logic delay one would incur as a result of utilizing three, five, and seven copies of a sense amplifier flip-flop (SAFF) design [5] in realizing an overall N-modal version of flip-flop as shown in Figure 2.7.1.

Table 2.7.1: Tabulation of N-modal flip-flop performance parameters

Number of Copies (N)	Reliability	Transistor Count	Equivalent Power Consumption	Equivalent Delay In Majority Logic
3	94.3% [12]	222	34 units	2 units
5	94.88% [12]	358	59 units	3 units
7	94.98% [12]	556	95 units	5 units

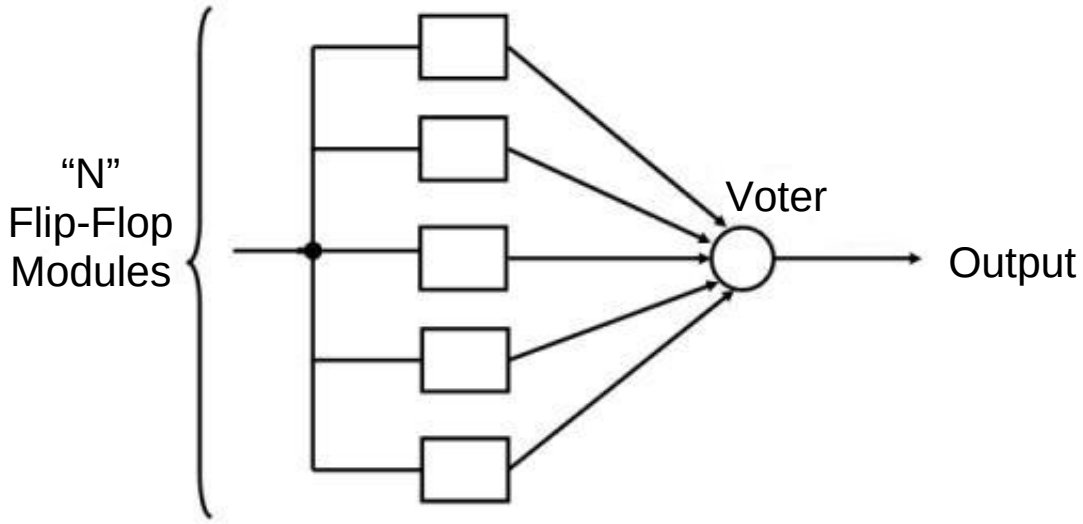

Figure 2.7.1: N-modal flip-flop [12].

The equation used to calculate the reliability of the N-modal flip-flop shown in Figure 2.7.1 was [11]:

$$R_{M\text{-}of\text{-}N} = R_{voter} \sum_{i=0}^{N-M} \left(\frac{N!}{i!\ (N\text{-}i)!} \right) (1-R)^i\, R^{N-i} \qquad \text{(Eq. 2.7.1)}$$

where $R_{M\text{-}of\text{-}N}$ is the reliability of an N-modal structure, R_{voter} is the reliability of the voting circuit, N is the number of identical units, M is the number of modules that must be functional, and R is the reliability of the individual components. For purposes of the

reliability calculations conducted to generate Table 2.7.1, a value for R was chosen to be 0.95 which was deliberately chosen to be unrealistically low in order to slant the calculations in favor of the higher number of copies. The value for M was adjusted to reflect the minimum number of flip-flops required to conducted a rudimentary tie breaking situation. For three copies of flip-flop, the value for M was 3 while for five copies of flip-flop M was 3 and for seven copies of flip-flop M was also 3. To determine the transistor count, a tally of the number of the transistors needed to create a basic SAFF [5] was added to the number of transistors needed to carry out the following majority logic determinations:

3-copies - AB+BC+CA.

5-copies- ABC+ACD+ACE+BCD+BCE+CDE.

7-copies- ABCD+ACDE+ADEF+AEFG+BCDE+BDEF+BEFG+CDEF+CEFG+DEFG.

The majority logic determination on transistor count, power dissipation, and delay was conducted assuming that CMOS was the technology utilized and that logic gates no larger than three inputs would be utilized. The reason for this is because logic gates with more than three inputs is known to be inefficient and induces a large increase in both power dissipation and delay. The power dissipation of both a two and three input logic gate was assumed to have a power dissipation of 1 unit while each level of gates needed to realize a particular majority logic determination was assumed to have a delay of 1 time unit. This would in reality reduce the power dissipation and delay that a majority logic determination would need that utilized three input logic gates as opposed to two input logic gates. Despite advantages given to higher copy versions tabulated in Table 2.7.1 there was not a significant increase in reliability going from three copies up to five or

seven copies. In contrast, there was a drastic increase in transistor count which translates into greater Si area to create the circuit and a considerable increase in both power consumption and delay. Therefore, the gist of Table 2.7.1 is to say that using anything more than three copies would be an inefficient implementation and would degrade the resulting circuits performance.

III METHODOLOGY

3.1 OVERVIEW

The material that will be covered in this chapter will be:

1) Background.
2) Choice of basic flip-flop technology in the TMRSAFF design.
3) Choice of specific flip-flop technology to use in the design of the TMRSAFF.
4) Basic TMRSAFF structure.
5) Basic functionality determination.
6) Basic timing parameter determination.
7) Basic Radiation Simulation.
8) How TMRSAFF counters TID Effects.
9) Radiation hardening options created in the TMRSAFF design.
10) Transistor sizing.

3.2 BACKGROUND

Schematics for the TMRSAFF design created in this work can be found in Appendices 8-15. The software package used to design and test the TMRSAFF design was Design Architect-IC v2005.1_1.1 software. It is a graphical user interface which allows for the use of either transistor or gate level design of circuits. The actual simulations were carried out using the 2005 release version of ELDO software contained within the Design Architect package. ELDO is a Mentor Graphics specific version of SPICE which has Mentor Graphics operations capability. This package was chosen because of its 100% compatibility with SPICE, accuracy, and its availability to industry and the general education community. The package provides an easy to use graphical

user interface (GUI) by which to create circuits. This was deemed vital for large complex circuits like those proposed in this work. Using ELDO provided calculations on power consumption and the Design Architect package allowed for the generation of varied sets of graphs for viewing circuit performance. In addition, the overall Design Architect package generates a SPICE netlist which allows for quick, less error prone insertion into other software packages like High Accuracy Simulation Program with Integrated Circuit Emphasis (HSPICE) for further validation of results.

The technology family used to design the TMRSAFF was the American Megatrends Incoporated 05 (ami05, 0.6 micron) family whose transistor characteristics are provided in Appendix 7. The decision to use this was based on the fact that this is a long established technology family that is readily accessible to the education community at large and is long since known to be of a reliable functioning nature. The 0.6 micron technology family has been in use for many years and has a comprehensive listing of transistor circuit parameters which many smaller technology families which could have been used at the present time does not. In addition, by starting with a large technology family the speed of the design would be less than that possible for smaller technology families. As a result, downscaling would produce circuits that will run faster and have smaller mechanisms by which failures can occur (smaller diffusions).

The bulk of the work done to produce the TMRSAFF design was decided to be done empirically where initial decisions were made on issues such as transistor sizes. After initial device sizes were decided upon then tests were summarily conducted where faults which simulate radiation interactions were employed on various nodes to be analyzed and a size increasing algorithm employed to step up the size of devices was

employed to harden the node up to the prescribed level of a 100MeV Fe ion interaction.

Preliminary work which is not included in this write up was conducted by the author and it was determined that radiation hardening strictly through the brute force method of using larger transistors for larger capacitance would not work even for such a large technology family as the ami05 family. This was because of the fact that in radiation hardening one must manipulate resistor-capacitor (RC) time constants. The faster a circuit is for propagating correct signals then the faster it will be for propagating incorrect signals introduced into the system by radiation interactions. As such, some degree of compromise would have to be made at some point in the opposing performance criteria of speed versus reliability. Given this it really made little difference how large a capacitor like a transistor gate or diffusion was made when the circuit impedance was low. It was from this observation that the decision was made to allow for the use of resistors in the TMRSAFF design in order to achieve desired radiation hardening results

In general, it was decided for the purposes of conserving silicon area that a practical limit would be placed on the width of any transistor in the TMRSAFF design of no more than W = 50 or 50λ. This translates into a physical dimension of 15μm (0.6μm x 50/2). In practice, most transistor widths proposed in the TMRSAFF design this work is based upon were sized well below the limit of 50λ to allow for some room in increasing transistor widths as smaller technology sizes are used to scale the design down. It was also decided early on that for silicon area conservation, ease of design, and the fact that the practice is common that all transistors would be made to have a length (L) of 2λ. Thus, every transistor in the TMRSAFF design has L = 2. Another practical designation decision was made on the maximum size of resistors in the circuit. Resistors were

decided not to be larger in size than 15kΩ. This was done to allow for the potential use if the end user so desires of depletion mode transistors in design as exceedingly large resistances may be difficult to achieve using depletion mode transistors. In fact, the use of transistors to achieve impedance is limited generally to a range of 1-30kΩ. As such, limiting resistance values to 15kΩ would leave considerable room for increasing the size of resistors in the event the TMRSAFF design is downscaled to a smaller technology size.

3.3 CHOICE OF BASIC FLIP-FLOP TECHNOLOGY IN THE TMRSAFF DESIGN

Extensive literature review was conducted on basic flip-flop technologies where various types of state of the art flip-flops were considered for use in the development of the TMRSAFF design. Five parameters were focused in upon in order to choose the basic flip-flop technology. These parameters were power consumption, clock to Q delay, setup time, clock loading, and data line loading. The power consumption of the basic flip-flop technology would have to be as low as possible while at the same time providing the shortest clock to Q delay possible in order to have good speed characteristics. In addition since radiation hardening would slow the TMRSAFF design down, setup time would have to be as short as possible in order that the TMRSAFF design would not consume too much time in passing a value and thus leave more time per clock cycle for combinational logic to perform its functions. Because the system clock and its associated loads constitute the largest consumer of power in a system, and the data line constitutes the third largest consumer of power in a system it was decided to choose a flip-flop technology that would reduce these parameters too as low a value as possible in order to further reduce power consumption. The results of the research resulted in the choice of

using sense amplifier flip-flop (SAFF) technology in the TMRSAFF design. Table 3.3.1 provides parameters on clock power, data power, total power, delay and setup time for 6 state of the art flip-flop technologies.

Table 3.3.1: Tabulation of state of the art flip-flop designs [18]

Flip-flop Type	Clock Power (μW)	Data Power (μW)	Total Power (μW)	Delay (ps)	Setup Time (ps)
SAFF	18	3	158	272	-35
K6-ETL	15	5	349	200	-4
SSTC	22	4	160	592	267
DSTC	22	4	198	629	263
Hybrid SSTC	14	1	146	892	476
Hybrid DSTC	13	1	185	1060	480

3.4 CHOICE OF SPECIFIC FLIP-FLOP TO USE IN THE TMRSAFF DESIGN

The specific flip-flop design which was selected to create the TMRSAFF design was a design put forth by Weizhong Wang and Haiyan Gong from the University of Wisconsin [5]. The schematic for this design is provided in Figure 3.4.1. The design was chosen for several basic reasons as follows:

1) The design eliminated the occurrence of self-locking which has plagued SAFF technology and thus has prevented SAFF technology from be utilized in radiation environments.
2) The design generates fully redundant outputs (Q0, Q1 primary and Q2, Q3 redundant in Figure 3.4.1). This would allow for the creation of a redundant output path for the overall TMRSAFF design which would represent an alternative path for passing information to the output of the TMRSAFF design.

3) The design is fully static which translates into nodes which when interacted with by radiation would quickly recover and return to their original quiescent state prior to the interaction event.

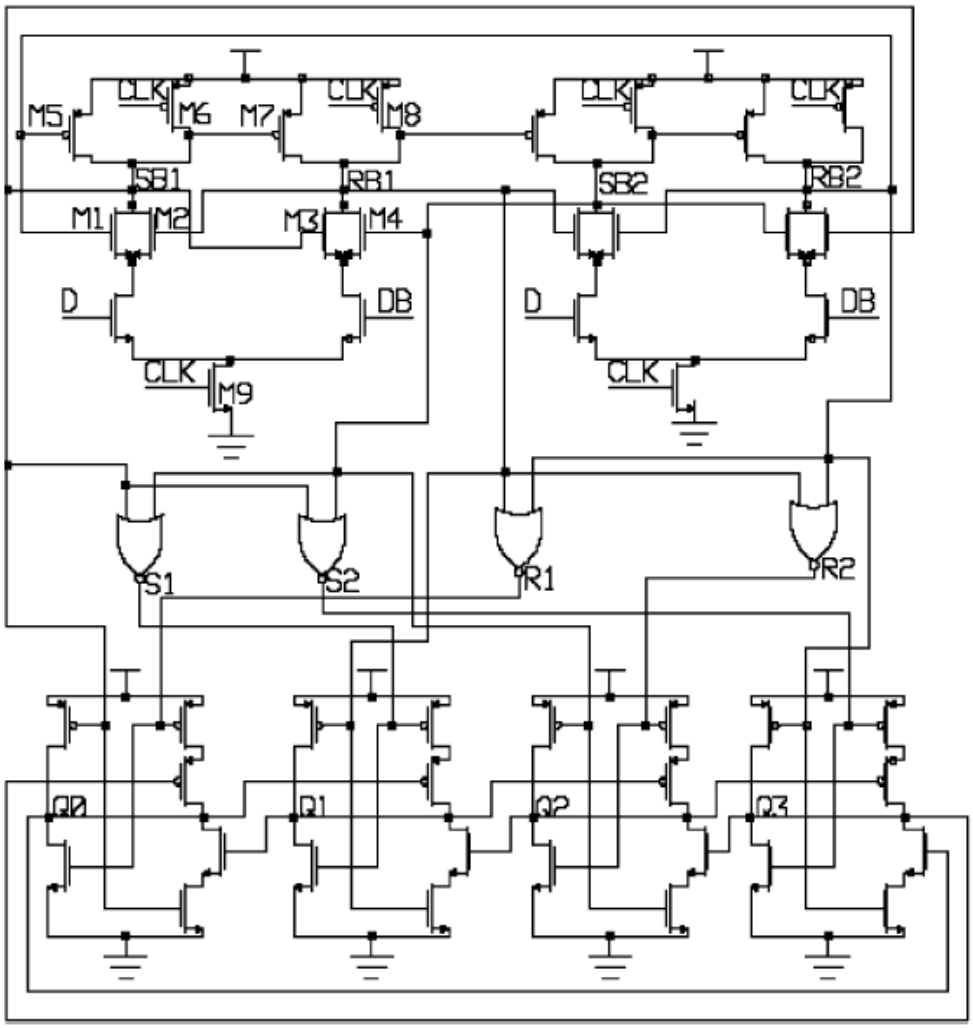

Figure 3.4.1: Schematic of Wang and Gong SAFF design [5].

In addition, the Wang and Gong design was compared to two state of the art flip-flop designs currently in use in space applications [5]. The results of these comparisons are provided in table 3.4.1 which compares the Wang and Gong design to the SAFF technology currently in use in the state of the art ALPHA 21264 space microprocessor and in Table 3.4.2 which compares the Wang and Gong design to the most commonly

utilized flip-flop design in space applications, the basic DICE flip-flop. The results of the comparison were that the Wang and Gong design was superior to both the ALPHA 21264 space microprocessor SAFF technology and basic DICE flip-flop technology in the areas of clock to Q delay, data line loading, and clock network loading.

Table 3.4.1: Comparison of the Wang and Gong SAFF design to the SAFF design utilized in the ALPHA 21264 space microprocessor

	WORST CASE CLOCK TO Q DELAY	LOADING TO DATA INPUT LINE	LOADING TO CLOCK NETWORK
W&GD SAFF	367ps	0.186pJ	0.484pJ
ALPHA 21264 SAFF	412ps	0.212pJ	0.536pJ
PERCENT CHANGE	-10.9%	-12.3%	-9.7%

Table 3.4.2: Comparison of the Wang and Gong SAFF design to basic DICE flip-flop technology

	WORST CASE CLOCK TO Q DELAY	LOADING TO DATA INPUT LINE	LOADING TO CLOCK NETWORK
W&GD SAFF	367ps	0.186pJ	0.484pJ
DICE FF	476ps	0.245pJ	1.03pJ
PERCENT CHANGE	-22.9%	-24%	-53%

3.5 BASIC TMRSAFF STRUCTURE

The basic structure of the TMRSAFF design was comprised of three copies of the Wang and Gong SAFF design as the input flip-flops. The primary outputs of each input SAFF were routed to one majority logic gate while the redundant outputs of each input SAFF were routed to a duplicate majority logic gate. Each majority logic gate was then routed into an output SAFF which was made by modifying the Wang and Gong flip-

flop design. The modifications employed were to remove the S2 and R2 NOR gates along with the Q2 and Q3 output latches seen in Figure 3.4.1. The master clock was routed into each of the input SAFF's and an appropriate delay of the master clock was used to provide the driving clock signal for each of the output SAFF's. Output SAFF's were employed with the TMRSAFF design in order to prevent the TMRSAFF from being a source of glitches in the system. In addition, the decision was made to derive the driving clock signal of the TMRSAFF output flip-flops local to the flip-flop in order to relieve reliance on outside sources for clocking. In order to ensure basic radiation hardness up to the level of a 100MeV Fe ion interaction, it was decided to harden all of the nodes of the input and output SAFF's up to the level of a 100MeV Fe ion interaction. Figure 3.5.1 shows in simplified block diagram form the basic structure of the TMRSAFF design.

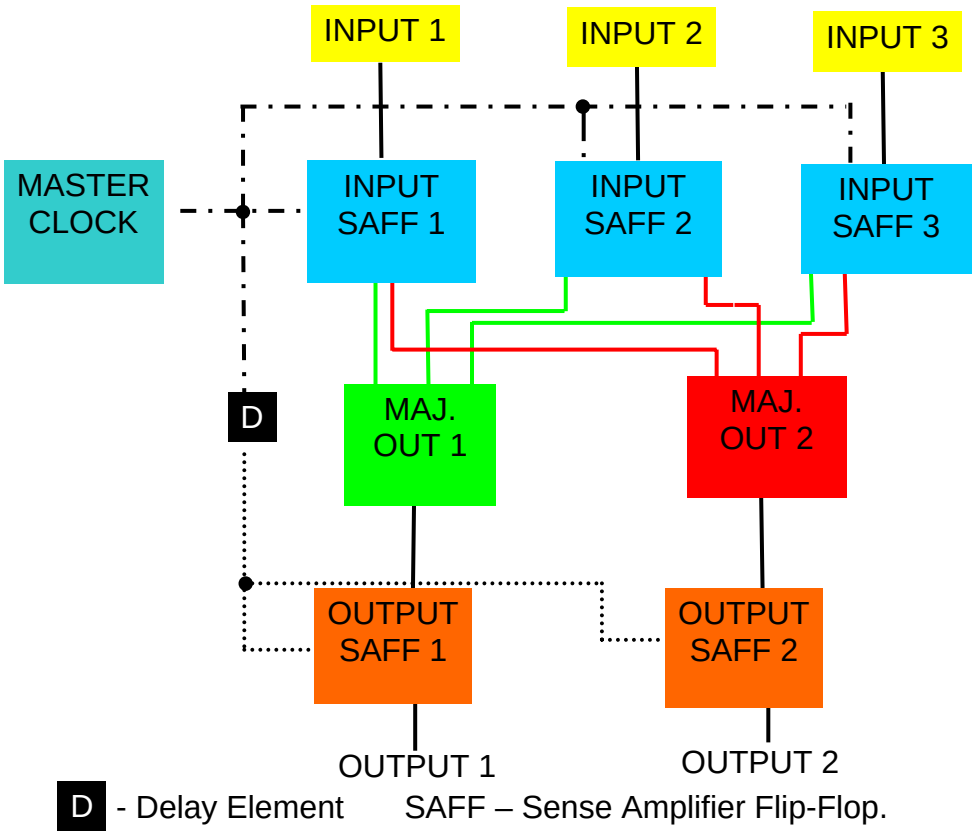

Figure 3.5.1: Basic block diagram of the TMRSAFF design.

3.6 BASIC FUNCTIONALITY DETERMINATION

In order to ensure that each individual flip-flop utilized in the TMRSAFF design was functioning properly as a flip-flop, the decision was made to create what is referred to as a basic functionality test vector. This vector is provided in Appendix 1 and is referred to in this text as the basic functionality test vector (D input). Because each individual SAFF, has both a D and DB (D complement) input the test vector provided in Appendix 1 was created to apply to the D input of an individual SAFF while the test vector provided in Appendix 2 was created to apply to the DB input of an individual SAFF.

In this way, items such as worst case clock to Q time, setup time, hold time, and power consumption could be determined for singular SAFF's like the SAFF design proposed by Wang and Gong or the modified SAFF design proposed by the author for use as the output stage of the TMRSAFF. A typical set of values for the basic functionality test vector (D Input), the basic functionality test vector (DB Input), and the corresponding correct flip-flop output responses are provided in Figure 3.6.1.

It was decided to test flip-flops for seven distinct events as follows:

1) With a high value already clocked into the output of the flip-flop if the data input stays at a high value then the output of the flip-flop should remain at a high value.
2) With the flip-flop output already at a high output value then the data input should go low prior to the incoming rising clock edge and the flip-flop should clock in a low value to its output.
3) With the flip-flop having clocked in a low value to its output then have what amounts to an out of phase input value corresponding to a high value come in during the

falling transition of the clock but which returns to a low value prior to the next rising edge of the clock. Here the flip-flop output should remain at a low value. This will verify that high data sitting at the input does not affect the output and that the design is a positive edge triggered device.

4) With a low value already clocked into the output of the flip-flop if the data input stays at a low value then the output of the flip-flop should remain at a low value.
5) With the flip-flop output already at a low output value then the data input should go high prior to the incoming rising clock edge and the flip-flop should clock in a high value to its output.
6) With the flip-flop having clocked in a high value to its output then have what amounts to an out of phase input value corresponding to a low value come in during the falling transition of the clock but which returns to a high value prior to the next rising edge of the clock. Here the flip-flop should remain at a high value. This will verify that low data sitting at the input does not affect the output and that the design is a positive edge triggered device.
7) Run the flip-flop through several oscillations so that it can be seen that repetitive transitions from high to low can be handled without error.

In Figure 3.6.1, Q1_CLK is the clock input, D1 is the D input, DB1 is the D complement input, Q0_1 is the primary output, Q1_1 is the primary complement output, Q0_11 is the redundant output, and Q1_11 is the redundant complement output for the SAFF's used in the design of the TMRSAFF. It should be understood that the Q0_1 output shown in Figure 3.6.1 is the correct response to all flip-flop primary outputs whether it be for the design proposed by Wang and Gong or the modified SAFF proposed

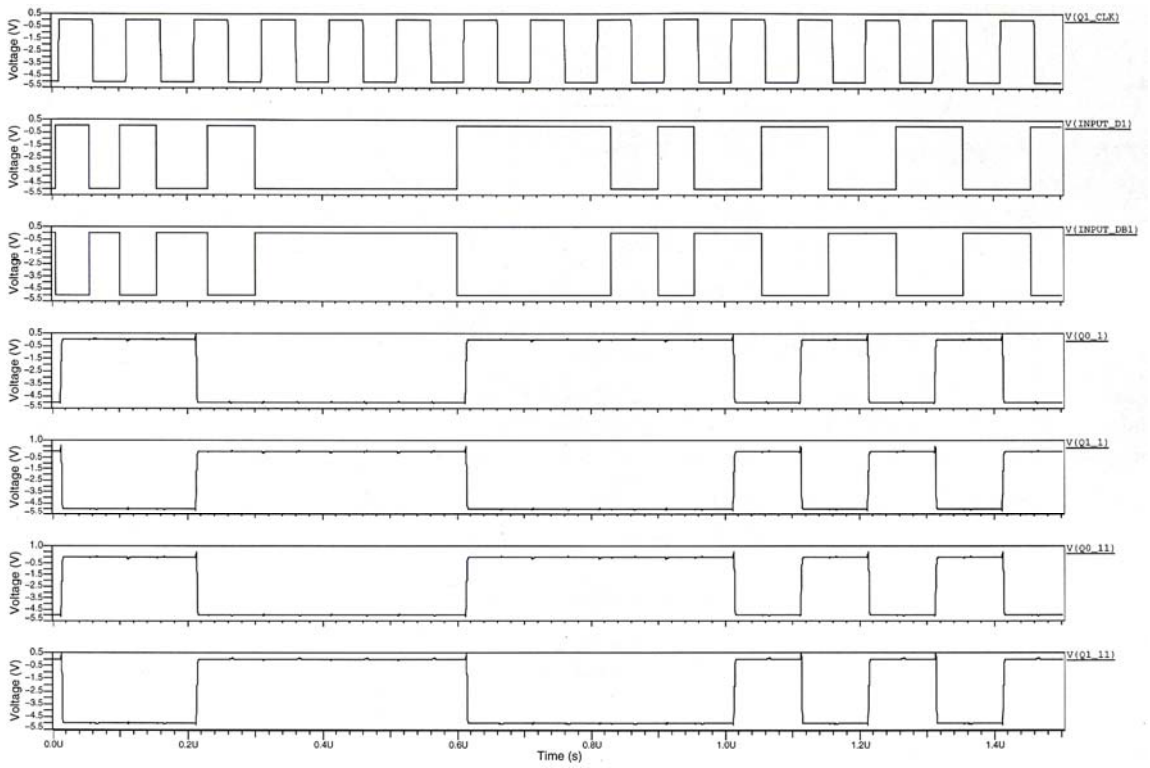

Figure 3.6.1: Graph of applied inputs and corresponding output results for running the basic functionality test vector/vectors in checking the performance of the individual flip-flops used in this work.

by the author for the TMRSAFF output, or the overall TMRSAFF design itself when running the basic functionality test vector/vectors.

Referring to Figure 3.6.1, one will note that D (and DB) oscillate low to high from t = 0 to t = 180ns. This is the portion of the basic functionality test vector that tests for the input being at a high and the output staying at a high in the face of oscillating input. Time t = 210ns tests the flip-flop input being low and the output transitioning to a low. The step function which occurs at 220ns and ends at 300ns is a test for an out of phase high signal being applied to the input. The period from 300ns to 600ns tests for the input of a flip-flop being at a low value and the output staying at a low. Time t = 610ns tests for the input of a flip-flop being at a high value and the output of the flip-flop transitioning to a high value.The time period from 610ns to 830ns tests for the input of a flip-flop being

high and the output staying at a high. The dip at t = 830ns and lasting to 900ns tests for an out of phase low signal coming in to the flip-flop. Finally, the oscillations which start at 1050ns and last the remainder of the 1500ns of the basic functionality test vector test for correct operation when the flip-flop is subjected to oscillatory input. This short test effectively accomplishes the task of testing a flip-flop's operation for each of the seven items previously listed. It was during basic functionality test runs where current barrages like those which will be described in the next section were applied and the response of the circuit judged for correct operation. It was also during basic functionality tests that power dissipation numbers for a flip-flop were taken.

Once all individual flip-flops to be used in the TMRSAFF design were verified for proper functionality using the basic functionality test vector, then the TMRSAFF shown in Figure 3.5.1 was created and the basic functionality test vector (D input) was applied to the TMRSAFF in order to verify its basic functionality and to acquire basic performance parameters on items such as clock to Q delay, setup time, hold time, and power dissipation.

3.7 BASIC TIMING PARAMETER DETERMINATION

The manner in which the TMRSAFF clock to Q delay was determined is illustrated in Figure 3.7.1. In order to calculate the clock to Q delay of either a high to low or low to high transition, it was decided to use the 90% transition point on the corresponding waveforms (-0.5V going from low to high or -4.5V going from high to low in Figure 3.7.1). This was done because when a transition reaches to within 0.5V of its final value one is assured that only the transistor type (either PMOS or NMOS) which was meant to be turned off downstream of the TMRSAFF would in fact be turned off.

Unfortunately, the threshold voltage of NMOS devices in the ami05 transistor family has a value of 0.7V while that of a PMOS device is -0.9V. So, a value less than 0.7V was required so that timing calculations could be universally conducted.

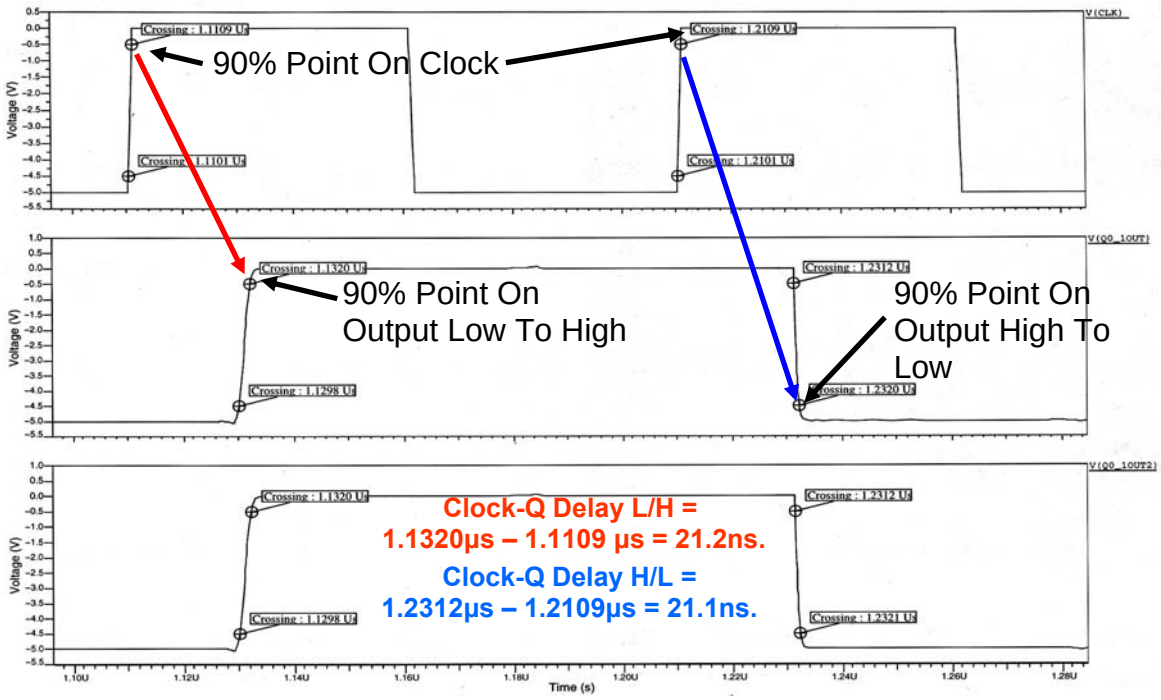

Figure 3.7.1: Basic determination of TMRSAFF clock to Q delay.

The manner in which setup time was calculated was to apply a regularly oscillating input signal to the TMRSAFF and checking that for both high to low and low to high data transitions that the TMRSAFF correctly produced the appropriate output. If the output was correct then the data input was delayed such that the transition edge of the input data signal was moved 5ps closer to the driving clock edge. This process of advancing the input data towards the driving clock edge was continued until finally the TMRSAFF failed to correctly pass appropriate data to its output. A similar methodology was used to determine TMRSAFF hold time where the incoming data was held steady for a certain period after the incoming driving clock signal. If the data was successfully

passed to the output of the TMRSAFF, then the data transition edge was moved 5ps closer to the clock driving edge until the TMRSAFF no longer correctly passed data to its output.

3.8 BASIC RADITION SIMULATION

To simulate the effects of charged particle interaction with the MOSFET's of the TMRSAFF design, it was decided to use the traditional methodology of applying a current source from the node to be tested to the low circuit rail voltage (NMOS FAULT) or from the high rail voltage to the node to be tested (PMOS FAULT). The reason for this is because NMOS devices are susceptible to "1" to "0" bit flips. This is so because as a particle goes through the n^+/p diode formed by the drain of an NMOS device into the p-substrate that it is formed in, the p-substrate is grounded to protect against latch-up. This creates a connection from ground to the node. Therefore, a current source from the node to be tested to the low rail voltage was considered adequate for testing the effects of a particle interaction through an n^+/p diode (NMOS FAULT).

As for PMOS devices, they are susceptible to "0" to "1" bit flips. This is so because as a particle goes through the p^+/n diode formed by the drain of a PMOS device into the n-well that it is formed in, the n-well is connected to the high rail voltage to protect against latch-up. As a result, a connection is formed from the high rail voltage to the node which creates a means by which charge can be forced on to a node. Given this then a current source from the high rail voltage to the node being tested was deemed adequate to test for a particle interaction through a p^+/n diode (PMOS FAULT). The issue of determining the shape and form which a 100MeV Fe ion would take as a result of interacting with Si was answered as a result of private communications with Paul Dodd (Project Manager of

Sandia Laboratories Radiation Effects Testing Division and a world expert in the area of radiation event testing) [13] who recommended the use of the Dorkel mobility model [14]. This model calculates semiconductor mobility and takes into account parameters such as temperature, doping concentration, and carrier injection. Figure 3.8.1 provides the current response of a 100MeV Fe ion interaction with an n+/p diode which is the basic structure one encounters in NMOS MOSFET's. It shows two curves which attempt to predict the amount of current that flows when a 100MeV Fe ion interacts with the n^+/p diode of an NMOS device. The curve labeled "No carrier-carrier model" is the result one would get as a result of neglecting carrier-carrier scattering in the Dorkel model. The model labeled "Dorkel model" is the result one would get as a result of running the Dorkel model with carrier-carrier scattering taken into account.

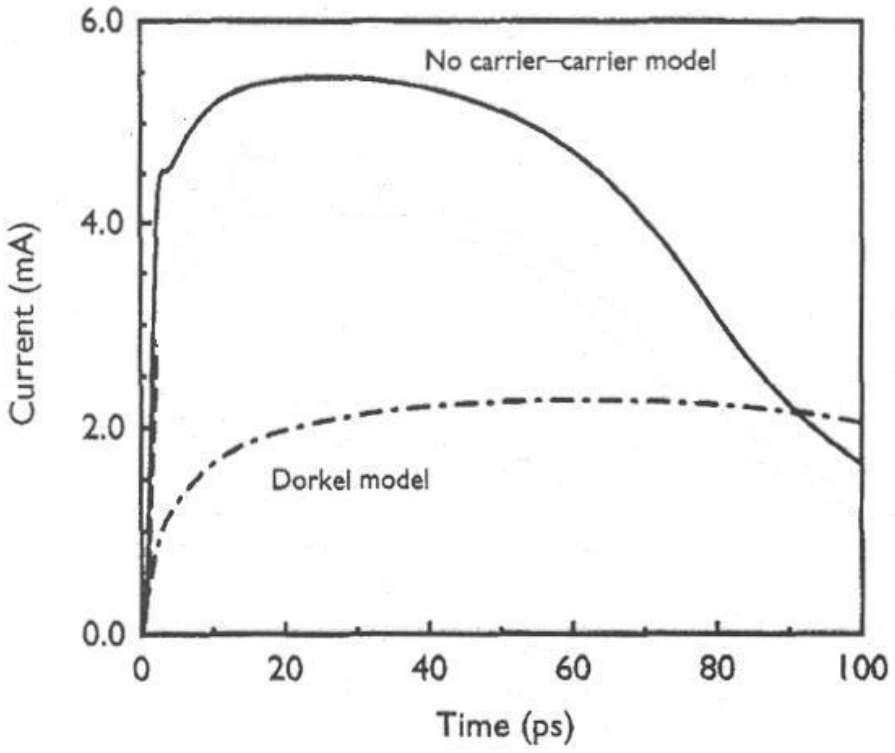

Figure 3.8.1: Graph of current response of 100MeV Fe ion interaction with an n+/p Si diode using the Dorkel model [24].

The decision was made to create a step function current source for the testing of faults on the n^+/p diodes of any NMOS transistors found in the TMRSAFF circuit design by composing it of two different components. The components would be composed of a prompt dose whose magnitude was determined by using the, "No carrier-carier model", peak amplitude in Figure 3.8.1 which can be seen to be 5.5mA. The duration of this prompt component was determined by finding the intersection of the two curves in Figure 3.8.1 and rounding up to the nearest factor of ten which in Figure 3.8.1 can be seen to be 100ps. So, the prompt component of a 100MeV Fe ion interaction would be 5.5mA for 100ps. The remaining component (referred to as a diffusion component) would be determined by using the Dorkel model where carrier-carrier interactions were taken under consideration from 100ps out to 2000ps. The decision to run the Dorkel model out to 2000ps was made on recommendation from Ken Label (NASA Radiation Effects Group. Project Manager) who stated that radiation affects intervals considered by NASA average approximately 2ns in duration [16]. An equation which mimicks the exponential decay from 100ps to 2000ps (2ns) is as follows:

$$I(t) = (0.002)\exp^{-(t-100)/1000}\ (A) \qquad \text{(Eq. 3.8.1)}$$

where the time t is measured in picoseconds and the result is in amps.

Figure 3.8.2 shows the resulting step function used as the basis for simulating a 100MeV Fe interaction on the n^+/p diodes which exist in the NMOS transistors of the TMRSAFF design. This type of current occurrence is referred to in this text as a low current test model. For purposes of pushing the design to a limit beyond that which it was designed, the author created another waveform which simply adds 0.5mA to all the values shown in Figure 3.8.2. This is referred to in this text as a high current test model

and is shown in Figure 3.8.3.

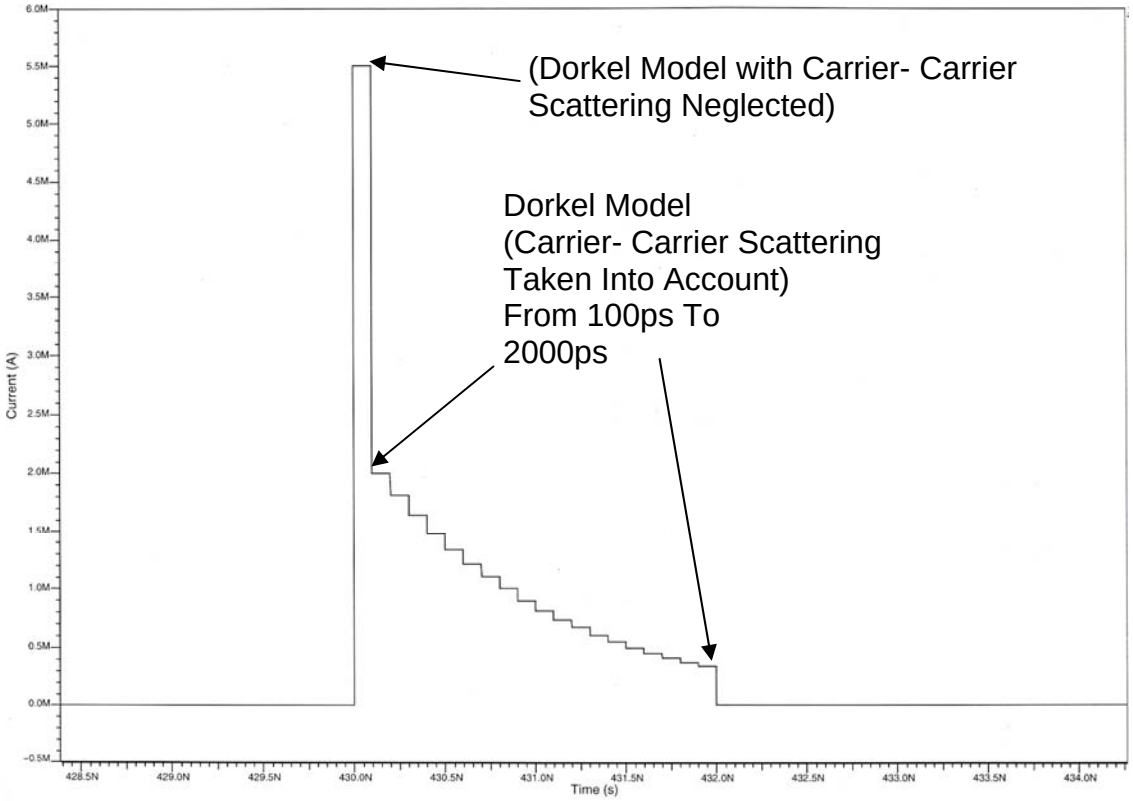

Figure 3.8.2: Low current test model.

For purposes of testing the various nodes in the TMRSAFF design, what were referred to as current barrages were created as test vectors for the circuit. One is provided in Appendix 3 and is known as a low current barrage test vector. It is comprised of current events like those shown in Figure 3.8.2. Along the same lines, something called a high current barrage test vector was created and a copy of one is provided in Appendix 4. It is comprised of current events that are like those shown in Figure 3.8.3 and are made to occur at the same times as those specified for the low current barrage test vector. Figure 3.8.4 shows the time spread for the low current barrage test vector provided in Appendix 3 and the high current barrage test vector provided in Appendix 4 in conjunction with the running of the basic functionality test vector which is shown as the top graph in Figure

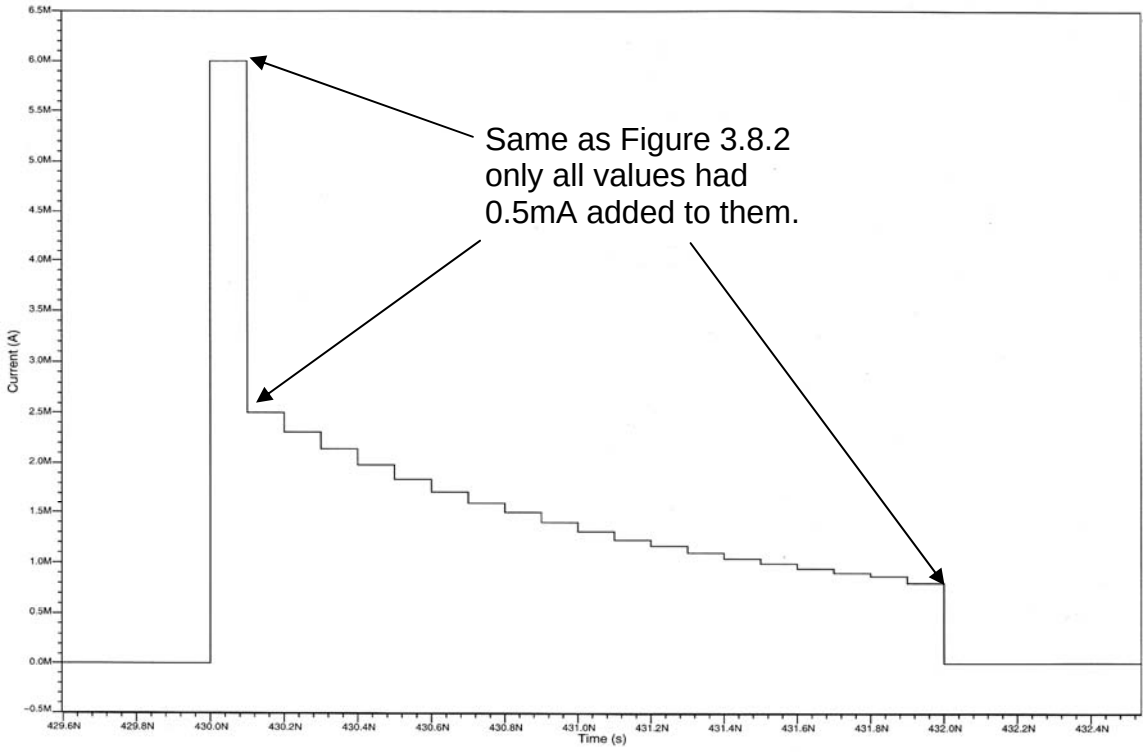

Figure 3.8.3: High current test model.

3.8.4. It was during the running of the basic functionality test vector on the TMRSAFF that these barrages were applied to a node and errors observed to occur on the TMRSAFF's output.

The theory behind generating two current barrages, each of a different magnitude was to try and come up with a method that would allow the development of near optimal results in terms of transistor and resistor sizing on circuit nodes. If a node passed the low current barrage test vector, but failed the high current barrage test vector then the node in question would be considered near optimal in terms of device sizing (capacitance and/or resistance applied to a node). As such, a designer would know that the choices for transistor and/or resistor sizing on the node were adequate to harden the circuit up to the prescribed radiation level but at the same time did not add unnecessary capacitance or resistance to a node which would increase power dissipation and increase delay. An

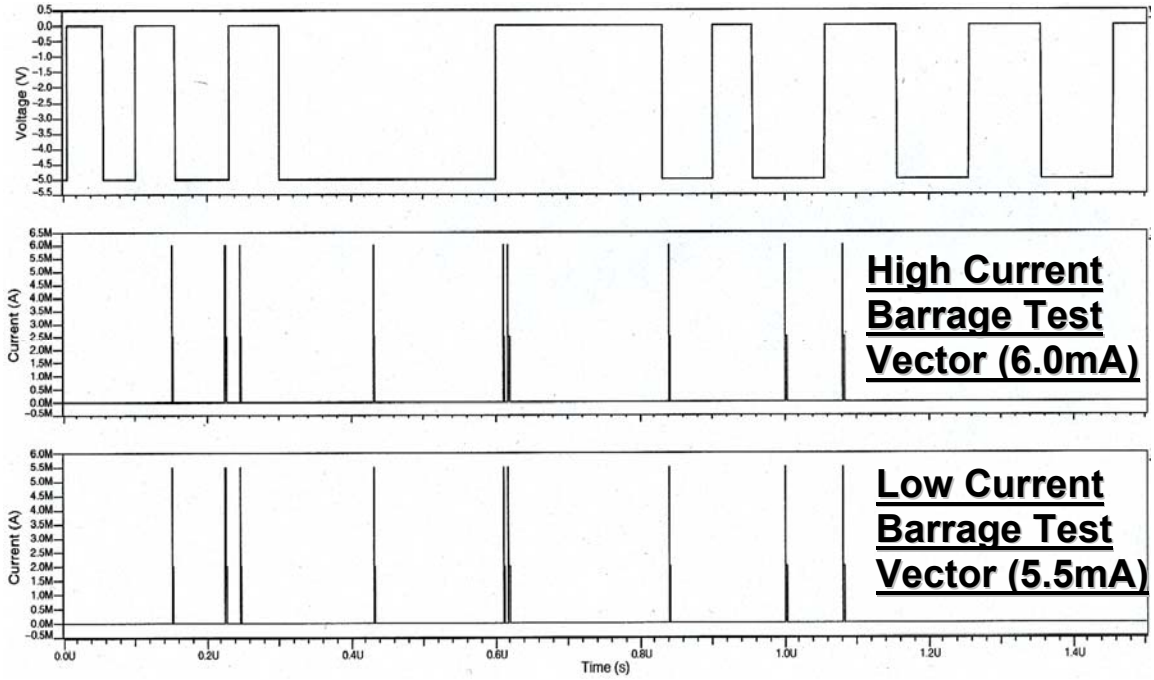

Figure 3.8.4: Timing graph showing the application of one high current barrage test vector and its corresponding low current barrage test vector to a node under radiation simulation testing.

example of how radiation testing was conducted on a node in the Wang and Gong SAFF design can be seen in Figures 3.8.5-3.8.7. Figure 3.8.5 shows the choice of node SB1 in and the propostion of connecting a current source to the node whereupon either a high current barrage test vector or a low current barrage test vector would be applied.

Figure 3.8.6 shows the results of running the low current barrage test vector shown in Figure 3.8.4 on node SB1 of Figure 3.8.5. The results were that several spikes appeared on the output Q0_1 but no incorrect information was latched into the flip-flop. However, when the high current barrage test vector shown in Figure 3.8.4 was applied to node SB1 in Figure 3.8.5 it resulted in an incorrect value being latched into output Q0_1 at approximately 0.24μs in Figure 3.8.7.

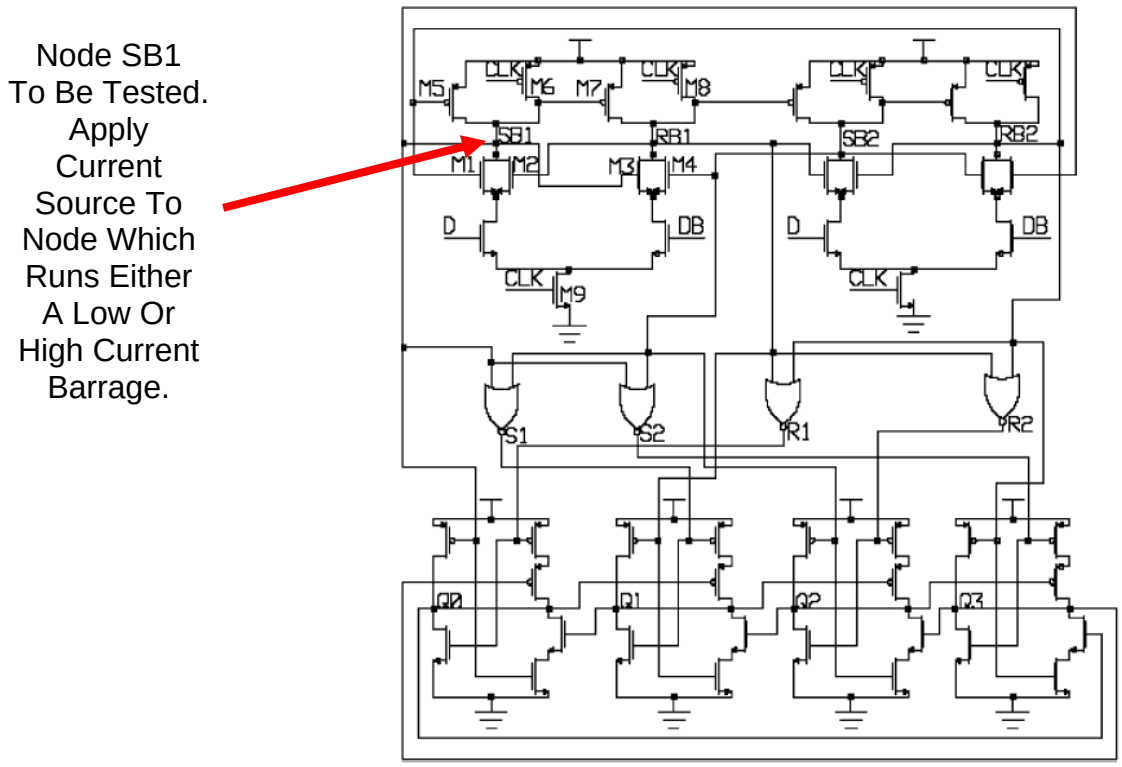

Figure 3.8.5: Example node to be tested for radiation hardness.

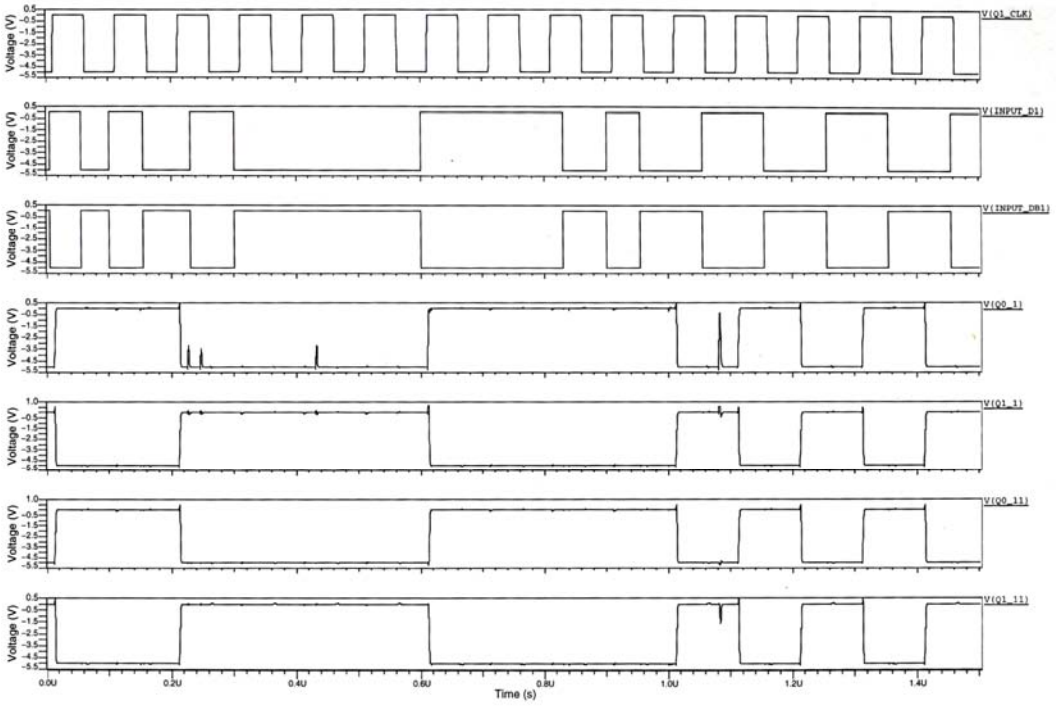

Figure 3.8.6: Results of running a low current barrage test vector on node SB1 in Figure 3.8.5.

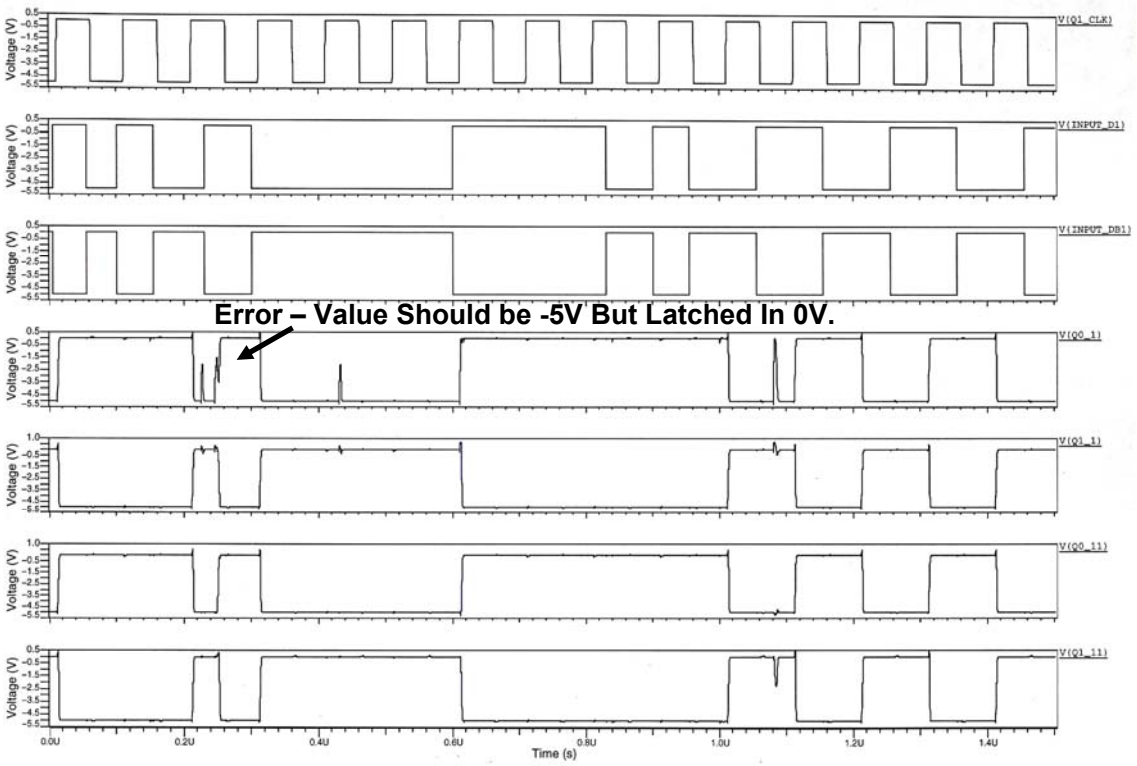

Figure 3.8.7: Results of running a high current barrage test vector on node SB1 in Figure 3.8.5.

3.9 HOW TMRSAFF COUNTERS TID EFFECTS

It has long since been shown that negative biases used on the gates of MOSFET's reduces the negative shift of threshold voltages and can help to reduce leakage current in NMOS devices that develops as a result of irradiation. This is so because the migration of positive charge to the Si/SiO_2 interface is reduced when a negative bias is applied to the gate of a transistor. This fact is illustrated in Figure 3.9.1 which shows how due to positive bias applied to a conductor, positive charge is encouraged to migrate to the Si/SiO_2 interface. In contrast, the application of a negative bias to the conductor in Figure 3.9.1 will encourage positive charge to migrate away from the Si/SiO_2 interface and in doing so break up shorting paths. Depending on how long negative bias is applied to the conductor in Figure 3.9.1 it may be possible to partially anneal the oxide by virtue of

some of the positive charge in the oxide tunneling out of the oxide and into the conductor.

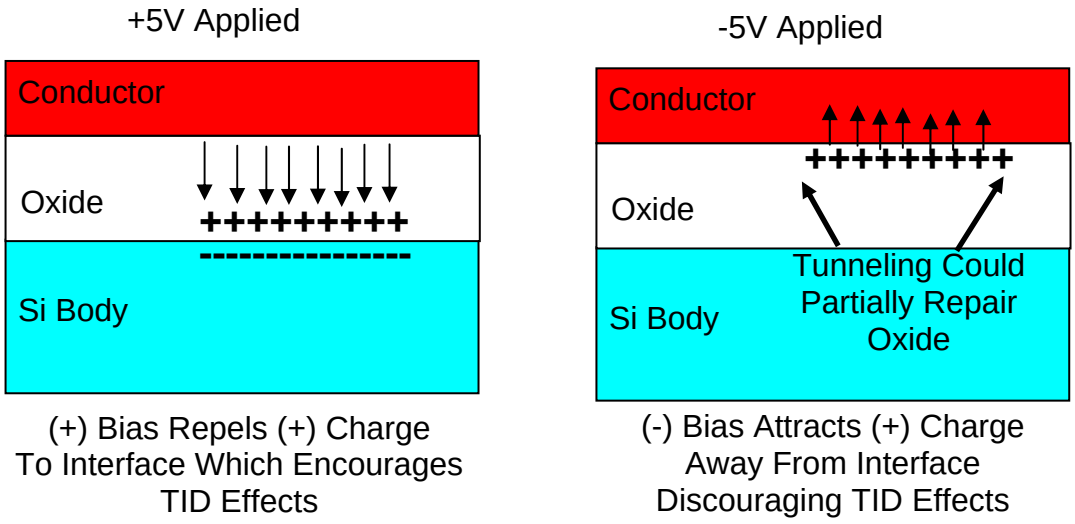

Figure 3.9.1: Effects of using either positive or negative bias in circuits.

Thus, it was decided for purposes of the TMRSAFF design to try one of two approaches:

1) Use a switching arrangement where in a standard (+5V high rail, 0V low rail) system, the +5V supply would be switched off and a multitude of switches used to bring negative voltage on to all nodes which feed at least one transistor gate.
2) Change the voltage used for the design and instead of using +5V as a high rail, use 0V as a high rail and use -5V as a low rail instead of 0V.

It was decided to design the TMRSAFF of this work using a 0V high rail, -5V low rail arrangement. This was not deemed detrimental because the same design would work just as well with a traditional +5V high rail, 0V low rail configuration. In fact, preliminary testing showed that power consumption, switching times and all other parameters were the same regardless. Even latch-up was not a concern using 0V high, -5V low configuration because biasing to prevent latch-up operates on the principle of

relative differences in voltage and not absolute voltage values. Therefore, as long as some maximum voltage value (10V) was not exceeded where breakdown may occur then it was concluded that operation in this somewhat different voltage regime would be feasible. In any event, attempting to do anything such as switching out supply voltages and switching in new voltages regardless of how it was done could lead to self induced breakdown because it would only take the failure of one switch to degrade the operation of the overall TMRSAFF.

3.10 RADIATION HARDENING OPTIONS FOR THE TMRSAFF DESIGN

The TMRSAFF design once completed was modified to incorporate seven distinct options which a designer can use to either further radiation harden their own version of TMRSAFF or improve its power consumption performance. These options are as follows:

OPTION 1: Radiation Hardened Majority Output - The majority logic gate of the TMRSAFF was designed using pass-gate logic in order to increase speed while not adding any diffusions to the output of the upstream input SAFF's. The majority logic gate represents a single point of failure in the TMRSAFF design. This option was created as a counter measure to multiple event upsets (MEU's) which could occur on both majority logic gates and their outputs which feed into the output SAFF's of the TMRSAFF design. The schematic of the radiation hardened majority logic gate is shown in Appendix 13.

OPTION 2: Radiation Hardened Output SAFF – As a general strategy, all SAFF's of the TMRSAFF and their internal circuitry were hardened to the level of a

100MeV Fe ion interaction. However, since the output SAFF of the TMRSAFF connects to downstream loads which may inadvertently turn on or off due to fluctuations in voltage caused by radiation interaction, it was decided to harden the output of the output SAFF's to direct interactions with a 100MeV Fe ion. The schematics of the output SAFF can be seen in Appendix 11. The performance of the design was to limit the magnitude of voltage fluctuation to no more than a 1.6V difference from quiescent for a duration less than 300ps which in tests was shown not to turn on or off any downstream PMOS or NMOS devices which may be connected to the output of the TMRSAFF. A hypothetical version of output SAFF is provided in Appendix 12 which incorporates resistors in the feedback connections of the output latches used in the output SAFF. The addition of these resistors reduces the potential for fluctuations to occur, for example, on the main output as a result of a radiation interaction which occurred on the complementary output of the SAFF. This type of occurrence was named, "radiation induced cross-talk", by the author and is another potential source of voltage fluctuation in the output of the TMRSAFF.

OPTION 3: Comparison Logics – Comparison logics were created to sample the output of the three input SAFF's of the TMRSAFF design. The schematics of the comparison logics developed in this work can be seen in Appendix 14. The comparison logics provide indications when the output of each possible pairing of input SAFF's is different (Q1 and Q2 compared to one

another, Q2 and Q3 compared compared to one another, and Q1 and Q3 compared to one another). For example, if the Q1/Q2 logics indicate that both outputs are the same but the Q2/Q3 logics indicate that both outputs are different then higher order controls can deduce that input SAFF Q3 was different from its counterparts. This can be useful in determining that a particular input SAFF is defective and as such could be switched out with a spare SAFF. The Q1/Q3 comparison logics were provided for redundancy purposes to tell if there was an error which occurred within the comparison logics themselves. Because the TMRSAFF was designed with full redundancy, there was included a redundant set of comparison logics to carry out the same operations on the redundant outputs of the input SAFF's. As such, they provide additional indications which would allow for checking of the validity of indications received.

OPTION 4 Tri-state Buffers on Data and Clock Lines – Tri-state buffering on the clock allows for the complete shutdown of the incoming master clock in the realization of a form of clock gating to reduce power consumption. In addition, when tri-state buffering is used on the master clock connection to the TMRSAFF it reduces the amount of capacitance that the TMRSAFF places on the clock tree. The reason for this is because using a tri-state buffer creates a situation where the incoming clock line only sees the input of an inverter which in the TMRSAF design was a PMOS W = 16, NMOS W = 6 inverter and translates into an equivalent transistor width of 22. This is in sharp contrast to directly connecting the incoming clock to each

of the input SAFF's individually which would equate into a total transistor width of 96. As such, capacitance would be reduced by a factor of greater than four and thus decrease overall system power consumption. Tri-state buffering on the data line also reduces power consumption by reducing the potential for transitions to get in to the TMRSAFF when it is supposed to be shutdown. The greatest strength of this option is the fact that when a tri-state device is utilized and the device is not enabled, its output goes into what is referred to as a high impedance state. This state allows for other devices to be switched on to the line and use the line without interfering with anything upstream of the tri-state device and in turn nothing upstream of the tri-state device could interfere with the new device switched on to the line. In conjunction with an overall system, the potential exists for redundant combinational logic blocks to be switched in to replace defect combinational logic blocks. The same potential exists for the clock where the TMRSAFF could have different clock versions switched in to drive the TMRSAFF either as a damage replacement strategy or as a dynamic operations feature. The tri-state buffers can be seen in Appendices 10 and 15.

OPTION 5: Radiation Hardened Data Lines – Radiation hardened data lines were developed to be resilient up to the level of interaction with a 100MeV Fe ion interaction. This was done as a counter measure to MEU's occurring at the output of the combinational logic which feeds into each of the TMRSAFF's inputs. As such, multiple events which could occur at the

input of the TMRSAFF would have less potential to feed incorrect data into the TMRSAFF. This was deemed especially advantageous when data change is possible right at the transition point of the incoming master clock because this is the time when the passing of incorrect data is most possible. Schematics for this option are provided in Appendix 10.

OPTION 6: Temporal Displacement – Temporal displacement was created as an option for the TMRSAFF design as a counter measure to MEU's in combinational logic. It can be used in conjunction with radiation hardened input data lines or as a stand alone option. The principle of temporal displacement is one of providing each input SAFF of the TMRSAFF with its driving clock signal at a different time from its counterparts. For example, input SAFF Q1 receives its clock at time t = 0s. Input SAFF Q2 then would receive its driving clock signal at approximately time t = 2ns and input SAFF Q3 would receive its driving clock signal at approximately time t = 4ns. This displacement in time allows for static logic to self correct and provide correct inputs to the TMRSAFF in the event of MEU's in combinational logic. As such, the potential exists for correct information to be provided to the TMRSAFF which in turn can be used in the majority logic determination built in to the TMRSAFF to filter out errors which may have been clocked in to the TMRSAFF. The amount of time displacement (approximately 2ns between each input SAFF) emulated the 2ns duration specified by NASA which was mentioned earlier in the text. Schematics for this option are provided in Appendix 15.

OPTION 7: Creation of All Clock Signals Local to the TMRSAFF – It was decided in this option to create all clock signals necessary to drive the TMRSAFF using logic that is actually built into the TMRSAFF itself. This option was created to reduce reliance on outside sources for clocking requirements. It was also provided to allow for the change of one clock which in turn would create equivalent adjustments in all driving downstream clocks which operate the TMRSAFF. For example, if a dynamic change in frequency were employed in an application or some manner of delay was added to the master clock then each of the driving clocks in the TMRSAFF would reflect the change in frequency and or delay automatically since all of the TMRSAFF's driving clock signals were created with appropriate delays from the master clock. Schematics for this option can seen in Appendix 15.

3.11 TRANSISTOR SIZING

The process of producing final transistor sizes in the TMRSAFF design is summarized in Figure 3.11.1. The entire process of sizing transistors was done by hand but the algorithm outlined in Figure 3.11.1 could be automated to create circuits. The first step in actually creating the TMRSAFF was to decide on the sizing rules to be adhered to in the formation of the circuit. In this work, it was decided to emulate the basic construction of an inverter and apply that to the formation of other circuit structures in the TMRSAFF design. In the sizing of the PMOS and NMOS transistors of a basic inverter, one must decide on how to size the NMOS and PMOS transistors of the inverter. In this work, it was decided to take the ratio of the NMOS transistor mobility of the

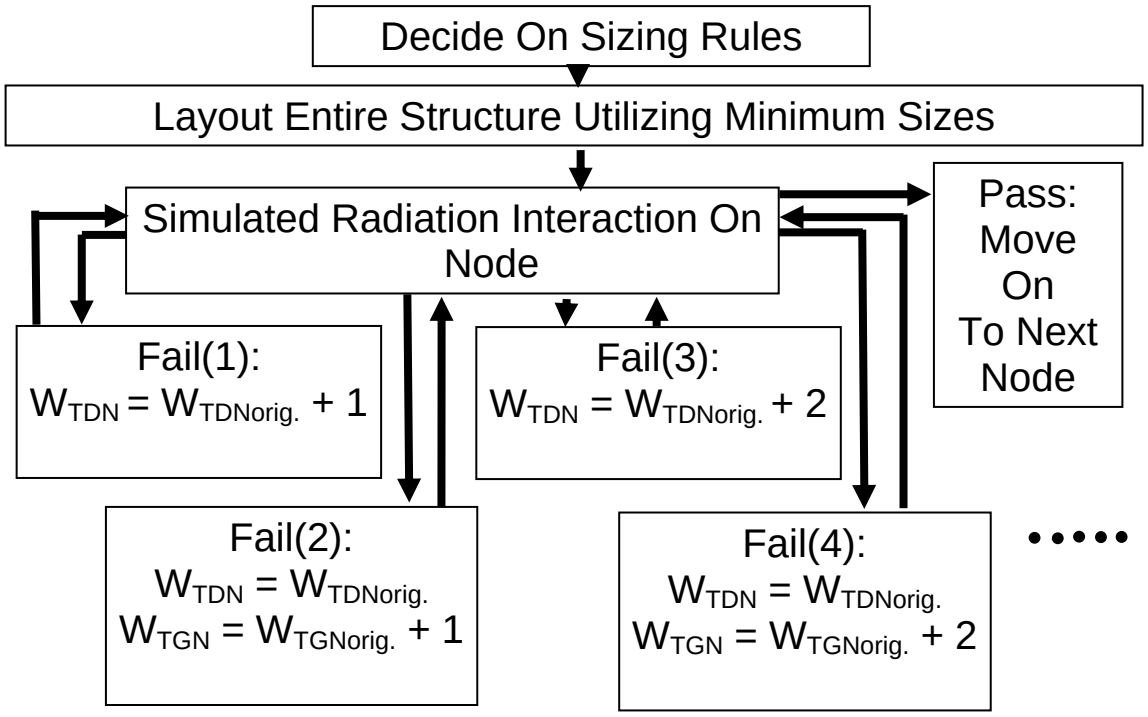

Figure 3.11.1: Flow chart of transistor sizing algorithm.

ami05 transistor family (complete list of ami05 transistor model parameters provided in Appendix 7) to the mobility of the PMOS transistors used in the ami05 transistor family. This was done to reduce power dissipation caused by glitches by producing output voltage waveforms which have approximately equal rise and fall times. The ratio of NMOS mobility to PMOS mobility resulted in a numerical value of 2.63. From there, it was determined that the smallest transistor size that a transsitor layout package would allow without declaring design rule errors was W = 3. So, in the case of a single NMOS device found in the TMRSAFF design, the width would be 3. Multiplying 3 by 2.63 results in a value of 7.89 which was an impractical value to specify for the width of a PMOS transistor and thus the width a single PMOS device would have in the TMRSAFF design would be 8. In situations where two PMOS devices were placed in series, the corresponding widths of the transistors would be increased to 16 in order to maintain an

equivalent transistor width of 8. Similar sizing adjustments were employed with NMOS devices. It was verified in testing for both loaded and unloaded versions of inverters which employed PMOS/NMOS sizing values of 6/3, 7/3, and 8/3 that 8/3 was the best in terms of producing output voltage waveforms which were equal in terms of rise and fall time. After a basic sizing strategy was decided upon, then the entire structure of the TMRSAFF design was laid out utilizing the smallest values for transistor widths possible. Starting from the output of the TMRSAFF design which was loaded with an 8/3 inverter, radiation simulations were conducted and results observed on graphs produced by the simulation software. If the node failed on the first simulation, then all of the transistors which existed on the node which had diffusions connected to the node would have their widths increased by one and the simulation repeated. This corresponds to the Fail(1) box in Figure 3.11.1 where widths of transistors that have diffusions on the node (W_{TDN}) would be increased by one. Assuming the node passed then the process would proceed on to the next node and start radiation simulations anew. However, if the node failed on the next simulation (Fail(2) in Figure 3.11.1) then the increase in size of the transistors which had diffusions on the node would be taken away and the transistors returned to their original size. Then all of the transistors on the node which had gates on the node would have their widths increased by one (W_{TGN} in Figure 3.11.1 in the the Fail(2) box). At that point, radiation simulations would be repeated and results observed. If the node passed then the process would move on to the next node and start radiation simulations anew. However, if the simulations failed once again (Fail(3) in Figure 3.11.1) then all of the transistors whose gate sizes had been increased in the Fail(2) step of Figure 3.11.1 would have their gates kept at their new values but all of the transistors which have diffusions

on the node would have their diffusions increased by two and simulations repeated. Here again, if the node passed the simulation then the process would proceed on to the next node. However, if the node failed then the transistors which had diffusions on the node would be reduced back to their original values and all of the transistors which had gates on the node would have their widths increased by two (Fail(4) step in Figure 3.11.1) and simulations repeated. This process of gradually increasing transistor widths would be repeated until the node under test finally passed all radiation simulation tests. Once all radiation simulation tests were successfully completed, then adjustments would occur to either PMOS or NMOS devices increasing their widths unitl the basic 8/3 ratio stated earlier was achieved.

IV. RESULTS

4.1 OVERVIEW

This chapter will go over the following material:

1) Performance tabulations on the TMRSAFF utilizing none of the options previously stated as well as all of the options previously stated.
2) Performance tabulations where certain stated options were either employed or not employed in the realization of a TMRSAFF circuit.

4.2 SUMMARY OF TMRSAFF CHARACTERISTICS IN THIS WORK

Table 4.2.1 shows the tabulated performance characteristics of the TMRSAFF design proposed in this work.

Table 4.2.1: Tabulation of TMRSAFF characteristics

	TMRSAFF (No Options)	TMRSAFF (All Options)
CLOCK TO Q DELAY (0 TO 1)	8.3ns	21.3ns
CLOCK TO Q DELAY (1 TO 0)	9ns	21.2ns
SET-UP TIME (0 TO 1)	-10ns	-2ns
SET-UP TIME (1 TO 0)	-10ns	-2ns
HOLD TIME (0 TO 1)	1.4ns	6.95ns
HOLD TIME (1 TO 0)	1.4ns	6.95ns
POWER DISSIPATION	9.42nW	173nW

The table provides values on the TMRSAFF clock to Q delay, set-up time, hold time, and power dissipation in the case where none of the previously mentioned options were employed (establishing a low performance bound) as well as when all of the previously stated options were utilized (establishing a worst case upper performance

bound). The values were determined while running the basic functionality test vector (D input) on all of the inputs of the TMRSAFF.

4.3 PERFORMANCE DIFFERENCE FOR DIFFERENT OPTION USAGE

This section is provided to give the end user data on the power consumption and clock to Q delay in several TMRSAFF configurations. The manner in which this was done was to take the TMRSAFF design of this work with its full complement of options and run the basic functionality test vector on the TMRSAFF. This established a baseline for both clock to Q delay and power consumption. Then one option as outlined in tables 4.3.1-4.3.6 was taken out of the TMRSAFF design and the basic functionality test vector was run and new values for clock to Q delay and power consumption were acquired. Additional tests were run for the instance where the TMRSAFF design had all options removed except for full redundancy and comparison logics, Table 4.3.6. In removing each option listed previously, it allowed modification of the overall TMRSAFF design. In the case of eliminating radiation hardened majority logic gates, it allowed the removal of seven of the nine buffers used to derive Q1_CLKOUT which drives the output SAFF's of the TMRSAFF design. Elimination of the radiation hardened data input lines allowed for the elimination of three of the nine buffers used to derive Q1_CLKOUT. Removal of the temporal displacement and clock enabling options allowed for the removal of the input clock buffer and the buffers used to delay the incoming clock to produce the temporal displacement of the TMRSAFF. As a result, the incoming clock signal fed directly into the input SAFF's of the TMRSAFF and then the same nine buffers used to delay and create Q1_CLKOUT were still utilized to create Q1_CLKOUT. Because temporal displacement was eliminated, the resistors used

in the comparison logics were removed and the inverters used in the outputs of the comparison logics were reduced to 8/3 inverters because there was no difference in the arrival of outputs from each input SAFF. This adjustment was deemed feasible in light of the fact that a redundant set of comparison logics was created with the TMRSAFF design. The removal of the comparison logic resistors and the reduction of the output inverters had the added advantage of decreasing the amount of time it took for the comparison logics to determine that two flip-flop outputs were different from a 6-7ns timeframe down to 800ps. In addition, the amount of time it took for the comparison logics to determine that two flip-flop outputs were the same decreased from 4.5-6ns down to 1.6ns. Switching the voltage regime of the circuit from the 0V (high)/-5V (low) rail system used in this work to a +5V (high)/0V (low) had no effect on either speed or power consumption of the TMRSAFF. The option of deriving all flip-flop clocks onboard the TMRSAFF was not eliminated (not entirely) as it was deemed better by the author to derive the Q1_CLKOUT signal onboard the TMRSAFF at all times.

Table 4.3.1: Tabulation of TMRSAFF design performance as a result of eliminating radiation hardened majority logic gates

CLOCK TO Q DELAY (0 TO 1)	CLOCK TO Q DELAY (1 TO 0)	POWER DISSIPATION	SPEED-UP (0 TO 1)	SPEED-UP (1 TO 0)	POWER CONSUMPTION REDUCTION
14.3ns	14.7ns	71.9805nW	32.86%	30.66%	58.5%

Table 4.3.2: Tabulation of TMRSAFF design performance as a result of eliminating radiation hardened data input lines and data enabling

CLOCK TO Q DELAY (0 TO 1)	CLOCK TO Q DELAY (1 TO 0)	POWER DISSIPATION	SPEED-UP (0 TO 1)	SPEED-UP (1 TO 0)	POWER CONSUMPTION REDUCTION
18ns	17.9ns	42.7308nW	15.49%	15.566%	75.36%

Table 4.3.3: Tabulation of TMRSAFF design performance as a result of not using full redundancy

CLOCK TO Q DELAY (0 TO 1)	CLOCK TO Q DELAY (1 TO 0)	POWER DISSIPATION	SPEED-UP (0 TO 1)	SPEED-UP (1 TO 0)	POWER CONSUMPTION REDUCTION
19.7ns	19.7ns	70.9203nW	7.51%	7.51%	59.11%

Table 4.3.4: Tabulation of TMRSAFF design performance as a result of eliminating temporal displacement and clock enabling

CLOCK TO Q DELAY (0 TO 1)	CLOCK TO Q DELAY (1 TO 0)	POWER DISSIPATION	SPEED-UP (0 TO 1)	SPEED-UP (1 TO 0)	POWER CONSUMPTION REDUCTION
13.5ns	13.5ns	66.8153nW	36.62%	36.32%	61.48%

Table 4.3.5: Tabulation of TMRSAFF design performance as a result of eliminating both sets of redundant comparison logics

CLOCK TO Q DELAY (0 TO 1)	CLOCK TO Q DELAY (1 TO 0)	POWER DISSIPATION	SPEED-UP (0 TO 1)	SPEED-UP (1 TO 0)	POWER CONSUMPTION REDUCTION
19.7ns	19.7ns	65.7743nW	7.51%	7.07%	62.08%

Table 4.3.6: Tabulation of TMRSAFF design performance as a result of eliminating all options except for full redundancy and comparison logics

CLOCK TO Q DELAY (0 TO 1)	CLOCK TO Q DELAY (1 TO 0)	POWER DISSIPATION	SPEED-UP (0 TO 1)	SPEED-UP (1 TO 0)	POWER CONSUMPTION REDUCTION
9.7ns	9.2ns	15.3848nW	54.46%	56.6%	91.1%

V. CONCLUSIONS

5.1 OVERVIEW

This chapter will go over the following material:

1) A basic conclusion statement.
2) Applications.
3) Future Studies.

5.2 CONCLUSION STATEMENT

The TMRSAFF design proposed in this work was successfully designed and characterized with no known defects or problems to report. The overall TMRSAFF design:

1) Had a plethora of options created to provide to designers greater flexibility in realizing their own radiation hardened versions of TMRSAFF.
2) Was verified for proper functionality as a flip-flop in all possible configurations considered in this work.
3) Was characterized for performance parameters in a variety of configurations ranging from a basic TMRSAFF design utilizing no radiation hardening options all the way to a TMRSAFF design utilizing all radiation hardening options formulated in this work.
4) Was verified for radiation hardness up to the prescribed level equivalent to a 100MeV Fe ion interaction with all of the circuits nodes.

5.3 APPLICATIONS

TMR designs at the present time are not recommended for low radiation environments. This is so because the redundancy built into a TMR design is unnecessary

where upsets due to radiation do not prevail. The reason for this is that in low radiation environments such as the terrestrial environment the use of current technology sizes (above 100nm) for the most part delivers reliable performance. As such, the use of Si area to produce a TMR design would be inefficient. This does not mean, however, that as technology sizes go into the sub-micron range (< 100nm) that low radiation environments such as the terrestrial environment could not benefit from the design of TMR devices like the TMRSAFF of this work to improve device reliability. Indeed, as technology sizes proceed down below 90nm (which is currently in full use in the industry today) what were once radiation resistant applications may become error prone like their space counterparts.

This is because of the reduced charge storage of nodes which will not only allow high energy delivery particles to upset nodes but will also allow low energy particles the opportunity to impart enough energy to upset nodes.

Given all of this the author envisions that there are three basic functions which a flip-flop of any kind can fulfill as follows:

1) Memory storage of individual bits.
2) Memory storage of bytes, words, and double words in registers.
3) Formation of pipelined digital devices.

The first function is impractical to implement in large scale using TMR designs. The second and third functions are better suited to the investment in Si area put in to creating a TMR design. Since most RISC processors have reasonable numbers of registers (32 or less and generally is the processor type of choice in most space applications), one could very much make use of TMR designs like the TMRSAFF where

the use of Si area is offset by the increased reliability of the device. As for pipelining, the author envisions practical space microprocessors utilizing anywhere from two to five pipeline stages at a maximum if any pipelining is utilized at all. This would tend to reduce power consumption due to glitches and reduce the distance that an error could propagate while at the same time not consuming too much Si area. The limit of two to five comes from the fact that TMR designs such as the TMRSAFF tend to consume large amounts of Si area and modern processor designs which utilize 20+ pipeline stages would in fact become impractical to implement using TMR designs. This would be due to the large amount of Si area that would be necessary to create large numbers of TMR flip-flops along with the fact that having too many radiation hardened devices in a circuit would tend to diminish speed and increase power dissipation.

In situations where all or most of the TMRSAFF's options are built in to the end product, it is best to utilize the TMRSAFF for both data registers and/or as an output register for an overall TMR device. In the case of an overall TMR device, three copies of combinational logic (perhaps three identical copies of a microprocessor) could each feed into one of the three inputs of a TMRSAFF output register. As such, the TMRSAFF could reliably pass information from the TMR processor described to the system which it serves while at the same time serving as a barrier against the propagation of either glitches or errors into downstream circuit components. This type of TMR computer realization is quite common in space applications and would make the TMRSAFF design an ideal candidate to utilize in such capacities.

5.4 FUTURE WORK

Future work which can follow directly from this work is best understood by

looking at figures 5.4.1-5.4.4. Figure 5.4.1 shows the formation of what the author refers to as Sensor and Integrated Circuit (S&IC) technology for future applications which would enable designs like the TMRSAFF to become self-sensing and self-correcting versions of themselves.

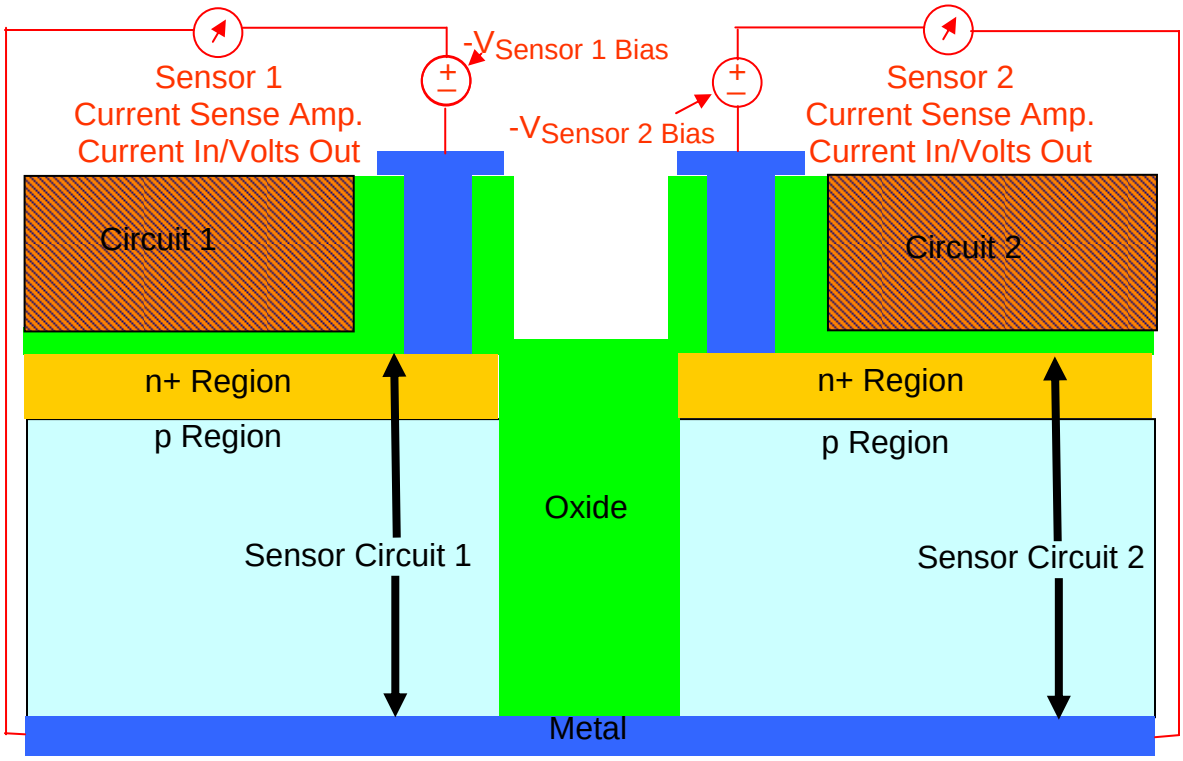

Figure 5.4.1: Final S&IC technology formation.

S&IC technology as shown in Figure 5.4.1 would employ independent n+/p diodes formed directly under each section of a circuit for which radiation interaction is important to sense (circuit 1 and circuit 2 in Figure 5.4.1). The top layer of Si in which circuits 1 and 2 are located, could be made as thin as that utilized for partially depleted silicon on insulator (PDSOI) or fully depleted silicon on insulator (FDSOI) which are both inherently more radiation hardened than their bulk-Si technology counterparts because of the fact that there is less Si in which EHP's can be formed. The separating

layer of oxide underneath of circuit 1 and circuit 2 would effectively breakup funnel formation and the potential such a phenomenon has in creating upsets. The use of the negative bias arrangement is utilized to draw positive charge down and away from circuits 1 and 2 and which is a methodology known to increase the radiation hardness of silicon on insulator (SOI) technology. The n+/p diode shown in Figure 5.4.1 is one possible realization of the overall S&IC technology which may reduce system power consumption by not allowing current to flow while no radiation interaction is occurring because the bias shown in Figure 5.4.1 reverse biases the diode. However, should a radiation event occur then what causes upsets in circuit information could be taken advantage of in building a sensing scheme where the generation of EHP's in the Si sensor portion of Figure 5.4.1 would under the influence of an external bias encourage current to flow. This current then could flow through an appropriate circuit element (the current sense amplifier shown in Figure 5.4.1) and convert the current flow to a voltage signal which would provide indication that radiation had just passed through the sensor. By keeping the top circuit layer in Figure 5.4.1 as thin as possible, it would make fabrication more practical while reducing the overall target size (circuit 1 and circuit 2 in Figure 5.4.1). This would also reduce the potential for radiation to miss the sensor while still interacting with the circuit that the sensor was designed to protect in Figure 5.4.1. This is why the sensor must be created with dimensions that are somewhat larger in planar area than the circuit being sensed so that extremely shallow angle radiation events will not miss the sensor entirely while interacting with the circuit. Extensive work could be conducted to come up with optimum sensor sizing, sensor and top circuit thickness, separating oxide thickness, and biasing voltage to produce reliable sensing while at the

same time not causing unnecessary power dissipation. The reason why this type of arrangement is seen as superior is because of the fact that radiation sensing of this nature is mainly currently conducted with sensors which are built into the packaging of a chip. This type of arrangement does not necessarily ensure accurate indication of an interaction with a portion of a chip which is deemed critical to circuit operation. This is so because it is not unusual for large amounts of chip area to not be utilized and radiation passing through a package may pass though an unoccupied portion of the chip and in any event does not necessarily mean that information on the chip is possibly of an erroneous nature. Therefore, by moving the sensors to a point where they are virtually one and the same with the portions of a circuit for which sensing is vital then this would allow for the creation of self-sensing and self-correcting designs which could revolutionize the manner in which work of this nature is done. Figure 5.4.2 shows at least one potential for joining what the author refers to as S&IC technology with the TMRSAFF design and in doing so create a self-sensing circuit. Figure 5.4.2 is a block diagram of a no options included TMRSAFF design where sensors are constructed under the single points of failure represented by each of the output paths created by MAJ. OUT1/OUTPUT SAFF 1 and MAJ. OUT 2/OUTPUT SAFF 2. In this example, future work could create an intelligent switching scheme which in Figure 5.4.2 is currently selected to TMRSAFF output 1 for passing information out of the flip-flop. Then as shown in Figure 5.4.3 if a radiation interaction event should occur with output path 1 which could call into question the accuracy of information contained there then the intelligent switching scheme alluded to earlier could take inputs from both sensors shown in Figure 5.4.3 and decide to switch from TMRSAFF output 1 to TMRSAFF output 2 and in doing so create a self-correcting

TMRSAFF. This type of methodology could be valuable in maintaining overall system throughput because it is not unusual for power cycling or the re-running of information through a system as a means of radiation hardening when a radiation interaction event occurs because the resulting self-sensing/self-correcting TMRSAFF could dynamically switch to its alternate output.

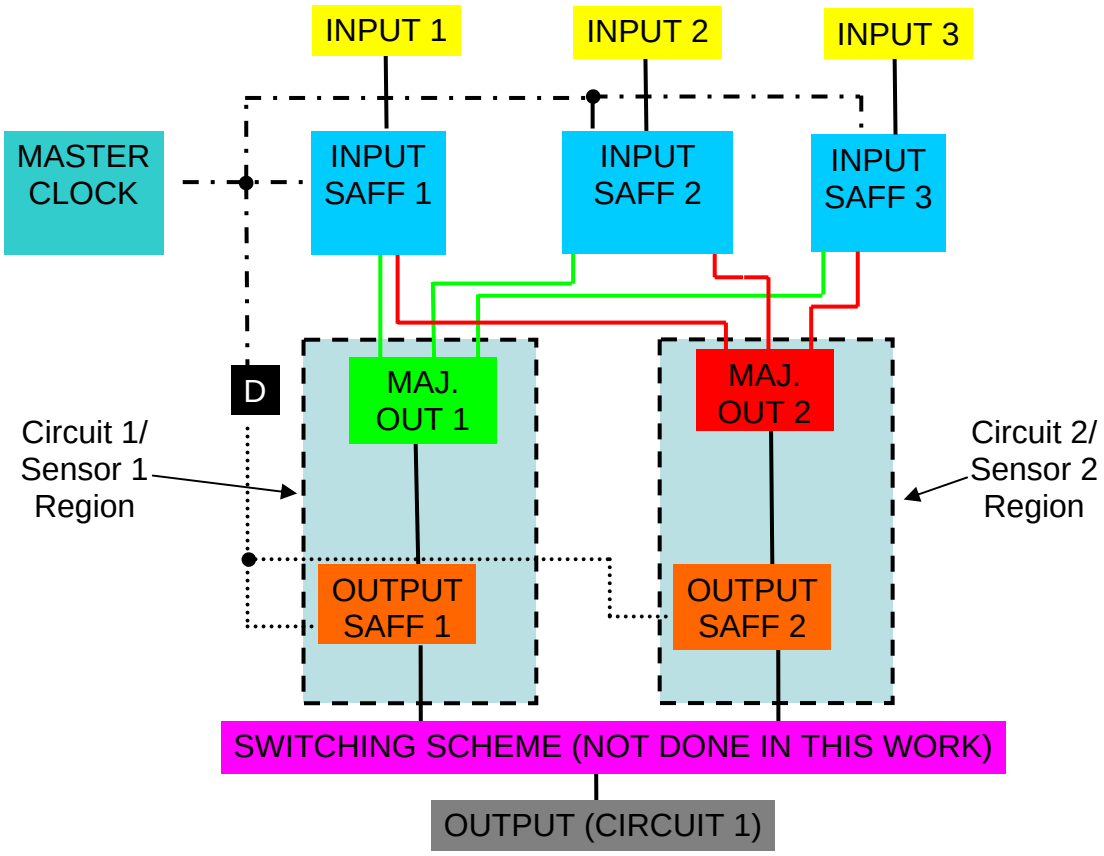

Figure 5.4.2: Depiction of S&IC technology with TMRSAFF.

The availability of an alternate output like that supplied by the TMRSAFF allows for a form of self-repair as shown in Figure 5.4.4. In Figure 5.4.4, test vectors whose outputs are known could be run on the TMRSAFF and as a result it could be determined that output path 1 of a TMRSAFF is permanently faulty. With an appropriate switching scheme then the overall output of the TMRSAFF could be switched

permanently from output path 1 to output path 2.

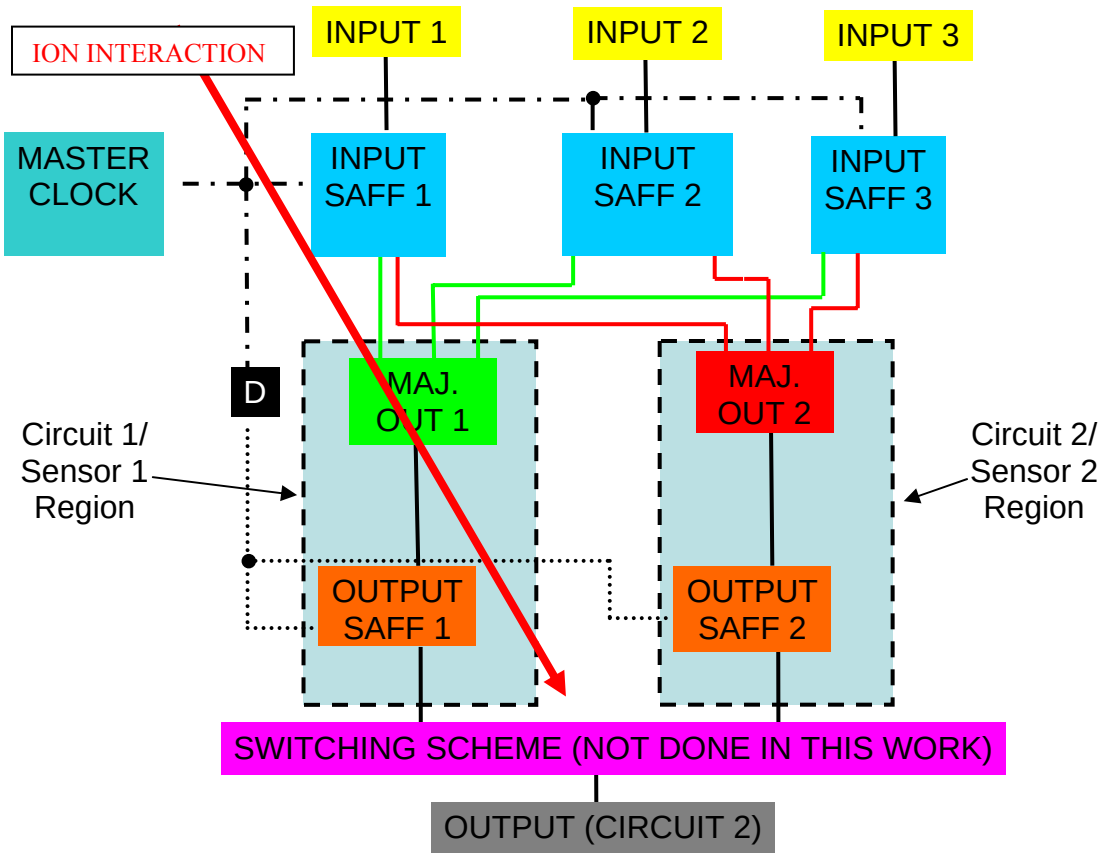

Figure 5.4.3: Depiction of TMRSAFF and S&IC technology after ion interaction.

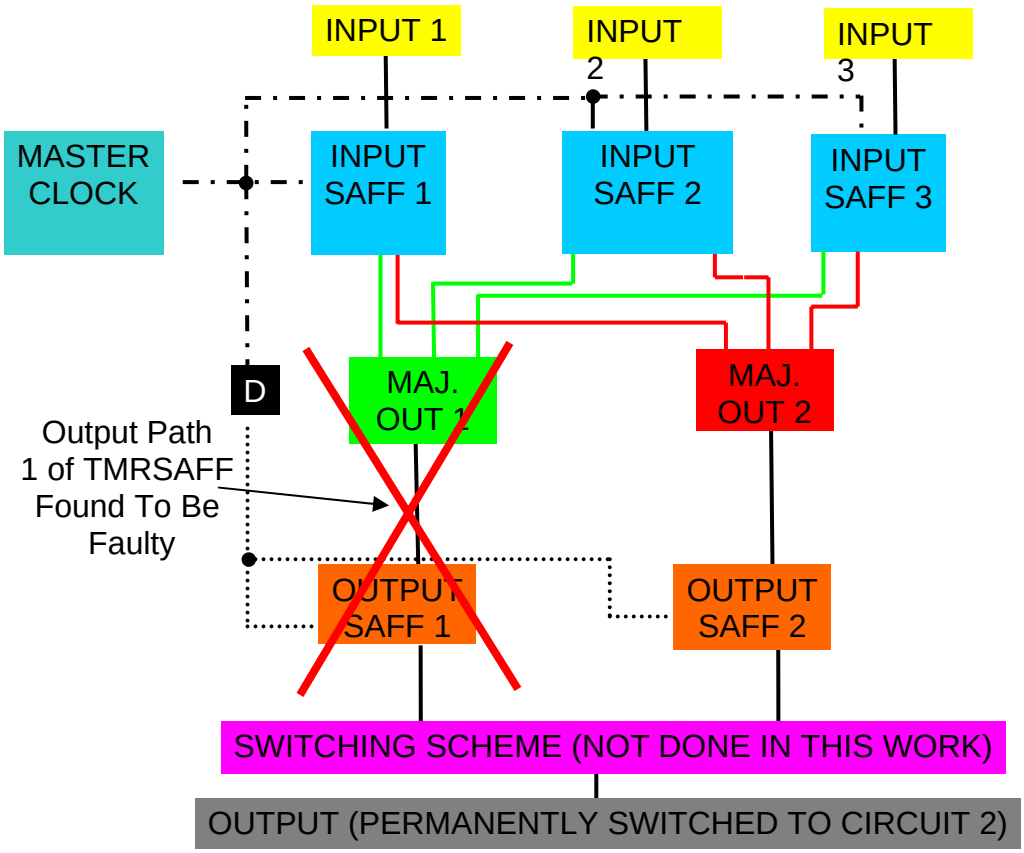

Figure 5.4.4: Self-repairing version of TMRSAFF.

APPENDIX 1: BASIC FUNCTIONALITY TEST VECTOR (D INPUT)

(NOTE: This is used to input into the "D" input of a SAFF. The format of the information that follows is a space delineated listing of time and magnitude of voltage to be applied at the stated time.

EXAMPLE: 5e-9 -5 means at 5ns apply -5V)

0e-9 -5
5e-9 -5
5.1e-9 0
55e-9 0
55.1e-9 -5
100e-9 -5
100.1e-9 0
155e-9 0
155.1e-9 -5
200e-9 -5
230e-9 -5
230.1e-9 0
300e-9 -5
300.1e-9 -5
600e-9 -5
600.1e-9 0
830e-9 0
830.1e-9 -5
900e-9 -5
900.1e-9 0
955e-9 0
955.1e-9 0
1055e-9 -5
1055.1e-9 0
1155e-9 0
1155.1e-9 -5
1255e-9 -5
1255.1e-9 0
1355e-9 0
1355.1e-9 -5
1455e-9 -5
1455e-9 0
1500e-9 0

APPENDIX 2: BASIC FUNCTIONALITY TEST VECTOR (DB INPUT)

(NOTE: This is used to input into the "DB" input of a SAFF. The format of the information that follows is a space delineated listing of time and magnitude of voltage to be applied at the stated time.

EXAMPLE: 5e-9 0 means at 5ns apply 0V)

0e-9 0
5e-9 0
5.1e-9 -5
55e-9 -5
55.1e-9 0
100e-9 0
100.1e-9 -5
155e-9 -5
155.1e-9 0
200e-9 0
230e-9 0
230.1e-9 -5
300e-9 -5
300.1e-9 0
600e-9 0
600.1e-9 -5
830e-9 -5
830.1e-9 0
900e-9 0
900.1e-9 -5
955e-9 -5
955.1e-9 0
1055e-9 0
1055.1e-9 -5
1155e-9 -5
1155.1e-9 0
1255e-9 0
1255.1e-9 -5
1355e-9 -5
1355.1e-9 0
1455e-9 0
1455e-9 -5
1500e-9 -5

APPENDIX 3: LOW CURRENT BARRAGE TEST VECTOR

(NOTE: This is used to simulate the effects of a 100MeV Fe ion interaction on the n^+/p junction of a MOSFET transistor (5.5mA prompt dose). It is applied as a general current value where current flows from the node applied to whatever the low rail voltage in the circuit is specified to be. The format of the information that follows is a space delineated listing of time and magnitude of current to be applied at the stated time.

EXAMPLE: 150.001e-9 5e-3 means at 150.001ns apply 5.5mA)

0e-9 0
150e-9 0
150.001e-9 5.5e-3
150.1e-9 5.5e-3
150.101e-9 2e-3
150.2e-9 2e-3
150.201e-9 1.81e-3
150.3e-9 1.81e-3
150.301e-9 1.64e-3
150.4e-9 1.64e-3
150.401e-9 1.48e-3
150.5e-9 1.48e-3
150.501e-9 1.34e-3
150.6e-9 1.34e-3
150.601e-9 1.21e-3
150.7e-9 1.21e-3
150.701e-9 1.1e-3
150.8e-9 1.1e-3
150.801e-9 1e-3
150.9e-9 1e-3
150.901e-9 8.94e-4
151e-9 8.94e-4
151.001e-9 8.1e-4
151.1e-9 8.1e-4
151.101e-9 7.3e-4
151.2e-9 7.3e-4
151.201e-9 6.7e-4
151.3e-9 6.7e-4
151.301e-9 6e-4
151.4e-9 6e-4
151.401e-9 5.4e-4
151.5e-9 5.4e-4
151.501e-9 4.9e-4
151.6e-9 4.9e-4
151.601e-9 4.4e-4
151.7e-9 4.4e-4
151.701e-9 4e-4
151.8e-9 4e-4

151.801e-9 3.65e-4
151.9e-9 3.65e-4
151.901e-9 3.3e-4
152e-9 3.3e-4
152.001e-9 0
224.6e-9 0
224.601e-9 5.5e-3
224.7e-9 5.5e-3
224.701e-9 2e-3
224.8e-9 2e-3
224.801e-9 1.81e-3
224.9e-9 1.81e-3
224.901e-9 1.64e-3
225e-9 1.64e-3
225.001e-9 1.48e-3
225.1e-9 1.48e-3
225.101e-9 1.34e-3
225.2e-9 1.34e-3
225.201e-9 1.21e-3
225.3e-9 1.21e-3
225.301e-9 1.1e-3
225.4e-9 1.1e-3
225.401e-9 1e-3
225.5e-9 1e-3
225.501e-9 8.94e-4
225.6e-9 8.94e-4
225.601e-9 8.1e-4
225.7e-9 8.1e-4
225.701e-9 7.3e-4
225.8e-9 7.3e-4
225.801e-9 6.7e-4
225.9e-9 6.7e-4
225.901e-9 6e-4
226e-9 6e-4
226.001e-9 5.4e-4
226.1e-9 5.4e-4
226.101e-9 4.9e-4
226.2e-9 4.9e-4
226.201e-9 4.4e-4
226.3e-9 4.4e-4
226.301e-9 4e-4
226.4e-9 4e-4
226.401e-9 3.65e-4
226.5e-9 3.65e-4
226.501e-9 3.3e-4
226.6e-9 3.3e-4

226.601e-9 0
245e-9 0
245.001e-9 5.5e-3
245.1e-9 5.5e-3
245.101e-9 2e-3
245.2e-9 2e-3
245.201e-9 1.81e-3
245.3e-9 1.81e-3
245.301e-9 1.64e-3
245.4e-9 1.64e-3
245.401e-9 1.48e-3
245.5e-9 1.48e-3
245.501e-9 1.34e-3
245.6e-9 1.34e-3
245.601e-9 1.21e-3
245.7e-9 1.21e-3
245.701e-9 1.1e-3
245.8e-9 1.1e-3
245.801e-9 1e-3
245.9e-9 1e-3
245.901e-9 8.94e-4
246e-9 8.94e-4
246.001e-9 8.1e-4
246.1e-9 8.1e-4
246.101e-9 7.3e-4
246.2e-9 7.3e-4
246.201e-9 6.7e-4
246.3e-9 6.7e-4
246.301e-9 6e-4
246.4e-9 6e-4
246.401e-9 5.4e-4
246.5e-9 5.4e-4
246.501e-9 4.9e-4
246.6e-9 4.9e-4
246.601e-9 4.4e-4
246.7e-9 4.4e-4
246.701e-9 4e-4
246.8e-9 4e-4
246.801e-9 3.65e-4
246.9e-9 3.65e-4
246.901e-9 3.3e-4
247e-9 3.3e-4
247.001e-9 0
430e-9 0
430.001e-9 5.5e-3
430.1e-9 5.5e-3

430.101e-9 2e-3
430.2e-9 2e-3
430.201e-9 1.81e-3
430.3e-9 1.81e-3
430.301e-9 1.64e-3
430.4e-9 1.64e-3
430.401e-9 1.48e-3
430.5e-9 1.48e-3
430.501e-9 1.34e-3
430.6e-9 1.34e-3
430.601e-9 1.21e-3
430.7e-9 1.21e-3
430.701e-9 1.1e-3
430.8e-9 1.1e-3
430.801e-9 1e-3
430.9e-9 1e-3
430.901e-9 8.94e-4
431e-9 8.94e-4
431.001e-9 8.1e-4
431.1e-9 8.1e-4
431.101e-9 7.3e-4
431.2e-9 7.3e-4
431.201e-9 6.7e-4
431.3e-9 6.7e-4
431.301e-9 6e-4
431.4e-9 6e-4
431.401e-9 5.4e-4
431.5e-9 5.4e-4
431.501e-9 4.9e-4
431.6e-9 4.9e-4
431.601e-9 4.4e-4
431.7e-9 4.4e-4
431.701e-9 4e-4
431.8e-9 4e-4
431.801e-9 3.65e-4
431.9e-9 3.65e-4
431.901e-9 3.3e-4
432e-9 3.3e-4
432.001e-9 0
609.8e-9 0
609.801e-9 5.5e-3
609.9e-9 5.5e-3
609.901e-9 2e-3
610e-9 2e-3
610.001e-9 1.81e-3
610.1e-9 1.81e-3

610.101e-9 1.64e-3
610.2e-9 1.64e-3
610.201e-9 1.48e-3
610.3e-9 1.48e-3
610.301e-9 1.34e-3
610.4e-9 1.34e-3
610.401e-9 1.21e-3
610.5e-9 1.21e-3
610.501e-9 1.1e-3
610.6e-9 1.1e-3
610.601e-9 1e-3
610.7e-9 1e-3
610.701e-9 8.94e-4
610.8e-9 8.94e-4
610.801e-9 8.1e-4
610.9e-9 8.1e-4
610.901e-9 7.3e-4
611e-9 7.3e-4
611.001e-9 6.7e-4
611.1e-9 6.7e-4
611.101e-9 6e-4
611.2e-9 6e-4
611.201e-9 5.4e-4
611.3e-9 5.4e-4
611.301e-9 4.9e-4
611.4e-9 4.9e-4
611.401e-9 4.4e-4
611.5e-9 4.4e-4
611.501e-9 4e-4
611.6e-9 4e-4
611.601e-9 3.65e-4
611.7e-9 3.65e-4
611.701e-9 3.3e-4
611.8e-9 3.3e-4
611.801e-9 0
616.5e-9 0
616.501e-9 5.5e-3
616.6e-9 5.5e-3
616.601e-9 2e-3
616.7e-9 2e-3
616.701e-9 1.81e-3
616.8e-9 1.81e-3
616.801e-9 1.64e-3
616.9e-9 1.64e-3
616.901e-9 1.48e-3
617e-9 1.48e-3

617.001e-9 1.34e-3
617.1e-9 1.34e-3
617.101e-9 1.21e-3
617.2e-9 1.21e-3
617.201e-9 1.1e-3
617.3e-9 1.1e-3
617.301e-9 1e-3
617.4e-9 1e-3
617.401e-9 8.94e-4
617.5e-9 8.94e-4
617.501e-9 8.1e-4
617.6e-9 8.1e-4
617.601e-9 7.3e-4
617.7e-9 7.3e-4
617.701e-9 6.7e-4
617.8e-9 6.7e-4
617.801e-9 6e-4
617.9e-9 6e-4
617.901e-9 5.4e-4
618e-9 5.4e-4
618.001e-9 4.9e-4
618.1e-9 4.9e-4
618.101e-9 4.4e-4
618.2e-9 4.4e-4
618.201e-9 4e-4
618.3e-9 4e-4
618.301e-9 3.65e-4
618.4e-9 3.65e-4
618.401e-9 3.3e-4
618.5e-9 3.3e-4
618.501e-9 0
839e-9 0
839.001e-9 5.5e-3
839.1e-9 5.5e-3
839.101e-9 2e-3
839.2e-9 2e-3
839.201e-9 1.81e-3
839.3e-9 1.81e-3
839.301e-9 1.64e-3
839.4e-9 1.64e-3
839.401e-9 1.48e-3
839.5e-9 1.48e-3
839.501e-9 1.34e-3
839.6e-9 1.34e-3
839.601e-9 1.21e-3
839.7e-9 1.21e-3

839.701e-9 1.1e-3
839.8e-9 1.1e-3
839.801e-9 1e-3
839.9e-9 1e-3
839.901e-9 8.94e-4
840e-9 8.94e-4
840.001e-9 8.1e-4
840.1e-9 8.1e-4
840.101e-9 7.3e-4
840.2e-9 7.3e-4
840.201e-9 6.7e-4
840.3e-9 6.7e-4
840.301e-9 6e-4
840.4e-9 6e-4
840.401e-9 5.4e-4
840.5e-9 5.4e-4
840.501e-9 4.9e-4
840.6e-9 4.9e-4
840.601e-9 4.4e-4
840.7e-9 4.4e-4
840.701e-9 4e-4
840.8e-9 4e-4
840.801e-9 3.65e-4
840.9e-9 3.65e-4
840.901e-9 3.3e-4
841e-9 3.3e-4
841.001e-9 0
1000e-9 0
1000.001e-9 5.5e-3
1000.1e-9 5.5e-3
1000.101e-9 2e-3
1000.2e-9 2e-3
1000.201e-9 1.81e-3
1000.3e-9 1.81e-3
1000.301e-9 1.64e-3
1000.4e-9 1.64e-3
1000.401e-9 1.48e-3
1000.5e-9 1.48e-3
1000.501e-9 1.34e-3
1000.6e-9 1.34e-3
1000.601e-9 1.21e-3
1000.7e-9 1.21e-3
1000.701e-9 1.1e-3
1000.8e-9 1.1e-3
1000.801e-9 1e-3
1000.9e-9 1e-3

1000.901e-9 8.94e-4
1001e-9 8.94e-4
1001.001e-9 8.1e-4
1001.1e-9 8.1e-4
1001.101e-9 7.3e-4
1001.2e-9 7.3e-4
1001.201e-9 6.7e-4
1001.3e-9 6.7e-4
1001.301e-9 6e-4
1001.4e-9 6e-4
1001.401e-9 5.4e-4
1001.5e-9 5.4e-4
1001.501e-9 4.9e-4
1001.6e-9 4.9e-4
1001.601e-9 4.4e-4
1001.7e-9 4.4e-4
1001.701e-9 4e-4
1001.8e-9 4e-4
1001.801e-9 3.65e-4
1001.9e-9 3.65e-4
1001.901e-9 3.3e-4
1002e-9 3.3e-4
1002.001e-9 0
1080e-9 0
1080.001e-9 5.5e-3
1080.1e-9 5.5e-3
1080.101e-9 2e-3
1080.2e-9 2e-3
1080.201e-9 1.81e-3
1080.3e-9 1.81e-3
1080.301e-9 1.64e-3
1080.4e-9 1.64e-3
1080.401e-9 1.48e-3
1080.5e-9 1.48e-3
1080.501e-9 1.34e-3
1080.6e-9 1.34e-3
1080.601e-9 1.21e-3
1080.7e-9 1.21e-3
1080.701e-9 1.1e-3
1080.8e-9 1.1e-3
1080.801e-9 1e-3
1080.9e-9 1e-3
1080.901e-9 8.94e-4
1081e-9 8.94e-4
1081.001e-9 8.1e-4
1081.1e-9 8.1e-4

1081.101e-9 7.3e-4
1081.2e-9 7.3e-4
1081.201e-9 6.7e-4
1081.3e-9 6.7e-4
1081.301e-9 6e-4
1081.4e-9 6e-4
1081.401e-9 5.4e-4
1081.5e-9 5.4e-4
1081.501e-9 4.9e-4
1081.6e-9 4.9e-4
1081.601e-9 4.4e-4
1081.7e-9 4.4e-4
1081.701e-9 4e-4
1081.8e-9 4e-4
1081.801e-9 3.65e-4
1081.9e-9 3.65e-4
1081.901e-9 3.3e-4
1082e-9 3.3e-4
1082.001e-9 0
1500e-9 0

APPENDIX 4: HIGH CURRENT BARRAGE TEST VECTOR

(NOTE: This is used to simulate the effects of an ion interaction on the n^+/p junction of a MOSFET transistor (6.0mA prompt dose) which is greater than the lower current barrage defined in Appendix 3. It is applied as a general current value where current flows from the node applied to the low rail voltage in the circuit. The format of the information that follows is a space delineated listing of time and magnitude of current to be applied at the stated time.

EXAMPLE: 150.001e-9 5e-3 means at 150.001ns apply 5.5mA)

0e-9 0
150e-9 0
150.001e-9 6.0e-3
150.1e-9 6.0e-3
150.101e-9 2.5e-3
150.2e-9 2.5e-3
150.201e-9 2.31e-3
150.3e-9 2.31e-3
150.301e-9 2.14e-3
150.4e-9 2.14e-3
150.401e-9 1.98e-3
150.5e-9 1.98e-3
150.501e-9 1.84e-3
150.6e-9 1.84e-3
150.601e-9 1.71e-3
150.7e-9 1.71e-3
150.701e-9 1.6e-3
150.8e-9 1.6e-3
150.801e-9 1.5e-3
150.9e-9 1.5e-3
150.901e-9 1.39e-3
151e-9 1.39e-3
151.001e-9 1.31e-3
151.1e-9 1.31e-3
151.101e-9 1.23e-3
151.2e-9 1.23e-3
151.201e-9 1.17e-3
151.3e-9 1.17e-3
151.301e-9 1.1e-3
151.4e-9 1.1e-3
151.401e-9 1.04e-3
151.5e-9 1.04e-3
151.501e-9 9.9e-4
151.6e-9 9.9e-4
151.601e-9 9.4e-4
151.7e-9 9.4e-4
151.701e-9 9e-4

151.8e-9 9e-4
151.801e-9 8.65e-4
151.9e-9 8.65e-4
151.901e-9 8.3e-4
152e-9 8.3e-4
152.001e-9 0
224.6e-9 0
224.601e-9 6.0e-3
224.7e-9 6.0e-3
224.701e-9 2.5e-3
224.8e-9 2.5e-3
224.801e-9 2.31e-3
224.9e-9 2.31e-3
224.901e-9 2.14e-3
225e-9 2.14e-3
225.001e-9 1.98e-3
225.1e-9 1.98e-3
225.101e-9 1.84e-3
225.2e-9 1.84e-3
225.201e-9 1.71e-3
225.3e-9 1.71e-3
225.301e-9 1.6e-3
225.4e-9 1.6e-3
225.401e-9 1.5e-3
225.5e-9 1.5e-3
225.501e-9 1.39e-3
225.6e-9 1.39e-3
225.601e-9 1.31e-3
225.7e-9 1.31e-3
225.701e-9 1.23e-3
225.8e-9 1.23e-3
225.801e-9 1.17e-3
225.9e-9 1.17e-3
225.901e-9 1.1e-3
226e-9 1.1e-3
226.001e-9 1.04e-3
226.1e-9 1.04e-3
226.101e-9 9.9e-4
226.2e-9 9.9e-4
226.201e-9 9.4e-4
226.3e-9 9.4e-4
226.301e-9 9e-4
226.4e-9 9e-4
226.401e-9 8.65e-4
226.5e-9 8.65e-4
226.501e-9 8.3e-4

226.6e-9 8.3e-4
226.601e-9 0
245e-9 0
245.001e-9 6.0e-3
245.1e-9 6.0e-3
245.101e-9 2.5e-3
245.2e-9 2.5e-3
245.201e-9 2.31e-3
245.3e-9 2.31e-3
245.301e-9 2.14e-3
245.4e-9 2.14e-3
245.401e-9 1.98e-3
245.5e-9 1.98e-3
245.501e-9 1.84e-3
245.6e-9 1.84e-3
245.601e-9 1.71e-3
245.7e-9 1.71e-3
245.701e-9 1.6e-3
245.8e-9 1.6e-3
245.801e-9 1.5e-3
245.9e-9 1.5e-3
245.901e-9 1.39e-3
246e-9 1.39e-3
246.001e-9 1.31e-3
246.1e-9 1.31e-3
246.101e-9 1.23e-3
246.2e-9 1.23e-3
246.201e-9 1.17e-3
246.3e-9 1.17e-3
246.301e-9 1.1e-3
246.4e-9 1.1e-3
246.401e-9 1.04e-3
246.5e-9 1.04e-3
246.501e-9 9.9e-4
246.6e-9 9.9e-4
246.601e-9 9.4e-4
246.7e-9 9.4e-4
246.701e-9 9e-4
246.8e-9 9e-4
246.801e-9 8.65e-4
246.9e-9 8.65e-4
246.901e-9 8.3e-4
247e-9 8.3e-4
247.001e-9 0
430e-9 0
430.001e-9 6.0e-3

430.1e-9 6.0e-3
430.101e-9 2.5e-3
430.2e-9 2.5e-3
430.201e-9 2.31e-3
430.3e-9 2.31e-3
430.301e-9 2.14e-3
430.4e-9 2.14e-3
430.401e-9 1.98e-3
430.5e-9 1.98e-3
430.501e-9 1.84e-3
430.6e-9 1.84e-3
430.601e-9 1.71e-3
430.7e-9 1.71e-3
430.701e-9 1.6e-3
430.8e-9 1.6e-3
430.801e-9 1.5e-3
430.9e-9 1.5e-3
430.901e-9 1.39e-3
431e-9 1.39e-3
431.001e-9 1.31e-3
431.1e-9 1.31e-3
431.101e-9 1.23e-3
431.2e-9 1.23e-3
431.201e-9 1.17e-3
431.3e-9 1.17e-3
431.301e-9 1.1e-3
431.4e-9 1.1e-3
431.401e-9 1.04e-3
431.5e-9 1.04e-3
431.501e-9 9.9e-4
431.6e-9 9.9e-4
431.601e-9 9.4e-4
431.7e-9 9.4e-4
431.701e-9 9e-4
431.8e-9 9e-4
431.801e-9 8.65e-4
431.9e-9 8.65e-4
431.901e-9 8.3e-4
432e-9 8.3e-4
432.001e-9 0
609.8e-9 0
609.801e-9 6.0e-3
609.9e-9 6.0e-3
609.901e-9 2.5e-3
610e-9 2.5e-3
610.001e-9 2.31e-3

610.1e-9 2.31e-3
610.101e-9 2.14e-3
610.2e-9 2.14e-3
610.201e-9 1.98e-3
610.3e-9 1.98e-3
610.301e-9 1.84e-3
610.4e-9 1.84e-3
610.401e-9 1.71e-3
610.5e-9 1.71e-3
610.501e-9 1.6e-3
610.6e-9 1.6e-3
610.601e-9 1.5e-3
610.7e-9 1.5e-3
610.701e-9 1.39e-3
610.8e-9 1.39e-3
610.801e-9 1.31e-3
610.9e-9 1.31e-3
610.901e-9 1.23e-3
611e-9 1.23e-3
611.001e-9 1.17e-3
611.1e-9 1.17e-3
611.101e-9 1.1e-3
611.2e-9 1.1e-3
611.201e-9 1.04e-3
611.3e-9 1.04e-3
611.301e-9 9.9e-4
611.4e-9 9.9e-4
611.401e-9 9.4e-4
611.5e-9 9.4e-4
611.501e-9 9e-4
611.6e-9 9e-4
611.601e-9 8.65e-4
611.7e-9 8.65e-4
611.701e-9 8.3e-4
611.8e-9 8.3e-4
611.801e-9 0
616.5e-9 0
616.501e-9 6.0e-3
616.6e-9 6.0e-3
616.601e-9 2.5e-3
616.7e-9 2.5e-3
616.701e-9 2.31e-3
616.8e-9 2.31e-3
616.801e-9 2.14e-3
616.9e-9 2.14e-3
616.901e-9 1.98e-3

617e-9 1.98e-3
617.001e-9 1.84e-3
617.1e-9 1.84e-3
617.101e-9 1.71e-3
617.2e-9 1.71e-3
617.201e-9 1.6e-3
617.3e-9 1.6e-3
617.301e-9 1.5e-3
617.4e-9 1.5e-3
617.401e-9 1.39e-3
617.5e-9 1.39e-3
617.501e-9 1.31e-3
617.6e-9 1.31e-3
617.601e-9 1.23e-3
617.7e-9 1.23e-3
617.701e-9 1.17e-3
617.8e-9 1.17e-3
617.801e-9 1.1e-3
617.9e-9 1.1e-3
617.901e-9 1.04e-3
618e-9 1.04e-3
618.001e-9 9.9e-4
618.1e-9 9.9e-4
618.101e-9 9.4e-4
618.2e-9 9.4e-4
618.201e-9 9e-4
618.3e-9 9e-4
618.301e-9 8.65e-4
618.4e-9 8.65e-4
618.401e-9 8.3e-4
618.5e-9 8.3e-4
618.501e-9 0
839e-9 0
839.001e-9 6.0e-3
839.1e-9 6.0e-3
839.101e-9 2.5e-3
839.2e-9 2.5e-3
839.201e-9 2.31e-3
839.3e-9 2.31e-3
839.301e-9 2.14e-3
839.4e-9 2.14e-3
839.401e-9 1.98e-3
839.5e-9 1.98e-3
839.501e-9 1.84e-3
839.6e-9 1.84e-3
839.601e-9 1.71e-3

839.7e-9 1.71e-3
839.701e-9 1.6e-3
839.8e-9 1.6e-3
839.801e-9 1.5e-3
839.9e-9 1.5e-3
839.901e-9 1.39e-3
840e-9 1.39e-3
840.001e-9 1.31e-3
840.1e-9 1.31e-3
840.101e-9 1.23e-3
840.2e-9 1.23e-3
840.201e-9 1.17e-3
840.3e-9 1.17e-3
840.301e-9 1.1e-3
840.4e-9 1.1e-3
840.401e-9 1.04e-3
840.5e-9 1.04e-3
840.501e-9 9.9e-4
840.6e-9 9.9e-4
840.601e-9 9.4e-4
840.7e-9 9.4e-4
840.701e-9 9e-4
840.8e-9 9e-4
840.801e-9 8.65e-4
840.9e-9 8.65e-4
840.901e-9 8.3e-4
841e-9 8.3e-4
841.001e-9 0
1000e-9 0
1000.001e-9 6.0e-3
1000.1e-9 6.0e-3
1000.101e-9 2.5e-3
1000.2e-9 2.5e-3
1000.201e-9 2.31e-3
1000.3e-9 2.31e-3
1000.301e-9 2.14e-3
1000.4e-9 2.14e-3
1000.401e-9 1.98e-3
1000.5e-9 1.98e-3
1000.501e-9 1.84e-3
1000.6e-9 1.84e-3
1000.601e-9 1.71e-3
1000.7e-9 1.71e-3
1000.701e-9 1.6e-3
1000.8e-9 1.6e-3
1000.801e-9 1.5e-3

1000.9e-9 1.5e-3
1000.901e-9 1.39e-3
1001e-9 1.39e-3
1001.001e-9 1.31e-3
1001.1e-9 1.31e-3
1001.101e-9 1.23e-3
1001.2e-9 1.23e-3
1001.201e-9 1.17e-3
1001.3e-9 1.17e-3
1001.301e-9 1.1e-3
1001.4e-9 1.1e-3
1001.401e-9 1.04e-3
1001.5e-9 1.04e-3
1001.501e-9 9.9e-4
1001.6e-9 9.9e-4
1001.601e-9 9.4e-4
1001.7e-9 9.4e-4
1001.701e-9 9e-4
1001.8e-9 9e-4
1001.801e-9 8.65e-4
1001.9e-9 8.65e-4
1001.901e-9 8.3e-4
1002e-9 8.3e-4
1002.001e-9 0
1080e-9 0
1080.001e-9 6.0e-3
1080.1e-9 6.0e-3
1080.101e-9 2.5e-3
1080.2e-9 2.5e-3
1080.201e-9 2.31e-3
1080.3e-9 2.31e-3
1080.301e-9 2.14e-3
1080.4e-9 2.14e-3
1080.401e-9 1.98e-3
1080.5e-9 1.98e-3
1080.501e-9 1.84e-3
1080.6e-9 1.84e-3
1080.601e-9 1.71e-3
1080.7e-9 1.71e-3
1080.701e-9 1.6e-3
1080.8e-9 1.6e-3
1080.801e-9 1.5e-3
1080.9e-9 1.5e-3
1080.901e-9 1.39e-3
1081e-9 1.39e-3
1081.001e-9 1.31e-3

1081.1e-9 1.31e-3
1081.101e-9 1.23e-3
1081.2e-9 1.23e-3
1081.201e-9 1.17e-3
1081.3e-9 1.17e-3
1081.301e-9 1.1e-3
1081.4e-9 1.1e-3
1081.401e-9 1.04e-3
1081.5e-9 1.04e-3
1081.501e-9 9.9e-4
1081.6e-9 9.9e-4
1081.601e-9 9.4e-4
1081.7e-9 9.4e-4
1081.701e-9 9e-4
1081.8e-9 9e-4
1081.801e-9 8.65e-4
1081.9e-9 8.65e-4
1081.901e-9 8.3e-4
1082e-9 8.3e-4
1082.001e-9 0
1500e-9 0

APPENDIX 5: DATA FAULTS TEST VECTOR

(NOTE: This is used to simulate the effects of a voltage spike of +5V starting at 409ns and ending at 413.5ns while running the basic functionality test vector (D Input). The format of the information that follows is a space delineated listing of time and magnitude of voltage to be applied at the stated time.

EXAMPLE: 5e-9 -5 means at 5ns apply -5V)

0e-9 -5
5e-9 -5
5.1e-9 0
55e-9 0
55.1e-9 -5
100e-9 -5
100.1e-9 0
155e-9 0
155.1e-9 -5
200e-9 -5
230e-9 -5
230.1e-9 0
300e-9 -5
300.1e-9 -5
409e-9 -5
409.0001e-9 0
413.5001e-9 0
413.50011e-9 -5
600e-9 -5
600.1e-9 0
830e-9 0
830.1e-9 -5
900e-9 -5
900.1e-9 0
955e-9 0
955.1e-9 0
1055e-9 -5
1055.1e-9 0
1155e-9 0
1155.1e-9 -5
1255e-9 -5
1255.1e-9 0
1355e-9 0
1355.1e-9 -5
1455e-9 -5
1455e-9 0
1500e-9 0

APPENDIX 6: MAJORITY LOGIC OUTPUT HIGH CURRENT BARRAGE TEST VECTOR

(NOTE: This is used to simulate the effects of an ion interaction on the n^+/p junction of a MOSFET transistor (6.0mA prompt dose) which is greater than the lower current barrage defined in Appendix 3. It is applied as a general current value where current flows from the node applied to the low rail voltage in the circuit. The format of the information that follows is a space delineated listing of time and magnitude of current to be applied at the stated time.

EXAMPLE: 150.001e-9 5e-3 means at 150.001ns apply 5.5mA)

0e-9 0
150e-9 0
150.001e-9 6.0e-3
150.1e-9 6.0e-3
150.101e-9 2.5e-3
150.2e-9 2.5e-3
150.201e-9 2.31e-3
150.3e-9 2.31e-3
150.301e-9 2.14e-3
150.4e-9 2.14e-3
150.401e-9 1.98e-3
150.5e-9 1.98e-3
150.501e-9 1.84e-3
150.6e-9 1.84e-3
150.601e-9 1.71e-3
150.7e-9 1.71e-3
150.701e-9 1.6e-3
150.8e-9 1.6e-3
150.801e-9 1.5e-3
150.9e-9 1.5e-3
150.901e-9 1.39e-3
151e-9 1.39e-3
151.001e-9 1.31e-3
151.1e-9 1.31e-3
151.101e-9 1.23e-3
151.2e-9 1.23e-3
151.201e-9 1.17e-3
151.3e-9 1.17e-3
151.301e-9 1.1e-3
151.4e-9 1.1e-3
151.401e-9 1.04e-3
151.5e-9 1.04e-3
151.501e-9 9.9e-4
151.6e-9 9.9e-4
151.601e-9 9.4e-4
151.7e-9 9.4e-4

151.701e-9 9e-4
151.8e-9 9e-4
151.801e-9 8.65e-4
151.9e-9 8.65e-4
151.901e-9 8.3e-4
152e-9 8.3e-4
152.001e-9 0
222.500e-9 0
222.501e-9 6.0e-3
222.600e-9 6.0e-3
222.601e-9 2.5e-3
222.700e-9 2.5e-3
222.701e-9 2.31e-3
222.800e-9 2.31e-3
222.801e-9 2.14e-3
222.900e-9 2.14e-3
222.901e-9 1.98e-3
223.000e-9 1.98e-3
223.101e-9 1.84e-3
223.200e-9 1.84e-3
223.201e-9 1.71e-3
223.300e-9 1.71e-3
223.301e-9 1.6e-3
223.400e-9 1.6e-3
223.401e-9 1.5e-3
223.500e-9 1.5e-3
223.501e-9 1.39e-3
223.600e-9 1.39e-3
223.601e-9 1.31e-3
223.700e-9 1.31e-3
223.701e-9 1.23e-3
223.800e-9 1.23e-3
223.801e-9 1.17e-3
223.900e-9 1.17e-3
223.901e-9 1.1e-3
224.000e-9 1.1e-3
224.001e-9 1.04e-3
224.100e-9 1.04e-3
224.101e-9 9.9e-4
224.200e-9 9.9e-4
224.201e-9 9.4e-4
224.300e-9 9.4e-4
224.301e-9 9e-4
224.400e-9 9e-4
224.401e-9 8.65e-4
224.500e-9 8.65e-4

224.501e-9 8.3e-4
224.6e-9 0
224.601e-9 6.0e-3
224.7e-9 6.0e-3
224.701e-9 2.5e-3
224.8e-9 2.5e-3
224.801e-9 2.31e-3
224.9e-9 2.31e-3
224.901e-9 2.14e-3
225e-9 2.14e-3
225.001e-9 1.98e-3
225.100e-9 1.98e-3
225.101e-9 1.84e-3
225.200e-9 1.84e-3
225.201e-9 1.71e-3
225.3e-9 1.71e-3
225.301e-9 1.6e-3
225.4e-9 1.6e-3
225.401e-9 1.5e-3
225.5e-9 1.5e-3
225.501e-9 1.39e-3
225.6e-9 1.39e-3
225.601e-9 1.31e-3
225.7e-9 1.31e-3
225.701e-9 1.23e-3
225.8e-9 1.23e-3
225.801e-9 1.17e-3
225.9e-9 1.17e-3
225.901e-9 1.1e-3
226e-9 1.1e-3
226.001e-9 1.04e-3
226.1e-9 1.04e-3
226.101e-9 9.9e-4
226.2e-9 9.9e-4
226.201e-9 9.4e-4
226.3e-9 9.4e-4
226.301e-9 9e-4
226.4e-9 9e-4
226.401e-9 8.65e-4
226.5e-9 8.65e-4
226.501e-9 8.3e-4
226.6e-9 8.3e-4
226.601e-9 0
245.000e-9 0
245.001e-9 6.0e-3
245.100e-9 6.0e-3

245.101e-9 2.5e-3
245.200e-9 2.5e-3
245.201e-9 2.31e-3
245.300e-9 2.31e-3
245.301e-9 2.14e-3
245.400e-9 2.14e-3
245.401e-9 1.98e-3
245.500e-9 1.98e-3
245.501e-9 1.84e-3
245.600e-9 1.84e-3
245.601e-9 1.71e-3
245.700e-9 1.71e-3
245.701e-9 1.6e-3
245.800e-9 1.6e-3
245.801e-9 1.5e-3
245.900e-9 1.5e-3
245.901e-9 1.39e-3
246.000e-9 1.39e-3
246.001e-9 1.31e-3
246.100e-9 1.31e-3
246.101e-9 1.23e-3
246.200e-9 1.23e-3
246.201e-9 1.17e-3
246.300e-9 1.17e-3
246.301e-9 1.1e-3
246.400e-9 1.1e-3
246.401e-9 1.04e-3
246.500e-9 1.04e-3
246.501e-9 9.9e-4
246.600e-9 9.9e-4
246.601e-9 9.4e-4
246.700e-9 9.4e-4
246.701e-9 9e-4
246.800e-9 9e-4
246.801e-9 8.65e-4
246.900e-9 8.65e-4
246.901e-9 8.3e-4
247.000e-9 8.3e-4
247.001e-9 0
430.000e-9 0
430.001e-9 6.0e-3
430.100e-9 6.0e-3
430.101e-9 2.5e-3
430.200e-9 2.5e-3
430.201e-9 2.31e-3
430.300e-9 2.31e-3

430.301e-9 2.14e-3
430.400e-9 2.14e-3
430.401e-9 1.98e-3
430.500e-9 1.98e-3
430.501e-9 1.84e-3
430.600e-9 1.84e-3
430.601e-9 1.71e-3
430.700e-9 1.71e-3
430.701e-9 1.6e-3
430.800e-9 1.6e-3
430.801e-9 1.5e-3
430.900e-9 1.5e-3
430.901e-9 1.39e-3
431.000e-9 1.39e-3
431.001e-9 1.31e-3
431.100e-9 1.31e-3
431.101e-9 1.23e-3
431.200e-9 1.23e-3
431.201e-9 1.17e-3
431.300e-9 1.17e-3
431.301e-9 1.1e-3
431.400e-9 1.1e-3
431.401e-9 1.04e-3
431.500e-9 1.04e-3
431.501e-9 9.9e-4
431.600e-9 9.9e-4
431.601e-9 9.4e-4
431.700e-9 9.4e-4
431.701e-9 9e-4
431.800e-9 9e-4
431.801e-9 8.65e-4
431.900e-9 8.65e-4
431.901e-9 8.3e-4
432.000e-9 8.3e-4
432.001e-9 0
609.800e-9 0
609.801e-9 6.0e-3
609.900e-9 6.0e-3
609.901e-9 2.5e-3
610.000e-9 2.5e-3
610.001e-9 2.31e-3
610.200e-9 2.31e-3
610.201e-9 2.14e-3
610.300e-9 2.14e-3
610.301e-9 1.98e-3
610.400e-9 1.98e-3

610.401e-9 1.84e-3
610.500e-9 1.84e-3
610.501e-9 1.71e-3
610.600e-9 1.71e-3
610.601e-9 1.6e-3
610.700e-9 1.6e-3
610.701e-9 1.5e-3
610.800e-9 1.5e-3
610.801e-9 1.39e-3
610.900e-9 1.39e-3
610.901e-9 1.31e-3
611.000e-9 1.31e-3
611.001e-9 1.23e-3
611.100e-9 1.23e-3
611.101e-9 1.17e-3
611.200e-9 1.17e-3
611.201e-9 1.1e-3
611.300e-9 1.1e-3
611.301e-9 1.04e-3
611.400e-9 1.04e-3
611.401e-9 9.9e-4
611.500e-9 9.9e-4
611.501e-9 9.4e-4
611.600e-9 9.4e-4
611.601e-9 9e-4
611.700e-9 9e-4
611.701e-9 8.65e-4
611.800e-9 8.65e-4
611.801e-9 8.3e-4
611.900e-9 8.3e-4
611.901e-9 0
612.000e-9 8.3e-4
612.001e-9 8.3e-4
612.002e-9 0
616.500e-9 0
616.501e-9 6.0e-3
616.600e-9 6.0e-3
616.601e-9 2.5e-3
616.700e-9 2.5e-3
616.701e-9 2.31e-3
616.800e-9 2.31e-3
616.801e-9 2.14e-3
616.900e-9 2.14e-3
616.901e-9 1.98e-3
617.000e-9 1.98e-3
617.001e-9 1.84e-3

617.100e-9 1.84e-3
617.101e-9 1.71e-3
617.200e-9 1.71e-3
617.201e-9 1.6e-3
617.300e-9 1.6e-3
617.301e-9 1.5e-3
617.400e-9 1.5e-3
617.401e-9 1.39e-3
617.500e-9 1.39e-3
617.501e-9 1.31e-3
617.600e-9 1.31e-3
617.601e-9 1.23e-3
617.700e-9 1.23e-3
617.701e-9 1.17e-3
617.800e-9 1.17e-3
617.801e-9 1.1e-3
617.900e-9 1.1e-3
617.901e-9 1.04e-3
618.000e-9 1.04e-3
618.001e-9 9.9e-4
618.100e-9 9.9e-4
618.101e-9 9.4e-4
618.200e-9 9.4e-4
618.201e-9 9e-4
618.300e-9 9e-4
618.301e-9 8.65e-4
618.400e-9 8.65e-4
618.401e-9 8.3e-4
618.500e-9 8.3e-4
618.501e-9 0
618.600e-9 8.3e-4
618.601e-9 8.3e-4
618.602e-9 0
622.700e-9 0
622.701e-9 6.0e-3
622.800e-9 6.0e-3
622.801e-9 2.5e-3
622.900e-9 2.5e-3
622.901e-9 2.31e-3
623.000e-9 2.31e-3
623.001e-9 2.14e-3
623.100e-9 2.14e-3
623.101e-9 1.98e-3
623.200e-9 1.98e-3
623.201e-9 1.84e-3
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623.301e-9 1.71e-3
623.400e-9 1.71e-3
623.401e-9 1.6e-3
623.500e-9 1.6e-3
623.501e-9 1.5e-3
623.600e-9 1.5e-3
623.601e-9 1.39e-3
623.700e-9 1.39e-3
623.701e-9 1.31e-3
623.800e-9 1.31e-3
623.801e-9 1.23e-3
623.900e-9 1.23e-3
623.901e-9 1.17e-3
624.000e-9 1.17e-3
624.001e-9 1.1e-3
624.100e-9 1.1e-3
624.101e-9 1.04e-3
624.200e-9 1.04e-3
624.201e-9 9.9e-4
624.300e-9 9.9e-4
624.301e-9 9.4e-4
624.400e-9 9.4e-4
624.401e-9 9e-4
624.500e-9 9e-4
624.501e-9 8.65e-4
624.600e-9 8.65e-4
624.601e-9 8.3e-4
624.700e-9 8.3e-4
624.701e-9 0
839.000e-9 0
839.001e-9 6.0e-3
839.100e-9 6.0e-3
839.101e-9 2.5e-3
839.200e-9 2.5e-3
839.201e-9 2.31e-3
839.300e-9 2.31e-3
839.301e-9 2.14e-3
839.400e-9 2.14e-3
839.401e-9 1.98e-3
839.500e-9 1.98e-3
839.501e-9 1.84e-3
839.600e-9 1.84e-3
839.601e-9 1.71e-3
839.700e-9 1.71e-3
839.701e-9 1.6e-3
839.800e-9 1.6e-3

839.801e-9 1.5e-3
839.900e-9 1.5e-3
839.901e-9 1.39e-3
840.000e-9 1.39e-3
840.001e-9 1.31e-3
840.100e-9 1.31e-3
840.101e-9 1.23e-3
840.200e-9 1.23e-3
840.201e-9 1.17e-3
840.300e-9 1.17e-3
840.301e-9 1.1e-3
840.400e-9 1.1e-3
840.401e-9 1.04e-3
840.500e-9 1.04e-3
840.501e-9 9.9e-4
840.600e-9 9.9e-4
840.601e-9 9.4e-4
840.700e-9 9.4e-4
840.701e-9 9e-4
840.800e-9 9e-4
840.801e-9 8.65e-4
840.900e-9 8.65e-4
840.901e-9 8.3e-4
841.000e-9 8.3e-4
841.001e-9 0
1000.000e-9 0
1000.001e-9 6.0e-3
1000.100e-9 6.0e-3
1000.101e-9 2.5e-3
1000.200e-9 2.5e-3
1000.201e-9 2.31e-3
1000.300e-9 2.31e-3
1000.301e-9 2.14e-3
1000.400e-9 2.14e-3
1000.401e-9 1.98e-3
1000.500e-9 1.98e-3
1000.501e-9 1.84e-3
1000.600e-9 1.84e-3
1000.601e-9 1.71e-3
1000.700e-9 1.71e-3
1000.701e-9 1.6e-3
1000.800e-9 1.6e-3
1000.801e-9 1.5e-3
1000.900e-9 1.5e-3
1000.901e-9 1.39e-3
1001.000e-9 1.39e-3

1001.001e-9 1.31e-3
1001.100e-9 1.31e-3
1001.101e-9 1.23e-3
1001.200e-9 1.23e-3
1001.201e-9 1.17e-3
1001.300e-9 1.17e-3
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1001.400e-9 1.1e-3
1001.401e-9 1.04e-3
1001.500e-9 1.04e-3
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1001.601e-9 9.4e-4
1001.700e-9 9.4e-4
1001.701e-9 9e-4
1001.800e-9 9e-4
1001.801e-9 8.65e-4
1001.900e-9 8.65e-4
1001.901e-9 8.3e-4
1002.000e-9 8.3e-4
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1022.600e-9 6.0e-3
1022.601e-9 2.5e-3
1022.700e-9 2.5e-3
1022.701e-9 2.31e-3
1022.800e-9 2.31e-3
1022.801e-9 2.14e-3
1022.900e-9 2.14e-3
1022.901e-9 1.98e-3
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1023.100e-9 1.84e-3
1023.101e-9 1.71e-3
1023.200e-9 1.71e-3
1023.201e-9 1.6e-3
1023.300e-9 1.6e-3
1023.301e-9 1.5e-3
1023.400e-9 1.5e-3
1023.401e-9 1.39e-3
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1023.501e-9 1.31e-3
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1023.601e-9 1.23e-3
1023.700e-9 1.23e-3

1023.701e-9 1.17e-3
1023.800e-9 1.17e-3
1023.801e-9 1.1e-3
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1023.901e-9 1.04e-3
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1024.300e-9 9e-4
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1024.400e-9 8.65e-4
1024.401e-9 8.3e-4
1024.500e-9 8.3e-4
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1080.001e-9 6.0e-3
1080.100e-9 6.0e-3
1080.101e-9 2.5e-3
1080.200e-9 2.5e-3
1080.201e-9 2.31e-3
1080.300e-9 2.31e-3
1080.301e-9 2.14e-3
1080.400e-9 2.14e-3
1080.401e-9 1.98e-3
1080.500e-9 1.98e-3
1080.501e-9 1.84e-3
1080.600e-9 1.84e-3
1080.601e-9 1.71e-3
1080.700e-9 1.71e-3
1080.701e-9 1.6e-3
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1081.300e-9 1.17e-3
1081.301e-9 1.1e-3
1081.400e-9 1.1e-3

1081.401e-9 1.04e-3
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1081.600e-9 9.9e-4
1081.601e-9 9.4e-4
1081.700e-9 9.4e-4
1081.701e-9 9e-4
1081.800e-9 9e-4
1081.801e-9 8.65e-4
1081.900e-9 8.65e-4
1081.901e-9 8.3e-4
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1123.700e-9 0
1123.701e-9 6.0e-3
1123.800e-9 6.0e-3
1123.801e-9 2.5e-3
1123.900e-9 2.5e-3
1123.901e-9 2.31e-3
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1124.501e-9 1.5e-3
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1124.601e-9 1.39e-3
1124.700e-9 1.39e-3
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1124.800e-9 1.31e-3
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1124.900e-9 1.23e-3
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1125.301e-9 9.4e-4
1125.400e-9 9.4e-4
1125.401e-9 9e-4
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1125.501e-9 8.65e-4
1125.600e-9 8.65e-4
1125.601e-9 8.3e-4
1125.700e-9 8.3e-4
1125.701e-9 0
1223.500e-9 0
1223.501e-9 6.0e-3
1223.600e-9 6.0e-3
1223.601e-9 2.5e-3
1223.700e-9 2.5e-3
1223.701e-9 2.31e-3
1223.800e-9 2.31e-3
1223.801e-9 2.14e-3
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1223.901e-9 1.98e-3
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1225.300e-9 9e-4

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1225.400e-9 8.65e-4
1225.401e-9 8.3e-4
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1323.700e-9 0
1323.701e-9 6.0e-3
1323.800e-9 6.0e-3
1323.801e-9 2.5e-3
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1325.401e-9 9e-4
1325.500e-9 9e-4
1325.501e-9 8.65e-4
1325.600e-9 8.65e-4
1325.601e-9 8.3e-4
1325.700e-9 8.3e-4

1325.701e-9 0
1423.500e-9 0
1423.501e-9 6.0e-3
1423.600e-9 6.0e-3
1423.601e-9 2.5e-3
1423.700e-9 2.5e-3
1423.701e-9 2.31e-3
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1425.200e-9 9.4e-4
1425.201e-9 9e-4
1425.300e-9 9e-4
1425.301e-9 8.65e-4
1425.400e-9 8.65e-4
1425.401e-9 8.3e-4
1425.500e-9 8.3e-4
1425.501e-9 0
1500e-9 0

APPENDIX 7: AMI05 TECHNOLOGY FAMILY TRANSISTOR PARAMETERS

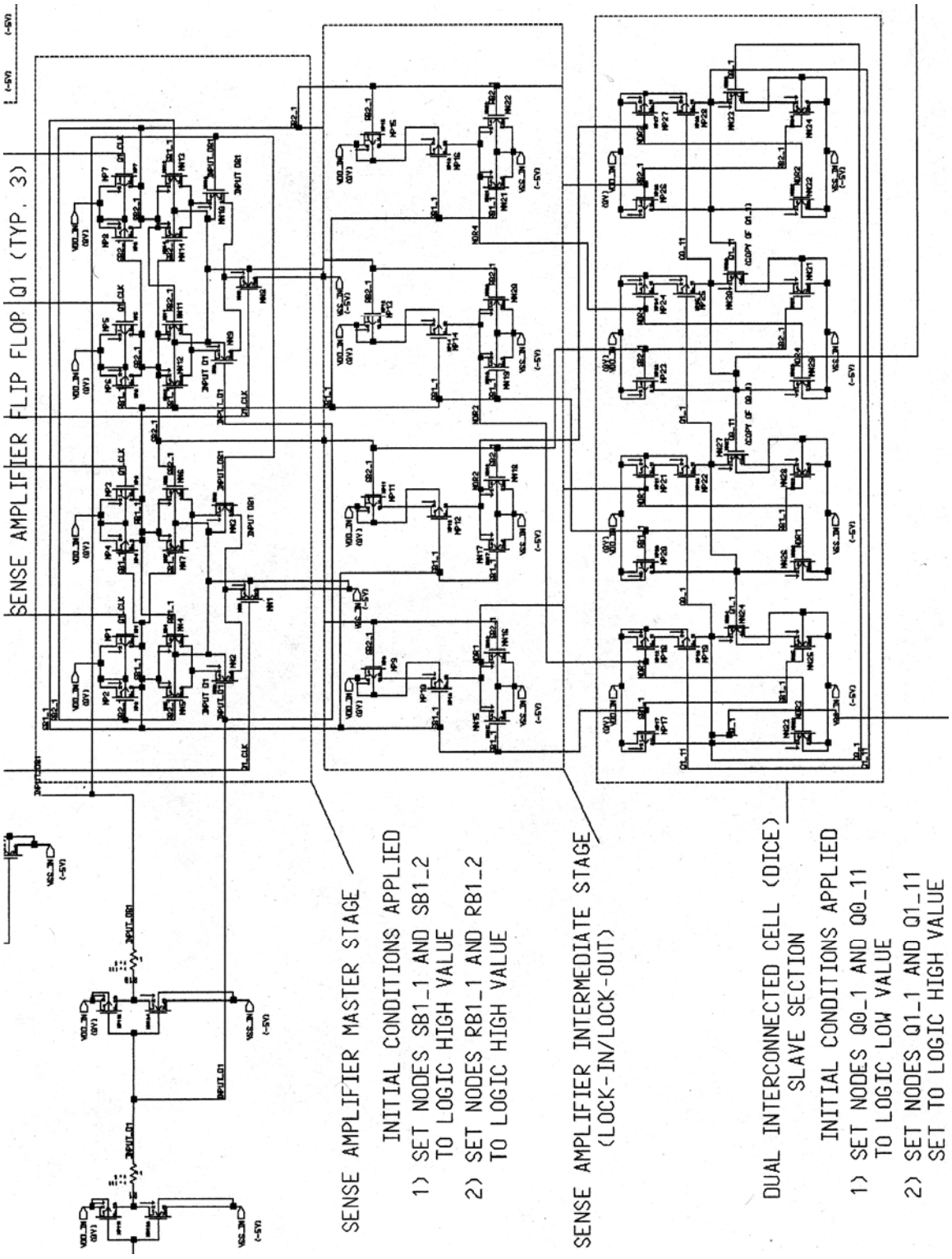
What follows is a listing of the NMOS transistor parameters for the ami05 technology family which were used for modeling purposes.

```
.MODEL n NMOS LEVEL = 53
+TNOM = 27                TOX = 1.41E-8
+XJ = 1.5E-7              NCH = 1.7E17              VTH0 = 0.7086
+K1 = 0.8354582           K2 = -0.088431            K3 = 41.4403818
+K3B = -14                W0 = 6.480766E-7          NLX = 1E-10
+DVT0W = 0                DVT1W = 5.3E6             DVT2W = -0.032
+DVT0 = 3.6139113         DVT1 = 0.3795745          DVT2 = -0.1399976
+U0 = 533.6953445         UA = 7.558023E-10         UB = 1.181167E-18
+UC = 2.582756E-11        VSAT = 1.300981E5         A0 = 0.5292985
+AGS = 0.1463715          B0 = 1.283336E-6          B1 = 1.408099E-6
+KETA = -0.0173166        A1 = 0                    A2 = 1
+RDSW = 2.268366E3        PRWG = -1E-3              PRWB = 6.320549E-5
+WR = 1                   WINT = 2.043512E-7         LINT = 3.034496E-8
+XL = 0                   XW = 0                    DWG = -1.446149E-8
+DWB = 2.077539E-8        VOFF = -0.1137226         NFACTOR = 1.2880596
+CIT = 0                  CDSC = 1.506004E-4        CDSCD = 0
+CDSCB = 0                ETA0 = 3.815372E-4        ETAB = -1.029178E-3
+DSUB = 2.173055E-4       PCLM = 0.6171774          PDIBLC1 = 0.185986
+PDIBLC2 = 3.473187E-3    PDIBLCB = -1E-3           DROUT = 0.4037723
+PSCBE1 = 5.998012E9      PSCBE2 = 3.788068E-8      PVAG = 0.012927
+DELTA = 0.01             MOBMOD = 1                PRT = 0
+UTE = -1.5               KT1 = -0.11               KT1L = 0
+KT2 = 0.022              UA1 = 4.31E-9             UB1 = -7.61E-18
+UC1 = -5.6E-11           AT = 3.3E4                WL = 0
+WLN = 1                  WW = 0                    WWN = 1
+WWL = 0                  LL = 0                    LLN = 1
+LW = 0                   LWN = 1                   LWL = 0
+CAPMOD = 2               XPART = 0.4               CGDO = 1.99E-10
+CGSO = 1.99E-10          CGBO = 0                  CJ  = 4.233802E-4
+PB = 0.9899238           MJ = 0.4495859            CJSW = 3.825632E-10
+PBSW  = 0.1082556        MJSW = 0.1083618          PVTH0 = 0.0212852
+PRDSW  = -16.1546703     PK2 = 0.0253069           WKETA = 0.0188633
+LKETA = 0.0204965
```

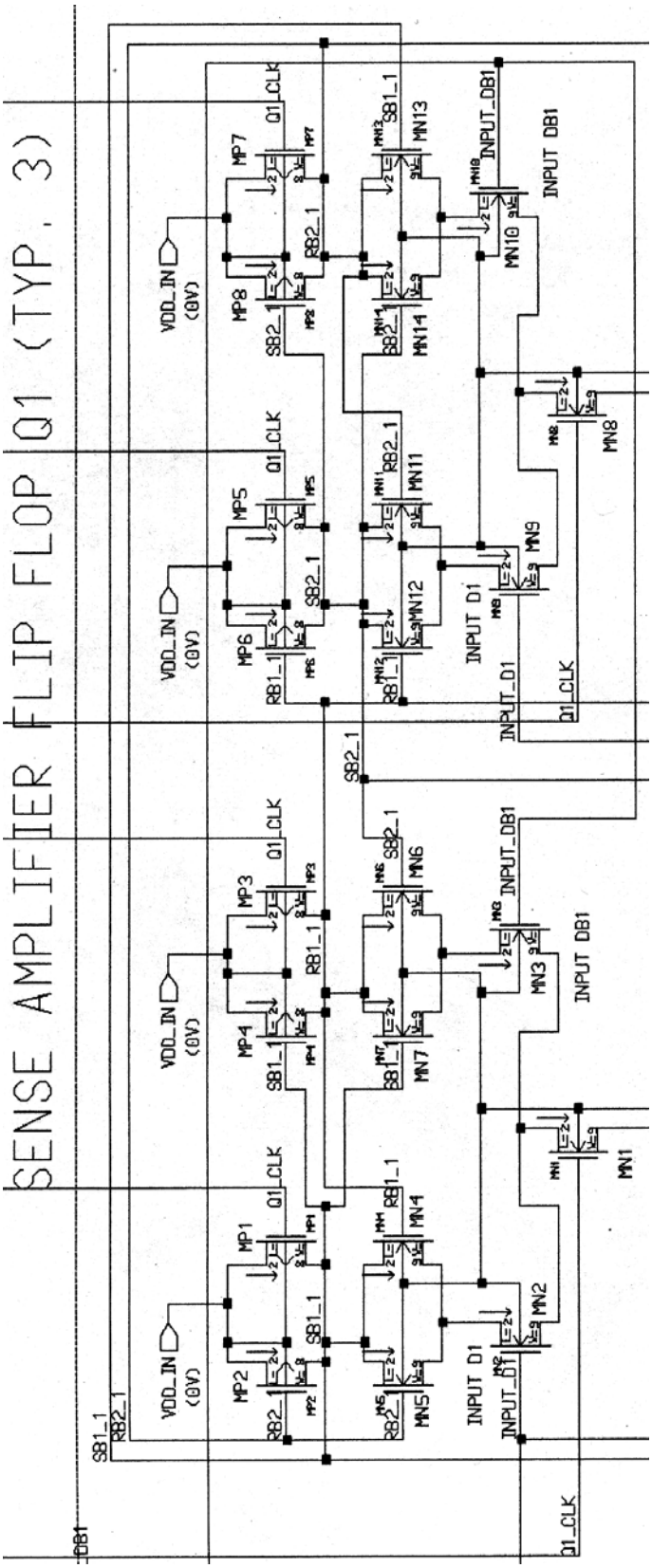
What follows is a listing of the PMOS transistor parameters for the ami05 technology family which were used for modeling purposes.

```
.MODEL p PMOS LEVEL   = 53
+TNOM  = 27                    TOX = 1.41E-8
+XJ = 1.5E-7                   NCH = 1.7E17          VTH0 = -0.9179952
+K1 = 0.5575604                K2 = 0.010265         K3 = 14.0655075
+K3B = -2.3032921              W0 = 1.147829E-6      NLX = 1.114768E-10
+DVT0W = 0                     DVT1W = 5.3E6         DVT2W = -0.032
+DVT0 = 2.2896412              DVT1 = 0.5213085      DVT2 = -0.1337987
+U0  = 202.4540953             UA = 2.290194E-9      UB = 9.779742E-19
+UC = -3.69771E-11             VSAT = 1.307891E5     A0 = 0.8356881
+AGS = 0.1568774               B0 = 2.365956E-6      B1 = 5E-6
+KETA = -5.769328E-3           A1 = 0                A2 = 1
+RDSW = 2.746814E3             PRWG = 2.34865E-3     PRWB = 0.0172298
+WR  = 1                       WINT = 2.586255E-7    LINT = 7.205014E-8
+XL = 0                        XW = 0                DWG = -2.133054E-8
+DWB = 9.857534E-9             VOFF = -0.0837499     NFACTOR = 1.2415529
+CIT = 0                       CDSC = 4.363744E-4    CDSCD = 0
+CDSCB = 0                     ETA0 = 0.11276        ETAB = -2.9484E-3
+DSUB = 0.3389402              PCLM = 4.9847806      PDIBLC1 = 2.481735E-5
+PDIBLC2 = 0.01                PDIBLCB = 0           DROUT = 0.9975107
+PSCBE1  = 3.497872E9          PSCBE2 = 4.974352E-9  PVAG = 10.9914549
+DELTA = 0.01                  MOBMOD = 1            PRT = 0
+UTE = -1.5                    KT1 = -0.11           KT1L = 0
+KT2 = 0.022                   UA1 = 4.31E-9         UB1 = -7.61E-18
+UC1 = -5.6E-11                AT  = 3.3E4           WL = 0
+WLN = 1                       WW = 0                WWN = 1
+WWL = 0                       LL = 0                LLN = 1
+LW = 0                        LWN = 1               LWL = 0
+CAPMOD = 2                    XPART = 0.4           CGDO = 2.4E-10
+CGSO = 2.4E-10                CGBO = 0              CJ = 7.273568E-4
+PB = 0.9665597                MJ = 0.4959837        CJSW = 3.114708E-10
+PBSW = 0.99                   MJSW = 0.2653654      PVTH0 = 9.420541E-3
+PRDSW = -231.2571566          PK2 = 1.396684E-3     WKETA = 1.862966E-3
+LKETA = 5.728589E-3
```

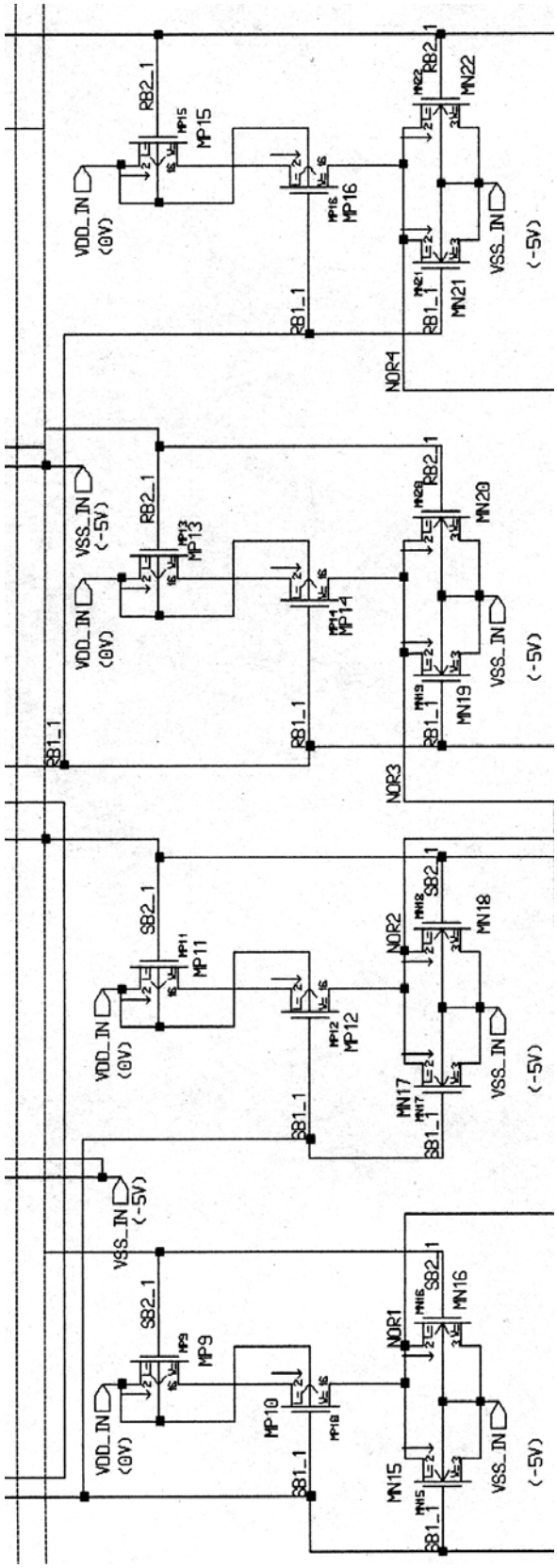
APPENDIX 8: INPUT SAFF SCHEMATICS



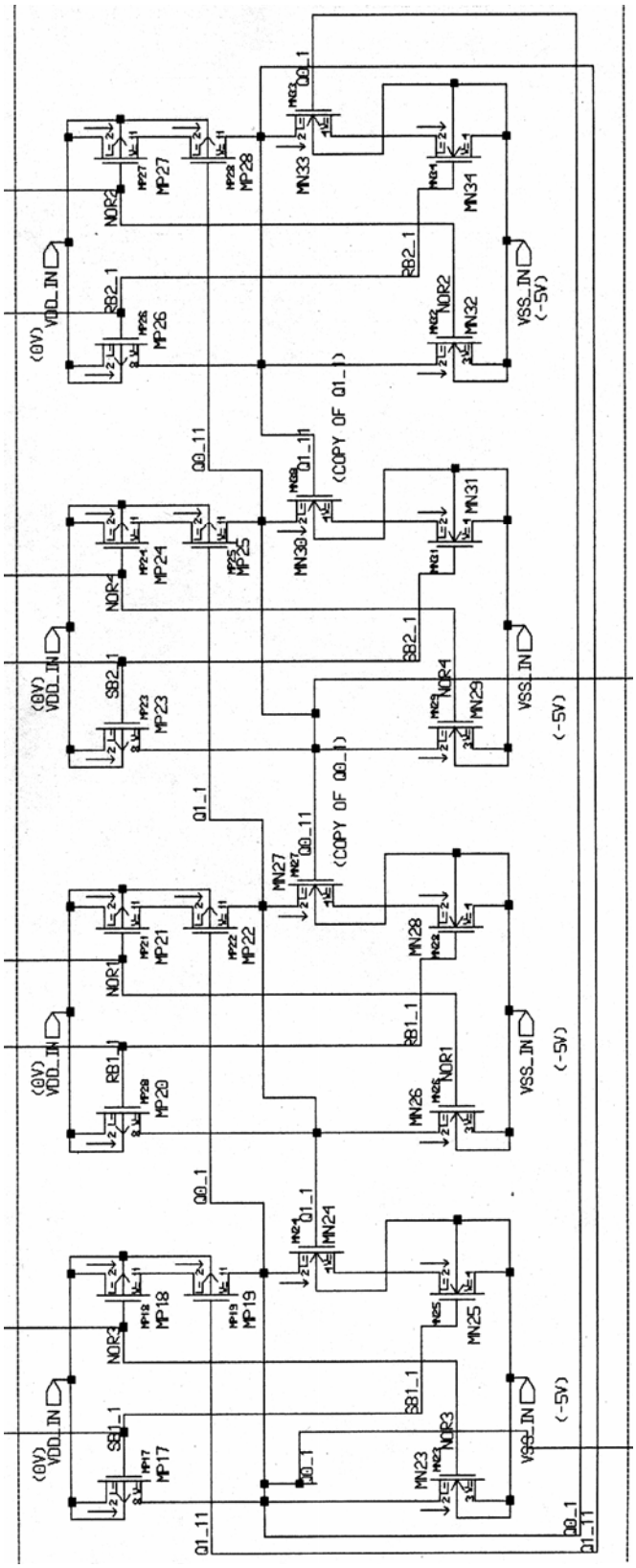
Overall view of TMRSAFF input SAFF (Typical 3).



Expanded view of input SAFF sense amplifier master stage (Typical 3).

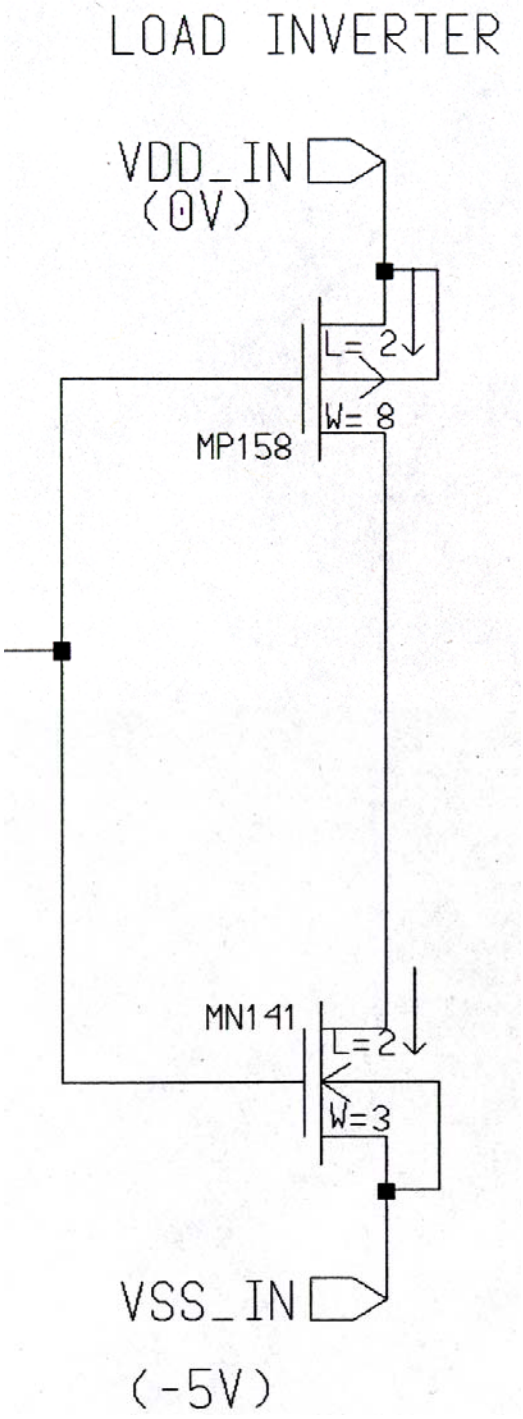


Expanded view of input SAFF intermediate stage (Typical 3).



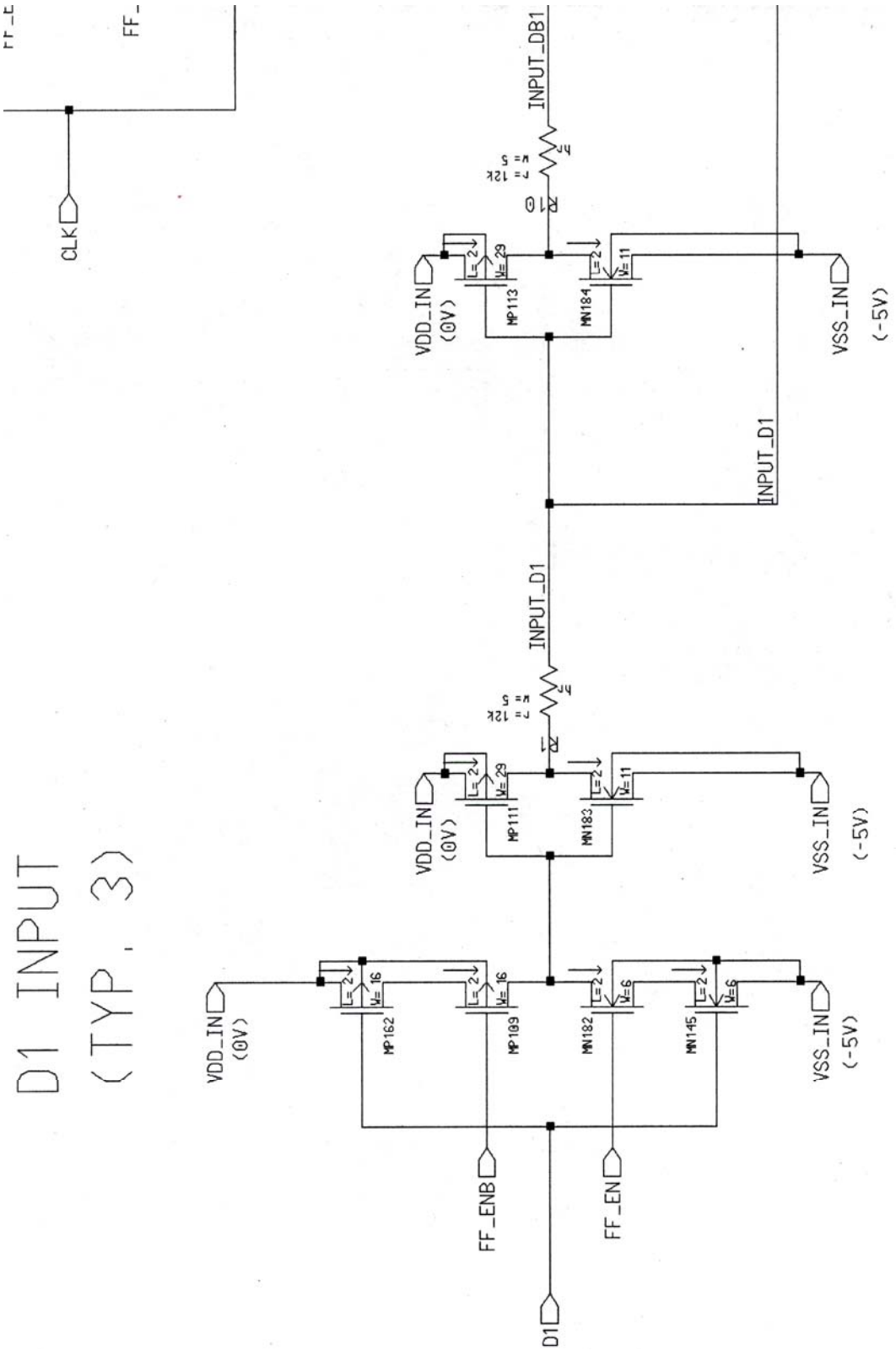
Expanded view of input SAFF slave stage (Typical 3).

APPENDIX 9: INVERTER LOAD SCHEMATIC

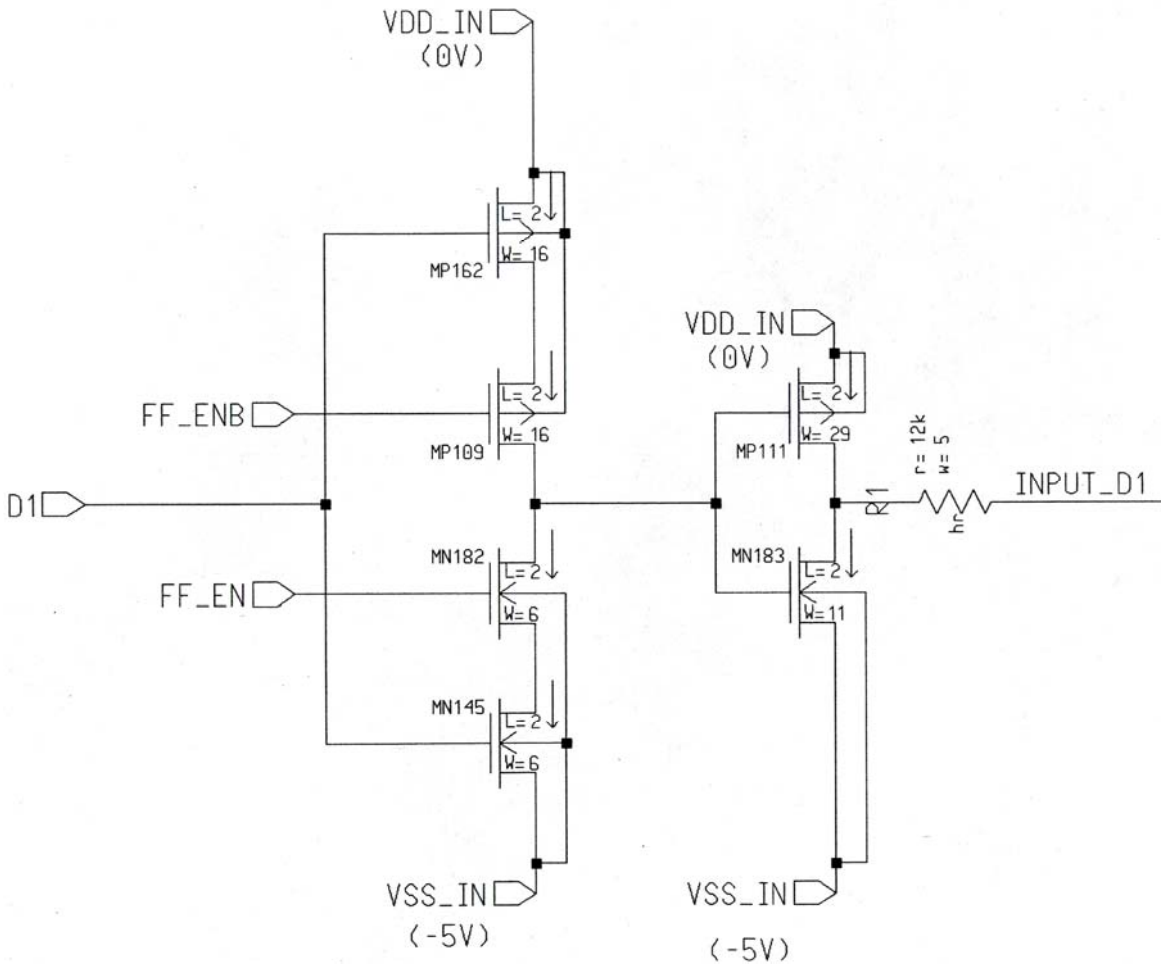


Typical load used throughout testing.

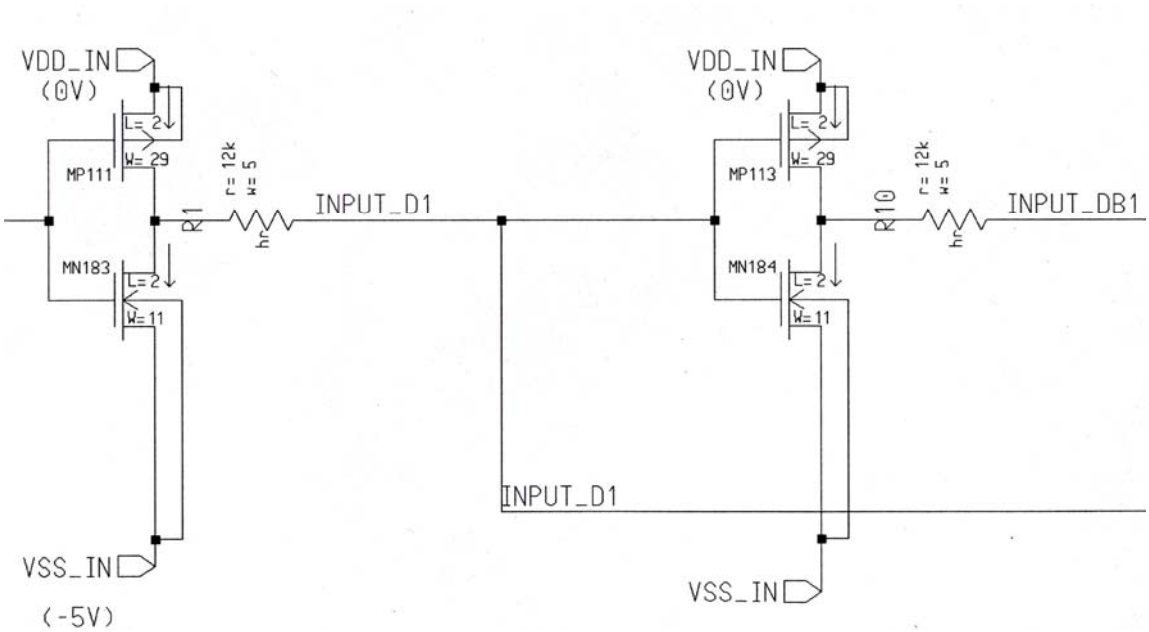
APPENDIX 10: HARDENED INPUT DATA LINE SCHEMATIC



Overall view of TMRSAFF radiation hardened input data line (Typical 3).

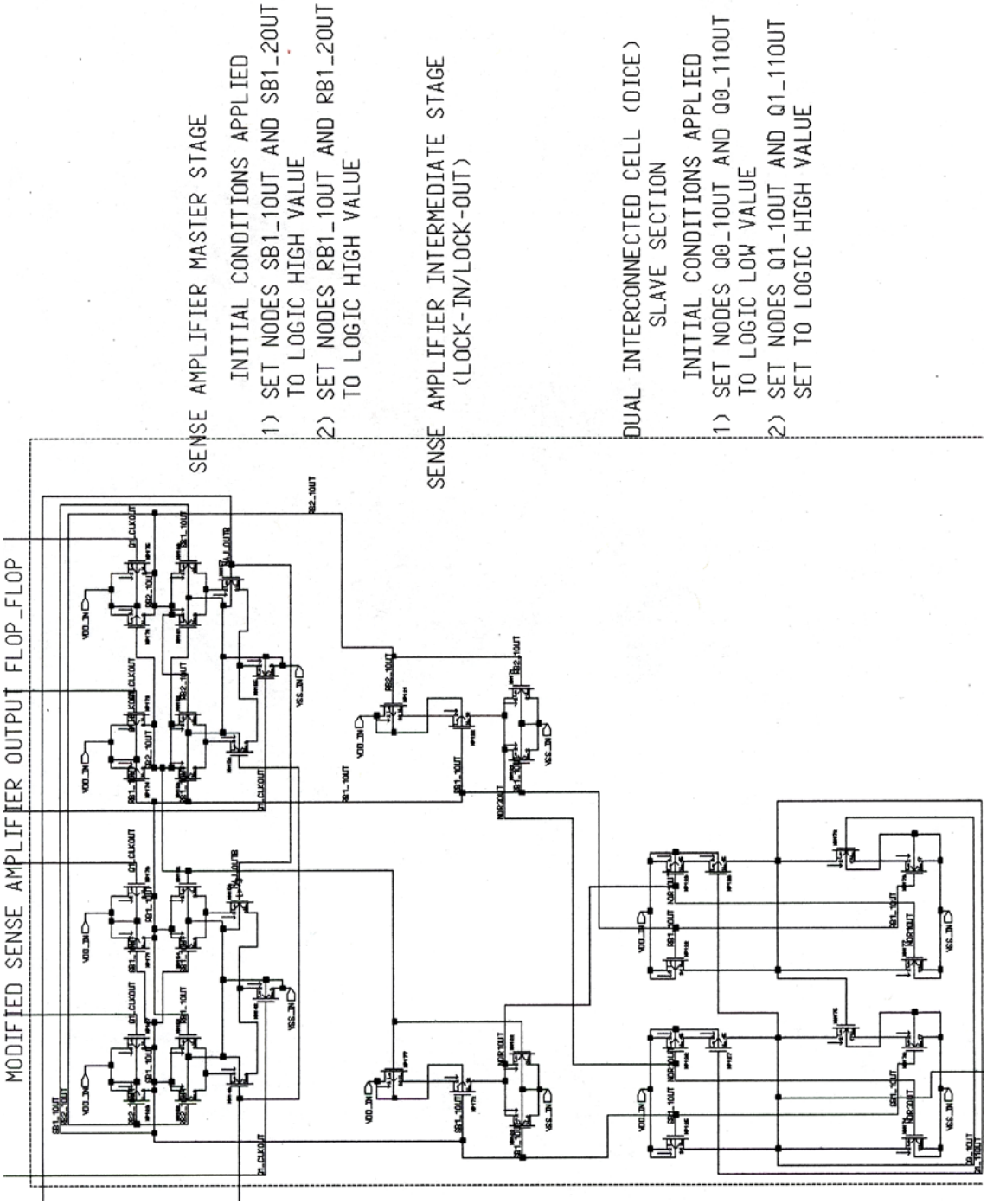


Expanded view of radiation hardened input data line tri-state inverter and inverter which derives the D input to each input SAFF.

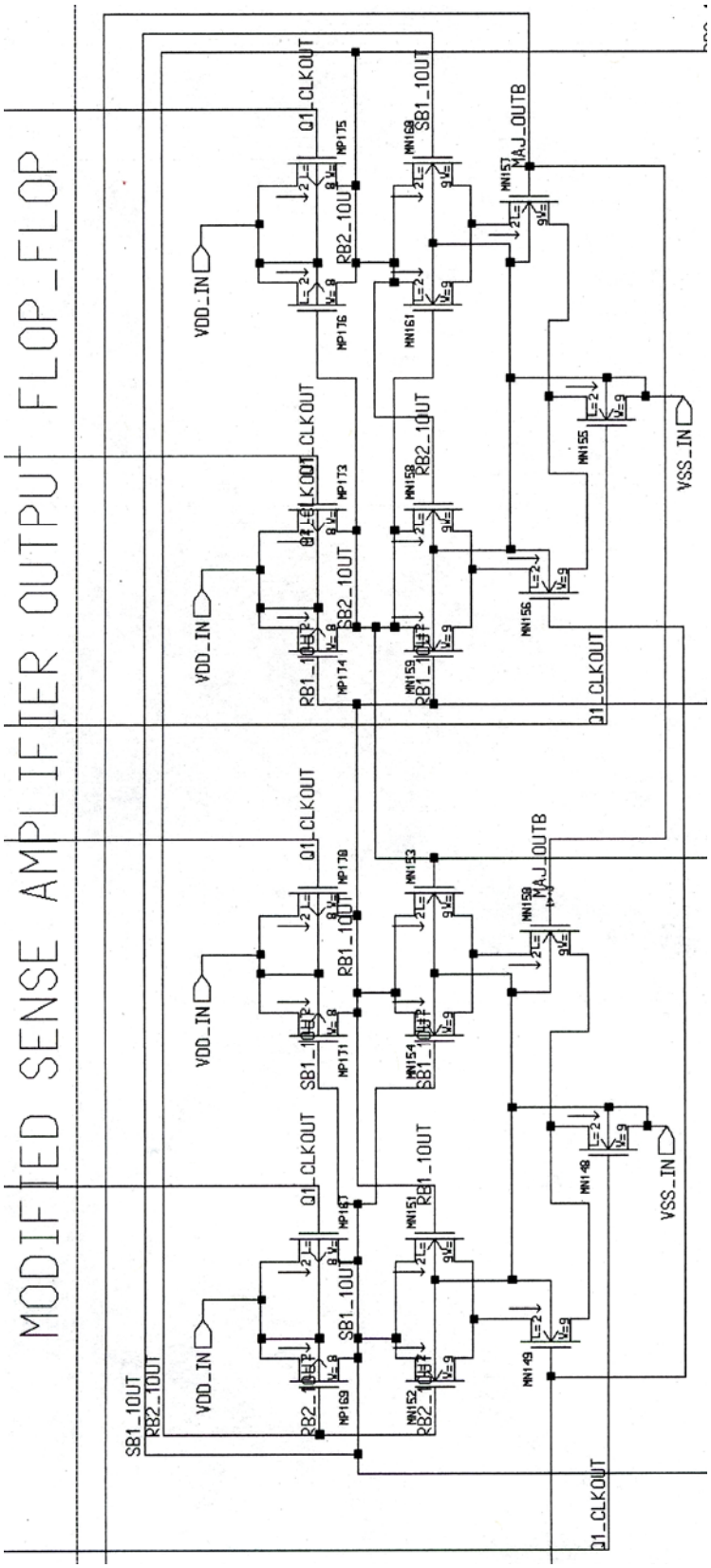


Expanded view of radiation hardened input data line showing inverters which derive both the D input and the DB input for each input SAFF (Typical 3).

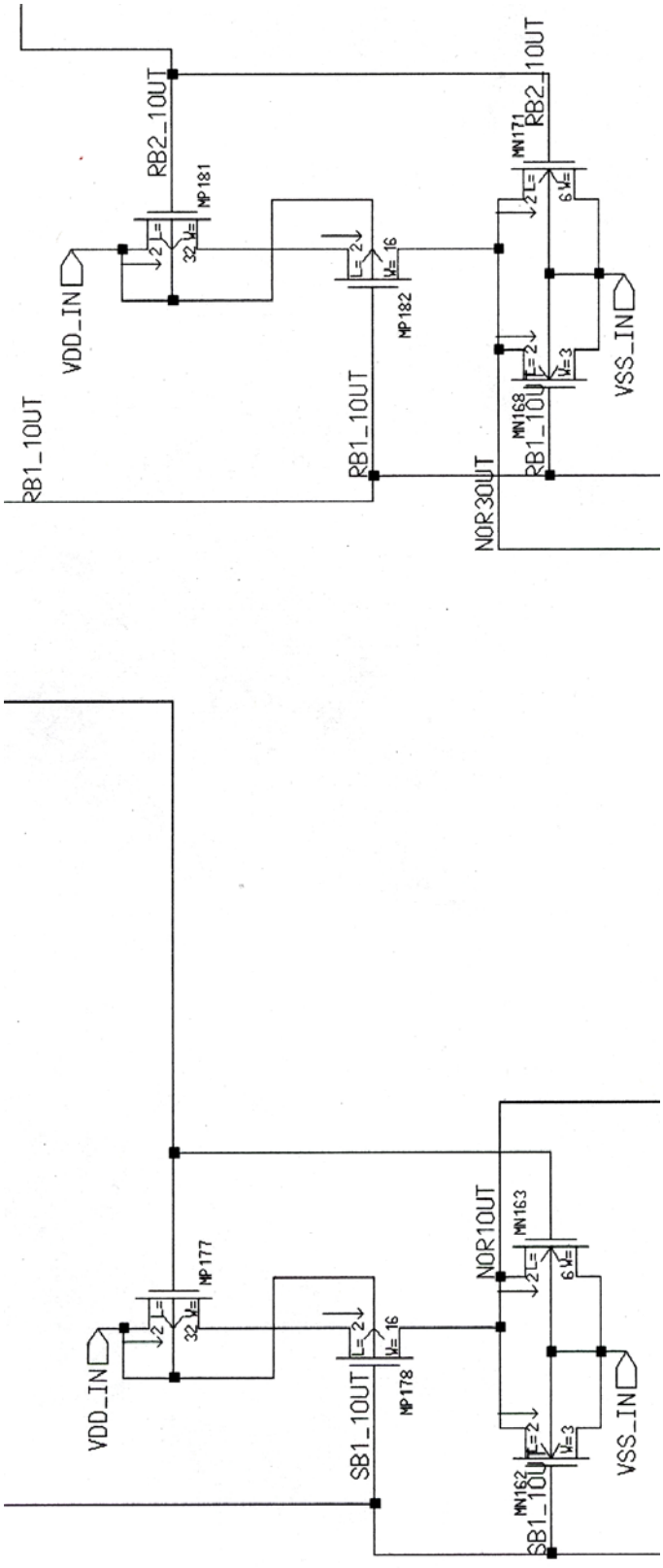
APPENDIX 11: OUTPUT SAFF SCHEMATICS



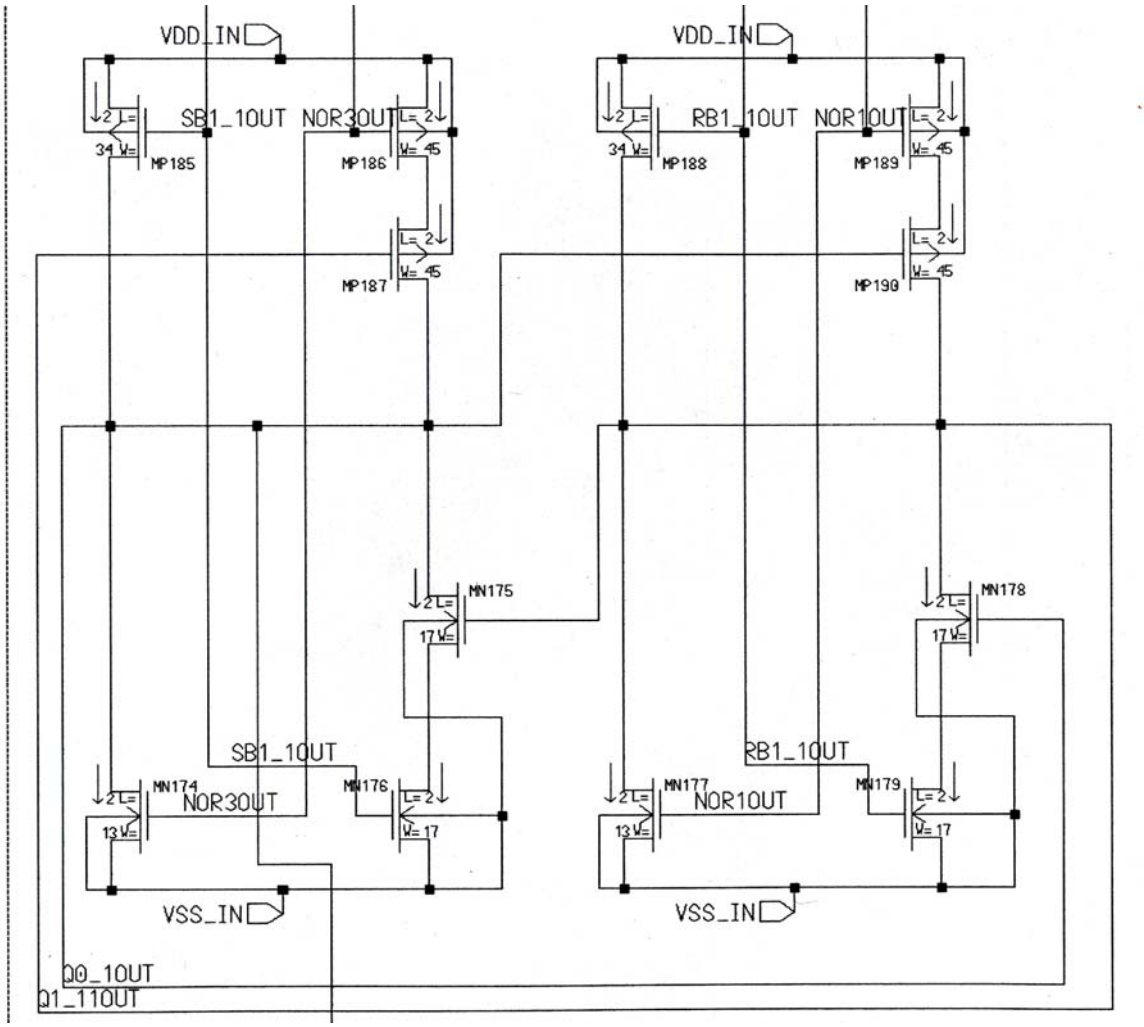
Overall view of TMRSAFF output SAFF (Typical 2 when full redundancy utilized).



Expanded view of output SAFF master stage (Typical 2 when full redundancy utilized).

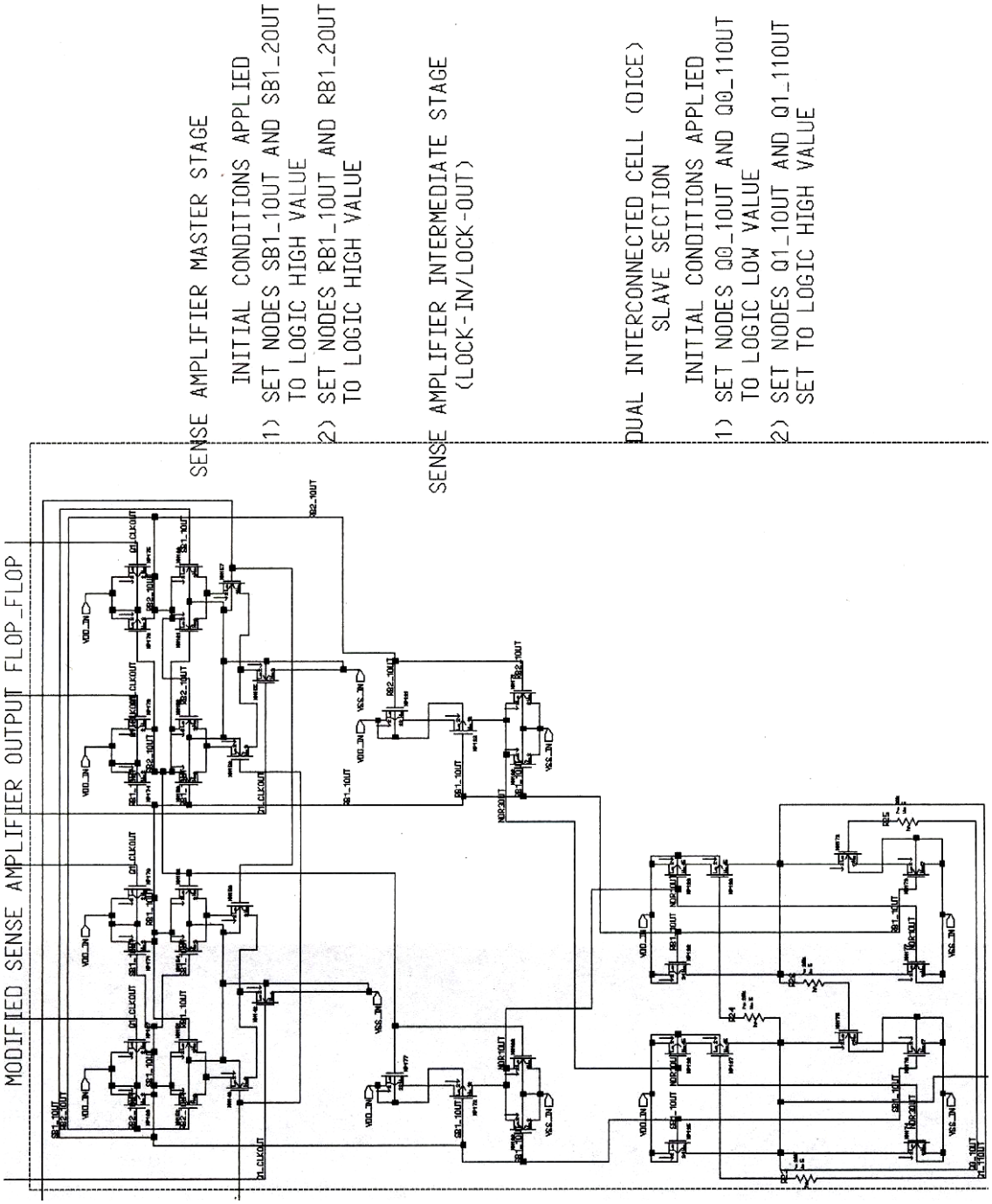


Expanded view of output SAFF intermediate stage (Typical 2 when full redundancy utilized).

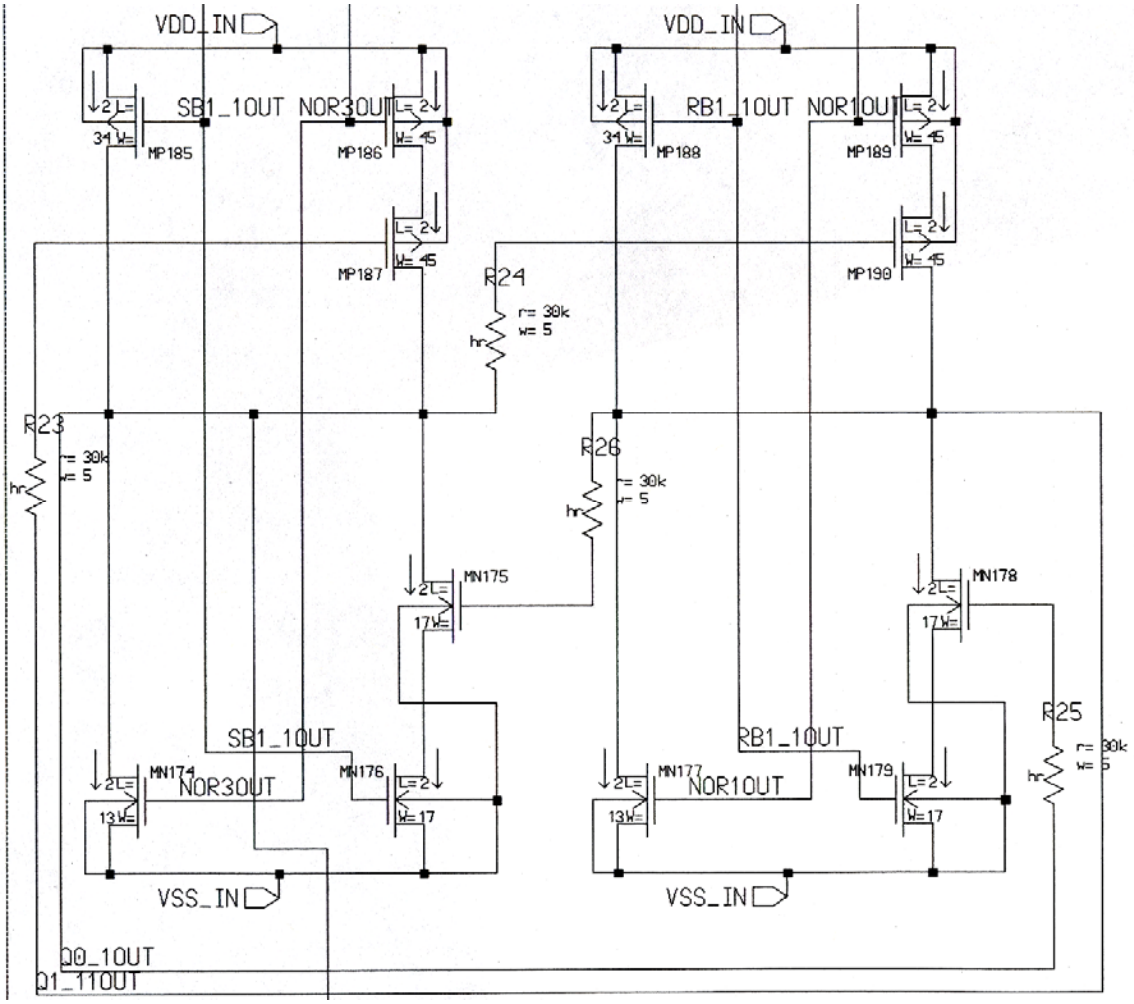


Expanded view of output SAFF slave stage (Typical 2 when full redundancy utilized).

APPENDIX 12: HYPOTHETICAL OUTPUT SAFF SCHEMATICS

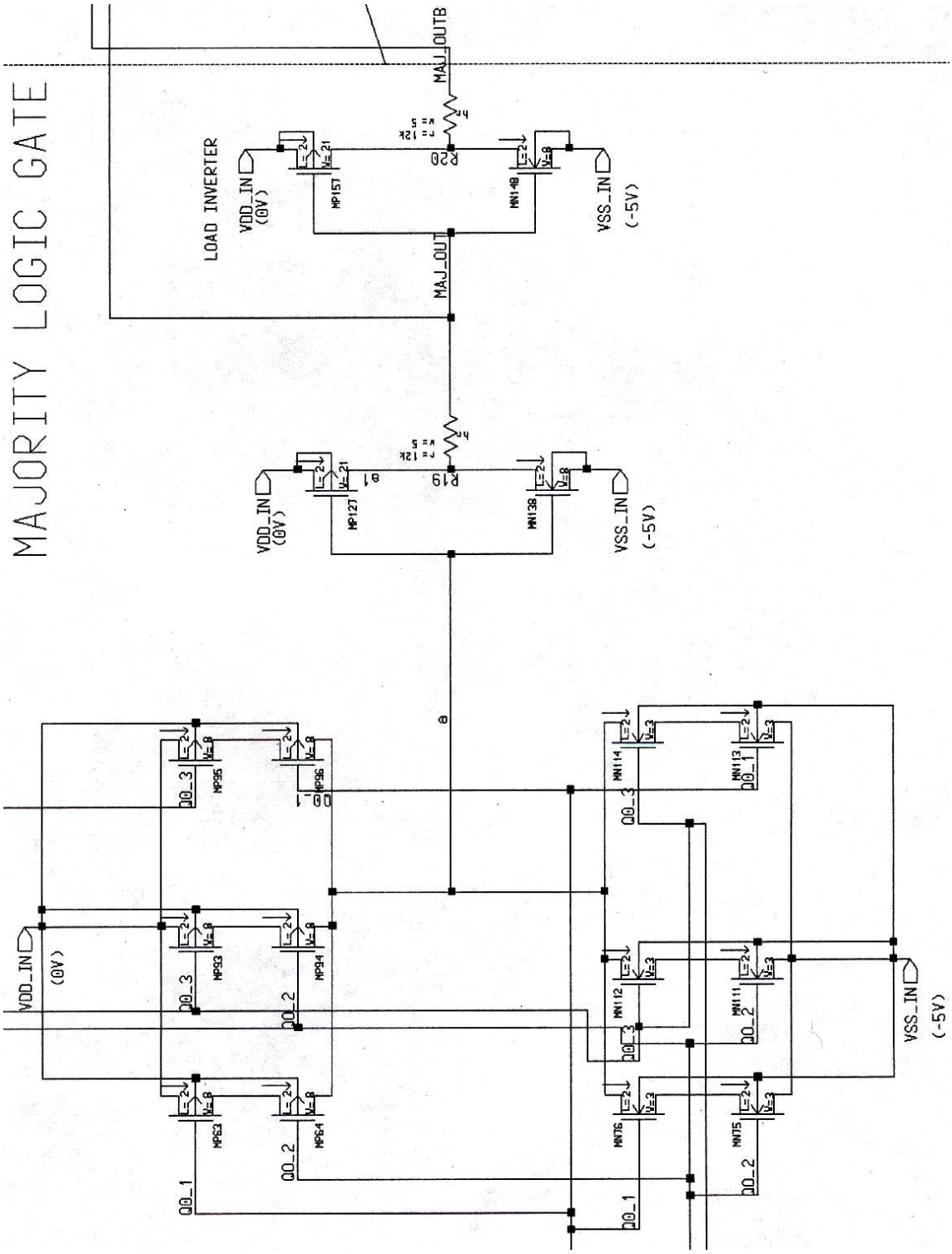


Overall view of hypothetical output SAFF which incorporates 30kΩ resistors in the feedback paths of the output slave section. All other components are identical to those used in the output SAFF of the TMRSAFF design.



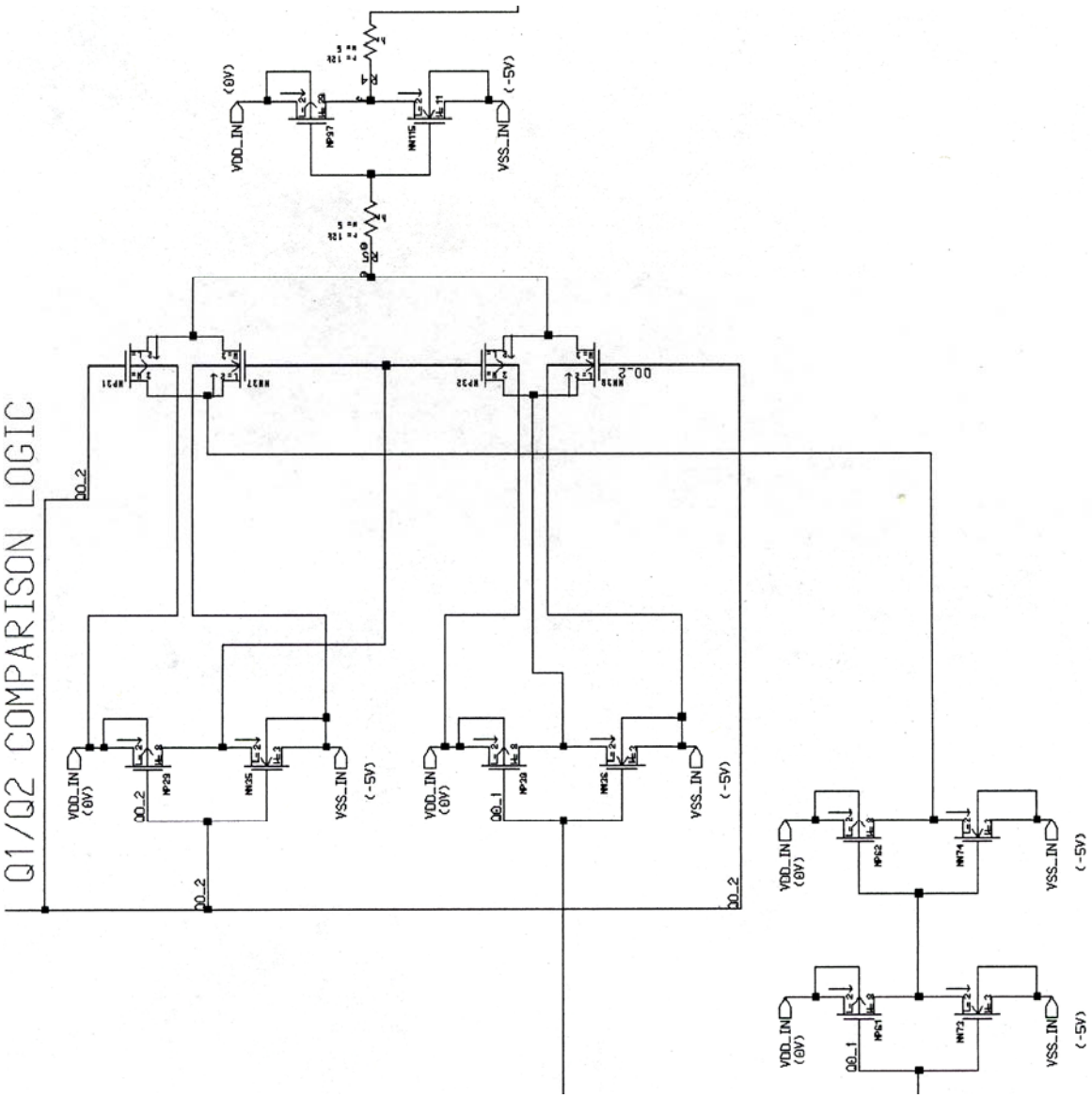
Expanded view of hypothetical output SAFF slave stage.

APPENDIX 13: MAJORITY LOGIC GATE SCHEMATICS

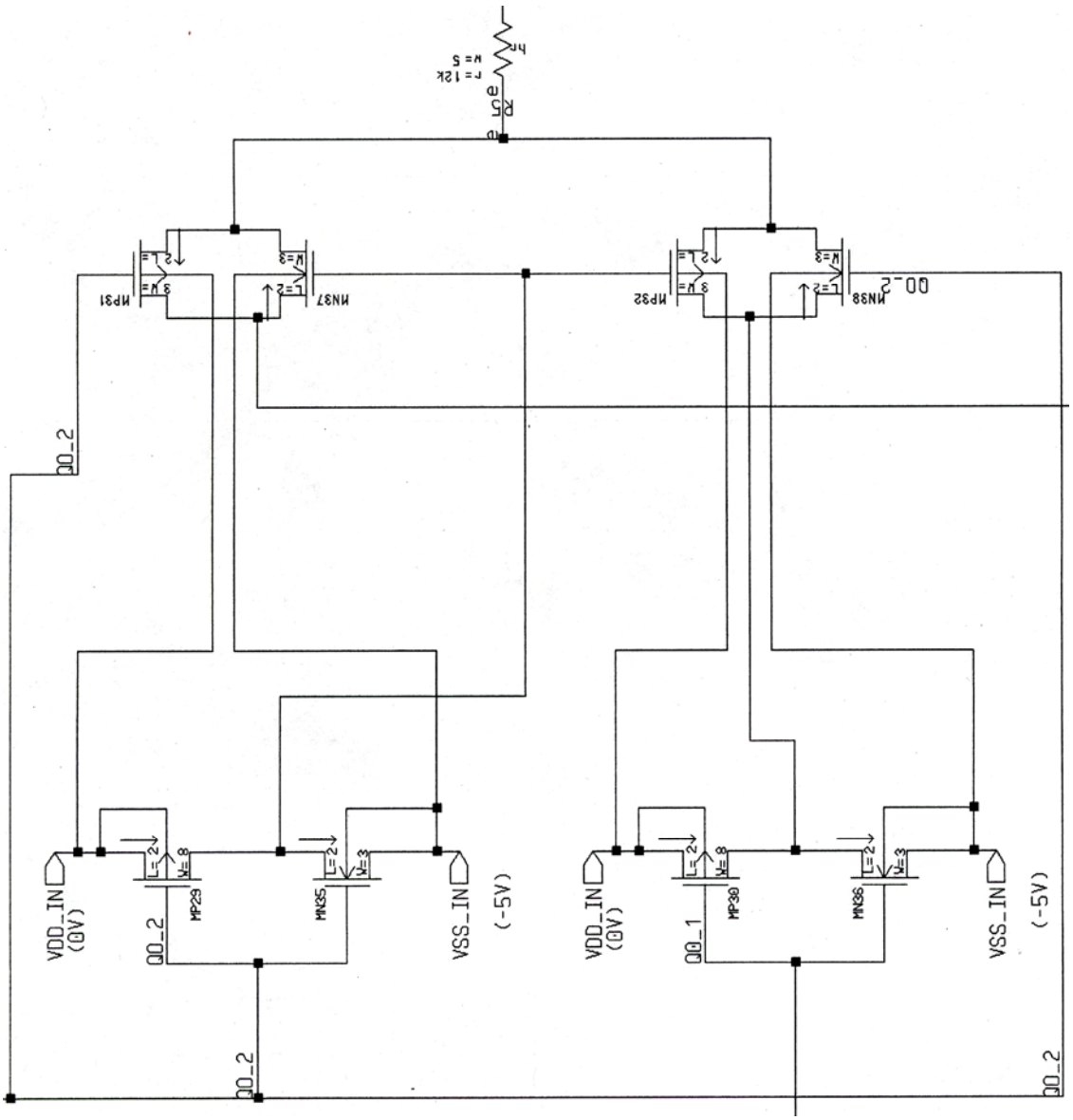


Overall view of TMRSAFF majority logic gate.

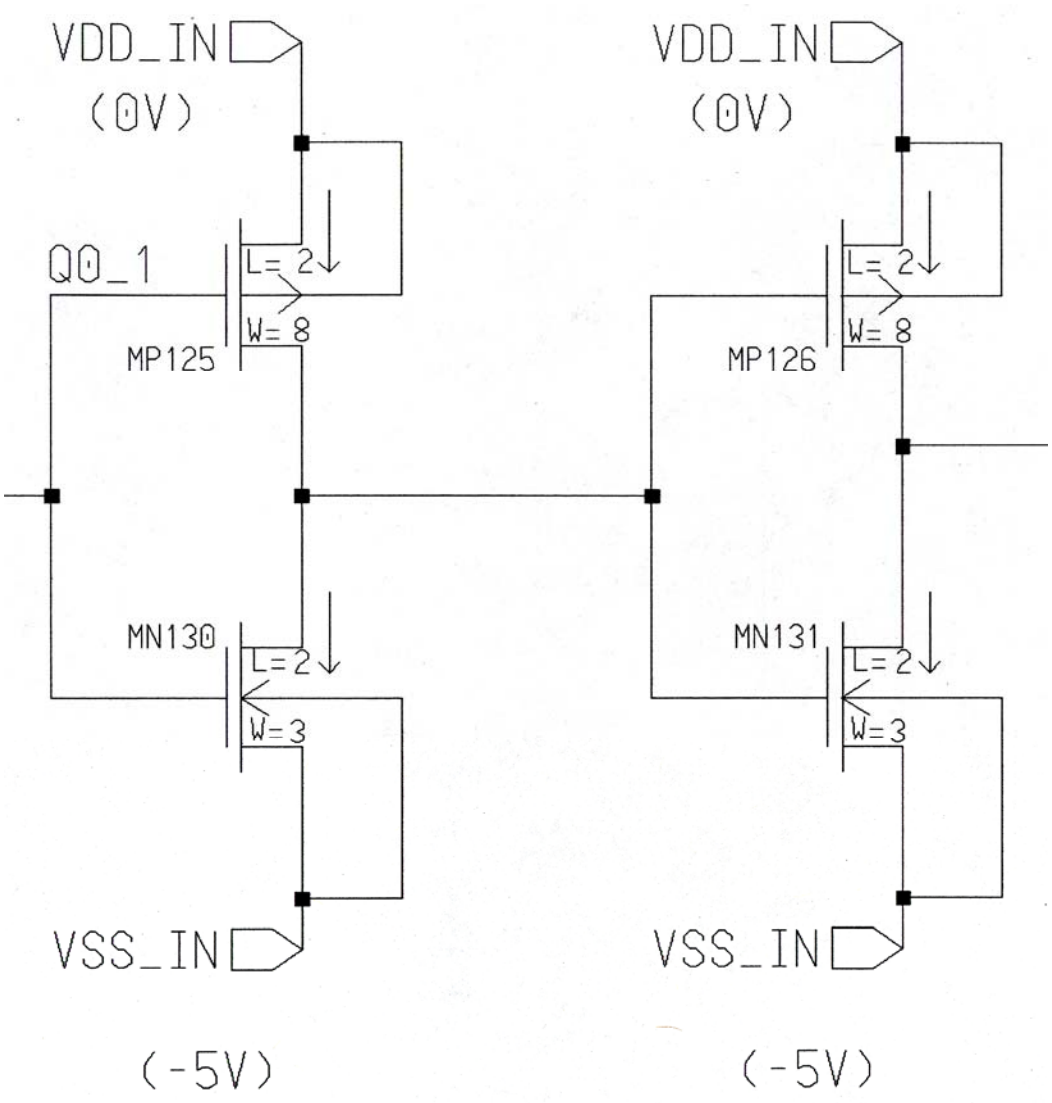
APPENDIX 14: COMPARISON LOGIC SCHEMATICS



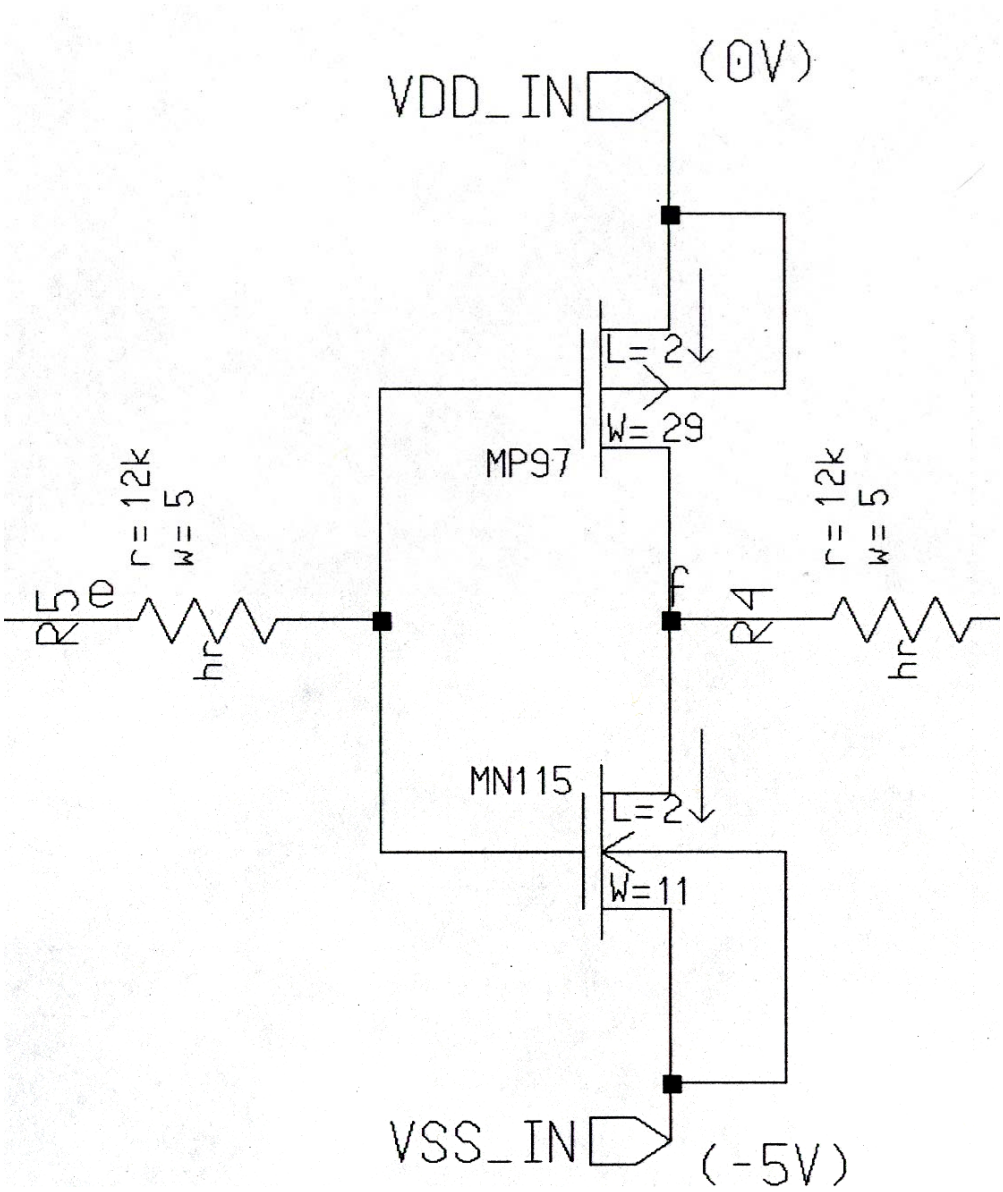
Overall view of Q1/Q2 comparison logics (Typical 3 when full redundancy not used, Typical 6 when full redundancy utilized). General structure is the same for all comparison logic. Only the output inverter varies. In the case of Q1/Q2 and Q2/Q3 comparisons, the output inverters are the same but the Q1/Q3 output inverter was sized larger.



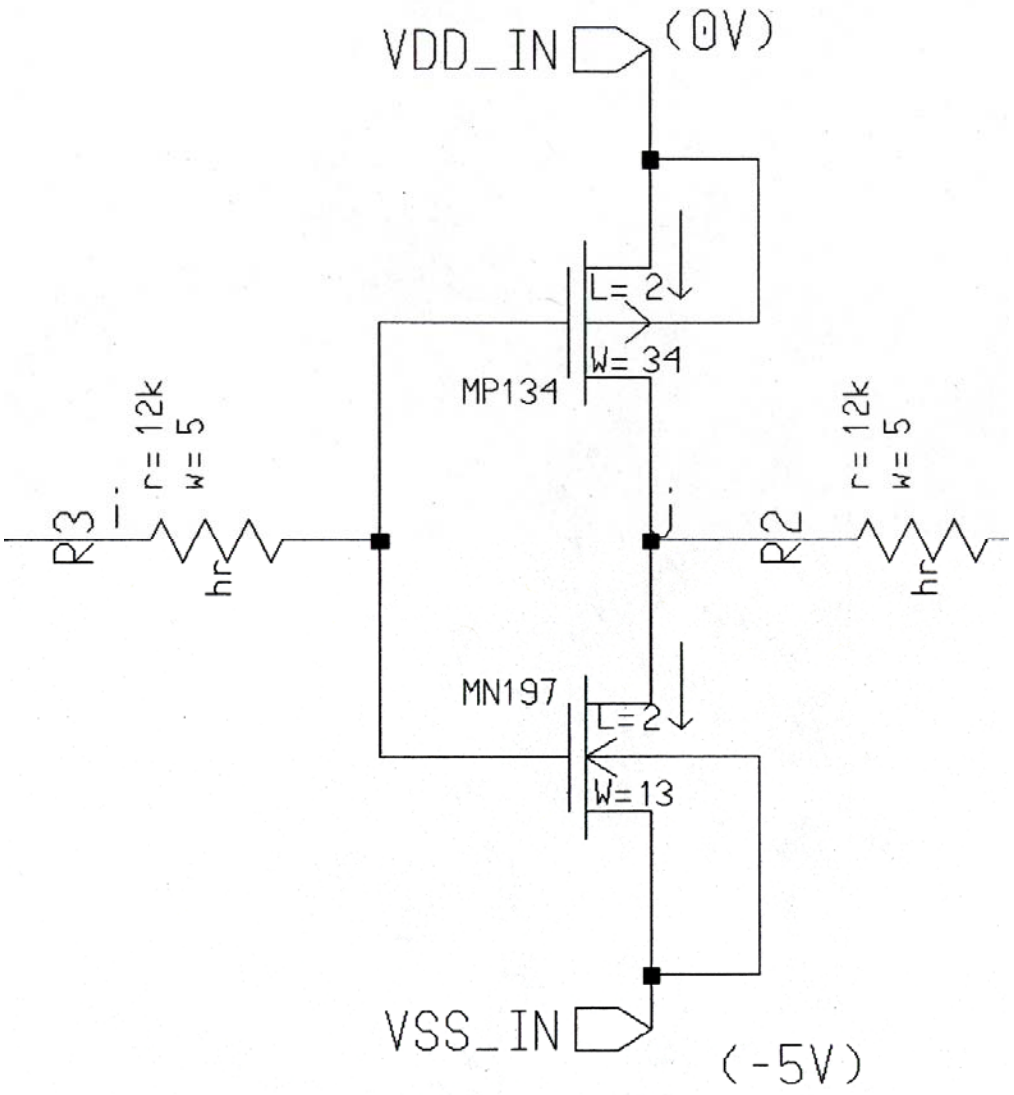
Expanded view of Q1/Q2 comparison logics XOR gate (Typical 3 when full redundancy not used, Typical 6 when full redundancy utilized).



Expanded view of Q1/Q2 comparison logic input inverters used to isolate the comparison logics transistor diffusion from connecting to the upstream input SAFF output (Typical 3 when full redundancy not utilized, Typical 6 when full redundancy utilized).

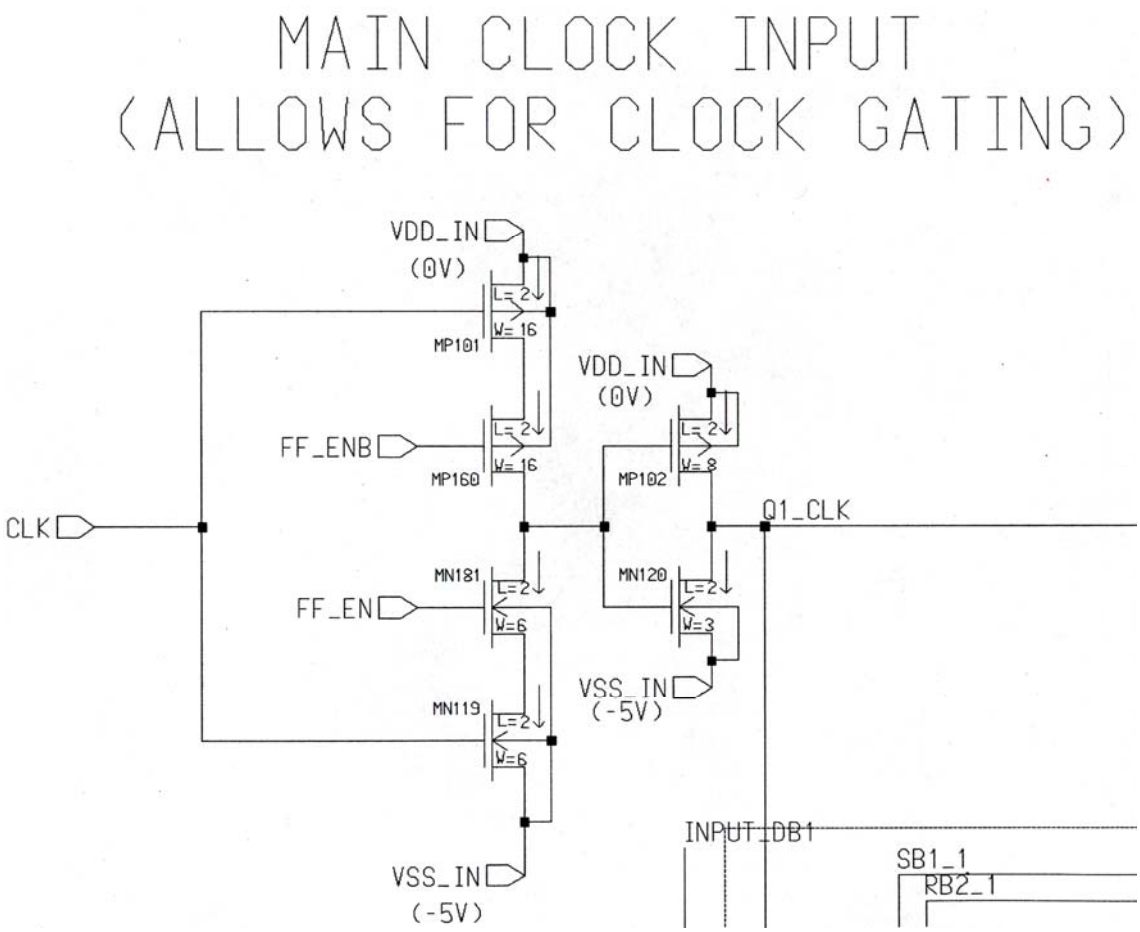


Expanded view of Q1/Q2 (same as Q2/Q3) comparison logic output inverter (Typical 2 when full redundancy not utilized, Typical 4 when full redundancy utilized).

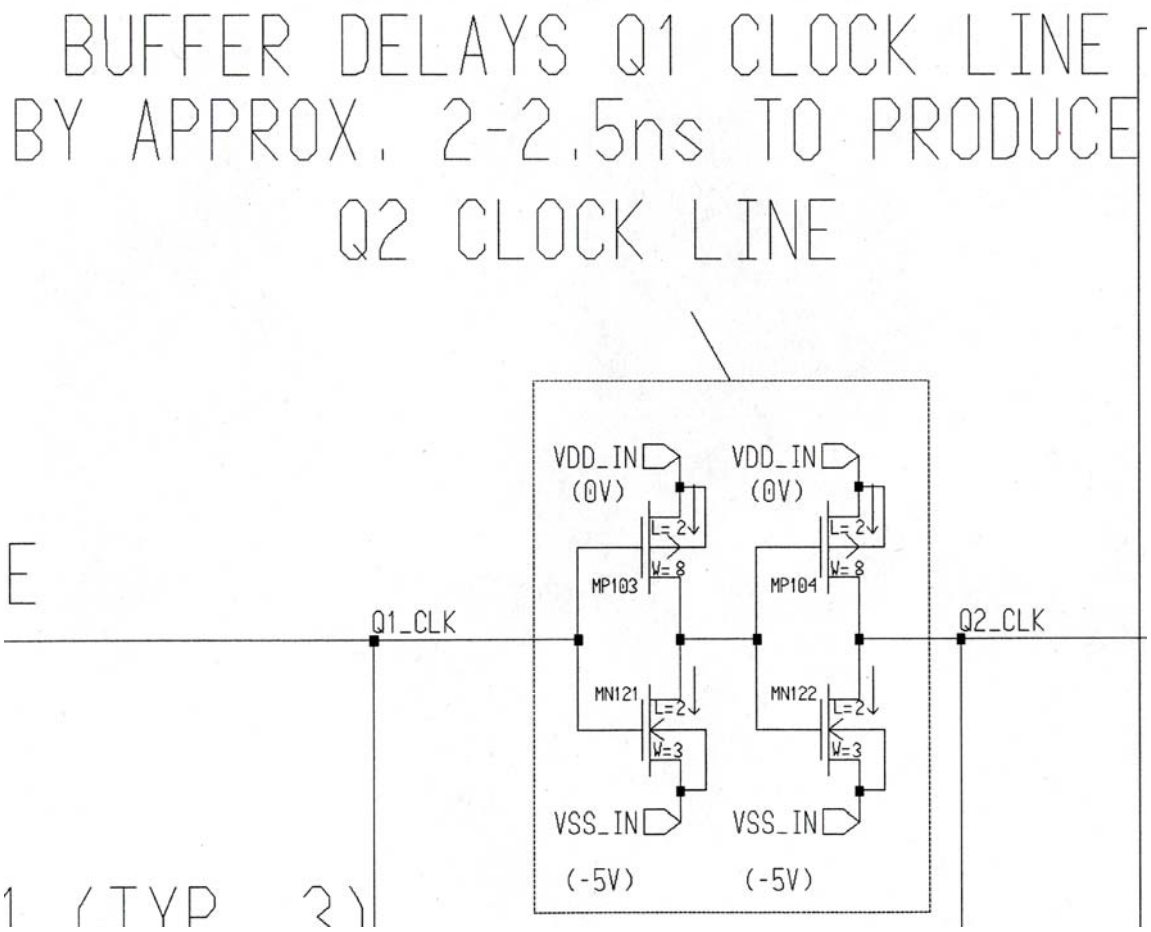


Expanded view of Q1/Q3 comparison logic output inverter (Used only for Q1/Q3 comparison when full redundancy not utilized, Typical 2 when full redundancy utilized).

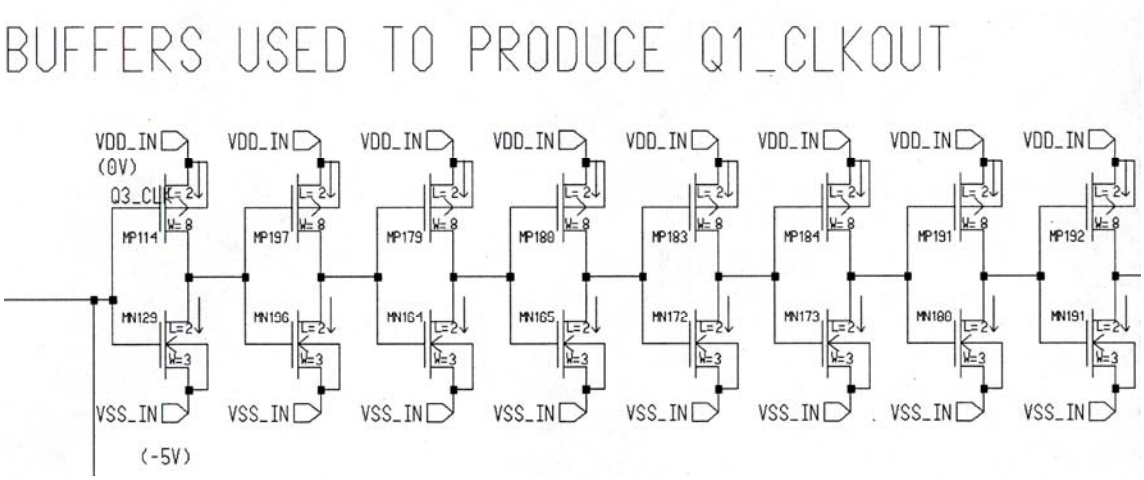
APPENDIX 15: CLOCK SCHEMATICS



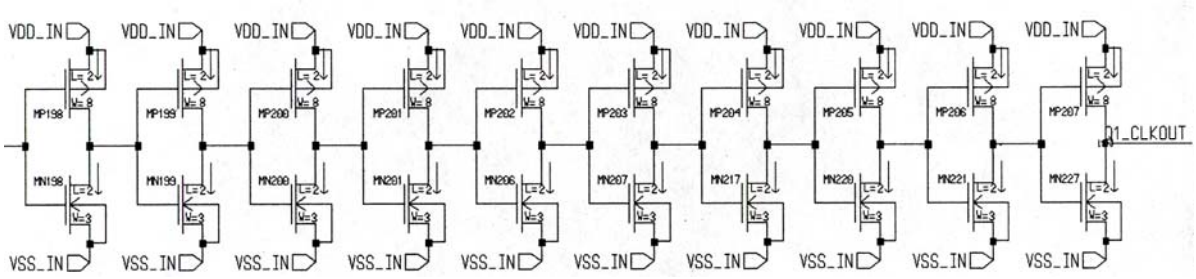
Overall views for clock tree were impractical to acquire so what follows in this appendix is expanded views zeroing in on the actual circuit portions of the clock tree. Here is shown as expanded view of the TMRSAFF clock input with its tri-state inverter input followed by an 8/3 inverter to create clock signal Q1_CLK which drives the first input SAFF of the TMRSAFF.



Expanded view of clock tree where a pair of 8/3 inverters (8/3 buffer) derives clock signal Q2_CLK from clock signal Q1_CLK. Q2_CLK drives the second input SAFF of the TMRSAFF. This arrangement is also used to create clock signal Q3_CLK from clock signal Q2_CLK. Q3_CLK drives the third input SAFF of the TMRSAFF.



Expanded view of four out of nine 8/3 buffers used to derive clock signal Q1_CLKOUT which drives the output SAFF's of the TMRSAFF.



Expanded view of the last five out of nine 8/3 buffers used to derive clock signal Q1_CLKOUT.

APPENDIX 16: TMRSAFF SPICE NETLIST

```
*
* .CONNECT statements
*
.CONNECT GND 0


* ELDO netlist generated with ICnet by 'memartin' on Tue Jan 31 2006 at 16:45:45

*
* MAIN CELL: Component pathname : $HOME/da/ff31
*
      MP39 RB2_2 Q2_CLK VDD_IN VDD_IN p L=2u W=8u
      MP94 A QO_2 N$69 VDD_IN p L=2u W=8u
      MP151 N$160 Q0_11 VDD_IN VDD_IN p L=2u W=8u
      R8 O N$161 hr 12k
      MN205 N$146 Q0_22 K VSS_IN n L=2u W=3u
      MP52 Q1_2 RB1_2 VDD_IN VDD_IN p L=2u W=8u
      R1 N$388 INPUT_D1 hr 12k
      R19 A1 MAJ_OUT hr 12k
      MN220 N$14402 N$14399 VSS_IN VSS_IN n L=2u W=3u
      MP205 N$14402 N$14399 VDD_IN VDD_IN p L=2u W=8u
      MN217 N$14399 N$14196 VSS_IN VSS_IN n L=2u W=3u
      MN82 RB1_3 SB2_3 N$46 VSS_IN n L=2u W=9u
      MP221 RB2_1OUT2 SB2_1OUT2 VDD_IN VDD_IN p L=2u W=8u
      MP24 N$15 NOR4 VDD_IN VDD_IN p L=2u W=11u
      MP113 N$11936 INPUT_D1 VDD_IN VDD_IN p L=2u W=29u
      MP99 N$12756 MAJ_OUT2 VDD_IN VDD_IN p L=2u W=21u
      MN144 N$320 Q2_Q3_DIFF2 VSS_IN VSS_IN n L=2u W=3u
      MN223 N$262 Q0_32 VSS_IN VSS_IN n L=2u W=3u
      MN114 A Q0_3 N$66 VSS_IN n L=2u W=3u
      MP17 Q0_1 SB1_1 VDD_IN VDD_IN p L=2u W=8u
      MP64 A QO_2 N$71 VDD_IN p L=2u W=8u
      MN11 SB2_1 RB2_1 N$3 VSS_IN n L=2u W=9u
      MP127 A1 A VDD_IN VDD_IN p L=2u W=21u
      MP185 Q0_1OUT SB1_1OUT VDD_IN VDD_IN p L=2u W=34u
      R4 F Q1_Q2_DIFF hr 12k
      MP160 N$185 FF_ENB N$15426 VDD_IN p L=2u W=16u
      MP159 N$314 Q2_Q3_DIFF VDD_IN VDD_IN p L=2u W=8u
      MN54 N$216 SB2_2 VSS_IN VSS_IN n L=2u W=3u
      MN80 SB1_3 RB1_3 N$45 VSS_IN n L=2u W=9u
      MP204 N$14399 N$14196 VDD_IN VDD_IN p L=2u W=8u
      MN9 N$3 INPUT_D1 N$19 VSS_IN n L=2u W=9u
      MP38 SB2_2 RB1_2 VDD_IN VDD_IN p L=2u W=8u
      MP109 N$370 FF_ENB N$333 VDD_IN p L=2u W=16u
```

MN70 Q2_22 N$217 VSS_IN VSS_IN n L=2u W=3u
MP120 N$382 INPUT_D3 VDD_IN VDD_IN p L=2u W=29u
MN193 N$7749 MAJ_OUT2 N$7748 VSS_IN n L=2u W=9u
MN242 RB1_1OUT2 SB1_1OUT2 N$7750 VSS_IN n L=2u W=9u
MN227 Q1_CLKOUT N$14606 VSS_IN VSS_IN n L=2u W=3u
MP207 Q1_CLKOUT N$14606 VDD_IN VDD_IN p L=2u W=8u
R20 N$501 N$15224 hr 12k
MP201 N$12963 N$12960 VDD_IN VDD_IN p L=2u W=8u
R16 INPUT_D3 N$12548 hr 12k
MP51 QO_2 Q2_22 N$36 VDD_IN p L=2u W=11u
MP175 RB2_1OUT Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MP62 N$355 N$276 VDD_IN VDD_IN p L=2u W=8u
MP104 Q2_CLK N$72 VDD_IN VDD_IN p L=2u W=8u
MN30 Q0_11 Q1_11 N$16 VSS_IN n L=2u W=4u
MP122 N$350 Q0_3 I VDD_IN p L=2u W=3u
MN157 N$398 N$15224 N$396 VSS_IN n L=2u W=9u
MP15 N$10 RB2_1 VDD_IN VDD_IN p L=2u W=16u
MP36 RB1_2 SB1_2 VDD_IN VDD_IN p L=2u W=8u
MN83 RB1_3 SB1_3 N$46 VSS_IN n L=2u W=9u
MP218 SB2_1OUT2 Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MN150 N$392 N$15224 N$390 VSS_IN n L=2u W=9u
MP133 C Q0_22 N$118 VDD_IN p L=2u W=8u
MN147 N$344 D3 VSS_IN VSS_IN n L=2u W=6u
MN51 RB2_2 SB1_2 N$26 VSS_IN n L=2u W=9u
MP95 N$70 Q0_3 VDD_IN VDD_IN p L=2u W=8u
MP165 N$317 Q1_Q2_DIFF2 VDD_IN VDD_IN p L=2u W=8u
MP149 N$262 Q0_32 VDD_IN VDD_IN p L=2u W=8u
MN5 SB1_1 RB2_1 N$1 VSS_IN n L=2u W=9u
R22 N$12756 N$15222 hr 12k
R21 N$12754 MAJ_OUT2 hr 12k
MP129 C Q0_22 N$116 VDD_IN p L=2u W=8u
MN37 N$355 N$136 E VSS_IN n L=2u W=3u
MN8 N$19 Q1_CLK VSS_IN VSS_IN n L=2u W=9u
MP190 Q1_11OUT Q0_1OUT N$416 VDD_IN p L=2u W=45u
MN178 Q1_11OUT Q0_1OUT N$526 VSS_IN n L=2u W=17u
MN176 N$531 SB1_1OUT VSS_IN VSS_IN n L=2u W=17u
MN201 N$12963 N$12960 VSS_IN VSS_IN n L=2u W=3u
MN183 N$388 N$370 VSS_IN VSS_IN n L=2u W=11u
MN244 N$513 Q0_1OUT VSS_IN VSS_IN n L=2u W=3u
MN153 RB1_1OUT SB2_1OUT N$392 VSS_IN n L=2u W=9u
MN156 N$397 MAJ_OUT N$396 VSS_IN n L=2u W=9u
MP203 N$14196 N$13167 VDD_IN VDD_IN p L=2u W=8u
MN65 Q1_2 Q0_22 N$39 VSS_IN n L=2u W=4u
MP134 J N$163 VDD_IN VDD_IN p L=2u W=34u
MP43 N$29 SB2_2 VDD_IN VDD_IN p L=2u W=16u
MN75 N$68 QO_2 VSS_IN VSS_IN n L=2u W=3u

MN138 A1 A VSS_IN VSS_IN n L=2u W=8u
MN196 N$8411 N$8413 VSS_IN VSS_IN n L=2u W=3u
MN16 NOR1 SB2_1 VSS_IN VSS_IN n L=2u W=3u
MP123 N$140 Q0_1 VDD_IN VDD_IN p L=2u W=8u
MN221 N$14606 N$14402 VSS_IN VSS_IN n L=2u W=3u
MP206 N$14606 N$14402 VDD_IN VDD_IN p L=2u W=8u
MP21 N$13 NOR1 VDD_IN VDD_IN p L=2u W=11u
MP132 N$118 Q0_11 VDD_IN VDD_IN p L=2u W=8u
MP128 N$116 Q0_32 VDD_IN VDD_IN p L=2u W=8u
MN197 J N$163 VSS_IN VSS_IN n L=2u W=13u
MN15 NOR1 SB1_1 VSS_IN VSS_IN n L=2u W=3u
MP174 SB2_1OUT RB1_1OUT VDD_IN VDD_IN p L=2u W=8u
MP170 RB1_1OUT Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MP138 N$146 N$143 K VDD_IN p L=2u W=3u
MN129 N$8413 Q3_CLK VSS_IN VSS_IN n L=2u W=3u
MN229 P N$161 VSS_IN VSS_IN n L=2u W=13u
MN104 N$61 RB1_3 VSS_IN VSS_IN n L=2u W=4u
MP176 RB2_1OUT SB2_1OUT VDD_IN VDD_IN p L=2u W=8u
MN202 N$143 Q0_22 VSS_IN VSS_IN n L=2u W=3u
MP181 N$408 RB2_1OUT VDD_IN VDD_IN p L=2u W=32u
MN154 RB1_1OUT SB1_1OUT N$392 VSS_IN n L=2u W=9u
MN173 N$9240 N$9237 VSS_IN VSS_IN n L=2u W=3u
MP230 Q1_11OUT2 RB1_1OUT2 VDD_IN VDD_IN p L=2u W=34u
MN166 N$267 Q0_3 VSS_IN VSS_IN n L=2u W=3u
MN52 RB2_2 SB2_2 N$26 VSS_IN n L=2u W=9u
MP98 N$245 Q0_3 VDD_IN VDD_IN p L=2u W=8u
MN86 N$49 INPUT_DB3 N$47 VSS_IN n L=2u W=9u
MN87 SB2_3 RB2_3 N$48 VSS_IN n L=2u W=9u
MP68 RB1_3 SB1_3 VDD_IN VDD_IN p L=2u W=8u
MN28 N$14 RB1_1 VSS_IN VSS_IN n L=2u W=4u
MP155 N$12754 C VDD_IN VDD_IN p L=2u W=21u
MP13 N$8 RB2_1 VDD_IN VDD_IN p L=2u W=16u
MP191 N$11315 N$9240 VDD_IN VDD_IN p L=2u W=8u
MN251 RB2_1OUT2 SB2_1OUT2 N$7760 VSS_IN n L=2u W=9u
MN249 N$174 Q1_Q3_DIFF VSS_IN VSS_IN n L=2u W=3u
MN226 N$160 Q0_32 O VSS_IN n L=2u W=3u
MN222 N N$154 VSS_IN VSS_IN n L=2u W=11u
MP233 N$7786 Q0_1OUT2 VDD_IN VDD_IN p L=2u W=8u
MP202 N$13167 N$12963 VDD_IN VDD_IN p L=2u W=8u
MP194 SB1_1OUT2 RB2_1OUT2 VDD_IN VDD_IN p L=2u W=8u
MP147 N$348 N$291 VDD_IN VDD_IN p L=2u W=8u
MP224 NOR1OUT2 SB1_1OUT2 N$7764 VDD_IN p L=2u W=16u
MP223 N$7764 SB2_1OUT2 VDD_IN VDD_IN p L=2u W=16u
MP75 N$52 SB2_3 VDD_IN VDD_IN p L=2u W=16u
MN36 N$134 Q0_1 VSS_IN VSS_IN n L=2u W=3u
MP23 Q0_11 SB2_1 VDD_IN VDD_IN p L=2u W=8u

MP37 SB2_2 Q2_CLK VDD_IN VDD_IN p L=2u W=8u
MN77 N$44 Q3_CLK VSS_IN VSS_IN n L=2u W=9u
MN38 N$134 QO_2 E VSS_IN n L=2u W=3u
MP135 N$143 Q0_22 VDD_IN VDD_IN p L=2u W=8u
MP189 N$416 NOR1OUT VDD_IN VDD_IN p L=2u W=45u
MP173 SB2_1OUT Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MN159 SB2_1OUT RB1_1OUT N$397 VSS_IN n L=2u W=9u
MP121 N$267 Q0_3 VDD_IN VDD_IN p L=2u W=8u
MN215 N$114 Q0_11 VSS_IN VSS_IN n L=2u W=3u
MP2 SB1_1 RB2_1 VDD_IN VDD_IN p L=2u W=8u
MP164 N$342 D3 VDD_IN VDD_IN p L=2u W=16u
MN257 Q0_1OUT2 Q1_11OUT2 N$7777 VSS_IN n L=2u W=17u
MP229 Q0_1OUT2 Q1_11OUT2 N$7774 VDD_IN p L=2u W=45u
MP14 NOR3 RB1_1 N$8 VDD_IN p L=2u W=16u
MP166 N$320 Q2_Q3_DIFF2 VDD_IN VDD_IN p L=2u W=8u
MN34 N$18 RB2_1 VSS_IN VSS_IN n L=2u W=4u
MN59 N$34 RB1_2 VSS_IN VSS_IN n L=2u W=3u
MP86 Q1_3 Q0_3 N$60 VDD_IN p L=2u W=11u
MN245 N$7759 MAJ_OUT2 N$7758 VSS_IN n L=2u W=9u
MN243 N$7758 Q1_CLKOUT VSS_IN VSS_IN n L=2u W=9u
MP196 RB1_1OUT2 SB1_1OUT2 VDD_IN VDD_IN p L=2u W=8u
MN212 C Q0_11 N$112 VSS_IN n L=2u W=3u
MN40 N$22 INPUT_D2 N$21 VSS_IN n L=2u W=9u
MP192 N$11318 N$11315 VDD_IN VDD_IN p L=2u W=8u
MP97 F N$166 VDD_IN VDD_IN p L=2u W=29u
MN94 N$233 SB2_3 VSS_IN VSS_IN n L=2u W=3u
MP219 SB2_1OUT2 RB1_1OUT2 VDD_IN VDD_IN p L=2u W=8u
MN192 N$7748 Q1_CLKOUT VSS_IN VSS_IN n L=2u W=9u
MN207 N$14196 N$13167 VSS_IN VSS_IN n L=2u W=3u
MN121 N$72 Q1_CLK VSS_IN VSS_IN n L=2u W=3u
MN206 N$13167 N$12963 VSS_IN VSS_IN n L=2u W=3u
MP116 N$375 N$373 VDD_IN VDD_IN p L=2u W=29u
MN160 RB2_1OUT SB1_1OUT N$398 VSS_IN n L=2u W=9u
MN165 N$9235 N$9232 VSS_IN VSS_IN n L=2u W=3u
MN20 NOR3 RB2_1 VSS_IN VSS_IN n L=2u W=3u
MP47 N$33 RB2_2 VDD_IN VDD_IN p L=2u W=16u
MN171 NOR3OUT RB2_1OUT VSS_IN VSS_IN n L=2u W=6u
MP4 RB1_1 SB1_1 VDD_IN VDD_IN p L=2u W=8u
MN68 Q0_22 Q2_22 N$41 VSS_IN n L=2u W=4u
MN132 N$286 Q0_11 VSS_IN VSS_IN n L=2u W=3u
MN127 N$359 QO_2 VSS_IN VSS_IN n L=2u W=3u
MP141 L N$147 VDD_IN VDD_IN p L=2u W=29u
MN12 SB2_1 RB1_1 N$3 VSS_IN n L=2u W=9u
MN95 N$232 RB1_3 VSS_IN VSS_IN n L=2u W=3u
MP78 N$232 RB1_3 N$54 VDD_IN p L=2u W=16u
MN169 N$140 Q0_1 VSS_IN VSS_IN n L=2u W=3u

MN175 Q0_1OUT Q1_11OUT N$531 VSS_IN n L=2u W=17u
MN188 N$197 FF_EN N$344 VSS_IN n L=2u W=6u
MN261 N$7784 RB1_1OUT2 VSS_IN VSS_IN n L=2u W=17u
MN185 N$373 FF_EN N$337 VSS_IN n L=2u W=6u
MN96 N$232 RB2_3 VSS_IN VSS_IN n L=2u W=3u
MN108 Q1_32 N$233 VSS_IN VSS_IN n L=2u W=3u
MN116 N$245 Q0_3 VSS_IN VSS_IN n L=2u W=3u
MN189 N$12548 N$197 VSS_IN VSS_IN n L=2u W=11u
MP225 N$7768 RB2_1OUT2 VDD_IN VDD_IN p L=2u W=16u
R13 N$375 INPUT_D2 hr 12k
MN259 Q1_11OUT2 NOR1OUT2 VSS_IN VSS_IN n L=2u W=13u
MP152 N$160 N$262 O VDD_IN p L=2u W=3u
MP108 N$125 N$245 G VDD_IN p L=2u W=3u
MN252 NOR1OUT2 SB1_1OUT2 VSS_IN VSS_IN n L=2u W=3u
MP227 Q0_1OUT2 SB1_1OUT2 VDD_IN VDD_IN p L=2u W=34u
MN255 NOR3OUT2 RB2_1OUT2 VSS_IN VSS_IN n L=2u W=3u
MP45 N$31 RB2_2 VDD_IN VDD_IN p L=2u W=16u
MN162 NOR1OUT SB1_1OUT VSS_IN VSS_IN n L=2u W=3u
MN225 N$160 Q0_11 VSS_IN VSS_IN n L=2u W=3u
MP102 Q1_CLK N$185 VDD_IN VDD_IN p L=2u W=8u
MN35 N$136 QO_2 VSS_IN VSS_IN n L=2u W=3u
MN67 Q0_22 N$34 VSS_IN VSS_IN n L=2u W=3u
MP161 H N$169 VDD_IN VDD_IN p L=2u W=29u
MP53 N$38 N$216 VDD_IN VDD_IN p L=2u W=11u
MN72 N$43 RB2_2 VSS_IN VSS_IN n L=2u W=4u
MN128 N$358 N$359 VSS_IN VSS_IN n L=2u W=3u
MP177 N$402 SB2_1OUT VDD_IN VDD_IN p L=2u W=32u
MN60 N$34 RB2_2 VSS_IN VSS_IN n L=2u W=3u
MP61 N$276 Q0_1 VDD_IN VDD_IN p L=2u W=8u
MP193 SB1_1OUT2 Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MP42 N$216 SB1_2 N$27 VDD_IN p L=2u W=16u
R2 J Q1_Q3_DIFF hr 12k
MN253 NOR1OUT2 SB2_1OUT2 VSS_IN VSS_IN n L=2u W=3u
MN115 F N$166 VSS_IN VSS_IN n L=2u W=11u
MP172 N$177 Q1_Q3_DIFF2 VDD_IN VDD_IN p L=2u W=8u
MN31 N$16 SB2_1 VSS_IN VSS_IN n L=2u W=4u
MN62 QO_2 Q1_2 N$37 VSS_IN n L=2u W=4u
MN136 N$296 Q0_11 VSS_IN VSS_IN n L=2u W=3u
MP9 N$5 SB2_1 VDD_IN VDD_IN p L=2u W=16u
MP26 Q1_11 RB2_1 VDD_IN VDD_IN p L=2u W=8u
MN134 N$291 Q0_22 VSS_IN VSS_IN n L=2u W=3u
MN92 N$234 SB2_3 VSS_IN VSS_IN n L=2u W=3u
MP29 N$136 QO_2 VDD_IN VDD_IN p L=2u W=8u
MP142 N$268 Q0_32 VDD_IN VDD_IN p L=2u W=8u
MP19 Q0_1 Q1_11 N$12 VDD_IN p L=2u W=11u
MP25 Q0_11 Q1_1 N$15 VDD_IN p L=2u W=11u

MP6 SB2_1 RB1_1 VDD_IN VDD_IN p L=2u W=8u
MN1 N$2 Q1_CLK VSS_IN VSS_IN n L=2u W=9u
MP10 NOR1 SB1_1 N$5 VDD_IN p L=2u W=16u
MN78 N$45 INPUT_D3 N$44 VSS_IN n L=2u W=9u
MP31 N$355 QO_2 E VDD_IN p L=2u W=3u
MN22 NOR4 RB2_1 VSS_IN VSS_IN n L=2u W=3u
MN139 N$12756 MAJ_OUT2 VSS_IN VSS_IN n L=2u W=8u
MP82 N$58 N$232 VDD_IN VDD_IN p L=2u W=11u
R15 N$377 INPUT_DB2 hr 12k
MN122 Q2_CLK N$72 VSS_IN VSS_IN n L=2u W=3u
MN130 N$281 Q0_1 VSS_IN VSS_IN n L=2u W=3u
MP106 Q3_CLK N$73 VDD_IN VDD_IN p L=2u W=8u
MP101 N$15426 CLK VDD_IN VDD_IN p L=2u W=16u
MN17 NOR2 SB1_1 VSS_IN VSS_IN n L=2u W=3u
MP57 Q0_22 Q1_2 N$40 VDD_IN p L=2u W=11u
MP27 N$17 NOR2 VDD_IN VDD_IN p L=2u W=11u
MP76 N$233 SB1_3 N$52 VDD_IN p L=2u W=16u
MN213 N$113 Q0_22 VSS_IN VSS_IN n L=2u W=3u
MN170 N$140 Q0_3 I VSS_IN n L=2u W=3u
MN112 A Q0_3 N$67 VSS_IN n L=2u W=3u
MN191 N$11318 N$11315 VSS_IN VSS_IN n L=2u W=3u
MN182 N$370 FF_EN N$328 VSS_IN n L=2u W=6u
MN49 SB2_2 RB2_2 N$25 VSS_IN n L=2u W=9u
MP66 SB1_3 RB2_3 VDD_IN VDD_IN p L=2u W=8u
MN63 N$37 SB1_2 VSS_IN VSS_IN n L=2u W=4u
MN69 N$41 SB2_2 VSS_IN VSS_IN n L=2u W=4u
MN13 RB2_1 SB1_1 N$4 VSS_IN n L=2u W=9u
MN263 N$7786 Q0_1OUT2 VSS_IN VSS_IN n L=2u W=3u
MN79 N$46 INPUT_DB3 N$44 VSS_IN n L=2u W=9u
MN74 N$355 N$276 VSS_IN VSS_IN n L=2u W=3u
MN210 N$348 N$268 M VSS_IN n L=2u W=3u
MN149 N$391 MAJ_OUT N$390 VSS_IN n L=2u W=9u
MP73 N$50 SB2_3 VDD_IN VDD_IN p L=2u W=16u
MN27 Q1_1 Q0_11 N$14 VSS_IN n L=2u W=4u
MP11 N$6 SB2_1 VDD_IN VDD_IN p L=2u W=16u
MN174 Q0_1OUT NOR3OUT VSS_IN VSS_IN n L=2u W=13u
MP168 N$174 Q1_Q3_DIFF VDD_IN VDD_IN p L=2u W=8u
MN254 NOR3OUT2 RB1_1OUT2 VSS_IN VSS_IN n L=2u W=3u
MP226 NOR3OUT2 RB1_1OUT2 N$7768 VDD_IN p L=2u W=16u
MP139 N$286 Q0_11 VDD_IN VDD_IN p L=2u W=8u
MN216 C Q0_32 N$114 VSS_IN n L=2u W=3u
MN56 N$217 SB2_2 VSS_IN VSS_IN n L=2u W=3u
MN110 N$65 RB2_3 VSS_IN VSS_IN n L=2u W=4u
MN61 QO_2 N$111 VSS_IN VSS_IN n L=2u W=3u
MN93 N$233 SB1_3 VSS_IN VSS_IN n L=2u W=3u
R11 G N$169 hr 12k

MN18 NOR2 SB2_1 VSS_IN VSS_IN n L=2u W=3u
MP153 N$296 Q0_11 VDD_IN VDD_IN p L=2u W=8u
MN203 N$351 N$143 K VSS_IN n L=2u W=3u
MN50 SB2_2 RB1_2 N$25 VSS_IN n L=2u W=9u
MN164 N$9232 N$8411 VSS_IN VSS_IN n L=2u W=3u
MP81 Q0_3 SB1_3 VDD_IN VDD_IN p L=2u W=8u
MP110 N$359 QO_2 VDD_IN VDD_IN p L=2u W=8u
R12 L Q1_Q2_DIFF2 hr 12k
MN2 N$1 INPUT_D1 N$2 VSS_IN n L=2u W=9u
R5 E N$166 hr 12k
MP130 N$117 Q0_32 VDD_IN VDD_IN p L=2u W=8u
MN6 RB1_1 SB2_1 N$20 VSS_IN n L=2u W=9u
MN26 Q1_1 NOR1 VSS_IN VSS_IN n L=2u W=3u
MN21 NOR4 RB1_1 VSS_IN VSS_IN n L=2u W=3u
MP54 Q1_2 QO_2 N$38 VDD_IN p L=2u W=11u
MP100 N$358 Q0_3 G VDD_IN p L=2u W=3u
MP220 RB2_1OUT2 Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MP28 Q1_11 Q0_11 N$17 VDD_IN p L=2u W=11u
MN102 Q1_3 N$234 VSS_IN VSS_IN n L=2u W=3u
MN23 Q0_1 NOR3 VSS_IN VSS_IN n L=2u W=3u
MP12 NOR2 SB1_1 N$6 VDD_IN p L=2u W=16u
MN126 N$125 Q0_3 G VSS_IN n L=2u W=3u
MN239 SB1_1OUT2 RB2_1OUT2 N$7749 VSS_IN n L=2u W=9u
MN195 SB1_1OUT2 RB1_1OUT2 N$7749 VSS_IN n L=2u W=9u
MP7 RB2_1 Q1_CLK VDD_IN VDD_IN p L=2u W=8u
MP93 N$69 Q0_3 VDD_IN VDD_IN p L=2u W=8u
MP158 N$311 Q1_Q2_DIFF VDD_IN VDD_IN p L=2u W=8u
MN32 Q1_11 NOR2 VSS_IN VSS_IN n L=2u W=3u
MP186 N$414 NOR3OUT VDD_IN VDD_IN p L=2u W=45u
MN90 RB2_3 SB2_3 N$49 VSS_IN n L=2u W=9u
MP35 RB1_2 Q2_CLK VDD_IN VDD_IN p L=2u W=8u
R6 K N$147 hr 12k
MN179 N$526 RB1_1OUT VSS_IN VSS_IN n L=2u W=17u
MN146 N$337 D2 VSS_IN VSS_IN n L=2u W=6u
MN100 Q0_3 Q1_3 N$59 VSS_IN n L=2u W=4u
MP195 RB1_1OUT2 Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MP115 N$373 FF_ENB N$335 VDD_IN p L=2u W=16u
MP169 SB1_1OUT RB2_1OUT VDD_IN VDD_IN p L=2u W=8u
MP119 N$12548 N$197 VDD_IN VDD_IN p L=2u W=29u
MN7 RB1_1 SB1_1 N$20 VSS_IN n L=2u W=9u
MP50 N$36 N$111 VDD_IN VDD_IN p L=2u W=11u
MP92 Q1_32 Q0_32 N$64 VDD_IN p L=2u W=11u
MP18 N$12 NOR3 VDD_IN VDD_IN p L=2u W=11u
MP65 SB1_3 Q3_CLK VDD_IN VDD_IN p L=2u W=8u
MN118 N$358 N$245 G VSS_IN n L=2u W=3u
MP89 Q0_32 Q1_3 N$62 VDD_IN p L=2u W=11u

MN14 RB2_1 SB2_1 N$4 VSS_IN n L=2u W=9u
MN33 Q1_11 Q0_1 N$18 VSS_IN n L=2u W=4u
MN45 RB1_2 SB1_2 N$23 VSS_IN n L=2u W=9u
MN262 N$177 Q1_Q3_DIFF2 VSS_IN VSS_IN n L=2u W=3u
MN181 N$185 FF_EN N$131 VSS_IN n L=2u W=6u
MN177 Q1_11OUT NOR1OUT VSS_IN VSS_IN n L=2u W=13u
MP30 N$134 Q0_1 VDD_IN VDD_IN p L=2u W=8u
MN29 Q0_11 NOR4 VSS_IN VSS_IN n L=2u W=3u
MN89 RB2_3 SB1_3 N$49 VSS_IN n L=2u W=9u
MP117 N$377 INPUT_D2 VDD_IN VDD_IN p L=2u W=29u
MP114 N$8413 Q3_CLK VDD_IN VDD_IN p L=2u W=8u
MP77 N$54 RB2_3 VDD_IN VDD_IN p L=2u W=16u
MN224 N$352 N$262 O VSS_IN n L=2u W=3u
MN76 A Q0_1 N$68 VSS_IN n L=2u W=3u
MP22 Q1_1 Q0_1 N$13 VDD_IN p L=2u W=11u
MN19 NOR3 RB1_1 VSS_IN VSS_IN n L=2u W=3u
MP41 N$27 SB2_2 VDD_IN VDD_IN p L=2u W=16u
MN113 N$66 Q0_1 VSS_IN VSS_IN n L=2u W=3u
MN163 NOR1OUT SB2_1OUT VSS_IN VSS_IN n L=2u W=6u
MP180 N$9235 N$9232 VDD_IN VDD_IN p L=2u W=8u
MN107 N$63 SB2_3 VSS_IN VSS_IN n L=2u W=4u
MN172 N$9237 N$9235 VSS_IN VSS_IN n L=2u W=3u
MP40 RB2_2 SB2_2 VDD_IN VDD_IN p L=2u W=8u
R18 N Q2_Q3_DIFF2 hr 12k
MN186 N$375 N$373 VSS_IN VSS_IN n L=2u W=11u
MP131 C Q0_11 N$117 VDD_IN p L=2u W=8u
MN167 N$350 N$267 I VSS_IN n L=2u W=3u
MN42 SB1_2 RB1_2 N$22 VSS_IN n L=2u W=9u
MP46 N$111 RB1_2 N$31 VDD_IN p L=2u W=16u
MP145 N$153 N$268 M VDD_IN p L=2u W=3u
MP124 N$140 N$267 I VDD_IN p L=2u W=3u
MN73 N$276 Q0_1 VSS_IN VSS_IN n L=2u W=3u
MN10 N$4 INPUT_DB1 N$19 VSS_IN n L=2u W=9u
MP111 N$388 N$370 VDD_IN VDD_IN p L=2u W=29u
MN190 N$382 INPUT_D3 VSS_IN VSS_IN n L=2u W=11u
MN117 N$12754 C VSS_IN VSS_IN n L=2u W=8u
MP148 N N$154 VDD_IN VDD_IN p L=2u W=29u
MP140 N$351 N$286 VDD_IN VDD_IN p L=2u W=8u
MP187 Q0_1OUT Q1_11OUT N$414 VDD_IN p L=2u W=45u
MN250 RB2_1OUT2 SB1_1OUT2 N$7760 VSS_IN n L=2u W=9u
MP184 N$9240 N$9237 VDD_IN VDD_IN p L=2u W=8u
MP183 N$9237 N$9235 VDD_IN VDD_IN p L=2u W=8u
MP103 N$72 Q1_CLK VDD_IN VDD_IN p L=2u W=8u
MN41 N$23 INPUT_DB2 N$21 VSS_IN n L=2u W=9u
MN124 Q3_CLK N$73 VSS_IN VSS_IN n L=2u W=3u
MN103 Q1_3 Q0_32 N$61 VSS_IN n L=2u W=4u

MN135 N$348 N$291 VSS_IN VSS_IN n L=2u W=3u
MP232 Q1_11OUT2 Q0_1OUT2 N$7781 VDD_IN p L=2u W=45u
MN145 N$328 D1 VSS_IN VSS_IN n L=2u W=6u
MN106 Q0_32 Q1_32 N$63 VSS_IN n L=2u W=4u
MP56 N$40 N$34 VDD_IN VDD_IN p L=2u W=11u
MN47 N$25 INPUT_D2 N$24 VSS_IN n L=2u W=9u
MN199 N$11525 N$11522 VSS_IN VSS_IN n L=2u W=3u
MP199 N$11525 N$11522 VDD_IN VDD_IN p L=2u W=8u
MP63 N$71 Q0_1 VDD_IN VDD_IN p L=2u W=8u
MP105 N$73 Q2_CLK VDD_IN VDD_IN p L=2u W=8u
MN214 C Q0_32 N$113 VSS_IN n L=2u W=3u
MN218 N$153 Q0_22 VSS_IN VSS_IN n L=2u W=3u
MN168 NOR3OUT RB1_1OUT VSS_IN VSS_IN n L=2u W=3u
MP143 N$348 Q0_32 M VDD_IN p L=2u W=3u
MN187 N$377 INPUT_D2 VSS_IN VSS_IN n L=2u W=11u
MN219 N$153 Q0_32 M VSS_IN n L=2u W=3u
MN71 Q2_22 QO_2 N$43 VSS_IN n L=2u W=4u
MP144 N$153 Q0_22 VDD_IN VDD_IN p L=2u W=8u
MN98 N$231 RB2_3 VSS_IN VSS_IN n L=2u W=3u
MN241 RB1_1OUT2 SB2_1OUT2 N$7750 VSS_IN n L=2u W=9u
MP88 N$62 N$231 VDD_IN VDD_IN p L=2u W=11u
MN101 N$59 SB1_3 VSS_IN VSS_IN n L=2u W=4u
MP197 N$8411 N$8413 VDD_IN VDD_IN p L=2u W=8u
MP125 N$281 Q0_1 VDD_IN VDD_IN p L=2u W=8u
MP167 SB1_1OUT Q1_CLKOUT VDD_IN VDD_IN p L=2u W=8u
MN208 L N$147 VSS_IN VSS_IN n L=2u W=11u
MN25 N$179 SB1_1 VSS_IN VSS_IN n L=2u W=4u
MN39 N$21 Q2_CLK VSS_IN VSS_IN n L=2u W=9u
MN152 SB1_1OUT RB2_1OUT N$391 VSS_IN n L=2u W=9u
MN97 N$231 RB1_3 VSS_IN VSS_IN n L=2u W=3u
MP34 SB1_2 RB2_2 VDD_IN VDD_IN p L=2u W=8u
MP90 Q1_32 RB2_3 VDD_IN VDD_IN p L=2u W=8u
MN46 N$24 Q2_CLK VSS_IN VSS_IN n L=2u W=9u
MP162 N$333 D1 VDD_IN VDD_IN p L=2u W=16u
R3 I N$163 hr 12k
MN99 Q0_3 N$232 VSS_IN VSS_IN n L=2u W=3u
MN3 N$20 INPUT_DB1 N$2 VSS_IN n L=2u W=9u
MP179 N$9232 N$8411 VDD_IN VDD_IN p L=2u W=8u
MN44 RB1_2 SB2_2 N$23 VSS_IN n L=2u W=9u
MP59 N$42 N$217 VDD_IN VDD_IN p L=2u W=11u
MN58 N$111 RB2_2 VSS_IN VSS_IN n L=2u W=3u
MN55 N$217 SB1_2 VSS_IN VSS_IN n L=2u W=3u
R7 M N$154 hr 12k
MN137 N$352 N$296 VSS_IN VSS_IN n L=2u W=3u
MP60 Q2_22 Q0_22 N$42 VDD_IN p L=2u W=11u
MP84 Q1_3 RB1_3 VDD_IN VDD_IN p L=2u W=8u

MP33 SB1_2 Q2_CLK VDD_IN VDD_IN p L=2u W=8u
MP1 SB1_1 Q1_CLK VDD_IN VDD_IN p L=2u W=8u
MP188 Q1_11OUT RB1_1OUT VDD_IN VDD_IN p L=2u W=34u
MP154 N$352 N$296 VDD_IN VDD_IN p L=2u W=8u
MP222 N$513 Q0_1OUT VDD_IN VDD_IN p L=2u W=8u
MP72 RB2_3 SB2_3 VDD_IN VDD_IN p L=2u W=8u
MP182 NOR3OUT RB1_1OUT N$408 VDD_IN p L=2u W=16u
MN198 N$11522 N$11318 VSS_IN VSS_IN n L=2u W=3u
MP44 N$217 SB1_2 N$29 VDD_IN p L=2u W=16u
MP171 RB1_1OUT SB1_1OUT VDD_IN VDD_IN p L=2u W=8u
MP85 N$60 N$234 VDD_IN VDD_IN p L=2u W=11u
MP3 RB1_1 Q1_CLK VDD_IN VDD_IN p L=2u W=8u
MN24 Q0_1 Q1_1 N$179 VSS_IN n L=2u W=4u
MP49 QO_2 SB1_2 VDD_IN VDD_IN p L=2u W=8u
MN4 SB1_1 RB1_1 N$1 VSS_IN n L=2u W=9u
R10 N$11936 INPUT_DB1 hr 12k
MN142 N$314 Q2_Q3_DIFF VSS_IN VSS_IN n L=2u W=3u
MN125 N$125 QO_2 VSS_IN VSS_IN n L=2u W=3u
MN105 Q0_32 N$231 VSS_IN VSS_IN n L=2u W=3u
MN131 N$350 N$281 VSS_IN VSS_IN n L=2u W=3u
MN85 N$48 INPUT_D3 N$47 VSS_IN n L=2u W=9u
MP80 N$231 RB1_3 N$56 VDD_IN p L=2u W=16u
MN91 N$234 SB1_3 VSS_IN VSS_IN n L=2u W=3u
MN240 H N$169 VSS_IN VSS_IN n L=2u W=11u
MN81 SB1_3 RB2_3 N$45 VSS_IN n L=2u W=9u
MP146 N$291 Q0_22 VDD_IN VDD_IN p L=2u W=8u
MP16 NOR4 RB1_1 N$10 VDD_IN p L=2u W=16u
MP48 N$34 RB1_2 N$33 VDD_IN p L=2u W=16u
MP83 Q0_3 Q1_32 N$58 VDD_IN p L=2u W=11u
MP74 N$234 SB1_3 N$50 VDD_IN p L=2u W=16u
MP107 N$125 QO_2 VDD_IN VDD_IN p L=2u W=8u
MN133 N$351 N$286 VSS_IN VSS_IN n L=2u W=3u
MP58 Q2_22 RB2_2 VDD_IN VDD_IN p L=2u W=8u
MP69 SB2_3 Q3_CLK VDD_IN VDD_IN p L=2u W=8u
MN248 SB2_1OUT2 RB1_1OUT2 N$7759 VSS_IN n L=2u W=9u
MN247 SB2_1OUT2 RB2_1OUT2 N$7759 VSS_IN n L=2u W=9u
MP87 Q0_32 SB2_3 VDD_IN VDD_IN p L=2u W=8u
MP8 RB2_1 SB2_1 VDD_IN VDD_IN p L=2u W=8u
MN53 N$216 SB1_2 VSS_IN VSS_IN n L=2u W=3u
MN57 N$111 RB1_2 VSS_IN VSS_IN n L=2u W=3u
MN43 SB1_2 RB2_2 N$22 VSS_IN n L=2u W=9u
MP32 N$134 N$136 E VDD_IN p L=2u W=3u
MN204 N$146 Q0_11 VSS_IN VSS_IN n L=2u W=3u
MP136 N$351 Q0_22 K VDD_IN p L=2u W=3u
MN143 N$317 Q1_Q2_DIFF2 VSS_IN VSS_IN n L=2u W=3u
MP5 SB2_1 Q1_CLK VDD_IN VDD_IN p L=2u W=8u

MP20 Q1_1 RB1_1 VDD_IN VDD_IN p L=2u W=8u
MP228 N$7774 NOR3OUT2 VDD_IN VDD_IN p L=2u W=45u
MN256 Q0_1OUT2 NOR3OUT2 VSS_IN VSS_IN n L=2u W=13u
MP198 N$11522 N$11318 VDD_IN VDD_IN p L=2u W=8u
MN211 N$112 Q0_22 VSS_IN VSS_IN n L=2u W=3u
MP157 N$501 MAJ_OUT VDD_IN VDD_IN p L=2u W=21u
MN88 SB2_3 RB1_3 N$48 VSS_IN n L=2u W=9u
MP126 N$350 N$281 VDD_IN VDD_IN p L=2u W=8u
MP79 N$56 RB2_3 VDD_IN VDD_IN p L=2u W=16u
MN48 N$26 INPUT_DB2 N$24 VSS_IN n L=2u W=9u
MN140 N$501 MAJ_OUT VSS_IN VSS_IN n L=2u W=8u
MN184 N$11936 INPUT_D1 VSS_IN VSS_IN n L=2u W=11u
MN246 N$7760 N$15222 N$7758 VSS_IN n L=2u W=9u
MN141 N$311 Q1_Q2_DIFF VSS_IN VSS_IN n L=2u W=3u
MN155 N$396 Q1_CLKOUT VSS_IN VSS_IN n L=2u W=9u
MP156 P N$161 VDD_IN VDD_IN p L=2u W=34u
MP70 SB2_3 RB1_3 VDD_IN VDD_IN p L=2u W=8u
MP71 RB2_3 Q3_CLK VDD_IN VDD_IN p L=2u W=8u
MN158 SB2_1OUT RB2_1OUT N$397 VSS_IN n L=2u W=9u
MN258 N$7777 SB1_1OUT2 VSS_IN VSS_IN n L=2u W=17u
MN66 N$39 RB1_2 VSS_IN VSS_IN n L=2u W=4u
MP150 N$352 Q0_32 O VDD_IN p L=2u W=3u
MN119 N$131 CLK VSS_IN VSS_IN n L=2u W=6u
R14 P Q1_Q3_DIFF2 hr 12k
MN148 N$390 Q1_CLKOUT VSS_IN VSS_IN n L=2u W=9u
MP118 N$197 FF_ENB N$342 VDD_IN p L=2u W=16u
MN64 Q1_2 N$216 VSS_IN VSS_IN n L=2u W=3u
MN120 Q1_CLK N$185 VSS_IN VSS_IN n L=2u W=3u
MN200 N$12960 N$11525 VSS_IN VSS_IN n L=2u W=3u
MP200 N$12960 N$11525 VDD_IN VDD_IN p L=2u W=8u
R17 INPUT_DB3 N$382 hr 12k
MP163 N$335 D2 VDD_IN VDD_IN p L=2u W=16u
MP91 N$64 N$233 VDD_IN VDD_IN p L=2u W=11u
MP112 N$358 N$359 VDD_IN VDD_IN p L=2u W=8u
MP55 Q0_22 SB2_2 VDD_IN VDD_IN p L=2u W=8u
MN109 Q1_32 Q0_3 N$65 VSS_IN n L=2u W=4u
MP67 RB1_3 Q3_CLK VDD_IN VDD_IN p L=2u W=8u
R9 H Q2_Q3_DIFF hr 12K
MN209 N$268 Q0_32 VSS_IN VSS_IN n L=2u W=3u
MP178 NOR1OUT SB1_1OUT N$402 VDD_IN p L=2u W=16u
MP137 N$146 Q0_11 VDD_IN VDD_IN p L=2u W=8u
MN151 SB1_1OUT RB1_1OUT N$391 VSS_IN n L=2u W=9u
MN123 N$73 Q2_CLK VSS_IN VSS_IN n L=2u W=3u
MN84 N$47 Q3_CLK VSS_IN VSS_IN n L=2u W=9u
MN161 RB2_1OUT SB2_1OUT N$398 VSS_IN n L=2u W=9u
MN194 N$7750 N$15222 N$7748 VSS_IN n L=2u W=9u

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MN180 N$11315 N$9240 VSS_IN VSS_IN n L=2u W=3u
MP96 A Q0_1 N$70 VDD_IN p L=2u W=8u
MN260 Q1_11OUT2 Q0_1OUT2 N$7784 VSS_IN n L=2u W=17u
MN111 N$67 QO_2 VSS_IN VSS_IN n L=2u W=3u
MP231 N$7781 NOR1OUT2 VDD_IN VDD_IN p L=2u W=45u
*
.end
```

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14. ABSTRACT

One of the more recently proposed flip-flop designs has been the sense amplifier flip-flop. It has gained acceptance in the commercial realm because of its power consumption, speed, setup time, clock line loading, and data line loading characteristics.

In this thesis, a recently designed RADHARD version of D sense amplifier flip-flop was taken and a triple mode redundant version for space and radiation environment use was created. The design was created with valuable options to increase radiation hardness and to give end users greater flexibility in realizing their own radiation hardened version of flip-flop. In addition, a methodology for using a traditional circuit simulation tool, SPICE, was developed to test the operation of the flip-flop design for both normal conditions and under the influence of radiation.

The prescribed level of radiation resilience was chosen to reflect the upper bound of radiation tolerant design which is equivalent to a 100MeV Fe ion interaction with Si.

This work provides the results of the design effort and the characteristics of the final triple mode redundant sense amplifier flip-flop design both as a device which did not utilize any of the options created for use with the design and with various combinations of options employed.

This work also provides information on a revolutionary technology coined by the author (S&IC Technology, Sensor and Integrated Circuit Technology) which when used in conjunction with the triple mode design of this work would realize a self-sensing, self-correcting, and self-repairing triple mode design which would be of immeasurable benefit to space applications, avionics, and terrestrial applications the world over.

15. SUBJECT TERMS

Triple Mode Redundancy, Self-Sensing, Self-Correcting, Self-Repairing, Radiation Tolerant, Sense Amplifier Flip-Flop

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