Modulator for 4-level Flying Capacitor Converter with Balancing Control in the Closed Loop

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Abstract — **This paper presents a modulator with an active voltage balancing control for the three-phase four-level FLC converter based electric motor drive for applications supplied directly from a 6 kV ac-grid. It describes a modulation algorithm of the FLC converter by using the phase shifted PWM modulation with balancing voltage of the flying capacitor by using P controllers in the closed loop. The proposed control was verified by experiments carried out on the down-scale drive prototype of the rated power of 35 kVA.**

Keywords — FLC, multilevel converter, medium-voltage converter, modulator, PWM, balancing, control, ac motor drive

I. Introduction

There are many papers reporting different topologies of multilevel converters and their control strategies [1]–[8]. This paper presents selected results of our research project, solved in cooperation with our industrial partner CKD Elektrotechnika targeting on a development of a new generation of a mining machine drive. The drive is considered to be supplied directly (i.e. without input transformer) from a 6 kV ac-grid and we have chosen the four-level flying capacitor topology for this task. The phase shifted PWM modulation (PS-PWM) with active balancing voltage of the FLC converter flying capacitor is based on [8] where the authors used PI controllers for voltage balancing (for more details see [8]). This paper is a follow-up to our previous publications [9], [10] and presents other possible way of the converter control of the developed four-level flying-capacitor based converter for medium-voltage high-power drives. The paper describes proposed modulation algorithm for the 4-level FLC inverter which is implemented into an FPGA unit. Proper function of the designed control system is verified by an extensive experimental study made on the developed converter/drive prototype.

II. Overview of Proposed Modulation Method for 4L-FLC Converters

This section deals with the phase shifted PWM modulation with active voltage balancing by using P controllers for the four-level flying capacitor converter (4L-FLC). Each phase of the developed down-scaled prototype of the three-phase 4L-FLC AC/DC/AC converter consists of two floating capacitors on the rectifier side and two capacitors on the inverter side and 12 IGBTs. A power circuit of the three-phase inverter is in Fig. 1. To achieve safe start-up and shut-down procedure it utilizes two relays. The first relay is used to bypass a pre-charge resistor on the rectifier side when pre-charging is completed and the converter is ready to run. The second relay has two opposite contacts, one for connecting rectifier to an ac power source and second contact for a quick discharge of the dc-link and flying capacitors to allow a fast restart procedure.

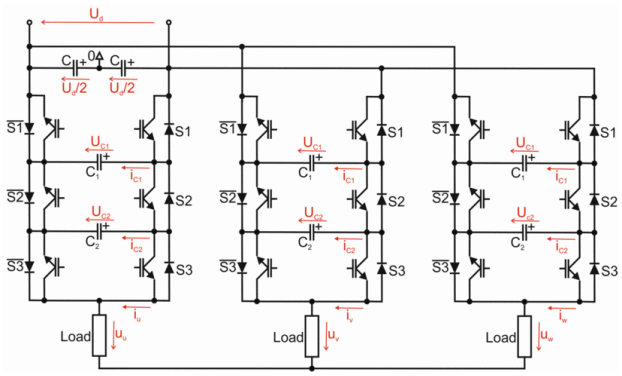

Fig. 1 Power circuit of the three-phase 4L-FLC inverter.

The phase shifted PWM modulation method uses natural balancing [5], [6], [7]. The value of each triangular signal is compared with the input modulation signal. In this case, controllers are used for proper balancing of the voltage on the capacitors. On each capacitor one controller is used. The block diagram of the balancing algorithm is shown in Fig. 2.

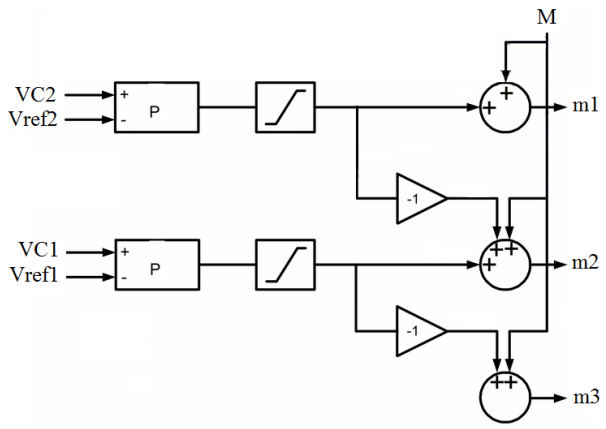

Fig. 2. Balancing control structure [8].

TELEN2016010
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Output of the controllers influence the modulation indexes for each transistor for reaching the balancing voltage of the flying capacitors. If the modulation index of the upper transistor is higher than the modulation index of the lower transistor, the flying capacitor between the upper and lower transistors will be charged, because the charging current is subtraction of the current through the upper and lower transistors.

III. Simulation Of 3 Phase 4L-FLC Converter

In contrast to paper [8], the PI controllers were replaced by proportional P controllers. If the input of the P-controller is zero, it means that the demanded voltage of the flying capacitor is equal to the measured voltage then the output of the P-controller will be zero. This fact means that the modulation signal will not be modified and the inverter voltage will not be distorted, then the converter will be balanced by the natural balancing, which is a good feature of the PS-PWM modulation. This is the reason for employment of the P controllers. Then our method in contrast to [8] was redesigned from the FLC H-bridge to the three-phase FLC inverter. The block diagram of the balancing of the flying capacitors control is shown in Fig. 2. The output signals of the balancing subsystem are multiplied by the modulation signal and the output is connected to the inputs of the phase shifted modulator. This method of the modulation of the FLC inverter was simulated in Simulink/PLECS due to better understanding of the system behaviour and to find out the suitable values of amplification of the P-controllers. The results of the simulation are shown in Fig. 3. Parameters used by simulation: U_{dc} = 600 V, three-phase *RL* load: R = 5 Ω, L = 20 mH, switching frequency f_s = 800 Hz.

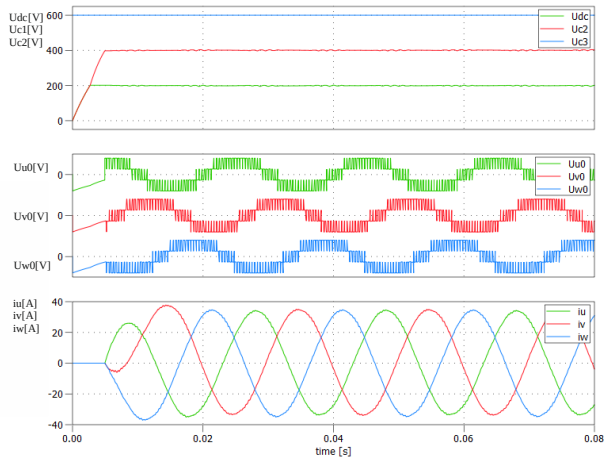

Fig. 3. Simulation results - voltage of the flying capacitors, three-phase voltage of the inverter, three-phase currents of the inverter with RL load.

IV. Implementation In FPGA

The structure of the control hardware is displayed in Fig. 4. This control system uses structure with the DSP and FPGA, where the DSP is the master control device, the FPGA works as a slave control device. All functions of the control algorithm are computed in the DSP. The DSP ensures measuring of voltage and currents. The measured data and the computed data are transmitted to the FPGA. The computed data are transmitted as two voltages, which represent the components of voltage space vectors for the inverter in the *XY* reference frame. The data are transmitted to the FPGA over a parallel bus. The FPGA performs generation of the pulses for transistors, balancing and precharging of the flying capacitors. The block diagram of the proposed modulator is shown in Fig. 5 (a suffix "*_16*" means that the input/output has 16 bit data resolution).

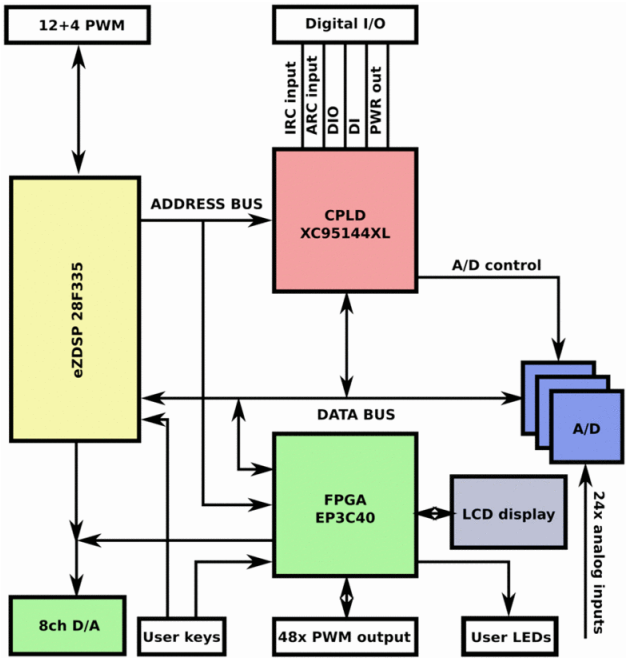

Fig. 4. A structure of a control hardware (MLC interface).

The *Register_In* entity transfers 16 bit data to outputs on each rising edge of the synchronization signal (*syn_D*). The data which are transferred are two components of the demanded voltage vector (*V_x_16*, *V_y_16*), the measured voltages of the flying capacitors (*V1a_16*,*V1b_16*, *V1c_16*, *V2a_16*, *V2b_16*, *V2c_16*), and the desired voltages of the flying capacitors (*V1a*_16*,*V1b*_16*, *V1c*_16*, *V2a*_16*, *V2b*_16*, *V2c*_16*).

The entity *Transformation* recalculates data from the *Register_In* entity (*Vx_16*, *Vy_16*) from the *XY* coordinates to the *ABC* coordinates. It means that the outputs (*Va_16*, *Vb_16*, *Vc_16*) are modulation signals for all three phases [9].

The modulation signal from the output of the *Transformation* entity is connected to the input of the *BalancingFLC* block (V_in_16). The measured and desired voltages (V1_s_16, V1*_s_16, V2_s_16, V2*_s_16) from the *Register_In* entity are connected to the inputs of this entity. The *BalancingFLC* entity uses proportional controllers for modification of the modulation signal for each transistor. If there is a demand on charging, the modulation index of the upper transistor will be higher than that of the lower transistor. If there is a demand on the discharging, the modulation index of the higher transistor will be lower than that of the lower transistor. The modulation signals are modulated in the *ModulatorFLC* entity.

The entity *ModulatorFLC* generates three triangular signals. The range of the value of the triangular signals is full range of the signed 16 bits integer type. The values of

TELEN2016010
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the triangular signals are compared with the values of the modulation signals from the entity *BalancingFLC (In1_16, In2_16, In3_16)* and the resulting signals from the output of the comparators are written on the outputs (*PWM1*, *PWM2*, *PWM3*).

The *PrechargingIogicFLC* block ensures the enabling of the precharging mode. In this case, the AC/DC/AC 4L-FLC converter was investigated. The precharging runs in the same time on the rectifier and inverter. After a start of the converter, it is necessary to measure the amplitude of the input voltage and from these voltage values are calculated demanded values of the flying capacitors for the precharging. All control functions of the precharging ensures the DSP. The function is switching the combination for charging C2 in Fig. 1; these are switches S1 and S2. Then the capacitors C2 will be charged through the diodes S3 of the rectifier side. If the C2 capacitors are charged on the demanded values, this is 1/3 U_{dc}, the DSP switches the combination for charging C1. For charging C1 there is necessary to switch the S1 switches. In this case the C1 capacitors will be charged trough the diodes S2 and S3 from the rectifier side. The *PrechargingIogicFLC* entity enables switching both transistors from the complementary pair at the same time. The precharging procedure is solved in detail in [11]. A CPLD circuit is placed behind the *PrechargingIogicFLC* which adds the dead-times for the IGBT transistors to the output signals from the FPGA.

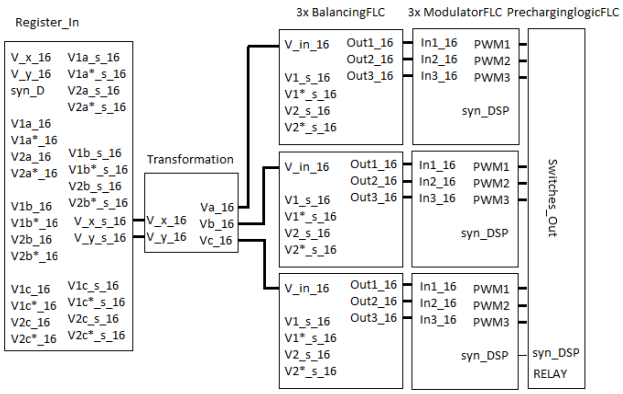

Fig. 5. Block structure of the proposed modulator (FPGA implementation).

V. Experimental Results

The developed laboratory converter prototype with the proposed control is shown in Fig. 6. The MLC interface which was used as the control system with the DSP and FPGA is shown in Fig. 7. The measured phase voltage, phase current and voltage of the flying capacitors are shown for a low frequency (lower than 8 Hz) and for a higher frequency (50 Hz). We have used an induction motor as a load. The switching frequency of the PWM was set to 800 Hz. The switching frequency appears to be three times higher in the phase voltage. That is 2.4 kHz. This phenomenon is caused by the chosen type of the modulation, which uses the three phase-shifted triangular signals per one switching period.

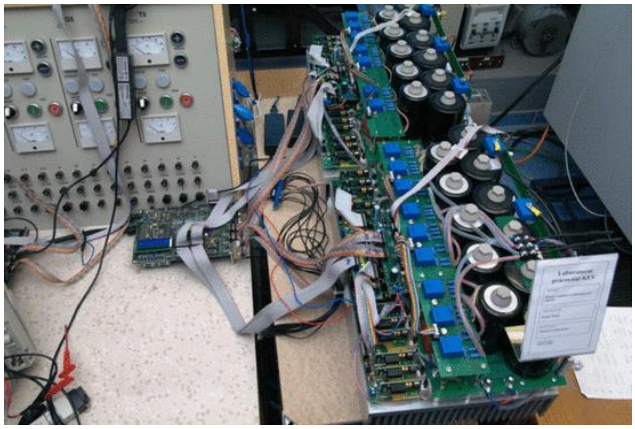

Fig. 6. The laboratory **4L-FLC AC/DC/AC** converter with **MLC**.

Fig. 7. **MLC interface** – control system with **DSP** and **FPGA**.

VI. Conlusions

This paper describes the proposed control of the 4-level FLC converter. We replaced the former PI controllers introduced in [8] by simple P controllers. The method was simulated in Simulink/PLECS. To support the simulation results, we tested the proposed control on the laboratory prototype of the drive with an induction motor and FLC four-level converter. The algorithm was implemented into the development board with the DSP and FPGA. The main benefit of this method is its simplicity and well understandable structure and the possibility of setting the parameters of the balancing controllers. Moreover, it could be easily extended to control converters with more voltage levels. If the amplification is set lower, the distortion of the inverter voltage will be lower, but balancing of the voltages of the flying capacitors will be worse. If the amplification is set higher, the balancing of the voltage of the flying capacitor will be better, but the distortion of the inverter voltage will be worse. The modulator implemented to the FPGA works correctly; selected experimental results are shown in Fig. 8 and Fig. 9. In the real applications it is necessary to check if the inverter is in the motor mode or generator mode. Because in the generator mode, the amplification values of the P controllers have to be used opposite. It means that in the generator mode the signs of the amplification values will be negative. It is simply implementable if the vector control of the machine is used, then according the polarity of the torque component of the stator current vector (i_{sq}),

TELEN2016010
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the polarity of the amplification of the balancing controllers could be changed. In the case if the machine is controlled without the vector control, the solution could be through the speed sensor of the induction machine and to check if the rotor speed is higher or lower than the stator frequency for the check of the mode for changing parameters of the balancing controllers.

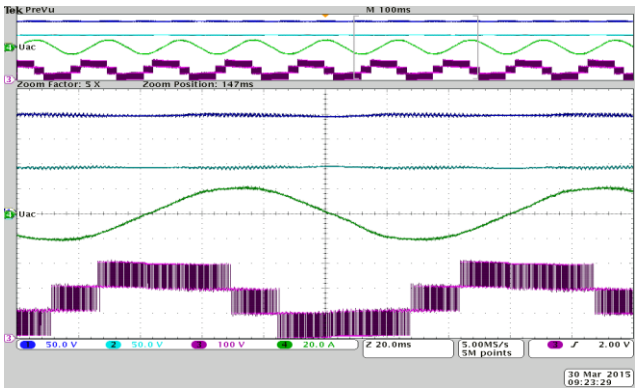

Fig. 8. Phase voltage, phase current and FLC voltage for converter output frequency of 8,3 Hz, Ch1: Capacitor voltage (C1) [50 V/d], Ch2: Capacitor voltage (C2) [50 V/d], Ch3: four-level line voltage of inverter [100 V/d], Ch4: inverter phase current [20 A/d].

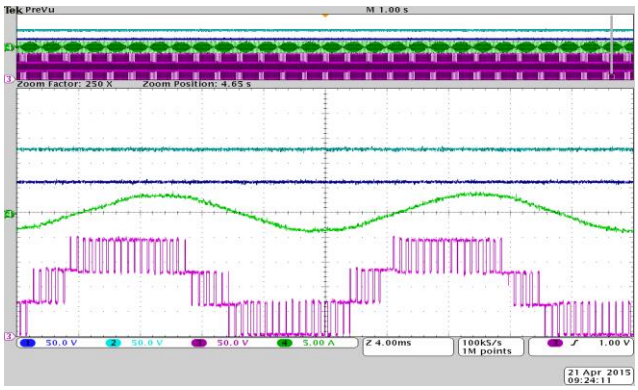

Fig. 9. Phase voltage, phase current and FLC voltage for converter output frequency of 50 Hz, Ch1: Capacitor voltage (C2) [50 V/d], Ch2: Capacitor voltage (C1) [50 V/d], Ch3: four-level line voltage of inverter [50 V/d], Ch4: inverter phase current [5 A/d].

VII. Acknowledgment

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