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Development of Multiport Single Stage Bidirectional Converter for Photovoltaic and Energy Storage Integration

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DEVELOPMENT OF MULTIPORT SINGLE STAGE BIDIRECTIONAL CONVERTER FOR PHOTOVOLTAIC AND ENERGY STORAGE INTEGRATION

by

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ABSTRACT

The energy market is on the verge of a paradigm shift as the emergence of renewable energy sources over traditional fossil fuel based energy supply has started to become cost competitive and viable. Unfortunately, most of the attractive renewable sources come with inherent challenges such as: intermittency and unreliability. This is problematic for today's stable, day ahead market based power system. Fortunately, it is well established that energy storage devices can compensate for renewable sources shortcomings. This makes the integration of energy storage with the renewable energy sources, one of the biggest challenges of modern distributed generation solution. This work discusses, the current state of the art of power conversion systems that integrate photovoltaic and battery energy storage systems. It is established that the control of bidirectional power flow to the energy storage device can be improved by optimizing its modulation and control. Traditional multistage conversion systems offers the required power delivery options, but suffers from a rigid power management system, reduced efficiency and increased cost. To solve this problem, a novel three port converter was developed which allows bidirectional power flow between the battery and the load, and unidirectional power flow from the photovoltaic port. The individual two-port portions of the three port converter were optimized in terms of modulation scheme. This leads to optimization of the proposed converter, for all possible power flow modes. In the second stage of the project, the three port converter was improved both in terms of cost and efficiency by proposing an improved topology. The improved three port converter has reduced functionality but is a perfect fit for the targeted microinverter application. The overall control system was designed to achieve improved reference tracking for power management and output AC voltage control. The bidirectional converter and both the proposed three port converters were analyzed theoretically. Finally, experimental prototypes were built to verify their performance.

Dedicated to my late parents, I wish you were here

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CHAPTER 1: INTRODUCTION

Renewable energy sources such as solar, wind etc are becoming predominant power sources in the modern age. They do not come with the negative environmental impact of traditional fossil fuel based energy sources. However, the main limitation of such green energy sources is their intermittent nature. Solar power is not available at night. During the day it is affected by natural, uncontrollable events such as varying solar irradiation, cloud cover etc. Similarly, wind flow is highly unpredictable and can not be modeled accurately. This gives rise to the need to use battery based energy storage systems in combination with the solar or wind energy sources to improve their reliability and dispatchability. The renewable energy dispatchability greatly influences its potential as a mainstream energy source to be used in a day ahead market. In order to allow such hybridized energy systems, multiport converters and multi stage two port converters are the only feasible way. The former type of power conversion system garnered major attention in recent years because of its high efficiency power conversion, reduced power conversion stages which directly results in high power density, reliability and lower cost. In this work, the existing state of the art of the multiport converter is reviewed and discussed in detail. An important part of the multiport conversion system is the bidirectional power flow control to and from the battery based energy storage system. The dual active bridge converter is one of the most popular choices for the bidirectional power flow control. Detailed analysis and optimization have been carried out on the dual active bridge converter both in order to fully understand it and improve its current performance level. Based on the depth of research available on dual active bridge converters, it is apparent that efficient modulation and control of the converter is still a challenge today. The main reason behind this is the multi-degrees of freedom control it offers. Because of this, generally an optimization based controller is best suited to navigate the control system towards a favorable operating point. This is often the most efficient operating point in terms of power conversion efficiency. Following this, building on the architecture of a dual active bridge two port DC-DC converter, a multi port converter has been proposed. It preserves the highly beneficial characteristics of a dual active

bridge such as high efficiency due to its ease of achieving soft switching operation, high power flow operation due to the bridge structure and simple control implementation because of its phase shift based modulation. The proposed multiport converter allows bidirectional power flow through any of its input or output ports, which provides high flexibility of operation. In addition to combining multiple input and output ports, the proposed converter integrates a DC-AC stage into the overall power conversion stage, removing the need for an additional power stage in a traditional multistage system. Thus the proposed converter falls into the class of microinverter family, while retaining its capability to interface multiple variable voltage DC sources. This feature is not available in today's commercial microinverters, which typically employs another front-end DC to DC converter to interface varying DC input voltage. After experimental verification, it was found that the proposed multiport converter system may not be cost effective for a low powered, residential solar plus battery application , due to the high number of active devices used. Based on this findings, in the second phase of the project, an improved three port converter is proposed which reduces the number of active devices by half, yet preserves the same soft switching/high efficiency conversion, control flexibility and wide power flow range operation. Both the proposed converters were simulated extensively using PSIM simulation software. The theoretical findings were validated in the Matlab environment. Subsequently, a hardware prototype for each of them was built and tested in an open loop configuration. The performance of each of the power converters were characterized and then validated against the theoretical predictions. The output AC load is typically assumed to be a standalone load. However, it can also be the power grid. Thus, the control of the output voltage, current or both is essential in this context. The improved three-port converter modulation was analyzed in details and a small signal model was developed which yields the open loop transfer function of the proposed converter. The small signal modeling was derived from the generalized average model proposed in the earlier literature intended to be used with single phase shift modulation of dual active bridge DC-DC converter. However this framework was modified for dual phase shift modulation(modulation scheme used in the proposed multiport converter) and also adapted to be used for DC-AC application. Following the model development, a feedback based closed loop

controller was developed and tested in the hardware prototype. The proposed controller aimed to maintain the AC output voltage peak at a desired set point. Additionally, the loop gains for the closed loop controller were designed specifically to reject the disturbances caused by varying input voltages of the solar or battery sources.

The dissertation is organized into 8 chapters with Chapter-1 being the introduction. Chapter-2 discusses the application of a solar plus storage system, with specific emphasis on "PV-firming" application. Chapter-3 discusses an extensive review of prior work on multiport converters, architecturally. In Chapter-4, the concept of dual active bridge and its optimization is introduced. Chapter-5 and 6 discusses the three port converter based on dual active bridge topology and the improved three port converter respectively. Chapter-7 elaborates on the small signal modeling and design of closed loop controller. Finally, the work is concluded in Chapter-8. Appendix-A provides pictures of the prototype. The related references of each part of the work are collected at the end of each chapter.

CHAPTER 2: INTEGRATED PHOTOVOLTAICS AND ENERGY STORAGE FOR PV FIRMING APPLICATION

As discussed in the introduction, the highly beneficial nature of photovoltaic (PV), and even with its ever decreasing cost, comes with some technical challenges which have limited its penetration into the grid. The most challenging one is its intermittent nature. Unless it is a clear sky, generally speaking, the sun light is highly influenced by cloud movement all day, causing the effective irradiation to vary continuously. Intermittent power generation is a challenging problem when supplying to a critical load as a non-firm, fluctuating power cannot sustain the critical nature of loads. As a result, when supplying the grid demand, PV power is often used as an intermediate or peak generation. Until recently this intermittency challenge posed a major obstacle to huge deployment of large PV systems. However, with the progress of energy storage technologies and more importantly, gradual decrease in their cost, this problem seems to have a solution in the horizon [1]. The irregular PV profile can be smoothed using a battery or other energy storage source. The concept revolves around the idea of supplying power at moments notice from the energy storage source during the time when PV output is suddenly decreased or increased heavily. This poses a risk at the load side because of its abnormal power output. Essentially, during an abrupt power increase the battery stores excess power and charges itself and during a sudden dip in PV power the battery discharges to provide for the power deficit. The process of PV capacity firming has attracted some attention recently [3]-[14]. Since the energy storage (battery storage) is an integrated aspect of the system, the impact of energy storage on the capacity firming is also a subject of much interest. However, most of the work in this area focuses on the different techniques used to smooth the PV profile, as little has been done to explore acceptable "firm" profiles. In this chapter, an effort has been made to understand the dispatchability of PV systems and the impact of energy storage controls on the performance of the PV system. This highlights key aspects of the system which can be controlled to enhance efficiency and reliability.

Traditionally, a moving average or ramp rate control (RRC) methods has been employed to firm the PV capacity [7]-[14]. In this work the ramp rate control has been improved to factor in the inefficiencies of the power conversion stage. In addition, the battery state-of-charge (SOC) is also actively controlled to prevent the battery from over charging or deep discharging during firming operation.

The architecture of a typical PV-Battery system requires either two separate power converters or a single three port converter to achieve a firm Profile. Both two converter or a single three port converter allows PV and battery side power management [23], [24]. In this work, the two converter approach has been adopted.

The dispatchability of PV and its intermittency is discussed in Section -II, the existing PV firming techniques are briefly discussed in Section-III, where the improved ramp rate control has been introduced. The proposed novel SOC controller is presented in Section III, while the combined RRC and SOC controller designs are given in Section-V. Finally, the results are discussed in Section-VI.

2.1 Dispatchable PV

Photovoltaics are one of the dominant distributed renewable sources in use today, which is gradually transforming the power grid. During the last decade, PV was deployed as an alternative energy resource and was mainly used for non-dispatchable generation, which prevented higher penetration of the PV into the grid [1]. However, In order to increase PV power systems penetration and reduce the energy loss by curtailing the energy spillage, energy storage can be employed as an attractive solution to the dispatchability problem, [1] - [3]. The unpredictable and unreliable nature of PV power can be complemented by energy storage to create predictable generation, which can be accepted in a "day ahead" energy market.

2.1.1 Intermittency of PV

The biggest drawback of PV power system is the intermittent nature due to ununiform irradiation through out the day. Various causes ranging from clouds passing as well as other weather conditions affect the solar irradiation which directly impacts the PV generated power [4, 5]. Although cloud passing may only affect a small geographical area, where PV plant spanning across vast geographical area tends to smooth out the effect of cloud passing, complete elimination of intermittency cannot be achieved [6].

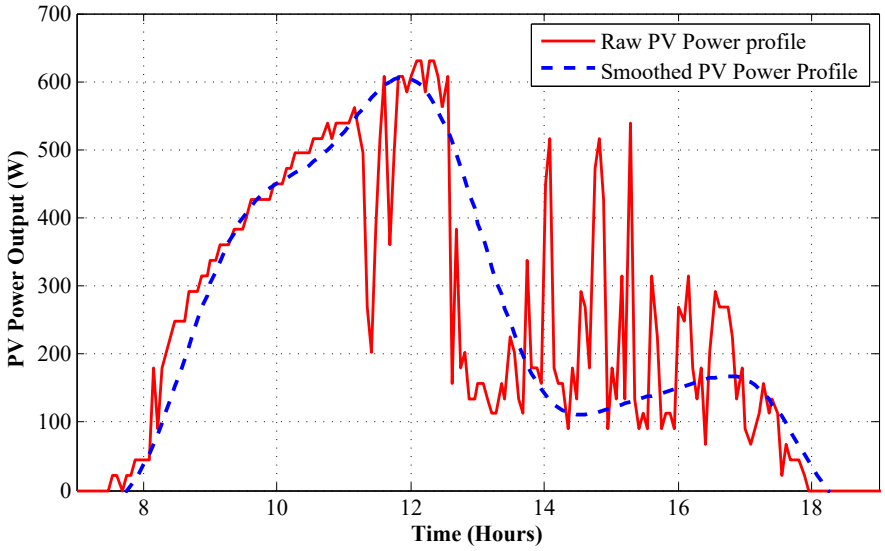

Figure 2.1: Typical PV power profile of a cloudy day

As evident from the Fig.2.1, the intermittent and oscillatory PV power profile can be used for a dispatchable generator if the profile is smoothed out to follow approximately the dotted profile using an energy storage device filling in the gaps. Naturally, as shown in Fig.2.1 it is clear that the energy storage must add or subtract power to the PV out put to make it dispatchable, therefore the energy storage device characterization is not only based on the voltage and power requirement, but also based on the efficiency of the bi-directional power converter connected to the DC bus.

From Fig.2.1, it is possible to calculate the amount of power lost in the conversion stage between

the battery and the DC bus by estimating the charge and discharge efficiency of the converter. When the smooth profile or the target profile is greater than the raw generation profile, the battery discharges and fills up the gap between them, and vice verse. The area under the curve for the battery profile can be multiplied by the respective efficiencies to obtain a time stamped plot for the loss, as shown in Fig.2.2. Therefore by accounting for the power loss due to the converter inefficiency, the battery size can be determined based on the charging and discharging capacity required for the battery storage to supply an economically dispachable load. The following equation can be used for calculating the battery size:

$$P_{Bat} = \eta_{dch} * (P_d - P_{PV}) + \eta_{ch} * (P_{PV} - P_d) \tag{2.1}$$

where, P_d is the dispatchable power, P_{PV} is PV power and η_{ch} and η_{dch} are the charging and discharging efficiencies of the power converter.

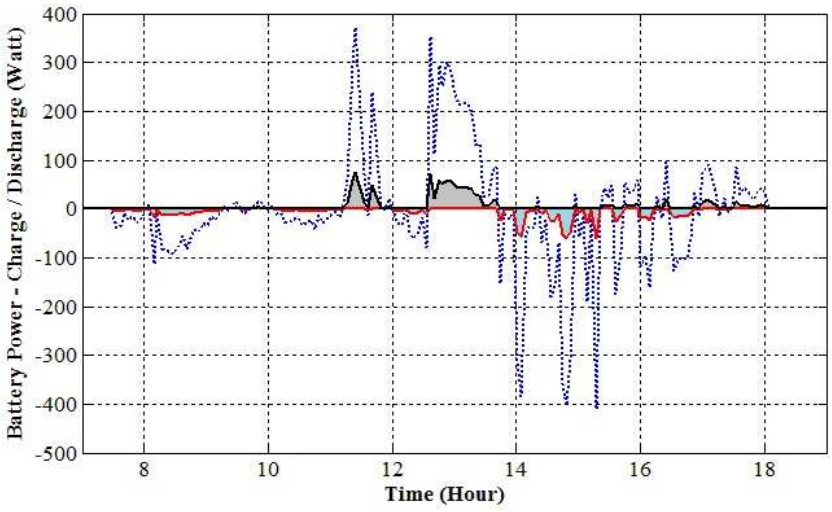

Figure 2.2: Battery charge and discharge power and losses

2.2 PV Capacity Firming

The disorderly profile of PV generation can be "firmed" by a number of control strategies as discussed in [7] - [11]. The central concept of these strategies is the "Ramp Rate" control of the PV power. The controller detects a sharp increase or decrease in PV power and employs the energy storage device to compensate or absorb the deficit or excess power. However, there are no clear guidelines to select the optimum ramp rate [13]. In an ideal scenario, when irradiance is maximum, the small intermittency will result in only very small ramp rates and hence doesn't give a good indication of what the ideal ramp rate should be. If a very accurate forecast of solar irradiation was available, the optimum ramp rate can be easily obtained by comparing the forecast to a dispatchable load profile. Some of the past work includes a "moving average" type algorithm which samples the PV output for a certain number of times and averages those samples to obtain a ramp rate set point. However, these types of algorithm generally depend on the sampling rate and past sample values and often leads to a completely different profile than expected. In addition, such algorithms can trigger the battery to charge or discharge even when there is no urgent need for that and the PV profile alone can maintain a dispatchable profile [12]. This in effect reduces system efficiency and reliability. Therefore, targeting a set ramp rate appears to be the best way to address present situation.

From the perspective of economy and sustainability of the system, it is important to keep in mind the size of the energy storage unit [12] - [14], the size of the critical local load (if any) to be supplied and the "day ahead" market requirements[15], when deciding the optimum ramp rate. As an example, in a fairly conservative market, the estimation of the ramp rate can be determined based on a maximum size of the battery and the mission critical load as described in the following equation:

$$\frac{dP_{ramp}}{dt} = \frac{d}{dt}(|P_L + P_G - P_{PV}|), \quad \int_{t_o}^{t_f} P_{ramp} dt \leq S_{Bat} \tag{2.2}$$

where, P_L is local critical load, P_G is the day ahead forecast of the market which corresponds to the power export to the grid. Referring to equation.(1), P_d can be represented as $P_d = P_L + P_G$. S_{Bat} is the total energy capacity of the battery, t_0 and t_f are the start and end time of the day. Based on the sampling window of the controller, the rate $\frac{dP_{ramp}}{dt}$ can be determined. Same data as shown in Fig.2.1 have been represented in Fig.2.3 with a conservative forecast and the ramp rate has been calculated from different battery capacities.

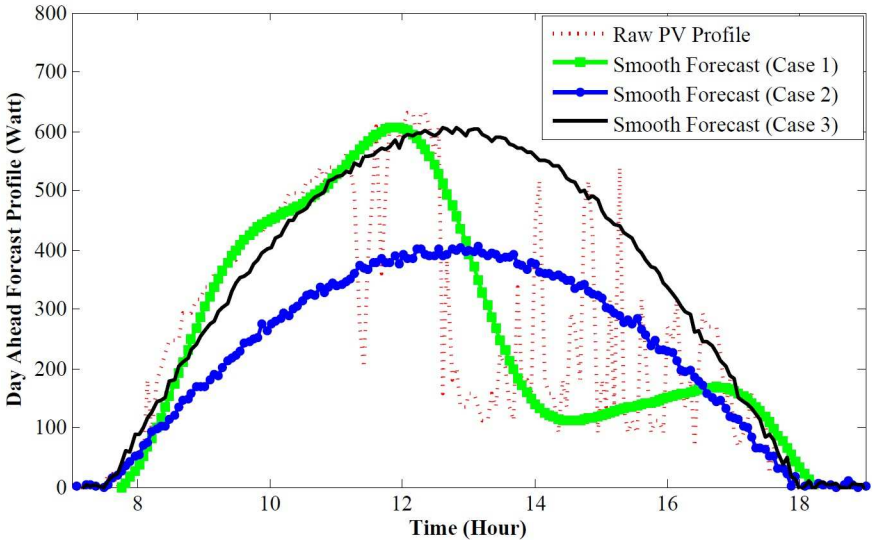

Figure 2.3: Day ahead forecast profiles

As evident from the figure, three forecast profiles have been shown. While case-2 is the most conservative one, case-1 is the closest to the raw PV profile. As a result, the battery size as well as the power loss due to inefficiencies are lowest for case-1. The analysis of the three cases are given in the following Table- 2.1.

As case-1 is very close to the actual PV data, the battery size is much smaller compared to case-2 and 3. Similarly the power loss is also less as the amount of charge and discharge required is naturally less. This gives an insight on how much the battery size and the ramp rate are based on

a given forecast profile. At the same time focus should be directed towards realizing a controller which forces the PV and battery system output to follow the raw PV profile closely so as to reduce the battery size and loss while at the same time "firming" the output to the extent it is dispatchable.

Case-2 is a moderate profile which has both charge and discharge cycle alternatively throughout the day. Therefore, the battery size is predominantly dictated by the the chosen ramp rate. whereas Case-3 has a peak that matches the raw PV profile, thus the battery is discharged in almost all of the intermittent cycles. In terms of system loss and maintaining adequate battery SOC till the end of the day, case-3 may not be the best choice. Yet, for off peak energy utilization, case-3 is perhaps the best option. Since the battery only discharges during day time, if the SOC at the start of the day is high and if the battery is properly sized, the SOC at the end of the day will reach a low enough value so that during the night, the battery can charge at off peak rate. However the battery size has to be increased to accommodate that. Also, it is to be noted that for the three cases, the battery capacity is given in "WH", so for a 10.5 hours solar day, the losses due to power conversion comes out to be $\leq 20\%$.

Table 2.1: Comparison of different forecase profiles

Ramp rate (W/min)	Energy storage size (Wh)	Loss (W)	Forecast case
12.5	806	6.3	Case-1
17.5	810	6.4	Case-1
22.5	772	6.3	Case-1
27.5	772	6.3	Case-1
37.5	767	6.2	Case-1
12.5	1456	11.4	Case-2
17.5	1453	11.3	Case-2
22.5	1452	11.3	Case-2
27.5	1446	11.28	Case-2
37.5	1441	11.26	Case-2
12.5	1438	13.1	Case-3
17.5	1443	13.1	Case-3
22.5	1447	13.2	Case-3
27.5	1448	13.15	Case-3
37.5	1448	13.22	Case-3

In case of a utility side load variation, values shown in Table-2.1 may change, therefore this work is limited with assumption that utility side demand is slowly varying compared to PV fluctuation.

2.3 State of Charge control(SOC)

Next, we focus on the storage element, which in this work, has been assumed to be a lithium ion battery. The charge and discharge model of a battery is straight forward and described below. The most important aspect of the dynamics of the battery storage in firm PV system is its capacity and rate of charge and discharge.

2.3.1 Battery Model

The electrical model for a battery is adequately described by a voltage source in series with a charging and discharging resistor which is parallel to the "polarization capacitance" and in series with the internal battery resistance as described in [16]-[18]. The state of charge and its estimation processes are described in [19]-[20]. Essentially, the state of charge is described by the following equation [19]

$$SOC(t) = \frac{\int_{t_0}^{t} I_b(\tau) d\tau}{Q_0} \tag{2.3}$$

Therefore if a measurement of the battery current is available, the SOC can be calculated as per (3). A discrete time representation of the (3)will be as follows:

$$\begin{aligned} SOC(k) = SOC(k-1) + \\ \frac{\frac{1}{2}\{I_b(k) + I_b(k-1)\} * \{t(k) - t(k-1)\}}{Q_0} \end{aligned} \tag{2.4}$$

where Q_0 is the total capacity of the battery. When the above equation is implemented, estimates the SOC of the battery at an interval of $t(k) - t(k-1)$. The integral of the I_b over one sampling window has been calculated here using a trapezoidal approximation. Thus a real time estimation of a battery SOC can be obtained using sampled measurement of the battery current I_b and its capacity Q_0 at any given time. The estimator hold one sample of previous measurement of I_b and

time, and therefore there is almost no memory effect in the estimator.

2.3.2 Impact of SOC on the battery controller

While the ramp rate control is effective in PV capacity firming, if it is implemented without any compensation for the battery state of charge, it may adversely affect the battery performance as previously discussed. This includes the full depletion of the battery energy or battery overcharge, both of which could prove to be fatal to battery health and overall system reliability. In addition, the charge and discharge rate of the battery needs to be controlled in order to preserve the battery life. The authors in [21] and [22] describes a state of charge (SOC) control strategies for wind farm power regulation. However, most of the focus in SOC regulation goes to maintaining the SOC between an upper and lower limit. The availability of the battery for charge or discharge is a factor of the present SOC and therefore, the charge and discharge rate should also be affected by the net amount of charge available. The proposed controller serves a dual function while controlling the SOC:

- Maintain the SOC between upper and lower limit

$$SOC_H \geq SOC(k) \leq SOC_L \tag{2.5}$$

- The rate of charge/discharge is weighted according to the availability of charge

$$\begin{aligned} I_b &= \overline{W} * (SOC_H - SOC(k)) * I_{b,ref} \ - Discharge \\ I_b &= \overline{W} * (SOC(k) - SOC_L) * I_{b,ref} \ - Charge \end{aligned} \tag{2.6}$$

where SOC_H and SOC_L are the upper and lower limits of the battery state of charge, and $\overline{W}$ is the normalized weighing factor. Based on the value of $\overline{W}$ the charge and discharge rate is amplified or reduced, but generally follows a constant pattern as described in the following Fig.2.4. The choice

of the weighting factor $\overline{W}$ affects the rate of amplification or reduction. The weighting factor is also a linear function of SOC, thus for a higher magnitude of the weighting factor generates steeper charge or discharge command when battery SOC is close to farthest from SOC_H or SOC_L and for a lower magnitude, the pattern is more flat in nature.

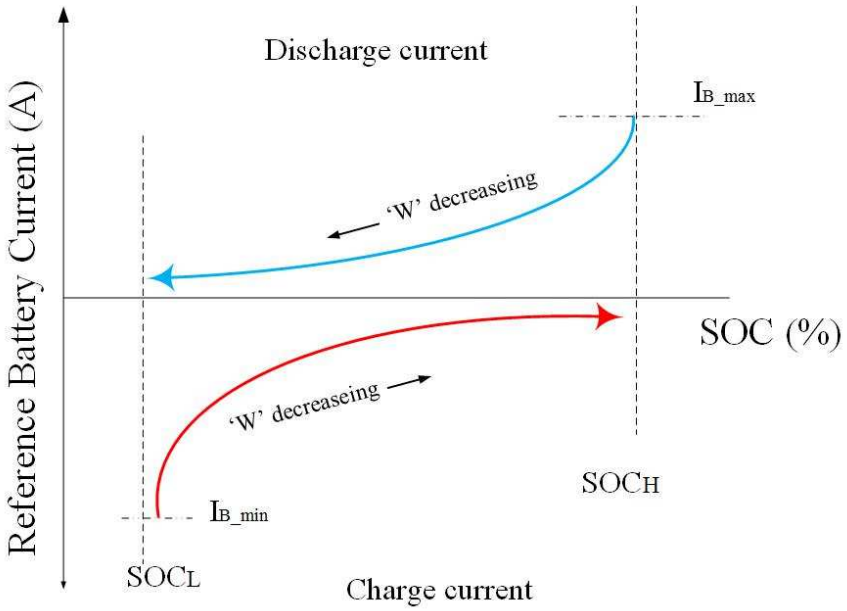

Figure 2.4: Dependence of battery output on the SOC

As shown in Fig.2.4, the battery current set point is determined based on the relative location of the SOC on the plot. When discharging, as the SOC moves further away from the SOC_H limit, the rate of discharge gradually decreases and while charging, the rate of charge decreases when the operating point moves away from the SOC_L limit. The trend is nonlinear as W, being linear function of SOC is multiplied with the linear variation of SOC along the horizontal axis.

2.4 Overall Controller Design

As discussed before, both the ramp rate controller(RRC) and the SOC controller are essential in controlling the PV and battery power to produce a smooth dispatchable power. The PV power stage

is controlled using maximum power point tracking (MPPT) algorithm, while the battery energy storage stage can be controlled by combining the ramp rate controller and SOC controller. The ramp rate control is essentially ON/OFF type. The central controller monitors the PV profile and calculates the ramp at every sample time, and compares it to a pre-set ramp rate. Whenever a ramp rate higher than the reference is detected, the controller allows the battery to charge or discharge accordingly. A hysteresis controller is appropriate in this case. Whenever the ramp rate exceeds the reference, the hysteresis block sends a current demand to the SOC controller. When the reference is not exceeded, zero demand is sent to the SOC controller. The hysteresis block resets at the end of every sample window. However, the amount of charge or discharge allowed for the given sample window is ultimately determined by the SOC controller. The SOC controller estimates current state of charge and depending on its location on the charge/discharge curve of Fig.2.4, where the amount of battery current is determined. The over all control scheme is represented in Fig.2.5.

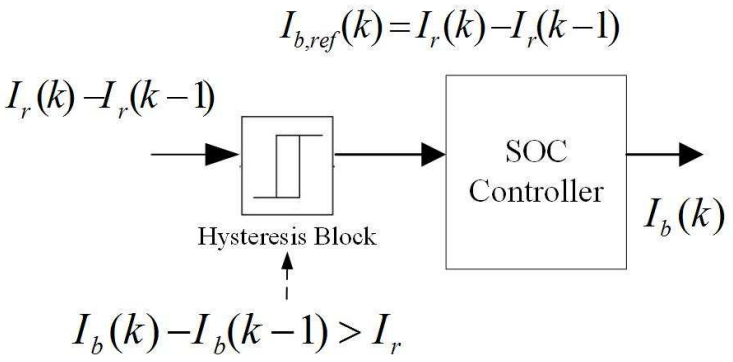

Figure 2.5: Combination of Ramp rate and SOC control

The SOC controller determines the battery current set point based on (5) and (6). I_r is the current flowing into the grid from PV. The overall system architecture for a firmed PV system is shown in Fig.2.6, where the battery is connected to the DC bus through a bidirectional converter. The PV panel is connected through a boost power stage. A maximum power point tracking algorithm (MPPT) determines the impedance seen by the PV in order to extract maximum power and based on the irradiation available, the power output of the MPPT boost converter changes as per Fig.2.1.

The direction of power flow in the bidirectional converter, i.e charging or discharging is determined by the polarity of $P_{PV} - P_L - PG$ as described by (2).

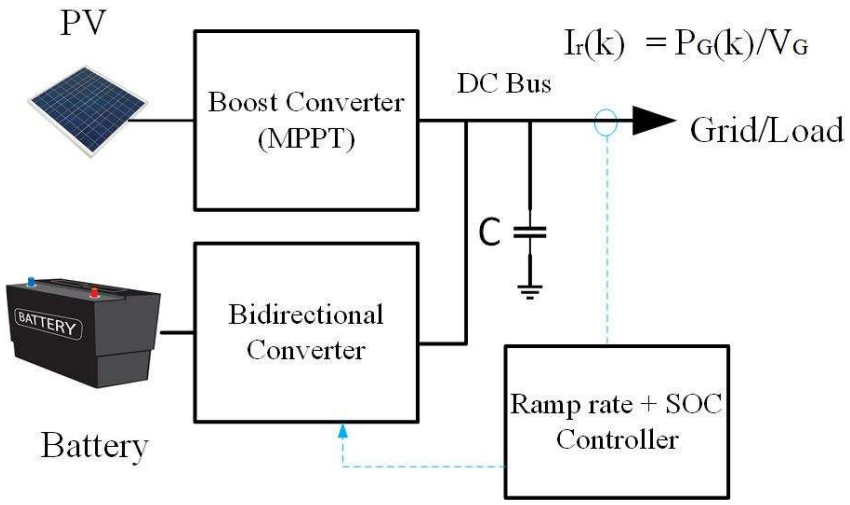

Figure 2.6: Firmed PV system architecture

The power converters of Fig.2.6 are separately controlled by the MPPT controller and the RRC-SOC controller. Note that there is no control interaction or information exchange required between the two controllers, so this scheme is decentralized in nature. This effectively improves the reliability of the system as minimal sensing is required and simpler control implementation is achieved.

2.5 Simulation Results

The concept of the ramp rate hysteresis controller and SOC controller has been implemented in Matlab environment and the results were validated through simulation. A 600 Watt PV raw data has been used to simulate the PV profile over the span of a day. To demonstrate the effectiveness of the controller, a highly intermittent profile has been chosen. Typically the sun is available from 7 AM in the morning to 6 PM in the evening, therefore an 11 hour time window is available for PV to generate power. The battery has been assumed to have a finite capacity. The upper and lower

levels of SOC has been assumed to be 80% and 20%. The reason for choosing the limits of the SOC well under the maximum and minimum possible limits 100% and 0%, is that in the event of a complete charge or discharge, the battery will still hold about 20% or 80% charge for the next cycle of charge and discharge. This enhances the performance and reliability of the system. As, shown in Fig.2.7, the intermittent PV profile is smoothed out when the ramp rate is $50W$ in 120 second sample widow or 0.0083Hz sampling frequency. Therefore, $\frac{dP_{ramp}}{dt} = 0.42W/s$.

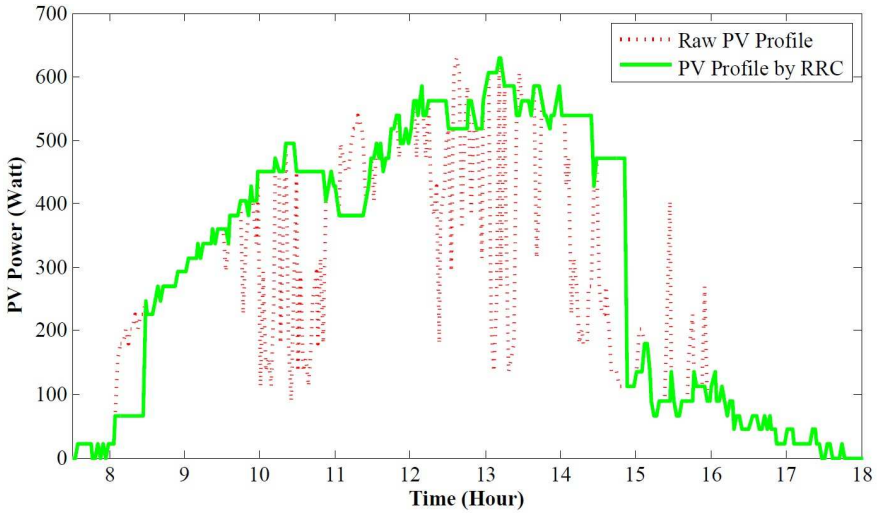

Figure 2.7: Ramp rate control for firming PV

It transpires from the result shown in Fig.2.7 that ramp rate controller alone will generate a relatively smooth profile while maintaining the ramp rate below certain limits. However this will unnecessarily burden the battery as discussed previously. For the given profile, the required battery charge discharge profile has been shown in Fig.2.8 with the dotted line.

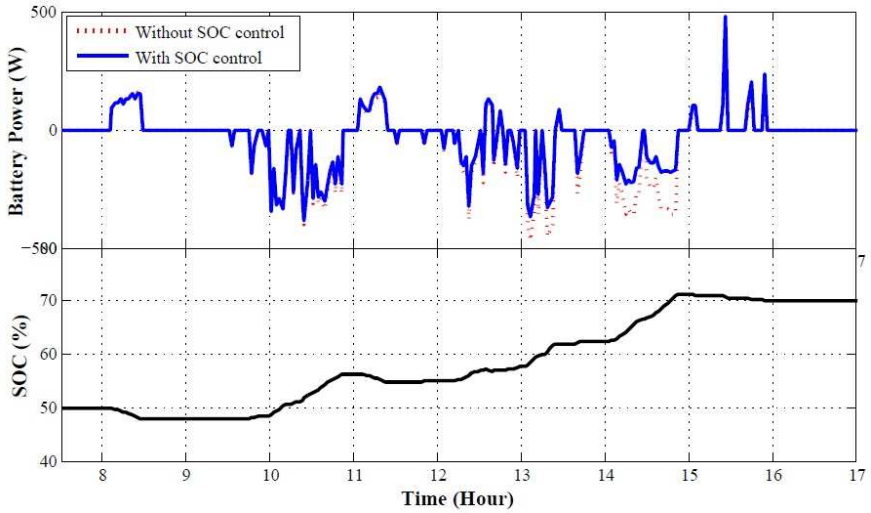

Figure 2.8: Battery power profile

The firm line represents the battery profile obtained by the SOC controller. Understandably, the SOC controller output is sometimes significantly different than the raw battery profile, where the controller acted to prevent overcharge and deep discharge using the state of charge weighted control described previously. The battery state of charge has also been represented in Fig.2.8, where it is clear that during a battery charge cycle, the SOC increases and during discharge, it decreases. The Battery SOC was maintained at 50% during the start of the day, and at the end of the day, after going through several cycles of charge and discharge, the SOC reaches about 70% of its capacity. The variation of the SOC is about 20% of the total capacity. Naturally, as the battery capacity increases the variation of the SOC decreases even further. Fig.2.9 shows a comparison of various battery capacities and corresponding plot of the SOC. The reference ramp rate can be updated based on the battery capacity plots.

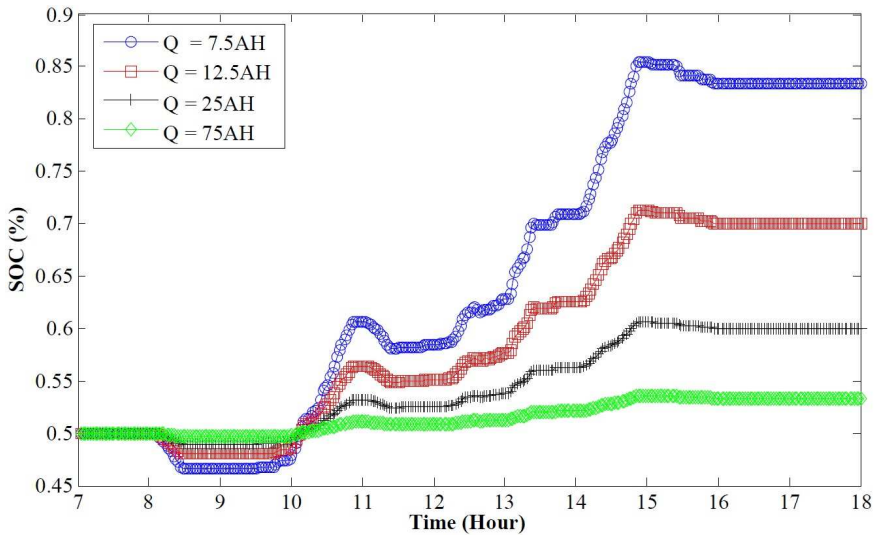

Figure 2.9: SOC plots for different battery capacity

When the RRC and SOC controllers work in cascade, they produce a better profile in terms of battery health and system reliability. Compared to this, when the RRC is working alone, the steep charge and discharge requirement for the battery contributes to the system loss and battery health degradation. The effect of RRC alone and RRC and SOC controller combined is demonstrated in Fig.2.10. It is noticeable that the RRC-SOC controller profile is also smoother as it filters out the sharp edges that RRC produces by using the SOC weighted controller.

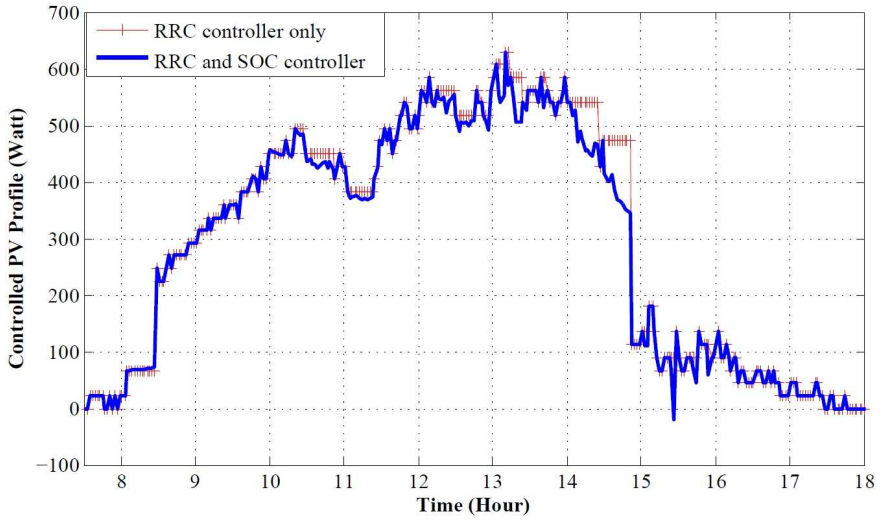

Figure 2.10: Performance of RRC and SOC controllers

2.6 Summary

The proposed combined ramp rate and state-of-charge (SOC) controllers, produce a firmed PV profile, allowing for power dispatchable capabilities. Although, with a smaller size battery, the firmed output power is relatively smooth, a day ahead forecast is still difficult in case of a wild PV power fluctuation. In that case the SOC controller will stop charging or discharging once the SOC is near its limits. Therefore, a trade-off between battery size and dispatchability must be made. The necessary analysis and tools have been presented here which enables one to determine the battery size and its possible dispatchability. The improved ramp rate controller enhances the system efficiency and therefore the overall control scheme helps PV systems to increase their penetration. Moreover, the sensors needed for sampling the load/grid power are placed on the DC bus side. The controller doesn't interact with the MPPT controller. Hence a decentralized controller is realized, which is an added advantage.

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CHAPTER 3: MULTIPORT CONVERTERS - PRESENT STATE OF THE ART

For almost a quarter century, conventional energy sources (fossil fuels) have been depleted and are gradually becoming economically nonviable. As a result, renewable energy sources (RES), such as wind and solar are becoming attractive replacements. Advances in renewable energy technologies over the last decade are also being matched by advances in power electronics as the enabling technology to harness renewable energy power. Only recently, the levelized cost of energy based on solar and wind sources has reached grid-parity in many countries around the world. However, as solar and wind energies are highly intermittent, and generally unreliable, these RESs are often used in conjunction with electrical energy storage (ES) systems to improve the reliability of the overall system [1]. In order to harness the full power generation capacity of wind and solar energy sources, a maximum power point tracking (MPPT) controller is required along with output voltage regulation so that the load voltage requirements can be met. These features are important for the commercial viability of these technologies. Typically, a DC-DC power converter stage capable of operating an MPPT algorithm as well as regulating the DC bus voltage, is used.

As the grid penetration rate of RES increases, combining it with ES may no longer be an option, but a requirement. States like California, have taken the lead in requiring RES systems include ES during installation [9]. With the gradual decline in cost of the ES systems, such as lithium ion based batteries, penetration of RES [10] can be improved significantly. Figure 3.1 illustrates projected deployable energy storage capacity and its cost over the next decade [4]-[7]. The forecast clearly shows an increasing trend of the deployable capacity of ES with a declining cost, making ES a perfect candidate to complement the intermittent nature of RES systems.

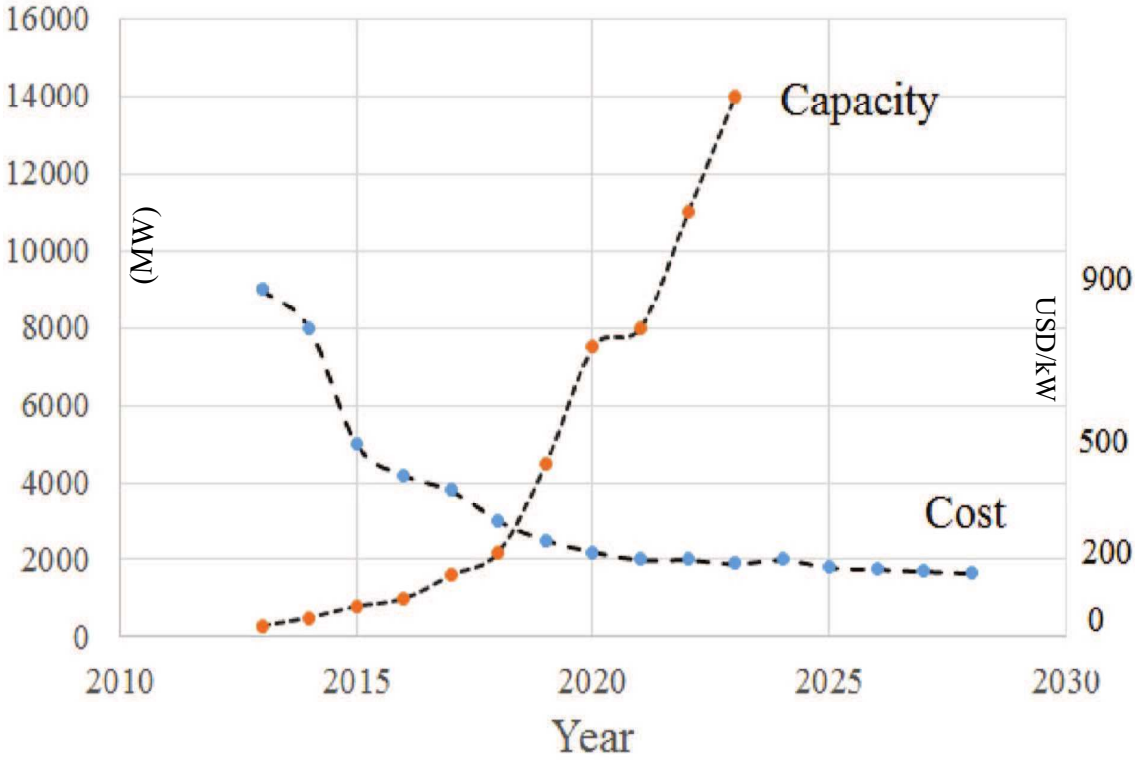

Figure 3.1: Forecast of ES cost and deployable ES capacity [5] & [7]

ES devices typically have voltage and ampere-hour ratings that are standardized for industrial application and often do not match the RESs. To independently control the power flow in and out of the ES device, a second power converter is required. The second power converter is usually installed between the common DC bus of the RES and the ES device. Therefore, it is necessary to use at least two different power conversion stages among the RES, the ES, and the load to enable power flow between each of them. However, it has been reported that if the ES device is chosen such that DC bus and ES voltages are equal, the need for a second converter is eliminated [17], [18]. This scenario is difficult to implement in grid tied systems where tight voltage regulation is required. A simpler approach is to use multiple separate power converters to integrate the multiple ports, although this may yield an inefficient and costly solution. A number of alternative designs

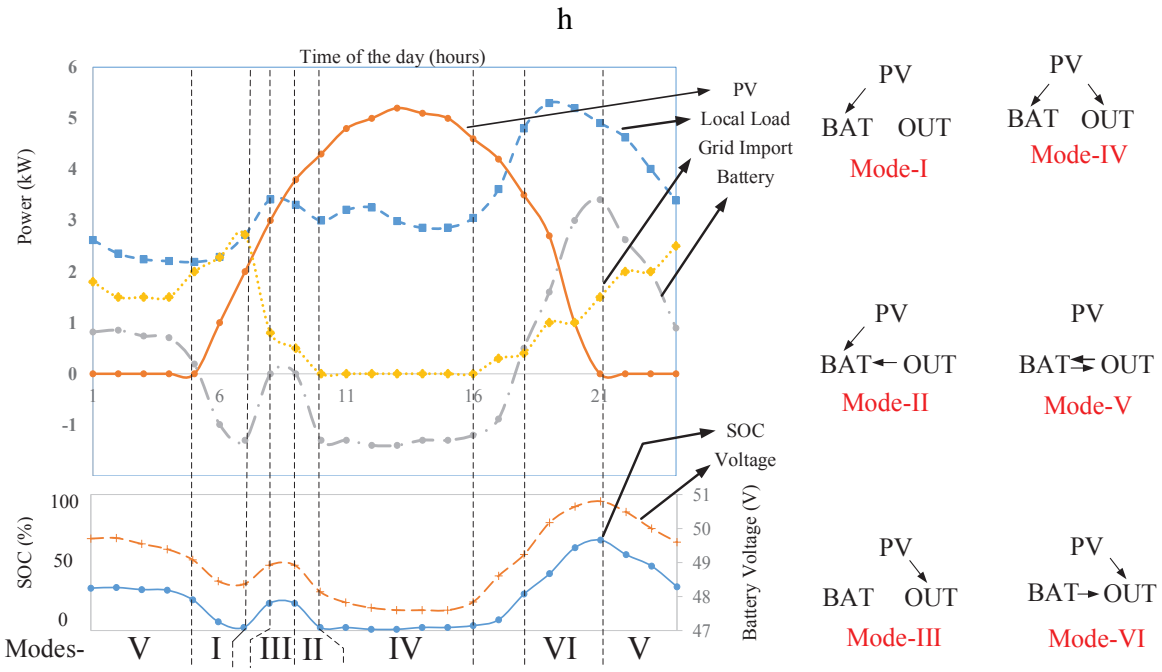

Figure 3.2: Main operating modes of an MPC integrating PV, battery energy storage, and a load for a typical day with 1C, 48V Battery DC Bus [3]

have been reported in the open literature that combine all stages into a single power stage with integrated multiple ports resulting in a Multi-Port Converter (MPC) [20]-[69]. In this chapter, a Three-Port Converter (TPC) and an MPC are used interchangeably since the majority of literature focuses on integrating three power ports into a single stage. In most cases, a TPC can be extended to an MPC without altering the architecture significantly.

The generalized modes of operation for a typical MPC are discussed in Section-II followed by the reported power converter architecture for a MPC in Section-III. The integrated MPC converter topologies are discussed in Section-IV. Section-IV is divided in two subsections discussing the non-isolated and isolated topologies with list of important parameters at the end of each subsection. Section-V details an overall comparison of all the topologies and how they are different from each other. In Section-VI, the future direction of research on MPCs are discussed along with concluding remarks.

3.1 Generalized operating modes for MPC

The primary purpose of MPCs is to integrate multiple ports into a single power stage allowing power flow between each port. Figure 3.2 shows the general operating modes of an MPC based grid tied PV-battery system along with typical daily power profiles of following sources and loads: PV, residential building load [8], optimized grid power import and battery. The grid profile is optimized to reduce overall costs for peak and off-peak tariffs. Based on the battery power flow, the state of charge (SOC) and battery voltage throughout the day is also plotted showing the battery charge and discharge profile. The C-rate of the battery for the Figure 3.2 is chosen as $1C$ which dictates the discharge rate of the battery. This implies that the battery will discharge from 100% SOC to its cutoff voltage in 1 hour.

As shown in the Figure 3.2, several power flow modes are possible which corresponds to different operational modes for the MPC. In order to analyze RES and ES system integration, the RES is assumed to be a photovoltaic (PV) source while the ES is assumed to be a Lithium Ion battery. The overall power flow equation can be represented as follows:

$$P_{Bat} + P_{PV} = P_{Load} + P_{Grid} \tag{3.1}$$

where P_{Bat} is the battery power, P_{PV} is PV generated power, P_{Grid} is power import or export to and from the grid, P_{load} is the demand from local loads and P_{Out} is the overall output power from a PV-Battery system. For a stand alone application $P_{Out} = P_{Load}$ and for Grid-tie systems, $P_{Out} = P_{Load}+P_{Grid}$ where P_{Grid} is positive or negative depending on power export or import, respectively. The most common and natural modes are "Peak shaving", "Firm PV" and "Grid tied PV". While "Grid tied PV" system is realized in Mode-III, "Firm PV" system can be realized by combination of Modes-IV and VI. "Peak shaving" is realized by switching between Mode-I and Mode-V. Note that the ES device can also be charged in Mode-II and Mode-IV. Therefore, peak shaving can be achieved by switching between Mode-I and either of II, IV or Mode-V. Different control strategies

can be employed based on the different operating modes [44]. However, the power flow between different ports plays an important role in selecting the topology to be used. With the decreasing cost of ES and the higher deployability of RES, many regulations are either encouraging or mandating the deployment of ES systems for PV firming and peak shaving, ancillary services like frequency and voltage regulation, which can also be accomplished by combining these modes of operation [5].

As an example, Mode-VI requires unidirectional power flow from PV to grid and unidirectional power flow from battery to grid. Therefore, the MPC for this application must block power flow between the PV and the battery entirely, as well as the power flow from the Grid to both PV and battery. A simpler approach involves the use of a reverse blocking power diode in series with the PV to block any power flow "into" the PV by turning off the power converter switches between PV and battery. It is important to note that bidirectional power flow requires an appropriate practical control strategy to allow seamless transfer between the operating modes. In [41] & [44], the control flow chart between different modes of operation is shown. Switching between various modes of operation for the bidirectional ports is challenging and difficult to implement.

3.2 Power converter architecture

Many different power converter topologies that integrate PV and ES systems have been proposed [11] - [19]. Figure 3.3 shows the four dominant architectures for integrating PV and ES with the red arrows indicating the direction of power flow. The most common architecture, which includes a separate DC-DC converter for the RES and ES units along with a second DC-AC inverter stage is shown in Figure 3.3(a). The second most popular architecture is the battery integrated with the DC link architecture as shown in Figure 3.3(b), where the battery DC-DC converter is eliminated. Figure 3.3(c) shows an AC battery architecture, where the battery is integrated into the AC side using a separate inverter. Each architecture has its advantage and disadvantages. In order to analyze

the various architectures, a typical 300W PV system along with a battery and a load is assumed as shown in the Table-3.1.

Table 3.1: Typical System Specifications

Port	Nominal Voltage	Current	Capacity
PV	32VDC	10A	-
Battery	48VDC/120VDC	-	10Ah
Grid/Load	120VAC	2.67Arms	-

The typical system specifications of Table-3.1 have been chosen based on practical and readily available PV and battery systems. It is immediately evident that the topology in Figure 3.3(b) is not suitable for the 48V battery system as the battery voltage is too low to be directly connected to the DC bus. Similarly, the topology in Figure 3.3(c) is also not viable. Topology in Figure 3.3(a) is the most plausible option since the intermediate DC-DC stage can boost the battery voltage to a high voltage DC bus compatible with the AC line.

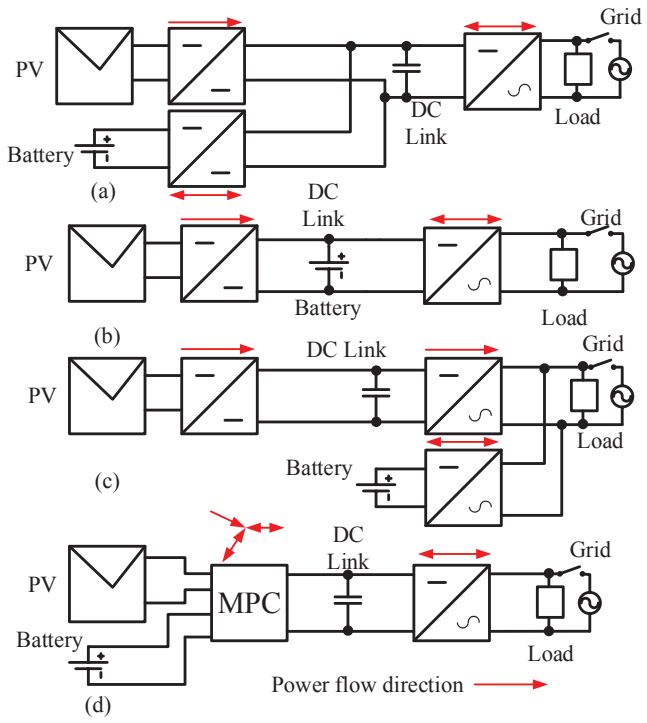

Figure 3.3: Main architectures for integrating PV and ES (a) Multi-converter architecture[11], [13]-[16], (b) DC link - battery architecture [17], [18], (c) AC side - battery architecture [12], [19], d) Integrated three port converter [20]-[69]

Topologies in Figure 3.3(b) and 3.3(c) are suitable for a higher voltage battery system, although the topology in Figure 3.3(b) requires additional switches/relays to steer the power flow from PV to battery or PV to grid without affecting the third port. These additions introduce reliability issues and system loss. Referring to Figure 3.3(b), since the battery is uncontrolled and directly connected to the DC bus, depending on the SOC of the battery, the DC bus voltage varies necessitating proper inverter control to maintain grid synchronicity.

The rating of the inverter varies between the topologies. In the topology of Figure 3.3(b) the inverter should be rated at 300W, while in the topology of Figure 3.3(c), both inverters should be rated at 300W each, thus adding significant cost to the system. Additionally, in the topology of Figure 3.3(c), integration of storage is considered as a separate distributed generation, requiring

additional circuit protection to be applied to the storage port as it is directly connected to the point of common coupling [2]. The advantage of this topology is that the battery can be used as an independent storage system to the grid. The multi-port converter shown in Figure 3.3(d) solves many of the challenges posed by the topologies shown in Figures 3.3(a)-(c), and thus offers a viable solution to integrated grid tied or standalone PV-battery system. Battery size and voltage are no longer determined by the DC bus. In addition, the choice of system configuration is much more flexible. It uses less components to achieve same performance as topologies in Figures 3.3(a) or 3.3(b), thus increasing system efficiency and power density. An analysis of a typical MPC structure of Figure 3.3(d) has been carried out in [44], which concluded that the converter has a lower device count and is highly compact with only one power conversion stage necessary. Naturally, the control complexity is reduced and overall flexibility of operation increased.

3.3 Integrated Multi-Port Converter Topologies

Various topologies have been reviewed in order to present a comparison of reported MPCs. All of the reported topologies can be divided into two main categories: "Non-Isolated" and "Isolated" topologies. As evident from their construction, isolated topologies incorporate galvanic isolation, as well as boost or buck functionalities to the power stage using the transformer turns ratio. Additionally, isolated topologies generally offer wider voltage range of operation; and, the power flow flexibility between all ports is generally higher. Non-Isolated topologies are more efficient as the transformer parasitic losses and leakage inductance are absent.

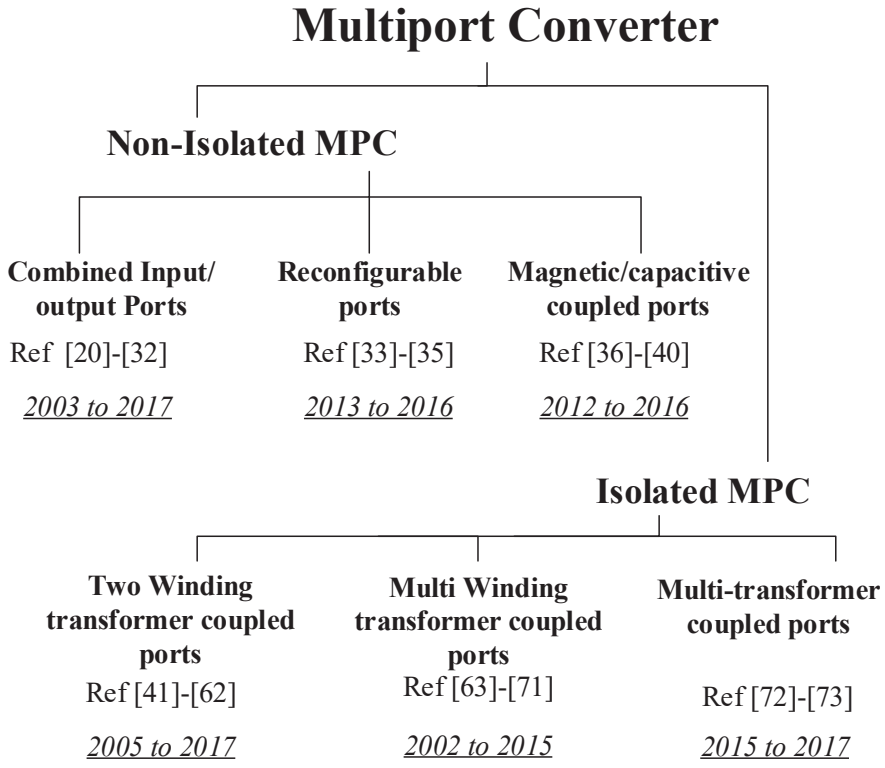

Figure 3.4: General classification of Multiport converter

In Figure 3.4, a detailed classification of the reported MPCs is shown. Non-isolated topologies can be subdivided in three groups. The "Combined input/output port MPCs" are constructed by combining various basic converter cells such as buck, boost or buck boost. Complex converter cells such as full bridge and half bridge can also be combined to develop this type of non-isolated MPCs. "Reconfigurable port MPC"s are simpler in construction. Typically they use one or two converters for interfacing multiple ports. Additionally, relays or other slow switching devices are used to reconfigure the circuit to use the same power converter for power flow among multiple ports. The third type of non-isolated MPC are constructed using "Magnetic/capacitive coupling" in addition to general combination of basic converter cells. Magnetic or capacitive coupling doesn't necessarily provides galvanic isolation between the ports, but generally used for greater voltage boost. This is particularly useful for RES and ES integration where wider voltage range can be accommodated. The isolated MPC can also be subdivided into three groups based on their con-

struction. The "Two winding transformer coupled port MPC" refers to topologies where usually a regular single core two winding transformer is used and two or more ports are combined either at the primary or secondary terminal of the transformer. "Multi winding transformer coupled port MPC"s are constructed when three or more ports are coupled using a single, multi-winding high frequency transformer which provides isolation for all ports. "Multi-transformer coupled MPC"s are constructed by combining two or more transformer. Based on the construction, this is generally a more costly alternative.

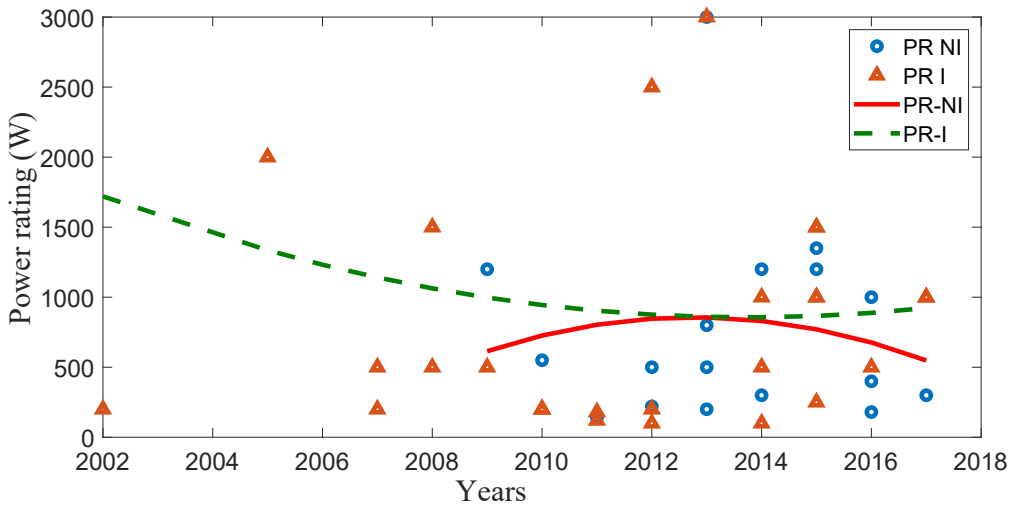

Figure 3.5: Trend of reported power rating (PR) of MPCs over last 15 years

Evolution of MPCs:

The evolution of MPCs is also shown in Figure 3.4 over last two decades. Both isolated and non-isolated topologies started appearing in literature around the early 2000s. The key motivation for the development of non-isolated topologies was to reduce the number of active switches and achieve better efficiencies. However, isolated topologies remained equally popular because of their higher flexibility in routing the power flow between multiple ports as well as their superior performance in higher power rated system. Based on the research efforts, the "combined input/output port MPC" and the "two/three winding transformer coupled port MPC"s are the most attractive options because of their low cost, high efficiency and high power density. In Figures 3.5 & 3.6, the

trend of power ratings, efficiency and switching frequency of the MPCs reported over last 15 years are shown for both non-isolated and isolated topologies.

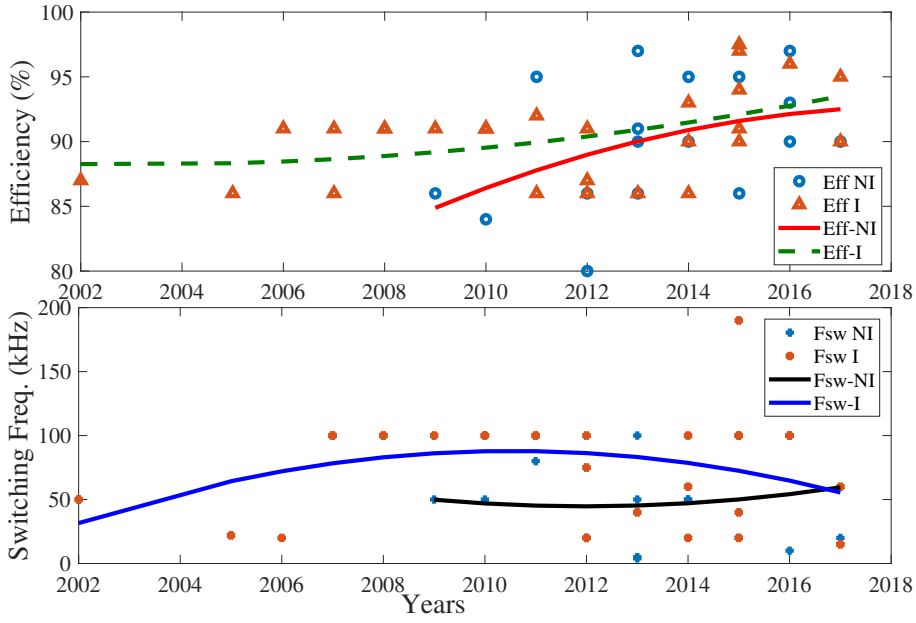

Figure 3.6: Trend of reported average efficiency (Eff) and switching frequency (Fsw) of MPCs over last 15 years

The plot is obtained by fitting the available data over a second order polynomial. It is apparent that, over time the efficiency of MPCs increased and became one of the driving forces for new development where the switching frequency remained around 100kHz for isolated and 50kHz for non-isolated topologies. Hence, the focus of the development was in the fundamental construction of the topology rather than techniques to achieve soft switching. The power ratings stayed around 500W-1000W. It appears that the non-isolated topologies settled at 500-600W range while the isolated topologies converged towards 1kW rating. This demonstrates that the focus of research has gradually shifted towards low power modules at ratings of 500-1000W. This progression matches the challenges of the growing residential PV market in the USA and worldwide. In the following subsections, a detailed discussion of each group of non-isolated and isolated MPCs are presented.

3.3.1 Non-Isolated Topologies

3.3.1.1 Combined Input/Output Port MPCs

Multiple power ports can be combined based on the voltage levels of each port and their interaction with each other. In [20], the authors describe a family of non-isolated converters realized by combining buck, boost and buck-boost cells in various configurations. However, this scheme allows only unidirectional power flow at the load port. In [21], battery charging and discharging to and from the other ports was demonstrated by implementing bidirectional switching cells. As reported in [20], combining the inputs of the basic converter cells can also produce a MPC, as as depicted in Figure 3.7(b), however the fundamental working principle remains the same. Other researchers reported a similar concept of combining the basic buck/boost/buck-boost converters into cascaded, series, or other combinations to realize a three port non-isolated converter topologies [22, 23, 24, 25].

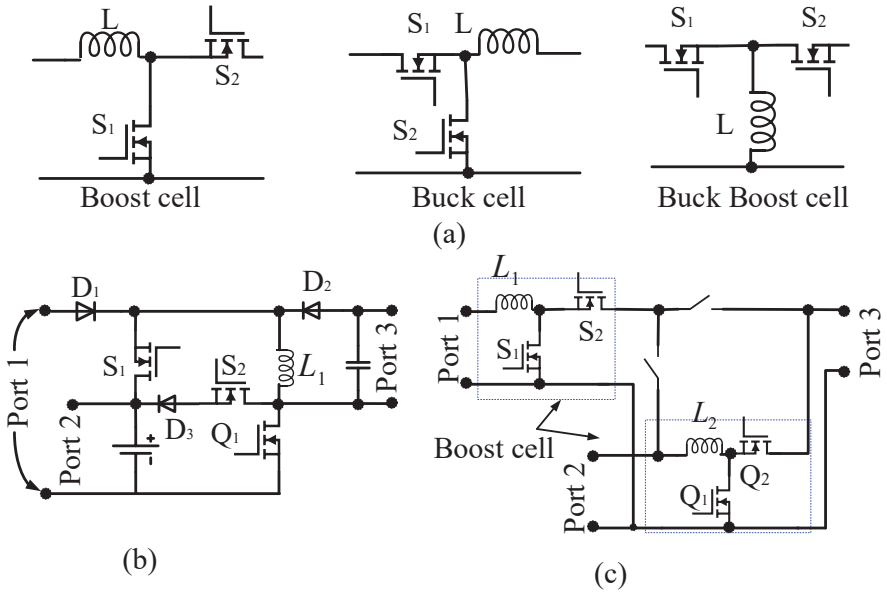

Figure 3.7: (a) Basic converter cells, (b) Boost derived MPC [20],[21] and (c) Bidirectional boost derived MPC

In Figures 3.7(c), a generalized bi-directional MPC topology is shown based on topologies reported in [20, 21, 22], which allows power flow between any two ports. The circuit has been constructed by combining basic converter blocks, with all bidirectional switches. For example, if a PV module with nominal output voltage of 32V is integrated with a battery energy storage device having nominal voltage of 48V, and the load voltage is 120V, three boost cell is required: the first between the PV and the battery, the second between the PV and load and the third between battery and load. However, if bidirectional power flow between the battery and load is required, a boost converter with bidirectional switches may be employed.

In Figure 3.8, the topology of [26] is shown. In this work, authors proposed a converter which cascades a boost and a bi-directional buck cell to create bidirectional power flow between the ports. Here the storage port acts as one of the input ports and the load is fed from the common DC bus.

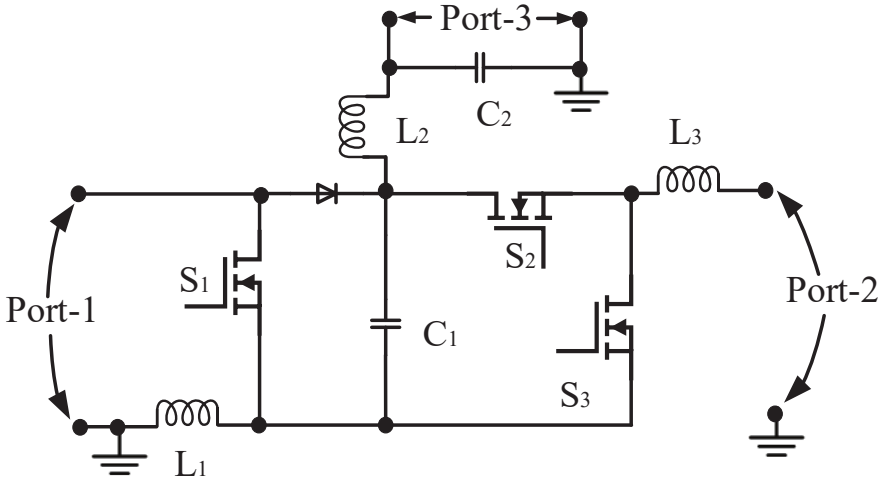

Figure 3.8: MPC based on cascaded Boost converter, [26]

In [27] and [28], the authors proposed a very simple implementation of a multi-input converter as shown in Figure 3.9, which can be used as an MPC for RES and ES integration. Different energy sources can be connected to each input ports of paralleled buck-boost or SEPIC or other fundamental power converter. However, two parallel sources can not export power to the load at

the same time as that might result in a circulating current. Thus, despite its simple implementation, the flexibility of such a configuration is reduced.

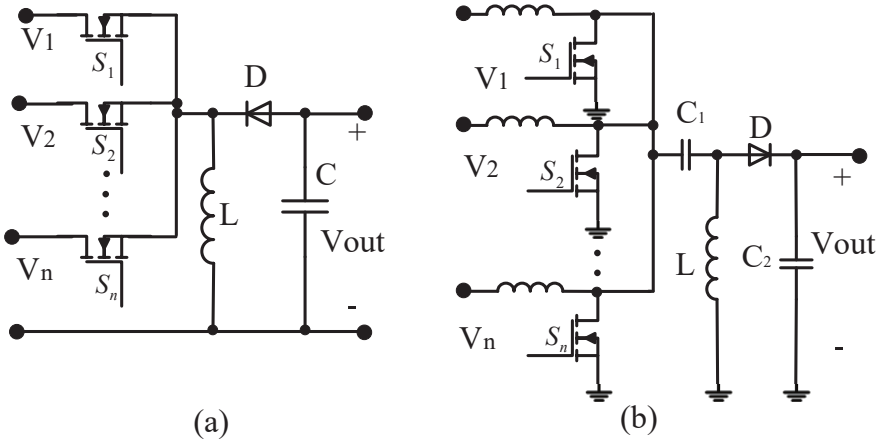

Figure 3.9: Multi input converter with sources paralleled at the input, (a) Multiinput buck-boost [27], (b) Multi-input SEPIC [28]

Authours in [29] proposed a multi-input boost converter. The topology has been constructed by combining multiple boost converters, where some of the inputs explicitly uses a specific boost stage and some inputs share the boost stage with other inputs. The topology utilizes resistive elements and no soft switching has been demonstrated, thus maximum efficiency achieved was 80%.

Since this class of MPCs are configured by combining basic converter cells, it is only natural that all ports will not be involved in power flow simultaneously. Most of the reported combined topologies primarily operate in single port to single port power flow mode or two port to the third port power flow (Dual-input or Dual-output) mode simultaneously. For the dual input or output mode, the inductor current is the summation of the two port currents. Depending on the switching sequence, one port is supplying current only a fraction of the time compared to the other port. This makes it suitable for PV-Battery applications when the battery port is not continuously active. However, since there is limited control over the amount of power flow due to topological limitations, often a reverse power flow into the PV needs to be blocked by diodes thus introducing a power loss. In [30] to [31], multiple energy sources are interleaved using current fed half bridge converters connected

to a common DC bus. The output AC port is powered from the DC bus through an inverter and a low frequency transformer. Although the AC port is isolated from all energy sources, the RES themselves are not isolated and parallel operation of multiple RES are not possible as they may result in circulating current between the RESs.

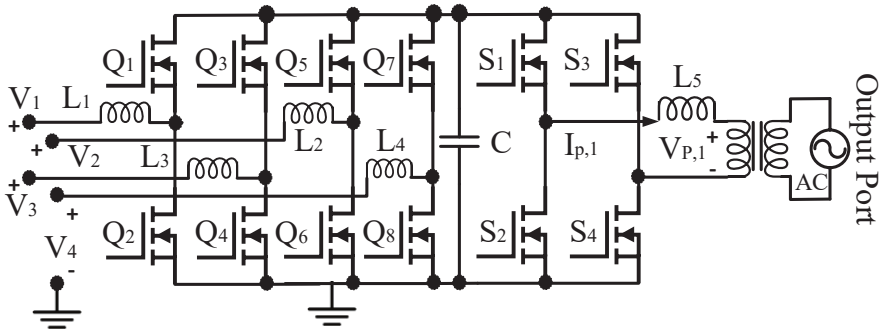

Figure 3.10: Interleaved Boost conevter based MPC [30]

In [32], an AC link multi-port converter has been proposed as shown in Figure 3.11. The main advantage of this topology is that it converts battery and PV power to AC without needing a de-coupling stage. The small inductor and capacitor between the DC-DC and DC-AC stage acts as an AC-link, thus reducing the overall power conversion stages to one. However the number of active devices employed, lowers the overall system efficiency and power density.

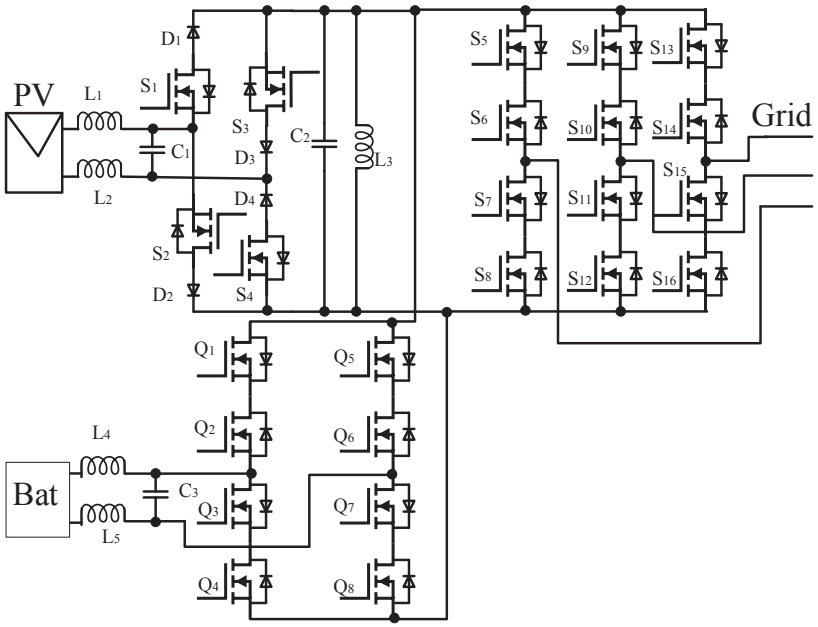

Figure 3.11: AC link Multi port converter [32]

3.3.1.2 Magnetic and Capacitive coupled MPCs

In [33], authors proposed a non-isolated MPC which is a combination of boost converters as shown in Figure 3.12. Boost inductors are replaced with coupled inductors for higher voltage gain. For wide voltage range renewable energy sources, this arrangement is particularly useful. An additional active clamp circuit allows softswitching and improves performance. In [34], a similar topology is proposed where the input ports transfers power to the output port through boost stage. The output port voltage gain is increased with the use of coupled inductor.

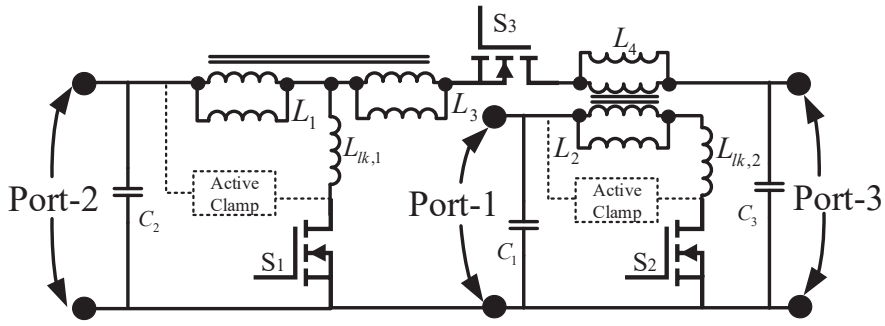

Figure 3.12: MPC with cascaded boost converter and coupled inductor, [33]

Capacitive coupling was utilized in [35] where multiple input ports were combined by capacitive coupling of two boost stages. The capacitive coupling is based on the principles of a charge pump circuit. It multiplies the output voltage based on the number of diode capacitor voltage multiplier stages.

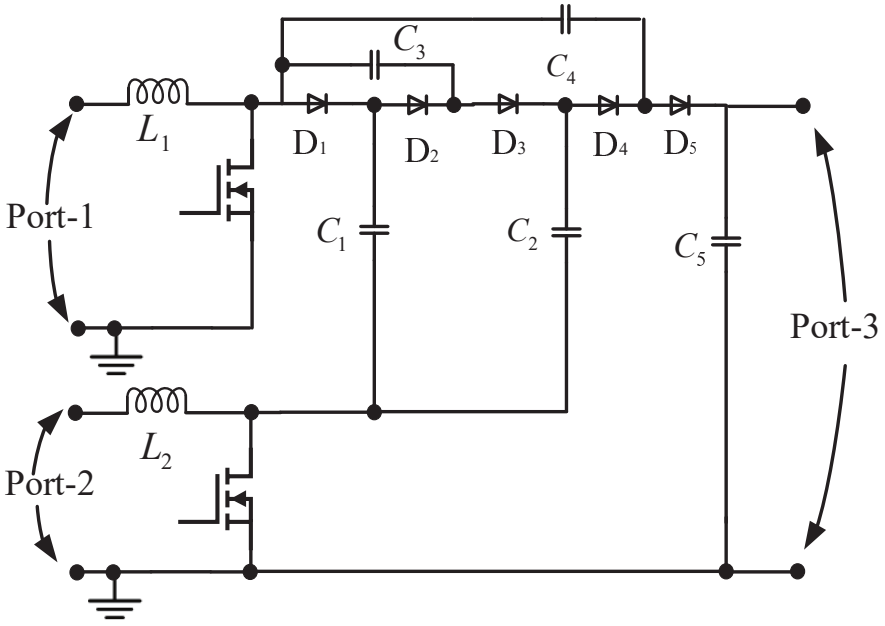

Figure 3.13: Double boosts stage MPC with capacitive voltage multiplier , [35]

3.3.1.3 Reconfigurable port MPCs

In [36, 37], a single pole multi throw power electronic switch has been used to select multiple input sources to a centralized buck or boost or other nonisolated converter. The switch can be realized with various combinations of active switches, and thus can be controlled easily with a digital controller. A compact MPC topology has been proposed in [38], as shown in Figure 3.14. Here, a three phase inverter is reconfigured for AC-DC front end conversion to charge the battery from the grid. The inverter stage is also used for DC-DC conversion between the PV and the battery when a portion of the three phase bridge is used. This topology is attractive due to its single stage operation and relatively low device count. However, the overall operational flexibility is low for all these topologies, since reconfiguring the converter to operate in different modes is difficult and involves a high number of relays/switches. This introduces unreliable transitions between power flow modes. In addition, for [38] the battery and the PV are directly connected to the DC bus, requiring advanced controls to regulate the inverter output rms voltage. Therefore, grid parallel operation is difficult.

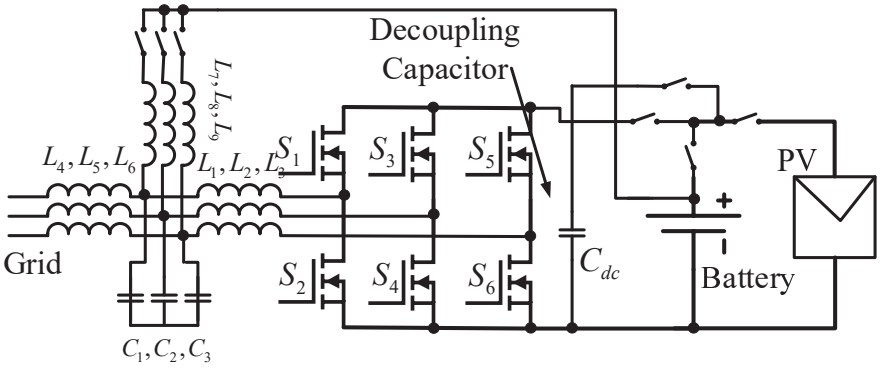

Figure 3.14: Single stage three phase reconfigurable converter [38]

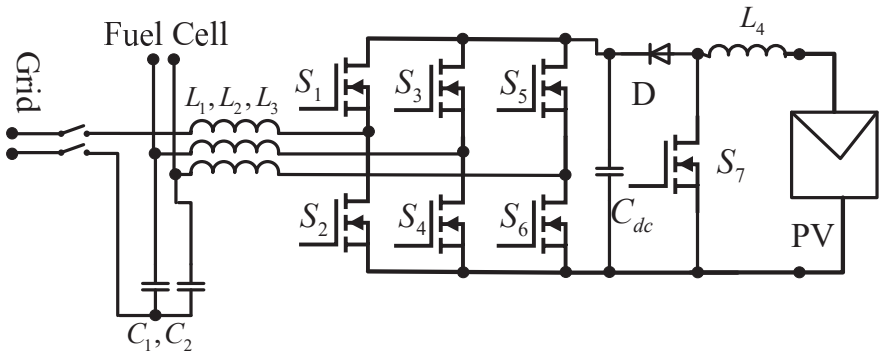

Figure 3.15: Single stage single phase reconfigurable converter [40]

Similarly [39] and [40] can also be configured to allow power flow between multiple ports using slow switching devices such as relays or circuit breakers. In Figure 3.15, the topology of [40] is shown. The main difference between Figures 3.14 and 3.15 is that the AC port is single phase in Figure 3.15. The three output phases of the three leg bridge converter are converted to single phase using a common mode circuit. With this configuration, lower number of slow switching devices are used and hence is more efficient and reliable compared to Figure 3.14, but the AC output is restricted to single phase.

In order to gain a better understanding of how each topology compares to others based on their power rating, voltage rating, size of passive components and device count, efficiency etc, Table-3.2 provides a comprehensive list of important parameters of the discussed topologies. The size of passives and overall device count directly influence the power density and cost of the converter while the number of hard and soft switched devices influences efficiency. System flexibility is determined by the available number of bidirectional ports, which indicates the ability of the TPC to achieve the six modes of operation discussed earlier. In terms of power rating of the reported topologies, they can be divided in to two broad groups. Power ratings of 500W or less are very suitable for use in a residential applications, while power rating of more than 500W is attractive for larger buildings or commercial establishments. The list of topologies in Table-3.2 are divided in these two power rating groups where the top half shows the low power group topologies and

the bottom half shows $> 500W$ topologies. While the topology in [20] reports high efficiency, lower device count and smaller passive components, the system flexibility is low and there is only one bidirectional port. Topology of [26] on the other hand, has two bidirectional ports allowing most of the power flow modes without any additional modification while maintaining high efficiency. The topology reported in [24] reports high efficiency, but utilizes wide band gap (WBG) devices, therefore comparatively costly. Topology of [35] demonstrate good efficiency, but only bidirectional power flow allowed is from port-I to port-II and thus not very attractive for PV-battery application. Other reconfigurable topologies reported, typically achieves low efficiency and low system flexibility. The "Combine input/output port MPC"s achieve the best efficiency and can also allow bidirectional power flow when bidirectional switches are used.

Table 3.2: List of key parameters of reported non-isolated topologies

Topology	Rated Power (W)	PV Voltage (V)	Bat. Voltage (V)	Load Voltage (V)	FETs and Diodes	Sw. Freq (kHz)	Inductor (μH)	Energy Storage Cap. (μF)	Bi directional ports	Avg. Efficiency
Ref [20]	140	15 -21	24	30	6	80	40	-	ES	95%
Ref [29]	220	40	24	120	8	20	2x 4000	500	ES	80%
Ref [33]	200	52.8	48	380	5	50	2 x 1	47	ES	$\leq$ 90%
Ref [35]	400	20	20	400	7	100	2x 100	4x 20, 22	ES	93%
Ref [39]	180	18	12	18	3	10	3x 2000	2x 470	ES, Load	90%
Ref [24]	4000	200 -500	150	600	10	20	1000, 800	35	ES, Load	97.5% (WBG devices)
Ref [26]	1200	80.1	70	100	4	100	3 x 75	60	ES, Load	95%
Ref [32]	800	150	200	208	24	4	880	0.4	ES, Load	91%
Ref [38]	3000	200	115.2	118, 200	13	5	3x1900, 1100	3300, 30, 410	ES, Load	-
Ref [36]	550	80	60	50	5	50	50	150	ES, Load	84%

3.3.2 Isolated Topology

As previously discussed, three types of isolated topologies have been reported in the literature based on the structure of the isolating transformer. In the "two winding transformer coupled MPC", isolation is provided using a two winding transformer, where two ports are non-isolated from each other while the third port is isolated from the non-isolated ports. On the other hand, in "Multi winding transformer coupled MPC"s, all ports are galvanically isolated using a multi-winding transformer. Either a half bridge or full bridge arrangement may be used for the DC to square wave AC conversion stage. Since high frequency AC power flows through the transformer, utilization of the transformer core is high compared to single ended topologies such as buck or boost derived converters. The third type is the "multi-transformer coupled MPC", where each transformer couples atleast two ports through a dual active bridge (DAB) type arrangement [74]. Then either the primary or secondary of the multiple DABs are combined to form an MPC.

3.3.2.1 Two winding Transformer Coupled Ports

In [41] - [44], the authors introduced a topology that integrates PV, battery and load port based on the principles of active clamped forward converter. In [45], a similar concept has been utilized to create a family of isolated MPCs. These circuits are shown in Figure 3.16.

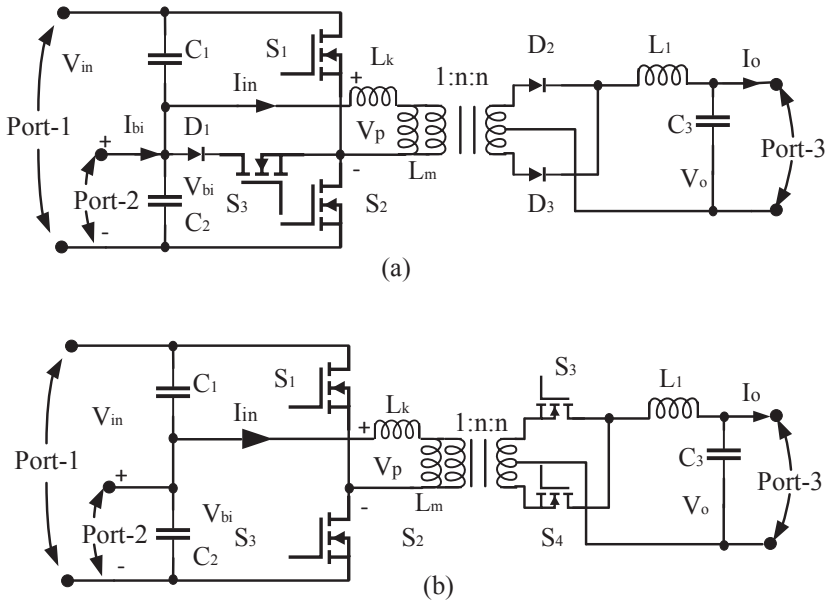

Figure 3.16: "Two ports-isolated" topology: (a) Primary freewheel [41], (b) Secondary freewheel [45]

Since two out of the three ports are required to be controlled independently for a PV application [45], switches S_1 and S_2 must be controlled independently along with a freewheeling path for the transformer magnetizing inductance in order to realize port-1 to port-2 power flow. This is realized in Figure 3.16(a) using D_1 and S_3 and in Figure 3.16(b), by shorting the secondary switches S_3 and S_4. The bidirectional port allows current flow to and from the port when S_1 or S_2 are on while the current will be zero when the switch S_3 is on. Thus the "on time" of the bidirectional port influences the output power. Although three port conversion is achieved, a seamless power flow in or out of the bidirectional port is difficult to implement.

The topology reported in [46] cascades two energy ports to the primary side of a full bridge converter to create an MPC, where as in [47], the third port was combined using a boost converter to the secondary of the center tapped transformer of a half bridge converter (Figure 3.17). A number of interleaved topologies that combines two energy ports has appeared in literature through out

the last decade. Although interleaved boost MPC first proposed in 2005 [48], over the years this topology has been improved by introducing bridgeless and bridge rectification as shown in [49], [50], reducing number of active switches. Similar interleaved boost topology at the primary side of the two winding transformer has been proposed in [51] which is shown in Figure 3.18(b). The work in [51] uses less number of active devices than [49], thus is cheaper in cost but the former allows a voltage doubler stage and also allows an additional degree of freedom for the controller implementation. This is particularly useful for renewable energy conversion and multi port power flow control. Topology in [52] is a buck derived half bridge configuration, however two input ports are combined on the transformer primary side. Use of bidirectional switch allows great flexibility of power flow control between all three ports with port-I and II being bidirectional. However, maximum power flow allowed from each port on the primary side is limited by the topology as it is directly influenced by the duty ratio of the other port. A combined input full bridge topology appears in [53], however this incorporates individual boost stages before the full bridge stage for the input ports. Thus the full bridge stage operates in double ended mode which allows better transformer utilization and easier implementation. The drawback of this topology is that additional active clamp circuit is required to contain the voltage stress on the input ports. Authors in [54] creatively used an interleaved boost converter to couple two ports where the boost inductors are coupled to a galvanically isolated secondary winding. The secondary winding couples an unidirectional load port after a rectifier stage. Three port conversion is achieved with isolation between the load and two input ports with with good efficiency, however the implementation is difficult and prevention of shoot through is critical. In [55], a three phase version of the interleaved MPC was first introduced. A three port micro-inverter topology was reported in [56], which utilizes the concept of active clamped flyback topology. The power decoupling capacitor was shifted to the PV side and thus, a small film capacitor can be utilized, prolonging the lifetime of the converter.

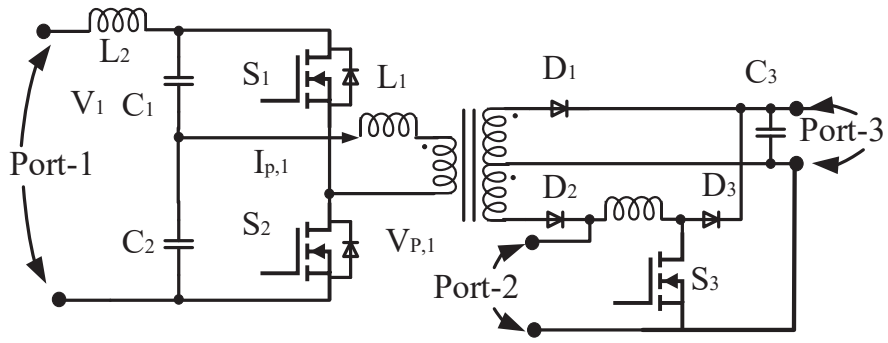

Figure 3.17: Secondary integrated ripple port TPC [47]

In [43, 57] multiple power sources were combined at the input port using a switch for each power sources (Figure 3.19). This is similar to the non-isolated multi input converters discussed in the previous section. As a result, this topology has similar drawbacks since no two sources can be active at the same time in order to avoid circulating current flow between them.

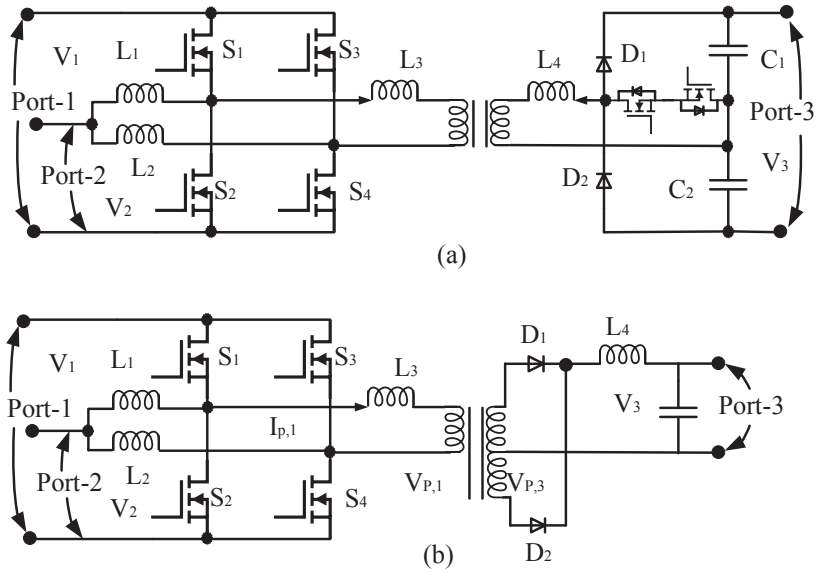

Figure 3.18: Bridgeless boost rectifier based topology of (a) ref [49], (b) ref [51]

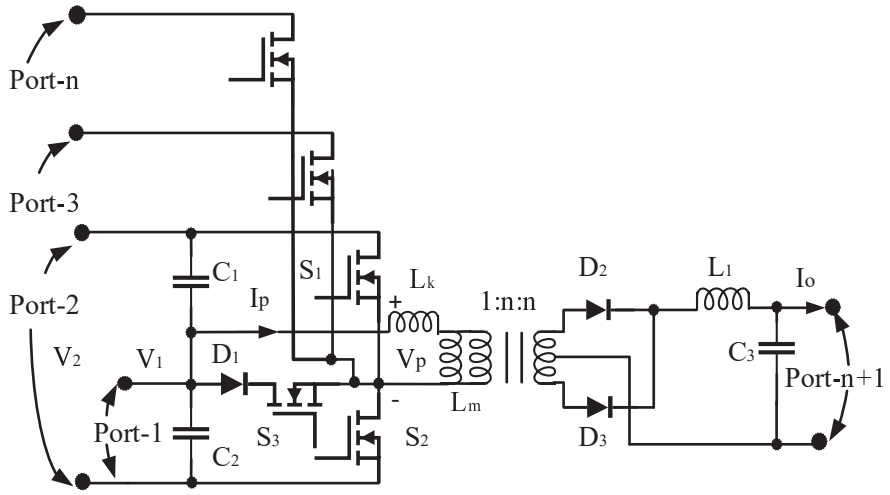

Figure 3.19: Multi input Isolated converter [43]

The approach of combining multiple ports through basic converter cells as presented earlier, has been adopted in developing isolated topologies as well. In [58], authors adopted combinations of buck, boost, cuk, SEPIC or zeta converters in the primary of the isolating transformer. Proper control ensures bipolar voltage applied to the transformer, additionally a DC blocking capacitor is used for flux balancing. The topology is similar to the topology of Figure 3.18 (b). Important differences include two different sources being connected to each inductor in port-2, making it four port converter. Also, instead of a center tapped secondary configuration, [58] uses a full bridge rectifier for the load port.

In [59] and [60], it was reported that a three port converter may be used to smooth out the $120Hz$ ripple caused by the line current at the inverter output. In both converters, a primary side auxiliary port has been added to reduce the 120Hz ripple. Additionally, authors in [60] demonstrated a similar functionality with an "AC link" MPC with three winding transformer where the third winding is dedicated to the ripple port. This is similar to the class of "Three Winding MPC" discussed next. The ripple port power equalization is given by:

$$P_{ripple} = P_o cos(2\omega t) \tag{3.2}$$

where P_o is the average real power and ω is the line frequency in radians. Power flow from the PV or other RES to the load is controlled by the duty ratio. The ripple port is typically a symmetrical bridge type, therefore the average power flow in and out of the port is zero over a 60Hz cycle, thus allowing a bulk capacitor to be used in the ripple port. This is functionally similar to a decoupling capacitor application; however, this approach allows end users to select lower voltage capacitors and not be constrained by the standard high voltage decoupling capacitor rated at the DC bus voltage level which greatly enhances the reliability [60]. In [61], author proposed a dual interleaved boost converter coupled through a two winding transformer. Four different ports can be interfaced using this topology with all ports being bidirectional. Thus the high flexibility of power flow is an attractive feature of this topology. The topology is shown in Figure 3.20.

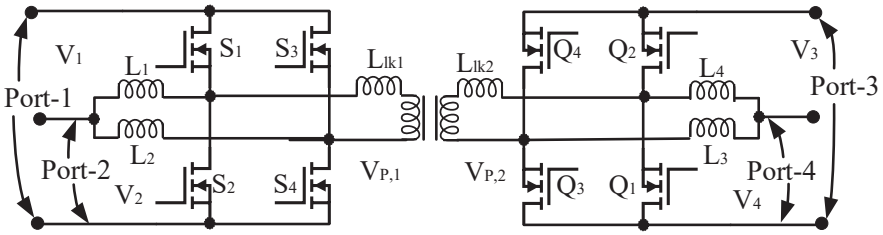

Figure 3.20: Dual interleaved boost MPC [61]

3.3.2.2 Multi-winding Transformer Coupled MPC

The second class of isolated MPC are realized using a multi winding transformer to provide isolation between all three ports and typically consists of a half bridge [63, 64] or full bridge [65]-[68] DC to AC conversion stages. These topologies allow for bidirectional power flow when bidirectional switches are used in the bridge. The topology is shown in Figure 3.21. The converter allows for a decoupled power flow between all three ports [65].

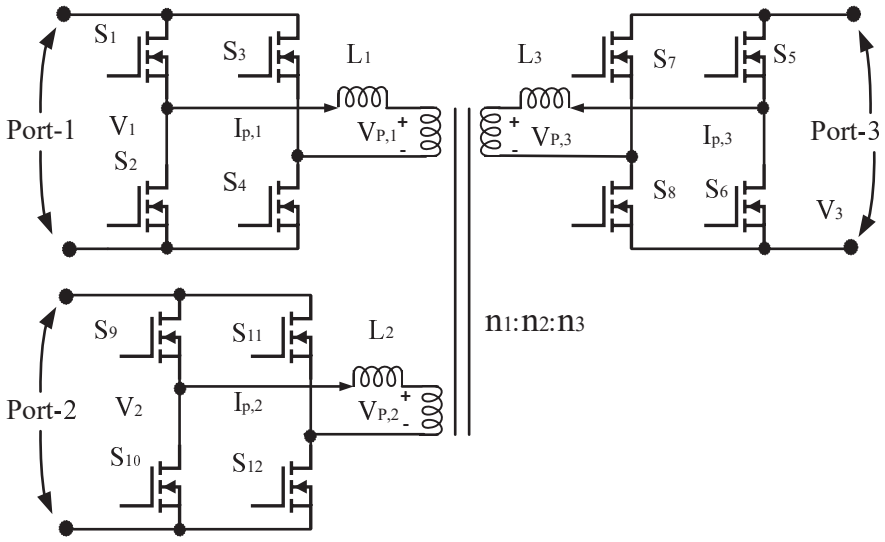

Figure 3.21: Isolated triple active bridge converter-Full Bridge [65]-[67], [68]- without the resonant tank

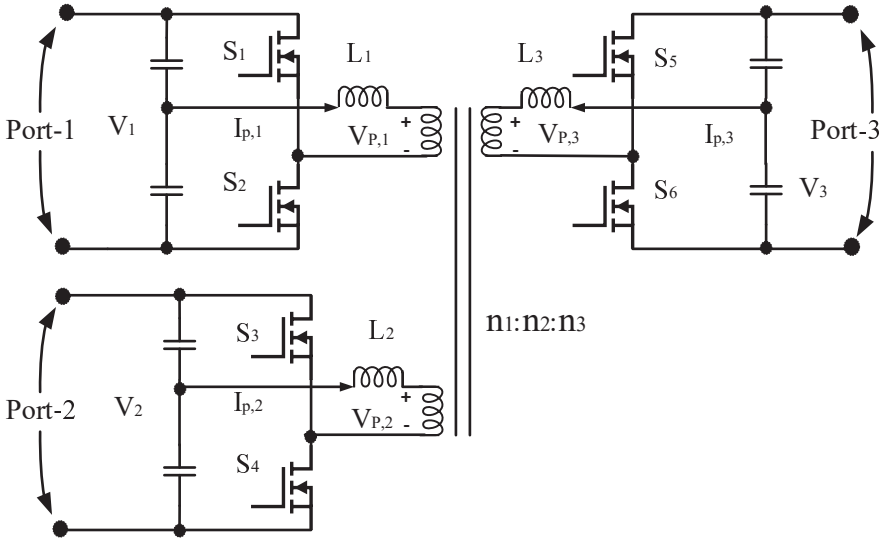

Figure 3.22: Isolated triple active bridge converter-Half Bridge [63, 64]

Many published works proposed the topology of Figure 3.21 [65] - [67]. In [68], a series resonant tank has been added to the converter to achieve higher switching frequencies and lower losses. A similar variant with one port, unidirectional power flow has been proposed in [69]. In [64], a half

bridge three port converter has been proposed as shown in Figure 3.22. The fundamental difference between the full bridge and half bridge TPCs is that the half bridge type converter can only operate at 50% duty cycle, therefore no duty ratio control can be implemented and hence the soft switching range is narrow and difficult to achieve.

In [70], a center tapped arrangement on both the primary and secondary of the isolating transformer of a dual active bridge topology has been made which allows four ports to be interconnected. [71] is a MPC based on multi active bridge converter. This is similar to [65] with integration of four or more ports instead of only three. The main disadvantage of this topology is, as the number of ports increases the design of the high frequency transformer becomes increasingly difficult., at times allowing the transformer core size to increase just to allow more winding.

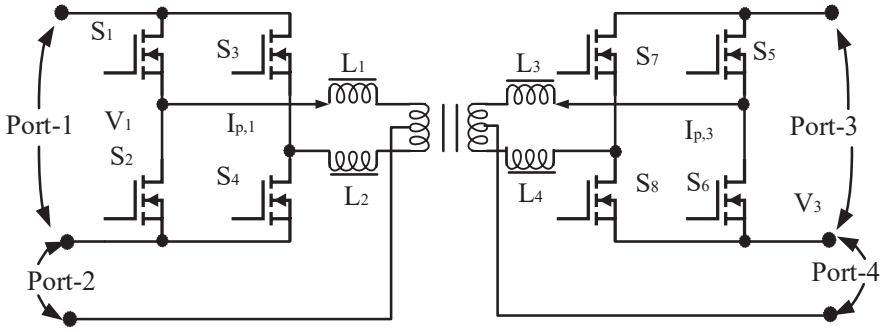

Figure 3.23: MPC with Center tapped transformer [70]

3.3.2.3 Multi-Transformer Coupled Ports

The other class of MPCs which uses multiple transformer coupled together to provide isolation as well as multi port power flow are reported in [72] & [73]. In [72, 73], two dual active bridge transformer were magnetically coupled and the secondaries were combined to form a three port converter. The topology of [72, 73] is shown in Figure 3.24.

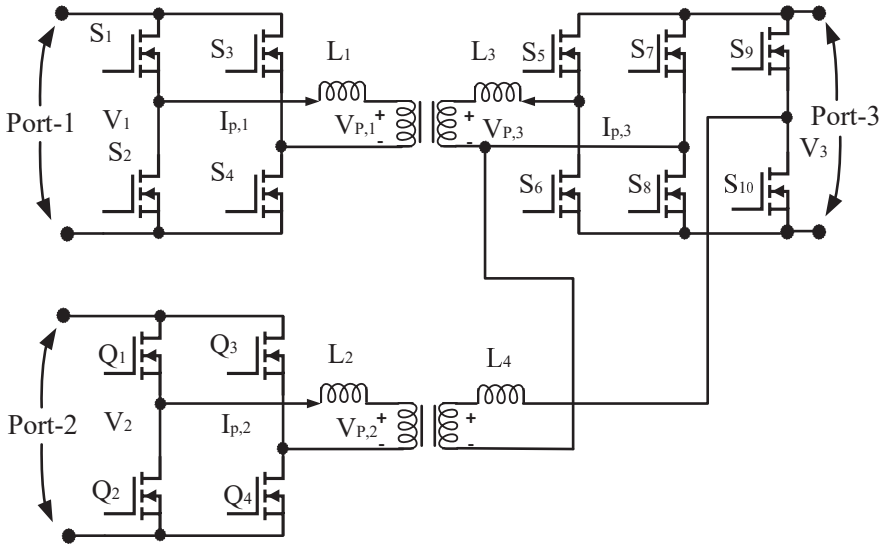

Figure 3.24: Dual transformer based triple port active bridge MPC [72, 73]

The converters of Figure 3.20 to 3.24 operates using the "phase shifted" PWM method as described in [65]. Each half bridge is controlled so that their outputs are phase shifted with respect to each other. Figure 3.25(a), shows the simplified equivalent circuit of the topology of Figure 3.22 while the key waveform for phase shifted PWM (PSPWM) operation are shown in Figure 3.25(b). The leakage inductances of the transformer $L_1^{'}$, $L_2^{'}$ and $L_3^{'}$ are the equivalent inductances for Y-type transformer. If the transformer is a 'delta'-type, the values of Y-inductances will have to be calculated accordingly. In [62], the transformer isolated dual active half bridge configuration is extended by adding multiple boost or buck derived half bridge legs on both the primary and secondary of the transformer. This allows multiple source and load ports to be coupled in a variety of configurations. The power conversion stage of [62] is similar to dual active half bridge topology (Figure 3.22) with the ports are either voltage fed or current fed type structure.

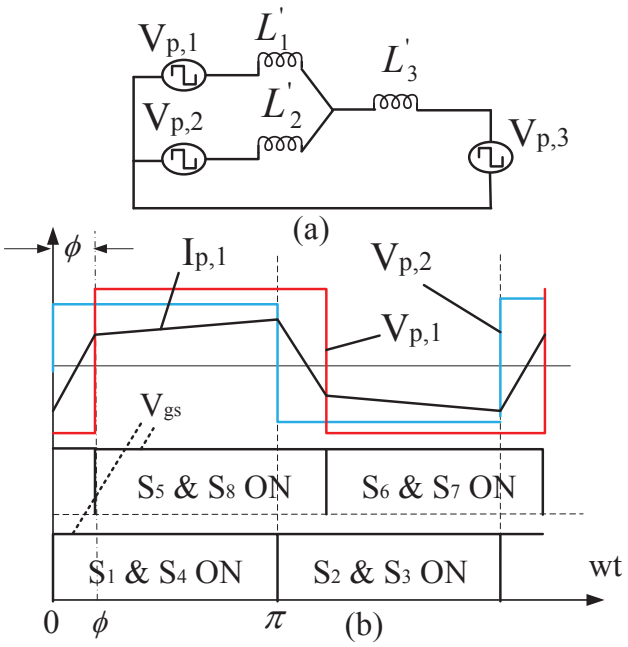

Figure 3.25: (a) Equivalent circuit of three winding MPC [63]-[69], (b) key waveforms

It was shown in [74] that the power transferred from one port to another is given by:

$$P = \frac{V_{P,1}V_{P,2}}{n\omega L}\phi(1 - \frac{\phi}{\pi}) \tag{3.3}$$

where ϕ is the phase shift angle between the two port and $n = \frac{n_2}{n_1}$ is turns ratio between the two ports (port-1 and port-2). The simple yet effective PSPWM method allows power flow in both directions by controlling the phase shift angle ϕ as given in (3), and can be easily implemented in a MPC. In [65] and [67], authors introduced duty ratio control in addition to the phase shifted PWM method. This was done in order to reduce the overall system loss and widening the ZVS region. The introduction of duty ratio control along with phase shift control reduces overall power transfer but ensures soft switching operation over a wide power range [67].

Similar to non-isolated topologies, list of efficiency, device count etc. for important isolated topologies are detailed in Table-3.3. Here, first four topologies belong to the low power ($\leq 500W$) group

and the rest of the topologies belong to higher power group ($> 500W$).

Table 3.3: List of key parameters of reported isolated topologies

Topology	Rated Power (W)	PV Voltage (V)	Bat. Voltage (V)	Load Voltage (V)	FETs and Diodes	Sw. Freq (kHz)	Inductor (μH)	Energy Storage Cap. (μF)	Bi directional Port	Avg. Efficiency
Ref [41] - [43]	200	40 -60	15-30	40	6	100	147	-	ES	91%
Ref [49]	500	70 -100	42	300	8	100	20, 2x35	-	ES, RES	96%
Ref [54]	250	16	12	80	7	20	-	2x470, 100	RES, ES	90%
Ref [67]	500	50	36	200	12	100	14.7, 28.4	-	RES, ES, Load	91%
Ref [47]	1500	80 -100	40 -45	50	7	100	100, 60	2x100	ES	94%
Ref [50]	1000	25-60	120	300-380	8	60	2x 155, 28	4x 10, 3x 22	RES, ES	95%
Ref [64]	6000	18	18	430	6	20	2x 0.3, 0.6	6x 10000	RES, ES, Load	91%
Ref [65]	1500	42	14	300	12	100	495, 21, 0.05	-	RES, ES, Load	91%
Ref [70]	1500	40	16	200	8	40	2x 4, 2x 15	4x 200	RES, ES, Load	91%
Ref [71]	1000	40	80	200	8	190	-	-	RES, ES	97.5%
Ref [72]	1000	50	50	100	14	15	2x 133	-	RES, ES, Load	90%

For isolated converters, galvanic isolation between the ports is an added advantage. Since two winding MPCs typically have lower device count and less copper winding and thus loss is reduced

compared to multiwinding MPCs, naturally [49, 47] and [50] report relatively higher efficiency. However, the three winding MPCs achieve both good efficiency (91%) and can accomdate all power flow modes as discussed in Section-II. Hence, topologies reported in [65]-[70] are also very attractive. The multi-transformer coupled MPCs [72]-[73] are usually of higher cost as they integrate two separate transformer. The efficiency is also similar or in a general case, less than the multi-winding transformer coupled MPCs. This is because the core loss is doubled in the multi-transformer coupled MPCs and thus doesnot provide any added advantage.

3.4 Review of control Strategies

The majority of control strategies reported in the literature attempt to solve three essential control problems, namely:

- Load voltage and current regulation: Maintaining a steady load voltage and accurate control of the load current as the load demand changes.
- MPPT: Maintaining maximum power tracking based on the irradiation level of sun.
- Battery SOC control: Controlling the charge and discharge of the battery based on PV generation and load demand.

To control the PV and battery power while at the same time maintaining a steady load voltage, all three control objectives must be fulfilled. For a limited application such as only battery charging from PV, or "Grid tied PV", only one or two of the above objectives are sufficient. Figure 3.26 shows a generalized set of control "building blocks" that have been proposed in the literature. These include output voltage regulation (OVR), output current regulation (OCR), battery voltage regulation (BVR), battery current regulation (BCR), maximum power point tracking (MPPT) along with input voltage regulation (MPPT/IVR) etc., where V_{PV} is PV voltage, I_{PV} is PV current, V_b and I_b are battery voltage and current respectively and V_o and I_o are the load voltage and current. A

decision block, which represents a controller block that makes a decision based on available inputs is also shown and may be as simple as selecting the maximum or minimum of the inputs. The building blocks are local system controllers regulating a given parameter. For example, the OVR control block controls the output voltage of the system. The local controllers C1-C4 are typical PI based controller. The MPPT/IVR is a composite controller that combines the MPPT algorithm along with the input voltage regulator. The outcome of the MPPT algorithm is a voltage command for the PV converter, which is then cascaded with the IVR to generate the reference current for PWM generation. While, [20]-[33] employ various parallel or cascaded combinations of the basic building blocks, in [55], the OVR is skipped due to the dual active bridge nature of the topology and hence the output voltage is held constant by a separate voltage source. The MPPT controller is implemented by varying the duty ratio of the three phase boost converter interfacing the PV port. In [41], the battery port has been left uncontrolled so that any mismatch between PV power and load demand will be compensated by the battery naturally. The load and PV voltages are regulated by the controller using load regulation and MPPT respectively. While this approach allows for a very simple controller implementation, additional burdens are placed on the storage port, thus requiring a sufficiently large battery.

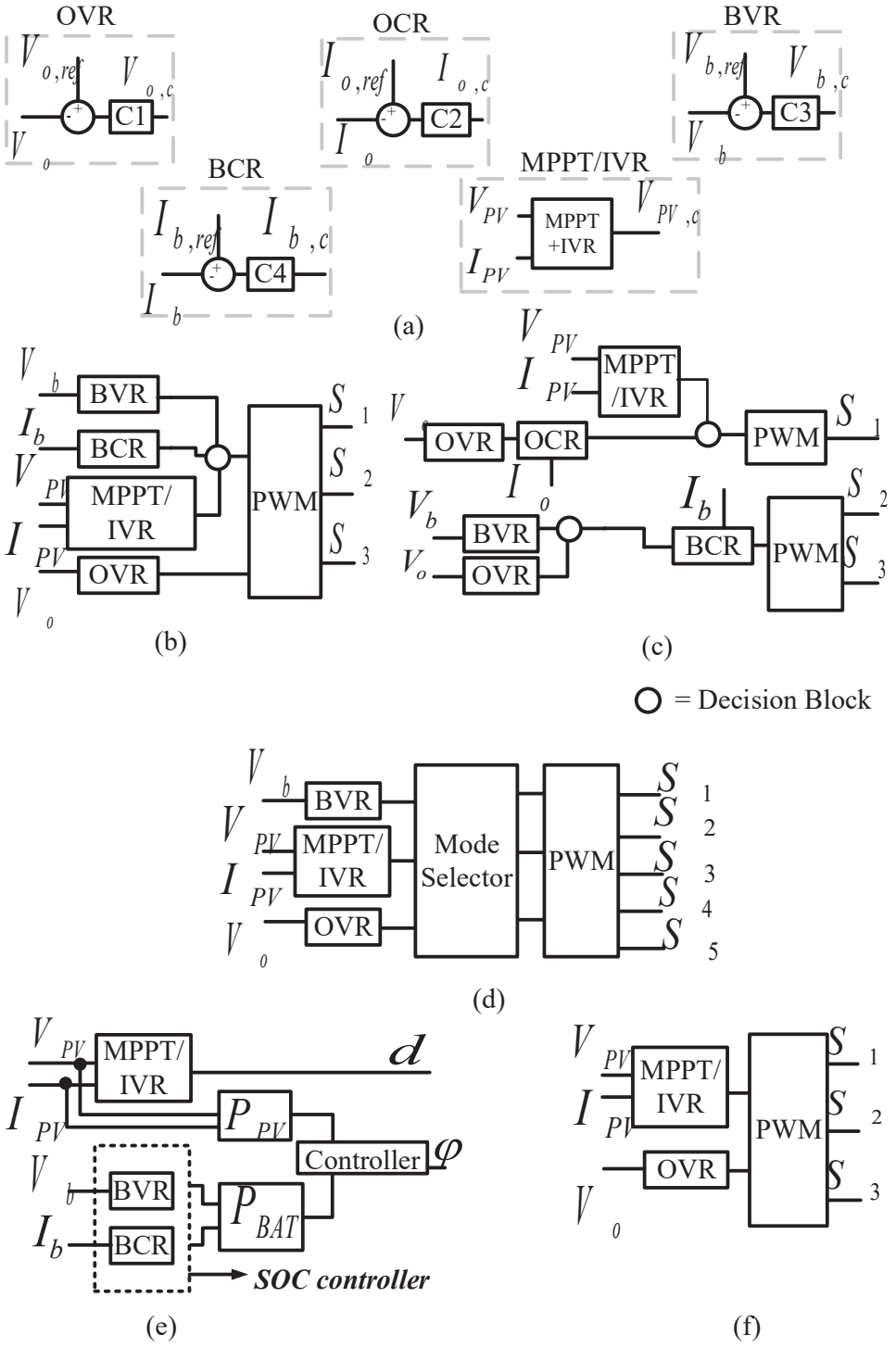

Figure 3.26: Various control architecture - (a) different generalized building blocks of control, (b)- Controller in [20], (c)- Controller in [26], (d)- Controller in [33], (e)- Controller in [55], (f)- Controller in [41]

Generally, three different control modes have been implemented, namely, "PV to Load", "PV to battery and load" and "battery to load". A mode selector block allows the controller to select the appropriate mode depending on the available measurement of local parameters [20] - [49]. Note that the three winding TPCs allows for seamless and decoupled power flow control between all ports. Therefore, with proper control of phase shift between the ports, all modes can be realized as demonstrated in [65]. A zero power port has also been realized by a implementing a zero sum of the respective ports power phasors, [65]. Other control functionalities can also be implemented in case of three winding TPC, including:

$$1)\ \sum_{n=1}^{3} P_n = 0$$

,

$$2)\ P_1 = P_2$$

This gives an increased flexibility for these types of architectures. As an example, the transition between "PV to grid" to "battery to grid" can be achieved by varying the phase shift angle between the three ports in the firmware, whereas for the other topologies, turning on/off multiple switch/relays is required.

3.5 Performance Comparison

As the MPC is broadly divided into isolated and non-isolated topologies, the performance of these topologies varies significantly. Combined input/output port and magnatic/capacitive coupled port MPCs generally have low device count and hence achieves higher efficiency. However most of the reported topologies support bi-directional power flow only between two specific ports, and therefore are less flexible. While the magnetic/capacitive coupled port MPCs offer higher voltage gain and therefore are more suitable for an intermittent power source such as PV, complexity of design increases and additional losses are introduced. The reconfigurable port MPCs share same

advantages of low device count, higher efficiency and power density, but use of slow switching devices affects the transition between power flow mode and overall dynamics becomes sloppy. Additionally, these topologies almost always offer only a single, unidirectional power flow mode in a specific configuration.

Unlike non-isolated topologies, isolated MPCs usually have higher device count, are costly, and their efficiencies are lower than most non-isolated MPCs. However, in most cases, two winding transformer coupled MPCs allow power flow between all ports simultaneously. Multiwinding transformer coupled MPCs offers additional benefit of all ports being bidirectional, thus achieve all power flow modes discussed before but at the cost of bigger core size. Increase in core size is required to allow multiple ports operate at the same time. Multi-transformer coupled MPCs retains all benefit of multiwinding transformer coupled MPCs but uses additional core and winding, thus less efficient design and performance. In addition, for all isolated topologies, the high frequency transformer provides important feature of isolation and can be used to step up/down the voltage.

Table-3.4 shows a comparison of all reviewed MPC topologies based on their relative cost, ease of implementation and control flexibility and possible power flow modes. For a fair comparison between all topologies, a cost estimate has been carried out. The cost of the MOSFET and diodes as well as the passive components such as capacitors and inductors were calculated based on their respective kVA, $\frac{1}{2}CV^2\Delta t$ and $\frac{1}{2}LI^2\Delta t$ respectively. The $\frac{1}{2}CV^2\Delta t$ and $\frac{1}{2}LI^2\Delta t$ represent the equivalent kVA rating of the passive components, so that all components are described, using same kVA units and hence their relative cost determination is simplified. $\Delta t = \frac{D}{f_{sw}}$ where f_{sw} is the switching frequency of the power stage and/or line frequency for decoupling capacitors and D is the duty ratio, which is assumed to be 0.5 for simple estimations. It has also been assumed that the energy stored in passive components is proportional to their cost, which is a good approximation based on the data presented in [76]. Some of the topologies discussed such as [32], [38], [40], have an integrated inverter. Since the pure DC-DC-DC three port converters requires an additional inverter stage, the cost of inverter was taken into account while calculating the overall cost. Finally

all costs were normalized to the cost of the topology of [20]. A commercially available 200W rated inverter cost is added to the topologies needing an external inverter and then normalized to a base cost. The size of the decoupling capacitor has been calculated as per [75] and [76] with an assumed 10% voltage ripple of a 60Hz sine wave inverter with power output P_o and DC bus voltage V_{DC}, given below:

$$C_{decouple} = \frac{P_o}{75.36V_{DC}^2} \tag{3.4}$$

Naturally, topologies in Figure 3.14 and Figure 3.11 do not require an additional decoupling capacitor as it is already integrated into the power stage. Gate drive circuitry and EMI filters were excluded from the cost calculation, so as to focus on the power conversion rather than overall packaging and commercial appeal of the power converter. From Table-3.4, it is evident that the cost of the converter is influenced by the passive devices as well as active devices and their kVA ratings. Similarly, the efficiency is also influenced by the device count since the switching and conduction losses for each device are included in the total loss. Thus majority of non-isolated topologies have lower cost, however the cost/watt parameter increases as most of them are only limited to low power application. As discussed before, only the "Multi winding transformer coupled MPC"s allow bidirectional power flow between all ports simultaneously, however, at the cost of complex and expensive three winding transformer design and gate driving circuitry, therefore the overall cost increases. In summery, the power conversion stage cost/watt is lowest for the topologies shown in Figures 3.7(b), 3.8 & 3.16, all of which with some enhancement of the hardware or the controller can achieve all modes of operation. A close second are the topologies of [65]-[68], which allows all six modes of operation and seamless transition. Finally majority of the class "Two winding transformer coupled port MPC"s achieve decent cost/watt figure with attractive efficiency and isolation at higher power ratings.

Table 3.4: Comparison of normalized cost and control/hardware limitations for the MPCs

Topology	Decoupling Capacitor (μF)	$\frac{1}{2}CV^2$ (mJ)	$\frac{1}{2}LI^2$ (mJ)	Total Passive Energy (mJ)	Normalized Cost/Watt	Achievable Power Flow modes	Power (W)	Control/Hardware complexity
Ref [20]	2064	50	0.88	974.76	1	I, III, IV, V(uni), VI	140	Output is unidirectional, bidirectional switches allow mode-II and V
Ref [26]	1592	300	21.82	8283.60	0.947	II-VI	1200	Output is directly connected to DC bus, Inverter control allows mode-I
Ref [32]	0	8.653	25.41	34.07	21.81	I-VI	800	Output is unidirectional, bidirectional switches allow mode-II and V
Ref [35]	530	8160	80	8240	0.90	I, III, IV, V(uni), VI	400	-
Ref [38]	0	66000	0	66000	11.185	I, III, IV, V	3000	Mode-II, VI not possible
Ref [41], [45]	1659	125	1.30	1453.26	0.95	I, III, IV, V(uni), VI	200	Fig. 3.16 (a)- Output is unidirectional, (b)- allows mode-II and V
Ref [49]	118	176.4	16.33	5500.58	1.26	I, III, IV, V(uni), VI	800	Output is unidirectional, bidirectional switches allow mode-II and V
Ref [50]	1326	6492	496	6989	1.62	I, III, IV, V(uni), VI	1000	Output is unidirectional, bidirectional switches allow mode-II and V
Ref [64]	7961	106690	1133.4	1067034	6.50	I-VI	6000	-
Ref [65]	221	88.2	0.32	10040.7	1.05	I-VI	1500	-
Ref [70]	1990	16000	27.78	16027	2.91	I-VI	1500	-
Ref [73]	1327	4000	26.6	4026	7.76	I-VI	1000	-

3.6 Summary

This chapter presented a comprehensive review of multi-port converter topologies for integrating PV with energy storage. The main purpose of the MPC is to provide a single stage power conversion that primarily integrates different energy sources while preserving their unique characteristics, such as MPPT for PV systems and charging/discharging capability for batteries. For example, in a standalone PV system supplying a small home, a "Peak Shaving" controller can be employed to maximize the PV power utilization. Therefore a multi-port converter which allows unidirectional power flow between PV - Load, PV - battery and battery - Load will be sufficient. If there is no need for isolation of the battery ground terminal from the load ground, a non-isolated topology may be used. Depending on the intended modes of operation, the choice of a suitable controller is also very important. The chapter further analyzes the relative cost and efficiency of various topologies, allowing a fair comparison between them. As seen from the Table-3.2 and Table-3.3, MPCs development is moving towards low power modular systems. Modular microinverters which can be used along with the MPCs to create low power (500W-1kW) rated PV and battery interface systems are also gaining much interest. With a growing residential PV market, this outcome is very significant. With the ambitious target of reducing the cost/watt for PV installations, future research will address the more efficient and cost effective design challenges at the same time retaining various feature such as isolation, modularity etc. From the discussion in this chapter, it is clear that for low power systems (<600W), non-isolated topologies are a better choice in terms of cost and efficiency, where as for higher power (>600W) isolated topologies are better suited. Thus in future research, the focus will be directed towards designing non-isolated MPCs for low power system which achieve better performance in terms of system flexibility an example of which is battery charging from grid and modularity. This allows both the PV and battery port to be bidirectional in nature and can be used interchangeably. For isolated topologies, research focus will be directed towards designing MPCs with lower device count and innovative design for improvement of cost and efficiency.

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CHAPTER 4: BIDIRECTIONAL POWER CONVERTER - "DUAL ACTIVE BRIDGE CONVERTER"

Bidirectional power conversion is important in many applications such as those involving automotive systems, fuel cell based hybrid power systems or renewable energy sources and energy storage devices. It is important to properly regulate the energy in and out of the storage device to compensate for the intermittent or sluggish nature of the renewable power source. With the recent emergence of batteries as viable energy storage devices, bidirectional charging and discharging techniques have received a renewed attention by industry and academia. Dual active bridge (DAB) converters are one of the most popular bidirectional converter topologies and have been well documented in the open literature [1]-[9]. Many possible modulation schemes for DAB have been proposed in last several decades, however based on the performance and efficiency, only handful of modulation schemes stand out. A comprehensive discussion of the modulation schemes are found in [20]. The triple phase shift modulation (TPS) has garnered a lot of attention because of its ability to achieve soft switching over the complete operational range. Synthesis of TPS modulation can be based on the phase shift between the gating signals of the two active bridges as well as between the legs of each active full bridge. There exists many possible TPS which can be equally appropriate for a given power and voltage gain. Thus, it is necessary to find the optimum TPS modulation for a given operating point which yields low switching loss, conduction loss, core loss, EMI and superior dynamic performance.

The majority of the literature focuses on exploring TPS schemes based on low rms or peak current optimization, as seen in [1],[3], [10]-[11], [14], [16], [23]. Some focuses on optimum zero voltage switching (ZVS) modulation [21]. Works presented on low rms or peak current modulation also discuss the possibility of ZVS within the optimum set, however none of these works integrate soft switching into the optimization model. It is therefore possible that the complete soft switching zone is not covered by the optimum set.

Most of the optimized TPS modulation is achieved by numerical optimization with online updation of the optimum operating point. It is difficult to generalize many different TPS modes in a single analytical expression, and therefore analytical optimization is generally not achievable. The work in [6], [11], [22] and [23] introduces harmonic analysis for the TPS schemes. It is the most well known generalization technique for all TPS schemes as well as other possible modulations for DAB, and considered to provide the best analytical model for the TPS modulation. However, the harmonic model is also highly nonlinear, rendering analytical optimization extremely difficult. In many cases numerical optimization becomes the only feasible way.

The other challenge for a fast and accurate optimization for the TPS modulation is the ability to derive an offline optimization model which can be implemented using a simple PI based controller. Previous works usually address the optimization by using an optimum controller which calculates the operating point online. This advanced controller significantly increases the cost and the control complexity, as noted in [23]. For most of the online based optimization, several CPU cycles are needed for convergence. Approaches in [3] and [14] both use a numerical solver for offline results. However it requires a controller to store offline data in large memory and is expensive to implement.

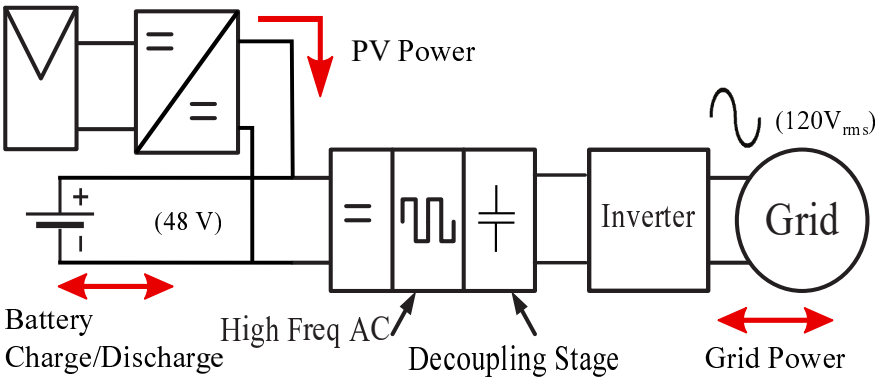


Figure 4.1: Typical application DAB for battery charge/discharge in a grid tied PV-Battery system

In [16], [17], [24] an analytical model based on the piecewise calculation of the steady state equa-

tions for DAB current stress was presented and a Karush Kuhn Tucker (KKT) or Lagrange Multiplier method (LMM) based optimality condition was derived. However, only two functional modes for TPS were considered. Most of the feasible region was left out of the analysis. Moreover, as noted in [18], such an optimization process doesnot yield a true optimum point, since the objective function is non convex in nature. In addition to that, the equality constraint is non conforming to a KKT condition and therefore doesnot guarantee a true minima for the current stress. [23] presents another approach to offline optimization based on the harmonic model where only the fundamental component is considered. In addition to the nonlinearily stated previously, this approach tends to be less accurate since only the fundamental component is considered. Authors in [18] adopt a different approach for optimizing such objective functions by checking the gradient of the objective functions iteratively at different operating points. However, being a non-convex function, a second order necessary condition is still required to be satisfied to achieve true global optima in a mathematical sense. In addition, the proposed method only considers three distinct TPS modes to cover all the power and voltage ranges, thus the global optima is restricted to the domain of the selected modes. A generalized analysis of all candidate modulations and the selection of the optimum mode for every operating point in a low, medium or high power scenarios is not presented. A discussion of soft switching and how it affects the current stress based optimization methods is also lacking.

In practical scenarios such as a battery charge/discharge system supporting grid tied PV application, both the high and low power flow range requires buck and boost mode power conversion. An example of which is bidirectional power conversion from battery voltage to line voltage, as shown in Fig. 4.1. Therefore a hybrid control structure implementing the optimum modulation for the whole operating region for the given application is necessary in order to operate at the highest efficiency.

In this chapter, the unique TPS modes have been clearly identified in the 3D space of the "Phase Shift" and "conduction angles" of the active bridges and generalized power flow and average current expressions are derived using a piecewise model. This model allowed an analytical opti-

mization framework in accordance to the nonconvex nature of the parameters. Additionaly, the proposed analytical optimization method includes the softswitching conditions and thus provides a complete solution. The harmonic model has been reintroduced for the purpose of developing a separate nonlinear model. It is used to validate the piecewise model and the analytical optimization results. Using rms current minimization approach requires soltion of nonlinear optimization, which is avoided by selectively minimizing the circulating and reactive currents that doesnot directly contribute to the output. For the controller design, the majority of the past work is focused on regulating power by phase shift. Regulating the conduction angles [6], [11] typically yielded soft switching and low rms current. Work in [23] addressed the global solution using all three degree of freedom to reach an operating point based on power flow requirement, but it did not include soft switching optimality. In this work, the optimal solution is found using all three degree of freedom (i.e phase shift and conduction angles of the two active bridges) and can be implemented by a simple PI based controller. Additionally, a hybrid controller has been proposed which switches between the appropriate TPS modes and operates at the local optima of each mode based on the power flow and output voltage requirements. The proposed hybrid controller enables the converter to operate at highest efficiency throughout the operating range without using a complex controller design or large memory controller hardware.

4.1 Review of Dual active bridge converter and modulations

Two full or half bridge structures are used for construction of a dual active bridge topology as shown in Fig. 4.2(a). A high frequency transformer is used for combining the two bridges. The transformer is not only used for isolation but the leakage inductance offered can also be used as the impedance required for regulating the current flow from the input to output or in the reverse direction. As noted in [8], the phase shifted PWM allows the control of power flow direction as well as magnitude. However, allowing the additional degree of freedom in the form of conduction angle for both the primary and secondary bridges, grants greater flexibility of control and reduced

conduction and switching losses for DAB. This chapter focuses on the use of triple phase shift (TPS) modulation modulation, where the conduction angles of the primary and secondary bridges are denoted as δ_1, δ_2 respectively, and the phase shift between the primary and secondary voltage is denoted as ϕ. In general, for single phase shift modulation (SPS), $\delta_1 = \pi$, $\delta_2 = \pi$ (Fig, 4.2(b)), for dual phase shift modulation (DPS) - δ_1 or $\delta_2 = \pi$ and δ_2 or $\delta_1 < \pi$ respectively (Fig, 4.2(c)). Finally for triple phase shift modulation (TPS), both $\delta_1, \delta_2 < \pi$. This is also demonstrated in Fig.4.2(d).

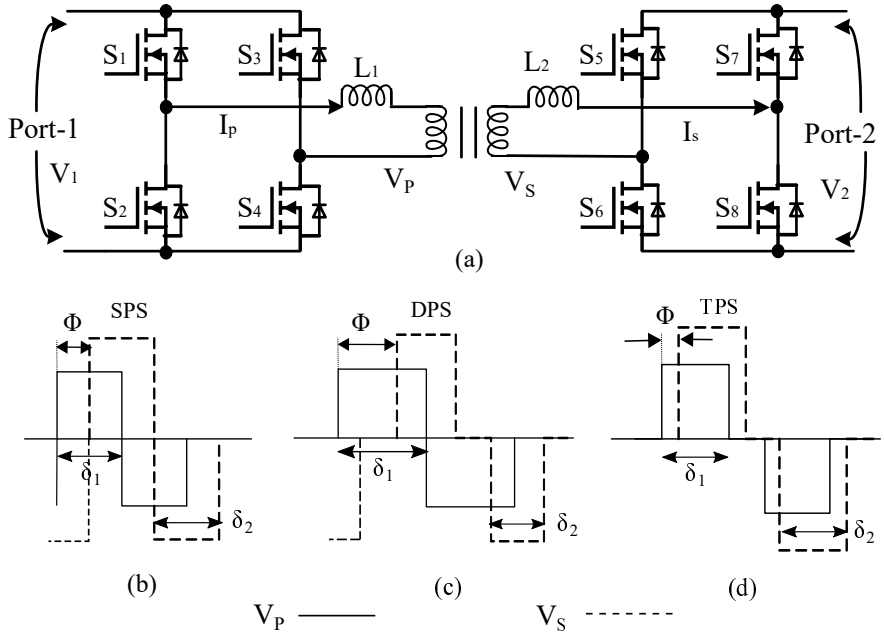


Figure 4.2: (a) Dual Active Bridge Topology (b) Different classes of modulation schemes based on conduction angle variation

The TPS scheme can be classified into six unique modes based on the phase shift and conduction angle variations. With a given range of $0 \leq \delta_1 < \pi$, $0 \leq \delta_2 < \pi$ and $0 \leq \phi \leq \pi$ over the horizontal axis - θ. The unique modes are shown in Fig. 4.3.

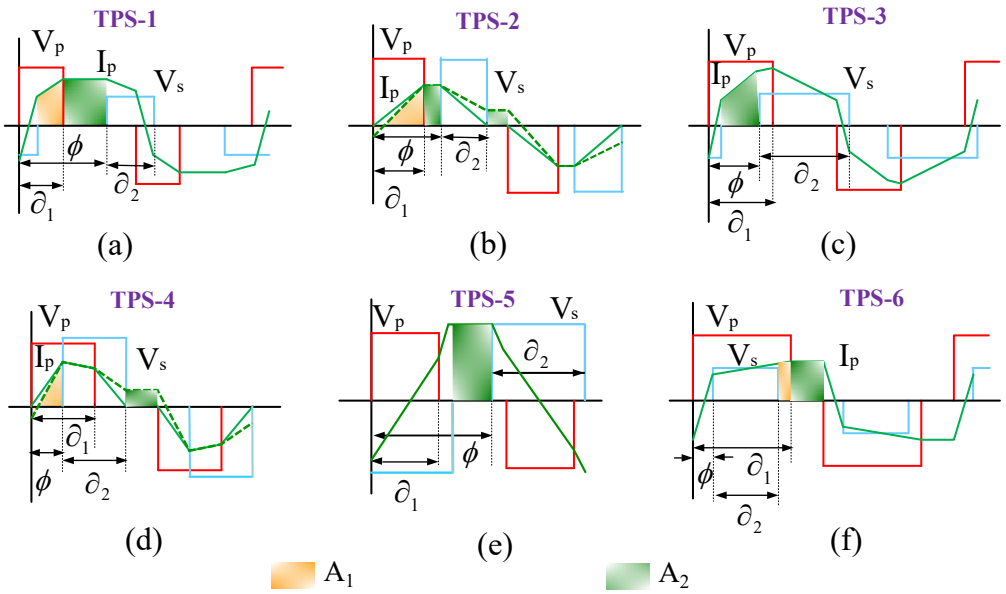


Figure 4.3: Unique modulation schemes of the TPS family based on the mode boundaries

Each of the six unique modes are restricted by specific boundaries. The mode boundaries for the six unique modes are as given in Table-4.1. For simplicity of representation, the high frequency transformer turns ratio has been assumed 1:1 through out the analysis presented in this chapter. Therefore, based on the mode boundaries specified, the volumes of each of the unique modes as a tetrahedron in the three dimensional δ_1-δ_2-ϕ space are shown in Fig. 4.4.

Table 4.1: Mode boundaries and soft switching conditions for fundamental modes

Modulation	Mode Boundary	Soft Switching condition
TPS-1	$0 \leq \delta_1 \leq \pi,\ 0 \leq \delta_2 \leq \pi,\ 0 \leq \delta_1 \leq \phi,$ $\phi + \delta_2 \geq \pi$	$\delta_1 V_1 + \delta_2 V_2 + 2\phi V_2 - 2\pi V_2 \geq 0,$ $2\delta_2 V_1 - \delta_1 V_1 + \delta_2 V_2 + 2\phi V_1 - 2\pi V_1 \geq 0$
TPS-2	$0 \leq \delta_1 \leq \pi,\ 0 \leq \delta_2 \leq \pi,\ 0 \leq \delta_1 \leq \phi,$ $\phi + \delta_2 \leq \pi$	$\delta_2 = \delta_1 \frac{V_1}{V_2}$
TPS-3	$0 \leq \delta_1 \leq \pi,\ 0 \leq \delta_2 \leq \pi,\ 0 \leq \phi \leq \delta_1,$ $\phi + \delta_2 \geq \pi$	$\delta_1 V_1 + \delta_2 V_2 + 2\phi V_2 - 2\pi V_2 \geq 0,$ $2\delta_2 V_1 - \delta_1 V_1 + \delta_2 V_2 + 2\phi V_1 - 2\pi V_1 \geq 0,$ $\delta_2 V_2 - \delta_1 V_1 + 2\phi V_1 \geq 0$
TPS-4	$\phi \leq \delta_1 \leq \pi,\ 0 \leq \delta_2 \leq \pi,\ \delta_1 \leq \phi + \delta_2 \leq \pi$	$\delta_2 = \delta_1 \frac{V_1}{V_2}, \delta_2 V_2 - \delta_1 V_1 + 2\phi V_1 \geq 0$
TPS-5	$0 \leq \delta_2 \leq \pi,\ 0 \leq \delta_1 \leq \phi,$ $\pi + \delta_1 \leq \delta_2 + \phi \leq 2\pi$	$\delta_1 V_1 + \delta_2 V_2 + 2\phi V_2 - 2\pi V_2 \geq 0,$ $2\delta_1 V_2 + \delta_1 V_1 - \delta_2 V_2 - 2\phi V_2 + 2\pi V_2 \geq 0$
TPS-6	$0 \leq \delta_1 \leq \pi,\ 0 \leq \delta_2 < \delta_1 - \phi,\ 0 \leq \phi < \delta_1$	$\delta_2 \leq \delta_1 \frac{V_1}{V_2}, \delta_2 V_2 - \delta_1 V_1 + 2\phi V_1 \geq 0,$ $\delta_1 V_1 + \delta_2 V_2 - 2\delta_2 V_1 - 2\phi V_1 \geq 0$

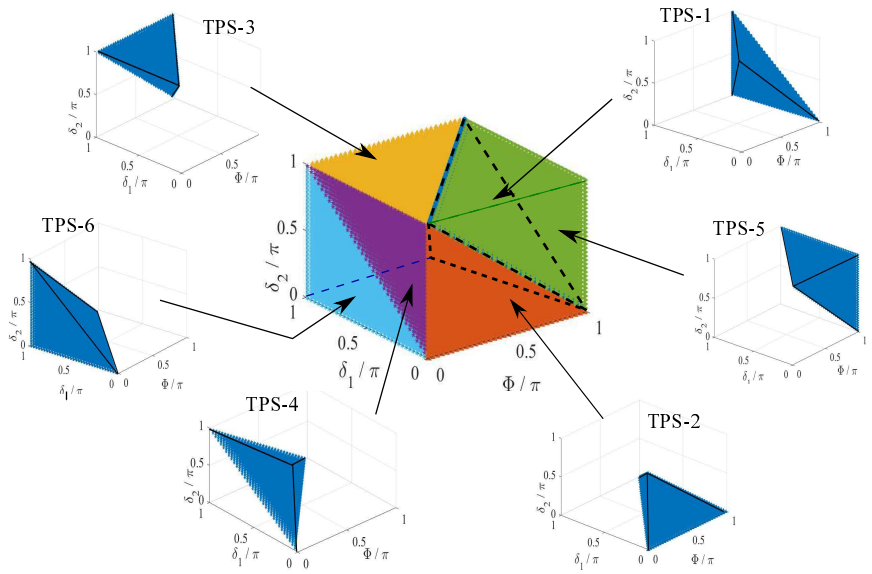


Figure 4.4: Exploded view of the six unique TPS modes in δ_1-δ_2-ϕ space

4.2 Harmonic and piecewise analytical model for TPS

The steady state equations for DAB can be solved analytically by two different methods, a piecewise integration of the transformer current over different modes over a switching cycle and by applying a harmonic analysis as attempted in [6], [11].

4.2.1 Harmonic Model

As described in [11], a generalized harmonics model can be realized using fourier series transformation on the primary and secondary voltages which are quasi square wave in nature for TPS modulation.

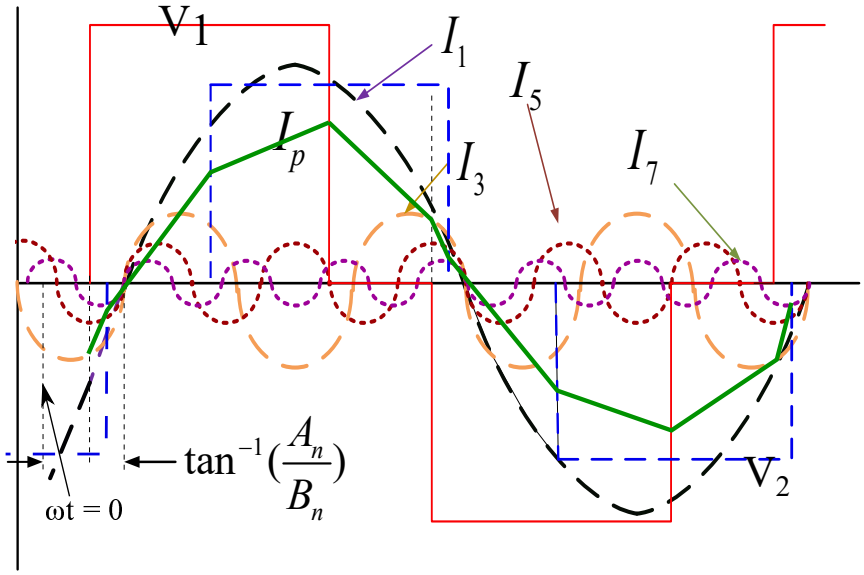


Figure 4.5: Harmonic model of the TPS scheme

The fourier series expression of V_1 and V_2 can be expressed as:

$$\begin{aligned} V_1 &= \sum_{n=1,3,5,..} \frac{4V_1}{n\pi} sin(\frac{n\delta_1}{2}) sin(n\omega t) \\ V_2 &= \sum_{n=1,3,5,..} \frac{4V_2}{n\pi} sin(\frac{n\delta_2}{2}) sin(n\omega t - n\phi) \end{aligned} \tag{4.1}$$

where n denotes the harmonics number of the fourier transform. The instantaneous and rms current can be represented by the following equation:

$$i(t) = \sum_{n=1,3,5,..} \frac{4sin(\frac{n\pi}{2})}{n^2\pi\omega L} \sqrt{A_n^2 + B_n^2}\, sin(n\omega t + tan^{-1}\frac{A_n}{B_n}) \tag{4.2}$$

where A and B are:

$$\begin{aligned} A_n &= -V_2 sin(\frac{n\delta_2}{2}) cos(n\phi) + V_1 sin(\frac{n\delta_1}{2}) \\ B_n &= -V_2 sin(\frac{n\delta_2}{2}) sin(n\phi) \end{aligned} \tag{4.3}$$

The rms current and power expressions are given as:

$$\begin{aligned} I_{rms} &= \sqrt{\sum_{n=1,3,5,..} \frac{8sin(\frac{n\pi}{2})}{n^4\pi^2\omega^2L^2}(A_n^2 + B_n^2)} \\ P &= \sum_{n=1,3,5,..} \frac{8V_1V_2 sin(\frac{n\pi}{2})}{n^3\pi^2\omega L} sin(\frac{n\delta_1}{2}) sin(\frac{n\delta_2}{2}) sin(n\phi) \end{aligned} \tag{4.4}$$

Because of the phase shift introduced in the PWM, there exists a reactive power element in the DAB converter. This was predicted by both [8] and [11]. The reactive power can be characterized by the following equation:

$$\begin{aligned} Q_1 &= \sum_{n=1,3,5,..} \frac{8V_1 sin(\frac{n\delta_1}{2})}{n^3\pi^2\omega L} A \\ Q_2 &= \sum_{m\neq n=1,3,5,..} \frac{8V_1 sin(\frac{m\delta_1}{2})}{mn^2\pi^2\omega L} \sqrt{A^2 + B^2} \end{aligned} \tag{4.5}$$

where Q_1 and Q_2 are the reactive power for $n = m$ and $n \neq m$ respectively. It has been demon-

strated in [11], [16] and [17] that the fundamental component of the harmonic model alone provides a fairly good approximation for all practical purposes. Therefore, through out this chapter, only the fundamental component of the harmonic model has been used for validating and comparing any results. A graphical representation of the harmonic analysis is shown in Fig. 4.5.

4.2.2 Piecewise Model

The piecewise model offers highly accurate and precise modelling of the DAB with TPS modulation. However the complicated expressions usually don't offer a meaningful understanding of the system most of the time, [18]. This is primarily the reason why the piecewise model has not been widely adopted in most of the prior work. However, in this work, an effort has been made to simplify the piecewise model and generalize DAB under TPS scheme to provide an optimized framework with soft switching and reduced rms current.

The power flow expression for TPS-1 to TPS-6 can be solved analytically and the expressions for normalized power flow are given as:

$$P_{TPS1} = P_m\{\mu_3 - \mu_1^2\} \tag{4.6}$$

$$P_{TPS2} = P_m\{\mu_3\} \tag{4.7}$$

$$P_{TPS3} = P_m\{\mu_3 - \mu_1^2 - \mu_2^2\} \tag{4.8}$$

$$P_{TPS4} = P_m\{\mu_3 - \mu_2^2\} \tag{4.9}$$

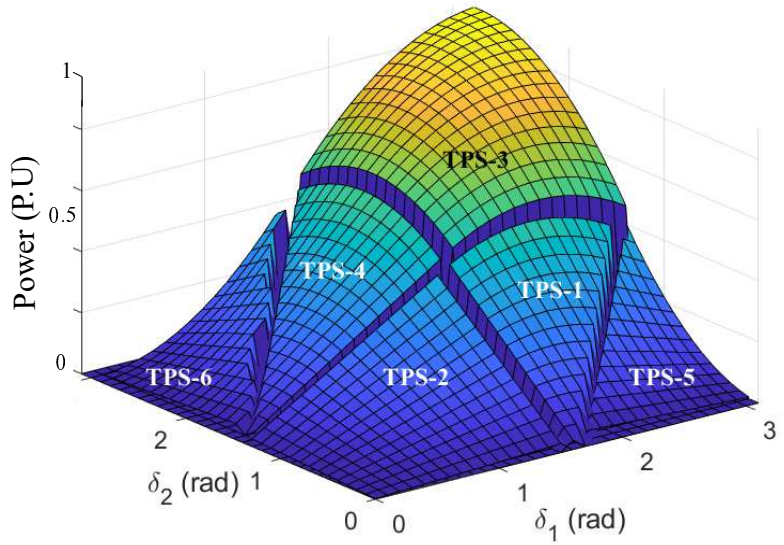
$$P_{TPS5} = P_m\{\mu_2^2 - \mu_3 + 2\pi\delta_1 - \phi^2\} \tag{4.10}$$

$$P_{TPS6} = P_m\{(\pi + \mu_1)^2 - \mu_3 - \phi^2\} \tag{4.11}$$

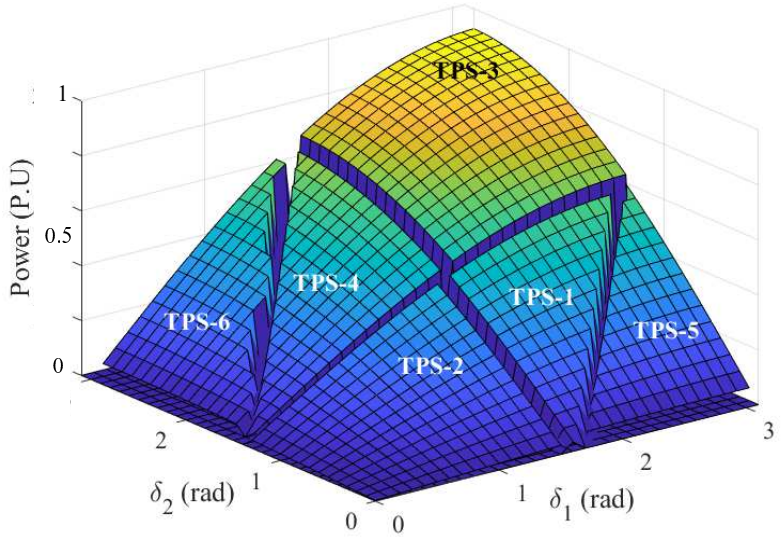
Where the additional angles introduces as μ_1, μ_2 and μ_3 are expressed as the linear and nonlinear combinations of the fundamental parameters - δ_1, δ_2 and ϕ as:

$$\begin{aligned} \mu_1 &= \phi + \delta_2 - \pi \\ \mu_2 &= \phi - \delta_1 \\ \mu_3 &= \delta_1\delta_2 \end{aligned} \tag{4.12}$$

The parameter P_m denotes the normalized maximum power. The power flow expression for both piecewise and harmonic model are presented in the Fig. 4.6 (a) and (b) respectively. It is clear from the picture that the piecewise model is in good agreement with the harmonic model. It should be noted that the harmonic model excludes a major portion of the harmonic spectrum and hence the nonlinearity is greatly reduced. This is clear from Fig. 4.6 as the piecewise model captures more nonlinearity of the power flow plot.



(a) 3D plot for the power for different TPS modes in piecewise model, corresponding to $\phi = \frac{\pi}{2}$

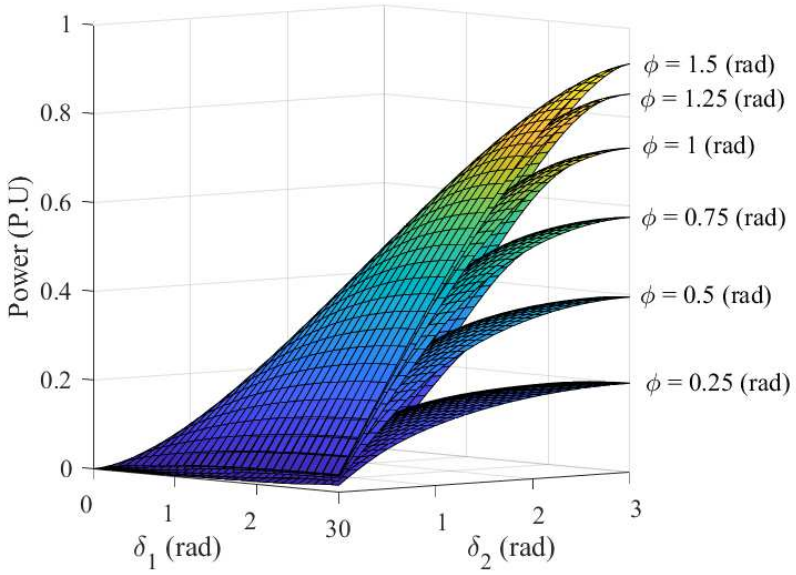


(b) 3D plot for the power for different TPS modes in harmonic model (fundamental component), corresponding to $\phi = \frac{\pi}{2}$

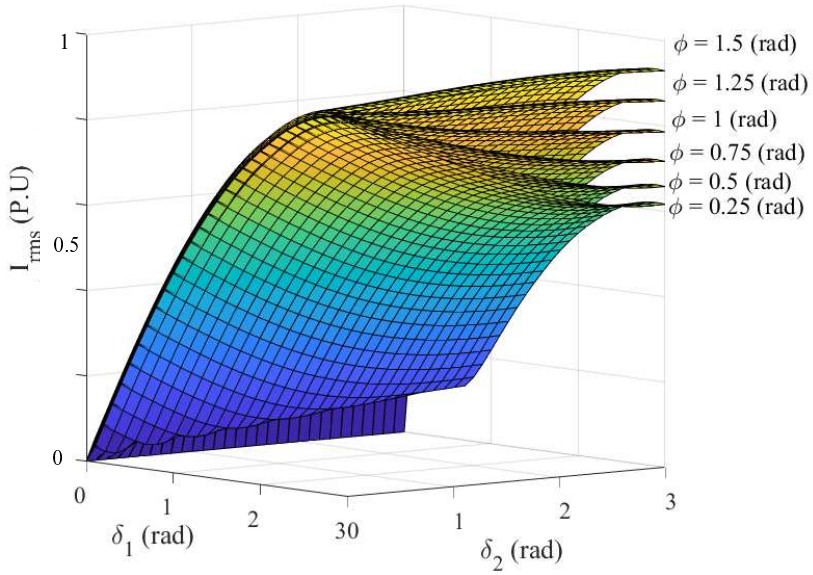
Figure 4.6: Power vs δ_1, δ_2 plot for a given ϕ

The representation is shown only for phase shift $\phi = \frac{\pi}{2}$. It is to be noted that the relation between

ϕ and the overall power flow is quadratic for a given δ_1 and δ_2 value from (6)-(12). This is further illustrated in Fig. 4.7 (a), where the harmonic model is shown for different value of phase shift strating from $\phi = 0.25\ rad$ to $\phi = 1.5\ rad$. Similarly, in Fig. 4.7 (b), the variation of the rms current vs the phase shift is shown, which similarly increases with increase in ϕ from $0.25\ rad$ to $1.5\ rad$.



(a) Variation of power flow for different ϕ in harmonic model



(b) Variation of rms current for different ϕ in harmonic model

Figure 4.7: Power and rms current plots for DAB operating in TPS

4.2.3 Soft Switching

The primary method for achieving soft switching in a DAB is by allowing the anti parallel diode of the active switches to conduct before the switch turns on, assuming ideal switches and negligible parasitics. However, this only allows a loss less turn on for the active switches. The turn off losses were mainly ignored until triangular modulation (TRM) and trapezoidal modulations (TZM) were introduced in [1], [3]. In these modulation schemes, the turn off transition of one or more active switches in the DAB happens when the transformer current reaches zero. Notably, TZM is one of the unique modulation described before, namely TPS-4. Thus, for soft switching transitions, the transformer current in the piecewise model at various point must be positive or negative. For ZVS, following conditions are to be met:

$$TPS1 : i(0) \leq 0,\ i(\phi + \delta_2 - \pi) \geq 0,\ i(\delta_1) \geq 0,\ i(\phi) \geq 0 \tag{4.13}$$

$$TPS2 : i(0) = 0,\ i(\delta_1) \geq 0,\ i(\phi) \geq 0,\ i(\phi + \delta_2) = 0 \tag{4.14}$$

$$TPS3 : i(0) \leq 0,\ i(\phi + \delta_2 - \pi) \geq 0,\ i(\phi) \geq 0,\ i(\delta_1) \geq 0 \tag{4.15}$$

$$TPS4 : i(0) = 0,\ i(\phi) \geq 0,\ i(\delta_1) \geq 0,\ i(\phi + \delta_2) = 0 \tag{4.16}$$

$$TPS5 : i(0) \leq 0,\ i(\delta_1) \geq 0,\ i(\phi + \delta_2 - \pi) \geq 0,\ i(\phi) \geq 0 \tag{4.17}$$

$$TPS6 : i(0) \leq 0,\ i(\phi) \geq 0,\ i(\phi + \delta_2) \leq 0,\ i(\delta_1) \geq 0 \tag{4.18}$$

Note that, ZVS is not feasible for all switches in all the TPS modes. TPS-2 and 4, do not allow ZVS at $i(0)$ and at $i(\phi + \delta_2)$ points. If $i(\phi + \delta_2) \leq 0$, Then the $i(0) \leq 0$ condition is never satisfied, and hence atleast one switch will lose ZVS. The switching transition and operations under different current breakpoints in the piecewise model is discussed in details in [12]. For a high current application, zero current switching (ZCS) prevents any turn off loss, and can be proved to be more effective [1].

Based on above analysis and equations (12)-(17), the soft switching conditions can be summarized from the steady state equation of the TPS modes. The soft switching conditions are as shown in Table-4.1. It is observed that, there are some redundancies between the soft switching conditions and the mode boundaries presented in Table-4.1. In some cases, simply following the mode boundary and some additional inequality will ensure soft switching for the specific mode. One such example is the equality: $\delta_2 V_2 = \delta_1 V_1$. Satisfying this expression along with the mode boundary ensures soft switching for TPS-2,4 and 6. This finding will be further explored in the following section where an optimized operating point will greatly simplify the soft switching condition and mode boundaries.

4.2.4 Power Flow and Voltage Ranges for TPS

The power flow expression given in (6)-(12) for the piecewise model conveys an important relationship between the input and output voltage and the overall power flow. Clearly, the higher voltage enables higher average and rms current and hence increased power flow. In order to maintain soft switching over wide operation range, the voltage gain ($\frac{V_2}{V_1}$) plays an important part. This has been illustrated for the generalized trapezoidal modulation or TPS-3 in [12]. Here, a detailed analysis of each unique TPS mode has been carried out. The effective mode boundary is reinforced with the soft switching conditions given in Table-4.1 to generate the loss less operation region over the power flow and voltage ratio range as shown in Fig. 4.8. The regions are obtained by sweeping through the $\delta_1 - \delta_2 - \phi$ space, and plotting the feasible points within mode boundary and enclosed

by the soft switching inequalities. It is observed that there are multiple operating points possible for a given power and voltage ratio. Thus there exists multiple combination of δ_1, δ_2, ϕ for a given power which can lead to different rms currents.

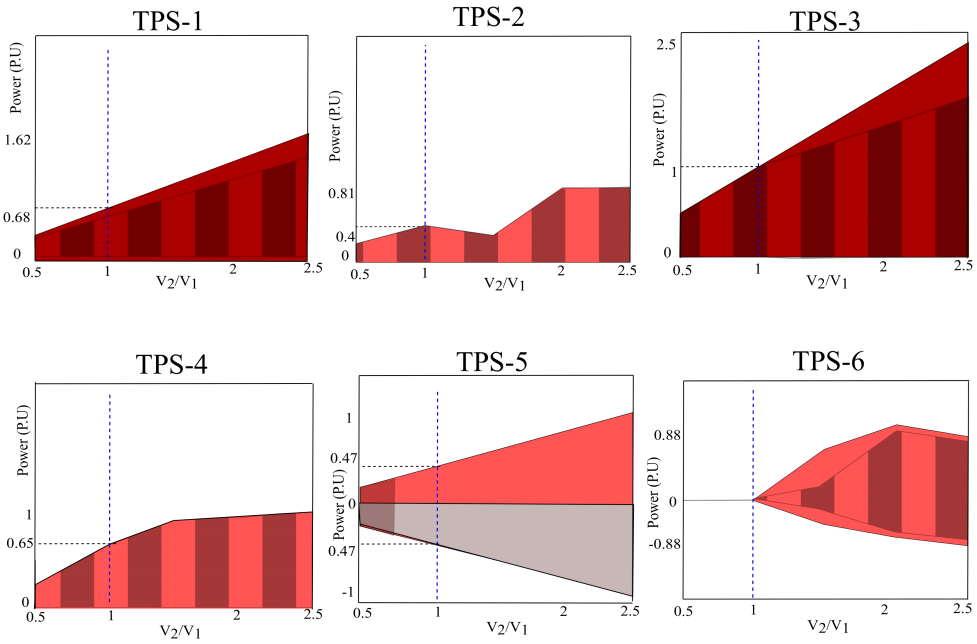


Figure 4.8: Power (in P.U) vs Voltage (in voltage gain) range for the TPS modulations maintaining soft switching

As it is seen from the Fig. 4.8, each fundamental TPS modulation offers wide power and voltage ranges throughout its "soft switched operating range". The maximum power swing is offered by TPS-3, followed by TPS-1 and TPS-5. TPS-2, 4 and 6 generally provides lower power ranges. This can be seen in the figure where the output to input voltage ratio is aligned across the horizontal axis and the power flow is plotted on the vertical axis. The power flow in buck ($V_2 < V_1$) and boost ($V_2 > V_1$) mode is separated by the dotted line on the plots. It is to be noted that the power flow in buck and boost modes is significantly different in some cases. For example, TPS-6 doesn't offer any buck mode power flow at all, if soft switching is to be maintained. Similarly, TPS-2 and TPS-4 offer wider power flow range in boost mode compared to buck mode.

4.3 Optimized Triple Phase Shift Modulation

Based on the previous analysis, it appears that each of the TPS modulations are able to achieve relatively wider power flow ranges for a wide voltage ratio, with some exceptions as discussed. Clearly, for high power applications, TPS-3 or TPS-1 are obvious choices. However, for lower power applications, the solution is not easily obtained and generally an optimization framework is required. One of the most practical optimizable parameter for this problem is the rms current as discussed before.

Lower rms current leads to higher efficiency by reducing conduction loss, core loss etc. A similar approach of reducing the rms current for the given power flow has been explored in [13], [14] and [18]. However, the rms current expression is complex because per the piecewise model, as it is typically consists of nonlinear terms. Nonlinear equations renders analytical optimization unsolvable in some cases and numerical solution is the only feasible way. Therefore, for the piecewise model, the average transformer current over one half of the switching cycle has been used as the minimizable function.

4.3.1 Non-convexity and Analytical Optimization with Soft switching

As noted in the introduction, the rms, average current and power flow expression are all non-convex and non-affine functions. The tools such as KKT condition or simple LMM doesn't produce local or global optima. The LMM usually indicates a stationary point on the minimizable function curve which can lead to either a maxima, minima or a saddle point, and it is impossible to decide the nature of the stationary point with out checking the second order necessary condition (SONC). Therefore, the non convex optimization has been formulated so that the correct optima (minima) is reached. It is also verified that the local minima is also a global minima for the specific modulation.

Since in this case, the local optimal point for the objective function (average transformer current

over one half of the switching cycle) lies orthogonal to the equality constraint (power flow expression) and is subject to the inequality constraints (soft switching conditions), the local optimization problem in terms of KKT can be expressed as following:

$$\begin{aligned} &minimize\ f(\theta) = i_{avg} \\ &subject\ to\ g_i(\theta) \leq 0,\ i = 1, 2, ..p \\ &\quad h_j(\theta) = 0,\ j = 1, 2, ..q \end{aligned} \tag{4.19}$$

where $f(\theta)$ is the minimizable function, $g(\theta)$ is the function representing inequality constraints, and $h(\theta)$ represents equality constraint. θ is function of δ_1, δ_2, ϕ.

The optimization problem can be solved by using LMM within the local boundary where the inequality constraints are bounding. Thus the problem can be reformulated as:

$$\begin{aligned} &min \\ &J(f, g, h, \theta, \lambda_{1,j}, \lambda_{2,i}) = |f(\theta)| + \sum_j \lambda_{1,j}\ h(\theta) \\ &+ \sum_i \lambda_{2,i}\ g(\theta) \end{aligned} \tag{4.20}$$

where j is the objective function and $\theta = \omega t$. λ_1 and λ_2 are lagrange coefficients and $\lambda_1 \geq 0$ and $\lambda_2 \geq 0$. The objective function tries to find the mimina of the average current, $f(\theta)$, thus the absolute value of the function is used.

Table 4.2: Normalized average currents for different TPS Schemes over half of switching cycle ($\frac{1}{I_m}\int_0^\pi i(t)dt$)

Mode	Normalized i_{avg}
TPS-1	$-(V_1\delta_1^2 - V_1\pi\delta_1 + V_2\delta_2^2 + 2V_2\delta_2\phi - 3V_2\pi\delta_2 + 2V_2\phi^2 - 4V_2\phi\pi + 2V_2\pi^2)$
TPS-2	$\delta_1\delta_2V_1 - \delta_1^2V_1 + \delta_1\phi V_1 + \delta_2\phi V_2$
TPS-3	$-(V_1\delta_1^2 - V_1\pi\delta_1 + V_2\delta_2^2 + 2V_2\delta_2\phi - 3V_2\pi\delta_2 + 2V_2\phi^2 - 4V_2\phi\pi + 2V_2\pi^2)$
TPS-4	$\delta_1\delta_2V_1 - \delta_1^2V_1 + \delta_1\phi V_1 + \delta_2\phi V_2$
TPS-5	$-(V_1\delta_1^2 - V_1\pi\delta_1 + V_2\delta_2^2 + 2V_2\delta_2\phi - 3V_2\pi\delta_2 + 2V_2\phi^2 - 4V_2\phi\pi + 2V_2\pi^2)$
TPS-6	$\delta_2^2V_2 - \delta_1^2V_1 + \pi\delta_1V_1 - \pi\delta_2V_2 + 2\delta_2\phi V_2$

The individual average currents for each modulation scheme are given in Table-4.2, where I_m is the maximum average current. Here, the average current expression for TPS-1, 3 and 5 are smiliar and TPS-2 and TPS-4 are the same as well. The optimization results provide a global solution for TPS-1,3,5 and for TPS-2 and 4 separately. Therefore, using the objective function given in (4.20), a locally optimized solution can be obtained. A closed form solution doesnot exist since both the minimizable function and the equality constraint are non convex and non affine in nature respectively [15]. Thus in order to obtain a closed form analytical solution, the equality constraint must be an affine function. This could be achieved by linearizing the power flow expression in the neighborhood of the optimum point. However, this is based on the assumption that there exists an optimum point inside the feasible region ($\mathcal{F}$), at a finite and real location (i.e real number $\Re$). Following equation summarizes the postulate and the linear expression of the equality constraint:

Assumption:

If $\{\delta_1^*, \delta_2^*, \phi^*\}$ is the optimum solution and $\{\delta_1^*, \delta_2^*, \phi^*\} \in \mathcal{F}$, where, $\mathcal{F} \subset \Re$.

The equality constraint is differentiable and the linearized expression in the neighborhood of $\{\delta_1^*, \delta_2^*, \phi^*\}$ is given as:

$$P_o = C_1\delta_1 + C_2\delta_2 + C_3\phi + C_4 \tag{4.21}$$

where, $C_1, C_2, C_3, C_4 = f(\delta_1^*, \delta_2^*, \phi^*)$ and $\mathcal{F}$ is the feasible region enclosed by the mode boundaries given in Table-4.1. Hence, an affine expression for the equality constraint $h(\theta) = P_o - C_1\delta_1 - C_2\delta_2 - C_3\phi - C_4$ is obtained.

Solving the optimization problem of (4.20) with modified equality constraint, yields the optimum - $\delta_1^*, \delta_2^*, \phi^*$. However, since the value of C_1, C_2, C_3 and C_4 are not deterministic and depends on the optimal point itself, an independent value of the optimum point is still not achievable. Solving (4.20), the following relationship between the optimal parameters can be obtained, which reduces the number of unknown parameters to only one.

$$\left.\begin{aligned} \delta_2 V_2 &= \delta_1 V_1 \;\; (TPS-2,4) \\ \delta_2 V_2 &\leq \delta_1 V_1 \;\; (TPS-1,3,5,6) \end{aligned}\right\} \tag{4.22}$$

$$\left.\begin{aligned} \phi + \delta_2 &\geq \pi, \quad (TPS-1,3,5) \\ \phi - \delta_1 &\leq \pi, \quad (TPS-5) \\ \phi &\geq 0, \quad (TPS-4,6) \end{aligned}\right\} \tag{4.23}$$

Equation (4.22) and (4.23) ensures soft switching operation over the feasible region for a given power flow. Note that, since TPS-2 has an unique solution for the soft switching condition per Table-4.1, the optimization problem is not valid for this particular mode since it always points to the unique solution for a given power flow. TPS-5 has an extra inequality to ensure soft switching of the primary bridge during the positive to zero level transition, as given in (23). For the group (TPS-4 and 6), the optimum solution effectively reaches TRM described in [1], [3] and achieves higher efficiency in the process.

As, determined previously, the objective function is non convex. Even though linearization of the nonlinear equality constraint $g(\theta)$ allows the problem to be formulated in LMM, there is no guarantee that the solution obtained will be local minimum. Thus, for the "sufficiency condition", the next step of the operation is to check the optimality by finding the SONC [19]. This can be verified by checking the positive definiteness of the hessian matrix (H) of J. Where $H = \Delta^2 J$, Δ^2 represents the second partial derivative of J with respect to δ_1, δ_2 and ϕ.

$$H = \begin{bmatrix} \frac{\Delta^2 J}{\Delta \delta_1^2} & \frac{\Delta^2 J}{\Delta \delta_1 \Delta \delta_2} & \frac{\Delta^2 J}{\Delta \delta_1 \Delta \phi} & \frac{\Delta^2 J}{\Delta \delta_1 \Delta \lambda_{1,j}} & \frac{\Delta^2 J}{\Delta \delta_1 \Delta \lambda_{2,i}} \\ \frac{\Delta^2 J}{\Delta \delta_1 \Delta \delta_2} & \frac{\Delta^2 J}{\Delta \delta_2^2} & \frac{\Delta^2 J}{\Delta \delta_2 \Delta \phi} & \frac{\Delta^2 J}{\Delta \delta_2 \Delta \lambda_{1,j}} & \frac{\Delta^2 J}{\Delta \delta_2 \Delta \lambda_{2,i}} \\ \frac{\Delta^2 J}{\Delta \delta_1 \Delta \phi} & \frac{\Delta^2 J}{\Delta \phi \Delta \delta_2} & \frac{\Delta^2 J}{\Delta \phi^2} & \frac{\Delta^2 J}{\Delta \phi \Delta \lambda_{1,j}} & \frac{\Delta^2 J}{\Delta \phi \Delta \lambda_{2,i}} \\ \frac{\Delta^2 J}{\Delta \delta_1 \Delta \lambda_{1,j}} & \frac{\Delta^2 J}{\Delta \delta_2 \Delta \lambda_{1,j}} & \frac{\Delta^2 J}{\Delta \phi \Delta \lambda_{1,j}} & \frac{\Delta^2 J}{\Delta \lambda_{1,j}^2} & \frac{\Delta^2 J}{\Delta \lambda_{1,j} \Delta \lambda_{2,i}} \\ \frac{\Delta^2 J}{\Delta \delta_1 \Delta \lambda_{2,i}} & \frac{\Delta^2 J}{\Delta \delta_2 \Delta \lambda_{2,i}} & \frac{\Delta^2 J}{\Delta \phi \Delta \lambda_{2,i}} & \frac{\Delta^2 J}{\Delta \lambda_{1,j} \Delta \lambda_{2,i}} & \frac{\Delta^2 J}{\Delta \lambda_{2,i}^2} \end{bmatrix}$$

Where Δ is the partial differential operator. For a positive definite hessian matrix, i.e ($\Delta^2 J \geq 0$), the eigen values of the hessian should be greater than zero. This is verified for every TPS local optimal solution.

From (6)-(11), (22), (23), the power flow can be controlled efficiently by commanding only one parameter. The power vs voltage ratio plot is modified according to the results from (22) and (23) with the striped area on top of the original soft switched region in Fig. 4.8. Since the optimization problem finds the solution on the enclosed region boundary, the effective soft switching area is reduced. This is a trade off to achieve a global solution.

It is to be noted that the solution in (22) and (23) is actually not dependent on the objective functions since the number of equality constraints are the same as the number of unknown variables. The optimum solutions here, are simply the solution of the equality constraints (soft switching conditions).

Table 4.3: Optimizers for minimum current without soft switching

Modulation	f_1 (Normalized)	f_2 (Normalized)	Optimum $\delta_1^*, \delta_2^*, \phi^*$ without Soft switching
TPS-1	$\delta_2 V_1 + \delta_2 V_2 + \phi V_1 - \pi V_1$	$\delta_1 V_1 + \delta_2 V_2$	$\delta_1^* = \frac{1}{V_1}\sqrt{\frac{8\pi V_2 \bar{P}_o}{\mathcal{U}_1}}, \delta_2^* = w\sqrt{\frac{8\pi \bar{P}_o}{V_2 \mathcal{U}_1}}, \phi^* = \pi - \frac{1+w}{2}\sqrt{\frac{8\pi \bar{P}_o}{V_2 \mathcal{U}_1}}$
TPS-2	$\delta_2 V_2$	$\delta_1 V_1 \pm \delta_2 V_2$	$\delta_1^* = \frac{1}{V_1}\sqrt{\frac{2\pi \bar{P}_o}{w}}, \delta_2^* = \frac{1}{V_2}\sqrt{2\pi \bar{P}_o w}, \phi^* = \delta_1^*$
TPS-3	$\delta_2 V_1 - \delta_1 V_1 + \delta_2 V_2 + 2\phi V_1 - \pi V_1$	-	$\delta_1^* = \pi, \delta_2^* = \pi \pm V_2\sqrt{\frac{\pi \mathcal{U}_2}{V_1 V_2 (V_1^2 + V_2^2)}}, \phi^* = \frac{\pi}{2} \pm (V_1 - V_2)\sqrt{\frac{\pi \mathcal{U}_2}{V_1 V_2 (V_1^2 + V_2^2)}}$
TPS-4	$\delta_2 V_2 - \delta_1 V_1 + \phi V_1$	$\delta_1 V_1 - \delta_2 V_2$	$\delta_1^*(\phi^*) = \sqrt{\frac{\mathcal{U}_3}{V_1(V_2 - V_1)}}, \delta_2^*(\phi^*) = \frac{2V_2 - V_1}{V_2}\sqrt{\frac{\mathcal{U}_3}{V_1(V_2 - V_1)}} - 2\phi^*$
TPS-5	-	$\delta_1 V_1 + \delta_2 V_2$	No Solution
TPS-6	$\delta_2 V_1 - \delta_2 V_2 + \phi V_1$	$\delta_1 V_1 - \delta_2 V_2$	$\delta_1^*(\phi^*) = 2\phi^* - \frac{V_2 - V_1 - wV_1}{V_1}\sqrt{\frac{2\pi \bar{P}_o}{wV_2(V_2 - V_1)}}, \delta_2^*(\phi^*) = \sqrt{\frac{2\pi \bar{P}_o w}{V_2 - V_1}}$

Where $\mathcal{U}_1 = 4V_2 w + 2V_1 w - V_1 - V_1 w^2$

$$\mathcal{U}_2 = \pi V_1 V_2 - 4\bar{P}_o$$

$$\mathcal{U}_3 = \phi^{*2} V_1 V_2 + 2\pi \bar{P}_o$$

$$\bar{P}_o = P_o \omega L$$

4.3.2 Analytical Optimization without soft switching

As previously discussed, when using soft switching conditions as inequality constraints, the solution lies at their intersection and doesnot necessarily represent the minimum average or rms current. Ultimately, it is important to achieve a low rms current while maintaining soft switching. The optimization problem can be reformulated by focusing on minimizing the rms current and not considering the soft switching conditions. Eventually, the optimization results for "with"

and "without" soft switching can be combined to find the optimum point. In this subsection, the optimization without soft switching is considered. This allows LMM to be a candidate for the optimization and thus the restrictions of using the affine equality constraint are removed. However, the non convex objective function is still not solvable with sufficiency when using the LMM. Instead of using the average or rms value of the current over the entire period (0, π), the shaded area A_1 and A_2 as shown in Fig. 4.3 has been considered as the objective function. Since the soft switching condition is excluded from this analysis, the ideal current wave forms for TPS-2 and 4 are different. This is as shown in Fig. 4.3 by the dashed line. Areas, A_1 and A_2 represent the portion of the current which doesn't contribute to the output power. A_1 is the integral of the current when the secondary voltage is zero, thus circulates through the source and the overlapping switches of the secondary bridge. A_2 is the integral of the current during both primary and secondary voltage is zero and hence simply circulates through the overlapping switches in primary and secondary. The circulating current contributes to the overall conduction loss and core loss. Minimizing them reduces the overall rms current as well as peak current, without affecting the output power flow.

The average current for the areas A_1 and A_2 can be obtained by dividing the areas by the angle spans (θ_1 and θ_2) across them: $f_1 = \frac{A_1}{\theta_1}$ and $f_2 = \frac{A_2}{\theta_2}$. Note that for TPS-6, the interval ($0 \leq \theta \leq \phi$) is excluded. This area and the interval ($\phi + \delta_2 \leq \theta \leq \delta_1$) both can be classified as A_1, and hence when they are added, the optimizer will attempt to equalize the negative and positive area. This will minimize the objective function but not necessarily minimize the overall rms current. A similar problem is encountered by TPS-2 and TPS-4 as well. However, in this case the soft switching condition forces the zero crossing of the current to be at $\theta = 0$. Thus the erroneous solution found by the optimizer is canceled when the optimization results for both "with" and "without soft switching" are combined.

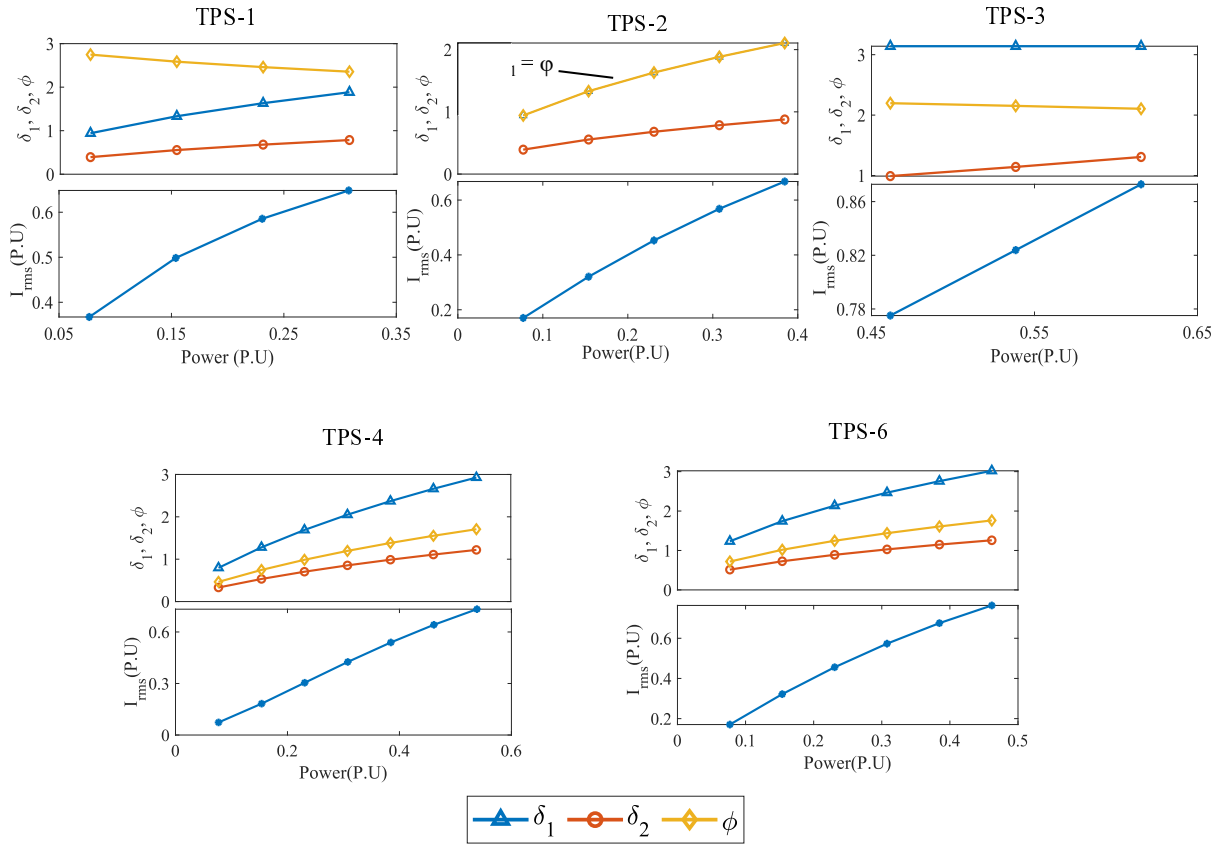


Figure 4.9: Variation of δ_1, δ_2 and ϕ over the power flow range optimizing the rms current for boost mode operation ($\frac{V_2}{V_1} = 2.5$)

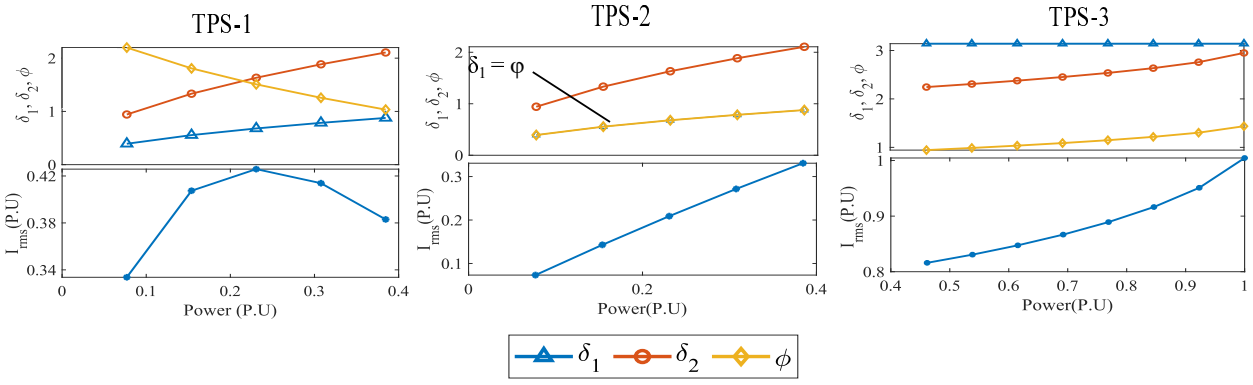


Figure 4.10: Variation of δ_1, δ_2 and ϕ over the power flow range optimizing the rms current for buck mode operation ($\frac{V_2}{V_1} = 0.5$)

Thus, the optimization problem can be reformulated as a multi-objective optimization problem as:

$$\begin{aligned} &min \\ &J(f,g,h,\theta,\lambda_{1,j}) = \underbrace{w|f_1(\theta)| + w^{'}|f_2(\theta)|}_{O(\theta)} + \sum_j \lambda_{1,j}\ h(\theta) \end{aligned} \tag{4.24}$$

where $0 \leq w \leq 1$ is a weighting factor and $w^{'} = (1-w)$. $O(\theta)$ is the composite objective function as shown in (4.24). Equations (6) - (11) can now be used as equality constraint, and directly used in the optimization problem. The problem is solved in the Matlab symbolic toolbox environment by solving the nonlinear equations formed by:

$$\nabla_{\delta_1,\delta_2,\phi,\lambda_1} J = 0 \tag{4.25}$$

The solution to the modified optimization problem is given in Table-4.3. Note that the solution for TPS-5 is invalid since it produces complex numbers. Also, the solutions for TPS-4 and 5 are not independent and instead are represented as functions of optimum ϕ.

Based on (4.22), (4.23) and the results produced in Table 4.3, all of the optimum solutions except TPS-3, also follow the soft switching conditions. For TPS-3, buck mode always ensures soft switching, but boost mode soft switching conditions are not always automatically satisfied and needs to be combined with minimum current conditions. It should also be noted that $w = 0$ produces invalid optimization results and thus is ignored when finding the optima. Similarly, any complex number solution is also ignored.

In Fig. 4.9 and Fig. 4.10, the trajectory of δ_1^*, δ_2^* and ϕ^* is shown for the boost and buck mode operation respectively. The voltage ratios 2.5 and 0.5 for boost and buck mode are shown, respectively. The optimum values of the conduction and phase shift angles are obtained form Table-4.3, which is based on minimizing the average current areas as discussed before. A rms current plot also accompanies δ_1^*, δ_2^* and ϕ^* trajectories, showing the rms current at these operating points, where

the I_{rms} is obtained from the harmonic model. The power and rms current values are normalized based on the maximum power and rms current.

4.4 Hybrid Modulation for wide operating range

Based on the analysis of the previous section, it can be determined that the modulations for TPS-1 to 6 can be combined into a hybrid modulation scheme. This allows minimum current over a wide range of power flow, both for buck and boost modes. As seen in Fig. 4.9, during the boost mode, TPS-4 allows minimum current up to 0.55 p.u power flow. After that point, only a small increment in power flow with minimum loss can be achieved by TPS-3. Afterwards, SPS can be used for optimum modulation. Hence, a hybrid scheme can be formulated using TPS-4, 3 and SPS for boost mode operation. Similarly for buck mode (Fig. 4.10), only TPS-1,2 and 3 are feasible, but only TPS-2 and 3 based hybrid modulator improves efficiency.

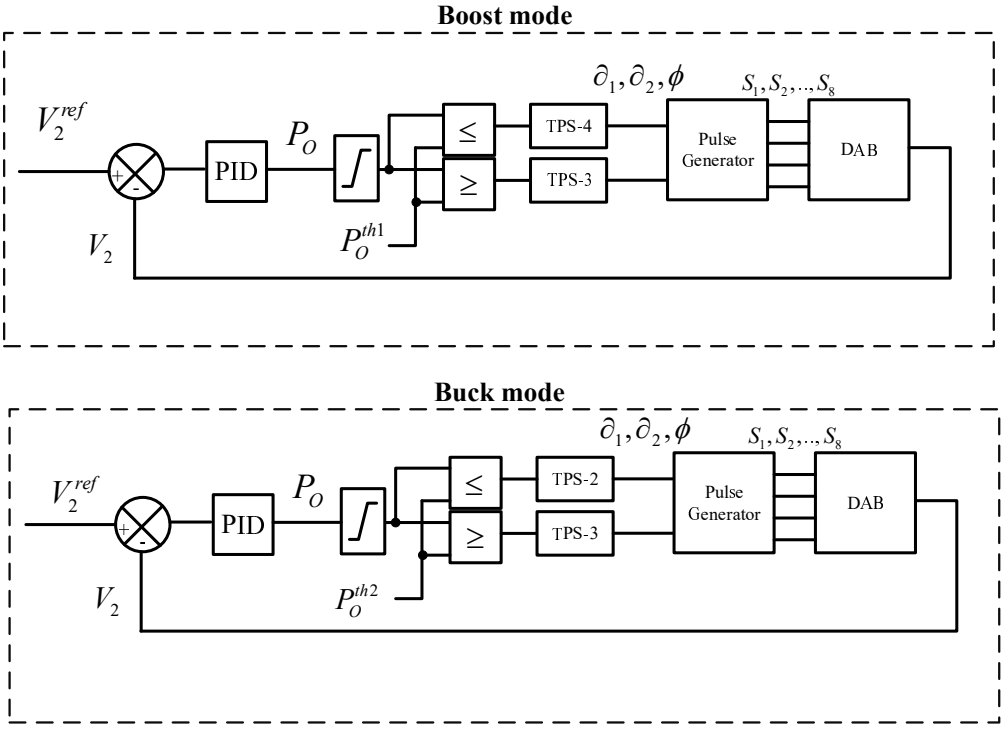


Figure 4.11: Closed loop controller architecture with hybrid modulation for both buck and boost mode operation

It is noted in Fig.4.9 and 4.10, that for the boost mode hybrid controller, the threshold of power flow between TPS-4 and TPS-3 is reached at the mode boundary, when $\delta_1 = \pi$. Thus, analytically the power threshold becomes:

$$P_o^{th_1} = P_m \phi \left(\delta_1 - \phi\right)$$

with operating point at:

$$\{\phi, \delta_1, \delta_2\} = \{\pi(1 - \frac{V_1}{V_2}),\ \pi,\ \frac{V_1}{V_2}\pi\}$$

The expression of power can be found in [12], as the optimum modulation for TPS-4 is TRM modulation. TPS-3 is used from P_o^{th1} up to 0.65 P.U. SPS can be used for the rest of the power flow range. Similarly for buck mode, the power flow threshold between TPS-2 and TPS-3 is found when the boundary condition $\delta_1 + \delta_2 = \pi$ is reached. Hence the power flow expression can be

written as:

$$P_o^{th_2} = P_m \frac{V_1}{V_2} \phi^2$$

with the operating point at:

$$\{\phi, \delta_1, \delta_2\} = \{\frac{V_2 \pi}{(V_1 + V_2)}, \frac{V_2 \pi}{(V_1 + V_2)}, \frac{V_1 \pi}{(V_1 + V_2)}\}$$

Power flow from $P_o^{th_2}$ to 1 P.U is obtained by TPS-3 modulation. A closed loop controller based on the threshold powers are shown in Fig. 4.11, where the operating TPS modes are changed accordingly. From the analysis in [22], for a control oriented model, the effect of the inductor can be ignored and this produces a constant transfer function as no other dynamics present in the approximated circuit. Thus the output power can be proportionally controlled by simply varying phase shift or the conduction angles.

4.5 Experimental Results

In order to validate the proposed optimized modulation scheme as well as the hybrid modulation, a 200W prototype was built. The primary voltage used for the experiment was 32V and secondary voltage was 48V. Both the voltages are varied by $\pm 5V$ for wide voltage range validation. A 48V DC bus is commonly used in PV battery systems, and is also a very popular choice for electric transportation systems. A high frequency transformer was designed with turns ratio of 1:1, and negligible leakage inductance. An external auxiliary inductance of $10\mu H$ was added on the primary side. Utilizing an 1:1 transformer allowed verification of the hybrid modulation over a wider operating range in both buck and boost mode. The output was filtered using a $100\mu F$ capacitor. An output resistive load was used instead of DC voltage source. The primary and secondary switches were realized by using SUM10250GE3 mosfets, which have low $R_{ds,on}$ of around 0.031Ω. The converter was operated at a constant switching frequency of $50kHz$. Both buck and boost mode hybrid modulation as demonstrated in Fig. 4.11 was verified through experimental results.

From Table-4.3, the optimum operating point for TPS-3 was approximated to a much simpler expression as $\delta_2^* = 3.14 - \sqrt{6.83 - 0.04P_o}$ and $\phi^* = 1.57 + \sqrt{0.43 - 0.003P_o}$ for the given input and output voltage of 32V and 48V respectively. For buck mode, i.e input and output voltage being 48V and 32V respectively, the expression for δ_2 changed to $\delta_2 = 3.14 - \sqrt{3.03 - 0.02P_o}$ while the phase shift expression remained same. δ_2^*, ϕ^* were represented in rad here. The transition between TPS-4 to TPS-3 (boost mode) or TPS-2 to TPS-3 (buck mode) was determined by the threshold power as shown in Fig. 4.11. This requires measurement of output current in addition to output voltage. In a cost effective design, additional sensing is not desired. Since the proposed closed loop controller utilizes the monotonically increasing relation between power and δ_1, the power thresholds were calculated using δ_1. Therefore, using the thresholds: $\delta_1^* = \pi$ instead of $P_o = P_{th1}$ and $\phi^* + \delta_2^* = \pi$ instead of $P_o = P_{th2}$ were used to switch the modes. This successfully eliminated the need for additional sensing.

It is noted that, due to nonidealities of the circuit, the calculated values for the optimum parameter deviated from the actual optimum parameters. This was also noted in [24]. In order to accurately track the optimum points, the high frequency transformer current needs to be sensed, however similar argument makes this undesirable. The experimental result captured such nonidealities. Thus in most cases, small manual adjustments to the optimum parameters were made to nullify these effects. This effect is more profound in case of TPS-2, TPS-4 and TRM modulations where, without precise measurement of the transformer current ZCS is difficult to achieve. A simpler solution is to use TPS-6, TPS-1 instead, which allows ZVS and a wider deadtime ensures continued soft switching with varying operation range, at the cost of small reduction in overall efficiency.

In Fig. 4.12, a slow closed loop controller has been implemented for boost mode operation based on the control scheme shown in Fig. 4.11. Controller response has been chosen to be slow deliberately to demonstrate the transition of the proposed hybrid controller. As seen from the figure, when the converter was operated at 80W, optimum TPS-4 is applied. When a step load of additional 80W is added, the controller modulates the δ_1 and other parameters. When δ_1 reaches π, the modulation

transitioned to optimum modulation for TPS-3.

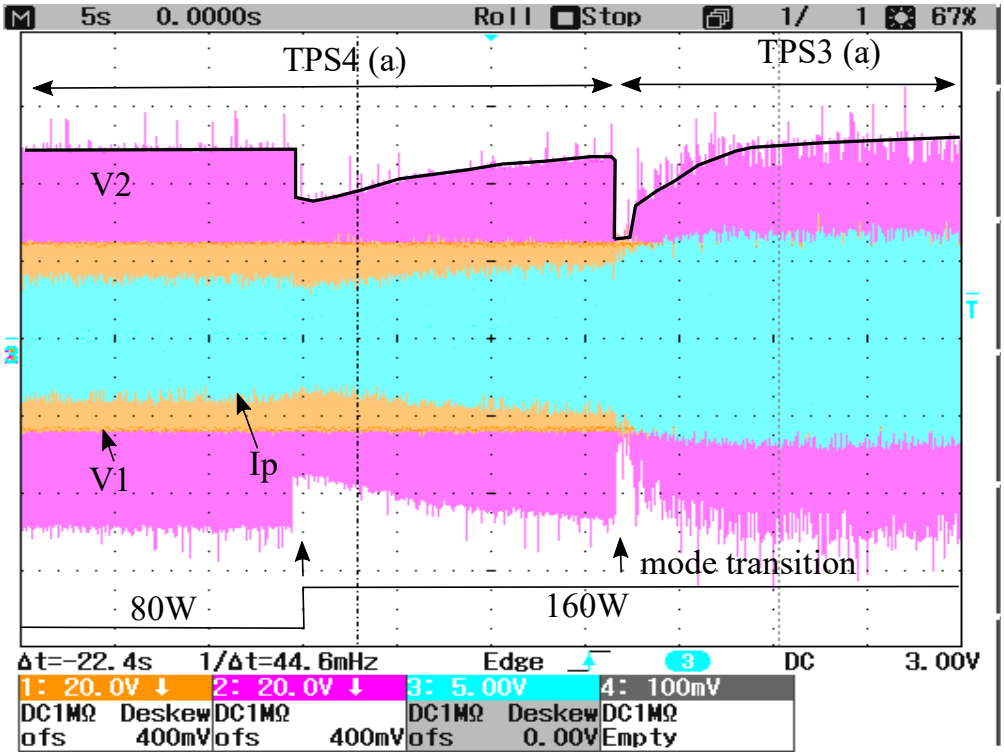


Figure 4.12: Response of hybrid modulation controller under step load for boost mode operation

In Fig. 4.13 and Fig. 4.14, the overall efficiency, rms current and peak current has been plotted against the power flow. It is seen that for boost mode, TPS-4 and TPS-3 are used as hybrid modulation. The optimum modulation of TPS-4 is TRM as discussed before. This was validated from the efficiency and rms current plots, as it is demonstrated that as the parameters move close to the optimum δ_1^*, δ_2^* and ϕ^*, the rms current and overall efficiency improves.

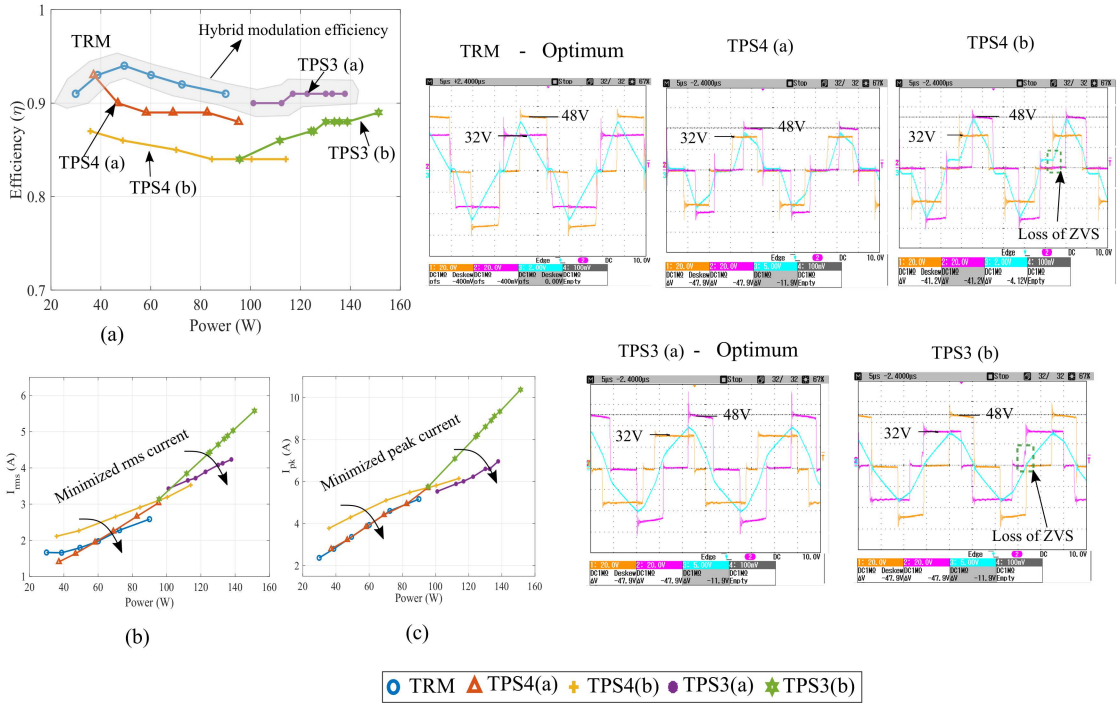


Figure 4.13: (a) Efficiency, (b) rms current and (c) peak current of the triple phase shift modes TPS-4 and TPS-3 at optimum and non optimum operating points for boost mode operation

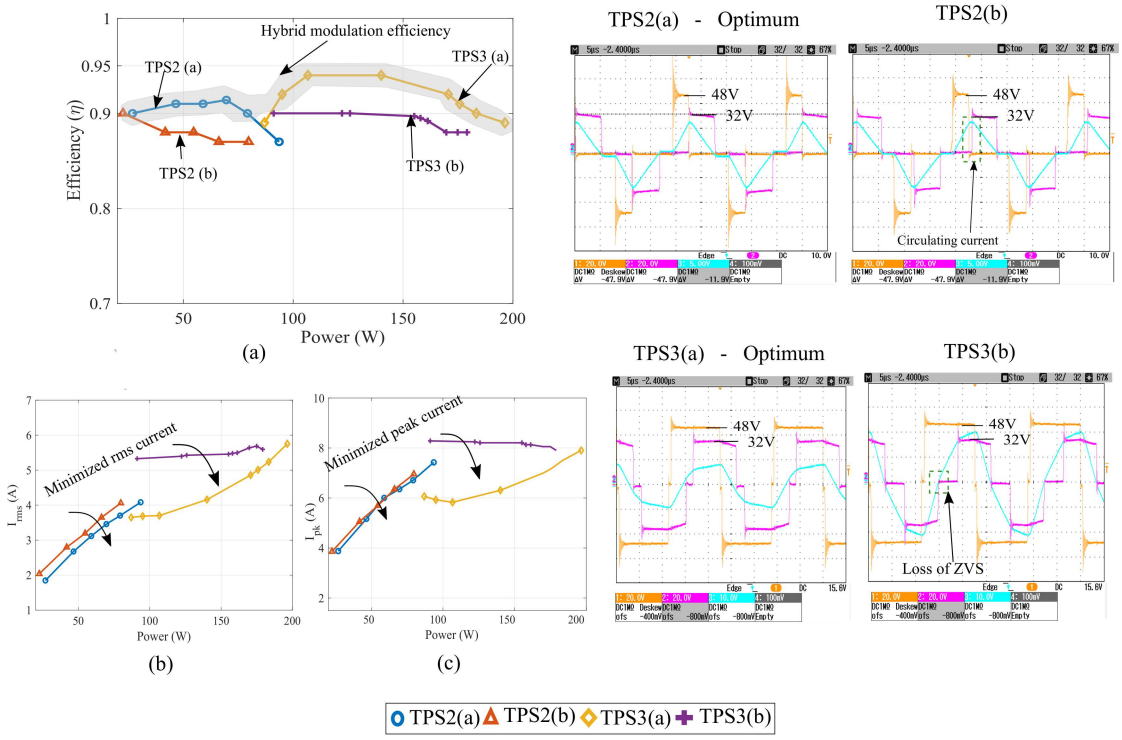


Figure 4.14: (a) Efficiency, (b) rms current and (c) peak current of the triple phase shift modes TPS-2 and TPS-3 at optimum and non optimum operating points for buck mode operation

A similar trend was noticed for TPS-3. The shaded region shown in the efficiency plot, represents the optimum hybird modulation efficiency. As seen in [18] and [24], SPS is generally much lower in efficiency compared to other DPS or TPS schemes, so the comparison of the proposed hybrid modulation with SPS is not repeated here. Instead, from Figs. 4.13 and 4.14 it is clear that the hybrid modulation improves efficiency over wide power flow range compared to each individual TPS modulation, and is much more efficient than SPS.

4.6 Summary

TPS modulation allows soft switching operation over the complete power flow range and is much more attractive than traditional SPS modulation schemes. However, without careful control, it can introduce reactive or circulating power, which reduces the overall efficiency. Prior work has addressed the optimization framework to minimize rms or peak current for TPS schemes using offline optimization based algorithm but no analytical framework was developed. An optimization framework for the family of TPS modulation of DAB was discussed in this work. A piecewise analytical model of the TPS schemes was introduced which minimized the component of the rms current that contributes to losses and doesnot yield to the output. In addition, soft switching conditions were integrated into the optimization framework. This made the optimization complete, achieving both conduction and switching loss reduction. Finally, a hybrid control scheme based on the optimization was developed, which successfully maintained high efficiency throughout the operating range.

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CHAPTER 5: BIDIRECTIONAL SINGLE STAGE MICROINVERTER BASED ON DUAL ACTIVE BRIDGE CONVERTER

With an increasing trend of adopting renewable energy sources such as solar, wind etc as a replacement of high carbon footprint and diminishing fossil fuel based energy sources, research on power conversion systems for the integration to power grid has reached its peak. Research on interfaces such as micro and string inverters have seen heavy application throughout the last few decades. However, with improved lifetime and reliability of commercially available PV systems, the research on power converters is generally driven to match those characteristics. The primary concern with existing micro inverter system is that they employs a DC link system to decouple of the DC and AC power [1], [2], [9]. The required capacitance for decoupling, depends on the DC bus voltage and the power transferred. Usually, for a 200W grid tied ($110\ or\ 120V_{rms}$) microinverter system, the typical value for decoupling capacitor is around $14mF$. Practical and cost effective candidates to supply this massive amount of capacitance are electrolytic capacitors. They are usually high in capacitance but come in smaller packages. However their lifetime is very low which directly impacts the overall lifetime of the microinverter.

It is also very important to reduce the number of energy conversion stages in DC-AC applications, Traditionally, a grid tied PV system uses a DC-DC stage and a DC-AC stage as shown in Fig. 5.1 (a).

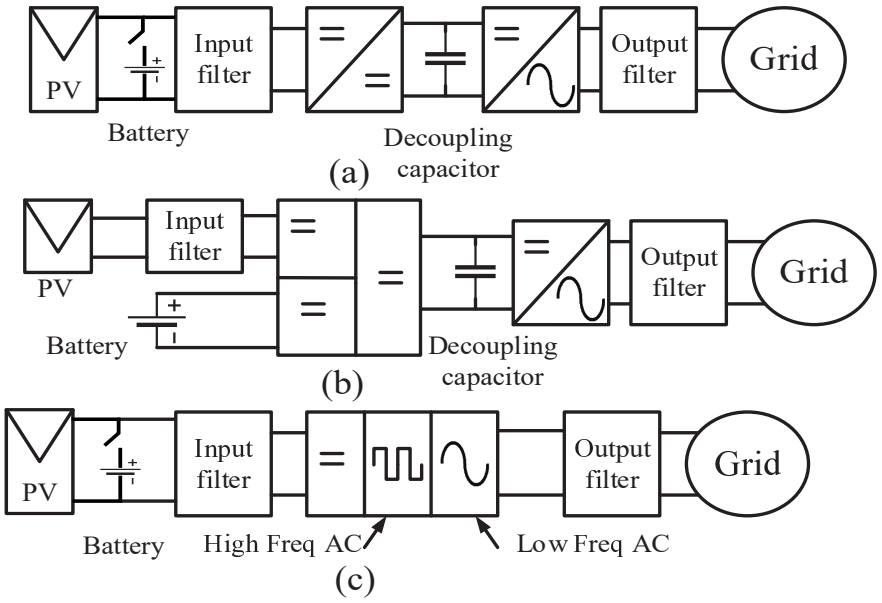

Figure 5.1: Architectures of popular PV-battery systems (a) two stage, two port, DC link system (b) two stage multiport system, DC link system (c) Single stage, two port, AC link system

The DC-DC stage is typically required for stepping up the PV voltage and maximum power point tracking etc. The DC-AC stage is the microinverter, responsible for generating grid compatible AC output. However, with multiple conversion stage, the efficiency is low. This is because while each stage individually is fairly efficient, efficiency of each stage is multiplied to obtain the overall efficiency.

In addition to improving the lifetime and reliability, recent improvement of energy storage technology has dramatically lowered the cost of battery storage systems such as lithium ion or nickel cadmium based options. Employing an energy storage device enhances the power quality of the renewable energy system greatly by improving its dispatchability, overall reliability and performance [3]. In a grid parallel PV system that employs battery energy storage, the traditional method of battery charging is directly from PV and discharging is into the DC bus of the inverter. However, with the evolving power quality regulations such as IEEE1547 and IEEE1547.a, California rule 21 etc, battery discharging and charging to and from grid is becoming an important feature

for smart inverters and PV systems. In terms of system flexibility and smart operation, improving dispatchability, reducing energy spillage and bidirectional charging/discharging are highly desired characteristics.

Many multiport converters [4] have been proposed which combines the renewable energy port with an energy storage port to create a single DC bus that drives an inverter to generate the AC output. For a grid tied solar system, this architecture (Fig. 5.1.(b)) is particularly useful and allows important grid interactive operations such PV firming, peak shaving etc. From the hardware design perspective, this multistage design still poses challenges as the reliability degrades and the overall architecture is not durable. And as discussed before, the DC link microinverter employs an electrolytic capacitor which is a single point of failure over the product life cycle.

Substantial work has been done to address this issue by either improving the control architecture for the microinverter [5] or by improving the topology to incorporate active decoupling techniques [6]-[9]. However, there are limitations to these approaches such as high control complexity and the addition of active switches which otherwise do not take part in power conversion. Therefore, single stage AC link inverters are a good alternative for renewable energy applications where the reliability and cost of the microinverter are highly important. A standard architecture for AC link microinverter is shown in Fig. 5.1(c). Many different AC link inverters have been proposed in recent times for PV applications [10] that have bidirectional power flow control [11]. Achieving soft switching for these reported topologies is challenging and requires resonant commutation. In addition, all active devices are not switched at zero current or voltage.

In this chapter, a new sinusoidal modulation for the bidirectional AC link micro inverter discussed in [17], [18] or [19] is proposed which is based on the concept of a dual active bridge converter (DAB). Since DAB are popular for low cost, simpler control implementation and easy to achieve soft switching [12], [13] the converter retains all the merits of DAB. The proposed modulation scheme ensures an AC link power conversion from DC to AC, while simultaneously eliminating the DC link and improving the reliability of the microinverter. The basic topology was first pro-

posed in the early nineties by [17], [18] where the author have used bidirectional switch using MOSFET or IGBT. The proposed topology in [17] uses back to back MOSFETs with DC blocking diodes in series in order to cancel the anti parallel diodes. It then adds an external diode in order to combine the two switches effectively into one bidirectional switch which helps in softswitching under any line/load condition. This arrangement adds upto three additional diodes for each bidirectional switch and overall additional device required can go upto 12. The work in [18] uses IGBTs and largely depends on additional snubber circuitry for loss less switching. The work in [19], uses similar 4-quadrant switches on a resonant version of the similar topology, however the modulation doesn't follow sine PWM and operates similar to a DAB under dual phase shift. Similar cycloconverter based topology appears in [20], but the architecture restricts the modulation to dual phase shift without a sine PWM. Similarly, in [21] an AC-DC converter was proposed based on DAB topology with a front end unfolding circuit. In this work, author used an optimization based approach which uses the AC current measurement to generate optimum modulation. A look up table is used to store the offline optimization data and called based on the AC current sensing to implement the modulation. This approach requires large processor memory as well as processing power to carryout an optimization like this, and generally too expensive and complex to implement. Most of the previous work uses only dual phase shift control thus the soft switching region is limited, and they are based on generation of low frequency square wave AC output and thus depends on heavy filter design to attenuate high frequency harmonics. Proposed modulation is fundamentally different because, the low frequency AC synthesis is sine PWM modulation, similar to most of todays microinverters. Therefore, only a small output filter is required. Additionally, a triple phase shift modulation is used for high frequency AC link, which allows higher soft switching range. Thus, the proposed microinverter provides a new topology in terms of active elements used, along with new modulation for high frequency AC link DC-AC power conversion. Finally, the implementation is completely analytical only and hence can be implemented very simply by low power digital signal processors and does not require a closed loop structure to implement. Overall implementation is much simpler than previous works.

The DAB based DC-AC microinverter that is discussed later in this chapter is based on a composite modulation. The composite is formed from the six unique modulation schemes for the TPS family shown in Fig. 5.2, repeated here from the previous chapter. The operating region defined as $0 \leq \delta_1 \leq \pi$, $0 \leq \delta_2 \leq \pi$ and $0 \leq \phi \leq \pi$.

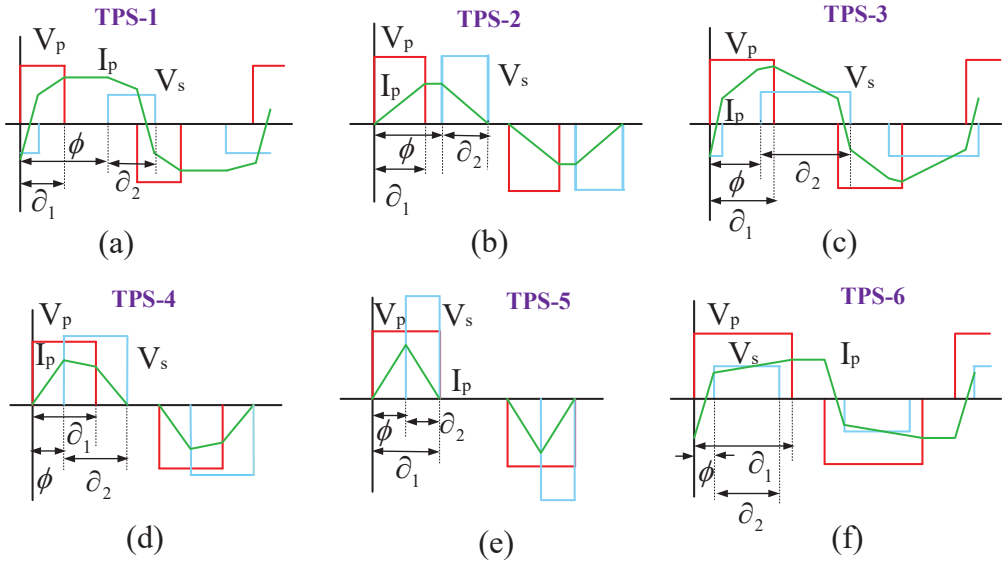

Figure 5.2: Different modulation schemes of the TPS family

In Fig.5.2 (a) - (f), the modulation schemes can be achieved by varying the phase shift ϕ between the input and output bridges and the conduction angles of the primary bridge, δ_1 and secondary bridge, δ_2. Here, the transformer primary voltage is denoted as V_P, secondary voltage as V_S and the primary current as I_P.

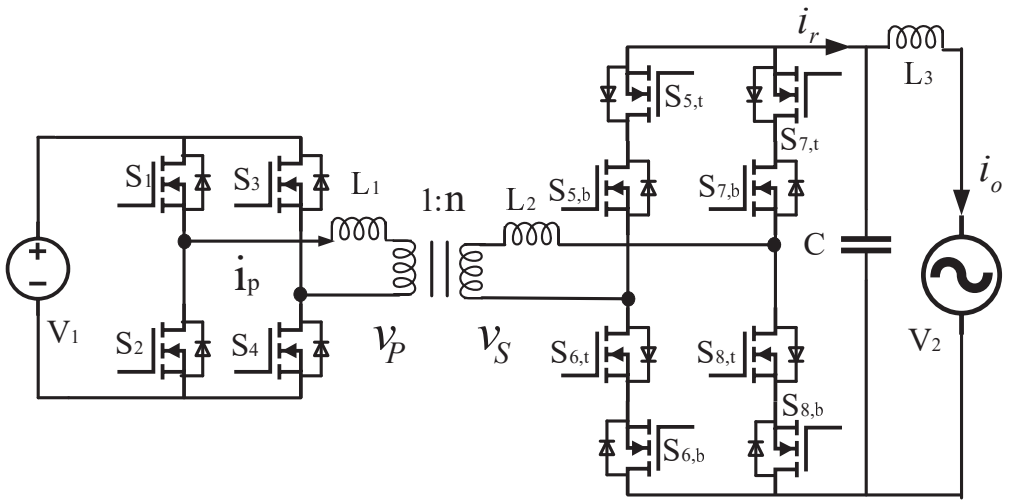

Figure 5.3: High frequency AC-link DC-AC converter based on DAB

The traditional AC link inverter topology eliminates the need for a DC link with bulky electrolytic capacitor for decoupling purposes. This allows a smaller AC link to be used for DC to AC decoupling. However, is it noted that the decoupling is still needed at the DC input side. Since the DC input voltage is often lower than the DC link voltage, typically the capacitor size and cost is less. As the bidirectional active switches are used, the power flow can be bidirectional. Carefully designed control is necessary to achieve seamless bidirectional power flow. The PWM for DC-AC and AC-DC conversion is likely to be very different. Therefore certain applications, like a battery discharging and charging to and from the grid, will require frequent switching between DC-AC and AC-DC conversion mode. This may require an advanced control scheme. This arrangement makes the operation expensive, unreliable and complex.

DAB allows spontaneous bidirectional power flow with a very simple control scheme that varies the phase shift ϕ. It also allows soft switching with relative ease as compared to other PWM methods. It doesn't require additional components to achieve soft switching like resonant converters. Thus, a high frequency AC-link micro inverter based on a DAB converter has been proposed here. It

overcomes the shortcomings of regular AC link inverters that struggle to achieve soft switching and seamless bidirectional power flow control with complex control schemes. The topology of the proposed converter is derived from a DAB converter. The only modification to the original DAB shown in Fig.4.2 is that, on the secondary, back to back switches are implemented to avoid shorting the secondary AC port through the anti parallel diodes of the active switches. The secondary bridge is similar to a cycloconverter structure with the arrangement of four quadrant switches. The proposed high frequency AC-link DC-AC converter based on DAB is shown in Fig.5.3.

5.1.1 Synthesis of Low Frequency AC

The proposed converter utilizes a high frequency AC (HFAC) link created by the primary or secondary bridges for DC to AC conversion. A simple modulation scheme using only SPS as the fundamental modulation to synthesize a low frequency AC square wave as shown in Fig.5.4. Application of the TPS that generates a smooth sine wave is discussed later.

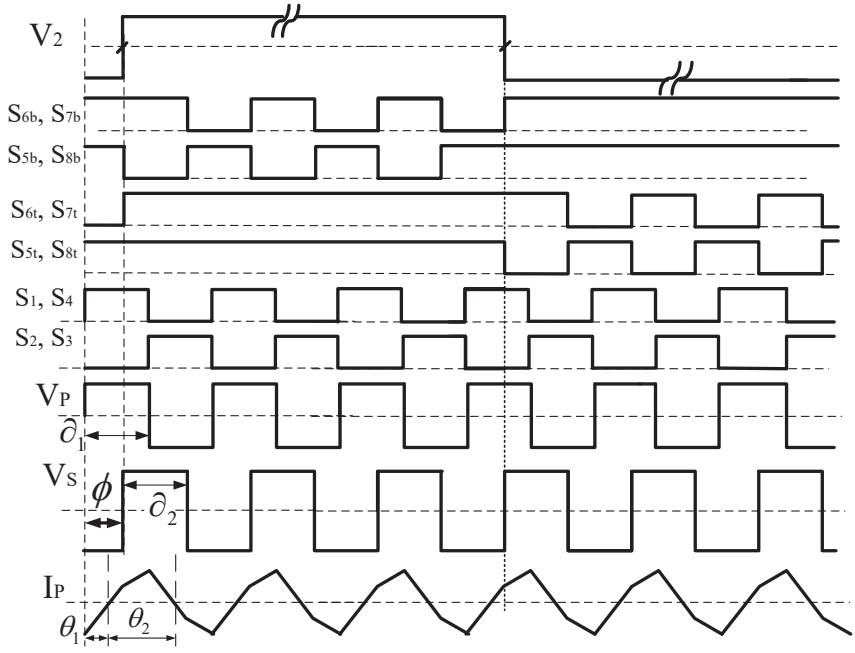

Figure 5.4: Key wave forms of the AC link topology with fundamental SPS modulation

In Fig.5.4, both positive and negative DC bus voltage can be converted into a high frequency square wave AC by switching the bridge using PWM pulses.

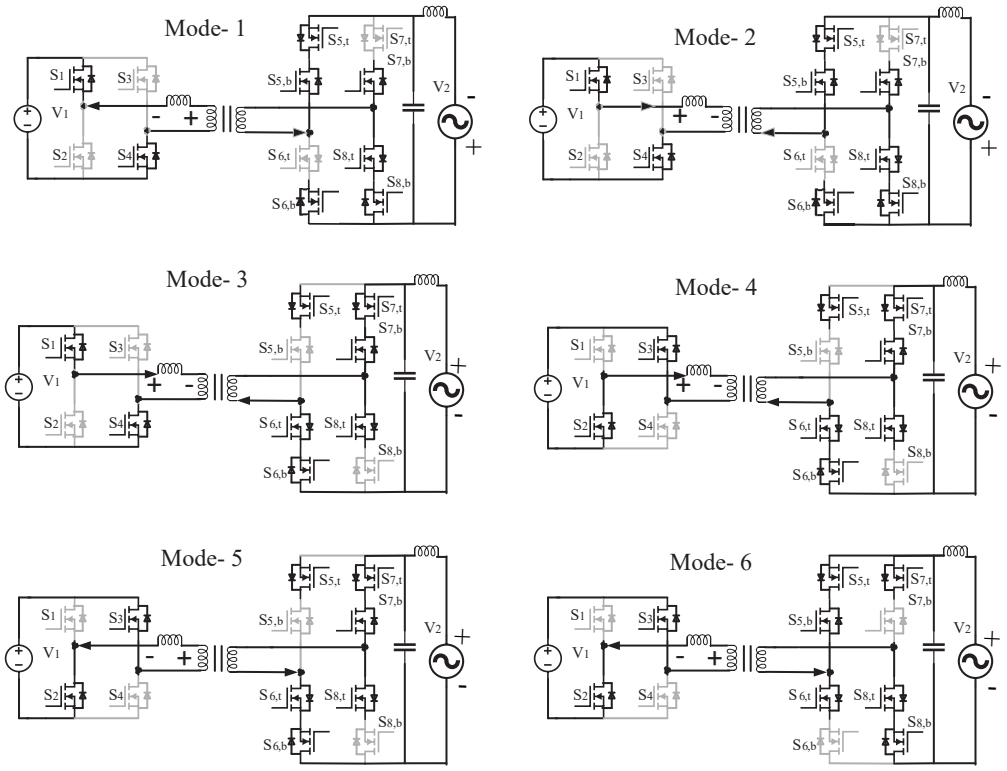

Figure 5.5: Mode analysis for the proposed converter during positive half cycle of the output AC waveform

However, for a negative DC bus, a 180^o phase shift is introduced at HFACL square wave. This can be mitigated by introducing a 180^o phase shift on the gate pulses. The same bridge can produce a continuous HFAC output from a bipolar input by properly controlling the PWM. Based on this principle, the proposed HFAC link topology can generate an AC sine wave from a DC input, where the transformer leakage inductance acts as the AC link. Since, the rms current is low for the HFAC link, the inductor size remains small.

In Fig.5.5, a mode analysis of the proposed topology is shown. In the first mode $0 \leq \theta \leq \theta_1$, the transformer current increases with slope $\frac{V_P+V_S}{\omega L}$ starting from a negative current. The transformer

primary current transitions to a positive current starting from mode-2, $\theta_1 \leq \theta \leq \phi$, and continues to increase with the same slope. In the third mode, $\phi \leq \theta \leq \delta_1$, the slope becomes $\frac{V_P - V_S}{\omega L}$ as the secondary bridge voltage reverses its polarity. Similarly, for mode-4 ($\delta_1 \leq \theta \leq \theta_1 + \theta_2$) and 5 ($\theta_1 + \theta_2 \leq \theta \leq \phi + \delta_2$), the slope becomes $\frac{-V_P - V_S}{\omega L}$. At the end of mode-4, the transformer primary current reverses again from positive to negative. In mode-6, $\phi + \delta_2 \leq \theta \leq \pi$, the slope becomes $\frac{-V_P + V_S}{\omega L}$. During the negative half cycle of the secondary AC voltage source, identical modes appear in same sequence.

The transformer primary current expression during the modes for SPS modulation is summarized as:

Mode-1 & 2:

$$i(\theta) = \frac{v_P + v_S}{\omega L}(\theta) + i(0) \tag{5.1}$$

Mode-3:

$$i(\theta) = \frac{v_P - v_S}{\omega L}(\theta - \phi) + i(\phi) \tag{5.2}$$

Mode-4 & 5:

$$i(\theta) = \frac{-v_P - v_S}{\omega L}(\theta - \delta_1) + i(\delta_1) \tag{5.3}$$

Mode-6:

$$i(\theta) = \frac{-v_P + v_S}{\omega L}(\theta - \phi - \delta_2) + i(\phi + \delta_2) \tag{5.4}$$

Also from symmetry:

$$i(\pi) = -i(0) \tag{5.5}$$

Solving the above equations, yields the power flow expression in each switching cycle that can be used to calculate the overall rms power. The soft switching conditions can also be obtained from

above expression by solving the inequalities:

$$\begin{aligned} i(0) &\leq 0 \\ i(\phi) &\geq 0 \\ i(\delta_1) &\geq 0 \\ i(\phi + \delta_2) &\leq 0 \end{aligned} \tag{5.6}$$

Details of soft switching condition for SPS can be found in [12].

5.1.2 Sine PWM and Implementation of Phase Shift

Although generation of HFAC from a low frequency square wave can be achieved using proper control of the PWM pulses, generation of HFAC "quasi" square wave or HFAC "square wave with dead time", is more challenging. Naturally, it requires TPS modulation instead of SPS modulation. The dead time can be implemented by simultaneously turning on the top or bottom switches of the bridge.

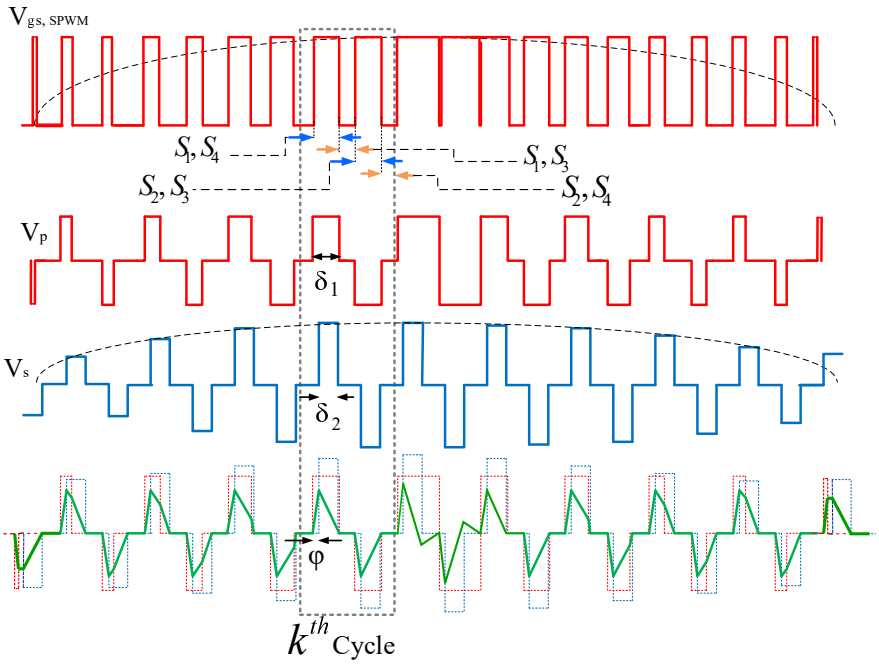

Figure 5.6: Proposed modulation scheme for the AC link topology

In order to maintain ZVS for different modes, the sequence in which the top or bottom switches overlap and the direction of transformer current are very important. Fig.5.6 shows the output voltages of the primary and secondary bridge along with the primary current under the proposed modulation scheme. Here the primary bridge is driven by sine PWM (SPWM) and secondary bridge is driven by a constant phase shift - constant conduction angle (or constant dead time). Since the primary bridge is driven by SPWM, the dead time or conduction angle of the bridge varies sinusoidally. Therefore, over the range of one half cycle of a 60Hz sine wave, the converter goes through several different modes of TPS modulation that are termed as "fundamental modulation" through out this chapter. The negative half cycle is symmetric to positive half cycle and similar fundamental TPS modes will appear in identical order. In Fig.5.6, the gate-source pulses for the input bridge are shown as $V_{gs,SPWM}$. A modulating signal is compared with a carrier wave of saw tooth shape to produce a SPWM waveform. For the proposed modulation, the carrier frequency is same as the switching frequency of the primary bridge. The sequence of which the primary

switch pairs turn on in order to correctly synthesize symmetric quasi square wave output at the transformer primary is: $\underline{S_1, S_4}$, $\underline{S_1, S_3}$, $\underline{S_2, S_3}$ and $\underline{S_2, S_4}$ respectively. To explain this further, for the k^{th} switching cycle which comprises of two switching cycle of $V_{GS,SPWM}$, during the first span when $V_{gs,SPWM}$ is on, S_1, S_4 turns on, and when $V_{gs,SPWM}$ is off for the first cycle, S_1, S_3 turns on. During the next switching cycle within k^{th} cycle, the pairs S_2, S_3 and S_2, S_4 turns on similarly as shown in Fig. 5.6. The output current is filtered using the first order low pass filter to produce sine wave. On the output bridges, $S_{5,t}$ to $S_{8,t}$ are kept on during the positive half cycle of the 60Hz AC while the other switches are modulated. $S_{5,b}$ to $S_{8,b}$ are kept on during the negative half cycle while the other switches are modulated similarly. This provides unfolding for the low frequency AC.

5.2 Performance Characterization

The power flow expression for the proposed modulation can be derived from the modulation scheme employed. The modulation scheme shown in Fig.5.6 is achieved by keeping the phase shift between the primary and secondary bridges, constant. Also the dead time or conduction angle of the secondary bridge was kept constant while applying a SPWM pattern on the primary bridge. This allows a simpler implementation of the modulation scheme. However, over the span of a half cycle, multiple different fundamental TPS schemes are employed as shown in Fig.5.2. Hence, calculating the power expression becomes difficult.

5.2.1 RMS current and power

In Fig.5.6, a constant phase shift modulation (CPSM) has been proposed, where the shaded part of the transformer current is converted to the output current. For the given example of Fig.5.6 with CPSM being the chosen method of modulation, one 60Hz half cycle consists of TPS-2, TPS-4, TPS-5 and TPS-6 fundamental modulations. For simplicity, following assumptions are made: the

proposed composite modulation scheme is restricted to TPS-2, 4, 5 and 6 by constraining the phase shift angle to be $\phi \leq \delta_1$. Ignoring the effects of parasitic elements, the average output power over one half of the 60Hz cycle can be written as:

$$p_{out}(t) = \frac{\sum_{i2} p^{i2}_{TPS-2}(t) + \sum_{i4} p^{i4}_{TPS-4}(t) + \sum_{i5} p^{i5}_{TPS-5}(t) + \sum_{i6} p^{i6}_{TPS-6}(t)}{\pi} \quad (5.7)$$

where, p_{TPS-2}, p_{TPS-4} , p_{TPS-5} and p_{TPS-6} are the average power flow over each high frequency switching cycle, for TPS-2, 4, 5 and 6 respectively. Each of these high frequency average power is expressed by following:

$$p^{i2}_{TPS-2} = \frac{V_1 V_2 sin(\omega_L t)\delta_1^{i2}(t)\delta_2}{2\omega L} \quad (5.8)$$

$$p^{i4}_{TPS-4} = \frac{V_1 V_2 sin(\omega_L t)\{-\delta_1^{i4\,2}(t) + 2\delta_1^{i4}(t)\phi + \delta_2\delta_1^{i4}(t) - \phi^2\}}{2\omega L} \quad (5.9)$$

$$p^{i5}_{TPS-5} = \frac{V_1 V_2 sin(\omega_L t)\ \phi\{\delta_1^{i5}(t) - \phi\}}{2\omega L} \quad (5.10)$$

$$p^{i6}_{TPS-6} = \frac{V_1 V_2 sin(\omega_L t)\ \delta_2\{\delta_2 - \delta_1^{i6}(t) + 2\phi\}}{2\omega L} \quad (5.11)$$

where the indices $i2$, $i4$, $i5$ and $i6$ are the number of high frequency switching cycle appears in each to the TPS span over the 60Hz half cycle. This span of fundamental modes are called "angle span". V_2 is the peak output voltage of the output 60Hz sine wave and $\omega_L = 2\pi f_L$, f_L = 60Hz.

Note that the instantaneous time varying power flow expression contains the $sin^2(\omega_L t)$ term, when the sinusoidal variation of δ_1 is taken into account. However, the overall power flow expression contains additional nonlinear term such as $sin^3(\omega_L t)$ from equations (9) - (11), which introduces additional harmonics at the output. Close investigation of the power flow expression reveals that with proper selection of ϕ, δ_2 and modulation index (m_p) yields low harmonic distortion output.

Detailed harmonic analysis has been presented in section 5.2.3, for improved design.

A more simplistic approach for obtaining the average power is defining the angle spans of each fundamental modes and average it over the 60Hz span. Therefore, $\sum_{ih} p_{TPS-h}^{ih}$ can be equivalently represented by $\Delta\tau_h \; p_{TPS-h}$, where $h = 1, 2, 3, 4, 5, 6$ and τ_h represent the angle span of each TPS modes.

The angle span of TPS-2, 4, 5 and 6 over one half of a 60Hz cycle are denoted as: $\Delta\tau_2, \Delta\tau_4, \Delta\tau_5$, and τ_6. The angle span of a 60Hz half cycle is $\Delta\tau$. Typically $\Delta\tau = \pi$. Referring back to Fig.5.2, the angle spans can be represented by the following equations in per units (P.U):

$$\begin{aligned}
\Delta\tau_1(P.U) &= \frac{1}{\pi} sin^{-1}\frac{\phi}{\pi},\ \Delta\tau_2(P.U) = \frac{1}{\pi} sin^{-1}\frac{\phi}{\pi}, \\
\Delta\tau_3(P.U) &= \frac{1}{\pi}(\pi - sin^{-1}\frac{\phi}{\pi}) \\
\Delta\tau_4(P.U) &= \frac{1}{\pi}(sin^{-1}\frac{\phi+\delta_2}{\pi} - sin^{-1}\frac{\phi}{\pi}), \\
\Delta\tau_6(P.U) &= \frac{1}{\pi}(\pi - sin^{-1}\frac{\phi+\delta_2}{\pi})
\end{aligned} \tag{5.12}$$

. The angle spans are illustrated in the Fig. 5.7 assuming a modulation index for the SPWM being 1 for CPSM-1, thus $\delta_1 = \pi$ at the peak of the modulating wave. The secondary bridge conduction angle is represented here as δ_2^* or δ_2^{**}, where δ_2^* is the conduction angle which yields $\phi + \delta_2^* \leq \pi$ and δ_2^{**} yields $\phi + \delta_2^{**} > \pi$. Note that TPS-5 is a generalized modulation of TPS-4 and thus the angle span and power flow expression can be derived from TPS-4. Further in the analysis, it is ignored and TPS-4 is used instead.

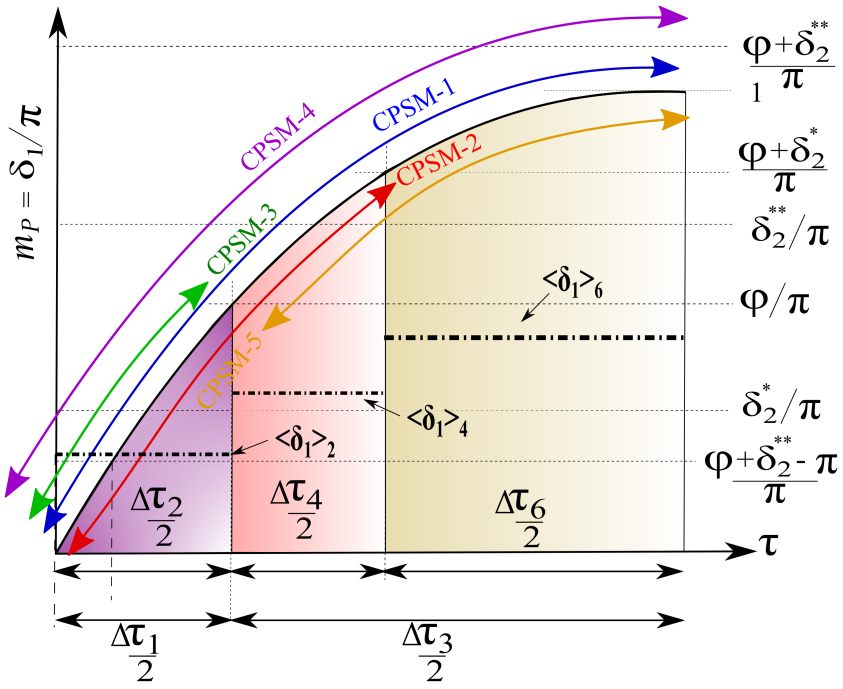

Figure 5.7: Illustration of angle span for different TPS modes under SPWM modulation

Thus, low frequency average output power over one half cycle is give as:

$$P_{avg} = \frac{2P_m}{\pi} \tag{5.13}$$

Where:

$$P_m = \Delta\tau_2 \; p_{TPS-2}|_{sin(\omega_L t)=1}^{\delta_1=\langle\delta_1\rangle_2} + \Delta\tau_4 \; p_{TPS-4}|_{sin(\omega_L t)=1}^{\delta_1=\langle\delta_1\rangle_4}$$
$$+ \Delta\tau_6 \; p_{TPS-6}|_{sin(\omega_L t)=1}^{\delta_1=\langle\delta_1\rangle_6}$$

Where $\langle\delta_1\rangle_h$ denotes the average value of δ_1 over its respective angle span of $TPS-h$. As an example, $\langle\delta_1\rangle_4$ can be calculated as: $= \frac{1}{\delta_2}\int_{\phi}^{\phi+\delta_2} m_p sin\tau d\tau$.

Through out this chapter, the analysis has been restricted to the given example where the fundamental TPS modes are TPS-2, 4 and 6, however, it can easily be extended to other combinations of fundamental modulation.

5.2.2 Soft Switching

Achieving loss less or soft switching is an important aspect for low power converters. As the composite modulation scheme is achieved by combining the fundamental modulations shown in Fig.5.2, the soft switching condition is also dependent on the fundamental modulations. The soft switching conditions for TPS-2 to TPS-6 can be obtained by applying appropriate inequalities at different instances of the transformer current; ωt = 0, ϕ, δ_1 and $\phi + \delta_2$. For all switches in both primary and secondary bridge, the soft switching condition is: $i(0) \leq 0$, $i(\phi) \geq 0$, $i(\delta_1) \geq 0$ and $i(\phi + \delta_2) \leq 0$. The parameter ranges to achieve soft switching are given in Table-4.1.For the modulation scheme shown in Fig.5.6, the combined soft switching condition for CPSM is:

$$\delta_2 = \delta_1 \frac{V_1}{V_2}, \quad \phi \leq \delta_1 - \delta_2 \tag{5.14}$$

From (5.14) it is obvious that to guarantee soft switching during all fundamental modulation, the phase shift ϕ must be either proportional to the primary bridge conduction angle, δ_1 and the voltage conversion mode must be boost ($V_1 \leq V_2$). Since δ_1 varies as it follows a SPWM pattern, ϕ can be modulated proportionally. This gives rise to a different modulation scheme called variable phase shift modulation (VPSM).

Varying ϕ proportional or at a fraction of δ_1, yields a constant fundamental modulation through out the 60Hz cycle.

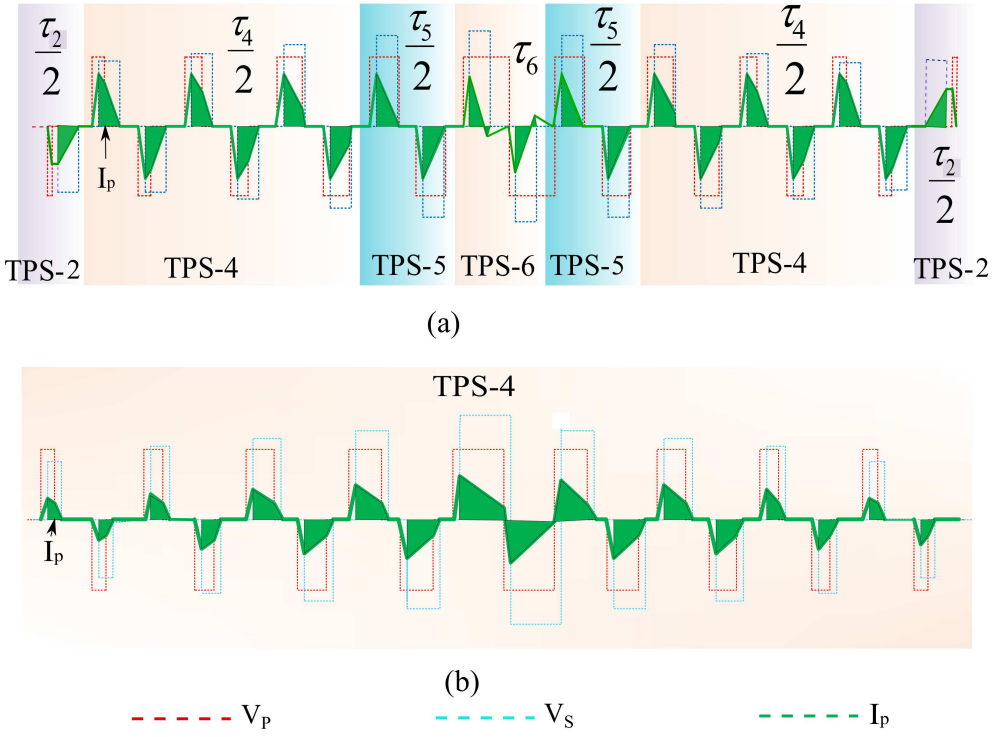

Figure 5.8: Different modulation schemes proposed for the HFACL inverter with - (a) Constant phase shift modulation, (b) Variable phase shift modulation

In Fig.5.8, both CPSM and the VPSM is demonstrated. As seen from Fig.5.8(a), the CPSM consists of TPS-2, 4, 5 and 6, where as the VPSM consists of only the TPS-4 fundamental modulation. Therefore the output power for the VPSM shown in Fig. 5.8(b) is:

$$P_{out} = p_{TPS-4} \tag{5.15}$$

The soft switching condition for VPSM is:

$$\delta_2 = \delta_1 \frac{V_1}{V_2}, \quad \phi \geq 0$$

Previously discussed TPS-5 is an attractive candidate for VPSM for it low rms current and soft switching abilities [16], [22]. Note that, since δ_1 and ϕ are both modulating sinusoidally, δ_2 is not

necessarily a constant in VPSM and may vary according to the mode boundary and soft switching condition of the specific operating TPS mode.

5.2.3 Harmonic analysis

In addition to the rms power, the harmonic distortion of the output current waveform is also affected by the fundamental modulation scheme and its composition.

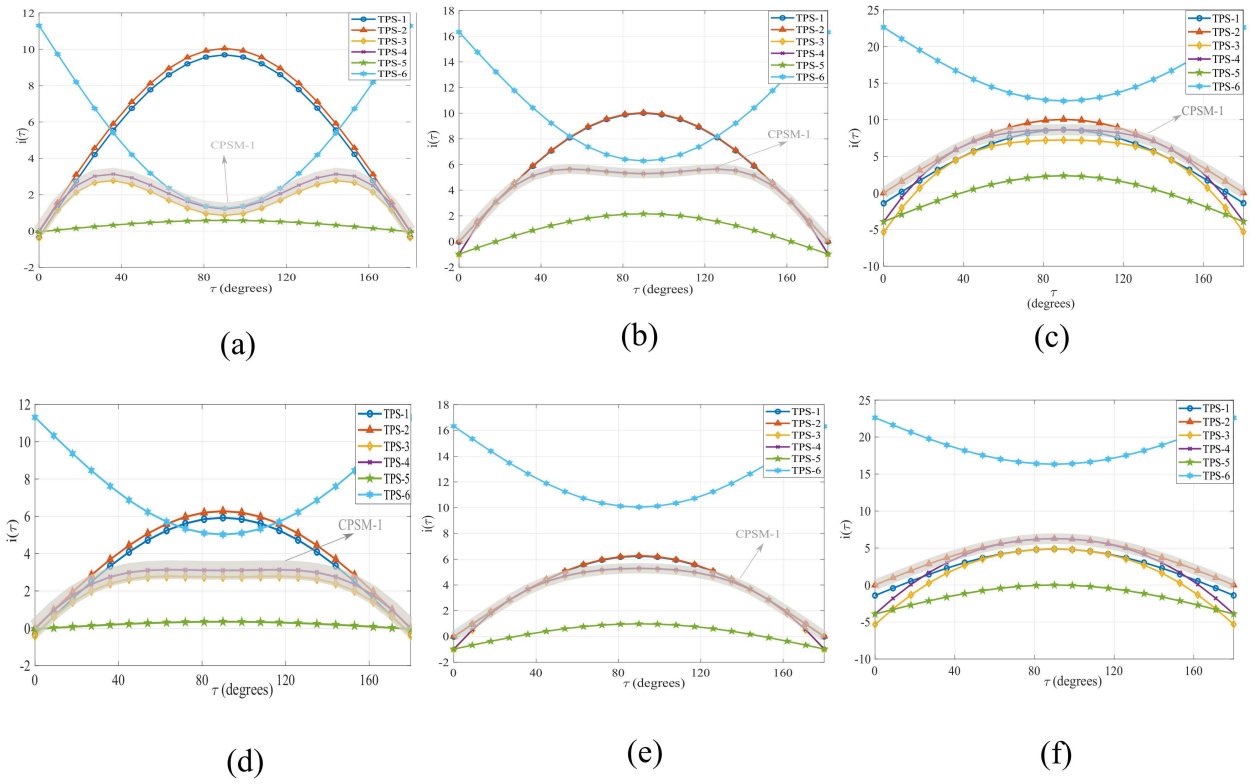

Figure 5.9: AC output current waveform over one half cycle for different fundamental modulations, TPS-1 to 6. Current waveform for (a) $m_p = 0.8, \delta_2 = 0.8\pi, \phi = 0.05\pi$, (b) $m_p = 0.8, \delta_2 = 0.8\pi, \phi = 0.25\pi$, (c) $m_p = 0.8, \delta_2 = 0.8\pi, \phi = 0.5\pi$, (d) $m_p = 0.5, \delta_2 = 0.8\pi, \phi = 0.05\pi$, (e) $m_p = 0.5, \delta_2 = 0.8\pi, \phi = 0.25\pi$, (f) $m_p = 0.5, \delta_2 = 0.8\pi, \phi = 0.5\pi$

In Fig. 5.9, the plot of the instantaneous output current over one half of a 60Hz cycle is shown with

different combination of ϕ and m_p. The secondary bridge conduction angle δ_2 is kept constant at 0.8π since lower harmonic distortion is observed when δ_2 is close to π. As seen from Fig. 5.9, current waveforms for all TPS modes are almost perfectly sinusoidal when m_p is lower and ϕ is close to $\frac{\pi}{4}$. Generally, TPS-6 is always 180^o out of phase. It also has a DC offset. TPS-2 is perfectly sinusoidal, regardless of ϕ or m_p value. In Fig. 5.9 (a) & (b) , TPS-1, 2 & 5 exhibits low harmonics and a dc offset. However TPS-3 & 4 are distorted and a significant third harmonic is present. In Fig. 5.9(c) & (f), TPS-1 to 5, all exhibits low harmonics. However, except TPS-2, all of the other modes have negative dc offset present in the current waveform. Fig. 5.9(d) is similar to (b) where higher harmonics are present for TPS-3 & 4. Only in case of Fig. 5.9(e), TPS-1 to 5, do all modes exhibit low harmonics and negligible dc offset. Thus, it can be concluded that regions around $\phi \approx 0.25\pi$ and $m_p \approx 0.5$ provides the least harmonic distortion. In the event when a wide range of ϕ is required, TPS-1, 2 or 3 is generally the best choice. Similar trend is reflected when the composite CPSM-1 is also plotted (transparent thick gray line) for the above conditions. Lowest harmonic distortion is observed in Fig. 5.9 (e) and (f).

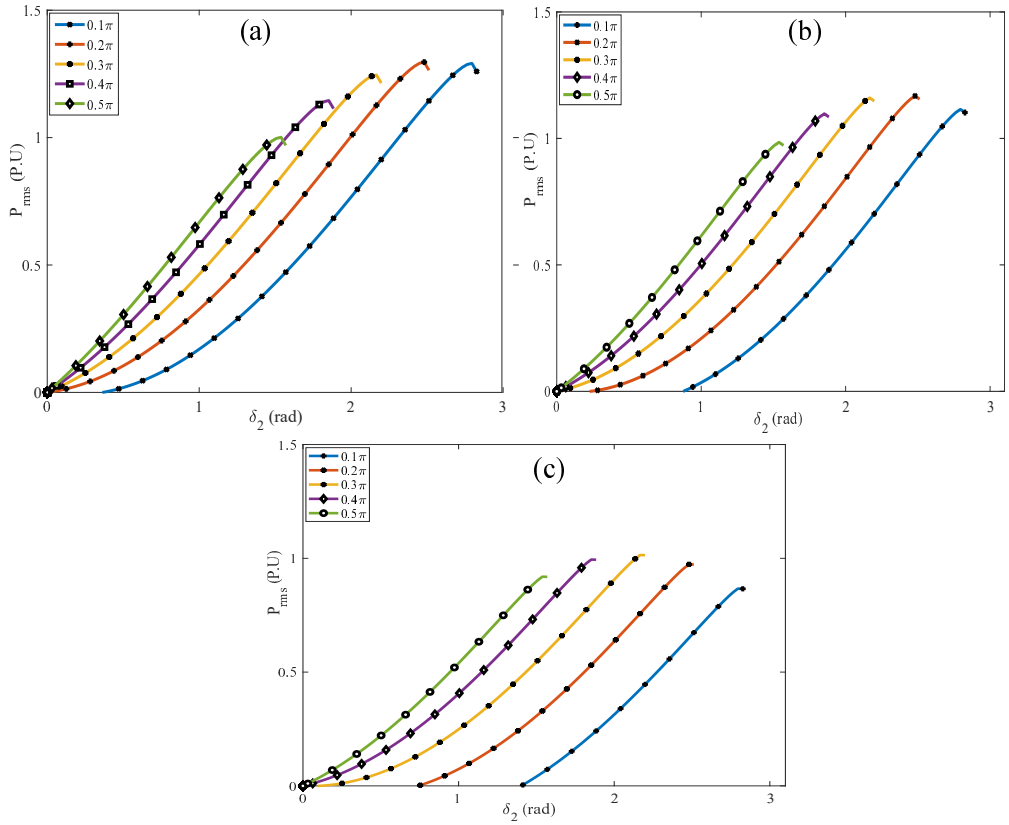

Figure 5.10: rms power plot vs δ_2 with base power calculated from $m_p = 0.5$, (a) for $\phi = 0.1\pi$ - 0.5π and $m_p = 0.5$, (b) for $\phi = 0.1\pi$ - 0.5π and $m_p = 0.75$, and (c) for $\phi = 0.1$ - 0.5π and $m_p = 1$

In Fig. 5.10, the overall rms power is plotted against δ_2 for different ϕ and m_p for the given example in (8). For any other composite modulation scheme, similar plot may be obtained easily, but not shown here for brevity. As seen from figure (a), the power increases gradually with increment in δ_2 and reaches peak rms power before decreasing again. It is observed that with an increase in ϕ from 0 to 0.5π for a given δ_2, the rms power increases. However, the total power flow range offered by $\phi = 0.1\pi$ is much higher compared to $\phi = 0.5\pi$. This is intuitive as with increase ϕ, the SPWM sweep is restricted and hence results in a lower power flow range. Overall peak rms power is higher with lower ϕ when the modulation index is lower, but increases with higher modulation index. Therefore, the power is dependent on both the phase shift as well as the modulation index.

5.2.4 *Different composite modulation and their comparison*

From (5.14) it is clear that since δ_1 and V_2 both vary in SPWM fashion assuming that they are synchronized in time. Thus, to maintain CPSM and soft switching at the same time, δ_2 can be kept constant. Appropriate value of δ_2 can be based on the value of modulation index, input and output voltage etc. When soft switching can be partially sacrificed, an wide range of possible value of ϕ and δ_2 can be used. A multitude of such composite modulation can be used with each having different advantage and disadvantages. The effect of the loss of soft switching can be kept at a minimum by strategically choosing ϕ and δ_2. This is also illustrated in Fig. 5.7. The CPSM-1 to CPSM-4 demonstrate different composite modulation, which is obtained with different modulation index and choice of ϕ and δ_2. CPSM-2 is achieved when $m_p = \frac{\phi+\delta_2}{\pi}$. CPSM-4[1] is specifically selected when $\phi + \delta_2 \geq \pi$. CPSM-5 is another distinct composite modulation which is obtained when the SPWM is varied instead of "0 to $m_p\pi$" to "ϕ to $m_p\pi$". In case when ϕ chosen to be very small, CPSM-5 becomes a feasible candidate. Since TPS-6 requires high boost mode for soft switching, CPSM-5 is only attractive for those applications.

In Table-5.1, a detailed description of the possible CPSM and VPSM scheme is outlined. Along with this, the topology and modulation presented in [17], [18] and [19] is compared in terms of number of active devices used and filtering requirement with assumptions on the total harmonic distortion (THD) based on the information presented in the open literature . The two references are chosen since the power level and efficiencies are comparable with the microinverter under discussion. The harmonic distortion values are obtained from simulation results in PSIM. As seen from the table, the SPWM based modulation achieves significantly better THD than the predicted THD of the uniform PWM modulations, and thus require much smaller filtering. Overall efficiency also improves because of low harmonic losses, as discussed later.

[1]It is seen from Fig. 5.7 that for CPSM-4, there exists another fundamental modulation when $\delta_1 \leq \phi + \delta_2 - \pi$, however, with the limited scope of this work, this mode is not considered a practical solution due to its low output power

Table 5.1: Comparison of output filtering for different composite modulations and past works

Items	Fundamental Modulations	Active/Passive devices	Filter size	THD
CPSM-1	TPS-2, TPS-4, TPS-6	12/3	L = 100μH, C = 5 μF L = 100μH, C = 1 mF	47.6 % 5 %
CPSM-2	TPS-2, TPS-4	12/3	L = 100μH, C = 5 μF	5%
CPSM-3	TPS-2	12/3	L = 100μH, C = 5 μF	5 %
CPSM-4	TPS-1, TPS-3	12/3	L = 100 μH, C = 5 μF L = 100 μH, C = 500 μF	36% 5%
CPSM-5	TPS-4, TPS-6	12/3	L = 100 μH, C = 1 mF	25 %
VPSM	TPS - 1 / 2 / 3 / 4 / 5 / 6	12/3	L = 100μH, C = 5 μF	5 %
Ref. [17]	DPS	24/3	L = 100 μH, C = 5 μF L = 1 mH, C = 5 mF	74.6 % 5 %
Ref. [19]	DPS	12/5	L = 100 μH, C = 5 μF L = 1 mH, C = 5 mF	74.6 % 5 %

5.3 Simulation and Experimental Results

A 300W converter was simulated and a prototype was build to verify the concept both in simulation and on the hardware. For both cases, the circuit parameters are, V_p = 48V, $V_{s,rms}$ = 120V, transformer turns ratio = 1:5, with leakage inductance of 265 μH placed on the secondary, filter inductance and capacitance of 300 μH and $90nF$ respectively. The power FETs are switched at 50kHz. An input filter was used for attenuating the low frequency ripple current caused by the AC load. A filter inductor of 1mH was used with a capacitor of 15mF. The winding resistance of the non-ideal inductor was assumed to be $\approx 0.1\Omega$.

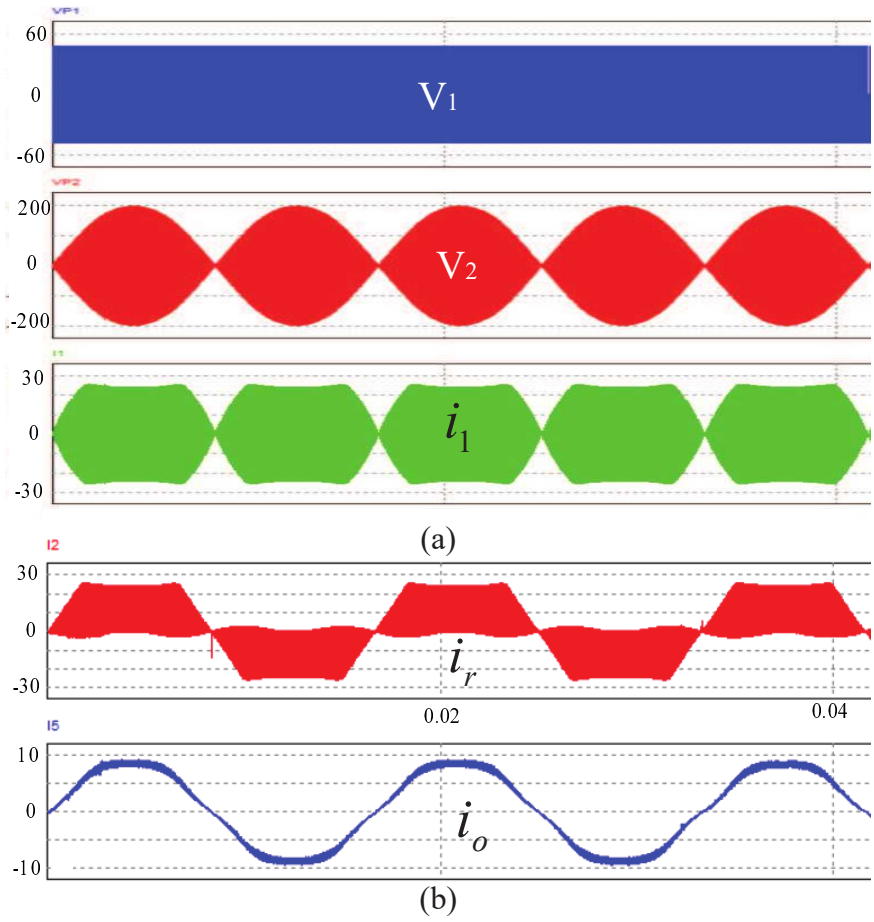

Figure 5.11: Simulation results of the HFACL converter, (a) Primary voltage, current and secondary voltage (one 60Hz cycle), (b) Output unfiltered current and output filtered current

The choice of input voltage is driven by the commercially available battery systems. The primary purpose of the HFACL converter is to enable bidirectional power flow between the PV and battery system to and from grid. The output voltage is standard single phase residential outlet voltage. The peak voltage for a $120V_{rms}$ system reaches around 164V, thus the switching devices on the AC side bridge are rated upto 250V to allow a comfortable margin of safety. The placement of auxiliary inductance is important for the design, since an inductor placed in the primary versus the secondary, will lead to different current on the primary and secondary winding.

This can be elaborated using an example. With the specifications mentioned above, the peak cur-

Table 5.2: System parameters for the experimental and simulation setup

Items	Specifications (Simulation)	Specifications (Experiment)
Power (P_{out})	300W	300W
Input Voltage (V_1)	48V (constant voltage source)	48V (constant voltage source)
Output Voltage(V_2)	120V_{rms} (constant voltage source)	120V_{rms} (R-C load)
Auxiliary Inductor ($L_1 + L_2$)	10 μH (Primary)	265μH (Secondary)
Transformer magnetizing inductor (L_m)/ Turns ratio ($n_1 : n_2$)	2.5mH / 1:5	1.2mH / 1:5
output filter (L_3, C)	200μH, 1μF	300μH, 90 nF
Switches	Ideal switches	SUM90142E-GE3 (Primary), IPB17N25S3 (Secondary)

rent at the transformer primary and secondary will be proportional to $5V_1V_2$, since the input voltage is reflected to secondary. If the same inductor is placed at the primary, the peak current is proportional to $\frac{V_1V_2}{5}$. This is a significant difference and the peak current varies with a factor or n^2, where n is the transformer turns ratio. Overall design is affected by the placement, as the PCB traces, switching device ratings and current sensors has to be rated for this. In practice,the primary and secondary leakage inductance can be considered lumped into an equivalent auxiliary inductance, and thus, the design considerations for the high frequency transformer needs to include this. Additionally, the design of the magnetizing inductance of the transformer is very important. Since, with a low magnetizing inductance, the primary current peak value increases and the converter will have to withstand that. The prototype transformer was designed with a magnetizing inductance of $1.2mH$. A detailed description of system parameters for both the simulation and experimental set up is given in Table-5.2.

Fig.5.11(a) demonstrates the simulated waveforms of the primary voltage and current and the secondary voltage. Fig.5.11(b) shows the unfiltered and filtered output current. In case of the experimental study, the output AC voltage source is replaced by a resistive load and a $2\mu F$ capacitor in parallel. This can be approximated as a constant AC voltage source.

The CPSM has been verified in both simulation and hardware and the results seem to be in good agreement with the theoretical analysis. In Figures 5.12 and 5.13, the CPSM and VPSM modulations schemes are simulated respectively. As seen from Fig.5.12, the phase shift between the primary and secondary voltage is kept constant throughout the SPWM sweep. The figures from top to bottom shows the transformer voltages and current at 10^o, 45^o and 90^o angles respectively, over the 60Hz SPWM span. Similarly, in Fig. 5.13, the phase shift varies for different point over the SPWM sweep, thus for instances A, B and C denoted by angles 10^o, 45^o and 90^o, the phase shift change for VPSM is as shown in the figure. The soft switching condition for this specific simulation example has been set as $\phi + \delta_2 = \pi$, and the phase shift angle ϕ is approximately half of δ_1, thus, δ_2 is modulated proportional to $(\pi - m_s sin(\tau))$, where m_s is the modulation index of δ_2. The modulation indexes m_p band m_s are chosen as 0.8 and 0.4 respectively, therefore the $\frac{\phi}{\delta_1}$ ratio and the modulation indexes cancel each other out and the soft switching condition is maintained.

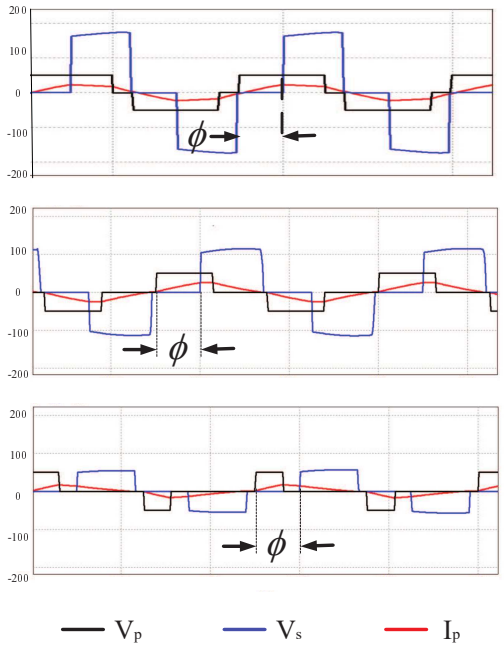

Figure 5.12: Simulation of transformer primary, secondary voltages (V_P, V_S) and primary current (I_P), for CPSM

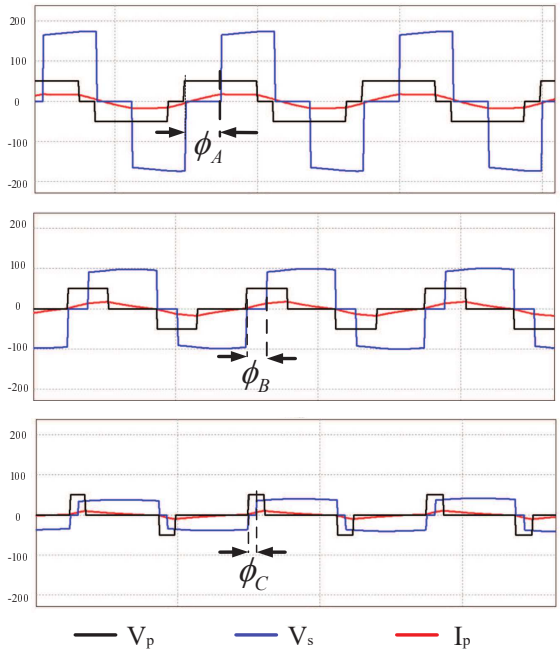

Figure 5.13: Simulation of transformer primary, secondary voltages (V_P, V_S) and primary current (I_P), for VPSM

The input DC voltage has been set to 48V and the output voltage was set to 164Vpeak, or 120Vrms to match typical single phase grid voltage. The primary bridge was modulated with a SPWM keeping the modulation index constant at 0.7 to achieve a low harmonic distortion output. The individual experimental waveforms for the primary and secondary bridge voltage and transformer primary current around the peak of the sine wave of the SPWM, are shown in Fig.5.14. As seen from the figure, the primary and secondary bridge switches such that the soft switching conditions as given in Table-4.1, are satisfied, Thus the switches transition in ZVS. The CPSM has been demonstrated by magnifying part of the waveform in Fig. 5.15 where it is clear that the phase shift between the primary and secondary bridge voltage is kept constant. In Fig.5.16 the output AC voltage is shown. The output current is in phase with the output voltage as a resistive load is used. Although a peak efficiency of 91% is obtained, it has been noted based on the winding loss in the transformer, approximately $3-4\%$ improvement in efficiency can be achieved with a transformer winding made up of stranded wires or planar winding. Majority of the losses were contributed

by winding losses and the conduction losses. Since high rms current was needed on the primary side as the primary voltage is much less, it is difficult to reduce the conduction loss with regular Si-based FETs. It is also expected to further improvement to the efficiency can be made by using VPSM where the fundamental modulation with ZCS on the primary bridge (such as TPS-5) helps with ZCS and low rms current. A breakdown of the observed losses for the converter is shown in Fig. 5.18.

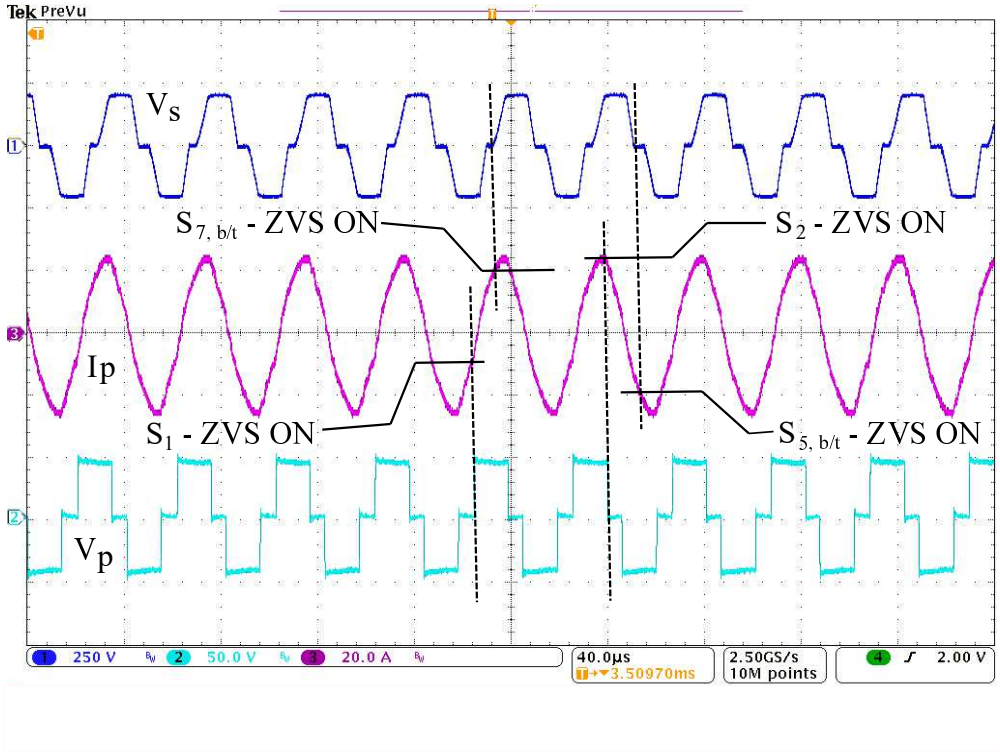

Figure 5.14: Transformer primary (V_p), secondary (V_s) voltage and transformer primary current (I_p)- magnified at the peak

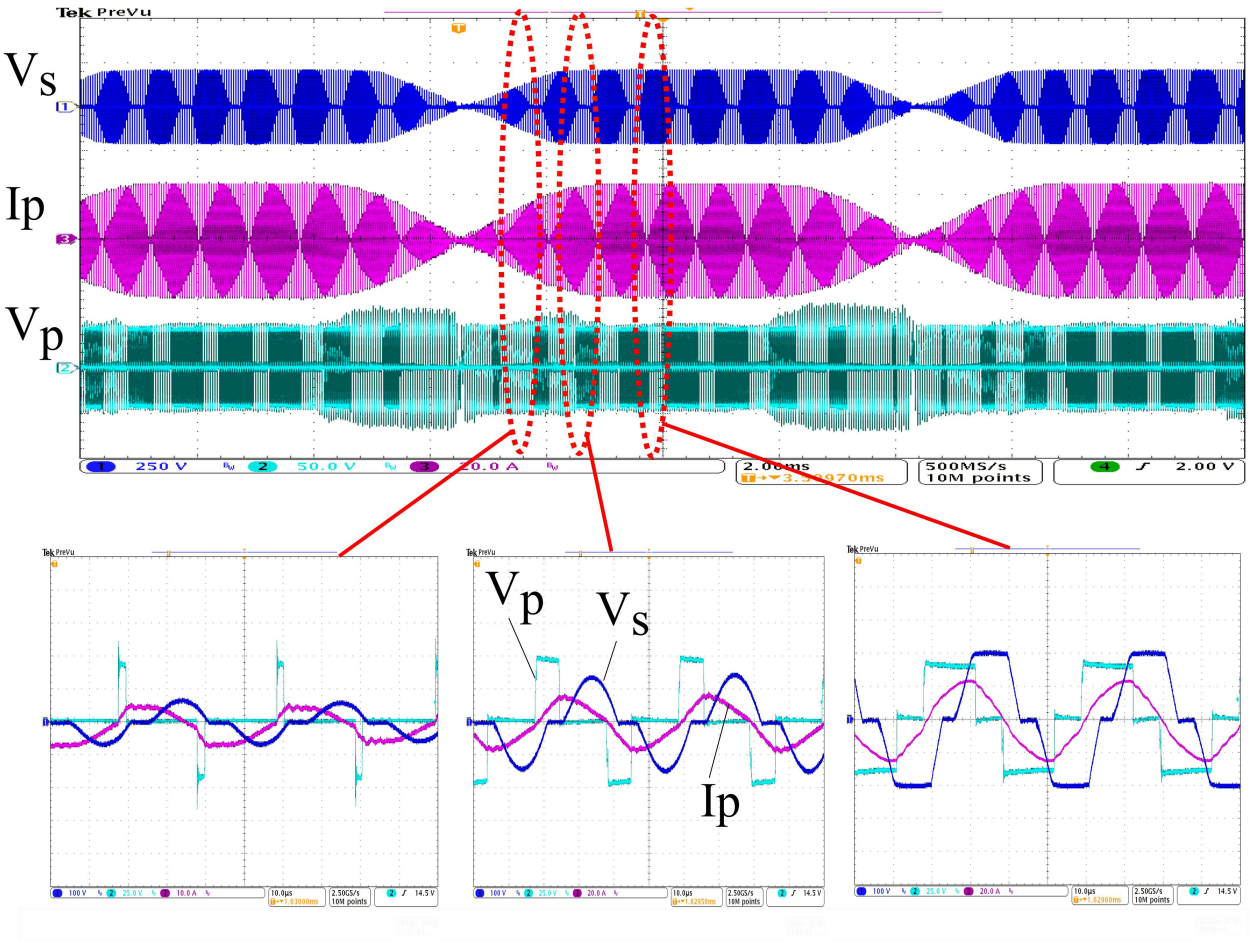

Figure 5.15: Experimental verification of CPSM

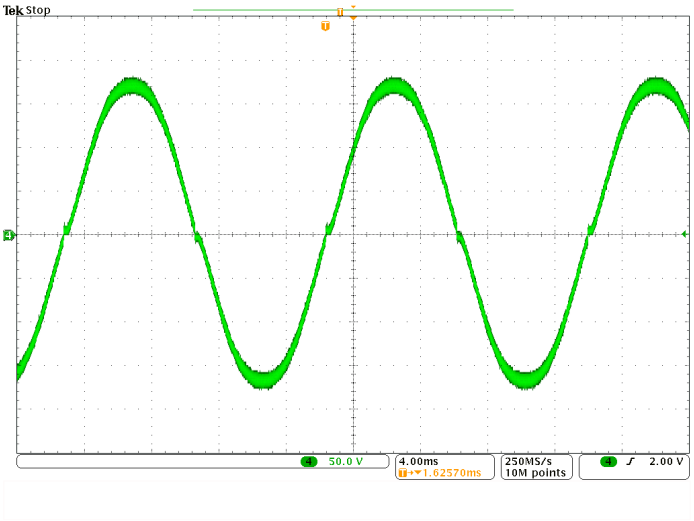

Figure 5.16: Output voltage V_2 across a resistive load for the HFACL converter

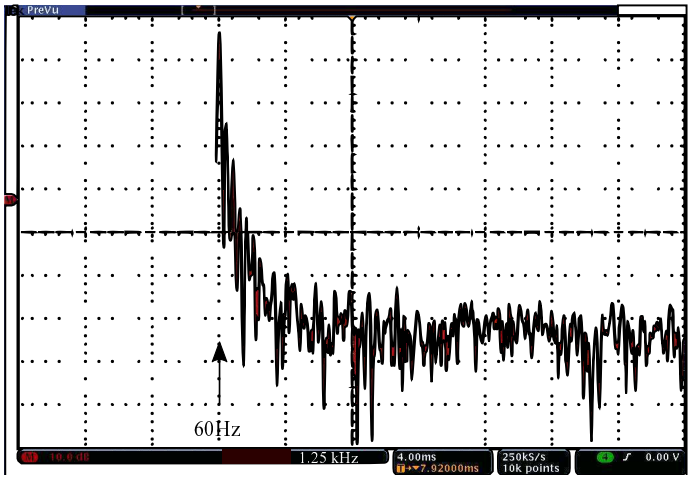

Figure 5.17: Fast fourier transform of the output AC voltage

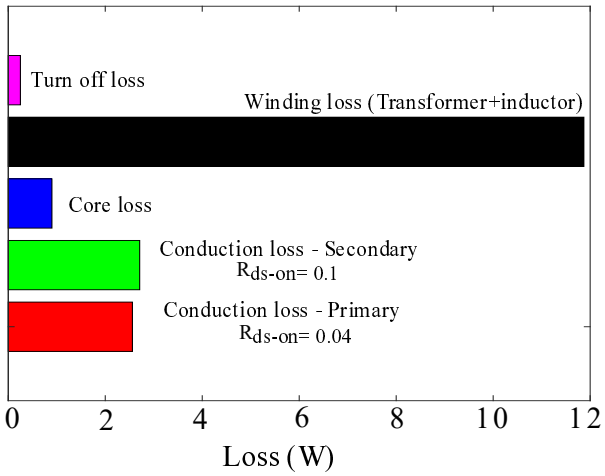

Figure 5.18: Breakdown of different losses for 200W operation

A fast fourier transform of the output voltage is shown in Fig. 5.17. It is seen from the figure that the overall harmonic distortion is low.

5.4 Summary

This chapter presented a new modulation scheme for bidirectional AC link micro inverter based on dual active bridge (DAB) topology concept. The proposed converter allows DC-AC conversion without requiring the use of an unreliable, costly and bulky DC link capacitor. This significantly improves the lifetime of the microinverter. In addition to the power conversion for interfacing renewable energy sources in a grid tied system, the converter allows soft switching operation for all active switches with simple implementation. The novel topology uses 12 active switches to interface a bidirectional DC port to the grid. Any general power source can be used since the converter functionality doesn't depend on the voltage level of the sources connected to it. Additionally, the use of triple phase shift modulation allows the converter to achieve soft switching over a very wide range of load and voltages. A novel modulation scheme for the converter is also proposed which combines the fundamental triple phase shift modulations to form a composite modulation

to achieve a low harmonic distortion sinusoidal output with high efficiency. Single stage operation has its advantages of removing the need for a decoupling stage, and also improving the efficiency of the overall converter. However, single stage operation has a drawback of introducing low frequency ripple current at the input. This is detrimental for operations such as maximum power point tracking etc. Thus an input filter is employed for smooth input current. A three winding transformer with a full bridge interfacing the third winding upgrades the converter to a new three port converter where the third port may act as an energy storage port and can complement the intermittent nature of the renewable sources. Additionally, the third port can also act as a ripple port that eliminates the input current ripples that are typical for a single stage single phase microinverter. Brief description and simulation result are presented for the three port converter, derived from the proposed topology.

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CHAPTER 6: IMPROVED THREE PORT CONVERTER BASED ON DUAL ACTIVE BRIDGE

The MPC is an important component of a renewable energy based power system. Typically, multiple energy sources supplying a single load uses multiple power conversion units in a cascaded or parallel fashion. These arrangements comes at a cost of high loss and reduced flexibility of operation [4]. Increasingly, MPCs are being used for single stage power conversion systems, which interfaces two or more input sources and supplies one or multiple load. A detailed discussion of the present state of the art on MPCs are given in [4]. Most of the reported MPCs typically used for DC to DC power conversion [5]. An additional DC-AC stage is necessary when the renewable sources are feeding the grid or any AC appliances. Only a few multiport DC-DC-AC converters are currently reported in the open literature. In [6] and [7], an AC-link based TPC is proposed. Topologies proposed in [6], [7] and [8] utilize an AC-link based four quadrant bridge which requires a back to back switch for all the input and output ports. Here, the overall cost and efficiency is typically less. Additionally, series resonant or parallel resonant tank are used to achieve soft switching. In [2], a bridgeless boost rectifier is proposed, which can be extended to realize a three port converter. However, detailed analysis and verification for the TPC are not presented. The DAB based "DC to AC" conversion is discussed in [9], [10], [11]. It utilizes a single or dual stage conversion by means of a two winding transformer isolated DAB topology with four quadrant switches on the AC port. The fundamental modulation schemes used in these works are widely varied. For the DAB based converters, the majority of the works use dual phase shift modulation, except in [10], where a triple phase shift modulation was used. A detailed description of the dual and triple phase shift modulation is given in [12] - [16]. Since the triple phase shift modulation has effectively three degree of freedom control, many researcher have used numerical, online optimization based approach to control DABs in [17] - [19]. This approach is later adopted in DAB based DC-AC conversion as seen in [10] and [11]. However, online optimization based modulation is computa-

tionally intensive and expensive to implement, especially for applications like photovoltaic (PV) microinverters systems. In [1], the authors proposed a sine pulse width based modulation for the DAB based DC-AC topology which significantly reduces the computational burden and the output filter size while improveing harmonic distortion. Additionally, a TPC is proposed by extending the DAB based DC-AC by simply adding another winding and a full or half bridge to interface the third DC port. This is architecturally similar to [7] and [8] but the novel modulation ensures ZVS with simple control implementation.

However, the proposed TPC in [1] still uses 16 active switches for three port power conversion which significantly increases the power loss and cost of the power stage. In this work, a reduced and improved three port topology is proposed which utilizes similar DAB based DC-AC architecture, but employs a half bridge on the AC side. This limits the modulation scheme to be dual phase shift only, but doesn't alter the feasibility of using a SPWM based composite modulation scheme. The proposed composite modulation scheme consists of dual phase shift modes at the switching frequency level, and over the span of the modulating low frequency sine wave individual dual phase shift modes change their parameters. The proposed topology reduces the required number of active devices to half of what is used in [1], greatly improving the cost and efficiency greatly. The proposed topology uses an interleaved boost converter for power conversion between the two DC ports and hence, requires no transformer isolation. Therefore, a two winding transformer can be used for three port power flow. This is a significant improvement as the design of the three winding transformer in a tight package is increasingly difficult for higher power flow. Also, since most of the time a TPC is used for two port power flow at a given time (e.g for a PV-Battery system, power flows between PV to load majority of the day), typical utilization of a three winding transformer is approximately 66%. In the proposed TPC, the transformer being two winding has a 100% utilization and the construction is much simpler.

The detailed analysis of the proposed TPC in all three different power flow modes are given in Section - II, the characterization of the proposed converter is given in Section - III where various

important features such as soft switching, variation of power flow based on system parameters etc, are discussed. In Section - IV, design considerations for the proposed converter as well as the modification required for implementing embedded ripple port are discussed. This is followed by experimental validation in Section - V. The discussion is concluded in section -VI.

6.1 Proposed Three port Converter

The proposed TPC is illustrated in Fig. 6.1. As seen from [1], the proposed TPC is based on a DAB structure, where the secondary bridge is replaced by a half bridge architecture. The secondary switches are capable of four quadrant operation. This not only allows seamless bidirectional power flow, it also ensures the output can be directly connected to AC and no additional unfolding circuit is required. The DC-AC conversion is accomplished by using the high frequency transformer and the leakage inductance as the AC link. No intermediate power decoupling stage is required. However, decoupling is needed on the DC terminals, when interfacing a purely DC source.

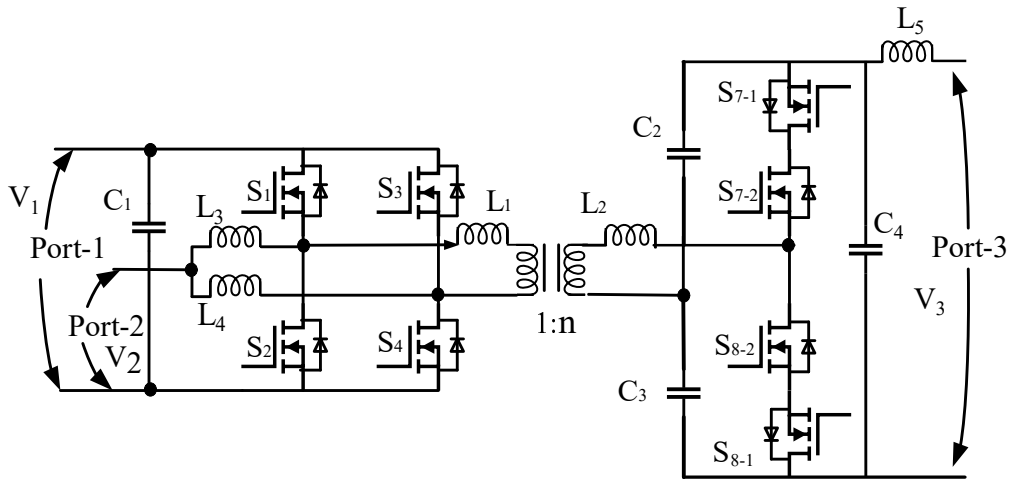


Figure 6.1: Proposed three port converter based on dual active bridge topology

The proposed TPC also includes two interleaved inductors that acts as the input to the second port. The inductors L_3 and L_4 are typically of large value compared to the leakage inductances L_1 and

L_2. Note that the leakage inductances are considered to be at both the primary and secondary of the high frequency transformer. For simplification of analysis, the leakage inductances can be considered lumped on to either the primary or secondary. In case of a lumped and primary referred equivalent inductance, its value can be represented as: $L = L_1 + \frac{L_2}{n^2}$. As the secondary bridge is essentially a half bridge, the capacitors C_2 and C_3 are used as the AC link capacitors. Since the output is AC and hence the magnitude of the output voltage is sinusoidally varying, the choice of C_2 and C_3 impacts the DC voltage of the secondary bridge during each high frequency switching cycle. With large capacitance for C_2 and C_3, the DC voltage remains steady however, it introduces low frequency reactive power. Therefore, in the design, a trade off is required to balance the reactive power and low ripple voltage. Additionally, since they are carrying AC voltage, polar electrolytic capacitors cannot be used and non polar capacitors are required.

6.1.1 Operation Principles

The operating principles for the proposed TPC can be subdivided largely into four power flow modes: Port-1 to port-3, port-2 to port-3, port-1 and port-2 to port-3 (three port power flow) and finally port-1 to port-2.

6.1.1.1 "Port-1 to Port-3"

The equivalent circuit for the power flow from port-1 to port-3 is shown in Fig. 6.2. Since the port-2 is not energized, the two parallel boost inductors L_3 and L_4 are directly connected across the primary side of the high frequency transformer. Since the values of L_3 and L_4 are typically high, the impact of the boost inductors is diminishing and only contributes a small leakage current through them. The effect of which can be characterized by a marginal increases in the peak value of the overall primary current.

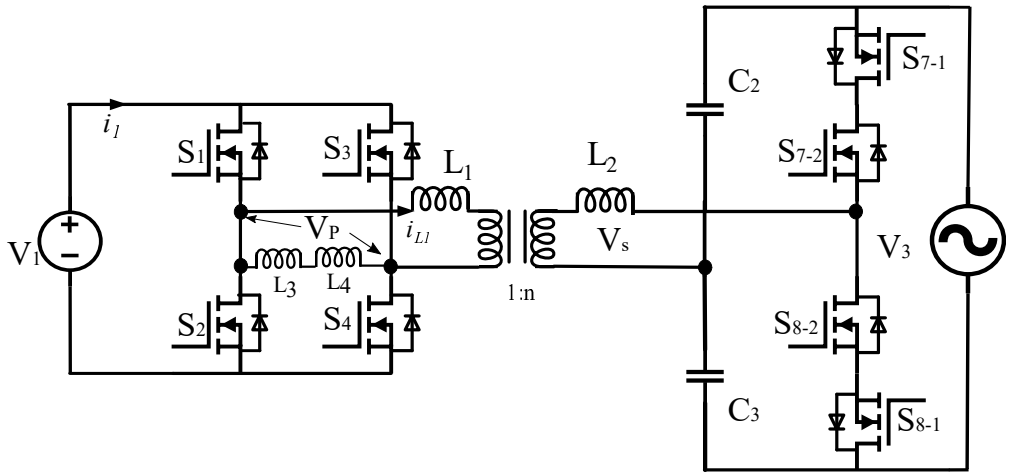


Figure 6.2: Port-1 to Port-3 equivalent circuit

Thus, the power flow mode between port-1 to port-3 follows the DAB principles. The proposed modulation is similar to the analysis carried out in [1], except the fundamental modulation is dual phase shift (DPS) in nature, rather than triple phase shift. There may be several different DPS modes possible, however, since the secondary bridge structure is half-bridge in nature, and primary is modulated in three level waveform, only the feasible DPS modes are as shown in Fig. 6.3.

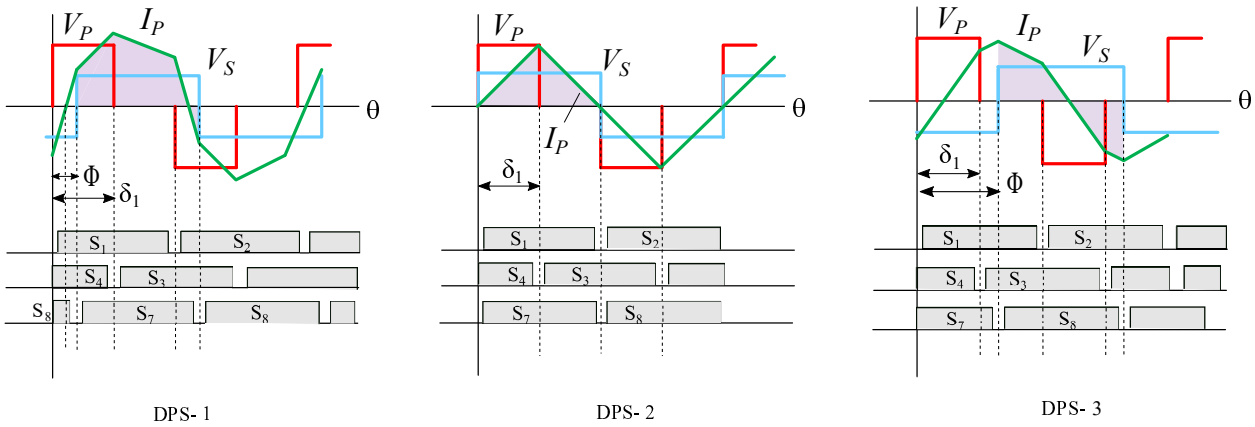


Figure 6.3: Dual phase shift modulations and gating signals for both the primary and secondary bridges

The gate pulses for both the primary and secondary bridges are shown in Fig. 6.3. Note that for

the secondary switches, S_7 and S_8 represents either or both the back to back switches S_{7-1}, S_{7-2} and S_{8-1}, S_{8-2} respectively. The synthesis of the 60Hz AC waveform is demonstrated in Fig. 6.4 using sine PWM (SPWM) modulation. Based on whether the output AC voltage is in positive or negative half cycle, S_{7-1}, S_{8-1} or S_{7-2}, S_{8-2} are kept turned on through out the half cycle. This is done to prevent the AC bus being shorted through the anti parallel diodes. It also allows soft switching during the switch turn on dead time. This is explained in details in [1].

In Fig. 6.4, the composite modulation is shown for the positive half cycle of the AC sine wave, where the high frequency fundamental modulation changed between DPS-1, DPS-3 and single phase shift modulation (SPS). The quarter cycle symmetry is maintained. As a result, the fundamental modulation pattern repeats in each quarter cycle.

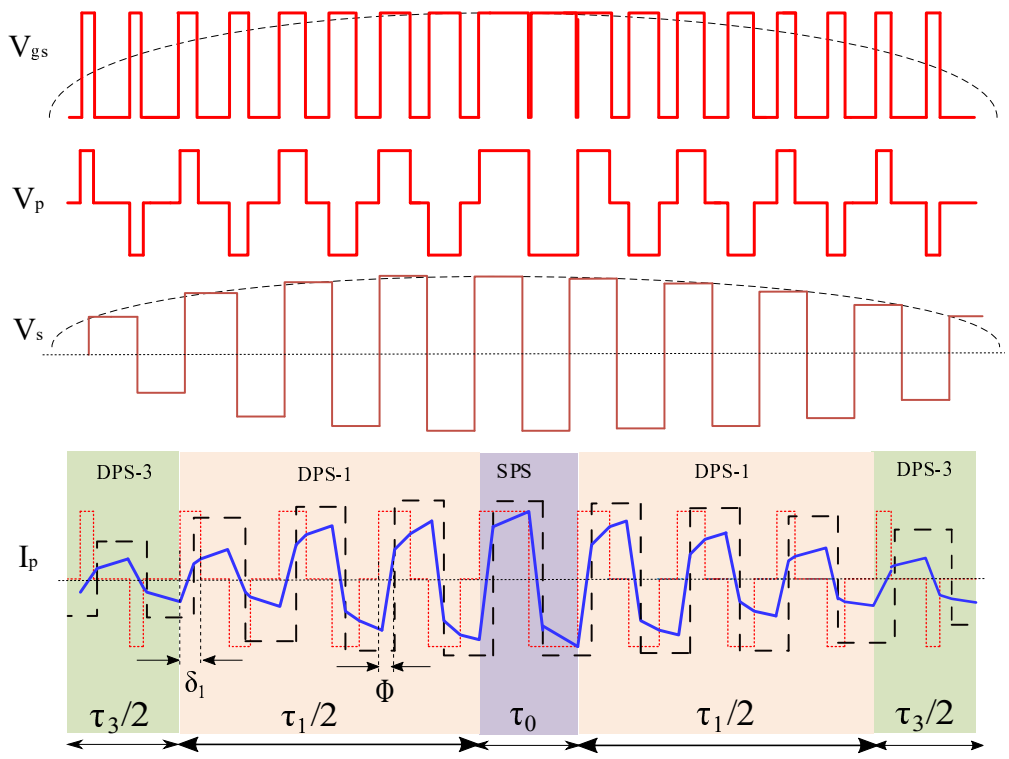


Figure 6.4: Composite modulation during the AC positive half cycle using fundamental DPS and SPS modulation

It is noted that the SPS appears in the composite modulation only if the SPWM index (m_P) is 1.

For any $m_P < 1$, the composition comprises of DPS-1 and DPS-3 only. Also note that, DPS-2 is an unique mode where the phase shift between input and output bridge, $\phi = 0$. The conduction angle of the primary bridge is noted as δ_1 through out this work. Therefore, a composite modulation comprising of only DPS-2 is also a feasible candidate, but not discussed here.

The analytical expression for the power and the soft switching inequalities can be found similar to [1]. In Fig. 6.3, the shaded portion represents the average current over one switching cycle and can be calculated analytically by integrating the current expression over the angle span: $\{\phi : \pi + \phi\}$ for DPS-1 and DPS-3, and $\{0 : \pi\}$ for DPS-2. Depending on the modulation index and the phase shift ϕ, the angle spans of each fundamental DPS mode within one half cycle of the composite modulation is denoted by τ_1, τ_2 and τ_3 respectively. This is also represented in Fig. 6.4.

Table 6.1: Mode boundaries and soft switching conditions for fundamental modes

Modulation	Mode Boundary	Soft Switching condition
DPS-1	$0 \leq \delta_1 \leq \pi,$ $0 \leq \phi \leq \pi,\ \delta_1 \geq \phi$	$\delta_1 V_1 - \pi V_3 + 2\phi V_3 \geq 0,$ $\pi V_3 - \delta_1 V_1 + 2\phi V_1 \geq 0,$ $\pi V_3 + \delta_1 V_1 - 2\delta_1 V_3 + 2\phi V_3 \geq 0$
DPS-2	$0 \leq \delta_1 \leq \pi,\ \phi = 0$	$\pi V_3 = \delta_1 V_1,$ $\pi V_3 + \delta_1 V_1 - 2\delta_1 V_3 \geq 0$
DPS-3	$0 \leq \delta_1 \leq \pi,$ $0 \leq \phi \leq \pi,$ $0 \leq \delta_1 \leq \phi$	$\delta_1 V_1 - \pi V_3 + 2\phi V_3 \geq 0,$ $\pi V_3 + \delta_1 V_1 + 2\delta_1 V_3 - 2\phi V_3 \geq 0,$ $\pi V_3 + \delta_1 V_1 \geq 0$

Table- 6.1 contains the soft switching conditions and the mode boundaries in terms of range of δ_1 and ϕ. Note that for DPS-2, the soft switching conditions are obtained based on zero current switching scheme, however, for DPS-1 and DPS-3 it is based on ZVS instead. The power flow

expressions for each DPS scheme over one switching cycle can be summarized as:

$$\mathcal{P}_1^i = V_1 V_3 sin(\omega_L t) \frac{\{\pi\delta_1^i - \phi^2 - (\delta_1^i - \phi)^2\}}{4\omega L} \tag{6.1}$$

$$\mathcal{P}_2^j = V_1 V_3 sin(\omega_L t) \frac{\delta_1^j(\pi - \delta_1^j)}{4\omega L} \tag{6.2}$$

$$\mathcal{P}_3^k = V_1 V_3 sin(\omega_L t) \frac{\delta_1^k(\delta_1^k - 2\phi + \pi)}{4\omega L} \tag{6.3}$$

where, $\omega_L = 2\pi f_L$, f_L being the line frequency, which is 60Hz for this work. $\omega = 2\pi f$ where, f is the switching frequency. i, j, k are the indices describing the number of high frequency switching cycle of DPS-1, 2 and 3 respectively, that appears in a composite modulation. $\mathcal{P}_1$, $\mathcal{P}_2$ and $\mathcal{P}_3$ are power flow for each high frequency switching cycle of DPS-1, 2 and 3 respectively.

Typically, in SPWM modulations, modulation index $m_P < 1$. When the similar range of m_P is applied here, no single phase shift (SPS) modulation is possible. Also, typically, $\phi \neq 0$ as it will be demonstrated in experimental results, therefore DPS-2 does not appear in the composite modulation as well and the composite modulation is synthesized purely using DPS-1 and DPS-3.

The overall output average power can be calculates in this case as:

$$P_{out} = \frac{2\tau_1 \sum_i \mathcal{P}_1^i|_{sin(\omega_L t)=1} + 2\tau_3 \sum_k \mathcal{P}_3^k|_{sin(\omega_L t)=1}}{\pi^2} \tag{6.4}$$

From 6.4, the output power can be found. However, since the output AC voltage is time varying as noted in (1) - (3), the output power will also be sinusoidally varying. Thus, the average output power can be found by setting $sin(\omega_L t) = 1$. Based on the modulation index and the phase shift, the angle span of the DPS modulation in the composite modulation can be expressed as following:

$$\tau_1(P.U) = \frac{2}{\pi} sin^{-1} \frac{\phi}{\pi} \tag{6.5}$$

$$\tau_3(P.U) = \frac{2}{\pi}(\pi - sin^{-1}\frac{\phi}{\pi}) \tag{6.6}$$

In addition, the DPS modes over the composite modulation, changes because δ_1 varies sinusoidally as per SPWM. Thus a practical approach to determine the average output power will be to replace the δ_1 values with its average value, over the corresponding angle spans for a given composite modulation. The average δ_1 can be calculated as following:

$$DPS1: \ \delta_1 = \frac{2}{\tau_1}\int_{\frac{\tau_3}{2}}^{\frac{\tau_3+\tau_1}{2}} m_p sin\tau d\tau \tag{6.7}$$

$$DPS3: \ \delta_1 = \frac{2}{\tau_3}\int_{0}^{\frac{\tau_3}{2}} m_p sin\tau d\tau \tag{6.8}$$

Therefore, based on the phase shift and modulation index, the average output power can be varied. From fundamental DAB modulation principle, the power flow can be reversed if the phase shift becomes negative, or in other words, if the phase of port-3 leads the phase of port-1, current flows from port-3 to port-1 and in this way, bidirectional power flow is achieved. However, for AC to DC power flow, other important aspects are needed to be considered, such as synchronizing the secondary bridge modulation with the AC single phase locked loop (PLL) etc. Failing to do so, can cause the AC bus to be shorted by the anti parallel diodes of the secondary switches. Also, the power flow can be reduced to zero between port-1 to port-3 bus using $\phi = 0$ or $\phi = \pi$ when $\delta_1 = \pi$ kept constant through out the SPWM cycle, instead of modulating. This is validated from (1)- (4).

6.1.1.2 "Port-2 to Port-1"

For the power flow from port-2 to port-1 is as shown in Fig. 6.5. As discussed previously, with properly chosen δ_1 and ϕ, the average power flow between port-1 and port-3 becomes zero. The equivalent circuit for the power flow between port-1 and port-2 becomes similar to an interleaved bidirectional boost converter.

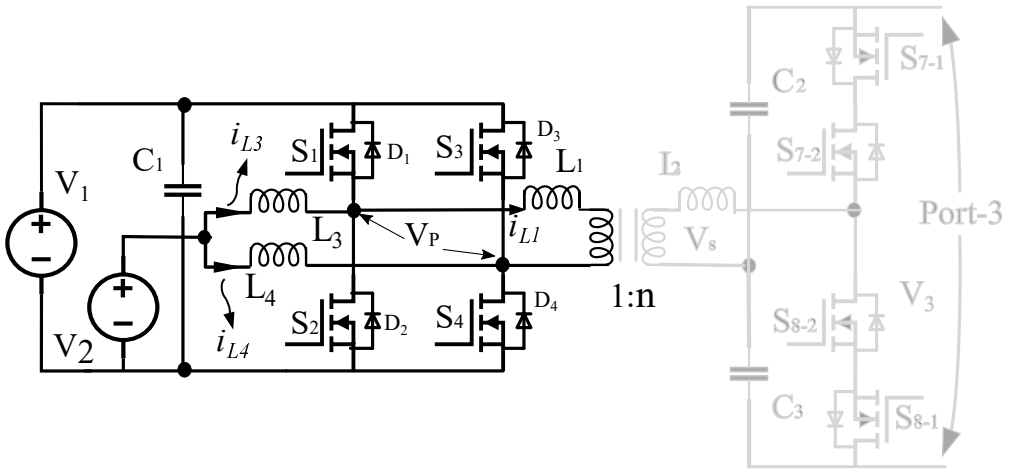


Figure 6.5: Port-2 to Port-3 power flow mode equivalent circuit

As seen from Fig. 6.5, with a DC voltage source connected to port-2, the boost inductors L_3 and L_4 act as a constant current source. With δ_1 and ϕ equals to π, the S_1 and S_4 pair and S_2 and S_3 have no overlap between them. Thus, the two boost circuits are 180 degree out of phase from each other. This is typically how an interleaved boost converter operates, as discussed in [2]. Since the primary bridge is still operated at $\delta_1 = \pi$, the primary current i_1 is non zero. It increases with a ramp of $\frac{V_1}{\omega L}$ for the duration when the switches S_1 and S_4 are turned on and decreases with the same ramp rate when S_2 and S_3 are on. This inherently provides ZVS turn on for the primary bridge switches. This primary current is generated because of the DAB operation and it does not contribute to the boost converter output. The circulating current simply circulates back to the source, which contributes to to the turn off losses as well as overall conduction loss. Addiitonally, i_1 contributes to the core loss of the high frequency transformer which will otherwise not be present if the power flow is strictly between port-1 and port-2. Therefore the proposed switching strategy in [3] is not adopted here.

Instead, the top and bottom switches are constantly overlapped during the switching period. With this strategy, the boost converters operate in parallel to each other. i_1 becomes zero with this proposed switching and thus there is no circulating current which contributes to turn off, conduction and core losses. However, this naturally removes the advantage of ZVS switching as well. With

the proposed switching strategy, the boost inductors are designed so that ideally the converter operates at critical conduction mode (CCM). The design is elaborated in the following section. An illustration of the two different switching strategies is shown in Fig. 6.6 and 6.7.

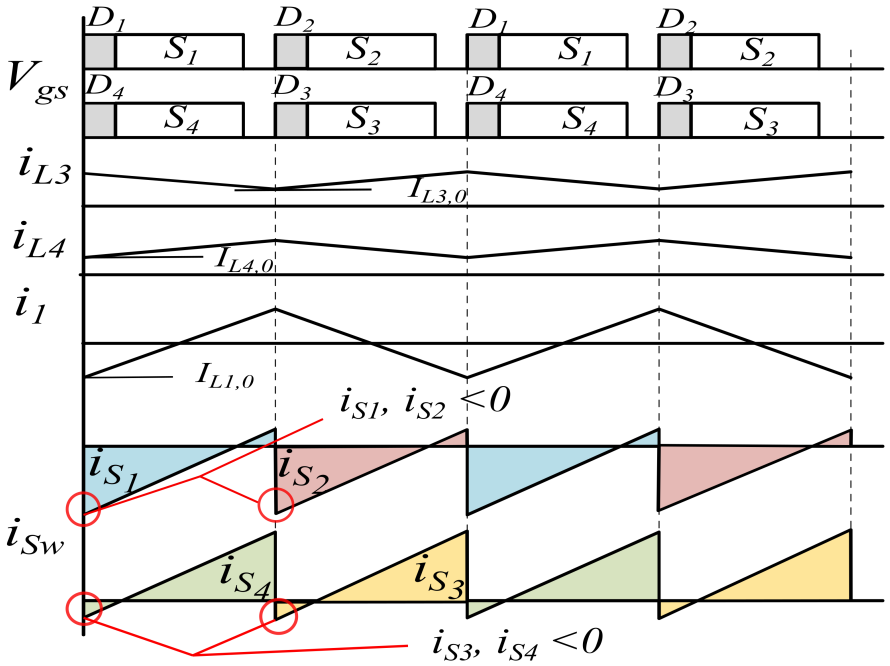


Figure 6.6: Key waveforms for Boost converter mode of operation - Switching strategy with $\delta_1 = \pi$

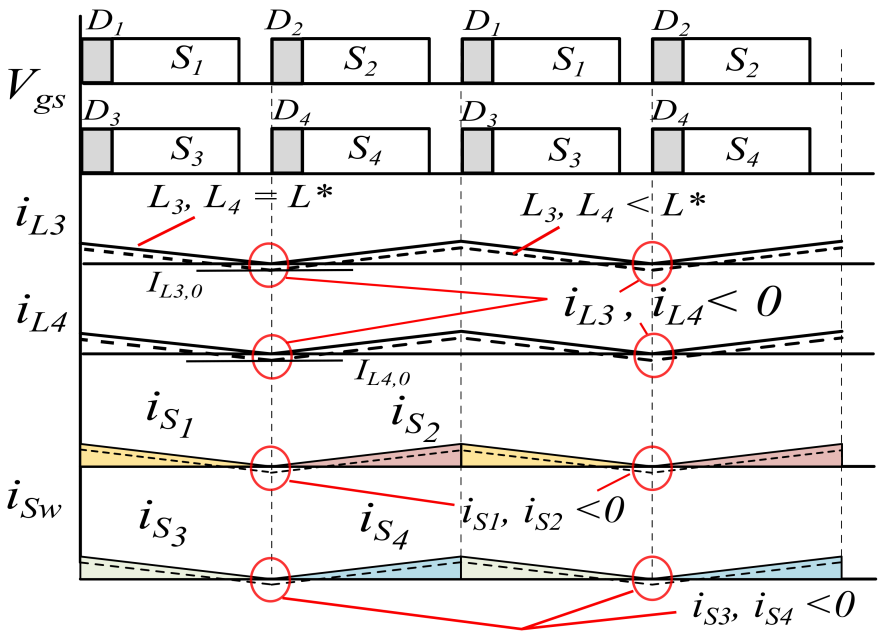


Figure 6.7: Key waveforms for Boost converter mode of operation - Switching strategy with $\delta_1 = 0$

It is noted that in Fig. 6.6, the traditional switching strategy is employed where the two interleaved boost converter operate in 180 degree out of phase from each other. The inductor current peak for the inductor L_3 occurs when S_2 turns off and S_1 turns on. Similarly for L_4, peak occurs during the transition between S_4 turn off and S_3 turn on. With an underlying assumption that the leakage inductance L_1 is chosen to be much less than the boost inductors ($L_1 << L_3, L_4$), it can be concluded that the primary current due to DAB operation is much higher than the boost inductor currents. Thus, soft turn on is achieved for all primary switches because of primary current alone. The expression for the switch currents in terms of θ, are as follows:

$$i_{S1} = \frac{V_1}{\omega L_1}\theta - \frac{V_2(\pi+\theta) - V_1\theta}{\omega L_3} + I_{L_{1,0}} - I_{L_{3,0}} \tag{6.9}$$

$$i_{S2} = -\frac{V_1}{\omega L_1}(\theta) + \frac{V_2(\theta-\pi)}{\omega L_3} + I_{L_{3,0}} - I_{L_{1,0}} \tag{6.10}$$

$$i_{S3} = \frac{V_1}{\omega L_1}\theta + \frac{V_1}{\omega L_4}(\theta - \pi) - \frac{V_2}{\omega L_4}\theta + I_{L_{1,0}} - I_{L_{4,0}} \tag{6.11}$$

$$i_{S4} = -\frac{V_1}{\omega L_1}\theta + \frac{V_2}{\omega L_4}\theta + I_{L_{4,0}} - I_{L_{1,0}} \tag{6.12}$$

where, the duty ratio of all the primary switches are assumed to be approximately equal to 50% with a small dead time before turn on and off to facilitate ZVS. Thus the port-1 voltage $V_1 = 2V_2$.

The proposed parallel boost modulation strategy described in Fig. 6.7 takes advantage of having the two boost converter operating in phase with each other and avoiding the circulating current because of DAB operation. From a high level controller perspective, this can be achieved by setting $\delta_1 = 0$. The boost inductor and switch currents can be easily found in many previous literatures. However, since the operation requires atleast CCM operation and in practice, the inductor current is required to reach a negative value in order to forward bias the anti-parallel diodes before turning on any switch. This is also illustrated in Fig. 6.7. As discussed previously, the boost inductor design is critical for this modulation and the critical boost inductor value is shown here as L^*, which ensures CCM. As seen from the Fig. 6.7, with $L_3 = L_4 = L^*$, the inductor current reaches zero at $\theta = \pi$ and with a boost inductor of $L_3, L_4 < L^*$, the currents (i_{L3} and i_{L4}) becomes negative.

The expression for the switch currents are given as:

$$i_{S_2}, i_{S_4} = \frac{V_2}{\omega L^*}(\theta - \pi) + I_{3,0}\ (or\ I_{4,0}) \tag{6.13}$$

$$i_{S_1}, i_{S_3} = \frac{V_2}{\omega L^*}(\theta + \pi) - \frac{V_1}{\omega L^*}\theta + I_{3,0}\ (or\ I_{4,0}) \tag{6.14}$$

The critical inductance value can be obtained from the rated power flow between the port-1 and port-2 and the voltage of port - 1.

6.1.1.3 "Port-2 to Port-3" or "Port-1 and Port-2 to Port-3"

The power flow between port-2 and port-3 or simultaneously from port-1 and port-2 to port-3 is a combination of the previously described power flow modes. During "port-2 to port-1" power flow mode, the port-1 capacitor C_1 is charged through the interleaved boost converter to the voltage V_1. Whereas, the power flow from the primary to the secondary side of the transformer is governed by the DAB (DPS) principle. Thus the SPWM composite modulation described previously, is maintained here. An equivalent circuit of this mode is shown in Fig. 6.8.

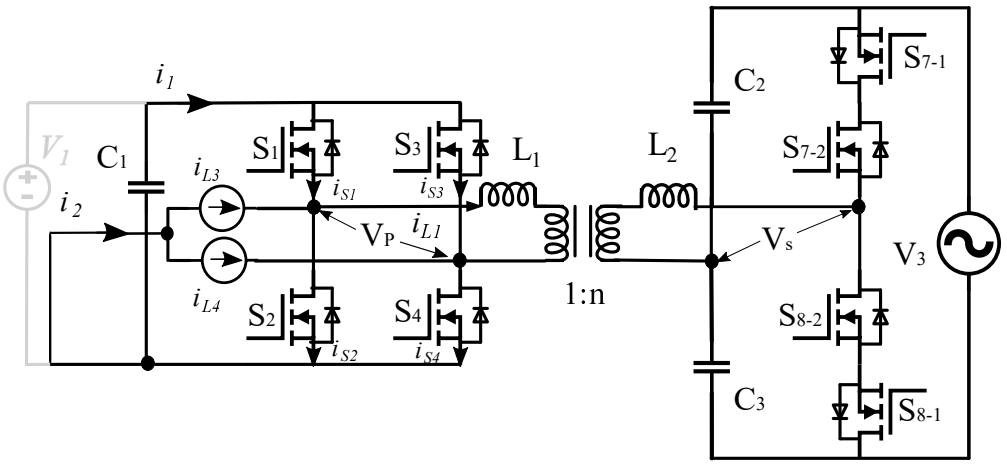


Figure 6.8: Equivalent circuit for power flow mode between port-1, port-2 to port-3

The port-2 boost inductors together with the applied voltage source, can be approximated to two interleaved current sources. Since the inductors act as traditional boost inductors, inductor currents are similar to previously discussed expressions. The current sources are shown as i_{L_3} and i_{L_4} respectively. From the previous analysis, the primary current i_{L_1} can be expressed as the sum of the port-2 current sources and the current supplied from the port-1 power source. Note that, if a voltage source is not connected to the port-1 (as seen by the faded portion of Fig. 6.8), the capacitor C_1 acts as a voltage source. The expression for i_{L_1} in DPS-1 mode is as follows:

$$i_{L_1}(\theta) = \frac{V_1 + V_3}{\omega L}.\theta + i_{L_1}(0) + i_{L_3}(\theta) \tag{6.15}$$

$$i_{L_1}(\theta-\phi) = \frac{(V_1 - V_3)(\theta-\phi)}{\omega L} + i_{L_1}(\phi) + i_{L_3}(\theta-\phi) \tag{6.16}$$

$$i_{L_1}(\theta-\delta_1) = \frac{-V_3(\theta-\delta_1)}{\omega L} + i_{L_1}(\delta_1) \tag{6.17}$$

where, L is the combined leakage inductance of the high frequency transformer considering both primary and secondary leakage, $L = L1 + \frac{L_2}{n^2}$. The negative half cycle can be analyzed similarly as the DAB waveforms are symmetrical, ignoring parasitics or assuming that the effects of parasitics are symmetric as well. It is to be noted that during the positive half cycle, inductor current - i_{L_3} and during negative half cycle, inductor current - i_{L_4} contributes to the overall primary current i_{L_1}.

For DPS-3, mode equations can be obtained similar to "port-1 to port-3" analysis. Assuming perfectly matched boost inductors, it can be concluded that the average boost inductor currents are equal. Hence there is no direct contribution from port-2 to port-3 power flow. However, if there is no active voltage source present in port-1, port-1 voltage is maintained at $\frac{V_2}{1-D}$ by the boost stage, where D is the duty ratio (which is 50 % as discussed before). Thus, the steady state equations can be obtained by replacing V_1 with $2V_2$ in (15) - (17) for DPS-1 and DPS-3 mode.

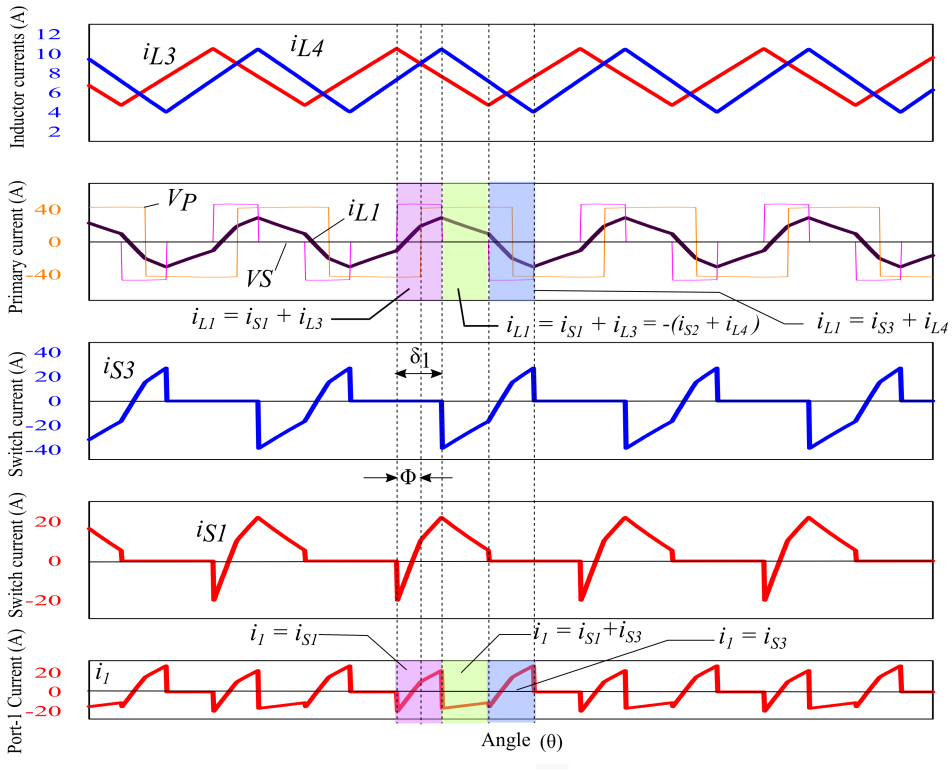


Figure 6.9: Simulation of boost inductor current, switch currents and the port-1 input or output current

In Fig. 6.9, the boost inductor currents, i_{L_3} and i_{L_4}, the upper two switch currents - i_{S1} and i_{S2} and the port-1 current - i_1 are simulated. As seen from the figure, port-1 current is always equal to the sum of the switch currents i_{S1} and i_{S3}. The port-2 current i_2 is the summation of i_{L_3} and i_{L_4}:

$$\begin{aligned} i_1 &= i_{S_1} + i_{S_3} \\ i_2 &= i_{L_3} + i_{L_4} \end{aligned} \tag{6.18}$$

When an active voltage source is connected across the port-1, the average of inductor current becomes zero as there is no power flow between port-1 and port-2. Thus active power flow is only between port-1 and port-3.

6.2 Performance Evaluation

The proposed topology can achieve power flow between any two ports and can simultaneously allow power flow from port-1 and 2 to port-3. Each of the ports is bidirectional since the switching devices allow bidirectional power flow inherently. Major performance metrics for the proposed converter can be the power flow range, soft switching range, low frequency input ripple current rejection etc.

6.2.1 Soft switching

As shown in the Table- 6.1, the necessary soft switching condition for all three DPS modes mentioned are given in terms of a set of inequalities. The simplest way of determining a soft switching condition that is true for multiple DPS modes is to map the overlapping zones enclosed by these inequalities.

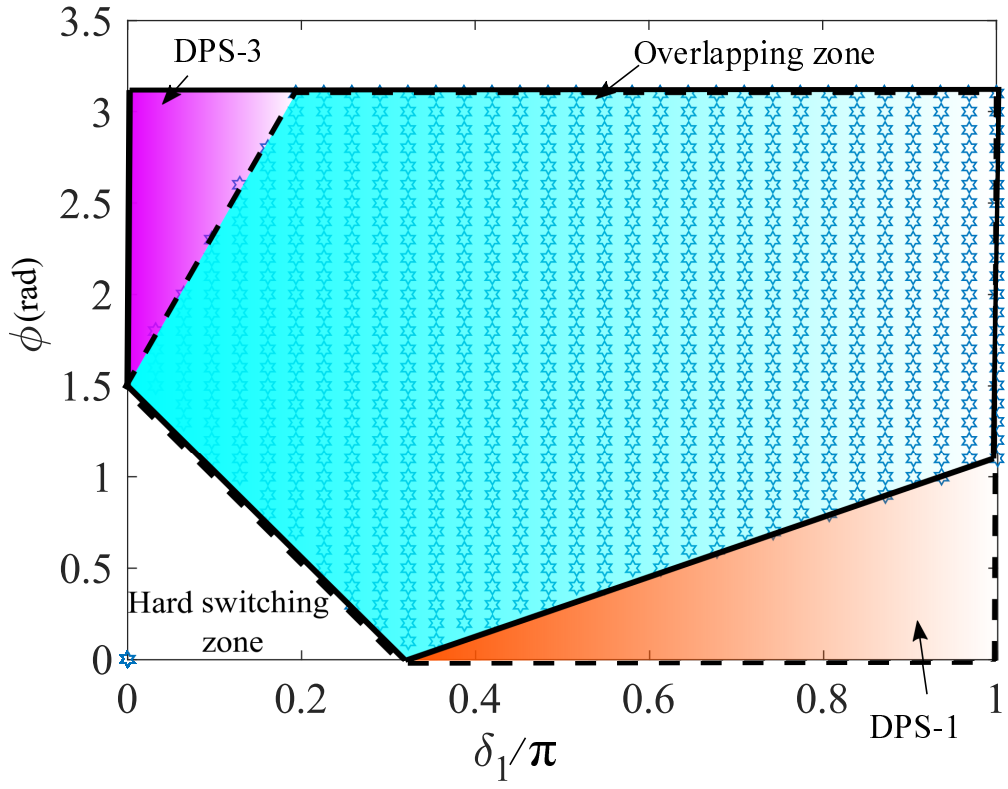


Figure 6.10: Soft switching zone for DPS-1, DPS-3 and the composite modulation using DPS-1 and DPS-3

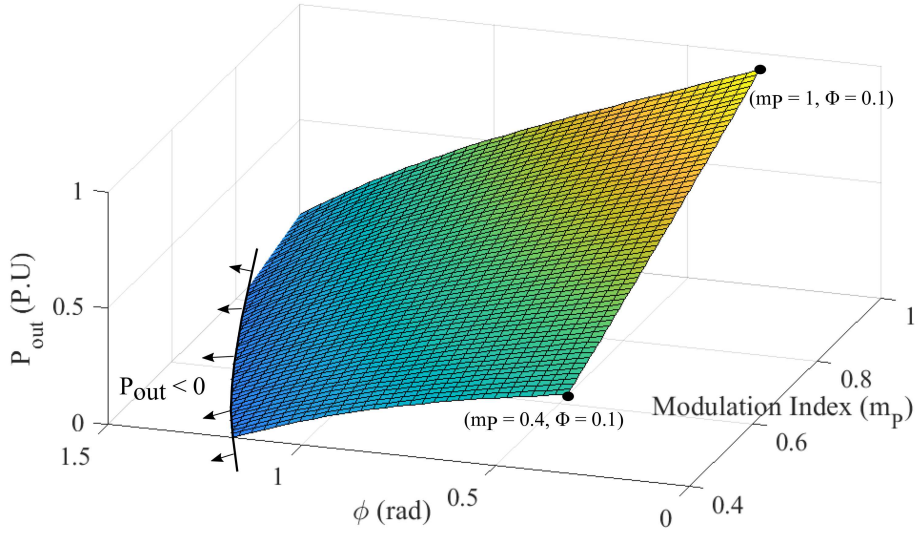
As shown in Fig. 6.10, the soft switching zone for DPS-1 and DPS-3 are plotted based on the inequalities. Therefore, the composite modulation utilizing DPS-1 and 3 is the overlapped area of the two soft switching zones as shown. It is clear from the figure that the modulation index used, has a significant impact on the ability to achieve soft switching. For a proposed system with parameters given in Table - 6.2, the soft switching zone is enclosed by coordinates - $\{0, 1.57\}$, $\{0.3, 0\}$, $\{1, 1.1\}$, $\{1, 3.14\}$, $\{0.2, 3.14\}$. Thus, it is generally concluded that for $m_p \geq 0.3$ and $\phi \geq \frac{\pi}{2}$ yields soft switching for the composite modulation. However, in case when $\phi < \frac{\pi}{2}$, soft switching is partially lost.

Note that the area near low ϕ and m_P has no soft switching capability. During a regular SPWM based modulation, with low output voltage/input bridge conduction angle, the modulation enters

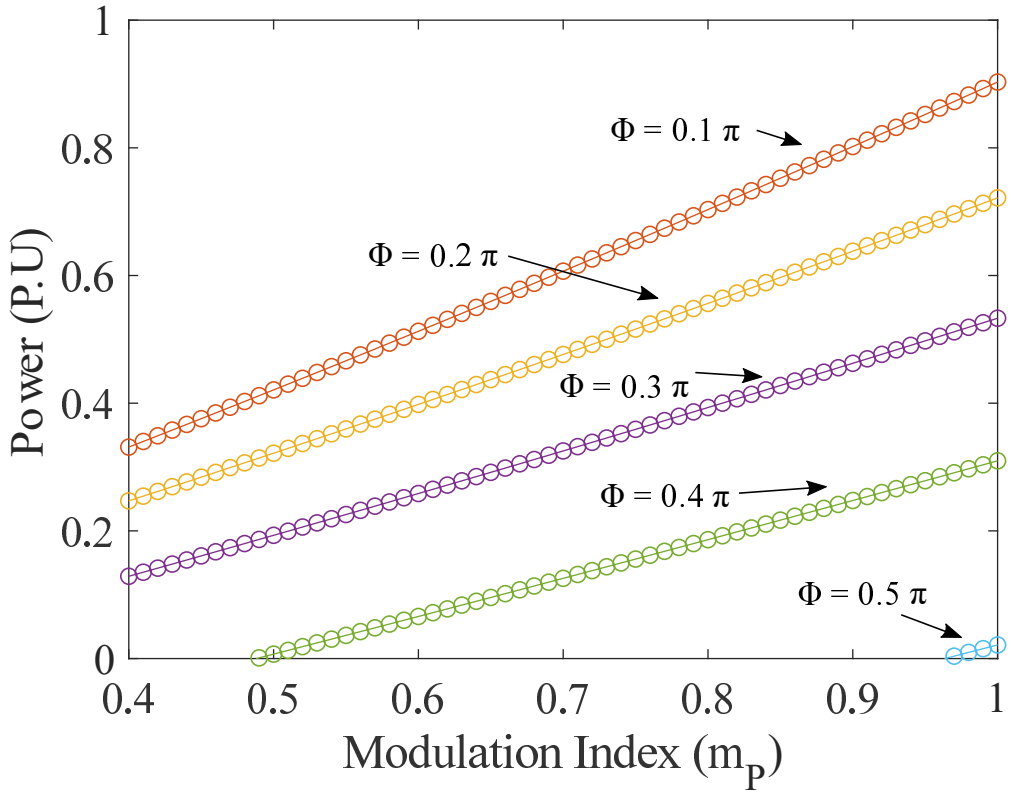
this area and goes through hard switching. This can be easily prevented by creating a "dead zone", in which δ_1 is kept constant at a sufficiently high positive value. This allows the modulation to stop at the boundary of the overlapping zone, and maintain soft switching. The output voltage harmonic distortion has no significant impact with proper output filtering.

6.2.2 Power flow range

As discussed previously, power flow between port-1 to port-3 (mode - M13) and between port-2 to port-3 (mode - M23) is based on the DAB principle. Power flow between port-1 and port-2 (mode- M21) is based on the parallel boost converter. Power flow can potentially be controlled by duty ratio variation. However, since the power switches are operated close to 50% duty ratio, this method doesn't apply. Alternatively, the required frequency modulation can be used to regulate the power in M21. In Fig.6.11, the plot shows the power flow range in per units (P.U), based on variation of the phase shift (ϕ) and modulation index (m_P) of the SPWM.



(a) Power flow plot in 3D space -$\{m_P, \phi, P_{out}\}$



(b) Projection of the power flow plot in 2D space - $\{m_P, P_{out}\}$

Figure 6.11: Power flow plots for varying modulation index and phase shift

From Fig. 6.11 it can be seen that the power flow can be regulated by varying the modulation index m_p. This forms the basis of power flow control for the proposed converter. It is also noted that, $\phi << \frac{\pi}{2}$ yields wider power flow range and ϕ close to $\frac{\pi}{2}$ yields a very limited positive power flow range. Variation of the modulation index takes the converter to negative (port-3 to port-1) quadrant. Combining the soft switching criterion discussed previously, it appears that for a wide power flow range, part of the soft switching must be sacrificed. However as discussed before, a dead zone for the SPWM can be applied when the instantaneous AC output voltage is very low (in other words δ_1 is close to zero), which prevents hard switching.

6.3 Design consideration

The proposed three port converter has been developed as an interface module between PV, battery energy storage and AC output load. Fig. 6.12 demonstrates such a system architecture using the proposed TPC.

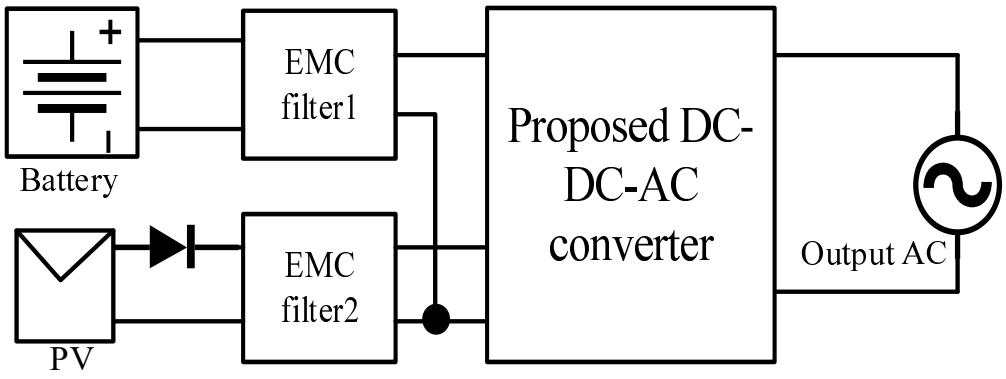


Figure 6.12: System architecture of the proposed TPC in a PV-battery system integration

The proposed system specification is given in Table - 6.2.

Table 6.2: System specifications

Items	Specifications
Nominal PV voltage (V_2)	24V
Nominal battery voltage (V_1)	48V
Output AC Voltage (V_3)	110V (rms)
Transformer ratio (n)	5
Power (P_o)	200W
Auxiliary inductance (L_1)	Transformer coupled, negligible
Auxiliary inductance (L_2)	120 μH
Boost inductance (L_3, L_4)	50 μH, 50 μH
Switching frequency (f_{sw})	$50kHz$
Port-2 Capacitance (C_1)	100 μF
Half bridge Capacitance (C_2, C_3)	1 μF, 1 μF
Active devices ($S_1 - S_8$)	MOSFETs

As the duty ratio of the primary side switches are kept constant at 50 % (without considering the small dead time of about $\approx 100nS$ required for soft transition of switches), the port-1 (Battery port) and port-2 (PV port) voltages should be related by the boost converter gain expression. Hence, the nominal voltages are selected as 24V and 48V for PV and battery port respectively. Selection of the auxiliary inductor value largely depends on the power flow range and soft switching requirement as described before. For a 200W converter, with a peak output AC voltage of 155VAC, the inductance value can be calculated from (4). It is noted that the inductance value calculated is referred to transformer primary. Since the placement of the inductor is chosen to be on the secondary side so that the inductor winding size is reduced, the inductor value should be reflected to the secondary by multiplying with square of the transformer turns ratio, which is approximately $140\mu H$. The

actual inductor value is less than that when the conversion losses and non-idealities are taken into account, thus the chosen inductor value is $120\mu H$. As discussed previously to accommodate the wide power flow range of a PV battery system, a lower value of ϕ is typically chosen. Selection of the half bridge capacitor value impacts the output AC wave shape. For a bigger capacitance, significant energy is stored in them, causing a small phase lead of the current to the reference SPWM voltage. The boost inductor (L_3, L_4) design follows the discussion on M21 power flow mode. Typically a frequency modulation is applied in order to achieve ZVS for the M21 mode. The inductor design is dependent on the frequency modulation capability of the proposed converter prototype.

6.3.1 Ripple port for power decoupling

Similar to all single stage AC link inverters, the output power decoupling is achieved by using energy storage devices. As explained in [20], the power decoupling capacitor is placed on the DC side in this topology. Since the proposed converter is capable of power flow in both modes - M13 and M23, both port-1 and port-2 need a decoupling capacitor to ensure power decoupling in either M13 or M23 mode. This increases the cost and reliability concern significantly. However, when a reverse power blocking diode is used in series with the PV port, port-1 inherently becomes the ripple port regardless if there is any active power flow between port-1 and port-3. The introduction of the diode doesn't allow any negative current to flow from the PV port, therefore the boost inductor currents are always positive throughout the switching cycle. Which implies, the instantaneous boost inductor current - $i_{L,3}(t), i_{L,4}(t) \geq 0$. Therefore, when a small low pass filter (to filter switching frequency oscillations) is placed at the PV input, the average input current is positive and may only partially contributes to the decoupling. If a large capacitor is placed at the battery port, regardless of whether a battery is actually connected or not, provides the required decoupling power. Thus the PV port supplies approximately P_{out} and the battery port, equipped with decoupling capacitor provides $P_{out}cos(2\omega_L t)$ portion of the AC power, where t denotes time.

The capacitance value can be calculated as described in [20], [21] and [22].

$$C_1 = \frac{P_{out}}{\omega_L V_1 \Delta V_1} \tag{6.19}$$

where ΔV_1 is the ripple voltage across C_1. Thus for a design with 1V ripple, the proposed capacitance value is calculated to be approximately $13mF$. The performance of the ripple port is demonstrated using both a 1V and 2V ripple, which requires $13mF$ and $6.5mF$ capacitance. Based on the decoupling capacitor used in the battery port, the PV port may or may not contribute to the ripple power.

6.4 Experimental results

As discussed in the Section - 6.3, the proposed converter specifications are chosen based on the performance metrics given in Table - 6.2. The waveforms for the power flow mode M13 is as shown in Fig. 6.13.

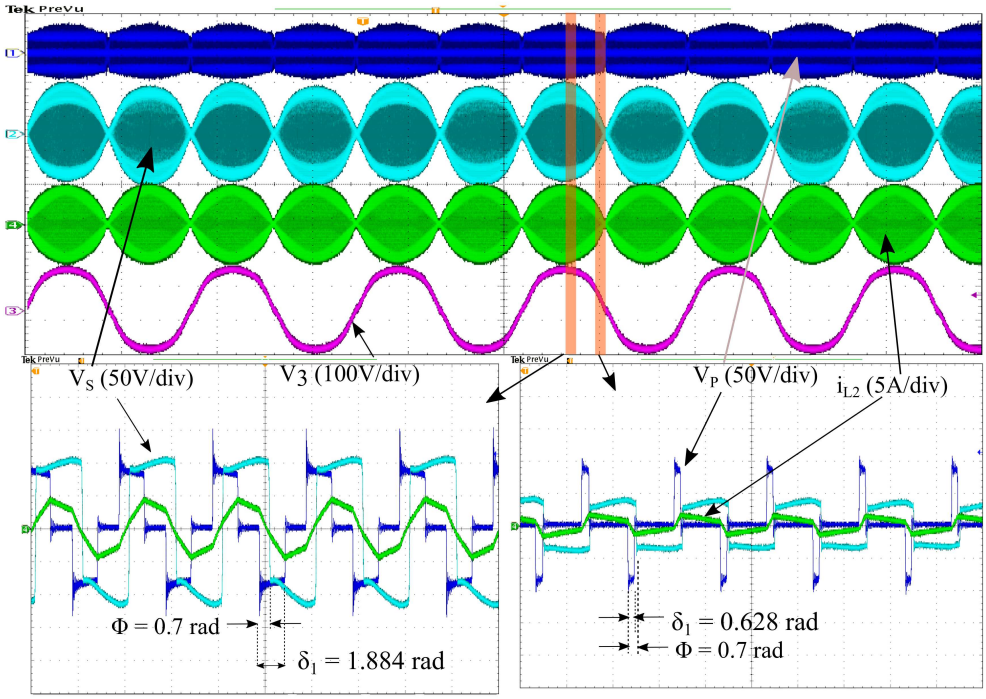


Figure 6.13: Key waveforms for power flow mode M13 with transformer primary voltage (V_p), secondary voltage(V_S) and secondary current ($\frac{i_{L,1}}{n}$)

Similarly, for M23 mode, the key waveforms are shown in Fig. 6.14. The key difference between the M13 and M23 mode is that the voltage source is connected to port-1 and port-2 respectively, and the remaining port has no active voltage supply.

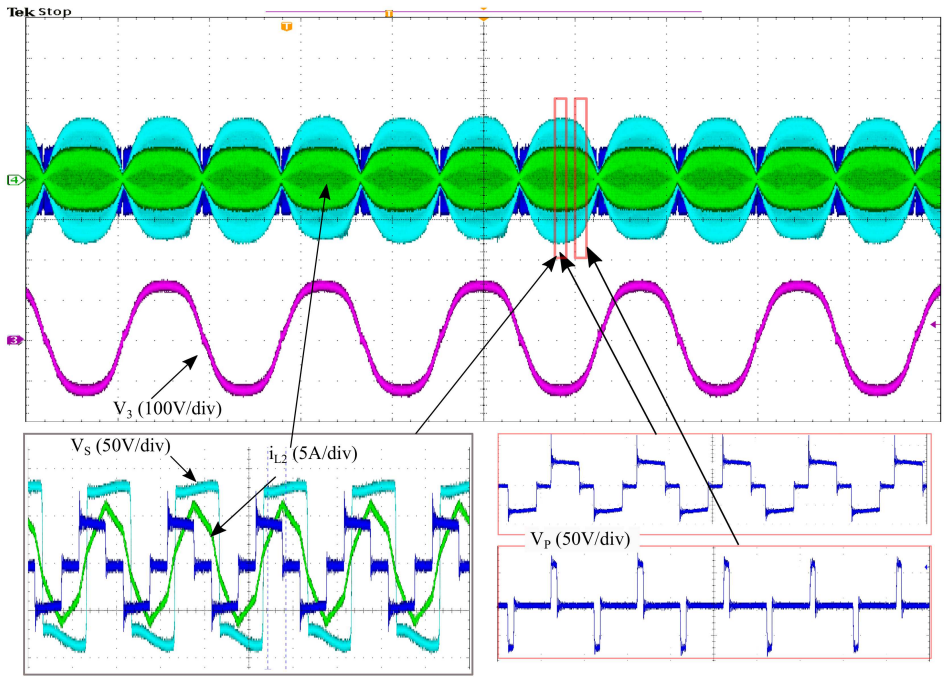


Figure 6.14: Key waveforms for power flow mode M23 with transformer primary voltage (V_p), secondary voltage(V_S) and secondary current ($\frac{i_{L,1}}{n}$)

Thus both M13 and M23 modes are experimentally verified. For power flow between port-1 and port-2(mode - M21) is also validated experimentally in Fig. 6.15 and Fig. 6.16. The modulation using usual SPWM based modulation (interleaved boost) is demonstrated in Fig. 6.15 and using modulation with $\delta_1 = 0$ (parallel boost) is shown in Fig. 6.16.

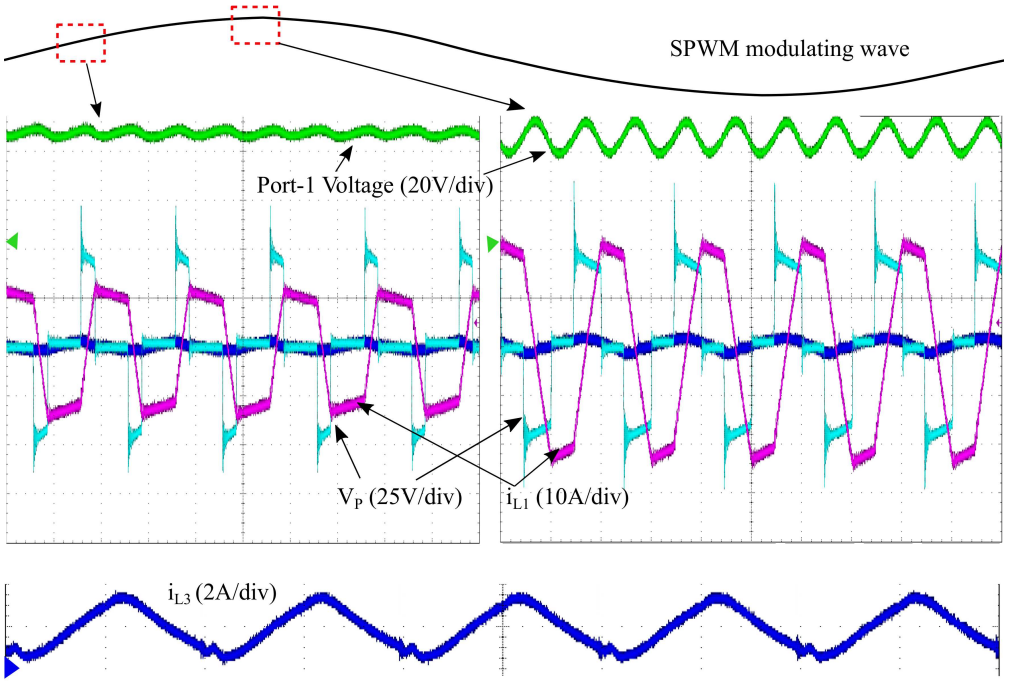


Figure 6.15: Key waveforms for power flow mode M21 with transformer primary voltage (V_p), primary current ($i_{L,1}$), port-1 voltage (V_1) during the interleaved boost modulation

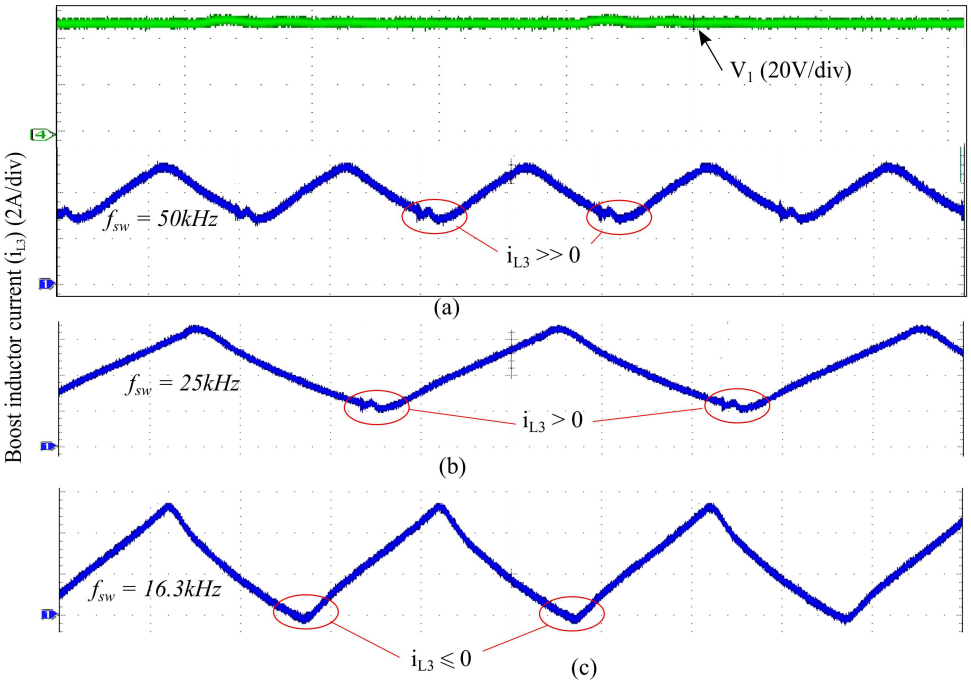


Figure 6.16: Key waveforms for power flow mode M21 with transformer boost inductor current ($i_{L,3}$) and port-1 voltage (V_1) during the parallel boost modulation - (a) 50 kHz Switching frequency, (b) 25 kHz Switching frequency and (c) 16.3 kHz switching frequency

As seen from the figures, for the parallel boost modulation, the switching frequency is varied from $50kHz$ to $16.3kHz$ until the CCM modulation is achieved. Thus, the parallel boost mode achieves ZVS and provides better efficiency (peak efficiency = 97 %) as compared to the interleaved boost mode which achieves around 87% average efficiency in the experimental verification. The interleaved boost modulation also generated much higher peak current and hence overall conduction loss is higher. Therefore, it is generally not the preferred modulation for standalone M21 power flow mode.

As discussed previously, the input current ripple due to power decoupling is a major disadvantage. The effect of decoupling on the port-2 current ripple is demonstrated in Fig. 6.17. The 120Hz current ripple can be mitigated naturally when the port-1 is supplied through a reverse blocking power diode, and the input current ripple shifts to the port -1 decoupling capacitor, as seen in Fig.

6.18

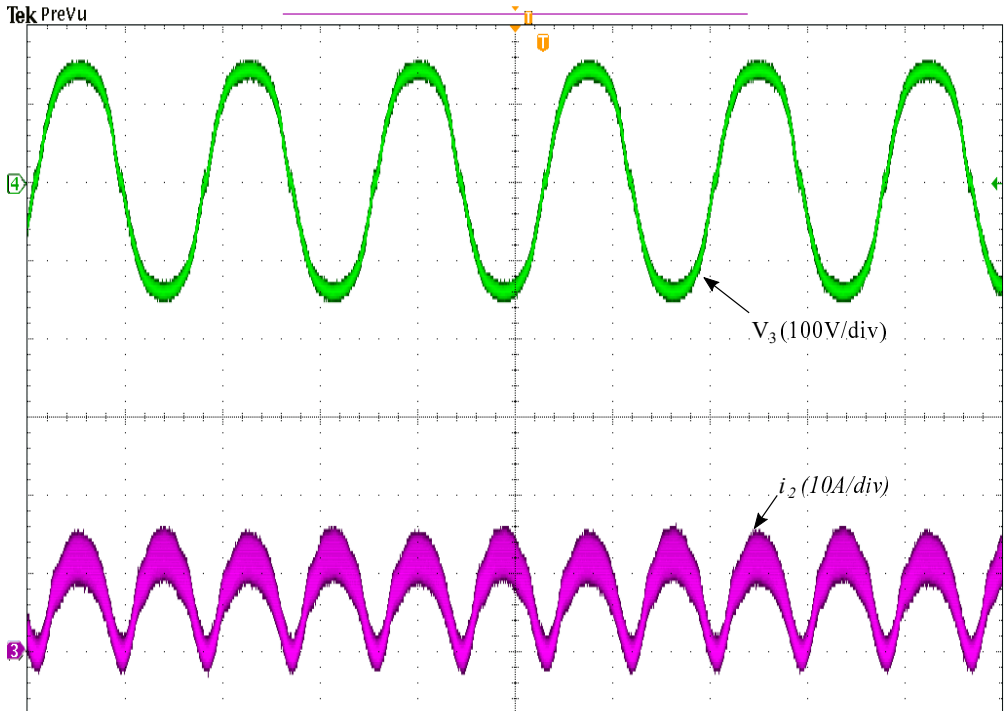


Figure 6.17: Illustration of output AC sinusoidal voltage (V_3) and the Port-2 low frequency input current (i_2) ripple

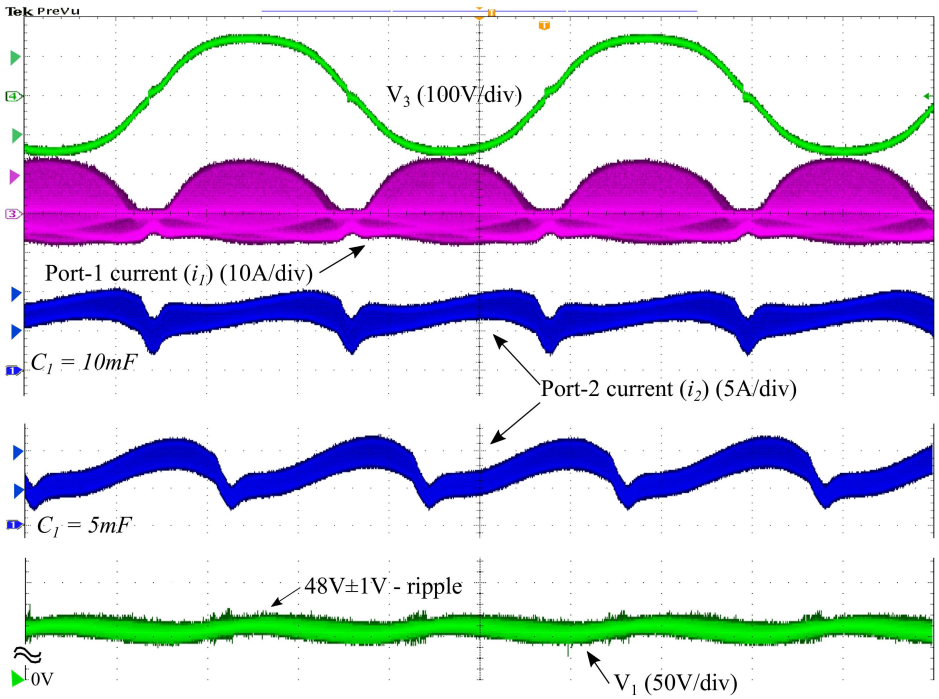


Figure 6.18: Illustration of output AC sinusoidal voltage (V_3) and reduced/mitigated Port-2 low frequency input current (i_2) ripple and vanishingly low port-2 voltage ripple

The decoupling capacitor calculated in Section - 6.3.1 is about $13mF$. Since it is not an available standard value capacitor, a $10mF$ is used instead. Additionally, a $5mF$ is used to demonstrate the intermediate stage when the decoupling is partially being provided by port-1 and partially by port-2, hence the current waveform for i_2 is not completely free of 120Hz ripple. Note that a small low pass filter was used to remove the high frequency ripple, and its value was not sufficient to remove the low frequency dip that appears during the zero crossing of the output sine wave. A small increase in the low pass filter can eliminate this.

Overall output voltage and current has good total harmonic distortion (THD) as demonstrated by the Fig. 6.19.

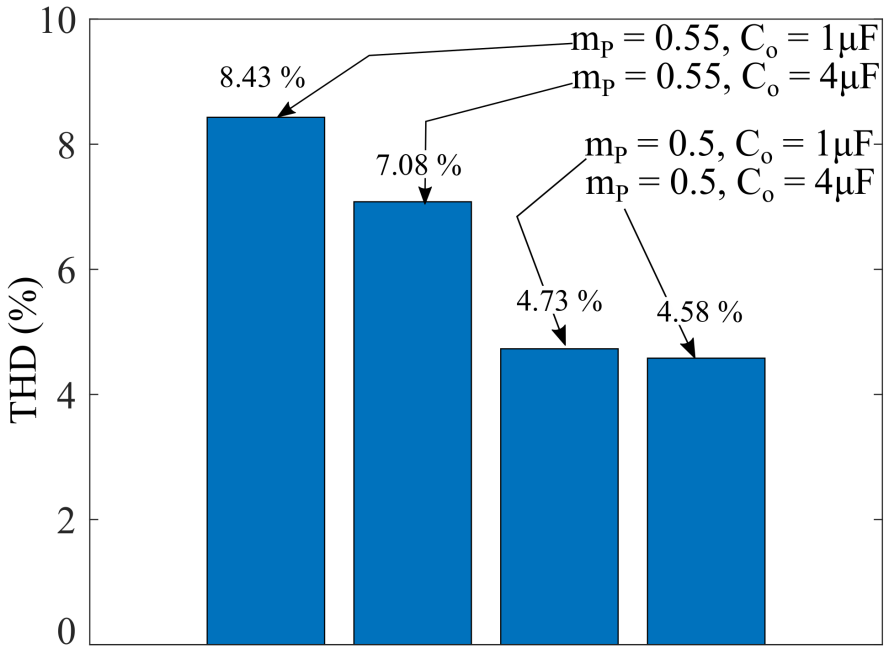


Figure 6.19: Total harmonic distortion of the proposed converter for different output filter capacitance and modulation index

In this figure, the overall THD improves when a larger output filter capacitance is used. Also, the THD can be improved by varying the modulation index as noted in [1]. Four different measurements are shown here where the output filter capacitor (C_O) is changed from $1\mu F$ to $4\mu F$ and the modulation index m_P in changed from 0.55 to 0.5. It was noted that for $m_P = 0.5$ and $C_O = 4\mu F$ provides $\leq 5\%$ THD and it can also be improved further by increasing the output filter size and reducing the modulation index further.

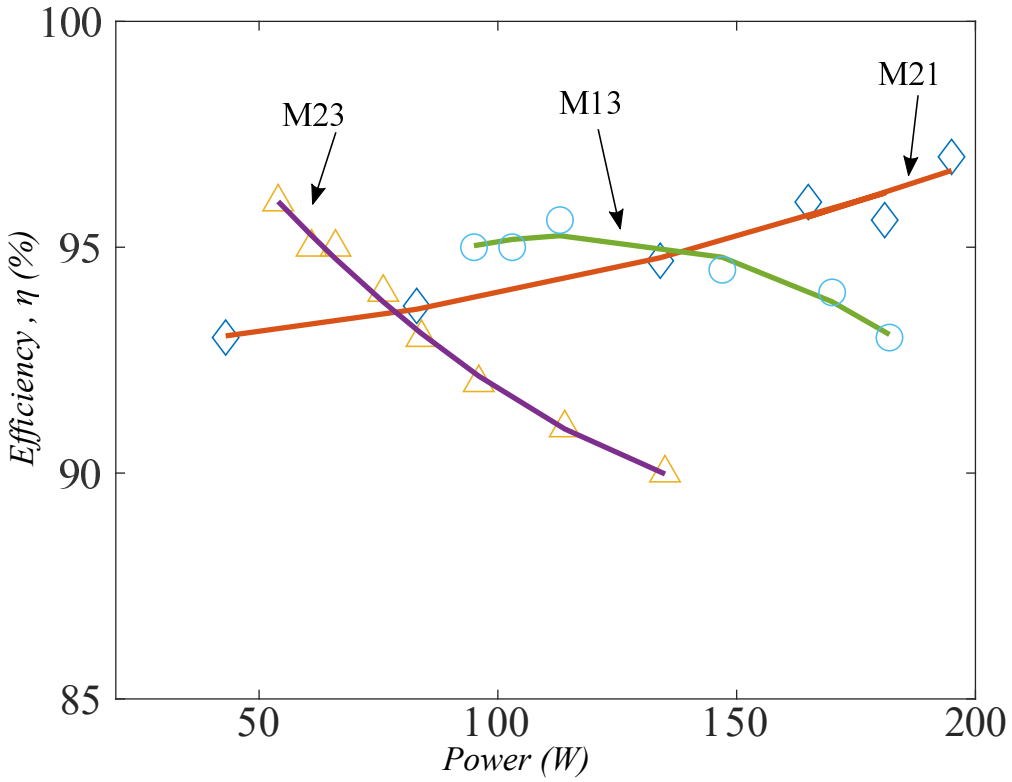


Figure 6.20: Efficiency of the proposed TPC in M21, M13 and M23 power flow modes

The efficiency of the three power flow modes M21, M13 and M23 is shown in Fig. 6.20. Naturally, M21 yields highest efficiency of the all modes as it is essentially a nonisolated boost conversion. With the pulse frequency modulation, ZVS is ensured for all power levels and hence achieves a peak efficiency of 97 %. M13 also achieves high efficiency with a peak of around 96 % around half load. However, since the switches turn on at zero voltage and turn off loss is negligible, the major contributor to the loss is the conduction loss across the active switches. Hence with increased power flow, efficiency decreases. This is true for mode M23 as well. Additionally, since the input voltage is almost half compared to mode M13, the peak efficiency of around same value, occurs at low load and gradually reduces from that point onward. For this reason, the port-2 is rated lower compared to port-1 so that over complete power flow range, a consistent efficiency is achieved for multiple different power flow direction.

6.5 Summary

In this chapter, a novel three port power converter is proposed which interfaced two DC port and an AC output port. The typical three port converter converts power between the two DC ports, whereas in this work a DC-AC stage has been integrated and a single stage DC-DC-AC converter is constructed. The converter is based on a dual active bridge topology, where the secondary bridge is a half bridge type architecture with four quadrant switches used as active bridge. During the positive AC line cycle, the top switches of the secondary half bridge are kept on. During negative line cycle, the bottom switches are kept on. This allows DAB based modulations (in this case DPS) to be applied, which preserved the soft switching capability and other advantages of the DAB. Power flow between the DC ports to the AC port is achieved using this sinusoidal modulation. This places a very minimal computational burden on the controller and allows it to update every line cycle. This is a significant improvement for low power microinverter control. Power flow between the two DC ports is achieved using the interleaved boost converter. It is shown that the modulation used for DC-AC conversion can be used for DC-DC conversion as well and still achieve stable power flow. However, the efficiency degrades. Thus a new parallel boost modulation is proposed which uses critical conduction mode for DC-DC conversion and is able to achieve higher efficiency. The proposed converter achieves low harmonic distortion and improved efficiency for all power flow modes, which makes it a good candidate for a PV battery system integration in both a grid tied or standalone setting.

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CHAPTER 7: SMALL SIGNAL MODELING AND CONTROLLER DESIGN OF IMPROVED TPC

As discussed in the Chapter 6, the proposed improved TPC follows the two different DPS modes as demonstrated. The overall low frequency modulation constitutes the DPS-1 and DPS-3 modulation. Therefore, it is important to understand the dynamic model for the fundamental dual phase shift modulations before designing a closed loop controller for the improved TPC. With an accurate dynamic model, the AC output voltage can be controlled in every high frequency switching cycle since each of them are DPS. Alternatively, the peak switching cycle may be controlled once every line cycle to maintain peak voltage at a desired value.

7.1 Review of average model for DAB

The traditional averaging techniques used in DCDC converters shown in [1], utilize the duty ratio of the PWM switches and then averages the parameters by multiplying them by the duty ratios and then adding them together. A control oriented simplistic modelling approach has been introduced in [5] and [6]. Other detailed models include works in [7] - [9]. Traditional method given in [1] is proven to be a very intuitive and powerful tool for modeling almost all DCDC converters whose state variables are inherently DC in nature. However, converters whose state variables are AC, cannot be modeled in this way as the DC average of such parameters yields zero. So the model will not be influenced of any AC terms. This is particularly encountered in bridge type resonant power converters where the resonant tank current is often AC (having zero average). Dynamic model of DAB also consists of AC state variable terms. The transformer current for DAB is AC so no DC average exists. Therefore, traditional averaging techniques cannot be used. In [3], the authors proposed a generalized averaged modeling (GAM) technique to address challenges like this. The essence of the proposed technique is to transform the state variables of the dynamical

system, into its fourier transforms. This includes, not only the state variables but the switching functions as well. In [2], authors proposed a generalized average model for dual active bridge converters following the same principles of GAM technique, using SPS modulation.

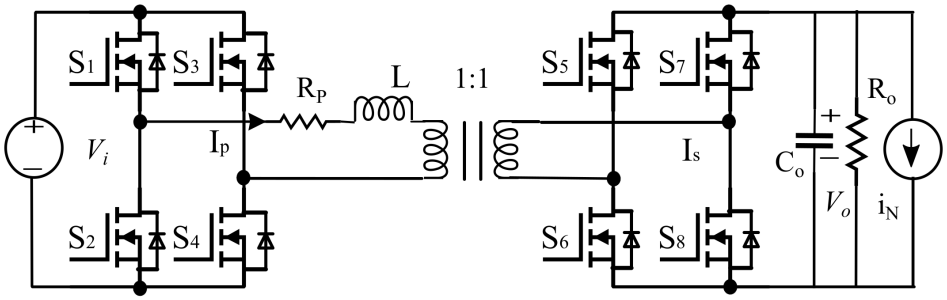

Figure 7.1: Ideal circuit model of the DAB

In Fig. 7.1, the equivalent circuit of the DAB converter is shown, with similar parameters as discussed in the previous sections. The only additional parameters in this circuit are that the output port is terminated with a bulk capacitor of value C_O and a resistor R_O in parallel. For simplification, any load applied to the circuit is modeled as a current source i_N. Naturally, if a load resistor R is applied at the output, that implies, $i_N = \frac{V_O}{R}$, where V_O is the output DC voltage. Similarly, the input DC voltage source amplitude is V_i.

The dynamical equations for the system can be written in time domain as:

$$\frac{di_p(\tau)}{d\tau} = -\frac{R_P}{L} i_P(\tau) + \frac{s_1(\tau)}{L} v_i(\tau) - \frac{s_2(\tau)}{L} v_o(\tau) \tag{7.1}$$

$$\frac{dv_o(\tau)}{d\tau} = -\frac{1}{R_o C_o} v_o(\tau) + \frac{s_2(\tau)}{C_o} i_p(\tau) - \frac{I_N}{C_o} \tag{7.2}$$

where, s_1 and s_2 are the switching functions of the primary and secondary bridge. They are defined

as:

$$s_1 = \begin{cases} 1, & 0 \leq \tau \leq \frac{\delta_1 T}{2} \\ 0, & \frac{\delta_1 T}{2} \leq \tau \leq \frac{T}{2} \\ -1, & \frac{T}{2} \leq \tau \leq \frac{\delta_1 T}{2} + \frac{T}{2} \\ 0, & \frac{\delta_1 T}{2} + \frac{T}{2} \leq \tau \leq T \end{cases} \tag{7.3}$$

$$s_2 = \begin{cases} 1, & \frac{\phi T}{2} \leq \tau \leq \frac{\phi T}{2} + \frac{T}{2} \\ -1, & 0 \leq \tau \leq \frac{\phi T}{2} \\ -1, & \frac{\phi T}{2} + \frac{T}{2} \leq \tau \leq T \end{cases} \tag{7.4}$$

Using definitions in [2], [3], fourier transforms for the parameters and their product can be deduced. The fourier transform of the switching functions s_1 and s_2 can be represented as:

$$\begin{aligned} &< s_{10} >=< s_{20} >= 0 \\ &< s_1 >_{1R} = \frac{sin(\delta_1 \pi)}{\pi} \\ &< s_1 >_{1I} = \frac{-1 + cos(\delta_1 \pi)}{\pi} \\ &< s_2 >_{1R} = \frac{-2sin(\phi \pi)}{\pi} \\ &< s_2 >_{1I} = \frac{-2cos(\phi \pi)}{\pi} \end{aligned} \tag{7.5}$$

Based on equations 7.1 - 7.5, the system matrix can be derived as follows:

$$\underbrace{\frac{d}{dt}\begin{bmatrix} v_o \\ i_{P,R} \\ i_{P,I} \end{bmatrix}}_{X} = \underbrace{\begin{bmatrix} -\frac{1}{R_o C_o} & -\frac{4sin(\phi\pi)}{\pi C_o} & -\frac{4cos(\phi\pi)}{\pi C_o} \\ \frac{2sin(\phi\pi)}{\pi L} & -\frac{R_P}{L} & \omega_s \\ \frac{2cos(\phi\pi)}{\pi L} & \omega_s & -\frac{R_P}{L} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} v_o \\ i_{P,R} \\ i_{P,I} \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} 0 & -\frac{1}{C_o} \\ \frac{sin(\delta_1\pi)}{\pi L} & 0 \\ \frac{1-cos(\delta_1\pi)}{\pi L} & 0 \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} v_i \\ i_N \end{bmatrix}}_{U} \tag{7.6}$$

7.2 Small signal model with control variable - δ_1

Contrary to the GAM approach taken up in [2], and [4], the controlling variable is selected to be δ_1 instead of ϕ. This is because the conduction angle of the primary bridge - δ_1 can be used to regulate the output power flow of the improved TPC as seen in section 6. Since the primary purpose of the improved TPC is for standalone mode operation, a resistive load is expected to be applied at the output port. The output voltage can be regulated by controlling the power using δ_1 as a control variable. ϕ is assumed to be either constant or slowly varying. Therefore, during a switching cycle, the system matrix A can be considered to be a constant, and only the input matrix B is time varying.

Therefore, small signal perturbation can be applied as follows:

$$\begin{aligned} \Delta_1 + \Delta\delta_1 &= \delta_1 \\ V_o + \Delta v_o &= v_o \\ I_{P,R} + \Delta i_{P,R} &= i_{P,R} \\ I_{P,I} + \Delta i_{P,I} &= i_{P,I} \end{aligned} \tag{7.7}$$

Where, Δ_1 is the steady state value of the primary bridge conduction angle δ_1, and $\Delta\delta_1$ is the small signal perturbation. Similarly, V_o, $I_{P,R}$ and $I_{P,I}$ are the steady state output voltage and real and imaginary component of the transformer current and Δv_o, $\Delta i_{P,R}$ and $\Delta i_{P,I}$ are the small signal perturbation of the same parameters respectively.

Thus applying these perturbations and approximating higher order nonlinear terms, the small signal

model can be represented as following:

$$\frac{d}{dt}\underbrace{\begin{bmatrix}\Delta v_o\\ \Delta i_{P,R}\\ \Delta i_{P,I}\end{bmatrix}}_{X^*} = \underbrace{\begin{bmatrix}-\frac{1}{R_oC_o} & -\frac{4sin(\phi\pi)}{\pi C_o} & -\frac{4cos(\phi\pi)}{\pi C_o}\\ \frac{2sin(\phi\pi)}{\pi L} & -\frac{R_P}{L} & \omega_s\\ \frac{2cos(\phi\pi)}{\pi L} & \omega_s & -\frac{R_P}{L}\end{bmatrix}}_{A^*}\underbrace{\begin{bmatrix}\Delta v_o\\ \Delta i_{P,R}\\ \Delta i_{P,I}\end{bmatrix}}_{X^*} + \underbrace{\begin{bmatrix}0\\ \frac{v_i cos(\Delta_1\pi)}{L}\\ \frac{v_i sin(\Delta_1\pi)}{L}\end{bmatrix}}_{B^*}\Delta\delta_1 \tag{7.8}$$

Assuming ideal components and ignoring the nonidealities of the DAB circuit, the transfer function for the plant (DAB) can be represented by the following equation:

$$G_P(s) = C^*(sI - A^*)^{-1}B^* \tag{7.9}$$

where C is the output matrix, $C = [1,\ 0,\ 0]^T$.

In Fig. 7.2, an open loop transfer function (OLTF) bode diagram is shown for a DPS mode operation with constant $\phi = \frac{\pi}{2}$ and a steady state $\delta_1 = \frac{8\pi}{10}$.

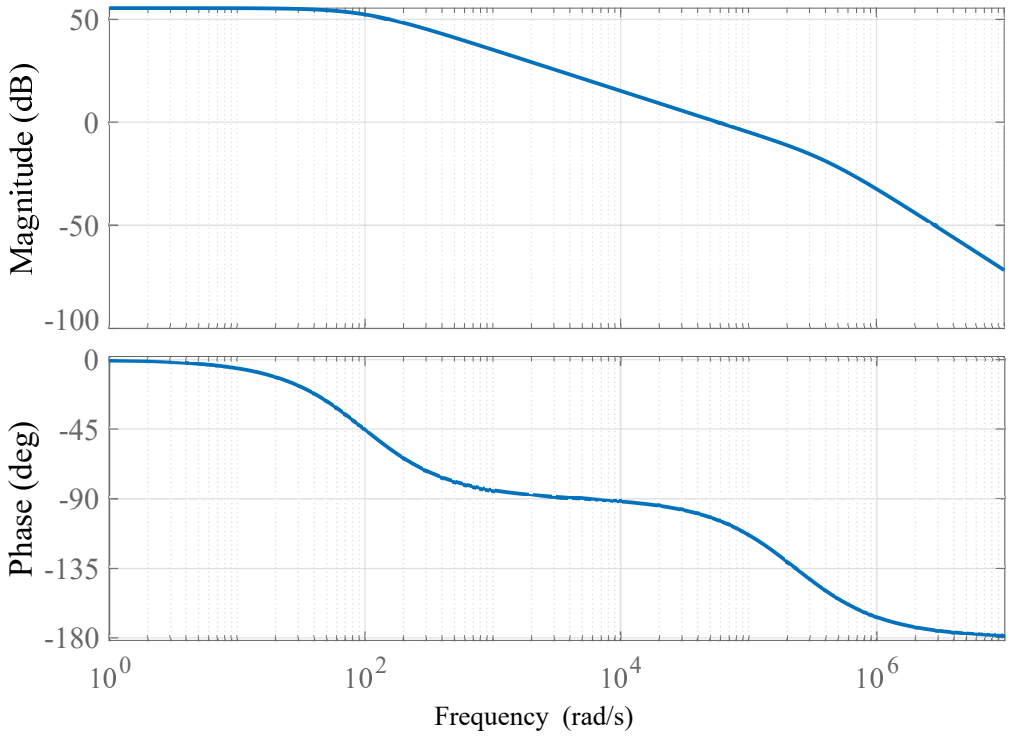

Figure 7.2: Frequency response of the open loop transfer function (OLTF) of the DAB operating under DPS with constant $\phi = 0.5\pi$

As seen from the figure, the OLTF has a cut off frequency of about 1.3kHz for a given system operating at switching frequency of 50kHz. Detailed system specification for the model is given in the Table-7.1.

Table 7.1: System specifications

Items	Specifications
Nominal input voltage (V_i)	50V
Output Voltage (V_2)	150V
Transformer ratio (n)	1
Power (P_o)	200W
Auxiliary inductance (L)	$10\mu F$
Primary winding resistance (R_P)	0.1 Ω
Output resistance (R_O)	36 Ω
Output capacitance (C_O)	200 μF
Switching frequency (f_{sw})	$50kHz$
Active devices	Ideal Switches
Proportional gain (k_P)	10
Integral gain (k_I)	0.5

7.3 Feedback controller design with PI term

Traditionally, a PI controller has been the single most popular choice as a closed loop compensator for DC-DC converter applications. The PI controller is both robust in nature and provides very good reference tracking for a well designed controller. One of the disadvantages of a PI based controller is that the percentage overshoot tends to increase when a fast integrator is used to achieve faster response time. Thus, the design of PI controller becomes a trade off between key performance metrics to suits a given application.

For the given system of DAB operating under DPS scheme, an appropriate PI controller is investigated. In Fig.7.3, a block diagram of the closed loop control system is shown.

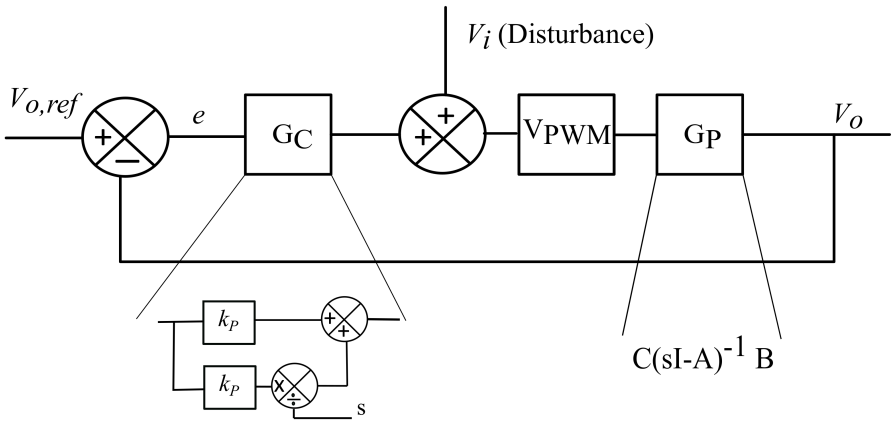

Figure 7.3: Block diagram representing the closed loop architecture of the DAB with output voltage feedback

Here the error signal between the referenced output voltage and the measured output voltage is denoted as e. A disturbance signal is included in the control structure as V_i which is the input voltage to the DAB. V_i is usually a PV or battery voltage for the proposed improved TPC. Naturally, during normal operation, the PV voltage fluctuates about $\pm 3 - 4V$ when operating under maximum power point tracking. This small signal fluctuation can be incorporated into the actual control structure as shown.

As seen from the small signal model of the DAB where δ_1 is the control variable, the disturbance input can be rejected by increasing the loop gain of the proposed structure. Therefore, increasing the proportional gain of the controller improves the disturbance rejection property of the proposed structure. Based on the controller gains given in the Table-7.1, the loop gain bode plot and finally overall closed loop transfer function plots are given in Fig.7.4 and Fig.7.5 respectively.

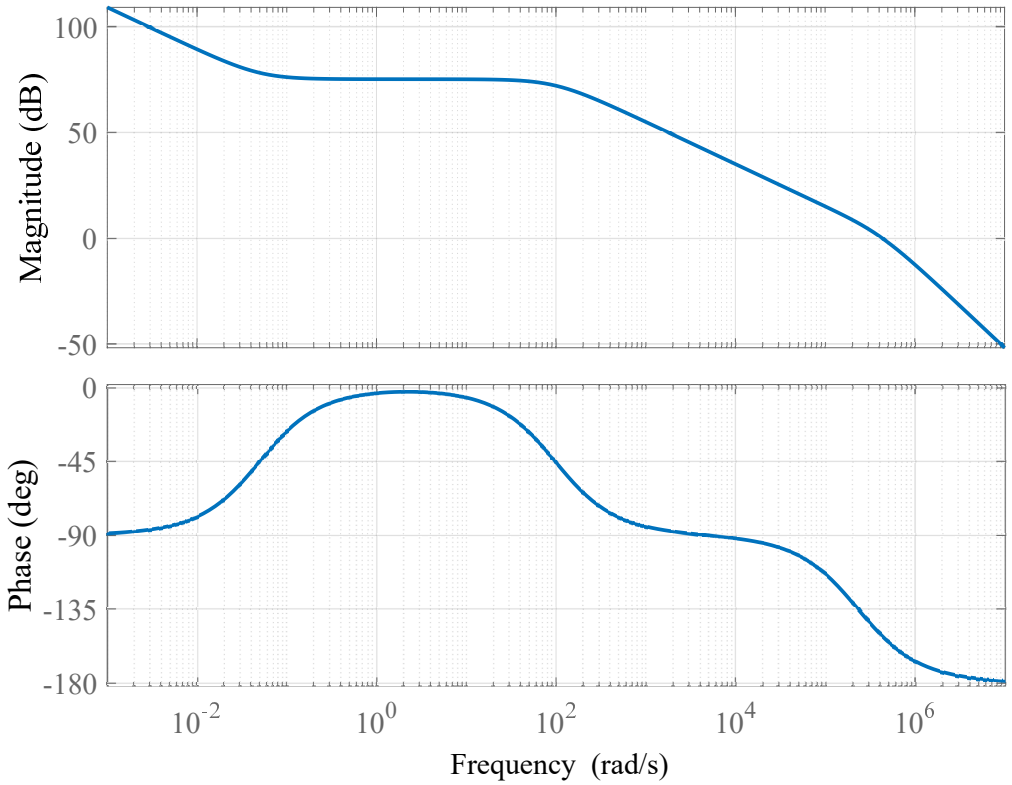

Figure 7.4: Frequency response of the loop gain of the DAB operating under DPS with constant $\phi = 0.5\pi$

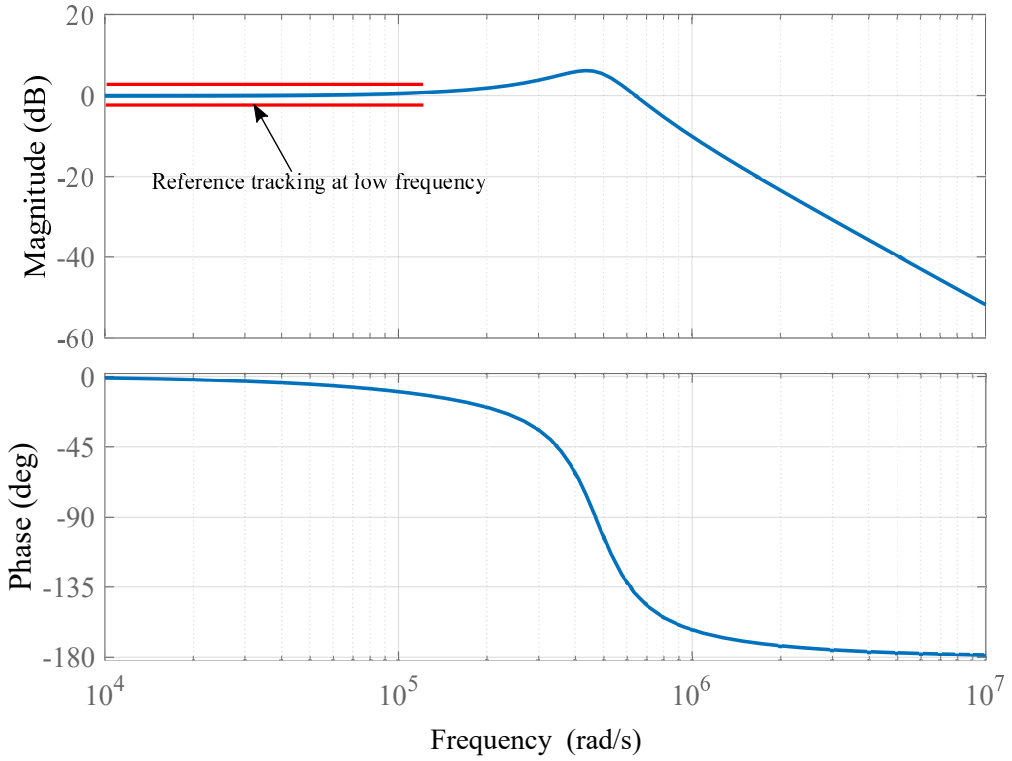

Figure 7.5: Frequency response of the closed loop transfer function (CLTF) of the DAB operating under DPS with constant $\phi = 0.5\pi$

As seen from Fig.7.4, after applying the PI controller, the loop bandwidth improves 10 fold. This improved bandwidth comfortably includes the $120Hz$ double line frequency component with a higher gain (75dB) compared to open loop case (50dB). Therefore, the addition of the PI controller provides better tracking for the 120Hz disturbance. Additional increase of the proportional gain improves the tracking even further and rejects other disturbances, as discussed previously.

7.4 Application to DAB based DC-AC converter

Proposed closed loop control strategy developed based on DC-DC DAB converter can be applied to the DAB based DC-AC converter directly. This is because the fundamental modulation strategy (DPS) is same for both DC-DC and DC-AC converter. In order to maintain low update rate of

the controller, only the peak voltage of the DC-AC converter can be controlled which ensures that the rms voltage of the output sine wave voltage is controlled assuming a low enough harmonic distortion exists in the output voltage waveform. In that case the rms and peak voltage are relates to each other by the following expression:

$$V_{rms} = V_{peak}/\sqrt{2} \tag{7.10}$$

The half line cycle carrier waveform of the DC-AC converter is repeated here (Fig. 7.6) to emphasize the control sequence of the proposed δ_1 based closed loop controller.

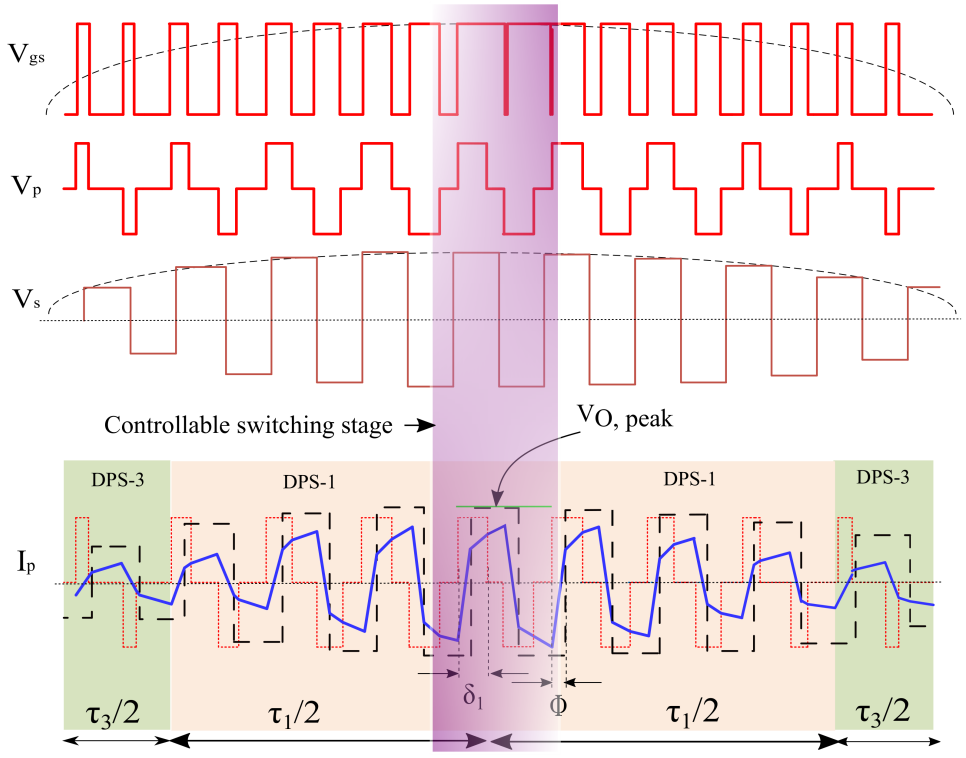

Figure 7.6: Switching and line cycle of "improved TPC" with peak voltage control

As seen from the figure, only the switching cycle during the peak of the voltage sinusoid participates in the closed loop control. The controller speed remains constant and updates at every line cycle. Therefore, no extra burden is placed on the computational engine of the controller. The

output voltage is assumed to be constant during this switching interval as there is no noticeable change in the magnitude of the voltage during the $20\mu S$ switching cycle at the peak of the sine wave.

7.5 Experimental verification

The 200W prototype built for validating the improved TPC is used here for validating the controller design. The system parameters are same as given in Table-7.1. The output voltage is specified as $110V_{rms}$ sinusoidal output.

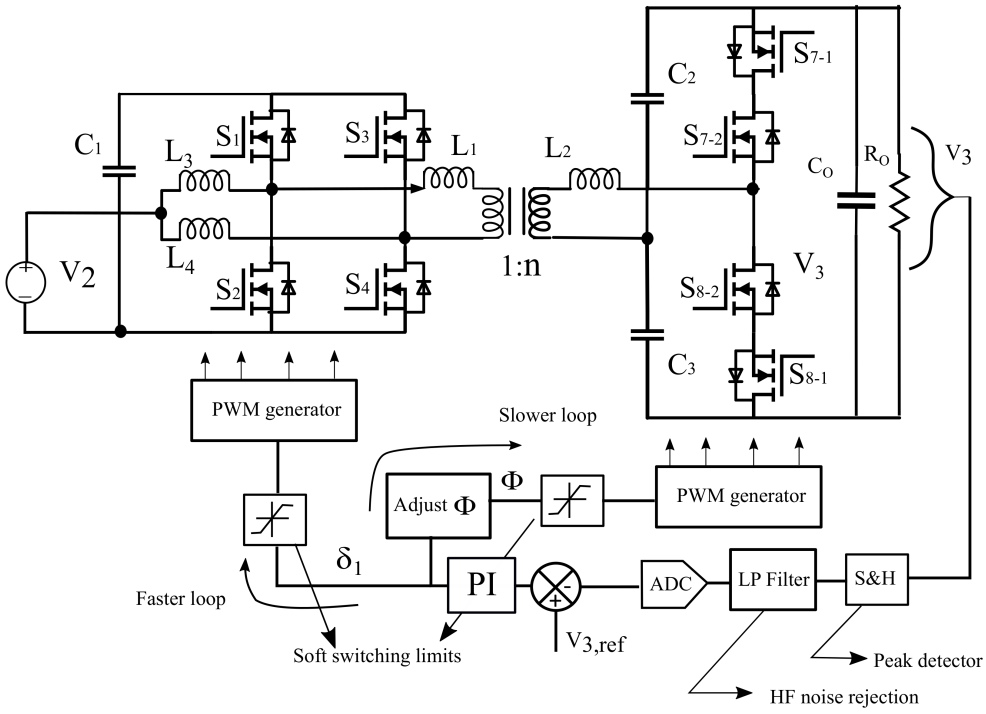

Figure 7.7: Overall control architecture of the "improved TPC"

Fig. 7.7 shows the overall control implementation in hardware. The output AC voltage is first stepped down using a low leakage resistance divider. Then the half-wave rectified signal is con-

verted to DC by applying a large capacitor at its output. Thus, the average of the AC output halfcycle is generated. This DC measurement is directly fed to the internal 12-bit ADC of the controller STM32F334K8 chip. Due to hardware limitation, significant amount of noise is propagated along with the measured value, thus a moving average type digital filter is applied in the controller, and finally the feedback is passed through a digital PI controller to generate the commanded δ_1 for the primary bridge. Note that from Fig. 7.7, there is a slow acting loop to adjust the phase shift ϕ included in the controller diagram. This is because, as seen in Fig. 6.11 in Chapter - 6, the power flow range can be expanded or reduced by varying the phase shift. From the steady state equations given in (5.1)-(5.3), it is noted that the output power is related to the ϕ by following:

$$P_{out} \propto k_1(k_2 - k_3\phi) \tag{7.11}$$

where k_1-k_3 are different functions of δ_1, which can be obtained from (5.1)-(5.3). Since the gain of the "ϕ adjustment" loop is very slow, it is effectively constant for δ_1 variations. This preserves the closed loop controller designed on δ_1 perturbation. Since the peak of the modulating sine wave is being controlled by adjusting δ_1 at the peak of the sine wave, it is effectively adjusting the modulation index of the controller. This is in agreement with the note in Chapter-6 on power flow control using the variable modulation index (m_P).

In Fig.7.8 and Fig.7.9, the output voltage dynamic behavior is presented, with an applied input voltage perturbation of ± 5V. The output voltage responds to the change in input voltage and the closed loop controller brings the output voltage back to the reference value. A relatively low proportional gain is used here since a higher gain reduces the phase margin and degrades overall system performance under transient conditions.

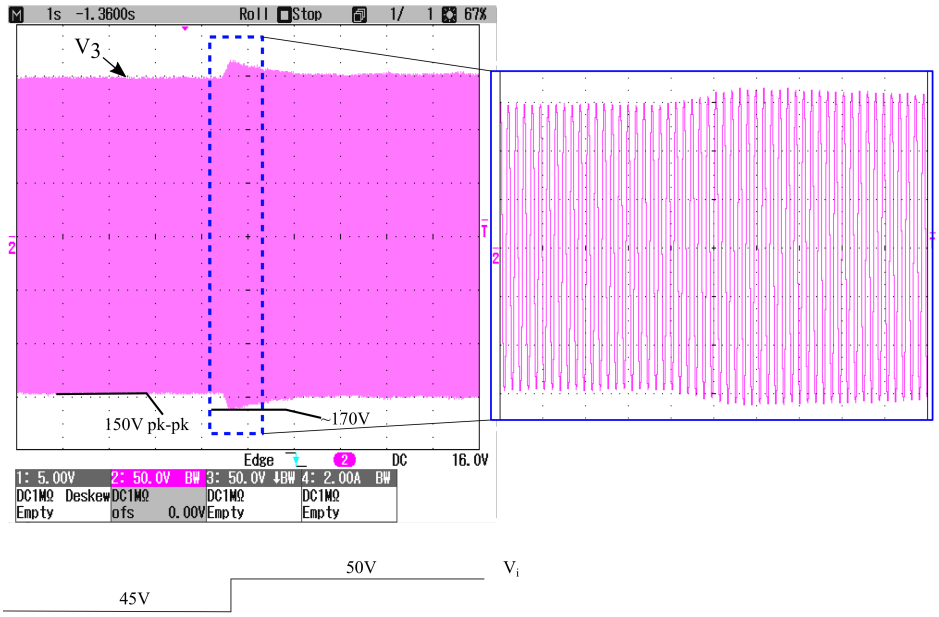

Figure 7.8: Step increase in input voltage and corresponding output voltage response

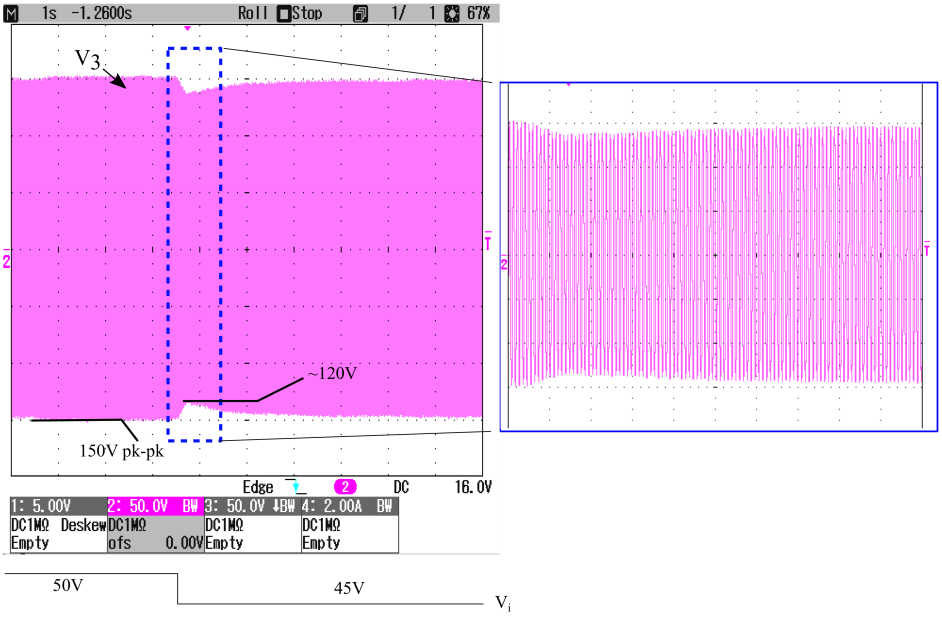

Figure 7.9: Step decrease in input voltage and corresponding output voltage response

It is noted that the conduction angle δ_1 varies between 0.45π to 0.78π for the given perturbation range. This is closely maintained within the broader range of 0.4π to 0.8π which is the soft switching range for the given phase shift angle $\phi = 0.5\pi$.

7.6 Summary

In this work, a closed loop controller has been designed based on the GAM proposed in past literature. Existing methods on GAM only considers the phase shift (ϕ) as a control variable and are not applicable to DPS modulations. In this work, the DAB based DC-AC operated in DPS modes. Here the GAM model is modified here to use δ_1 as a control variable and the phase shift ϕ is kept as a constant or a very slowly varying parameter. The control to output transfer function is derived and a frequency response plot reveals that when the DAB is used as an input to a single phase inverter (Such as the proposed improved TPC topology) a higher tracking gain is required. This cancels out the disturbances introduced by the double line frequency harmonics and input voltage variation due to the MPPT operation of the PV. A PI based controller has been introduced which is shown to improve the loop gain bandwidth, provide excellent reference tracking and provide a good stability margin (phase margin) over the open loop system. The proposed control structure and modified GAM is validated using experimental results. A ± 5V perturbation is provided to the input and the output voltage is observed to track the reference output voltage.

7.7 List of References

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CHAPTER 8: CONCLUSION

In this work, an introduction to PV plus battery storage systems and methods of improving the current state of the art was presented. This involved the novel design and development of multiport converters. The present state of the art of multiport converters provides ample options for selecting a suitable power conversion system. However when performance metrics such as low cost, high efficiency, high power density and flexibility of operation on a modern power grid system are considered, only a handful of options emerges as viable. Therefore, it was determined that there is a gap in the multiport converter technology between what is available today and what will be expected in future. Based on these findings, a dual active bridge based bidirectional DC-DC power conversion systems was investigated. DAB provides three degree of freedom control based on the conduction angle and phase shift between the PWMs that are used to switch the bridges. It was found that the modulation parameters can be optimized to provide higher efficiency and reduce the current and voltage stresses on the devices. A KKT based formal optimization approach was used and analytical solutions were presented which improved efficiency and reduced rms and peak current when used in a hybrid fashion. Furthermore, a single stage microinverter was developed based on the DAB topology which used an AC-link arrangement to convert DC-AC and to maintain the attractive benefits of DAB, such as soft switching, simple control scheme etc. By combining the DC-DC and DC-AC converter stage, a three port single stage DC-DC-AC converter was proposed, which allows bidirectional power flow between any two ports. However, the proposed converter suffered from cost and efficiency impacts as it used 16 active switches. So in a second phase, an improved TPC was proposed. It was partially based on similar concepts of DAB topology with an interleaved boost stage integrated into it. The improved TPC achieved similar power conversion capability with only half the number of switches, which improved efficiency and lowered cost. In addition to this, the proposed TPC allowed power decoupling on one of its ports when a bulk capacitor was connected. The TPC allowed PV and battery to be connected

to its input DC ports and either grid parallel or standalone AC at its output port. The proposed converter provided a complete solution to the PV-battery integration problem from a topology and architecture standpoint. Finally, an output voltage mode controller was developed which maintained the output AC rms voltage at 110V and rejected the input disturbances which could be expected from a PV module operating under maximum power point tracking.

APPENDIX A: DETAILS OF HARDWARE RESOURCES

Picture of the prototypes:

Dual Active Bridge DC-DC Converter:

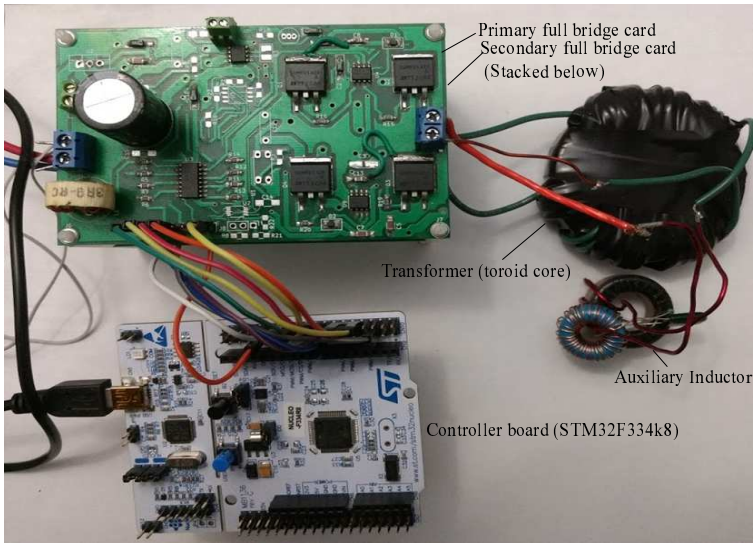

Figure A.1: Picture of DAB DC-DC converter prototype

Improved Three Port Converter:

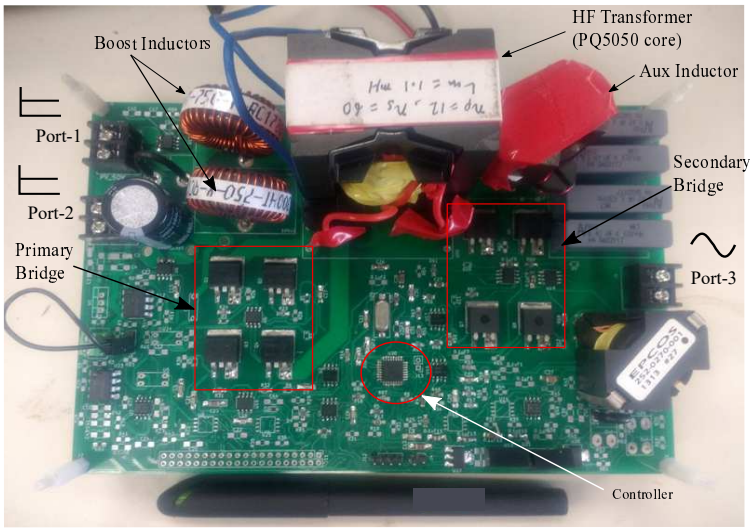

Figure A.2: Picture of the improved TPC prototype