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On-Chip ESD Protection Design: Optimized Clamps

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ON-CHIP ESD PROTECTION DESIGN: OPTIMIZED CLAMPS

by

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ABSTRACT

The extensive use of Integrated Circuits (ICs) means complex working conditions for these tiny chips. To guarantee the ICs could work properly in various environments, some special protection strategies are required to improve the reliability of system.

From all the possible reliability issues, the electrostatics discharge (ESD) might be the most common one. The peak current of electrostatics can be as high as tens of amperes and the peak voltage can be over thousand voltages. In contrast, the size of semiconductor device fabricated is continuing to scale down, making it even more vulnerable to high level overstress and current surge induced by ESD event. To protect the on-chip semiconductor from damage, some extra "clamp cells" are put together to consist a network. The network can redirect the superfluous current through the ESD network and clamp the voltage to a low level.

In this dissertation, one design concept is introduced that uses the combination of some basic ESD devices to meet different requirements first, and then tries to establish parasitic current path among these devices to further increase the current handling capability.

Some design cases are addressed to demonstrate this design concept is valid and efficient: 1. A combination of silicon-controlled-rectifier (SCR) and diode cluster is implemented to resolve the overshoot issue under fast ESD event. 2. A new SCR structure is introduced, which can be used as "padding" device to increase the clamping voltage without affecting other parameters.

Based on this ”padding” device, two design cases are introduced. 3. A controllable SCR clamp structure is presented, which has high current handling capability and can be controlled with by small signal. All these structures and topologies described in this dissertation are compatible with most of popular semiconductor fabrication process.

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CHAPTER 1
INTRODUCTION

The integrated circuit (IC) might be the most important invention in past decades. The evolution of semiconductors and ICs paves the road for our human beings to the great information age. With improving technology, hundreds of million transistors were filled into a tiny block smaller than a fingernail. The advanced precision manifacturing transforms the computing monsters from monolith to small devices on our desk and even in our pocket. At the same time, the working environment of ICs were changed from clean laboratories to more complex conditions like chaotic office, noisy outdoors and unknown outer space. To guarantees these ICs could work properly in different environment, besides the functional design, IC designers usually need to pay some extra attention to the reliability problems.

1.1 ESD Protection in Industry

Among all the possible reliability issues, the electrostatics discharge (ESD) might be the most common problem one IC would encounter in its lifetime. The ESD happens when one object with higher or lower electrical potential approaching the IC. Depending on the characteristics of the object, the discharge event can sustain for tens to hundreds of nanoseconds (ns)[1][2]. The peak

voltage in this process can be over thousands of volts, and the peak current can be as high as tens of amperes. Regardless the short time, the high voltage and current level during ESD event are almost compatible with the value on high voltage power grids[3][4][5]. Therefore, the ESD protection should be an indispensable part of IC design.

The modern ICs benefit a lot from scaling down. The smaller transistor means higher density and more powerful circuits with the same die size. However, smaller size makes the transistor more vulnerable to high level overstress and current surge induced by ESD event. Besides, some special applications like high voltage and high frequency leaves more challenges to the ESD protection design, because the ESD protection should not interfere with the normal function of ICs. As a result, even the IC industry is already well developed nowadays, the high-robust and high-efficient ESD protection design is still required.

1.2 ESD Standards and Characterization

The ESD event could happen at any stage throughout the lifetime of ICs: from fabrication, packaging, transportation to the user-end usage[5]. In order to better describe and gauge these events, corresponding standard models were made based on the characteristics of object/subject[1][2].

The standard tests employ the pulse generated by different models to mimic the ESD event in corresponding category. The voltage level at the source are usually used as the guage to describe the intensity of the pulse (for example, HBM 2KV stands for 2KV source voltage in human body model). The product is rated according to the voltage level it can pass for a specified model[6].

1.2.1 Component-level ESD Models

Based on different purposes, the models/standards can be classified into two categories: the component-level and system-level[6]. The component-level models are used to simulate possible ESD events before the chip mounted to PCB board[7]. After mounting, the chip and the board consist the system. The ESD events to system are described using system-level models. The on-chip ESD protection schemes pay more attention to the component-level standards.

1.2.1.1 Human Body Model (HBM) and Machine Model (MM)

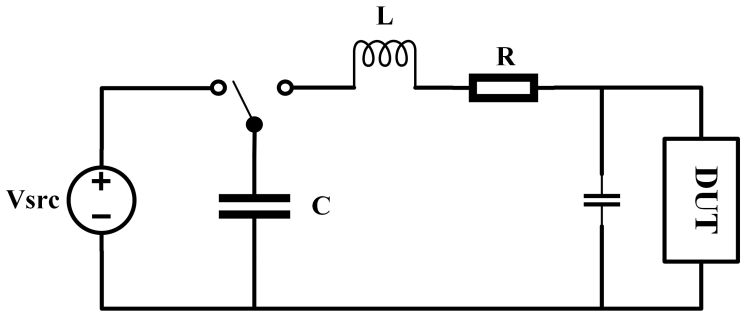


Figure 1.1: Equivalent Circuit of HBM& MM Model

Both human body model and machine model shares the same equivalent circuit (Figure.1.1). They are established to mimic the electrostatic discharging process when a charged human/mechanical arm touching the components[8][9]. As for the different characteristics of human and machine, the circuit parameters in these two models are not the smae. According to the JEDEC standard, in

human body model, the resistance value is 1k5Ω. The capacitance C = 100pf and the inductance L=7.5μH. The waveform for a 2kV HBM is shown in Figure.1.2[1].

In machine model, based on the standard, the resistance is 15Ω, while C=200pf, L=1.5μH[1].

Due to smaller resistance along discharge path, the current arises faster in machine model with lower voltage level. In most cases, the rating in these two models can be transformed because the similarity in their equivalent circuit structure. The tranform fomular is[2]:

$$V_{HBM} = 0.93 \times V_{MM} \tag{1.1}$$

As a result, the machine model becomes redundant and is gradually obsoleted by the industry.

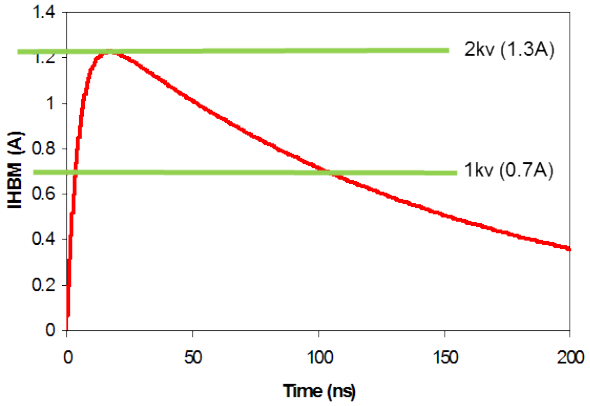


Figure 1.2: Current Waveform of 2kV HBM Event

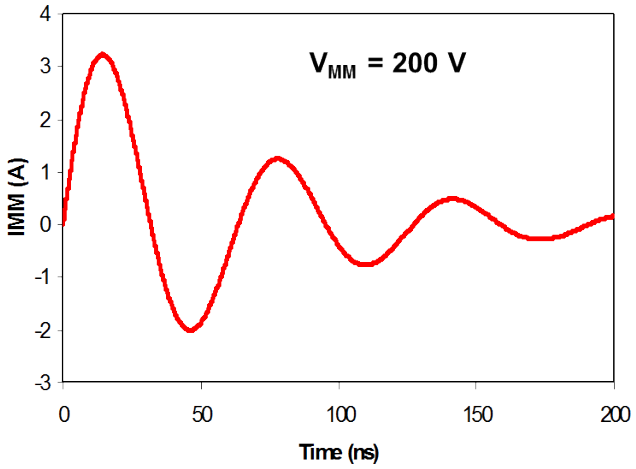


Figure 1.3: Current Waveform of 200V MM Event

1.2.1.2 Charged Device Model

The charged device model (in Figure.1.4) is established to emulate the discharge process when a charged component/chip approaching the metallic plate[10]. The charge will transfer from the circuit inside the chip to the metallic plate through pins. Comparing to HBM and MM, the process in this model is a reverse process. The charges move from inner circuits to the outside. The CDM event frequently occurs during the stage of packaging, transportation and mouting. Due to the small inductance along discharge path, the rise time and duration of its waveform are shorter than HBM and MM waveform, while the peak current could be extremely high[11]. The waveform is plotted in Figure.1.5. The rapid rising edge usually cause damage on the gate of MOSFETs if they are connected to the pins.

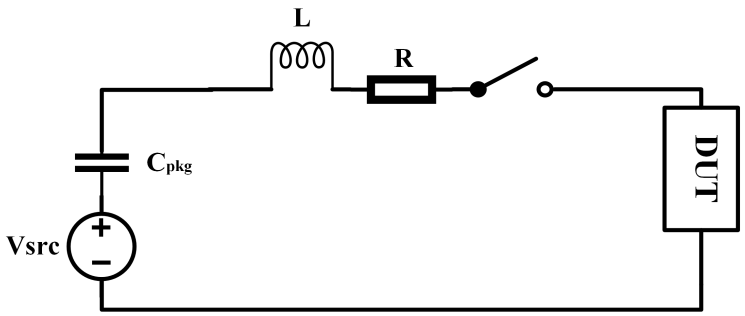


Figure 1.4: Equivalent Circuit of CDM Model

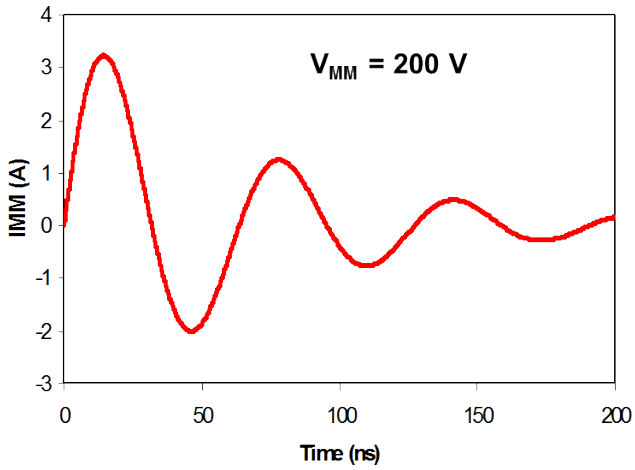


Figure 1.5: Current Waveform of 500V CDM Event

1.2.2 ESD Test Methods

The ESD tests are conducted to rate the ESD handling capability of the product or to extract behavior of the ESD protection design for analysis. Based on the purpose, accordingly, the ESD tests can be classfied into two major group.

1.2.2.1 ESD Qualification Test

For qualifying purpose, engineers only care at how much voltage level the product can survive under a specified pulse[12]. For instance, a batch of chips are going to be tested to see if they are able to survive under 2kV HBM pulse. The 2kV HBM stress will be applied to these chip directly. After stress, functional testing will be conducted on the chips. They could only get the 2kV HBM qualification when they can work properly after the HBM stress. For MM and CDM test, the test procedure is similar.

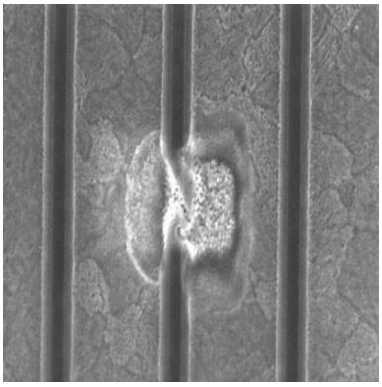


Figure 1.6: HBM-Induced Thermal Damage on Juntion

The ESD qualification test is destructive test, which means the target device under tests might be damaged[13].

Post-stress failure analysis could help find some clues about the defects of ESD design on chip[13]. For example, the HBM pulse usually cause thermal damage on P-N junctions (in Figure.1.6). With the aid of microscope, the failure point can be located and optimization on ESD protetion design can be made accordingly. However, the post-stress information is too limited

to have a comprehensive understanding of how the ESD protection design react during the ESD event. Another non-destrutive testing makes it possible.

1.2.2.2 Transmission Line Pulse Test

The Transmission Line Pulse (TLP) Test is one kind of non-destructive testing, which is first introduced into ESD testing by Maloney and Khurana in 1985[14]. It utilized a charged transmission line to generate square waves (zap) in time domain to the test target. During each zap, the voltage and current waveform on the test target will be captured and sampled to get the average voltage/current value. With progressive zaps, a I-V curve can be obtained. This I-V characteristics is usually different from its DC curve. Instead, it represents the behavior of test target under ESD stress[15][16].

There are two most frequently used TLP setups: the 100ns regular TLP and very fast TLP (vfTLP). The rise time of 100ns TLP pulse is set as 2ns to 10ns. The rise time and pulse duration are comparable to HBM pulse. So 100ns TLP can be used to estimate the HBM level of the test targets. The very fast TLP has much shorter rise time (100ns) and pulse width (5ns-10ns), which can be used to estimate the CDM level of the device[16][17].

1.2.3 ESD Protection Design

The signal and power transfer into and out from chips through the pins, so as the ESD stress. A successful ESD design should satisfy three requirements[2]:

- It shouldn't interfere with the working signal and power.
- It has the ability to clamp voltage to low level for all pins.
- It can always provide a current discharge path between any two pins.

To meet the first requirement, for each pin the ESD design must satisfy the design window. For the second requirement, high-efficient ESD clamp is needed. For the third requirement, a connected network for all the pins can be the solution.

1.2.3.1 ESD Design Window

The TLP testing can provide the I-V curve to show how an ESD clamp cell behave under ESD stress. Then the problem is how this curve can help in ESD design.

It's instructive to plot the signal swing range and failure voltage in the same I-V graph (Figure.1.7)[18]. The Vfail+ and Vfail- stand for the failure voltage in positive and negative direction, respectively. The signal swing range is from V- to V+. The area between the failure and normal operation range is defined as ESD design window.

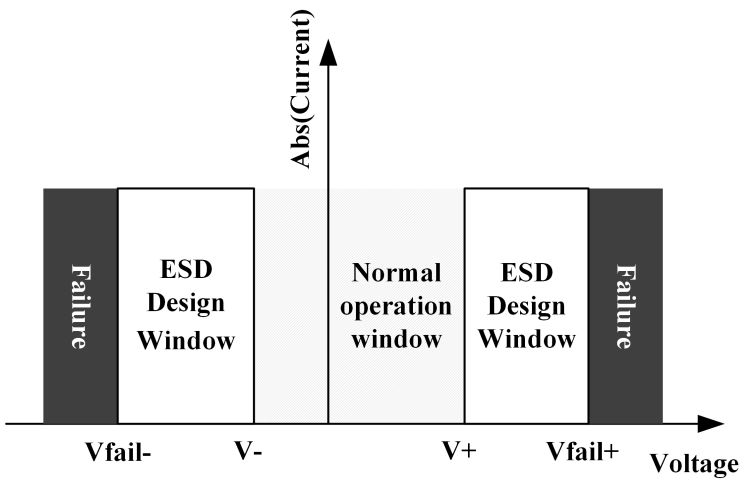


Figure 1.7: ESD Design Window

Suppose a ESD clamp cell placed between the pin and ground. Obviously, unless there is an active controll element in the ESD cell, it must stay in off state in the normal operation window and on state in ESD design window. If the on-state curve of ESD clamp overlaps with the normal opertaion window, it will intefere with the normal operation. On the other hand, before reaching a specified current level, if the voltage failed to be clampped below failure voltage, this pin will get damage.

With processing technology node, both of the failure voltage of circuit and operation voltage drop to extreme low level, making the ESD design window shallow, leaving more challenges to ESD designs[19][20].

1.2.3.2 ESD Network

In digital circuit design, to solve the problem of communication across multiple modules, the concept of signal bus is introduced. No need for indepednent connections between each two module, all the modules share the same signal bus, which significantly reduces the complexity and layout area for routing.

Likewise, the concept of bus can be implemented in ESD protection network design as well. That's so called the ESD bus.

The power grid can be used as the ESD bus[21]. One reason is that the power grid spreads over thie chips. Any pin can found a short path to the power grid. The sceond reason is that the power grid is design to deliver power to the chips, so it has wide interconnects, which is capable to carry large current in ESD event. The most common network setup is shown in Fig.1.8[22][23]. ESD clamp cells are placed between each I/O to VDD and VSS, which link the I/Os to the ESD busses VDD and VSS. Specially, a clamp cell called Power Clamp is placed between the VDD and VSS[24][25].

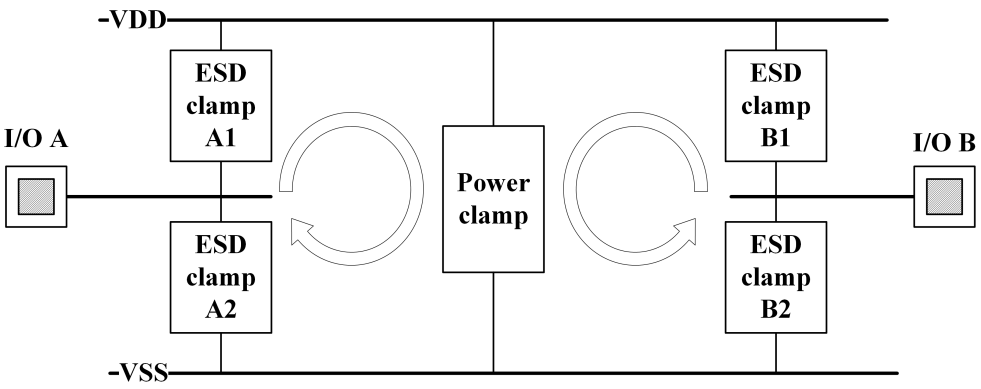


Figure 1.8: Power-grid-based ESD Protection Network

If the ESD clamp and power clamp is well designed, these clamps would be invisible for signals and power because all of these cells are in off state in normal operation[25]. When ESD event occurs, a current path can always been found between any two nodes for discharge. For example, the ESD current from I/O A to I/O B in Figure.1.8 can be discharged through ESD clamp A1, power clamp and ESD clamp B2. The clamping voltage is computed as the sum of voltage drops for all the clamp cells along the discharge path.

In more complex ICs such as System on Chips (SoCs) and mixed-voltage circuits, there exist multiple power domains. To ensure the connectivity among the networks in each subdomain, the cross-domain clamp is required (See in Figure.1.9)[26]. Similarly, these power domains are isolated in normal operation. The cross-domaind only conduct current when ESD event comes.

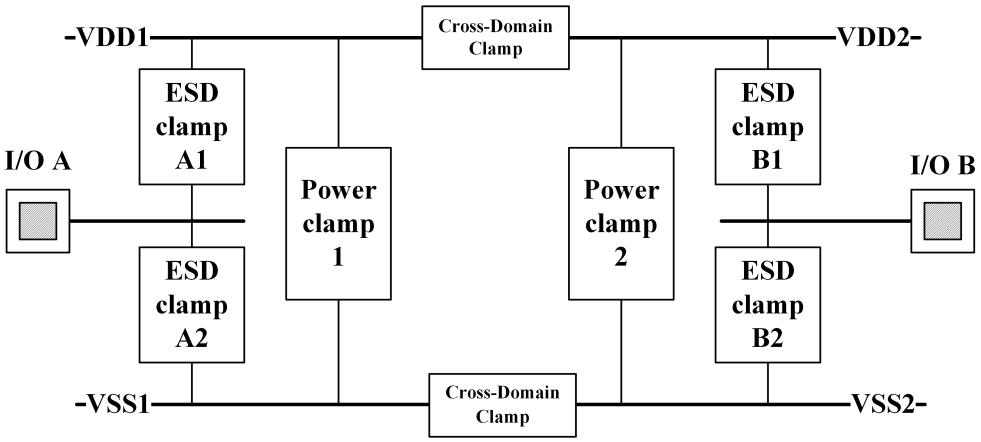


Figure 1.9: Cross-domain ESD Protection Network

In some mixed-voltage applications, the voltage swing on I/O might exceeds the range of power domain. If still adoptting the network in Figure.1.8, it would be impossible to keep the ESD clamp off in normal operation. The local protection solution in Figure.1.10 is introduced for this case. In this scheme, the ESD clamp here must have high blocking voltage in both direction to meet the high swing of signal on I/O[27]. The ground line is used as the ESD bus.

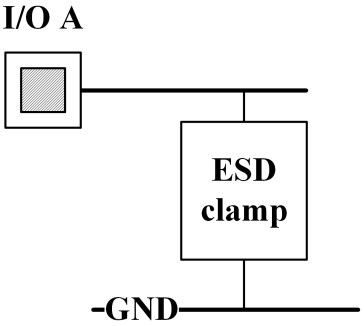


Figure 1.10: Local ESD Protection for Interface

1.2.3.3 ESD Clamps

Depending on different behaviors under ESD stress, the ESD clamp can be classfied into different categories: the voltage regulator and ESD switch with snapback charateristics.

The I-V behavior of the voltage regulator is plotted in Figure.1.11. It remains off in normal operation window. Once the voltage arises to the trigger point, the voltage regulator will be turned on and prevent the voltage from continuing rising. The corresponding voltage and current at this trigger point is called trigger voltage (V_{t1} for short) and trigger current (I_{t1}) respectively in the following paragraphs. When the current continues going up, the clamp will finally get failed. At the failure point, the voltage and current is called failure voltage and failure current, denoted by V_{t2} and I_{t2}. The slope after trigger stands for the on-resistance R_{on}.

The voltage regulator can be a zener diode, a cluster of PN junction diode or any other structures [28][29].

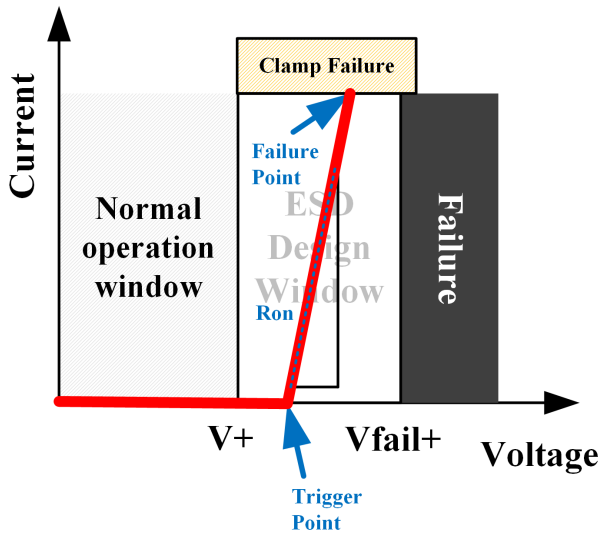


Figure 1.11: I-V Curve of Voltage Regulator

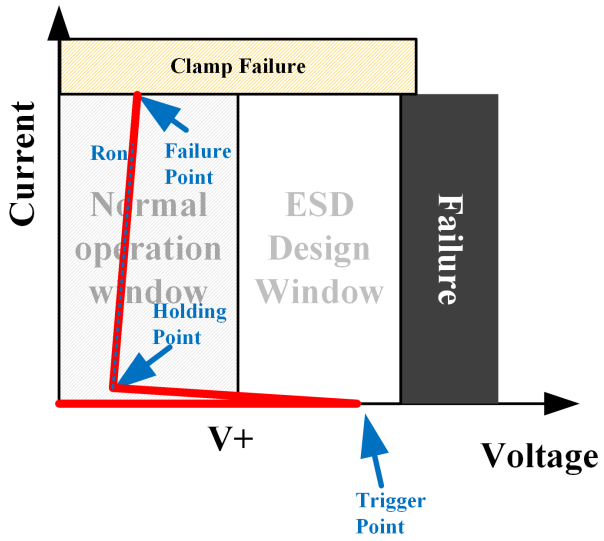


Figure 1.12: I-V Curve of Switch with Snapback Charatertics

Different from the voltage regulator, the voltage on switch with snapback charateristics will drop after turning on. The turning point is the trigger voltage (use V_{t1} and I_{t1} denoting the trigger voltage and trigger current as well). After triggering, the I-V drops a low-voltage state called

holding point, at which point the voltage and current is V_h and I_h, respectively. As with the voltage regulator, the snapback switch will get failed at some current level. The voltage and current at this point is denoted by V_{t2} and I_{t2}. The snapback swithes usually possess low on-resistance R_{on}, so it's very efficient in discharging.

The snapbak switch could be a SCR, a Gate-grounded NMOS or a NPN transistor[30][31].

In applications, the voltage regulator usually used as the clamp cell to prevent the victim circuit from being damaged by voltage overstress. The snapback switch can act as a low-voltage-drop discharge path. The high blocking (trigger) voltage of switch guarantee it remaining in off-state during normal operations.

CHAPTER 2
ON-CHIP ESD PROTECTION DESIGN

Essentially, most of the developments in engineering are complished through the trial-and-error procedure. Initially, the protype is designed and fabricated. Different kinds of tests are conducted to extract the performance factors and defects of the protype. With the extracted information, the protype design is going to be revised or optimized. This process will repeat several times until the output satisfying design targets.

2.1 ESD Design Flow

Like many other engineering design process, the ESD protection designs are also completed in the trial-and-error iteration. However, the tapeout cost become higher and higher with the evolution of fabrication technology. The trial-and-error cost soars in state-of-the-art process as well. To have better estimation on the performance of a design before fabrication, the computer-aided-design (CAD) is introduced to the design flow. Modern CAD tool allows engineers simulate the designs instead of doing testing after tapeout. It not only reduced overall cost of time and money significantly, but also provide more state information inside the designs.

2.1.1 Simulation Tools

In on-chip ESD protection design, there are two types of simulators that frequently utilized in industry. One is circuit/system level simulator, including spice-like circuit simulators and verilog-AMS based simualtors. This group of simulators treat the circuit as a nodal network. In the network, each node represents one equipotential point. The branchs connecting the nodes stand for the devices (transistors and so on) in circuit, which are described with compact models or behavior models. Based on the tasks, the network can be anaylzed using modified nodal analysis (MNA) algroithm in static condition, transient condition or freqency domain[32]. The circuit/system level simulation is fast, which is suitable for large-scale circuit/system. The accuracy of the simulation result is acceptable as long as the device model is good enough. This kind of simulator is widely adopted for ESD protection designs based on devices with avaiable model[33].

Another kind of simulator is an essentially physical numberical solver using finite element method or finite volumne method[34]. To run the simulation, users need to define the geometrical struture of the device, followed by meshing and boundry condition information. Then identify which physical models will be activated. This device-level simulation can give more physical output informaion than the circuit level simulation. The simulator is usually included in many modern TCAD tools. However, because high density of grids for each single device and more physical models involved, the device simulator costs more time. So it's usually used as device-level analysis.

Some state-of-the-art CAD tool allows combination of above two routes in one simulation task, which is so-called mixed-mode simulation. Both the netlist of target circuits and device structures are assigned as the input. For the devices with compact model, the simulator will analyze the branch using MNA method. For the device with structure and physical information, the FEM will get involved to analyze the branch[35]. The mixed-mode simulation enables analysis of some special devices in a large-scale circuit without compact model.

2.1.2 Design Flow

As discussed above, the ESD protection network is consisted of many ESD clamp cells. The design flow of ESD network can follow the top-down procedure. As shown in Figure.2.1, based on the working conditions of the pins on chip, the network type should be determined first. The next step is trying to request suitable ESD clamp from the clamp library. If can't find one, going into the ESD clamp design procedure in Figure.2.2. Following this procedure, fill the network with the selected clamp cells. Run the simulation to optimize the topology and parameteres of the network. The design will send out for tapeout. Finally, test will be conducted on the wafer. If some performance fator is not satisfied, it should go back to the design stage to fix the design. The iteration will continue until meeting all the requirements. The complished design will be implemeneted on the final products.

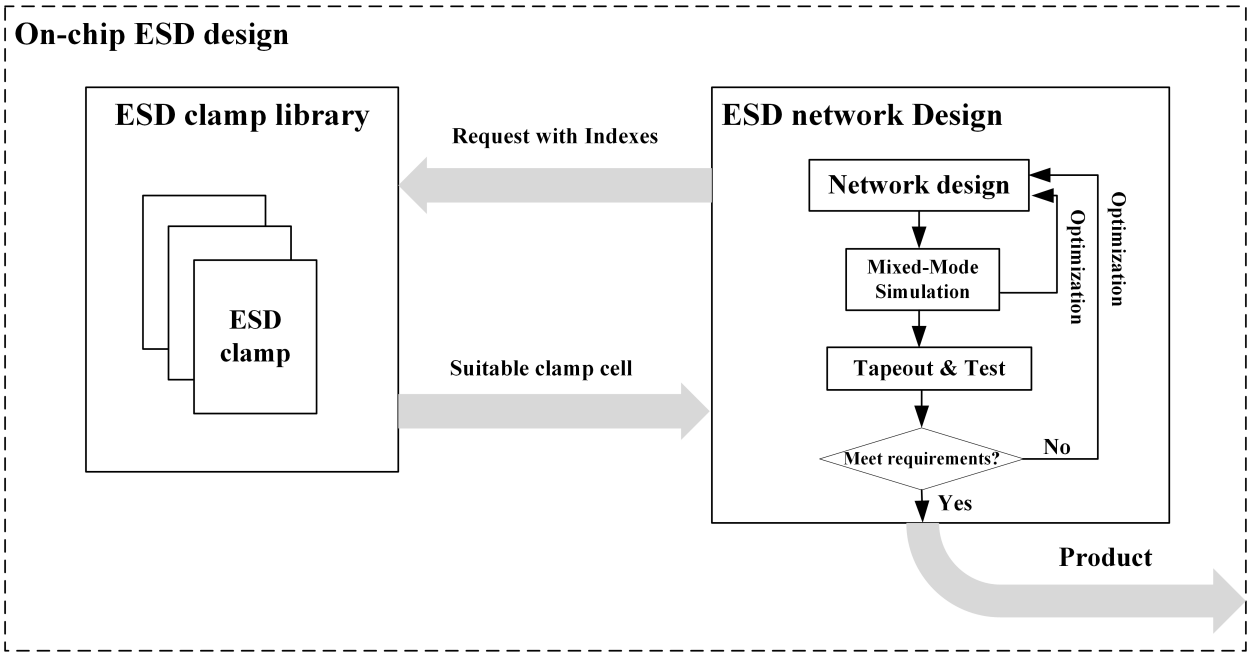


Figure 2.1: On-Chip ESD Protection Design Flow

The ESD clamp design flow is depicted in Fig.2.2. The ESD clamp cell could be a single device or a circuit composed by multiple standard/customized devices.

Most of the standard devices from foundry are equiped with verfied compact model. So the ESD circuit composed standard devices can be easily evaluated using circuit simulator. The design will be repeatedly tuned until design objectives satisfied.

User-customized ESD devices usually possess superior ESD performance than the standard device in specified environment. However, they lack support of compact models. In design and optimization stage of the ESD devices, the device simulator will be utilized. If one device meets all the requirements in testing, it will be delivered to ESD circuit design stage. Otherwise, it will go back to design stage for optmization.

In ESD circuit design with customized device, the mixed-mode simulation evaluate the customized device and circuit at the same time. The successful design will release to the next stage of integration with functional circuits. If the design failed in Test, by failure analysis on mixed-mode simulation result, optmization should be made ethier on the device structure or on the circuit topology.

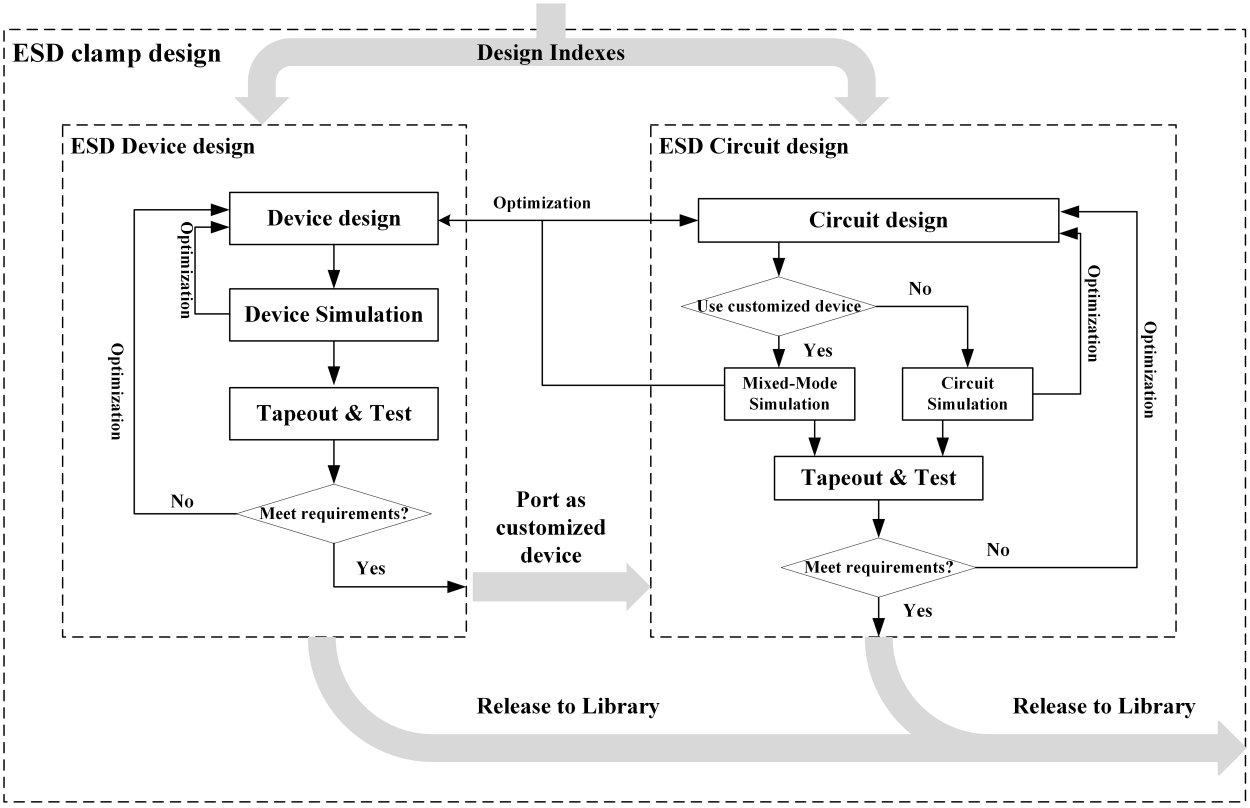


Figure 2.2: On-Chip ESD Protection Design Flow

CHAPTER 3
EMBEDDED SHUNT DIODE PAIR TO SUPPRESS OVERSHOOT VOLTAGE

In this charpter, a completed flow of ESD clamp design is addressed to show how it works. The major objective of this design is to optimize the turn-on speed of an basedline bi-directional SCR. In addition to the turn-on speed improvement, the clamping voltage under fast ESD event like vfTLP is reduced as well. Despite many benefits, the embedded structure leaves no influences on other paramters like DC breakdown voltage and trigger voltage. The optimized device can fit the original design window of baseline device perfectly. The concept of suppressing overshoot voltage using shunt diode can be implemented in many other structures as well.

3.1 Description of Objective

Following the top-down design flow described in Chatper.2, the clamp cell will be placed on a mixed-voltage interface, which should adopt the scheme in Figure.1.10. The wide-range voltage swing makes a request for high blocking voltage in both directions.

There already exists a baseline bi-drectional device in the library which fits the design window of this interface[36]. However, due to the long distance from anode to cathode in bi-directional

SCR, the transition time from off-state to on-state is longer than other ESD devices. The slow turn-on time of conventional bi-directional SCR induces high overshoot voltage under fast ESD stress like CDM.

The optimzed design should fit the original design window with reduced overshoot voltage.

3.2 Description of Structure

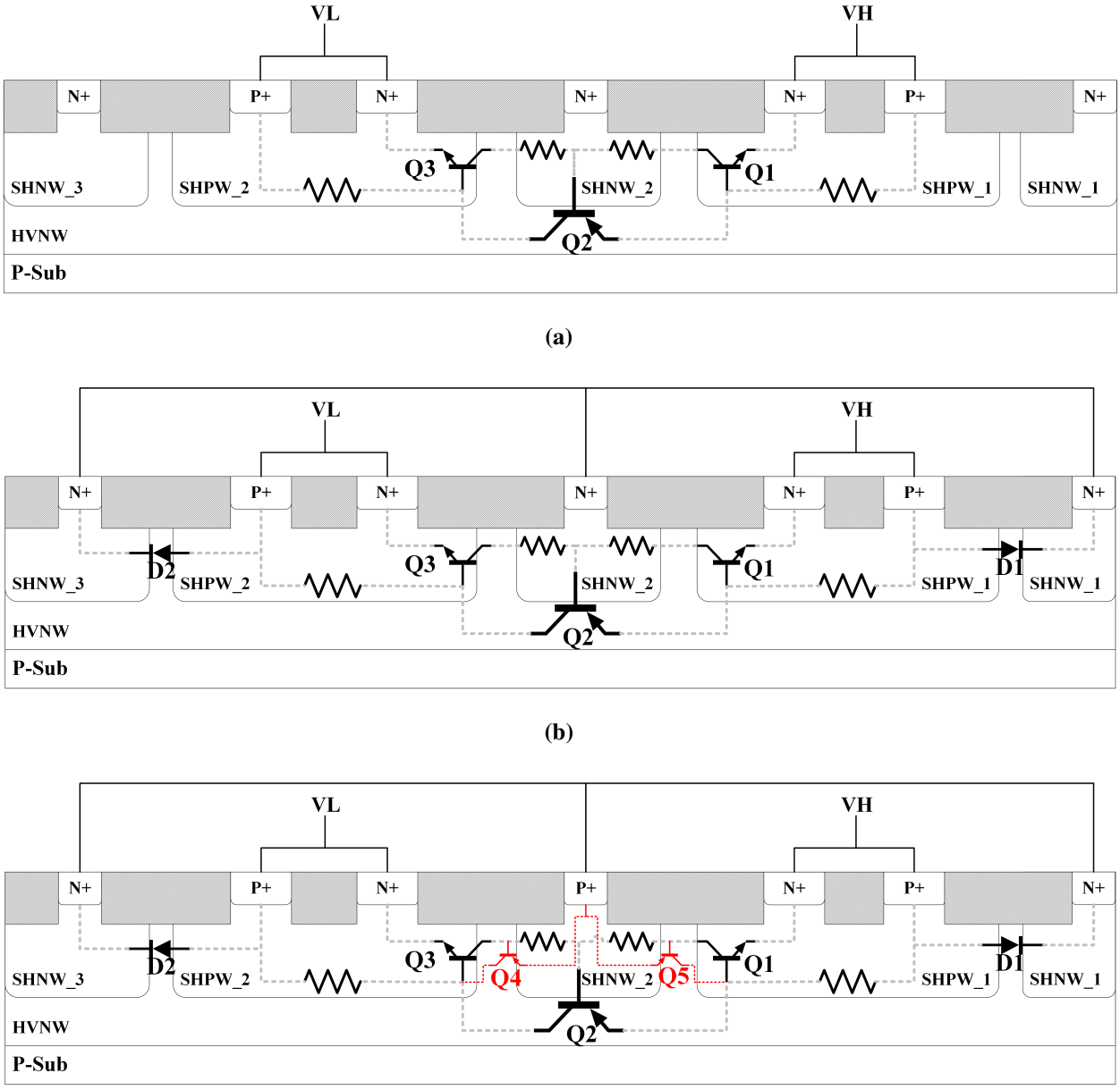


Figure 3.1: Cross-setion of Devices to be Investigated: (a) Baseline SCR (b) Baseline SCR with Shunt Diode Pair (c) Modified SCR with Shunt Diode Pair.

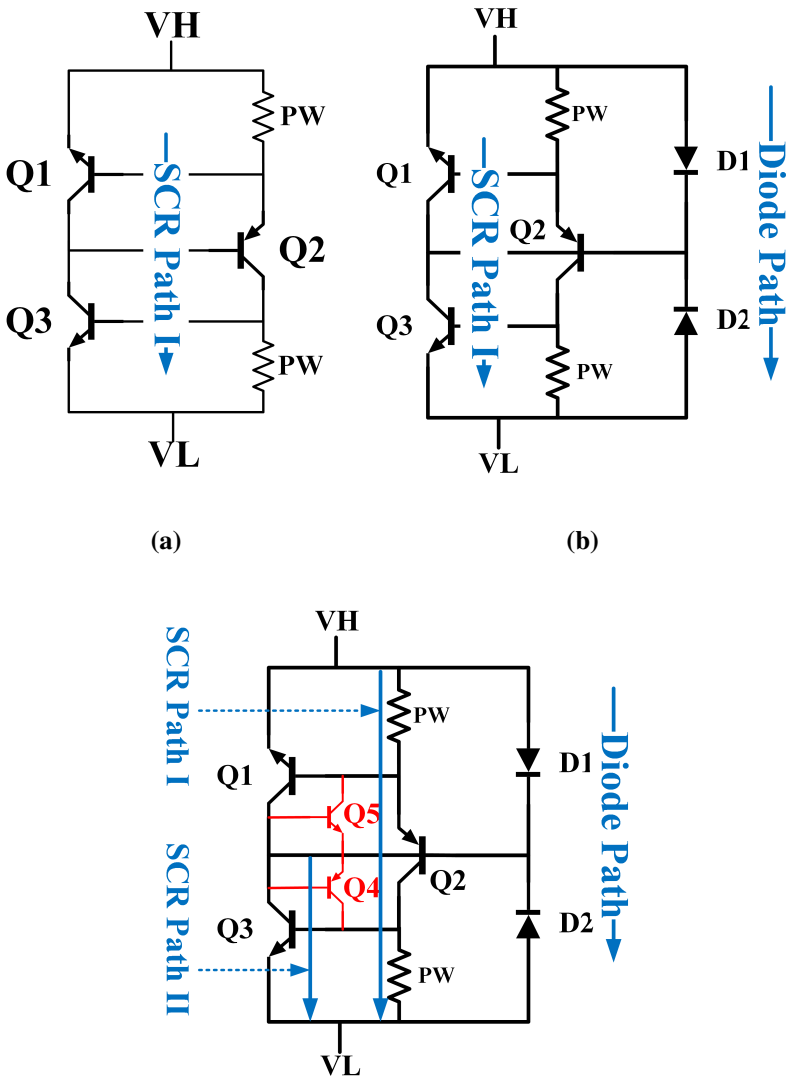


Figure 3.2: Equivlent Schematics of devices in Figure.3.1 (a) Baseline SCR (b) Baseline SCR with Shunt Diode Pair (c) Modified SCR with Shunt Diode Pair.

The cross-section of the baseline SCR is shown in Figure.3.1a. The symmetric structure guarantees high blocking voltage in both direction. In its equivalent circuits in Figure.3.2a, the SCR path is marked as SCR Path I.

As we already know, the turn-on time of diode is much faster than the SCR, because no conductivity modulation involved in its turning on process[37]. In principle, by puting the diode in parallel with SCR, the overall turn-on speed can be improved. This concept is implemented in Figure.3.1b. In order to compatible with the bi-directional feature of orginal baseline device, two reversely oriented diodes are put in series. This design is to gurrantee enought blocking voltage in both direction. The DC breakdown voltage (BV) of the the diode cluster is tuned beyond the BV of baseline SCR but lower than the SCR's trigger voltage. The purpose of such design is to make sure the diode cluster can be turned on successfully without impact on the overall BV.

The equivlent schematic for this struture is shown in Figure.3.2b. Besides the original SCR Path I, there is a diode path consisted of diode D1 and D2. The diode D1 is in parallel with the branch composed by emitter-base junction of parasitic transistor Q2 and the resistor in PWell. Obviously, D1 will redirect current from emitter of Q2 to D1-D2 diode path, making it more difficult to turn on Q2, so does the SCR path I conssited of Q2 and Q3. In this condition, the diode path is likely to be damaged before SCR path I fully turning on.

A modified SCR with the shunt diode pair is proposed as in Figure.3.1c[38][39]. The central N+ diffusion is replaced by P+ diffusion, introducing two more parasitic PNP transistor Q4 and Q5. Q4 and Q3 consist a extra SCR with shorter range in positive direction (as shown in Figure.3.2c). Due to shorter distance between anode and cathode, this short-range SCR (marked as SCR Path II)

will be turned on much faster than the long-range SCR path I. The current redirected by D1 will flow through SCR Path II. Before SCR Path I fully turned on, the SCR path II can conduct most of the current.

3.3 Simulation Analysis

To verify the assumption in previous section, the TCAD simulation is conducted. In addtion to the strutures in Figure.3.1, the indepdent diode pair in Figure.3.1b and Figure.3.1c is included in the simulation for comparison. The width of all the devices are set to 80μm;

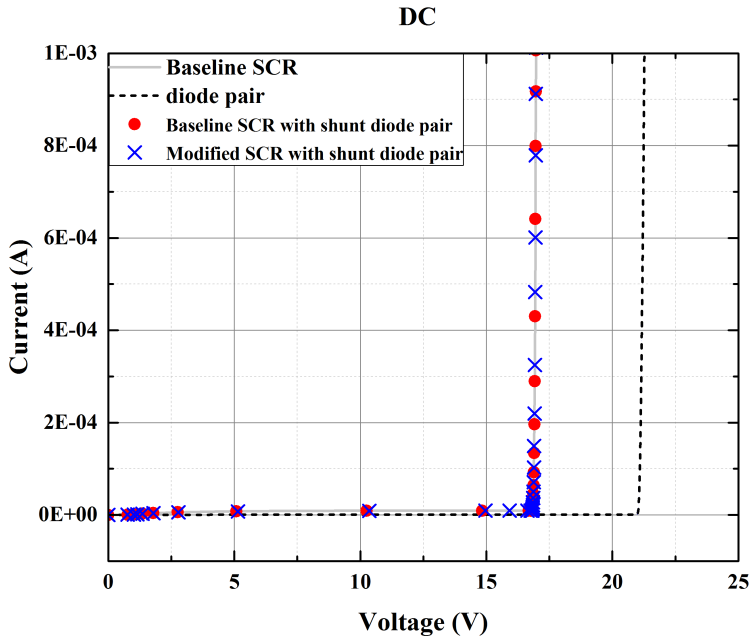
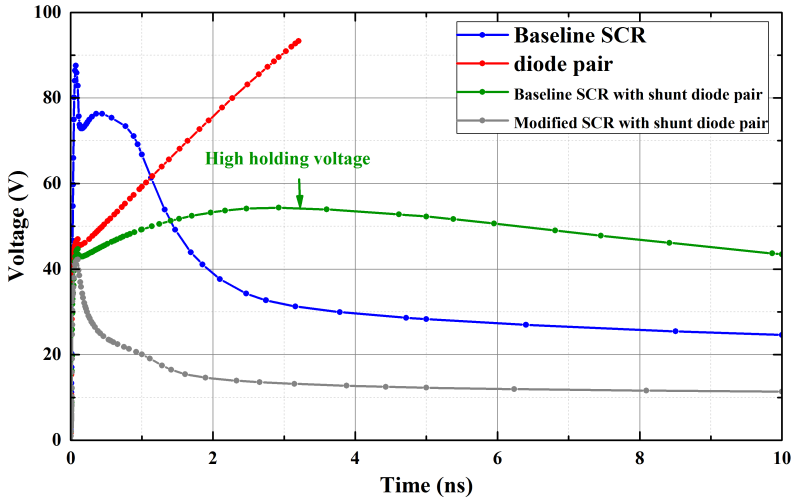
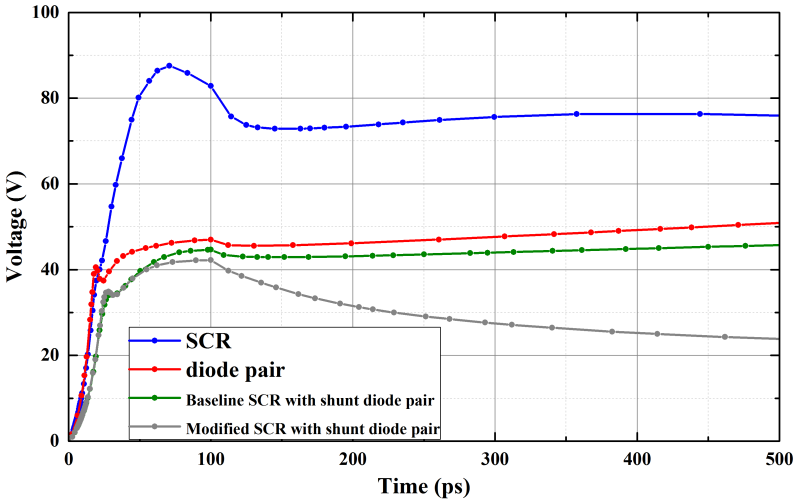


Figure 3.3: Simulated DC Curve.

The simulated DC sweeping curve in one direction is shown in Figure.3.3. Because the breakdown voltage of the diode pair is higher than SCR, putting it with the original SCR will not change the overall breakdown voltage.



(a)

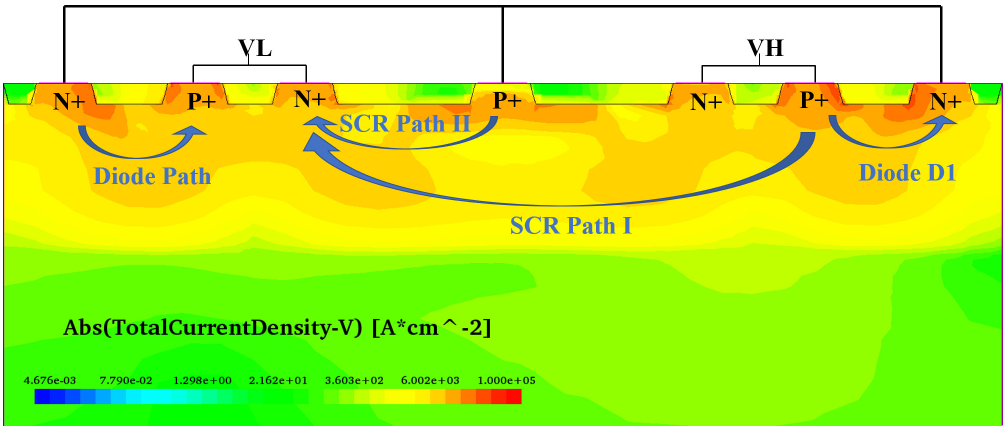


(b)

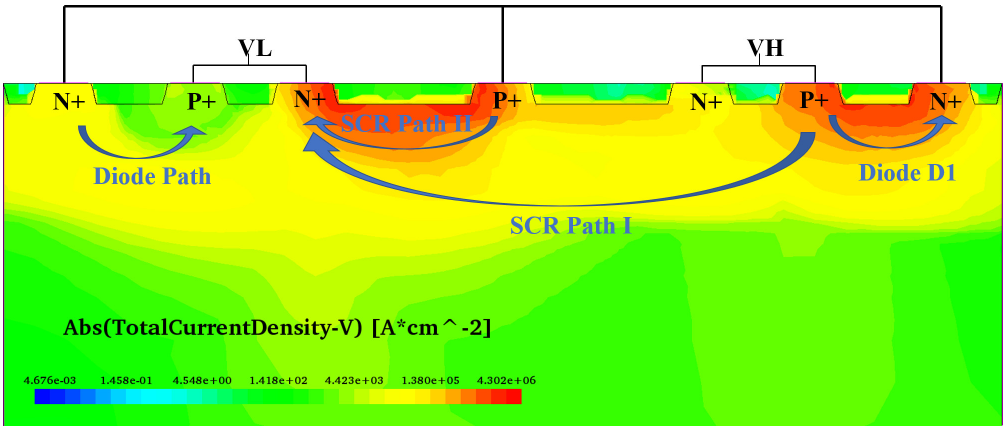
Figure 3.4: Voltage Waveform of VFTLP Simulation (a)0-10ns (b)0-500ps.

The vfTLP simulation is also conducted to verify its transient performance. The pulse width is set to 10ns and rise time to 100ps. The magnitude is 1A. The voltage waveform is plotted in Figure.3.4.

The simulation of diode pair was terminated at about 3ns because maximal lattice temperature exceeds 1400K. Figure.3.4b demonstrates the overshoot volages of all the sturctures with diode pair path decreased as expectation. In Figure.3.4b, the baseline SCR with shunt diode pair has higher holding voltage because the transistor Q2 in Figure.3.2b is obstructed by diode D1.



(a)



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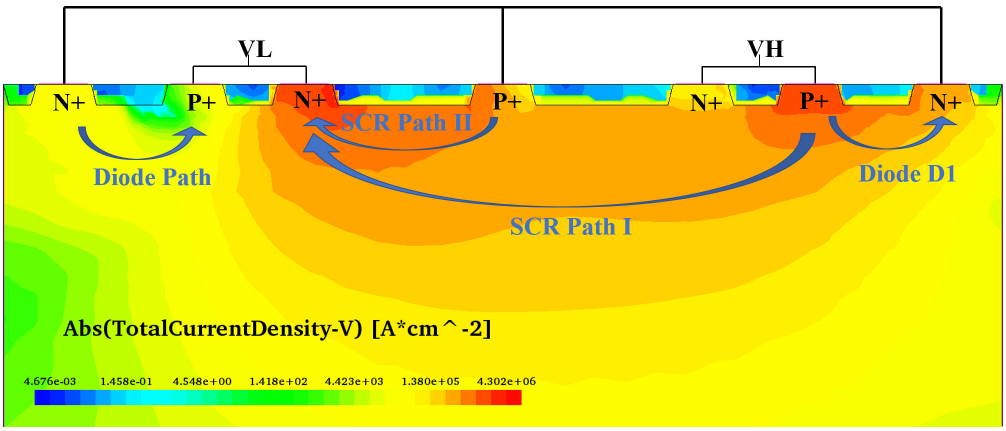


(c)

Figure 3.5: Current Distributions of Modified SCR with Shunt Diode Pair under vfTLP Pulse at (a)5ps (b)100ps and (c)5ns.

For the modified SCR with sunt diode pair, the current distribution at each stage is plotted in Figure.3.5. At 5ps (Figure.3.5a), the reverse diode in diode pair start to breakdown. The majority of the current is flowing through the diode path. At 100ps (Figure.3.5b), the short-range SCR path II started to conduct current. At 5ns (Figure.3.5c), The long-range SCR path I is finally turned on. To better observe the current evolution on each path, the percentage of current through diode path, SCR Path I and II over the total current is plotted in Figure.3.6

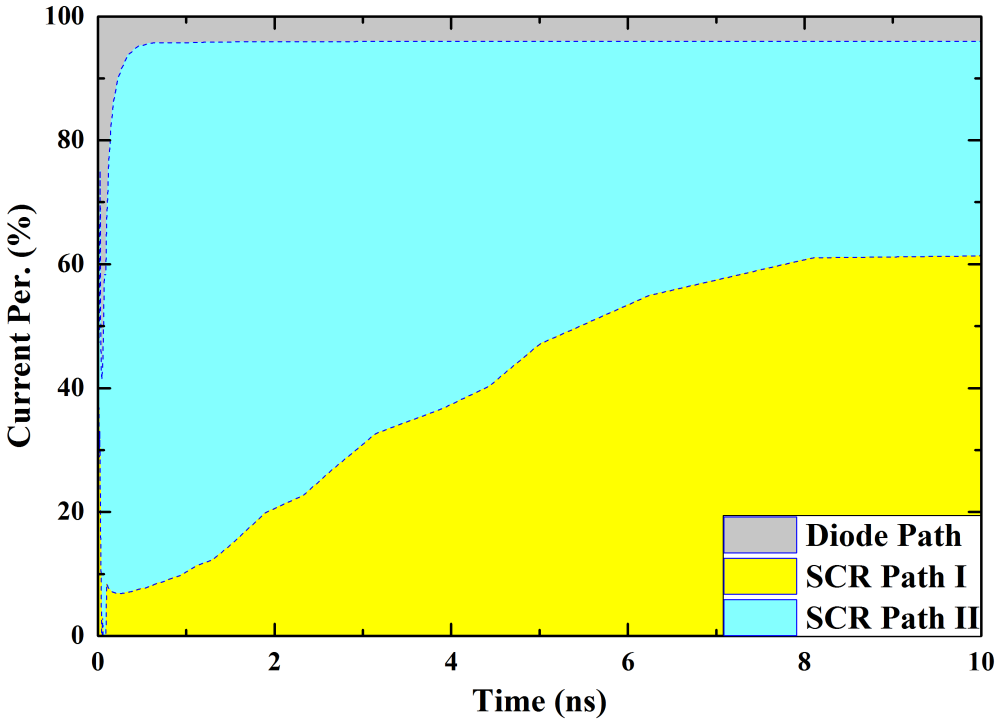


Figure 3.6: Current Proportion for Different Paths in Figure.3.2c during vfTLP Stress.

It's clear that Diode Path turns on first at the begining of vfTLP pulse. Followed by short-range SCR Path II and long-range SCR Path I. Eventually, it's the SCR Path I conducted most of the current.

3.4 Analysis on Test Results

After verfication in simualtor, the three structures in Figure.3.1 were fabricated on a 0.18μm BCD-MOS process. The three devices share the same configurations including spacing and dimension of each part. For reference, the total width of each device is 160μm.

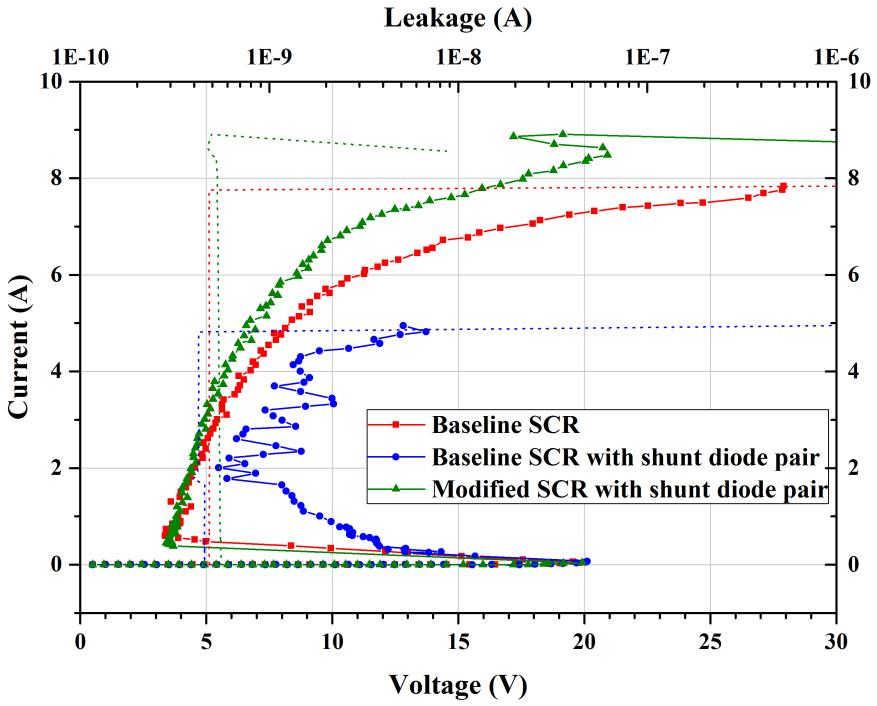


Figure 3.7: 100ns TLP Test Results.

Regular TLP with 100ns pulse width and 10ns rise-time is performed to probe the current handling capability of the three structures. The result is plotted in Figure.3.7, in which the bias voltage for the leakage test after each pulse is set to 15V. The DC voltage sweeps are plotted in Figure.3.8.

Both baseline SCR and modified SCR with shunt diode pair can handle current up to about 8A (50mA/μm). The insertion of additional current paths didn't degrade the current handling capability of the original SCR. The base SCR with shunt diode pair has relatively higher holding voltage due to the negative feedback on the base of transistor Q2 in Figure.3.2b.

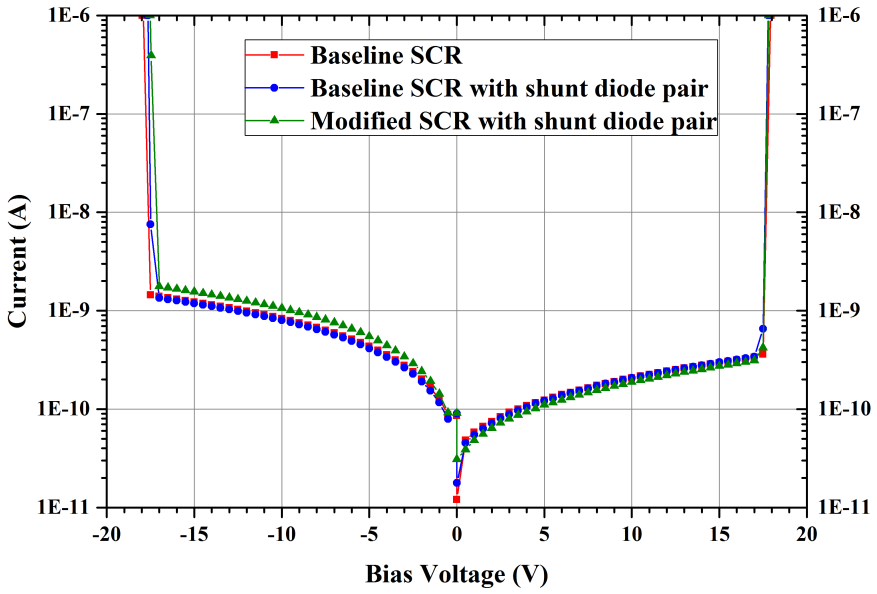


Figure 3.8: DC Sweeping Results.

VFTLP measurement are also used to characterize the turn-on speed and overshoot voltage of the devices. To better understand the result, multiple VFTLP pulses with 10ns pulse width and 100ps rise-time on the target devices were applied. The 100ps rise-time is used to check the overshoot voltage under transient stress. 10ns pulse width is chosen to observe the behavior of each device in quasi-equilibrium state.

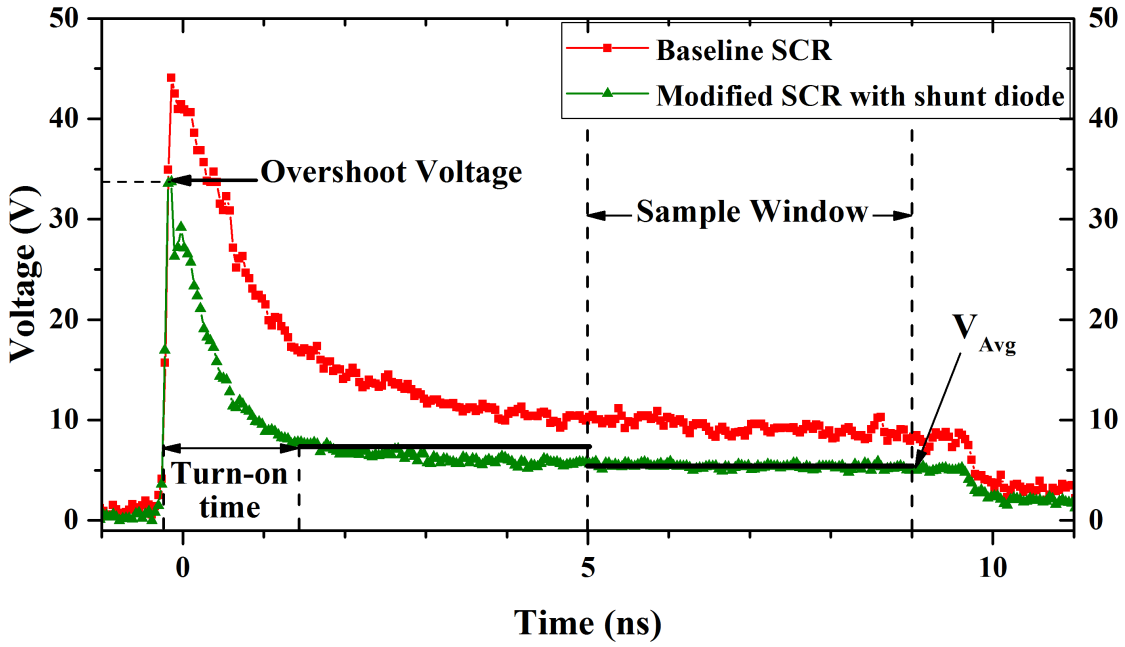
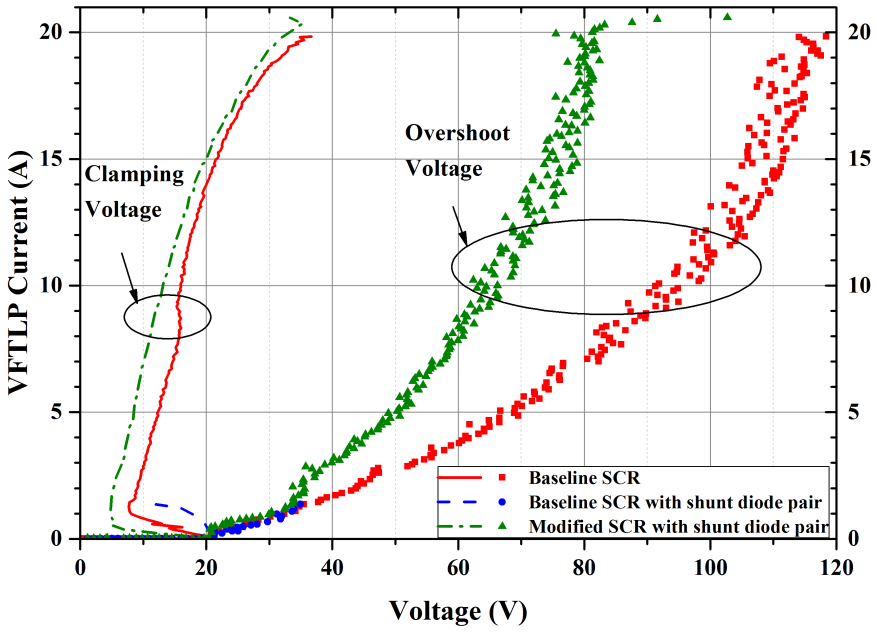
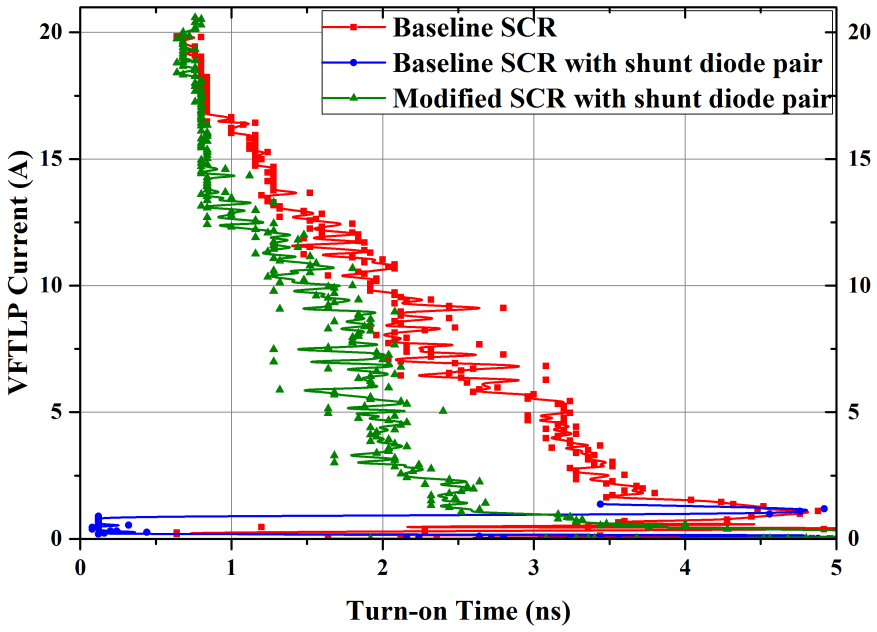


Figure 3.9: Voltage Waveform under VFTLP Pulse with 2A Magnitude, 10ns Pulse Width and 100ps Rise Time.

The resulting waveforms are shown in Figure.3.9. From the waveform, the overshoot voltage can be extracted by measuring the peak voltage. By taking a sampling window from 50% to 90% of the pulse time, the average voltage value V_{Avg} in the sampling window is calculated as the clamping voltage (using the same sampling window for current averaging on current waveform). Another key feature extracted from the test result is the turn-on time. The turn-on time is defined by the time span between the first time point when the voltage equals to V_{Avg} to the time point when voltage drops to 1.2 times of V_{Avg} post peak-voltage. The extracted features are depicted in Figure.3.10.



(a)



(b)

Figure 3.10: Extracted Features: (a) VFTLP Current vs. Clamping Voltage (Scatter Line) and Overshoot Voltage (Solid Line), (b) VFTLP Current vs. Turn-on Time.

In Figure.3.10a, the solid lines represent clamping voltage of each device under VFTLP pulse. Due to the strong conductivity modulation of two SCR paths, the SCR with Central P+ diffusion connected has lowest clamping voltage comparing to the other two. The SCR with Central N+ diffusion has a low failure current level of around 1.3A. This failure occurs on the diode path. The diode path can only handle small currents. Under VFTLP pulse, the voltage and current increase too fast to turn-on the SCR path. While for the modified SCR, the SCR path II can be turned on very fast and conducts current before diode path failed. Therefore, the modified SCR has very strong current handling capability even for fast ESD event.

The scatter lines in Figure.3.10a are the extracted overshoot voltage vs. VFTLP current. As expected, the modified SCR has lower overshoot voltage than the other two. The reason is as described in the previous section: with the shorter current path, the device can achieve faster turn-on speed and lower overshoot voltage.

Figure.3.10b shows the turn-on time of each device vs. VFTLP current. Note that the turn-on time when the current is below approximately 1A is not accurate, because in this regime the devices are not fully turned on. From the comparison the three devices, the modified SCR exhibits significantly reduced turn-on time over the their two structures.

3.5 Conclusion

In the design flow described in this chapter, the overshoot voltage is set as the first target at the initial stage. The diode path is introduced to resolve this issue. Followed by the improvement on failure current by establishing more current path.

The combination of fast-triggered diode path and robust SCR path provides a fast-response bidirectional voltage clamp. By carefully designing the trigger sequence of each path, the overshoot voltage can be reduced without losing the current handling capability for relatively long TLP and HBM stress.

CHAPTER 4
NEW STACKING STRATEGY TO ACHIEVE HIGH HOLDING VOLTAGE

4.1 Introduction

Profited from the relative low clamping voltage in high current state, the SCR is extremely effcient in current handling due to lower power density during discharging[3]. However, the low holding voltage usually leads to another issue - the latchup. If the protected pin is high-power-driven and the holding voltage of SCR is lower than the operation voltage, the pin is likely to get ”trapped” at a low-voltage, high-current state after SCR being triggred. Basically, the holding voltage should be higher than the operation voltage.

A lot of reaserch works have been conducted to improve the SCR's holding voltage[40][41]. Most of them uses process-related tricks in specified technology (like depending on special layers) and cannot be mapped into other process.

The simplest way to achieve the goal is using stacking structure in Figure.4.1[42][43]. With two SCRs in cascade, the holding voltage can be doubled as well. However, the on-resistance R_{on} and trigger voltage V_{t1} will be doubled at the same time.

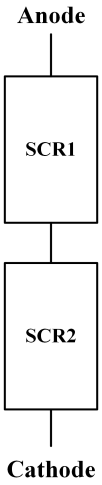


Figure 4.1: Simple Stacking of SCRs.

In reference [44][45], with the aid of bypass resistor, the trigger voltage of the whole cascade SCRs can be kept as the same with the first SCR. The diagram of this kind of stacking is depicted in Figure.4.2.

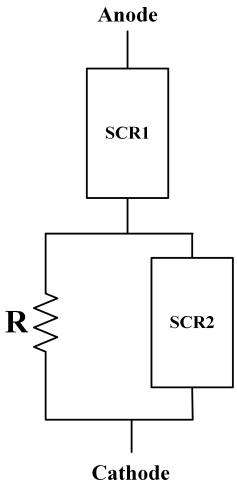


Figure 4.2: Improved Stacking Structure of SCRs to Increase Holding Voltage.

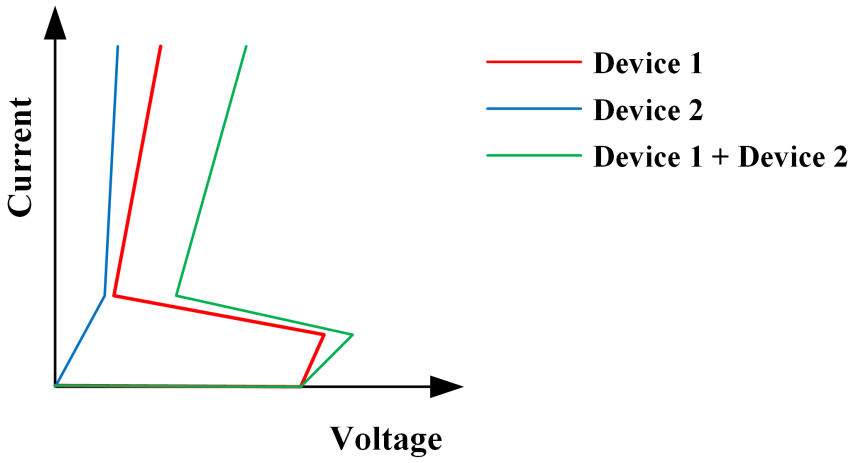


Figure 4.3: Superposed Voltage for Cascade Devices.

The essential of this kind of design can be abstracted into Figure.4.3. The device 1 can be any device requires enhancement on holding voltage, such as a SCR. Then the device 2 should have little influence on the trigger voltage of stacked device 1 + device 2. This means, the device 2 must be in low-resistance state when current level is low so that the increasement on trigger voltage can be minimized. And it requires a steep slope in high current state, which means it should have low on-resistance R_{on}. The device 2 satifying the two requirement can be utilized as the ”padding” device to elevate the holding voltage.

The lower parts of SCR2 with bypass resistor in Figure.4.2 meets the characteristics requirement. Because in low current state, the resistor branch dominates. The increament on trigger voltage ΔV_{t1} of the stacking structure is detemined by:

$$\Delta V_{t1} = I_{t1,1} \times R \tag{4.1}$$

where $I_{t1,1}$ is the trigger current of SCR1 and R is the bypass resistor value. To minimize ΔV_{t1}, the R must to be as small as possible.

Another constraint the bypass resistor R should satsify is:

$$I_{t2,1} \times R \geq V_{t1,2} \tag{4.2}$$

where $I_{t2,1}$ is the failuare current of SCR1 and $V_{t1,2}$ is the trigger voltage of SCR2. This constraint comes from the fact that SCR2 must already be turned on before the current on SCR1 reaching the failure point.

The above calculation is based on the assumption that the bypass resistor has good linearity in high current state, which is not valid in most cases. As a result, it's very hard to make a good estimation for the resistance value in design stage.

Another drawback of this design is relying on external resistors, which will cost extra layout area. More importantly, the current flow through the external resistor will do no contribution to the conductivity modulation inside SCR2.

Above all, we need a more efficient element to act the role of device 2 in Figure.4.3.

4.2 Resistive SCR

The structure in Figure.4.4 is one varition of SCR by making two extra body pick-up TP and TN and connecting them together. The corresponding equivalent circuit is illustrated in Figure.4.5. Two well resistors from AN to TN (R_{NW}) and TP to CP (R_{PW}) are embeded inside the SCR.

Obviously, in low current state, the SCR path from AP to CN remains off and the resistor path along the two resistors dominates. Due to its resistive characteristics at low current state, it is named as Resistive SCR (RSCR)

When the voltage drop between AN to TN is high enough to turn on the P-N junction AP to NW, the parasitic PNP composed by AP, NW and PW will be turned on. So does the NPN on the other side. When both parasitic PNP and NPN were turned on, the SCR path would also be turned on in high current state.

Different from the solution in Figure.4.2, in this RSCR, all the current flowing through the resistive path AN to TN and TP to CP would carry a large amount of carriers. The charge carries will participate the conductivity modulation process in NWell and PWell. As a result, the SCR path in this proposed RSCR structure can be activated at low current level.

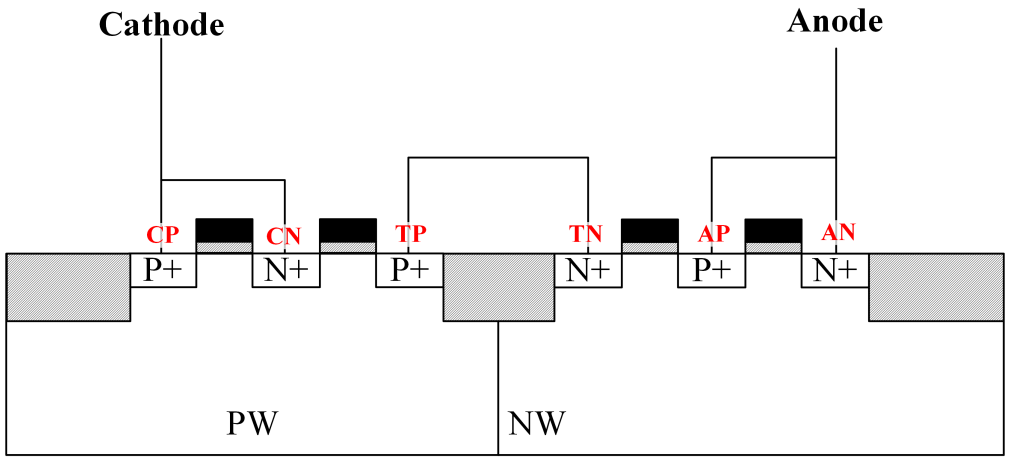


Figure 4.4: Proposed Resistive SCR.

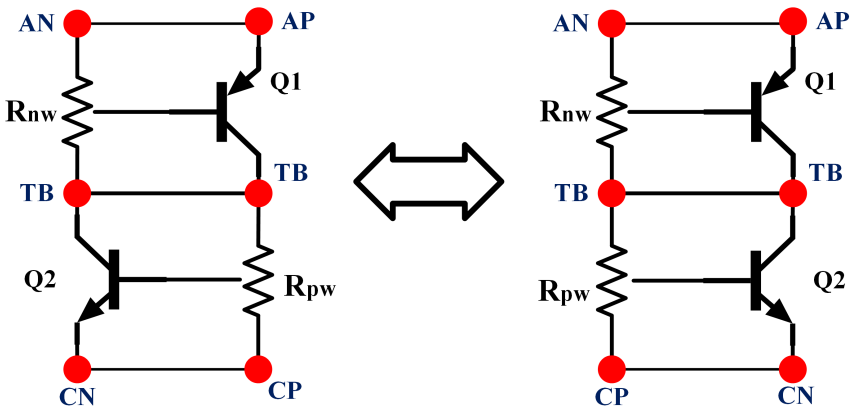


Figure 4.5: Equivalent Circuit of RSCR. The two representations are identical.

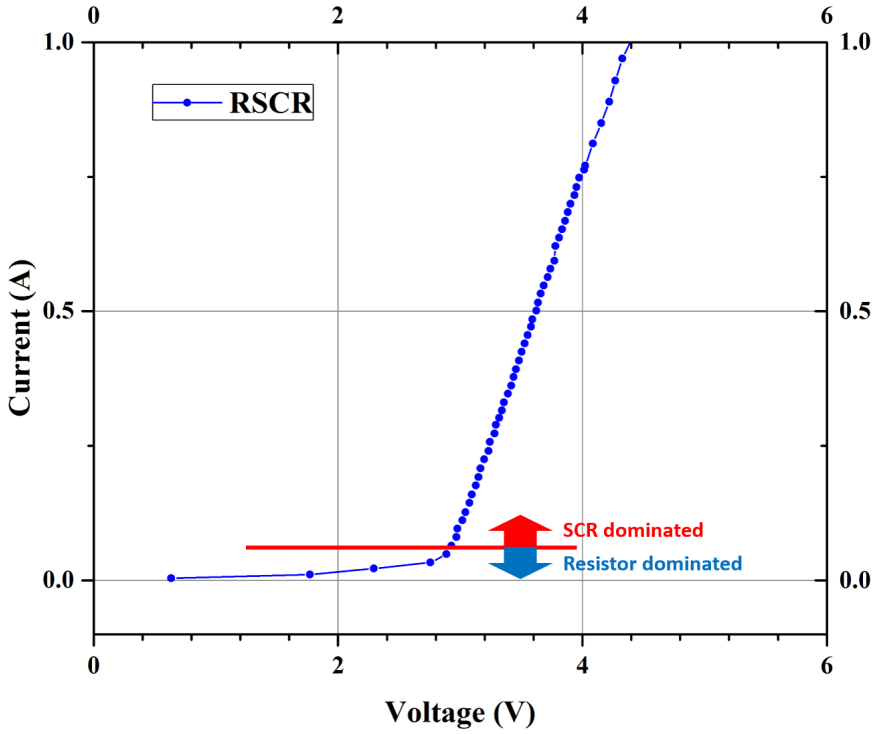


Figure 4.6: TLP Testing Result of RSCR.

Figure.4.6 gives out the TLP test result of single RSCR. A clear turning point can be identified where the transition from resistor to SCR occurs. It's an idea device to be implemented in stacking without any external resistor.

4.3 Stacking with RSCR: A Case for High Speed Interface

4.3.1 Description of Design

With the new designed RSCR, the stacking topology in Figure.4.2 can be transformed into Figure.4.7.

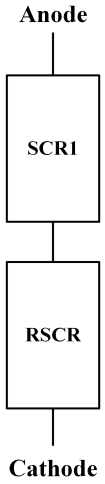


Figure 4.7: Stacking with RSCR.

As an example, one implementation of stacking with RSCR is introdued in this section.

In principle, the failure current of stacking structure is determined by the weakeast element in the cluster. So by no means the stacking structure could improve the current handling capability of the base structure. That's why the stacking structure is not so preferred in many applications because its waste of layout area. In this section, we will prove that the failure current can be improved as well in stacking structure.

The baseline device is a SCR with low capacitance, which is used for high-freqency interface protection. The cross-section of the baseline device is depicted in Figure.4.8

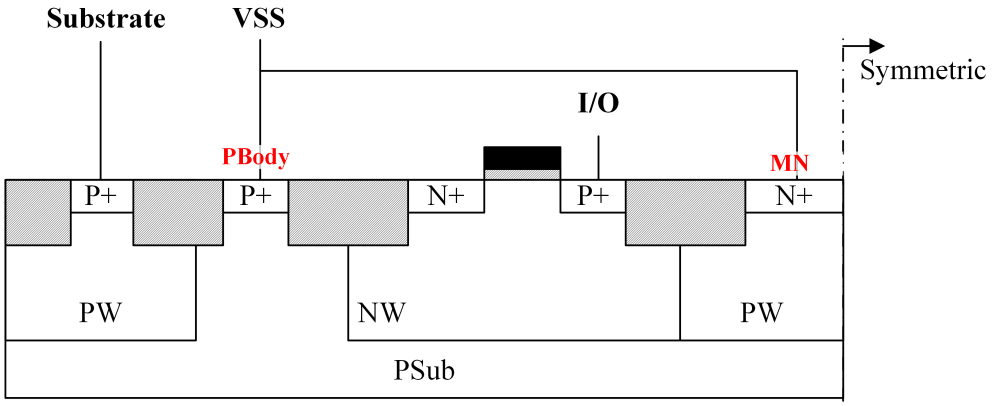


Figure 4.8: Cross-section of Baseline Device Requiring Higher Holding Voltge.

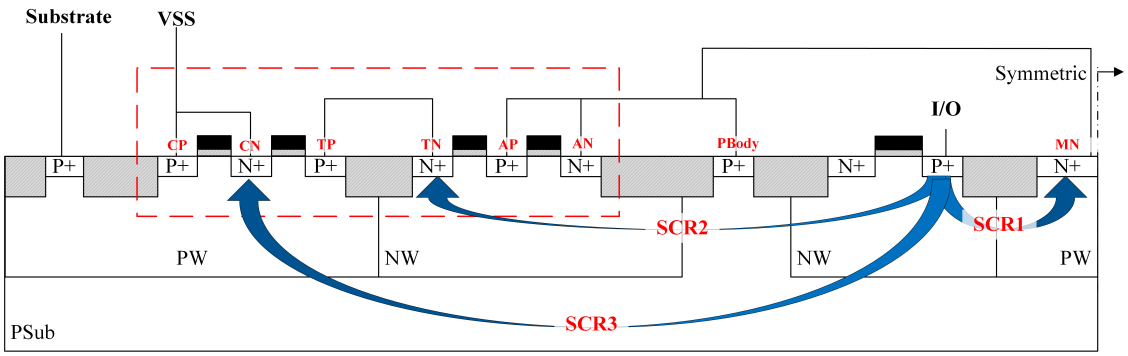


Figure 4.9: Cross-section of Baseline Device Stacked with RSCR.

The stacking structure is shown in Figure.4.9. The special point is, the RSCR and baseline SCR is placed back to back. Thus in addtion of the baseline SCR path SCR1, there exist a medium-range SCR path SCR2 and long-range SCR path SCR3. The equivalent circuit is plotted in 4.10. The SCR1, SCR2 and SCR3 shares the same parasitic transistor Q1 (marked as Q1, Q1' and Q1" in Figure.4.10, respectively). The medium-range and long-range SCR is triggered slower than the baseline SCR SCR1, so their existence has no influence on the trigger voltage. Once SCR1 get triggered, the Q1' and Q1" are turned on at the same time, helping to turn on the SCR2 and SCR3 path. eventually, all SCR paths will participate in current conduction. Due to longer base length, the holding voltage of SCR3 is much higher, which would not affect the enhancement of holding voltage through RSCR.

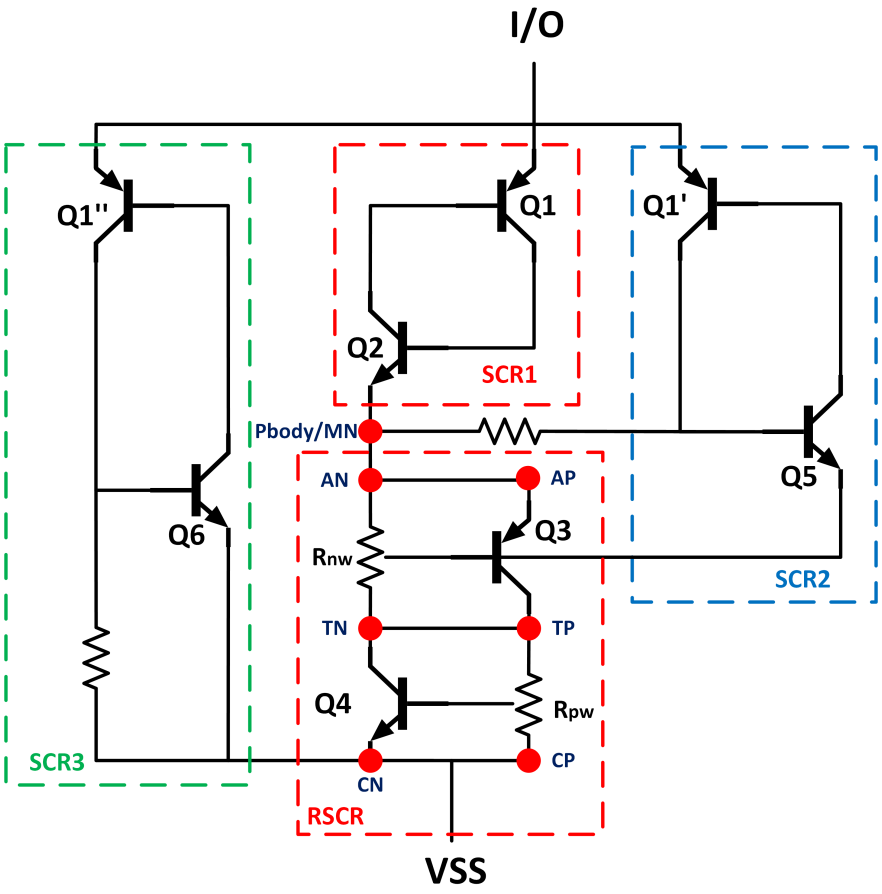


Figure 4.10: Equivalent Circuit of Baseline Device Stacked with RSCR.

4.3.2 Simulation Analysis

In order to verify the structure before tapeout, the quasi-stationary simulation is conducted first to investigate the behavior of the stacking device under different current level. The current distributions are depicted in Figure.4.11. When current is around 10μA/μm, the SCR1 path (from I/O to MN) in Figure.4.9 is triggered, while RSCR still working in resistor mode. When current comes

to 1mA/μm, the RSCR are turned on, which raising the overall holding voltage between I/O and VSS. In Figure.4.11c, the current rises to 20mA/μm and all parasitic SCRs are in on state.

The ratio of current through path SCR1 and SCR2+SCR3 are extracted from simulation and plotted in Figure.4.12. Obviously, the parasitic SCR path SCR2 and SCR3 in Figure.4.9 only conduct current when current level is high, would not affect the trigger characteristics of original path SCR1. Also, with multiple current path, the overall robustness can be improved.

Small signal AC analsys is conducted as well to extract the capacitance information. The capacitance vs. freqency is plotted in Figure.4.13. Even with extra current path, the capacitance of the device didn't rise at all. To the contrary, the capcitance per unit width decreased a little bit due to the cascade structure.

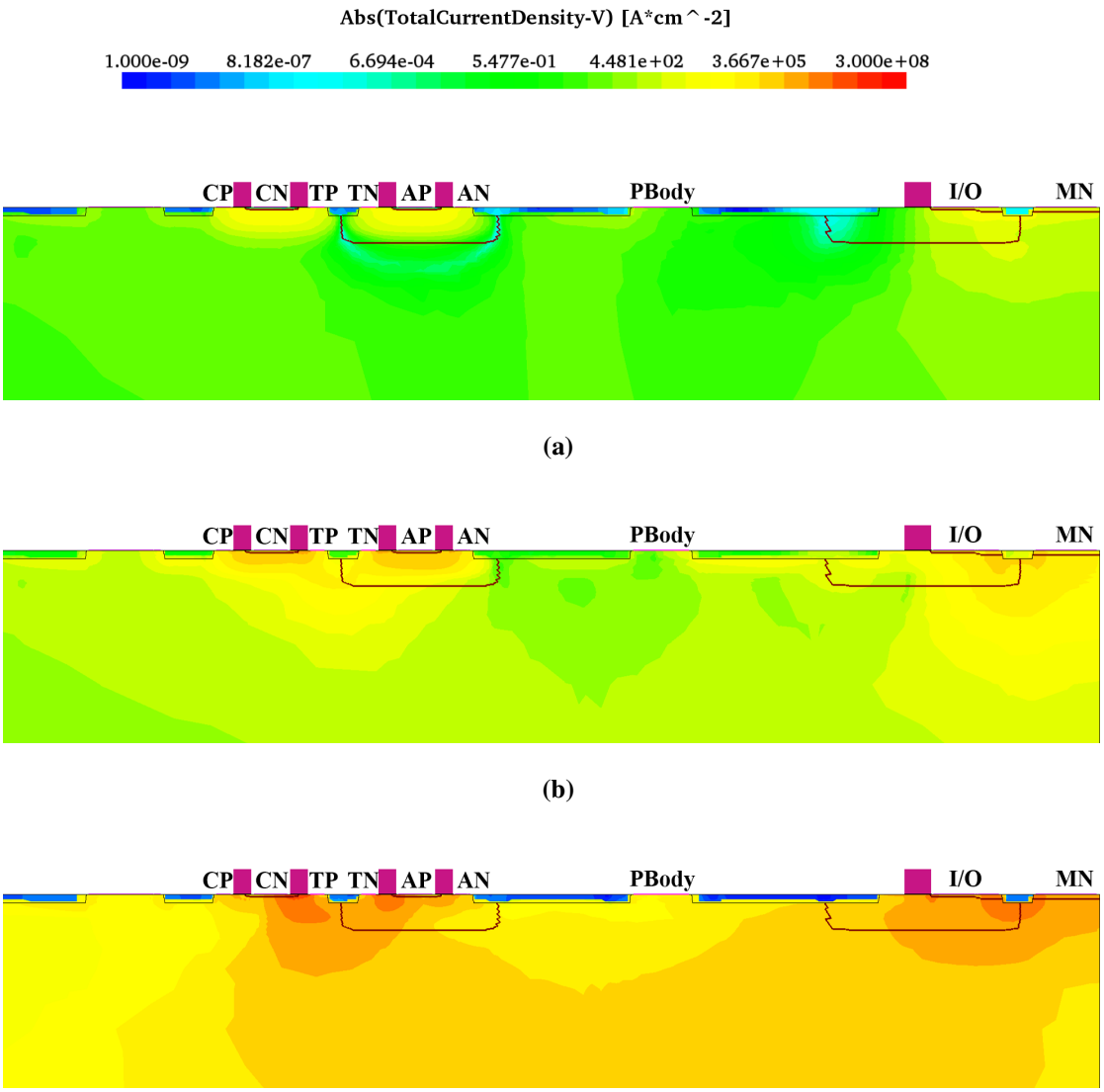


Figure 4.11: Current Distribution at (a) 10μA/μm (b) 1mA/μm (c) 20mA/μm.

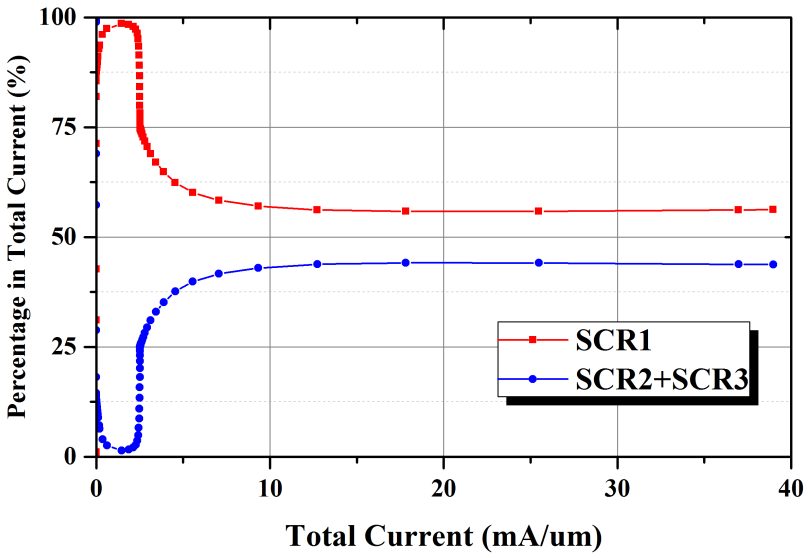


Figure 4.12: Percentage of Current through Different Paths in Total Current.

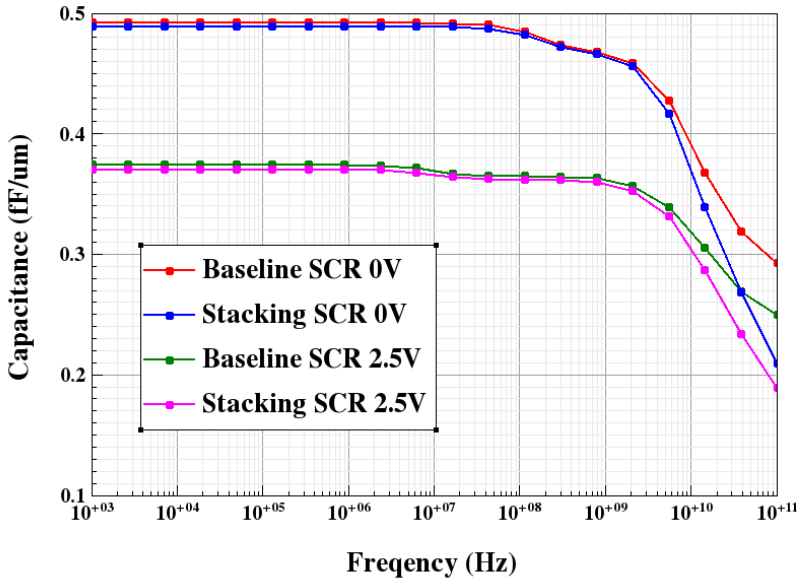


Figure 4.13: Capacitance per Unit Width Extracted from AC Simulation.

4.3.3 Test Results and Analysis

The baseline SCR and stacking struture are fabricated on a 28nm CMOS process. The total width of both structures is 56μm. The DC sweeping result is plotted in Figure.4.14, which proves the DC breakdown voltage of the stacking structure is solely determined by the baseline device, independent from RSCR.

In Figure.4.15, the regular TLP test result is plotted. The pulse with is 100ns and rising time is 2ns. Leakage test condition is set to 3V. The on-resistance Ron is fitted linearly after the holding point. The baseline SCR is 2.5Ω and stacking SCR is 2.1Ω. Benefited from the extra current path, the stacking SCR not only has lower Ron but also higher failure current.

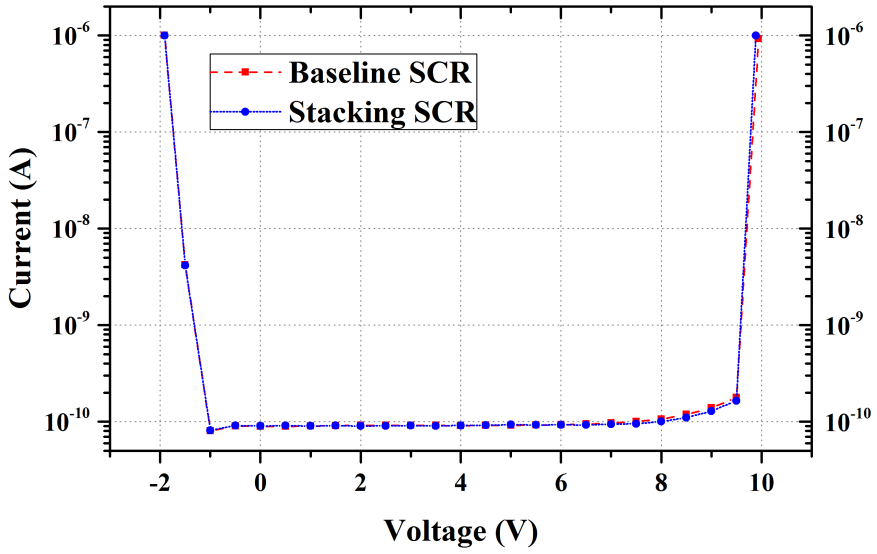


Figure 4.14: DC Sweeping Result.

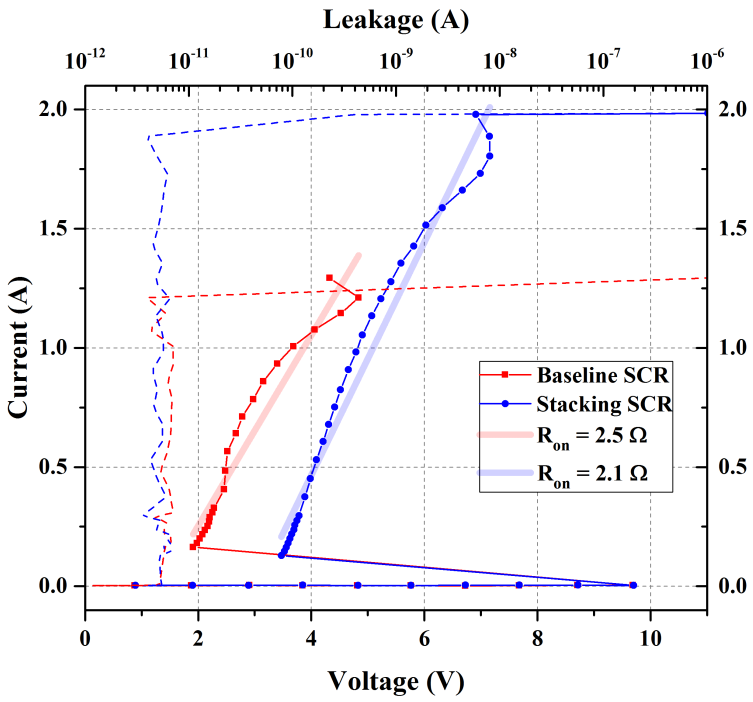


Figure 4.15: 100ns Regular TLP Test Result.

The vfTLP test with 10ns pulse width and 100ps rising time is also conducted. The result is summarized in Figure.4.16. The scatter line in Figure.4.16 is the overshoot voltage vs. VFTLP current. By introducing the RSCR, the stacking SCR would have a bit higher overshoot voltage. Similar to the regular TLP result, the clamping voltage in sampling window of stacking SCR is higher than the baseline SCR, with the same trigger voltage. The failure current level of the stacking SCR is also higher than the baseline device.

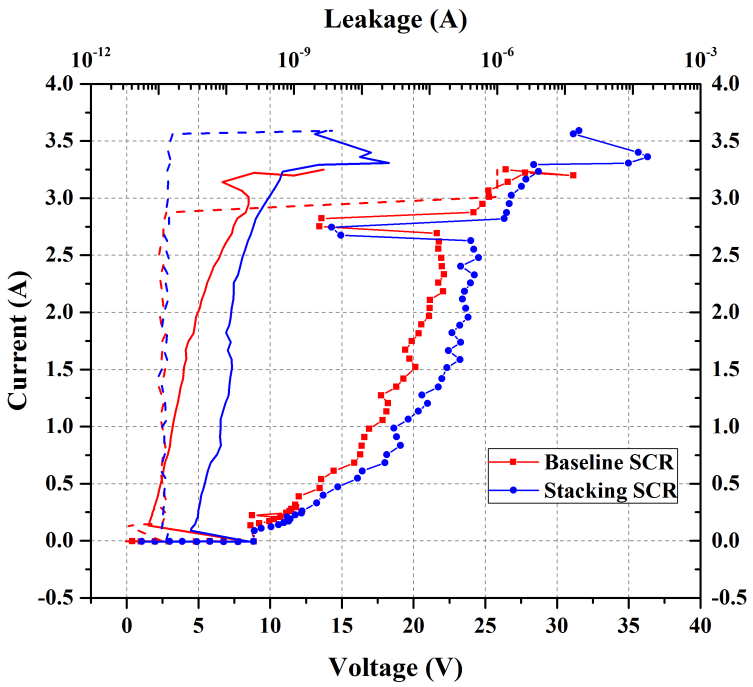
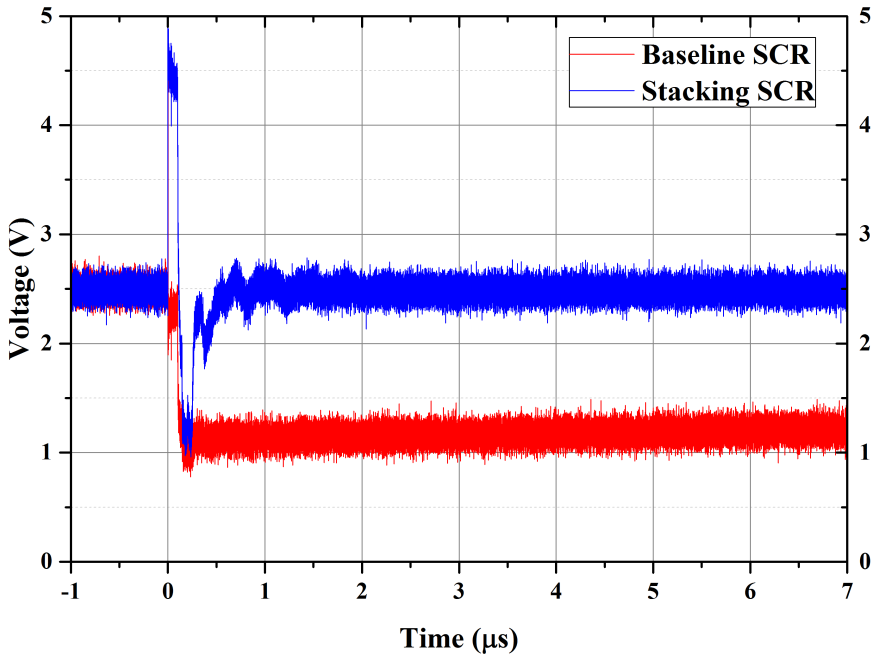
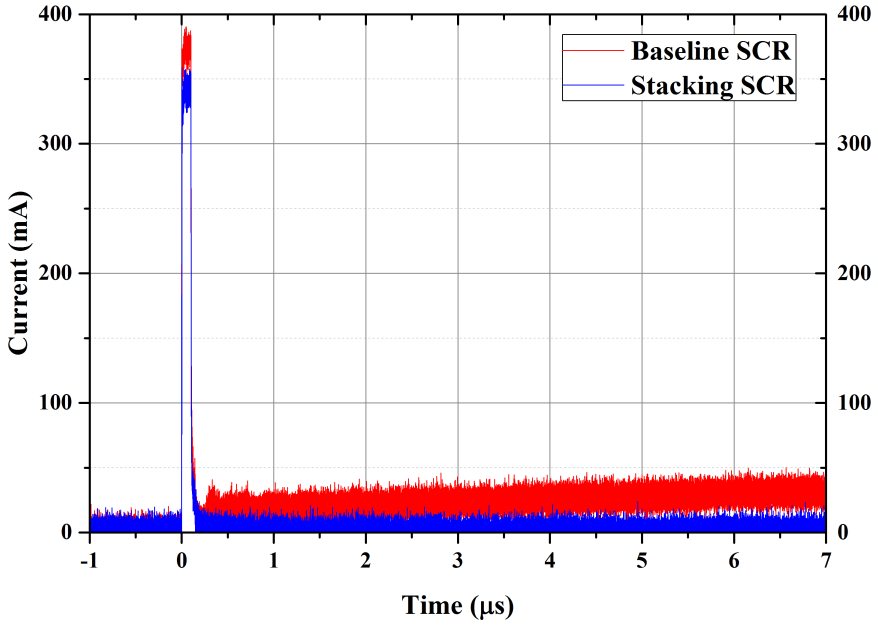


Figure 4.16: vfTLP Test Result: Overshoot Voltage(Scatter Line), Clamping Voltage(Solid Line) and Leakage Current (Dash Line).

The latch-up test is performed with 2.5V operation voltage. The 20V TLP pulse is applied from 0 to 100ns. The voltage and current waveforms are captured in Figure.4.17. The baseline SCR is latched after TLP pulse, while the stacking structure can recover to off state. The latch-up test result again demonstrate the holding voltage of the stacking structure is indeed enhanced.



(a)



(b)

Figure 4.17: Latch-up Test with 2.5V Operation Voltage: (a) Voltage Waveform and (b) Current Waveform.

4.4 Folded Stacking RSCRs: A Case with Higher Holding Voltage

In previous section, a design case in low-voltage application using single stacking RSCR is introduced. While in some high-voltage applications, higher holding votlage is desired, which in principle can be achieved by stacking more RSCRs. Despite using different configurations, the increment of trigger voltage with stacking RSCR can still be computed using Equation.4.1, where the R should stand for the total resistance value of all stacked RSCR in resistor mode. For a few number of RSCR, R could be small and the increment of trigger voltage ΔV_t can be omitted. With the stacking number increasing, R would become large and ΔV_t cannot be neglected any more.

As a result, a simple and flexible methodology is required to tune the resistance value R for multiple RSCR stacking. One clue is to adjust the distance from AN to TN and CP to TP in Figure.4.4. But this method is limited by the design rule: the distance can't decrease more when reaching the minimal design rule of the distance between different diffusion region.

Another possible solution is change the topology of stacking structure. A test case with 3 stacking RSCRs will be used to explain the machanism.

4.4.1 Folded Stacking Topology

First, using the same concept of creating parasitic long-range SCR between anode and cathode in previous section, topology of the 3-RSCR stacking structure should be as in Figure.4.18. The embedded long-range RSCR will provide higher current handling capability.

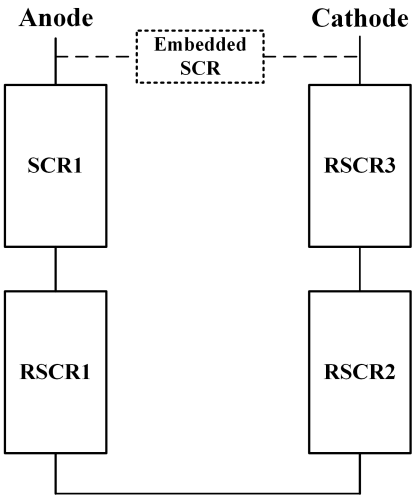


Figure 4.18: Stacking with 3 RSCRs.

By splitting the Anode into AP and AN, Cathode into CN and CP in Figure.4.4, the RSCR can be treated as four-terminal device. Moreover, if the TP and TN are used as a terminal, the RSCR becomes five-terminal device (Figure.4.19). According to the schematics in Figure.4.10, the resistance value from AN to TB is R_{nw}, from TB to CP is R_{pw}. The SCR path is from AP to CN. If stacked using the topology in Figure.4.18, the total resistance R in resistor regime of RSCRs should be:

$$R = 3 \times (R_{nw} + R_{pw}) \tag{4.3}$$

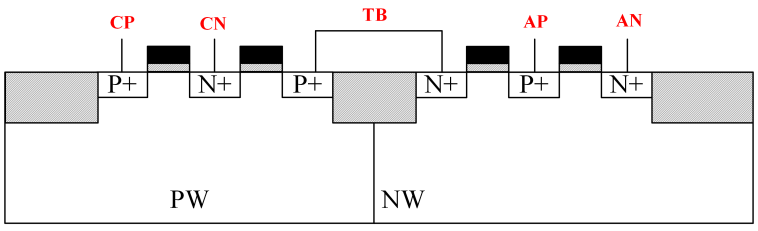


Figure 4.19: Crosssection of 5-terminal RSCR.

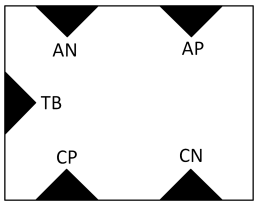


Figure 4.20: Symbol of 5-terminal RSCR.

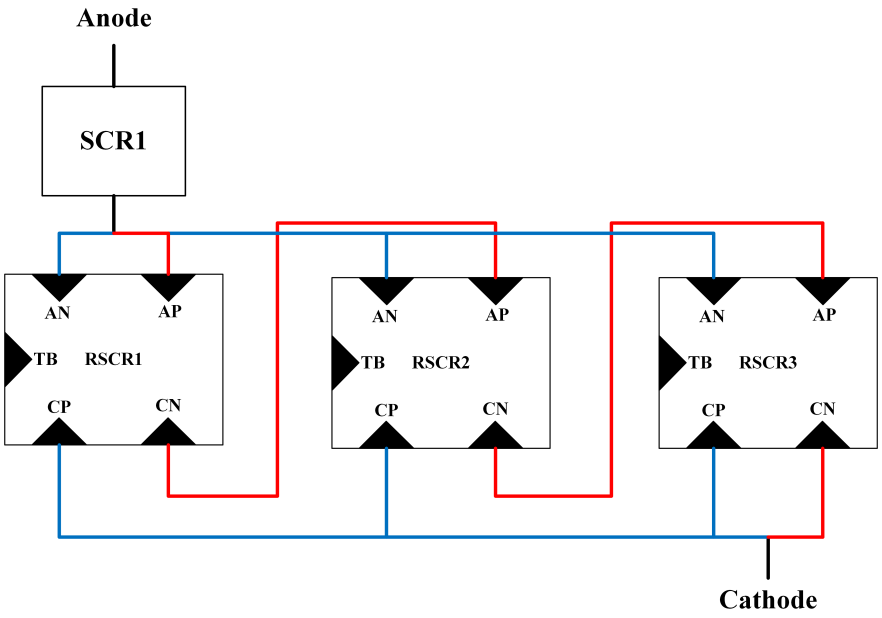


Figure 4.21: Folded Stacking Topology: Type I. Red Line: SCR Path Connection. Blue Line: Resistor Path Connection.

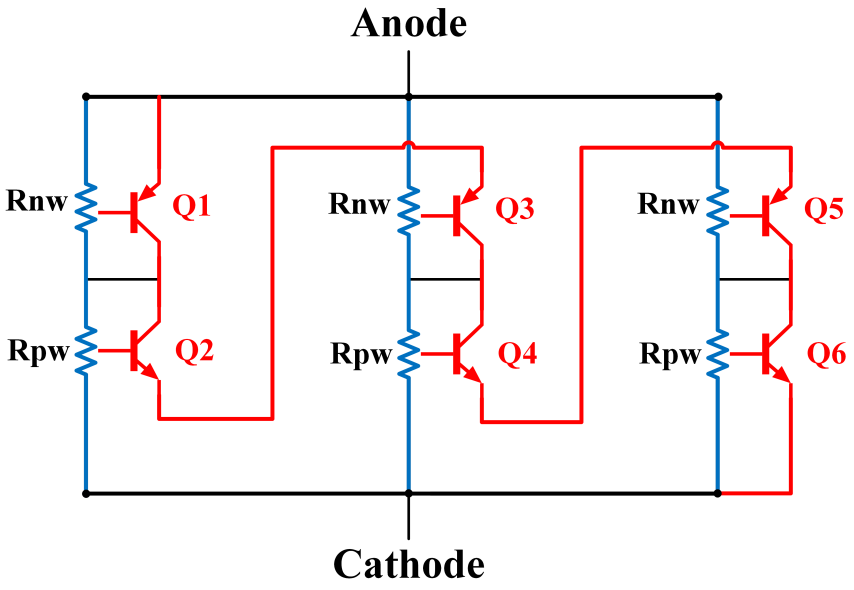


Figure 4.22: Equivalent Circuit of Type I Stacking Topology.

An improved topology is depicted in Figure.4.21 and the equivalent circuit is in Figure.4.22. The resistor paths are put in parallel while keeping the SCR paths in series. For its special connection, this type of stacking is called ”folded stacking”.

The total resistance R contributed by 3 folded stacking RSCRs can be easily calculated as:

$$R = (R_{nw} + R_{pw})/3 \tag{4.4}$$

which is only $1/3$ of the single RSCR. However, too small resistance value might violate the constraint in Equation.4.2.

Another possible risk is the unbalanced trigger. With this connection, the RSCR3 in Figure.4.21 suffers the highest voltage drop between AN to CN, which might unintentially trigger the NPN path

from AN to CN (Q6 in Figure.4.22). The snapback of parasitic NPN path can prevent RSCR1 and RSCR2 from triggering, in which case the RSCR1 and RSCR2 are not fully utilized.

The simulated current distribution at trigger point in Figure.4.23 demonstrate the possible risk described above, in which case only RSCR3 is turned on.

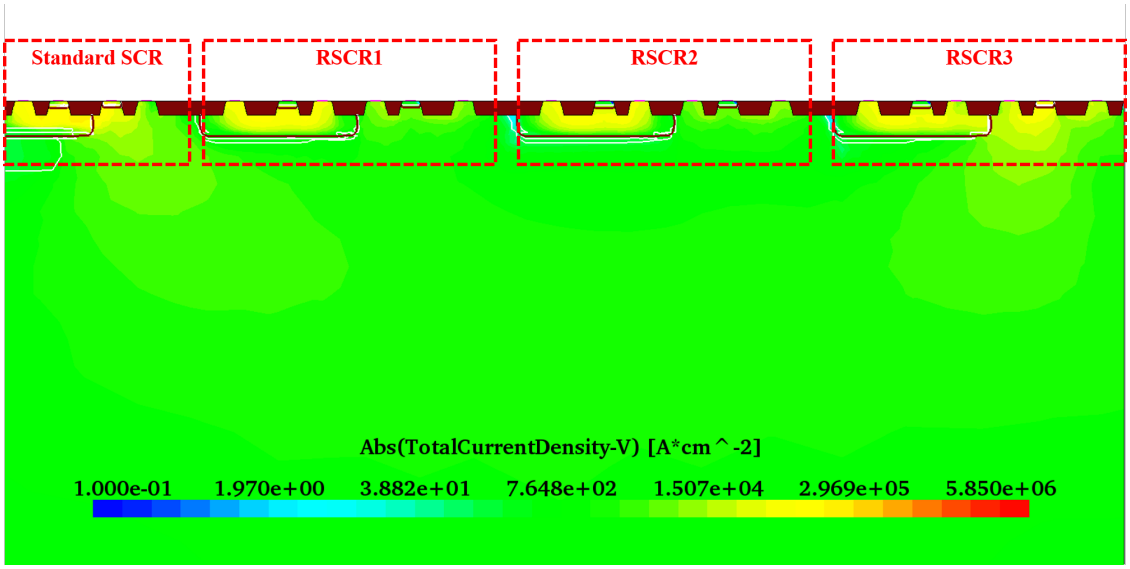


Figure 4.23: Current Distribution of Stacking SCR with Type I Connection in TCAD Simulation at 500μA/μm.

An improved topology can provide moderately reducing resistance value. The connection is plotted in Figure.4.24 and the equivalent circuit is in Figure.4.25. In off state, only the resistor paths conduct current. So the network of resistors along resistor paths can be extracted in Figure.4.26. Obviously the total resistance R can be computed as:

$$R = (R_{nw} + R_{pw}) + 2\frac{R_{nw}R_{pw}}{R_{nw} + R_{pw}} \tag{4.5}$$

which is higher than the Type I connection but still much smaller than the regular connection in Figure.4.18.

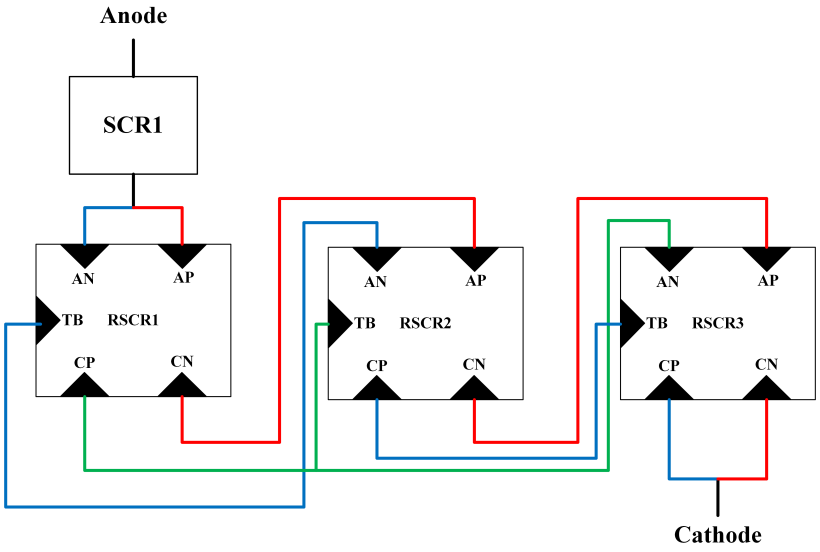


Figure 4.24: Folded Stacking Topology: Type II.

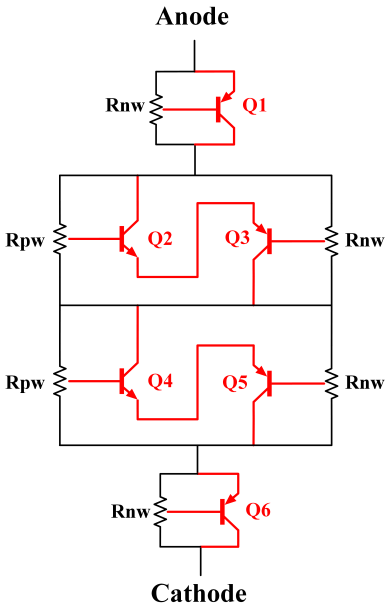


Figure 4.25: Equivalent Circuit of Type II Stacking Topology.

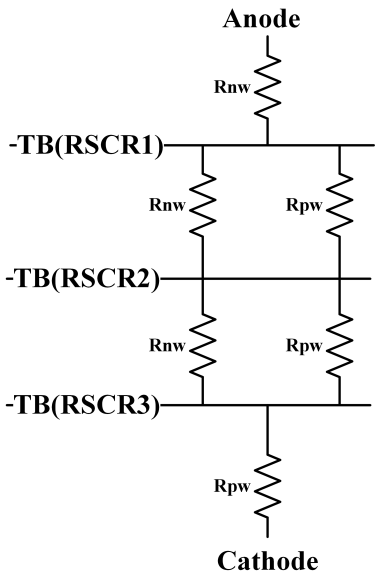


Figure 4.26: The Network of Resistor in Type II Connection.

Unlike the type I, this type II connection can ensure all the RSCRs triggered more uniformly. For example, in Figure.4.25, if NPN Q6 is turned on first, the high current through the resistors above will generate enough voltage drop to turn on the Q1-Q5. The same process works for Q1 and any other parasitic transistors, which guarantee all the RSCRs can be triggered before the current on any one device become too high.

The simulated current distribution is plotted in Figure.4.27. Comparing to the type I in Figure.4.23, at the same input current level (500μA/μm), the three stacked RSCRs are evenly triggered by using type II connection.

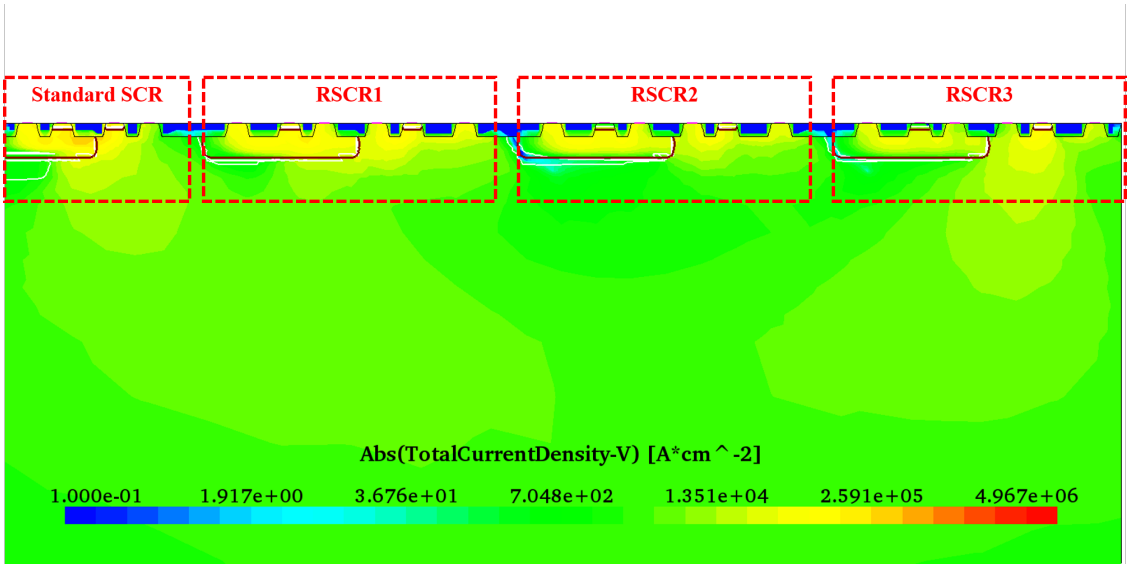


Figure 4.27: Current Distribution of Stacking SCR with Type II Connection in TCAD Simulation at 500μA/μm.

4.4.2 Test Results and Analysis

The three types of topoloies described in previous sections are fabricated on a 0.18μm BCD process.

The DC sweeping is performed on each device. The result is summarized in Figure.4.28. All the three stacking structure has the same DC breakdown voltage with the non-stacked one, proving the stacking of 3 RSCR cells has no influence on the breakdown voltage.

100ns regular TLP test are peformed. The results are compared in Figure.4.29a. By introducing the long-range parasitic SCR path, all the three stacking stucture has better I_{t2} performance than the

non-stacked SCR. One observation in Figure.4.29a is the type I stacking structure shows apparent multiple trigger. This is for the unbalanced trigger as described in previous subsection. A close look at the trigger point in Figure.4.29b shows that the type I has fewest impact on the trigger voltage, followed by the type II stacking structure. For conventional stacking of 3 RSCRs, the trigger voltage shifted by 5V, which might not be acceptable in the applications with narrow design window.

Therefore, a combination of type I connction and type II connection can be helpful to reduce the resistance *R* along resistor path, as well as the increment of trigger voltage.

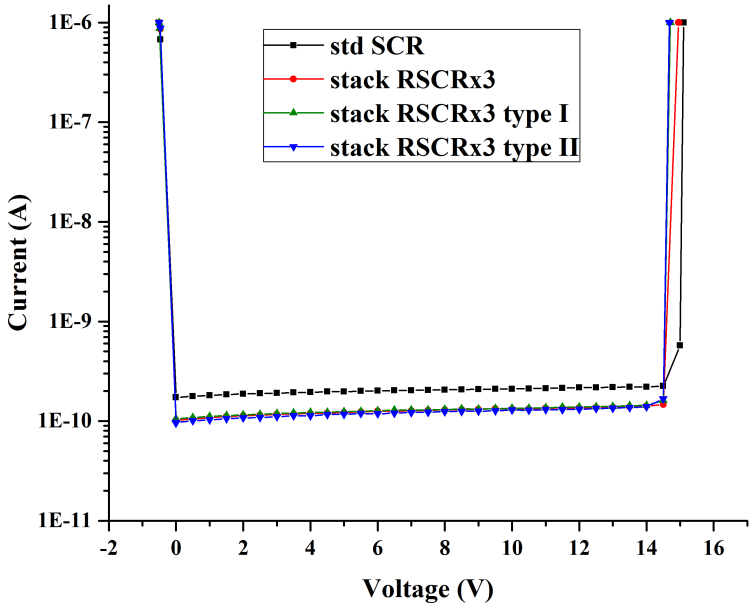
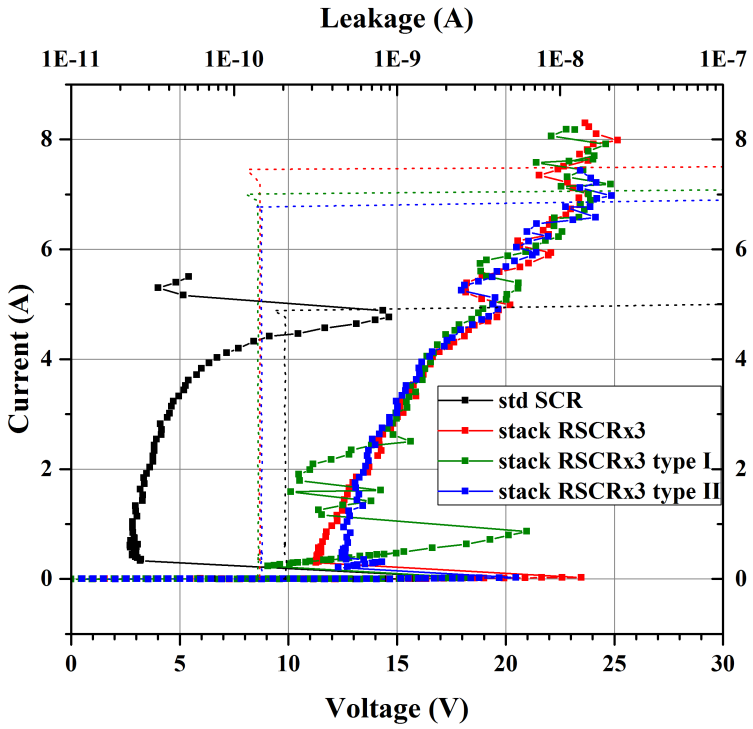
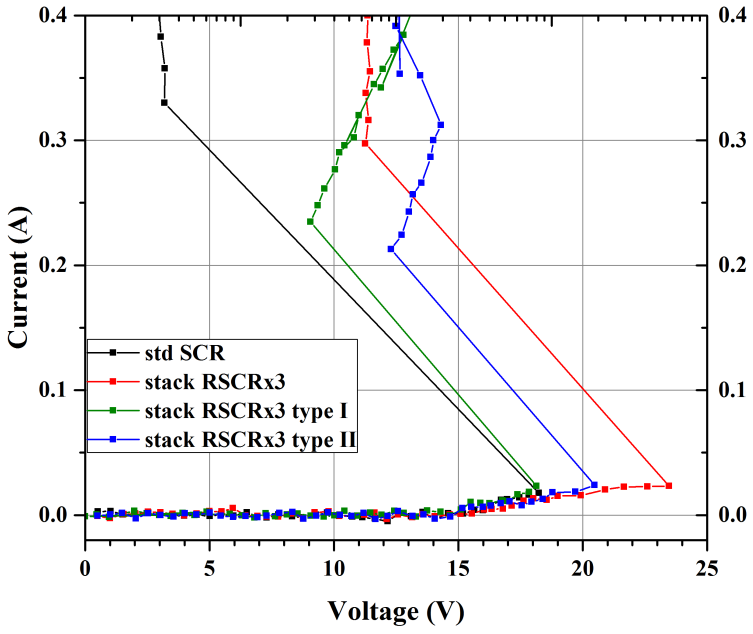


Figure 4.28: The DC Wweeping Result.



(a)



(b)

Figure 4.29: TLP Testing Results. (a) Full-view and (b) Zoom-in View at Trigger Point.

4.5 Conclusion

In this chapter, the essential in stacking structure design is emphasized. A new perspective on the stacking theory is discussed, based on which a new device structure RSCR is created to be used as a ”padding” device. The holding voltage is improved with this padding device without changing an other paramters related to design window. With the aid of extra current path along long-range SCR, the ESD robustness is enhanced at the same time. The layout area is fully utilized. Another experiment on optimizing the stacking topology in this chapter provide a route to achieve even higher holding voltage by stacking of multiple RSCR. The new topology allows reduce the side effect of stacking on trigger voltage without violating the design rule.

The theory and design of stacking devices in this chapter is independent from any technology, which can be easily implemented on other process.

CHAPTER 5
SCR BASED ACTIVE CLAMP

Power clamp plays a critical role in ESD protection network. For integrated circuits using whole-chip ESD protection strategy, the power clamp provides a common current path for pins in the same power domain[46]. In order to avoid the power clamp becoming the bottleneck of overall ESD performance, it requires the power clamp to be able to handle as much as possible current with low voltage overstress. Considering the possibility of latch-up between power rail and ground caused by power clamp itself[47], the power clamp should either have higher clamping voltage over operation voltage or be able to shut down efficiently after ESD event ended.

The power clamp design can be analyzed in different parts. Generally, the power clamp can be categorized into two parts: the controlling cell and discharge cell. The controlling cell is an active circuit which turns on/off when ESD event occurs/ends. Controlling cell could be RC-based[46][48][49] or a series of diode cluster[50], depending on the applications. In most previous designs, a big MOSFET is usually used as the discharge cell in power clamp, on which the current density is low to prevent the MOSFET goes into bipolar mode. Some also tried to improve the efficiency of discharge cell by using controllable SCR[51], but the SCR itself has risks of latch-up if controlling circuit cannot turn-off the SCR.

In this chapter, a new design of power clamp using SCR as the discharge cell will be proposed. Mixed-mode simulation is used to verify the design.

5.1 Description of Design

This power clamp is based on a controllable SCR with two controlling terminals (TN and TP).

Considering the characteristics of the SCR, there would be some issues when use it as discharge cell:

- Turn-on speed: Even with trigger circuit, the SCR still suffers from a slow turn-on speed comparing to the MOSFET, which lead to high overshoot voltage under ESD stimulus.
- Latch-up risk: The low clamping voltage might lead to latch-up in power-on situation.
- High driven current required: Different from the voltage-controlled MOSFET, the SCR is essentially current-controlled device. Large driven current is required to turn on and off the SCR.

To resolve the problems above, the SCR must be modified before implemented as discharge cell.

5.1.1 Trigger Cell

The proposed trigger circuit is shown in Figure.5.1.

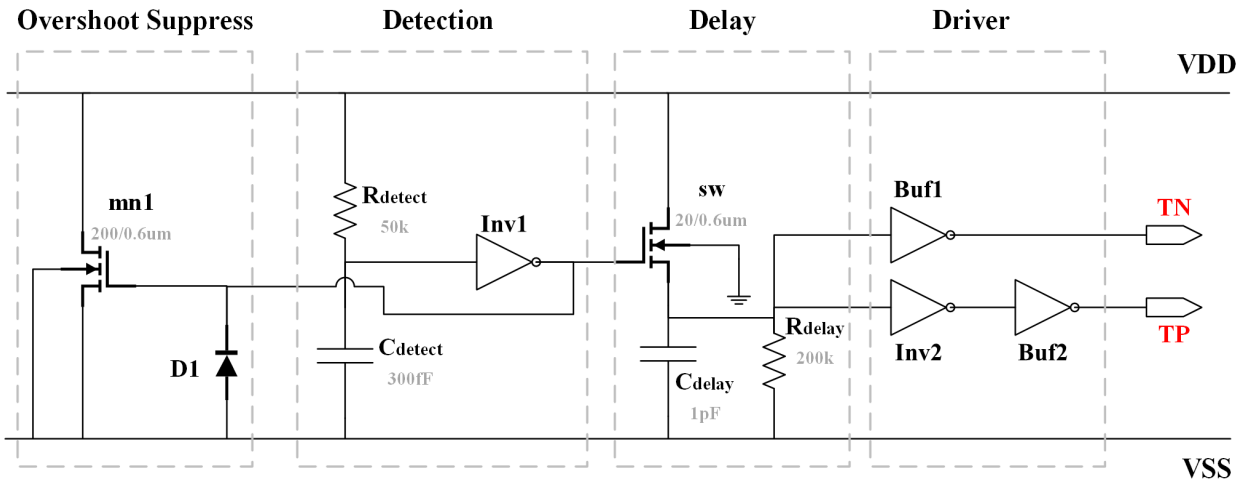


Figure 5.1: Trigger Circuit.

The trigger circuit is consisted of four parts:

- Detection circuit
- Delay timer
- Driver
- Overshoot-Suppress circuit

5.1.1.1 Detection Circuit

There are two categories of detection method for ESD event: edge-trigger and voltage/current-level-trigger.

The edge-trigger RC network (Figure.5.2a) is able to detect the rising edge of ESD pulse and send out a high signal for a short period of time. Therefore this kind of circuits are always implemented together with an additional delay network.

The problem of this detection method is that the magnitude of output signal varies with rising time and level of ESD pulse:

$$V_{out} = RC\frac{dV}{dt} \tag{5.1}$$

which constrained by:

$$V_{th} < V_{out} < V_f \tag{5.2}$$

where V_{th} and V_f represent the threshold voltage and failure voltage of next stage, respectively.

In sub-micro process, the ratio of V_f to V_{th} is usually very small, while the maximum to minimum of $\frac{dV}{dt}$ for different ESD event could be larger than 20, which leaves a dillemma for designs of R, C values. One solution is to put a transmission gate after the detection circuit to loose the constraints of V_f. However, it can't eliminate the risks of mis-trigger caused fast-rising noise.

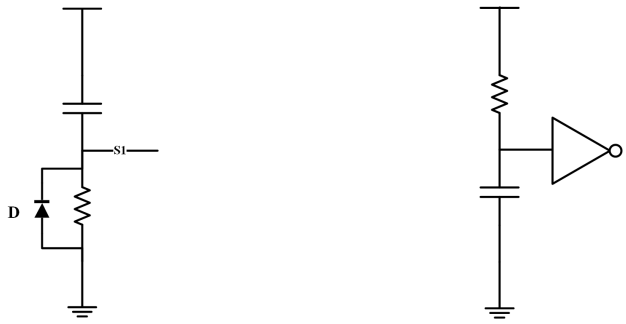


Figure 5.2: Detection Circuits for ESD Event: (a)Edge Trigger and (b)Level Trigger.

Level-trigger circuit (Figure.5.2b) is immune to mis-trigger caused by noise. The criteria to sense ESD can be computed as:

$$V_{ESD} - V_{DD} > V_{th} \tag{5.3}$$

where V_{ESD} is the voltage on power line during ESD event and V_{DD} is the original voltage on power line. V_{th} is the threshold voltage of successive stage.

Another merit of the RC level-trigger network shown in Figure.5.2b is it can sustain the turn-on signal for a while, which could guarantee sufficient time for the ESD devices in following stage to discharge.

However, when the SCR is used as discharge device, the voltage is likely to drop below V_{DD} during discharge process, leading to negative voltage over the resistor. In such case, the detection circuit is likely to send out turn-off signal before discharging completed.

Considering of this problem, I took the function of delay out from the detection circuit. Then the R_{detect}, C_{detect} in detection circuit can be set smaller.

5.1.1.2 Delay Circuit

The delay circuit in Figure.5.1 is consisted of a NMOS switch, a cap and a high-res resistor.

Once detection circuit sends out turn-on signal, the switch sw will turn on and C_{delay} will get charged quickly. After detection circuit reset, the C_{delay} will discharge through R_{delay}.

A reliability risk here is the voltage on C_{delay}. Since C_{delay} is charged by voltage on power line (V_{ESD}) through switch sw, when V_{ESD} is too high, the cap and gate in following stage will get damaged.

To ease the parameter setting, the voltage on cap can be estimated first. Suppose during ESD event the voltage on power line is $\overline{V}_{ESD}$. Average on-resistance of NMOS sw is $\overline{R}_{ch}$.

The on-time of detection circuit is roughly:

$$t_{detect,on} = R_{detect}C_{detect} \ln\left(\frac{\overline{V}_{ESD} - V_{th1}}{V_{DD}}\right) \tag{5.4}$$

where V_{th1} is the threshold voltage of inverter Inv1. Then the peak voltage V_p on cap V_{delay} is:

$$\begin{aligned} V_p &= \overline{V}_{ESD}\left[1 - \exp\left(-\frac{t_{detect,on}}{\overline{R}_{ch}C_{delay}}\right)\right] \\ &= \overline{V}_{ESD}\left[1 - \left(\frac{\overline{V}_{ESD} - V_{th1}}{V_{DD}}\right)^{-\frac{R_{detect}C_{detect}}{\overline{R}_{ch}C_{delay}}}\right] \end{aligned} \tag{5.5}$$

The V_p must satisfy:

$$eV_{th2} < V_p < V_f \tag{5.6}$$

where V_{th2} is the threshold in next stage and V_f is the failure voltage at this node.

The ratio r in Equation.5.7 can be adjusted to achieve the constriants in Equation.5.6.

$$r = \frac{R_{detect}C_{detect}}{\overline{R_{ch}}C_{delay}} \tag{5.7}$$

The effective delay time can be computed as:

$$t_{delay} = R_{delay}C_{delay} \ln\left(\frac{V_p}{V_{th2}}\right) \tag{5.8}$$

5.1.1.3 Driver

The SCR is enssentially composed by two current controlled bipolar devices, so it requires a large amount of current to control. Delay circuit alone is not capable to provide so high current. As a result driver is required. Moreover, because the structure has two complementary controlling terminal TN (negative) and TP (positive), an extra inverter is put before TP to guarantee TN and TP output inverse signal.

Note that Buffers are used before both TN and TP to decouple these two terminals to avoid interfere from loads.

5.1.1.4 Overshoot Suppress circuit

The multiple stages design would lead to delay of signal from detection circuit to controlling output. And the SCR also need some time to switch to on-state. Before the discharge SCR works, overshoot would occur on power line. To mitigate the overshoot, an extra discharge NMOS is put directly after detection cell, which could achieve fast conduction before SCR turned on.

5.1.2 Discharge Cell

The basic element for discharge cell is similar to the RSCR structure presented in previous charpter. The device structure is shown in Figure.5.3.

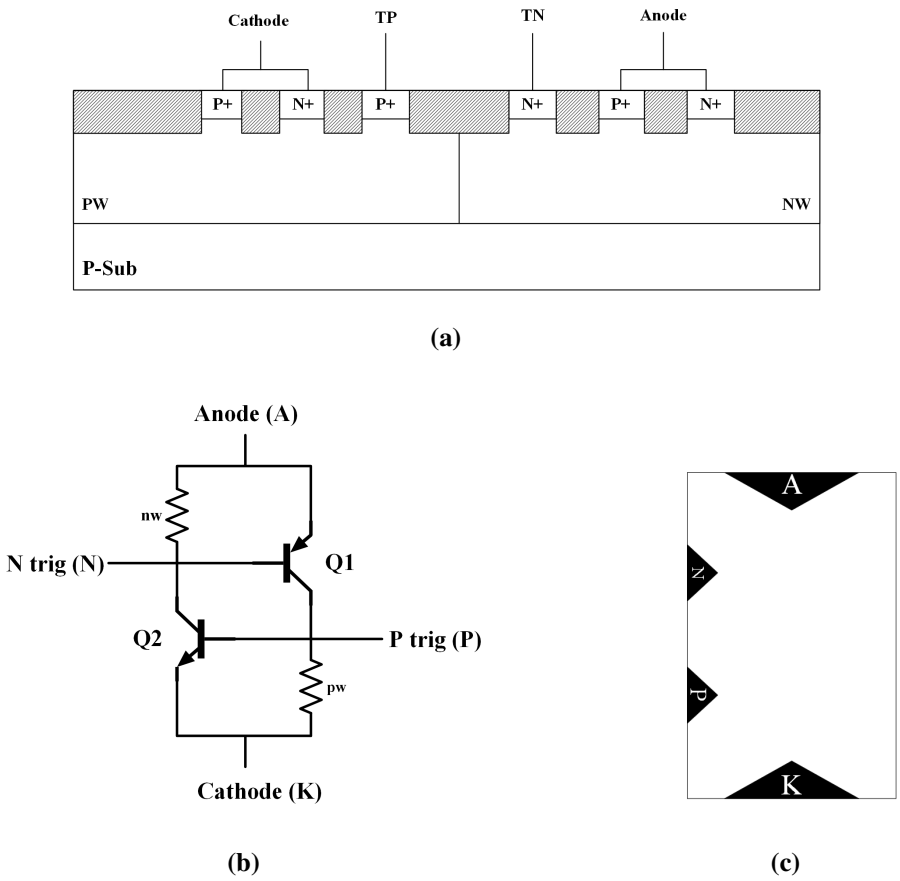


Figure 5.3: Controllable SCR (a)Cross-section, (b)Equivalent Circuit and (c)Symbol.

As shown in Figure.5.3b, to turn on the SCR, set TN to low and TP to high. Then Q1 and Q2 can be turned on, positive feedback established. To turn off it, set TN to high and TP to low, the emitter-base junction of Q1 and Q2 will get short and both will be turned off.

However, to drive such a huge device, it requires a huge amount of current on TN and TP. The MOSFET in active mode is hard to provide such large current as for its relatively high channel resistance.

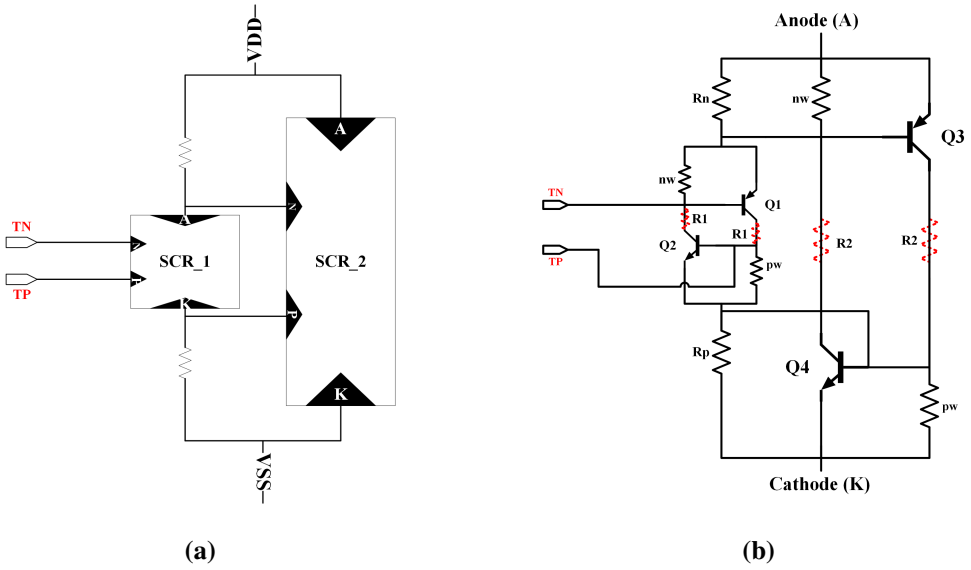


Figure 5.4: Proposed SCR-based Discharge Cell (a)Connection and (b)Equivalent Circuit.

Instead of driving the large discharge SCR directly, the new design uses trigger circuit to drive a small SCR first. Then, the small SCR is able to drive the large SCR. In this way, the burden on driver can be relaxed.

The connection and equivalent circuit is shown in Figure.5.4. In Figure.5.5 the current flowing directions are plotted for turn-on and turn-off process.

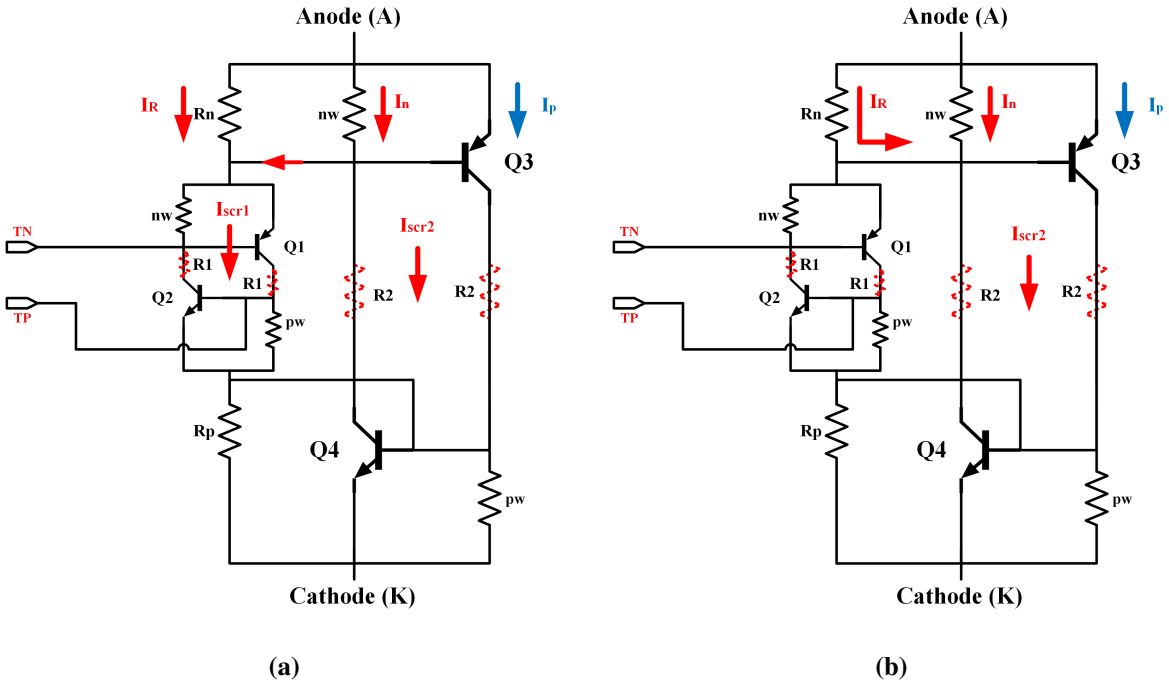


Figure 5.5: Equivalent Circuit for (a)Turn-on Process and (b)Turn-off Process.

To understand the behavior of this discharge cell and find the suitable parameters, a simple derivation is made as following.

First a simple model is shown in Figure.5.6 to describe the behavior of SCR. where V_d stands for forward voltage drop of a diode (0.6V - 0.8V). I_c is the minimal current required to sustain conductivity modulation inside SCR with unit width(1um). R_{on} is the on-resistance of SCR with unit width.

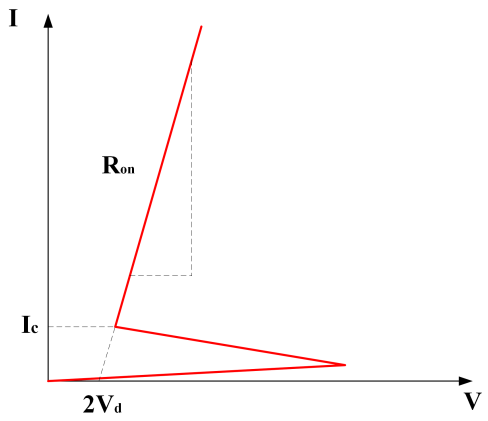


Figure 5.6: Simple IV Characteristics for SCR

Then the voltage drop of a SCR in on state can be represented as:

$$V_{SCR} = 2V_d + IR_{on} \tag{5.9}$$

In the following derivation, assume $R_n = R_p = R$.

Suppose the width of small SCR1 in Figure.5.4a is A_1 and SCR2 is A_2. Then their on-resistance (R_1 and R_2 in Figure.5.5) should satisfy:

$$R1 = \frac{A_2}{A_1} R_2 \tag{5.10}$$

Before SCR2 turned on, the current I_p in Figure.5.5a is extremely small comparing to I_R and I_n. So all the current will flow through either external resistor R_n or well resistance R_{nw} (so as to R_p and R_{pw}). The target of trigger current is set to I_t for this cell. Then before trigger, $I_t = I_R + I_n$.

When the voltage drop over R_n and R_{nw} is larger than V_d, SCR2 will be turned on. Therefore the lower bound of external resistor value R can be computed:

$$(R//R_{nw})\, I_t \geq V_d$$
$$\Rightarrow R \geq \frac{V_d}{I_t - V_d/R_{nw}} \tag{5.11}$$

In turn-off process, SCR1 will be turned off by trigger circuit. The original loop gain of SCR2:

$$\beta_{Q3}\frac{R_{nw}}{R_{nw}+r_{eb3}}\beta_{Q4}\frac{R_{pw}}{R_{pw}+r_{be4}} \tag{5.12}$$

will become:

$$\beta_{Q3}\frac{R_{nw}//R_n}{R_{nw}//R_n+r_{eb3}}\beta_{Q4}\frac{R_{pw}//R_p}{R_{pw}//R_n+r_{be4}} \tag{5.13}$$

To turn off the SCR, the loop gain is expected to be lower. Obviously, small value of Rn and Rp can achieve this target, which constrained by inequation Eq.5.11.

Another parameter pending to be determined is the size of SCR1 and SCR2.

When both two SCRs entered into turn-on state (holding state), the voltage on the two branch is:

$$\underbrace{2V_d + 2V_d + I_{scr1}R_1}_{\textbf{SCR1 branch}} = \underbrace{2V_d + I_{scr2}R_2}_{\textbf{SCR2 branch}} \tag{5.14}$$

To guarantee the large SCR2 work properly, I_{scr1} and I_{scr2} should satisfy:

$$I_{scr1} \ll I_{scr2} \tag{5.15}$$

The total discharge current $I_d = I_{scr1} + I_{scr2}$.

Combining Eq.5.14 and Eq.5.10 yields:

$$\frac{A_2}{A_1} \gg \frac{1}{1+\frac{4V_d}{I_d R_1}} \tag{5.16}$$

Eq.5.16 indicates the A_2 should be as large as possible to provide sufficient ESD protection capability. Note that another constraint for width A_2 is:

$$R_{nw} I_t \geq V_d \tag{5.17}$$

A_2 is included in R_{nw}

The design flow of the discharge cell is summarized in following list:

1. Determine design specification, including trigger current I_t, maximum discharge current I_d.
2. Using simulation or testing data to find on-resistance and well resistance of SCR per unit width.
3. Using simulation tool to find the maximum width A_1 of SCR1 that the trigger circuit is able to drive.
4. Determine the width of discharge SCR2 according to inequation in Equation.5.16.
5. Choose a small value for resistor *Rn* and *Rp* in Figure.5.4b which satisfy Equation.5.11.

5.2 Verification in Mixed-Mode Simulation

5.2.1 Parameters in Simulation

This power clamp design is verified in Sentaurus TCAD Tool. Trigger circuit and discharge devices are simultaneously simulated in mixed-mode simulation. The process information is based on an 0.18um BCD process. The parameters setting is shown in Figure.5.1. The MOSFET in Buffer1 and Buffer2 are set as Table.5.1.

Table 5.1 Parameters of Buffers in Proposed Design.

Buffer	Device	w/l
Buffer1	NMOS	20/0.6um
Buffer1	PMOS	10/0.5um
Buffer2	NMOS	2/0.6um
Buffer2	PMOS	20/0.5um

This buffer design is sufficient to drive a SCR with 10um width(A_1 = 10um). According to the rules in last section, the width ratio of SCR2 to SCR1 is set to 8 ($A_1/A_2 = 4$) which means the width of SCR2 is 80um. The R_n and R_p are both set to 50Ω.

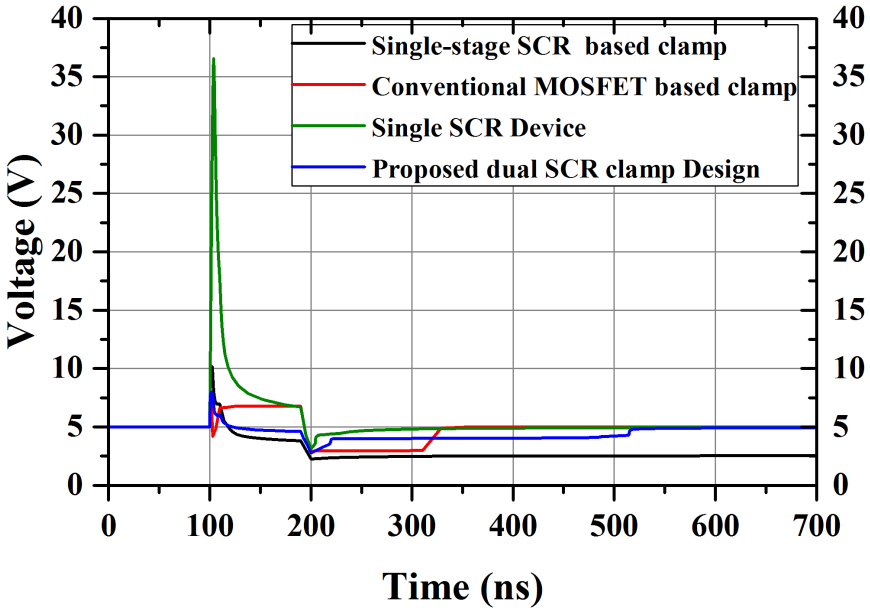
To better show the advantage of the proposed design, I simulated 5 clamp cells with different designs. Their differences are summarized in Table.5.2.

Table 5.2 Combination of Modules for Different Clamps in Simulation.

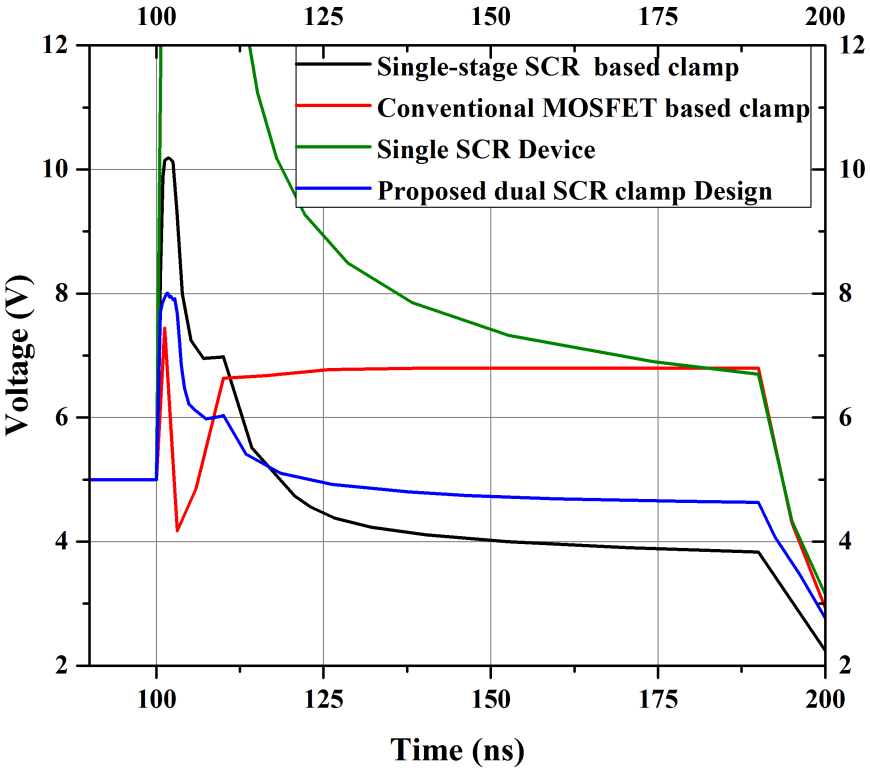
Design	Overshoot Suppress	Detection	Delay	Driver	Discharge
Single-Stage SCR based clamp	Figure.5.1				Single SCR in Figure.5.3
Conventional MOSFET based clamp	None	Figure.5.2b		1 inverter + 1 Buffer	NMOS (2000/0.6um)
Single SCR device	None				Single SCR in Figure.5.3
Proposed dual SCR clamp	Figure.5.2b				Figure.5.4

5.2.2 Simulation Result

In simulation, these cells are first charged to $V_{DD} = 5V$, to emulate the power cell used in working chip. TLP pulse with 100ns pulse with started would be applied on the power line then. The result is shown in Figure.5.7.



(a)



(b)

Figure 5.7: TLP Simulation: Power-on State (a)0-700ns and (b)100-200ns.

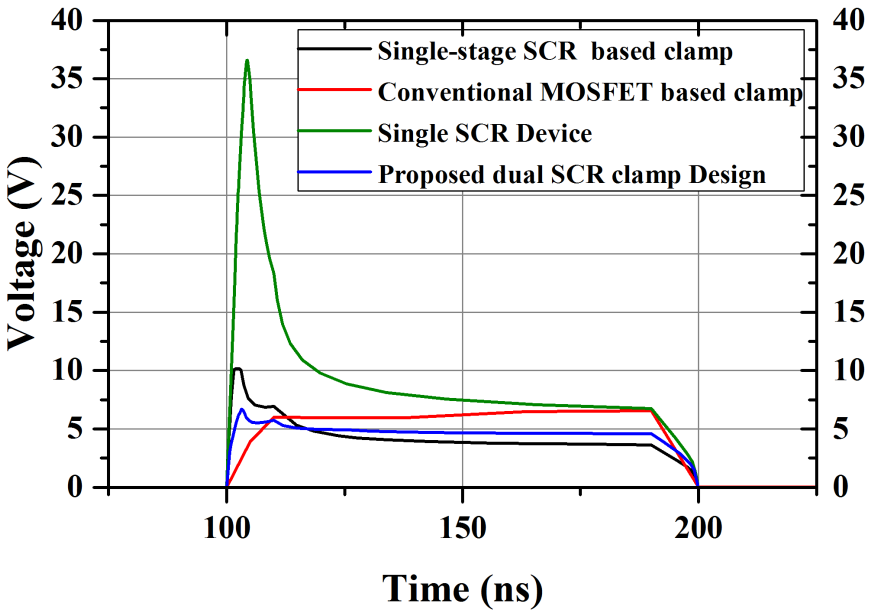


Figure 5.8: TLP Simulation: Power-off State

According to the results in Figure.5.7 and Figure.5.8, the proposed design has superior performance in terms of overshoot, clamping efficiency and Latch-up immunity over other structures.

5.2.2.1 Overshoot

The conventional MOSFET based clamp has the lowest overshoot voltage because MOSFET in active mode has faster response time comparing to SCR.

The proposed clamp also has good overshoot performance, because the two-stage SCR requires relatively low current to trigger.

Single-stage SCR based clamp has very high overshoot voltage because the SCR is so large and trigger circuit is not capable to drive it.

5.2.2.2 Clamping Voltage

The conventional MOSFET based clamp has the highest clamping voltage, because the channel resistance of MOSFET in active mode is very high.

Once turned on, the SCR would have extremely low clamping voltage, which will benefit safe discharge. As a result, all of the SCR based clamps have very low clamping voltage during the period when TLP was applied (100ns to 200ns).

5.2.2.3 Latch-up Immunity

With SCR as the discharge cell, the voltage is likely to drop below V_{DD} during ESD event. After ESD event, the low-voltage, high-current state might stay, leading to latch-up.

In Figure.5.7a, the single-stage SCR based clamp get latched after TLP pulse. As for the trigger circuit is not able to provide enough current to turn off the SCR.

The proposed clamp has no latch-up issue because the two-stage SCR (in Figure.5.4) requires only a small amount of current to turn off. Both of them turned off within a short period of time after TLP pulse.

The conventional MOSFET based clamp has no latch-up. Because the size of the NMOS is large enough and the current density is relatively low, which would not drive the parasitic NPN in NMOS into snapback mode.

5.3 Summary

In this chapter, a two-stage controllable SCR is created as the dischage cell in power clamp. The proposed SCR-based clamp possesses both controllability of active switch and the high current handling capability of SCR. A discharge SCR with 80μm width can provide comparable clamp performance comparing to the 2000μm MOSFET based clamp.

The design is verified in mixed-mode simulation. With the active controlling circuit, no latch-up is dected in the on-power state simulation.

CHAPTER 6
SUMMARY AND CONCLUSION

With the expanding applications of ICs in various scenarios, more and more performance factors are emphasized for ESD protection in addition to the most fundamental current handling capability. In short, these requirements can be summarized as ”Faster, Higher, Stronger”, same with the well-known Olympic motto.

The ”Faster” means faster response of the clamps to ESD events. ”Higher” can be interpreted in many ways, but here, I would like to say it’s higher holding voltage in some special high-voltage applications. ”Stronger” is of couse the better robustness. In this disseration, some design cases are presented to show how to make the clamps ”faster, higher and stronger”.

From the perspective of device, the clamp can be optimized by a combination of fast but weak devices and slow but strong devices. Among these devices, additional parasitic current paths can be established if the layout is placed in a proper way. Different current paths will conduct ESD current in different stage of the ESD event. The parasitic paths allow higher layout utilziation rates.

To achieve higher holding voltage, similarly, multiple clamping cells can be put in stacking. In the aid of the resistor path in proposed RSCR, a little impact is left on the overall stacking structure. With the modification on layout, more parasitic current paths are established to improve the current handlilng capability further.

In power clamp section, the high-efficient controllable SCR is implemented as the discharge device instead of MOSFETs. The dual-stage SCR design enables both good controllability and clamping capability. In the mixed-mode simulation, the proposed SCR clamp using only 80μm SCR shows better performance than the conventional soluting using big NMOS of 2000μm width.

The designs in this dissertation are process-independent and can be easily ported to other fabrication process. The concept of creating new parasitic current paths can also be applied in other ESD optmization design.

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