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Scalability and wide temperature range operation of spin-orbit torque switching devices using Co/Pt multilayer nanowires

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Spin-orbit torque (SOT) switching and retention properties in Co/Pt multilayer nanowire structures with various widths w down to 20 nm and the temperature dependences of the performance in the nanowire device with $w = 20$ nm are studied. Switching current I_{sw} scales down as w is reduced. The nanowire devices show high thermal stability factor $\Delta > 100$ for all the widths at room temperature. In the 20-nm-wide device, while a magnetization can be switched by current from –50 to 125 °C with a marginal increase in I_{sw} as the temperature decreases, Δ of more than 100 is kept up to 125 °C. These results indicate that SOT-switching devices using Co/Pt multilayers are scalable in nanoscale dimensions and can operate over a wide range of temperatures, offering high potential for a wide variety of applications including automobile and aerospace. *Published by AIP Publishing.* https://doi.org/10.1063/1.5045814

Nonvolatile spintronics memory devices, where a direction of a magnetization is switched by spin-transfer torques (STTs)[1,2] or spin-orbit torques (SOTs),[3–7] have been appealing as they are capable of realizing ultralow-power and high-performance integrated circuits. Being implemented in leading-edge integrated circuits, spintronics memory devices are required to be scalable in nanoscale dimensions, to operate with a small writing current, and to possess non-volatility for a long period of time or high thermal stability. Moreover, to use spintronics memory devices for a wide variety of applications, in particular, applications used in harsh conditions such as automobile and aerospace, they need to ensure operation over a wide range of temperatures, e.g., from –40 to 125 °C, which corresponds to the grade-1 level of the AEC-Q100,[8] the automobile standard for qualification of integrated circuits. While the devices need to be able to switch at low temperature, they are required to have a high enough thermal stability factor at high temperature. The thermal stability factor Δ ($\equiv E/k_BT$, where E is an energy barrier between two states, k_B is the Boltzmann constant, and T is the absolute temperature) needs to be more than 82 at 125 °C to achieve 20-year retention time in 1-Gbit memory with an error rate of 10^{-9}, corresponding to $\Delta > 110$ at 25 °C in case that E is independent of T. To meet these requirements in small dimensions, material systems such as Co/(Pt or Pd) multilayers are expected to be promising because of their high magnetic anisotropy.[9,10] Such material systems, in general, have high damping constant α,[11,12] which is detrimental for STT switching because high α causes high switching current density. On the other hand, a theoretical study pointed out that α has a little impact on threshold current density for SOT switching,[13] giving an opportunity to use Co/(Pt or Pd) multilayers. Moreover, Co/(Pt or Pd) multilayers exhibit a high SOT-switching efficiency.[14–16] We previously studied SOT switching in μm-scale Hall-bar devices using Co/Pt multilayers at room temperature and found that the SOT efficiency, given by effective areal anisotropy energy density divided by switching current density, increases with the increasing number of Co/Pt stacks.[16] In order for Co/Pt multilayers to be used in spintronics memory devices using SOT switching, it is of great interest to study the device scalability in nanoscale dimensions and the feasibility of wide temperature range operation in nanoscale devices. Here, we investigate SOT switching and the thermal stability factor of Co/Pt multilayer nanowire devices with nanoscale dimensions down to 20 nm from –50 to 125 °C.

Stacks of Ta(3)/Pt(3)/[Co(0.4)/Pt(0.4)]$_4$/Co(0.4)/Ta(0.2)/$(Co_{25}Fe_{75})_{0.75}B_{0.25}$(1)/MgO(1.2)/$(Co_{25}Fe_{75})_{0.75}B_{0.25}$(0.5)/Ta(1) are deposited on a highly resistive Si substrate by dc/rf magnetron sputtering [Fig. 1(a)]. The numbers in parentheses are nominal thicknesses in nm. To aim for three-terminal magnetic tunnel junctions, Ta/CoFeB/MgO/CoFeB layers are deposited on the top of Co/Pt multilayers as the CoFeB/MgO structure can show a high tunnel magnetoresistance ratio of more than about 100%.[17–19] We confirm that the CoFeB/MgO layers do not yield a major impact on the results; the top CoFeB(0.5) is magnetically dead, and the insertion of the bottom CoFeB(1) gives 5% smaller switching current (see supplementary material). The stacks are confirmed to have a perpendicular easy axis from a vibrating sample magnetometer (VSM). The stacks are patterned into nanowire devices with a Ta/Pt channel and a pair of Hall probes using electron-beam/photo-lithography, reactive ion etching, and Ar ion milling. Cr(5)/Au(100) electrodes are formed at the ends of the channels and the probes. The magnetic nanowire part

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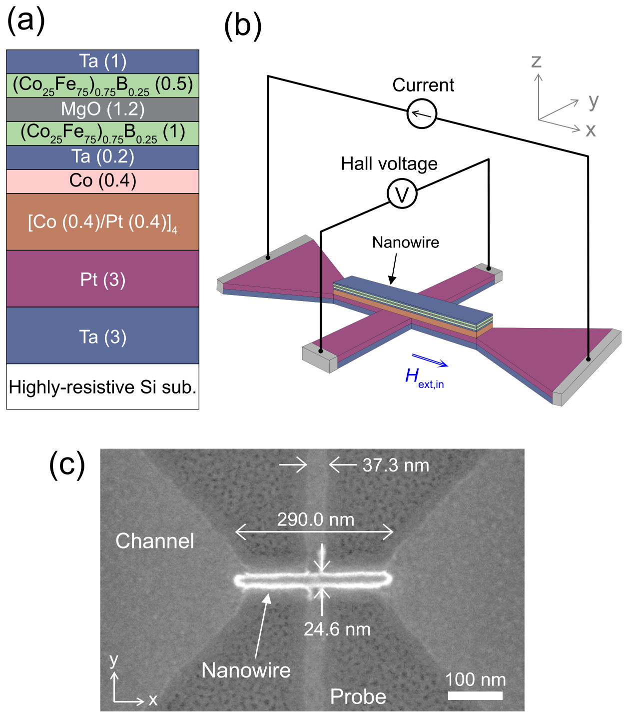

FIG. 1. (a) Film stack used in this study. (b) Schematic of a nanowire device and its measurement setup. (c) The top-down SEM image of the nanowire device with a 300-nm length and a 20-nm width (nominal). The numbers in the images are measured values.

is isolated from the electrodes to avoid any effects on a magnetization reversal originating from the contact between the magnetic layers and the electrodes. The nominal length of the magnetic nanowire structures is fixed at 300 nm, and the nominal width w is varied from 400 to 20 nm to examine the device scalability. Figures 1(b) and 1(c) show the schematic of the nanowire device along with the measurement setup and the top-down scanning electron microscopy (SEM) image of the device with $w = 20$ nm, respectively. The measured width is about 25 nm for $w = 20$ nm, as shown in Fig. 1(c). It is known that fabrication processes cause an electrically and/or magnetically dead region in magnetic materials.[20,21] Such a dead region has an impact on device performance in nanoscale dimensions.[22] Based on the w dependence of a Hall resistance difference between two states, the dead region width is determined to be about 5 nm in our devices (see supplementary material). After the processes, the devices are annealed at 300 °C for an hour in vacuum.

We first show representative results of SOT-switching and the thermal stability measurement at room temperature. To measure SOT switching, a current pulse I with a duration of 100-ms is applied through the channels under an external in-plane field $H_{ext,in}$ collinear with the current, and then, a Hall resistance R_{Hall} is measured from the Hall voltage between the probes with a dc current of 100 μA. Figure 2(a) shows the R_{Hall}-I loops for the device with $w = 20$ nm under $\mu_0 H_{ext,in} = +200$ and –200 mT (μ_0: the permeability in vacuum). The R_{Hall}-I loops show clear hysteresis, and the switching direction depends on the polarity of $H_{ext,in}$, indicating that the magnetization switching is induced by SOT. Similar results are obtained for all the other devices. We determine thermal stability factor Δ and effective magnetic

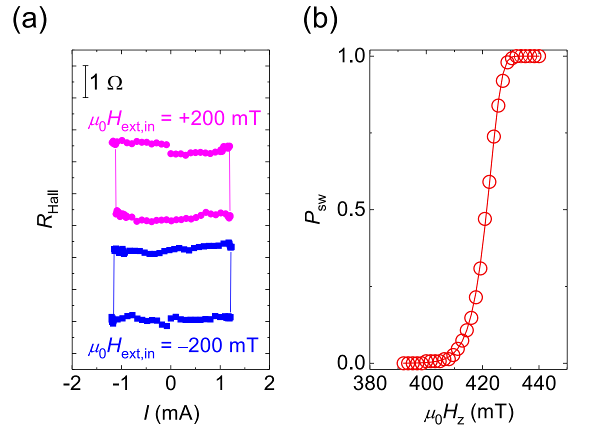

FIG. 2. (a) R_{Hall}-I loop under $\mu_0 H_{ext,in} = +200$ and –200 mT for the device with $w = 20$ nm. (b) P_{sw} as a function of H_z for the device with $w = 20$ nm. The solid line is the fitting based on the Stoner-Wohlfarth model.

anisotropy field H_K^{eff} based on the Stoner-Wohlfarth model[23] by measuring switching probability P_{SW} under a magnetic field H_z along the +z direction with various magnitudes. H_z is applied to the devices with initial magnetization pointing to the –z direction, and the magnitude of H_z is swept with a 1-s holding time, followed by the R_{Hall} measurement to examine whether the magnetization direction is switched. The measurement is repeated 150 times for each H_z to obtain P_{sw}. With the assumption that the dominant energy barrier governing the retention property is determined by a reversal of nuclei that follows a single-domain model, Δ and H_K^{eff} are obtained by fitting the experimental plots of P_{sw}-H_z curves with the attempt time of 1 ns.[23] Note that this assumption gives the lower bound of Δ.[24,25] Figure 2(b) shows the P_{sw}-H_z curve for the device with $w = 20$ nm, where Δ and H_K^{eff} are adopted as fitting parameters. Fitting yields Δ of 249 with $\mu_0 H_K^{eff}$ of 622 mT.

We now investigate the device scalability in the Co/Pt multilayer nanowire devices by evaluating a number of devices with various widths at room temperature. $\mu_0|H_{ext,in}| = 200$ mT is applied during the switching measurement. Switching currents I_{sw} for the width w from 400 to 20 nm are summarized in Fig. 3(a). I_{sw} scales along with w; I_{sw} reduces

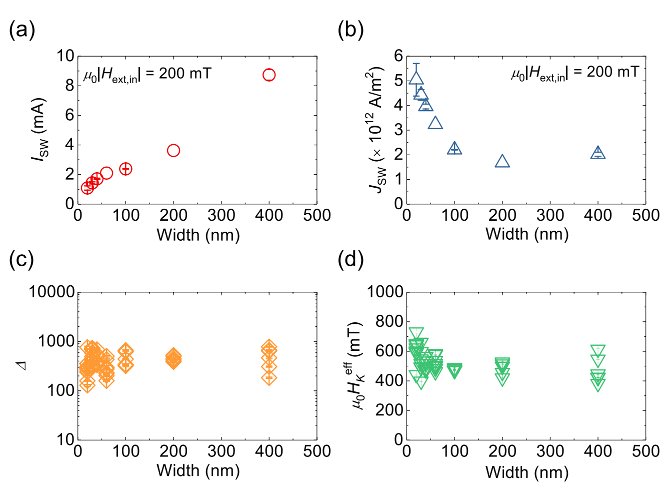

FIG. 3. (a) I_{sw} and (b) J_{sw} under $\mu_0|H_{ext,in}| = 200$ mT as a function of a width w. (c) Δ and (d) H_K^{eff} obtained from the P_{sw} measurement with various nanowire widths. Multiple devices with each width. Widths are all nominal.

from 8.7 mA for $w = 400$ nm to 1.1 mA for $w = 20$ nm. Figure 3(b) shows switching current density J_{sw} as a function of w, where J_{sw} denotes the average current density flowing in the layers from Ta(3) to CoFeB(1). While J_{sw} is almost constant for w from 400 to 100 nm, J_{sw} monotonically increases in the devices as w is reduced below 100 nm; J_{sw} is 2.0×10^{12} A/m^2 for $w = 400$ nm and 5.0×10^{12} A/m^2 for $w = 20$ nm. This result is in qualitative agreement with our previous works on other material systems[26,27] and can be explained by a scenario that less nucleation takes place for smaller w, leading to higher J_{sw}.[27] It is noted that I_{sw} (J_{sw}) is expected to increase with shorter current pulse due to less Joule heating, and there is still a need to reduce I_{sw} (J_{sw}) by material engineering for practical use. Next, we show the width dependences of Δ and H_K^{eff} in Figs. 3(c) and 3(d), respectively. All the devices with w from 400 nm down to 20 nm achieve Δ of higher than 100. H_K^{eff} is also kept high values ($\mu_0 H_K^{\text{eff}} \gtrsim 400$ mT) for all w down to 20 nm. The variations of Δ and H_K^{eff} may be caused by the difference in magnetization reversal modes among the devices. Overall, the results shown in Fig. 3 indicate that the nanowire devices using Co/Pt multilayers can exhibit the high enough retention property and yet can be switched by current even for the device with $w = 20$ nm.

Next, we focus on the device with $w = 20$ nm, the smallest device size in this study, and examine the temperature dependences of switching properties together with Δ. The temperature is varied from –50 to 125 °C during the measurement; a wafer stage is heated up for the high temperature measurement, and a holder mounting the device is cooled down by a cryostat for the low temperature measurement. R_{Hall}–I loops are measured under $\mu_0 H_{\text{ext,in}} = +200$ and –200 mT. I_{sw} (J_{sw}) at various temperatures is summarized in Fig. 4. I_{sw} (J_{sw}) shows a marginal increase at low temperature, indicating that the device can operate at low temperature. The temperature dependence of Δ is shown in Fig. 5(a). Note that the device and equipment for the low temperature measurement are not the same to the ones for the high temperature measurement. The obtained Δ decreases gradually with increasing temperature. Although the reason for a slight increase in Δ from 100 to 125 °C is not clear, the values of Δ are beyond 100 over all the range of temperatures. This result means that the device can secure long enough data retention time up to 125 °C.

We finally discuss the behavior of Δ. E ($= \Delta k_B T$) is given by $E = M_s H_K^{\text{eff}} V/2$ for a nucleation-mediated reversal,

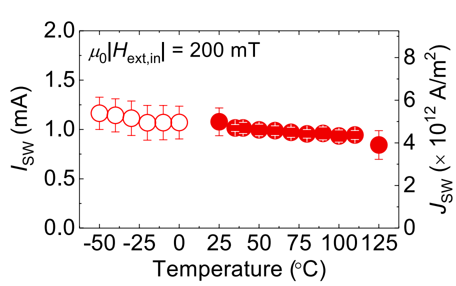

FIG. 4. I_{sw} as a function of temperature under $\mu_0|H_{\text{ext,in}}| = 200$ mT for the device with $w = 20$ nm. Error bar is given by obtaining I_{sw} from multiple devices. Solid and open symbols indicate the data points obtained with high and low temperature measurement setups, respectively.

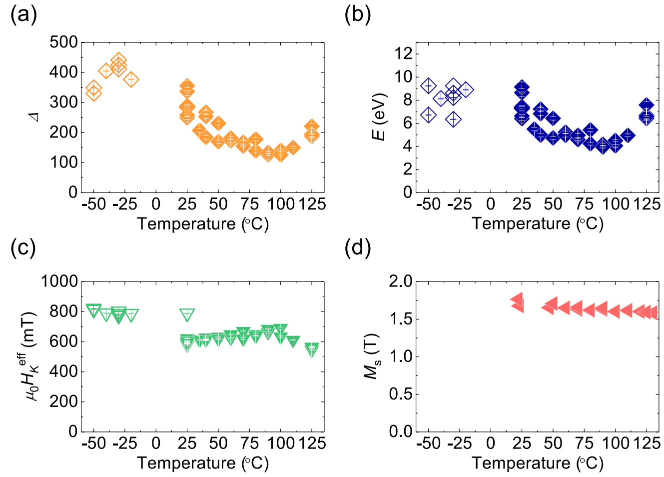

FIG. 5. (a) Δ, (b) E, and (c) H_K^{eff} as a function of temperature for the device with $w = 20$ nm. Multiple devices are measured at each temperature. Solid and open symbols indicate the data points obtained with high and low temperature measurement setups, respectively. (d) M_s as a function of temperature measured by the VSM using a blanket film.

where M_s is the spontaneous magnetization and V is the activation volume of the ferromagnet. Thus, we here have a look at the temperature dependence of E, H_K^{eff}, and M_s separately, where M_s is measured with the VSM at various temperatures using the blanket film of the same stack in Fig. 1(a). E, plotted in Fig. 5(b), is found to become almost half by increasing the temperature. On the other hand, H_K^{eff} and M_s, plotted in Figs. 5(c) and 5(d), respectively, are not sensitive to the temperature in the studied range and cannot explain the behavior of Δ or E. This implies that the activation volume in the nanowire structure varies with temperature. Another possibility is that the analysis based on the Stoner-Wohlfarth model does not yield true values of Δ (and H_K^{eff}). This is possible if the single-domain picture is not applicable to the process that poses the highest energy barrier during the magnetization reversal in the used nanowire devices. In this regard, it may be needed to employ a direct way such as retention time measurement at elevated temperature for more reliable evaluation of Δ.[28] Nevertheless, because the derived Δ, which might be underestimated in the procedure employed here, is high enough, the SOT-switching device with the Co/Pt multilayer has the scalability at least down to 20 nm in width and has the capability for wide temperature range applications.

In conclusion, we study the scalability of the Co/Pt multilayer nanowire devices operated by SOT and the feasibility of their wide temperature range operation. From the measurement at room temperature, we find that, while I_{sw} scales down as w of the device is reduced, Δ of more than 100 is obtained for all the devices with w down to 20 nm. The 20-nm-wide device exhibits Δ of more than 100 with a marginal change in I_{sw} over a wide range of temperatures from –50 to 125 °C. Even though there is still a necessity to reduce I_{sw} (J_{sw}) in the Co/Pt multilayer nanowire devices by further material engineering, these results indicate that the SOT-switching device using Co/Pt multilayers is an attractive candidate for use in a wide variety of applications, in particular, applications used in harsh conditions such as automobile and aerospace.

See supplementary material for the comparison of magnetic and switching properties of the stacks between with and without the insertion of the bottom Ta(0.2)/CoFeB(1) and details on the determination of a width of a dead region in nanowire devices.

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