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SYSTEM SI/PI MODELING AND ANALYSIS

by

BIYAO ZHAO

A DISSERTATION

Presented to the Faculty of the Graduate School of the
MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

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2020

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ABSTRACT

A physics-based circuit modeling methodology for 3D IC/packages is proposed here. The method is based on partial element equivalent circuit (PEEC) and layered Green's function (LGF). The LGFs are calculated from discrete complex image method (DCIM) with three terms, direct coupling, complex images, and surface wave, extracted to analyze the wave behavior. The dominate terms for LGFs are analyzed for four stack-ups in 3D IC/packages. Analytical formulas that include the contribution of complex images are proposed for partial capacitance calculation, with the complex image extracted from LGFs. A chip PDN geometry is used to illustrate the use of LGF in PEEC to validate the proposed method. A good match is observed between the input impedance from the proposed method and full wave simulation.

A physics-based circuit modeling methodology for system-level power integrity (PI) analysis and design is presented herein. The modeling methodology is based on representing the current paths in the power distribution network (PDN) with appropriate circuits based on cavity model and plane-pair Partial Element Equivalent Circuit (PEEC). The PDN input impedance looking from on-chip sources can be computed. A commercial simulation tool is used to corroborate the modeling approach where the system consists of a commercial IC, a complex organic package and a very high-layer-count printed circuit board. Two types of circuit models are proposed from the methodology with physical correspondence maintained in the circuit elements. The circuits can be used to analyze the geometry impact on the PDN impedance and explore design improvements. Voltage ripple simulations are conducted with the circuit models. The simulated results correlated with measurements.

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1. INTRODUCTION

Three-dimensional (3D) IC and packaging has been used to achieve high density and high performance for high-speed digital systems [1], [2], [3]. The 3D IC/packaging technologies have been widely used in many types of high-speed systems, such as smartphones, tables, HMC, HBM, etc [1]. Shorter interconnection in the 3D IC/packaging system leads to faster function speed, lower power consumption and higher bandwidth. Also, the dimension in the system adds to the design flexibility to reduce the system footprint and size. However, due to the density and complexity of the system, many new challenges are encountered in the manufacturing, design, modeling and analysis of the system. Heat management, yield, design complexity, TSV, testing equivalent, lack of EDA tools and design guidelines, all these factors limit the discovery and understanding of such complex systems. Serious signal integrity and power integrity issues are observed with the increase of cross-talk, jitter, etc.

Commercial simulation tools and numerical algorithm with acceleration algorithms have been used to model the system. One common method is to divide the system into different blocks, simulate each block using full-wave simulation, and cascade the S-parameter for all the blocks to represent the system [4][5][6]. The simulation may still take long time and large memory even with the segmentation method due to the complexity of the geometry. Any change in the geometry requires re-simulation, which is time-consuming to test out different designs. Also, the details of the structures are buried in S-parameters and it is hard to identify the geometry influence on the response of the system. Another method is based on unit cells [7][8][9]. Common and repeated structures in the geometry are identified first to obtain details for several unit cells. Then different unit cells

are simulated in full-wave tools to extract equivalent circuit models or S-parameter blocks for the unit cells. Then circuit models or S-parameter blocks are connected according to geometry connections to build the final model for the entire system. The circuit models for the unit cells can reflect the connection between geometry and response. However, due to large numbers of cells, it is difficult to identify the impact of specific changes. To summarize, due to the complexity of the geometry, it is difficult to build accurate models for the 3D IC/package within a short time for both methods.

A common characteristic for all 3D IC/package system is that different layers of structures and various materials [10] are stacked vertically and leads to a layered medium. A fast modeling methodology is proposed based on partial element equivalent circuit (PEEC) and a layered Green's function (LGF). The modeling method includes three acceleration treatments to handle the complex geometry and maintain the accuracy. The first one is to use the LGF to handle the vertical directional complexity, and use PEEC to handle the horizontal one. The second one is special procedures to include LGF in PEEC formulation to avoid multiple LGF extractions and time-consuming integrations. The discrete complex image method (DCIM) is used to extract the LGFs. The contribution of direct coupling, complex images, and surface wave is analyzed for 3D IC/package systems to identify critical pieces in the LGFs. The LGF calculation is divided into two steps to include LGF in PEEC for partial inductance (L) and capacitance (C) calculations. The first step is to extract the information needed to compose spatial domain Green's functions for all the source and observation locations along the vertical direction. The second step is to identify the information to compose spatial domain Green's function for L and C calculations. Analytical formulas are proposed to avoid integration in the calculation to

include LGF in PEEC. With these special procedures, the partial L and C values can be calculated within seconds for two bars. The third treatment is to identify the critical mutual L and C needed between PEEC meshes to reduce horizontal complexity. A chip PDN geometry is used here to illustrate these treatments. In this way, the computation complexity can be largely reduced while the accuracy of the results can be maintained. An equivalent circuit model can be extracted from PEEC to represent the 3D IC/package system, which can be used to analyze the influence of geometry change on response. The modeling methodology can be extended to large scale systems with high accuracy without increasing computation cost.

Digital and communication systems are operating at an increasing speed [11]. Further, the physical complexity of such systems is increasing with advances in package (PKG) integration and chip technology updates. The physical dimensions of the system are becoming smaller. The design density is becoming higher, which makes the designs more sensitive to noise and interference [12]. Power integrity (PI) is a design problem with many increasingly challenging issues.

The power distribution network (PDN) delivers the supply voltage to all circuits. The large switching current at the integrated circuits (IC) results in voltage droop and ripple. To minimize voltage droop and ripple, the PDN must exhibit a low impedance for all important frequencies [13], [14].

A fundamental PDN design principle is that the input impedance can be reduced by multiple parallel current paths [15]. Many decoupling capacitors are added at different levels of the system to increase the number of parallel paths. Another important rule in PDN design is the frequency aspect of design. In the PDN analysis, the chip, PKG and

printed circuit board (PCB) are designed to lower the input impedance over different frequency ranges. To ensure the effectiveness of the chip, PKG and PCB in different frequency ranges, the dimensions and values of the decoupling solutions vary among them [17].

Different numerical modeling methods, such as the finite difference time domain (FDTD) method [18], [19], the finite element method (FEM) [20], and boundary integral formulation [21], and commercial solver tools [22], [23], [24], are used to characterize the PDN performance at different levels. A common procedure using these methods and tools is that the geometry is meshed into nodes and small cells, and system equations are applied to obtain the voltage and current at the nodes. S-parameters or Z-parameters are exported as the results of the simulation. A challenge in using these methods and tools is that while the PDN input impedance for the problem is readily obtained [15],[16] it is hard to relate the frequency response to the current paths and geometric design details, as the geometry details are buried in the block by using the S- or Z-parameters. Another limitation is that any changes in the geometry require new simulations with extra setup and running time, which can be time-consuming due to the complexity of the geometry.

A PDN design objective is to determine the possibilities for placing the necessary decoupling capacitors (hereafter referred to as decaps for brevity) at the multiple levels and locations of the system. Usually, the decaps on the PKG and PCB are placed in the available space where the associated vias do not block high-speed signal trace routing.

A straight-forward design approach using commercial tools has been widely used to evaluate PDN designs. The tools provide the PDN input impedance that can be used to compare with the target impedance to determine if this specification is met [13]. However,

existing tools do not provide a physics-based inductance network where each part of the current path in the design can be correlated directly with the geometry, and its impact on the total input impedance. Special settings and extra simulation time in the commercial tools are required to extract the partial or loop inductances to correlate the geometry details directly to the input impedance. The port and shorts settings require clear and complete understanding of the current paths in the system. For the complex geometries where there are interactions between structures and components, the partial and loop inductances extraction can be overlooked. Also, the multitude of possible decap locations results in many viable decoupling solutions. It is undesirable to proceed with the design based on numerous iterations of a ‘trial-and-error’ process using commercial simulations and measurements. Moreover, the PDN geometry details are hidden in the S-parameters from the simulation or measurement results.

A physics-based circuit modeling methodology [16] is proposed herein based on tracing the current path. The methodology maintains the correspondence to the geometry with the elements in the models representing a single geometry feature or block. Two types of circuit models, a physics-based circuit model and an impedance equivalent circuit model, are proposed along with the methodology. A key feature in the physics-based circuit model is that it maintains the one-to-one physical correspondence to the geometry. The function and impact of the geometrical details can be mapped to the response through circuit elements. It can be also used to identify current paths and interactions because of the one-to-one correspondence to the geometry. The impedance equivalent circuit is extracted from the physics-based circuit model by tracing the current paths in the system. The inductances are extracted directly from the associated geometrical pieces by using the

physics-based circuit model instead of a fitting process from the input impedance. It maintains the convenience and simplicity of the hierarchical circuit model to be used both in time-domain [25][26][27][28] and frequency-domain [29][30] simulations. The geometry correlation features are passed on from the physics-based circuit model to the impedance equivalent circuit model. The current paths in the system are reflected geometrically and completely with interactions included in the impedance equivalent circuit model. The resonances can be associated with geometry blocks [15].

2. LAYERED GREEN'S FUNCTION

Green's function is solution to the wave equation with an impulse source under initial conditions and boundary conditions. It is similar to the impulse response in a linear system. In [31], electric fields and magnetic fields can be found using Green's functions and sources. For layered medium, several methods have been proposed based on reflection and transmission coefficients [31]-[36]. Then the Sommerfeld integration is applied to obtain the spatial-domain Green's function from spectrum-domain Green's function. One way to solve the Sommerfeld integration is to use discrete complex image method (DCIM) [32]. DCIM provides closed-form spatial Green's function for multi-layer medium by using Sommerfeld identity.

The LGF used here is extracted from DCIM [32][33]. The advantage of using DCIM for LGF calculation is that different wave behaviors can be analyzed. In this section, a brief summary of DCIM is included. A microstrip case is used to validate the LGF from DCIM. Then, the LGFs for four 3D IC/package stack-ups are analyzed by using the three components from DCIM to locate the critical wave behaviors in the system.

Layered Green's function extraction has two steps. The first step is to obtain the spectrum domain Green's function based on the transmission line Green's function [31]. Here, the generalized reflection and transmission coefficients along the vertical direction of a layered media are used to calculate the voltages and currents due to different types of sources. The spectrum domain Green's functions can be obtained using the calculated voltages and currents. The second step is to calculate the spatial domain Green's function based on the spectrum domain Green's function. For layered medium, since the medium is infinite large in the (x,y) plane, spectral-domain analysis are commonly used to transfer

the transverse coordinate $\boldsymbol{\rho} = \hat{\mathbf{x}}x + \hat{\mathbf{y}}y$ to its spectral counterpart $\mathbf{k}_\rho = \hat{\mathbf{x}}k_x + \hat{\mathbf{y}}k_y$ by the Fourier transform pair, as

$$\begin{aligned} F[f(\mathbf{r})] &= \tilde{f}(\mathbf{k}_\rho; z) = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} f(\mathbf{r}) e^{j\mathbf{k}_\rho \cdot \boldsymbol{\rho}} dx dy \\ F^{-1}[\tilde{f}(\mathbf{k}_\rho; z)] &= f(\mathbf{r}) = \frac{1}{(2\pi)^2} \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \tilde{f}(\mathbf{k}_\rho; z) e^{-j\mathbf{k}_\rho \cdot \boldsymbol{\rho}} dx dy = S_0(\tilde{f}(\mathbf{k}_\rho)) \end{aligned} \quad (1)$$

Sommerfeld integral has been used to obtain the spatial domain Green's function, which is defined as

$$S_0(\tilde{f}(\mathbf{k}_\rho)) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |\mathbf{k}_\rho| J_0(\mathbf{k}_\rho \cdot \boldsymbol{\rho}) \tilde{f}(\mathbf{k}_\rho; z) d|\mathbf{k}_\rho| \quad (2)$$

Here, J_0 is the Bessel function of 0 order.

The direct numerical integration is time-consuming since the kernel of the Sommerfeld integral is oscillatory and has singularities with slow decaying parts in the complex k_ρ plane. DCIM is used to accelerate the calculations of Sommerfeld integral to calculate the spatial domain Green's function. The idea of DCIM is to use complex exponential functions to approximate the kernel. Then the spatial domain Green's function can be used directly derived by using Sommerfeld identify as

$$F\left(\frac{e^{-jk|\mathbf{r}-\mathbf{r}'|}}{4\pi|\mathbf{r}-\mathbf{r}'|}\right) = \frac{e^{-jk_z|z-z'|}}{2jk_z} \quad (3)$$

Here, $k_z^2 = k_i^2 - k_\rho^2$, $k_\rho = \sqrt{k_x^2 + k_y^2}$ and $k_i = \omega\sqrt{\epsilon_i\mu_i}$.

2.1. LAYERED GREEN'S FUNCTION

A multi-layered media shown in Figure 2.1 is used to illustrate the calculation of the spectrum domain layered Green's function. Multiple reflections and transmissions happen at the boundaries, as shown in Figure 2.2.

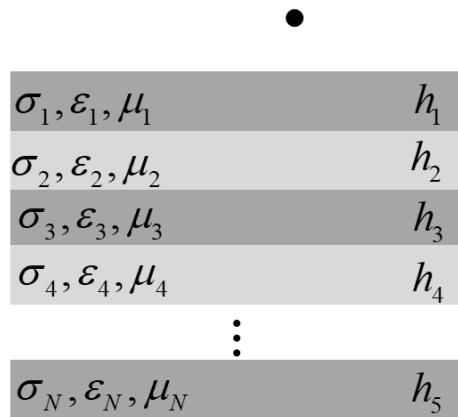


Figure 2.1. Multi-layered media

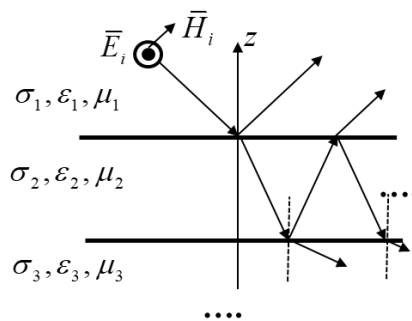


Figure 2.2. Reflection and transmission on the boundary.

A transmission line Green's function analysis is used here [31]. The multi-layered media can be changed to Figure 2.3 for the transmission line analysis.

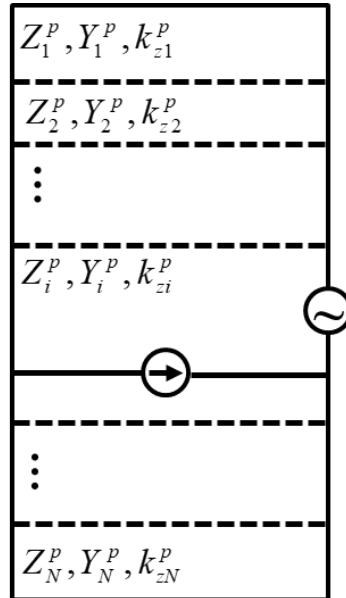


Figure 2.3. The transmission line analysis for spectrum domain Green's function based on transmission line Green's function.

The governing equations for the total spectrum domain Green's function based on the transmission line theory are the telegraph equation, as

$$\begin{aligned} \frac{dV^p}{dz} &= -jk_z Z^p I^p + v^p \\ \frac{dI^p}{dz} &= -jk_z Y^p V^p + i^p \end{aligned} \quad (4)$$

Here, p denotes either e or h type. The characteristic impedances of the transmission line are shown as

$$Z^e = \frac{1}{Y^e} = \frac{k_z}{\omega \epsilon_0 \epsilon_r}, \quad Z^h = \frac{1}{Y^h} = \frac{\omega \mu_0 \mu_r}{k_z}. \quad (5)$$

From

$$\begin{aligned} \mathbf{A}(\mathbf{r}) &= \int_{s_i} \underline{\underline{\mathbf{G}}}_A(\mathbf{r}, \mathbf{r}') \mathbf{J}(\mathbf{r}') dS' \\ \varphi(\mathbf{r}) &= \int_{s_i} G_\varphi(\mathbf{r}, \mathbf{r}') q(\mathbf{r}') dS' \end{aligned} \quad (6)$$

The spectrum layered Green's function can be written as

$$\underline{\underline{\tilde{\mathbf{G}}}}_A = \begin{bmatrix} \tilde{G}_{xx}^A & 0 & 0 \\ 0 & \tilde{G}_{yy}^A & 0 \\ \tilde{G}_{zx}^A & \tilde{G}_{zy}^A & \tilde{G}_{zz}^A \end{bmatrix} = \begin{bmatrix} \frac{1}{j\omega} V_i^h & 0 & 0 \\ 0 & \frac{1}{j\omega} V_i^h & 0 \\ \frac{\mu_0 \mu_r k_x}{jk_\rho^2} (I_i^h - I_i^e) & \frac{\mu_0 \mu_r k_y}{jk_\rho^2} (I_i^h - I_i^e) & \frac{\mu_0 \mu_r}{j\omega \epsilon_0 \epsilon_r} I_v^e \end{bmatrix} \quad (7)$$

$$\tilde{G}_\varphi = \frac{j\omega \epsilon_0}{k_\rho^2} (V_i^e - V_i^h) \quad (8)$$

Here, i means the source type is current source. V_i^e , V_i^h , I_i^e , I_i^h denote voltage and current due to shunt current source. I_v^e denotes current due to series voltage source. k_ρ is the propagation constant along horizontal directions. To derive the solutions of the transmission line voltages and currents V_v^p , V_i^p and I_v^p , I_i^p , the governing equations due to different current and voltage sources are changed to

$$\begin{aligned}
\frac{dV_i^p}{dz} &= -jk_z Z^p I_i^p \\
\frac{dV_v^p}{dz} &= -jk_z Z^p I_v^p + \delta(z - z') \\
\frac{dI_i^p}{dz} &= -jk_z Y^p V_i^p + \delta(z - z') \\
\frac{dI_v^p}{dz} &= -jk_z Y^p V_v^p
\end{aligned} \tag{9}$$

Here, δ is the Dirac delta function. Assume the source point at z' is in the m layer and the observation point at z is in the n layer. Layer n is defined with boundaries at z_{n-1} and z_n .

The propagation constants for m layer and n layer are k_z^m and k_z^n , respectively. And the characteristic impedance (admittance) are denoted as $Z^m(Y^m)$, $Z^n(Y^n)$, respectively.

Assume $z_0 = z_1$ and $z_N = z_{N-1}$. There are three relative locations for the source and observation points based on the layer numbers, as $m=n$, $m>n$, $m<n$.

When $m=n$, the source point and observation point are in the same layer. The voltage and current due to the current source can be calculated as

$$\begin{aligned}
V_i^p &= \frac{Z_n^p}{2} [e^{-jk_z^n |z-z'|} + M_n^p \sum_{s=1}^4 B_{ns}^p e^{-jk_z^n \gamma_{ns}}] \\
I_i^p &= \frac{1}{2} [\pm e^{-jk_z^n |z-z'|} + M_n^p \sum_{s=1}^4 (-1)^s B_{ns}^p e^{-jk_z^n \gamma_{ns}}]
\end{aligned} \tag{10}$$

Here, the upper and lower signs are for the case $z > z'$ and $z < z'$, respectively. And M_n^p can be calculated as

$$M_n^P = \frac{1}{\left[1 - \tilde{R}_{n,n-1}^P \tilde{R}_{n,n+1}^P e^{-2jk_z^n(z_n - z_{n-1})}\right]} \quad (11)$$

Here,

$$\begin{aligned} B_{n1}^P &= \tilde{R}_{n,n+1}^P, \quad \gamma_{n1}^P = 2z_n - (z + z') \\ B_{n2}^P &= \tilde{R}_{n,n-1}^P, \quad \gamma_{n2}^P = -2z_{n-1} + (z + z') \\ B_{n3}^P &= \tilde{R}_{n,n-1}^P \tilde{R}_{n,n+1}^P, \quad \gamma_{n3}^P = 2(z_n - z_{n-1}) - (z - z') \\ B_{n4}^P &= \tilde{R}_{n,n-1}^P \tilde{R}_{n,n+1}^P, \quad \gamma_{n4}^P = 2(z_n - z_{n-1}) + (z - z') \end{aligned} \quad (12)$$

The generalized reflection coefficients are

$$\begin{aligned} \tilde{R}_{n,n-1}^P &= \frac{R_{n,n-1}^P + \tilde{R}_{n-1,n-2}^P e^{-2jk_z^{n-1}(z_{n-1} - z_{n-2})}}{1 + R_{n,n-1}^P \tilde{R}_{n-1,n-2}^P e^{-2jk_z^{n-1}(z_{n-1} - z_{n-2})}} \\ \tilde{R}_{n,n+1}^P &= \frac{R_{n,n+1}^P + \tilde{R}_{n+1,n+2}^P e^{-2jk_z^{n+1}(z_{n+1} - z_n)}}{1 + R_{n,n+1}^P \tilde{R}_{n+1,n+2}^P e^{-2jk_z^{n+1}(z_{n+1} - z_n)}} \end{aligned} \quad (13)$$

Where,

$$R_{n,n+1}^P = \frac{Z_{n-1}^P - Z_n^P}{Z_{n-1}^P + Z_n^P}, \quad R_{n,n+1}^P = \frac{Z_{n+1}^P - Z_n^P}{Z_{n+1}^P + Z_n^P}. \quad (14)$$

When $m < n$, and the source point is above the observation point, the voltage and current due to the current source can be calculated as

$$\begin{aligned}
I_i^p &= \left\{ \frac{Z_m^p}{2} T_{mn}^{p,down} Y_n^p [e^{-jk_z^m(z_m-z')} + \tilde{R}_{m,m-1}^p e^{-jk_z^m(-2z_{m-1}+z_m+z')}] \right. \\
&\quad \cdot [e^{-jk_z^n(-z_{n-1}+z)} - \tilde{R}_{n,n+1}^p e^{-jk_z^n(-z_{n-1}+2z_n-z)}] \cdot M_m^p \left. \right\} \\
V_i^p &= \left\{ \frac{Z_m^p}{2} T_{mn}^{p,down} [e^{-jk_z^m(z_m-z')} + \tilde{R}_{m,m-1}^p e^{-jk_z^m(-2z_{m-1}+z_m+z')}] \right. \\
&\quad \cdot [e^{-jk_z^n(-z_{n-1}+z)} + \tilde{R}_{n,n+1}^p e^{-jk_z^n(-z_{n-1}+2z_n-z)}] \cdot M_m^p \left. \right\}
\end{aligned} \tag{15}$$

$$S_{i,i+1}^{p,down} = \frac{R_{i,i+1}^p + 1}{1 - R_{i+1,i}^p \tilde{R}_{i+1,i+2}^p e^{-2jk_z^{i+1}(z_{i+1}-z_i)}}, \quad T_{mn}^{p,down} = \prod_{i=m}^{n-1} e^{-jk_z^i(z_i-z_{i-1})} S_{i,i+1}^{p,down}. \tag{16}$$

When $m > n$, the voltage and current due to the current source can be calculated as

$$\begin{aligned}
I_i^p &= \left\{ \frac{Z_m^p}{2} T_{mn}^{p,up} Y_n^p [e^{-jk_z^m(-z_{m-1}+z')} + \tilde{R}_{m,m+1}^p e^{-jk_z^m(2z_m-z_{m-1}-z')}] \right. \\
&\quad \cdot [-e^{-jk_z^n(z_n-z)} + \tilde{R}_{n,n-1}^p e^{-jk_z^n(-2z_{n-1}+z_n+z)}] \cdot M_m^p \left. \right\} \\
V_i^p &= \left\{ \frac{Z_m^p}{2} T_{mn}^{p,up} [e^{-jk_z^m(-z_{m-1}+z')} + \tilde{R}_{m,m+1}^p e^{-jk_z^m(2z_m-z_{m-1}-z')}] \right. \\
&\quad \cdot [e^{-jk_z^n(z_n-z)} + \tilde{R}_{n,n-1}^p e^{-jk_z^n(-2z_{n-1}+z_n+z)}] \cdot M_m^p \left. \right\}
\end{aligned} \tag{17}$$

$$S_{i,i-1}^{p,up} = \frac{R_{i,i-1}^p + 1}{1 - R_{i-1,i}^p \tilde{R}_{i-1,i-2}^p e^{-2jk_z^{i-1}(z_{i-1}-z_{i-2})}}, \quad T_{mn}^{p,up} = \prod_{i=n+1}^m e^{-jk_z^i(z_i-z_{i-1})} S_{i,i-1}^{p,up}. \tag{18}$$

Complex exponential functions are used to approximate the total spectrum domain Green's function. The spectrum domain Green's function can be divided into three terms, primary field, surface wave, and complex image, as

$$\tilde{G} = \tilde{G}_{pri} + \tilde{G}_{sw} + \tilde{G}_{ci} \tag{19}$$

Here, \tilde{G}_{pri} is the direct coupling from the observation point to the source point. \tilde{G}_{sw} is the surface wave contribution, due to the poles in k_ρ . \tilde{G}_{ci} is the contribution of complex images and physically represents spherical waves. The three terms in spectrum domains are

$$\begin{aligned}\tilde{G}_{pri} &= \frac{e^{-jk_z^m |z|}}{2jk_z^m} \\ \tilde{G}_{ci} &= \sum_i^{N_G} \frac{a_i e^{-b_i k_z^m}}{2jk_z^m} \\ \tilde{G}_{sw} &= \sum_j^{N_p} \frac{2k_{\rho j} \text{Re } s_j}{k_\rho^2 - k_{\rho j}^2},\end{aligned}\tag{20}$$

Here, the source point is located in m layer and r is the distance between source point and observation point. The pole for surface is extracted following the pole extraction procedures in [37]. N_G is the number of complex images. a_i the coefficient of the i^{th} image. r_i the complex distance of the i^{th} image. N_p is the number of poles. k_ρ is the transverse propagation wave number. $k_{\rho j}$ and $\text{Re } s_j$ are the j^{th} surface-wave pole and residue. After the subtraction of primary field, and surface-wave poles, the remaining portion of the spectrum-domain Green Function can be written in the form of spherical waves using GPOF with the integration path formed by uniform samples along $k_z^m = k_m [-jt + (1-t/T_0)]$. Here, t is a running parameter from 0 to T_0 to represent a complex variable k_z^m . The accuracy of the GPOF is related to the value of T_0 and number of sampling points.

The three parts in the decomposition process has physical meanings. The primary field describes the direction coupling between the source and observation. The complex image term describes the image effects from the boundaries, and surface wave is related to the pole locations. For surface wave, the pole extraction is based on the two criteria, shown in (24) and (25) in [37] to eliminate the effects of branch cut. Here, \tilde{G} and \tilde{G}' are the spectral-domain Green's functions when $\text{Im}(k_m^z < 0)$ and $\text{Im}(k_m^z > 0)$.

$$|\text{Res}| = \left| \frac{1}{2\pi j} \oint_{C_r} (\tilde{G} + \tilde{G}') dk_\rho \right| > e \quad (21)$$

$$|\text{Res}| = \left| \frac{1}{2\pi j} \oint_{C_r} \tilde{G} dk_\rho \right| > e \quad (22)$$

By using Sommerfeld identify [32][33], the three terms can be transformed to spatial domain. The three terms are summed in spatial domain to represent the total spatial domain LGFs. The expressions for the three terms in spectrum domain are

$$\begin{aligned} G_{pri} &= \frac{1}{4\pi r} e^{-jk_m r} \\ G_{ci} &= \sum_i^{N_G} \frac{1}{4\pi} a_i \frac{e^{-jk_m r_i}}{r_i}, r_i = \sqrt{(-jb_i)^2 + \rho^2} \\ G_{sw} &= \sum_j^{N_p} \frac{-j2\pi}{4\pi} \text{Re } s_j H_0^{(2)}(k_{\rho j} \rho) k_{\rho j} \end{aligned} \quad (23)$$

And the total spatial domain Green's function can be calculated as the summation of the three terms, as

$$G = G_{pri} + G_{sw} + G_{ci} \quad (24)$$

Here, G_{pri} represents the primary field. G_{ci} represents the spherical wave from complex images. G_{sw} represents the surface wave due to poles. The total spatial domain layered Green's function is written as

2.2. LAYERED GREEN'S FUNCTION VALIDATION

Several stack-ups are used to validate the layered Green's function calculation following the procedures shown in Section 2.1. Complex image identify and poles for surface wave extraction are validated first. Then a microstrip case from [36] and a five layer stack-up [32] are used to validate the complete procedures.

A half space stack-up shown in Figure 2.4 is used to validate the complex image identification. Image theory can be used in this case. The analytical expressions for the half space Green's functions are

$$\begin{aligned} G_A &= \frac{\mu_0 e^{-jk r_1}}{4\pi r_1} - \frac{\mu_0 e^{-jk r_2}}{4\pi \epsilon_0 r_2} \\ G_\varphi &= \frac{e^{-jk r_1}}{4\pi \epsilon_0 r_1} - \frac{e^{-jk r_2}}{4\pi \epsilon_0 r_2} \end{aligned} \quad (25)$$

The LGFs from DCIM is compared with the analytical formulas. Good correlation is shown in Figure 2.5 and Figure 2.6. There is no pole found in the pole extraction as expected. The image location is the same as analytical expressions. From the comparison, the complex image extraction in DCIM is correct.

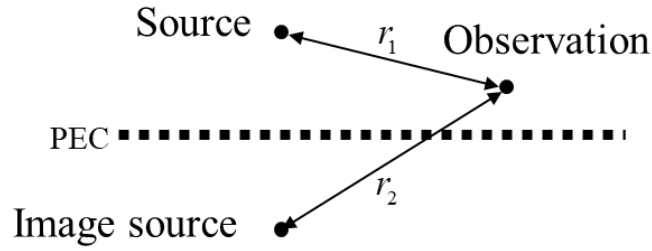


Figure 2.4. A half space stack-up case.

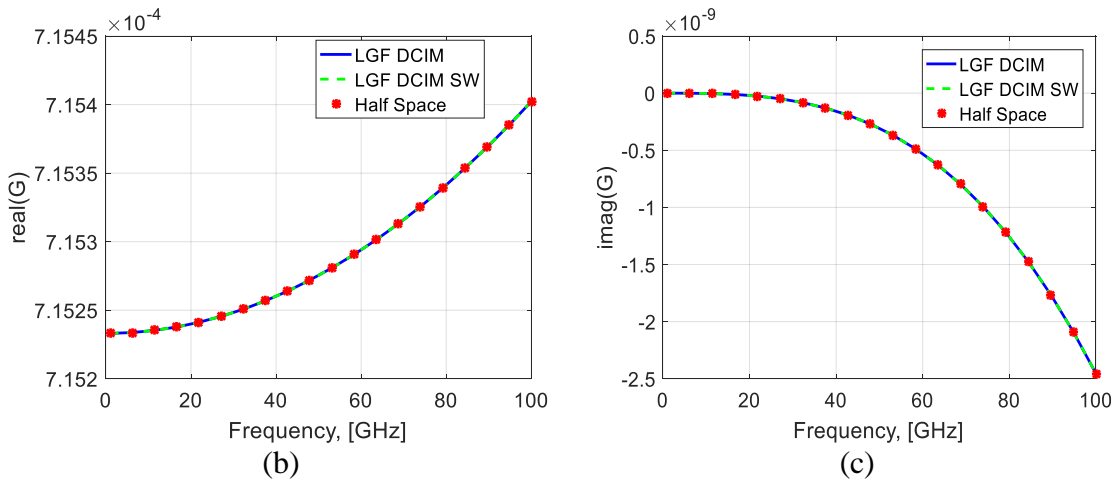


Figure 2.5. G_{xx}^A for the half space stack-up (a) The real part of G_{xx}^A . (b). The imaginary part of G_{xx}^A .

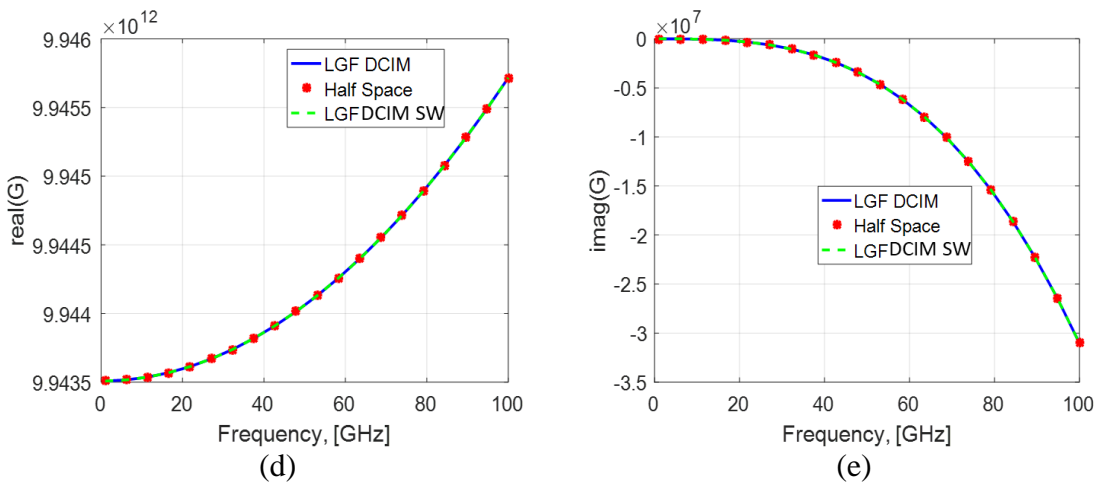


Figure 2.6. G_ϕ for the half space stack-up (a) The real part of G_ϕ . (b). The imaginary part of G_ϕ .

A microstrip case from [36] is used to validate the each step in the LGF extraction, as shown in Figure 2.7. Analytical formulas for the spectrum domain Green's function is included in [36] for the microstrip case. The spectrum domain Green's functions based on transmission-line Green's functions are compared with the analytical formulas. Good correlation for both \tilde{G}_{xx}^A and \tilde{G}_φ is observed, as shown in Figure 2.8 (a) and Figure 2.8 (b). Also, the pole location is clearly observed in Figure 2.8 (a) and Figure 2.8 (b), which is the same as the pole extraction using the method in [37].

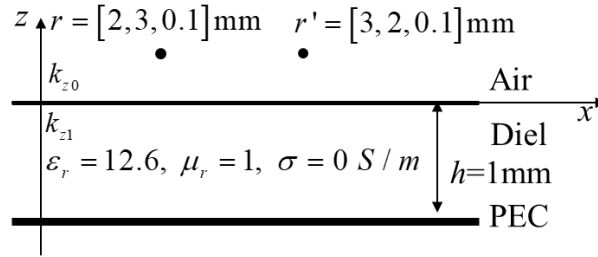


Figure 2.7. A microstrip stack-up case.

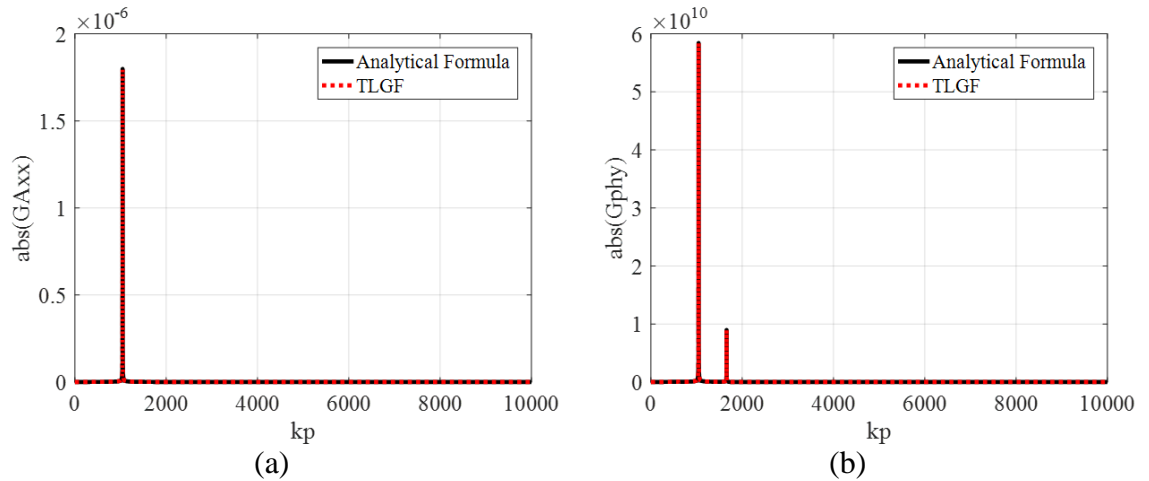


Figure 2.8. Spectrum domain LGF comparison using transmission line Green's function with the formulas from [36]. (a) \tilde{G}_{xx}^A comparison (b). \tilde{G}_φ comparison.

Then the spatial domain Green's function from DCIM is compared the numerical integration of the kernel along the Sommerfeld integral path, as shown in Figure 2.9. Good correlation proves that the LGF extracted from DCIM is correct.

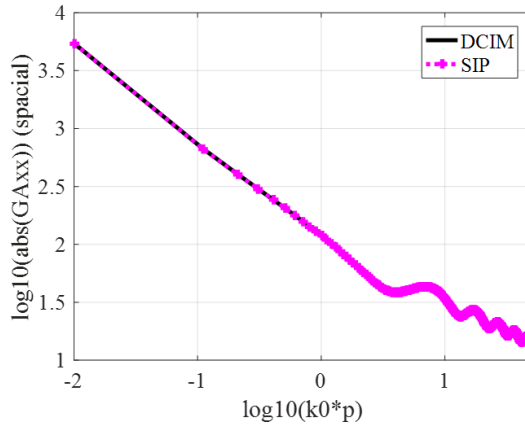


Figure 2.9. The spatial domain Green's function comparison using DCIM and Sommerfeld integral path for G_{xx}^A .

A five-layer media [32] shown in Figure 2.10 is used as a second example to show the LGF calculation. The source and observation points are in different layers. The spectrum domain Green's function is calculated using the transmission-line Green's function. One pole is found for \tilde{G}_{xx}^A , as labeled in Figure 2.11 (a). The pole identified using the method in [37] is $k_\rho = 1092.7$ rad/m. The difference comes from the resolution. The numerical identification using the method in [37] is more accurate than manual identification. Two poles are found for \tilde{G}_φ , as labeled in Figure 2.11 (b). The poles identified using the method in [37] are $k_\rho = 1092.7$ rad/m and $k_\rho = 1531.8$ rad/m, which can be observed in Figure 2.11 (b).

	ε_r, h
	1.0, ∞
$z = 1.4 \text{ mm}$	• 2.1, 0.7
	12.5, 0.3
$z' = 0.4 \text{ mm}$	• 9.8, 0.5
	8.6, 0.3

Figure 2.10. A five layer stack-up case.

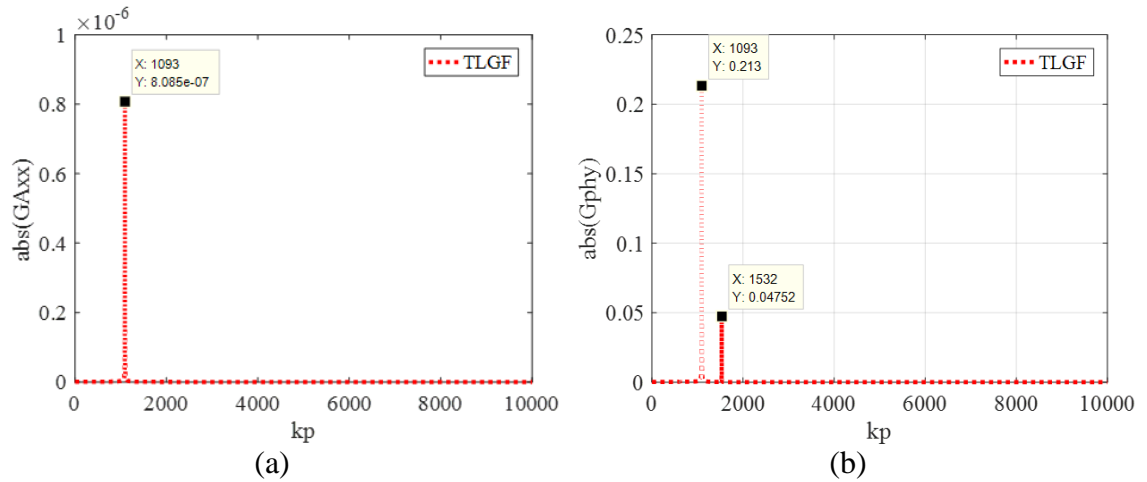


Figure 2.11. The spectrum domain LGFs. (a) \tilde{G}_{xx}^A with one pole found around $k_p = 1092 \text{ rad/m}$. (b). \tilde{G}_{ϕ} with two poles found around $k_p = 1093 \text{ rad/m}$, and $k_p = 1532 \text{ rad/m}$.

The three terms in the spatial Green's functions for the five-layer stackup are analyzed, as shown in Figure 2.12 (a) and Figure 2.12 (b). In this case, G_{xx}^A is dominated by the direct coupling from primary field, and surface wave. The contribution of complex images is small. In G_{ϕ} , the contributions from the three terms are important and cannot be ignored.

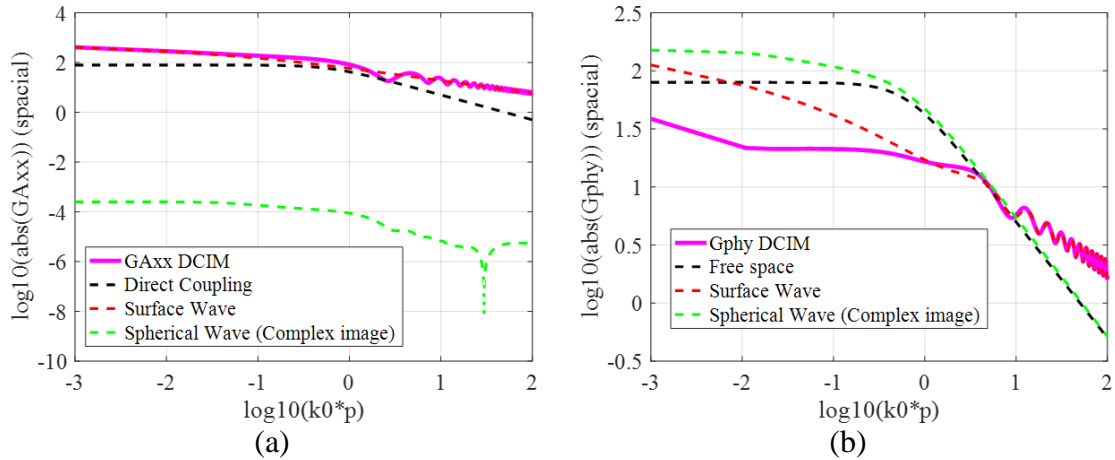


Figure 2.12. Three terms in spatial domain LGFs. (a). The three terms in G_{xx}^A . (b). The three terms in G_{ϕ} .

2.3. LAYERED GREEN’S FUNCTION IN 3D IC/PACKAGES

Four stack-ups are used here to identify the critical pieces in the LGFs for 3D IC/packaging systems. The first case is for the scenario that geometries are above silicon interposer and silicon dioxide. The source point and observation point are above silicon and silicon dioxide, as shown in Figure 2.13 .

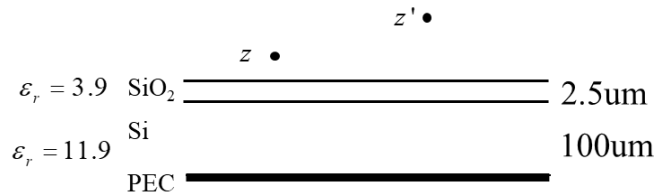


Figure 2.13. The analysis of LGFs in chip stack-up, case 1. The source and observation points are above the silicon dioxide and silicon interposer.

The three terms in the spatial domain G_A^{xx} and G_{ϕ} are analyzed, as shown in Figure 2.14 (a) and Figure 2.14 (b). There is no pole found in G_A^{xx} , which leads to no surface wave

contribution in G_A^{xx} . The number of complex images found is 6. And the contribution of the total complex image to G_A^{xx} is very small compared to direction coupling portion. Thus, only the direct coupling is needed for G_A^{xx} when structures are added on top of silicon interposer and silicon dioxide. For G_φ , one pole is found at $k_\rho = 629.9$ rad/s. When the highest frequency of interest is 50GHz, dimension on chip varies from 1um to 100 um, and the permeability of dielectrics in 3D IC/package systems varies from 1 to 20, then the range of $\log_{10}(k \times \rho)$ is from -2 to -0.3. In this range, the surface wave contribution to G_φ is very small and can be neglected. There are 13 complex images found for this stack-up in G_φ . And G_φ is dominated by direction coupling and complex images.

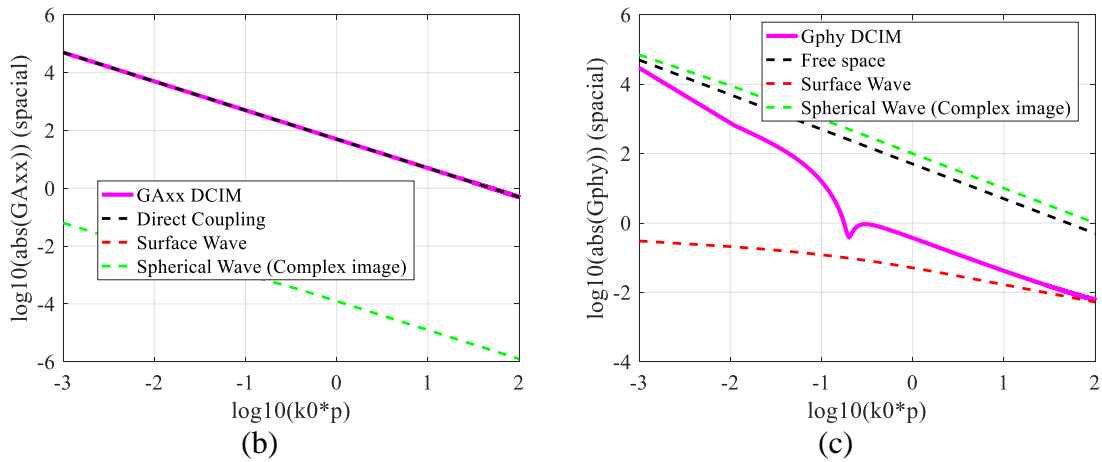


Figure 2.14. Direct coupling, complex image contribution, and surface in (a) G_{xx}^A and (c) G_φ for the stack-up shown in (b).

The second case is for the scenario that geometries are inside dielectric, above silicon interposer and silicon dioxide. The source point and observation point are as shown in Figure 2.15. The case is to represent the structures in the dielectric on chip.

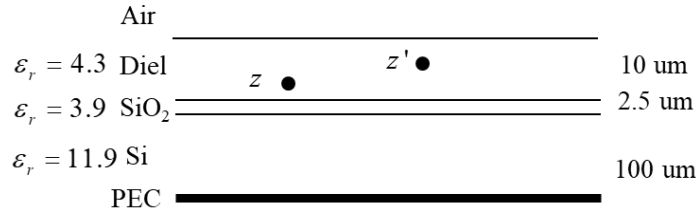


Figure 2.15. The analysis of LGFs in chip stack-up, case 2. The source and observation points are inside a dielectric, above the silicon dioxide and silicon interposer.

Similar analysis for LGFs is performed on this case. The three terms in the spatial domain G_A^{xx} and G_φ are analyzed, as shown in Figure 2.16 (a) and Figure 2.16 (b). There is no pole found in G_A^{xx} as well. The number of complex images found in G_A^{xx} is also 6. And the contribution of the total complex image to G_A^{xx} is very small. G_A^{xx} is dominated by direct coupling for this case. For G_φ , one pole is found at $k_\rho = 630.1$ rad/s, and there are 14 complex images located. For this geometry, the surface wave contribution is also very small. G_φ is dominated by direction coupling and complex images.

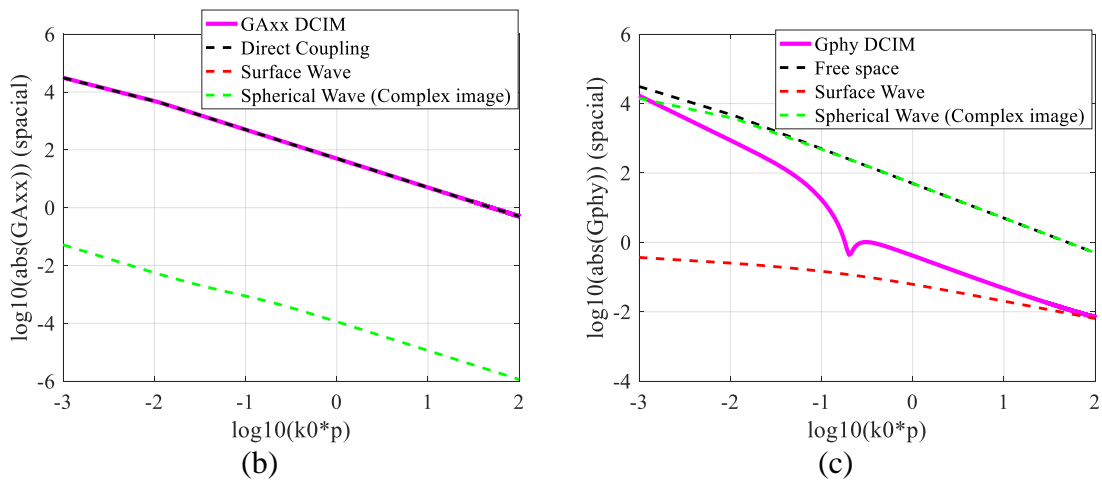


Figure 2.16. Direct coupling, complex image contribution, and surface analysis in (b) G_A^{xx} and (c) G_φ or the stack-up shown in Figure 2.15.

The third case is for the scenario that geometries are inside different dielectrics, above silicon interposer and silicon dioxide. The source point and observation point are as shown in Figure 2.17. The three parts in the spatial domain G_A^{xx} and G_φ are shown in Figure 2.18 (a) and Figure 2.18 (b). There is still no pole found in G_A^{xx} . The number of complex images found in G_A^{xx} is 6. And G_A^{xx} is dominated by direct coupling for this case. For G_φ , one pole is found at $k_\rho = 630.3$ rad/m, and there are 14 complex images located. For this geometry, G_φ is dominated by direction coupling and complex images.

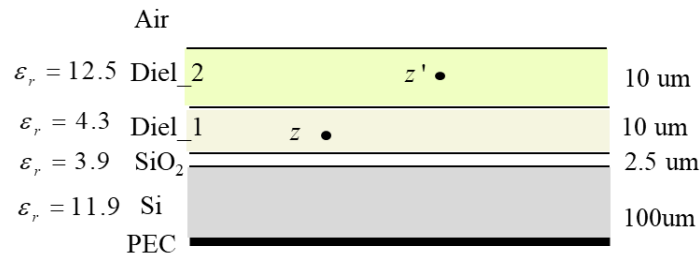


Figure 2.17. The analysis of LGFs in chip stack-up, case 3. The source and observation points are in different dielectrics, above the silicon dioxide and silicon interposer.

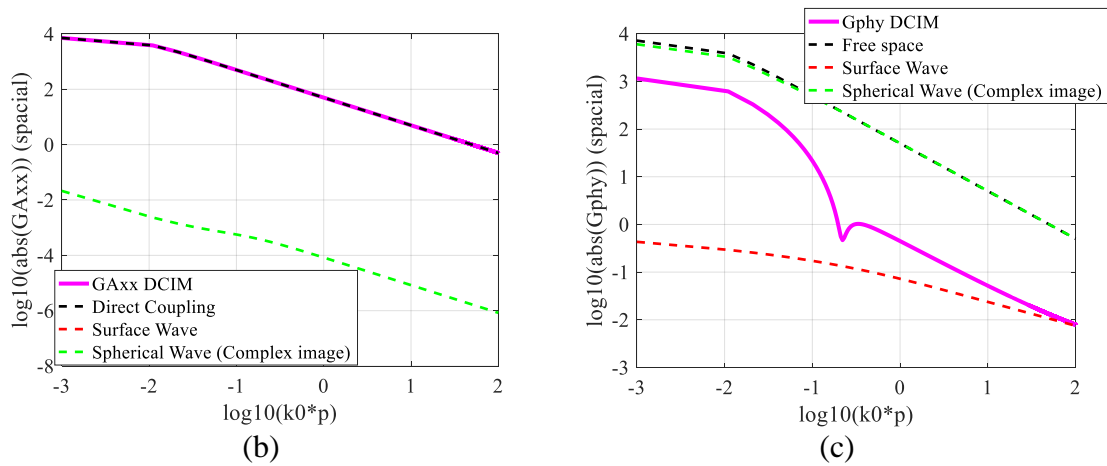


Figure 2.18. Direct coupling, complex image contribution, and surface analysis in (b) G_A^{xx} and (c) G_φ for the stack-up shown in Figure 2.17.

The fourth case is for the scenario that geometries are inside different chips. The source point is in Chip 1 and the observation point is in Chip 2, as shown in Figure 2.19. The three parts in the spatial domain G_A^{xx} and G_ϕ are shown in Figure 2.20 (a) and Figure 2.20 (b). There is no pole found in G_A^{xx} , and the number of complex images found in G_A^{xx} is 7. G_A^{xx} is dominated by direct coupling for this case. For G_ϕ , one pole is found at $k_\rho = 634.5$ rad/m, and there are 14 complex images located. For this geometry, G_ϕ is dominated by direction coupling and complex images.

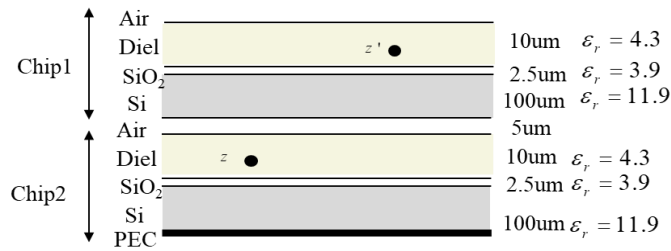


Figure 2.19. The analysis of LGFs in chip stack-up, case 4. The source and observation points are in different chips.

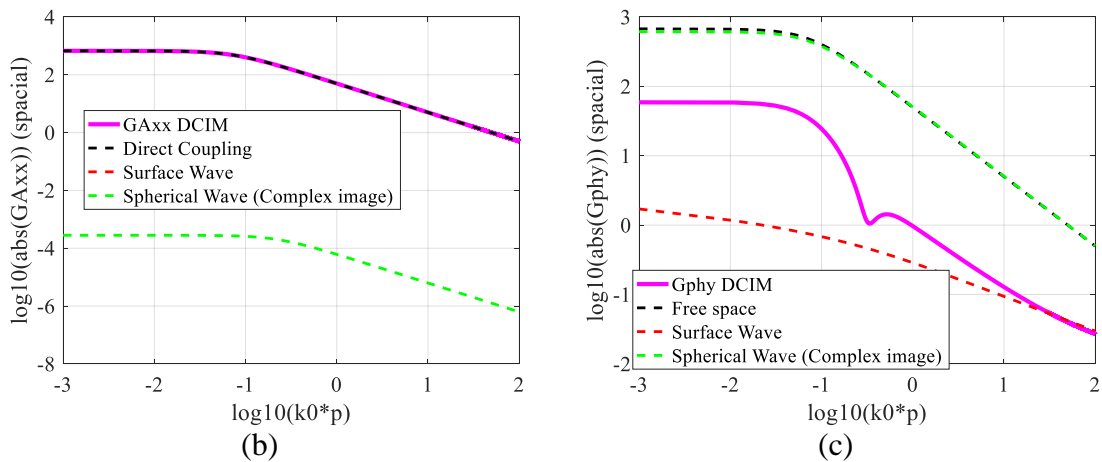


Figure 2.20. Direct coupling, complex image contribution, and surface analysis in (b) G_A^{xx} and (c) G_ϕ for the stack-up shown in Figure 2.19.

2.4. LOSS INFLUENCE IN 3D IC

The silicon substrate can be treated as a good conductor when the silicon substrate is heavily doped [38]. Quantifying the loss contribution due to lossy layered media is critical to 3D IC and packaging applications. By analyzing each term extracted from DCIM, it is observed that loss has two major effects on the layered Green's functions. The first effect is that loss changes the image locations and the effective distance of the images becomes complex values.

A source point in silicon substrate [39] is used to derive and validate the Green's function from DCIM. A half space in lossless and lossy silicon interpose shown in Figure 2.21 is used to illustrate the complex image location change due to loss. The source and observation points are at $z = 100\text{um}$. The spatial-domain G_{xx}^A and G_φ calculated from DCIM are shown in Figure 2.22 and Figure 2.23, respectively. The layered Green's function matches with the half space Green's function with only one complex image at $z = -100 + j1.8403 \times 10^{-9}\text{um}$ at 10MHz, and the coefficient for the complex image is -1. From Figure 2.22 and Figure 2.23 [39], loss influences both real and imaginary parts of Green's function for G_A^{xx} and G_φ . But the loss influence on real part of G_A^{xx} is relatively small. Also, since the real part of G_A^{xx} is much larger than the imaginary part, the loss influence on G_A^{xx} is relatively small. The loss has larger impacts on both the real part and imaginary part of G_φ , which shows that loss has large influence on the parasitic capacitance and conductance of the geometry.

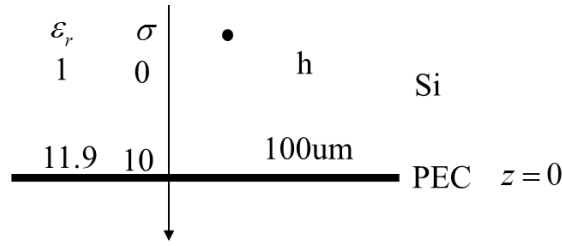


Figure 2.21. A layered media configuration to check the loss influence on layered Green’s function.

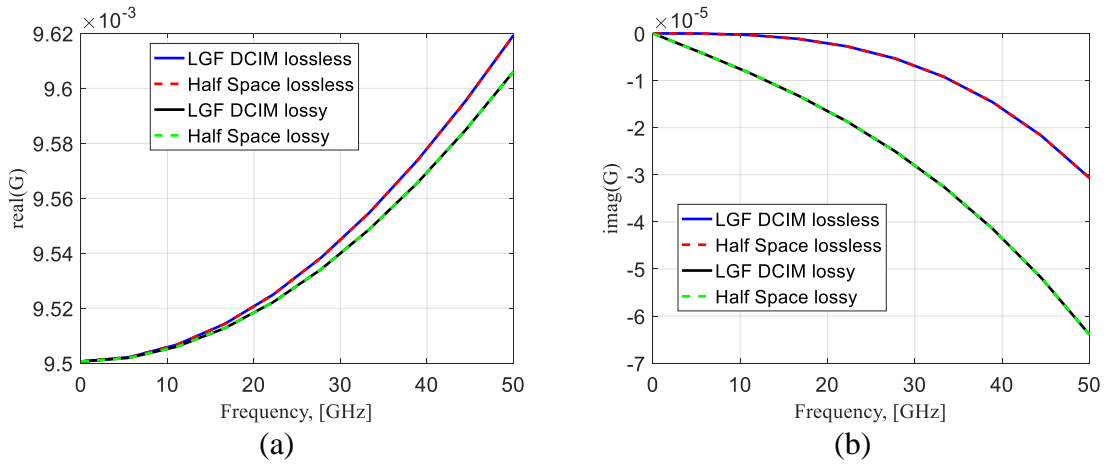


Figure 2.22. G_{xx}^A comparison from DCIM and half space Green’s function using complex image approach from 10MHz to 50GHz for lossless and lossy cases. (a). Real part of the Green’s function. (b). Imaginary part of the Green’s function.

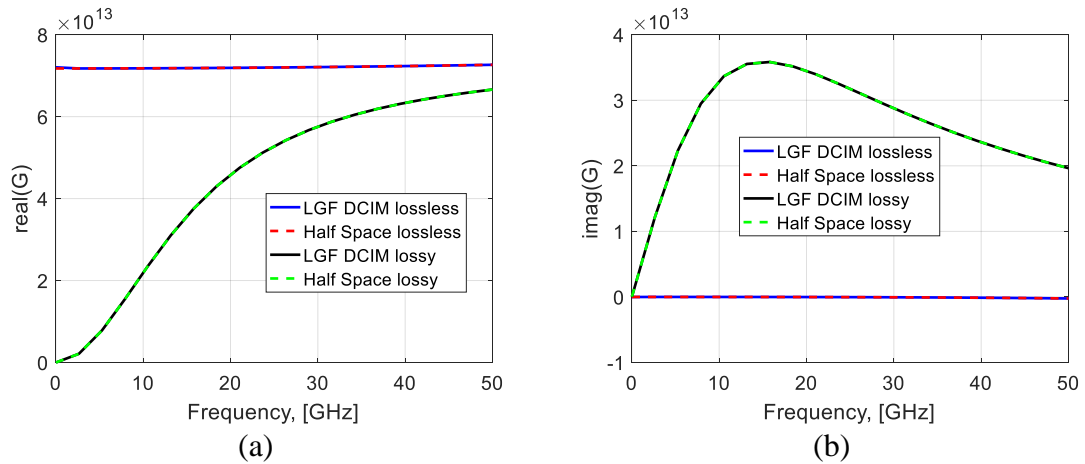


Figure 2.23. G^ϕ comparison from DCIM and half space Green’s function using complex image approach from 10MHz to 50GHz for lossless and lossy cases. (a). Real part of the Green’s function. (b). Imaginary part of the Green’s function.

The loss influence on near field and far field for both G_A^{xx} and G_φ for the stack-up in Figure 2.21 at 20 GHz is shown in Figure 2.24. Loss has larger impact on the LGFs in far field than that in near field for both real part and imaginary part of G_A^{xx} and G_φ . The loss impact on the real part of G_A^{xx} and G_φ in near field is very small.

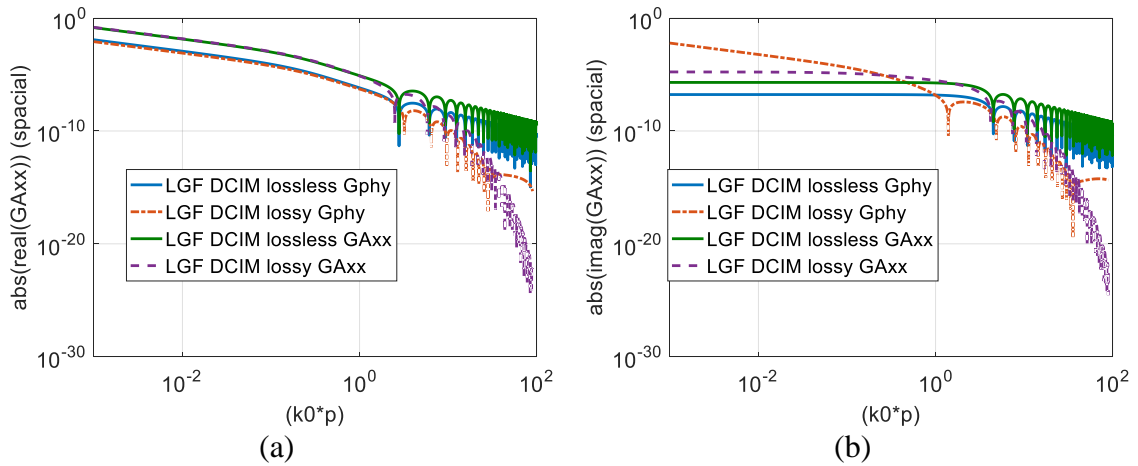


Figure 2.24. Spatial domain G_A^A and G_φ^φ comparison from DCIM for lossless and lossy cases at 20GHz. (a). Real part. (b) Imaginary part.

Two more stack-ups are used to illustrate the loss impacts on the LGFs. A source point and an observation point in the air above silicon interposer is analyzed here, as shown in Figure 2.25. The case is to observe the loss impact on the structures above silicon interposer. Similar analysis is performed. The loss influence on near field and far field for both G_A^{xx} and G_φ at 20GHz is shown in Figure 2.26 (a) and Figure 2.26 (b). The loss impact on G_A^{xx} and G_φ reduces compared to the case when observation point and source point are in silicon.

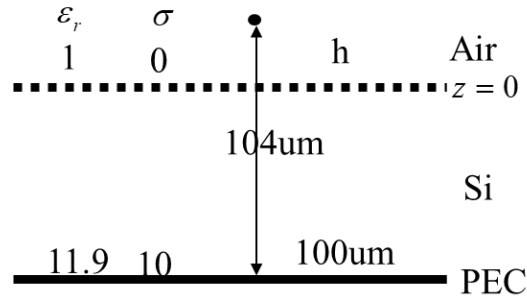


Figure 2.25. The first stack-up on chip to check loss impact for lossless and lossy cases at 20GHz.

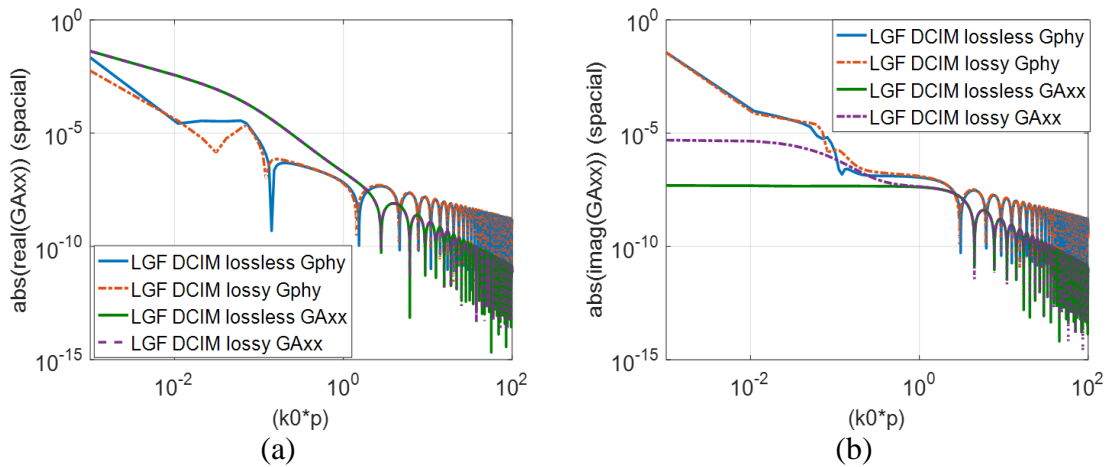


Figure 2.26. LGFs comparison from DCIM for lossless and lossy cases at 20GHz for the stack-up in Figure 2.25. (a). Real part. (b) Imaginary part.

A source point and an observation point in the air above silicon interposer and silicon dioxide is analyzed here, as shown in Figure 2.27. The loss influence on near field and far field for both G_A^{xx} and G_φ at 20GHz is shown in Figure 2.28 (a) and Figure 2.28 (b). The loss impact on G_A^{xx} and G_φ is similar to the case shown in Figure 2.25. The loss impact on G_A^{xx} and G_φ is relatively small for the real part and in the far field. The loss has larger impacts on the imaginary part of LGFs in the near field.

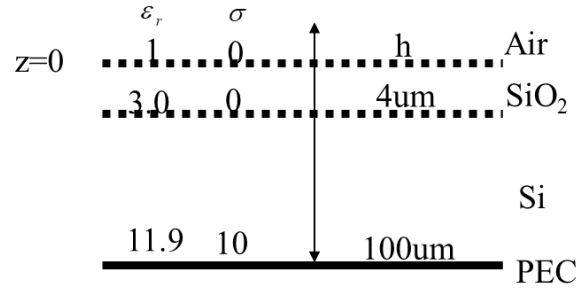


Figure 2.27. The second stack-up on chip to check loss impact for lossless and lossy cases at 20GHz.

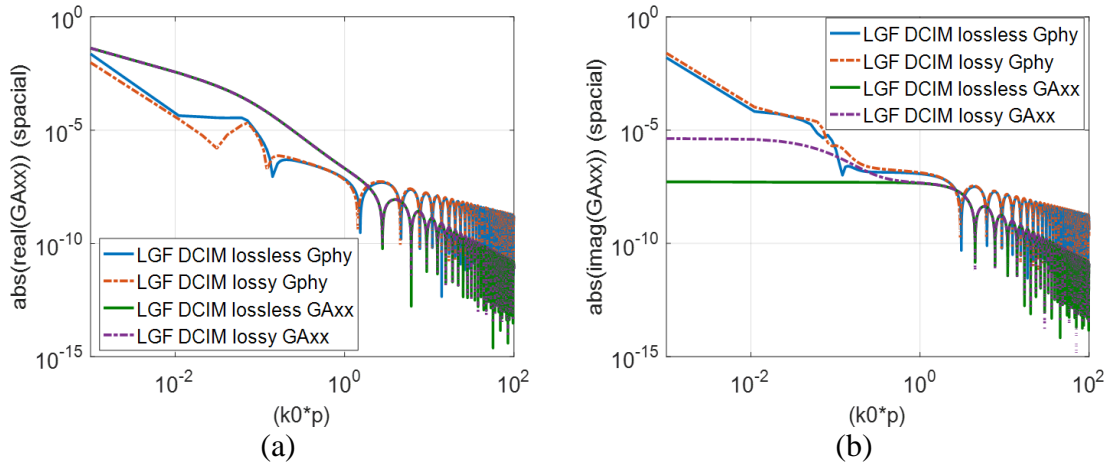


Figure 2.28. LGFs comparison from DCIM for lossless and lossy cases at 20GHz for the stack-up in Figure 2.27. (a). Real part. (b) Imaginary part.

The second effect of loss is that it changes the pole locations. The pole comes from the Sommerfeld integral with k_z in the denominator [36]. The pole location can be calculated as

$$k_z = \pm \sqrt{k^2 - k_x^2 - k_y^2} \quad (26)$$

$$k^2 = j\omega\mu(\sigma + j\omega\varepsilon) \quad (27)$$

Here, when σ is zero, the wave number k is a real number, and poles locate on real axis of k_z . When σ is non-zero, the poles will have imaginary part. A half space in lossless and lossy silicon interpose shown in Figure 2.29 is used to illustrate the complex image location change due to loss. The layer settings are changed to millimeter dimensions to enlarge the loss effect on pole locations. The TM wave poles when σ is 0 and 10 at 30GHz are shown in Figure 2.30 (a) and Figure 2.30 (b), respectively. It is observed that $\rho_{TM} = 5.971$ rad/cm for lossless case and, $\rho_{TM} = 6.085 + j0.096$ rad/cm for lossy case. The pole locations becomes complex when there is loss in the layered media.

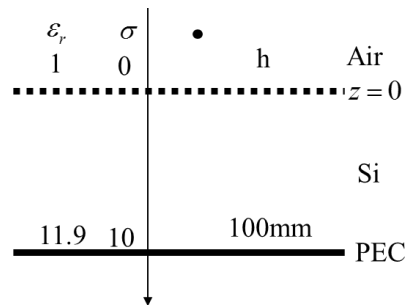


Figure 2.29. A layered media configuration to check the loss influence on pole locations.

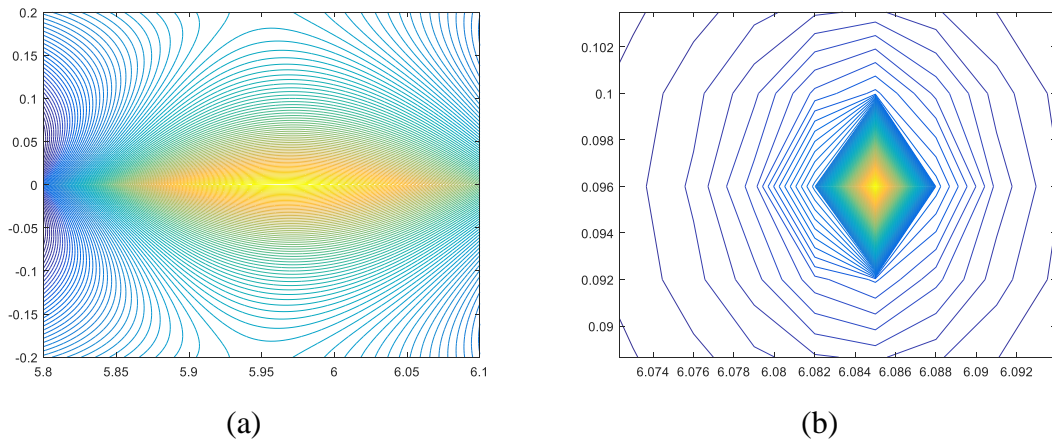


Figure 2.30. Pole locations for (a). lossless case and (b). lossy case. [35]

Loss in the layered media has two major impacts. One is that loss influences the image locations. Another is that loss influences pole locations. The Green's function for general layered media extracted from DCIM can be extended to more complex geometries with more layers. The image locations and number will change according to the frequency and layer settings. The proposed layered Green's functions can include the loss impacts in the calculation. Multiple major complex images can be identified. Also, it can extract poles to include the loss influence on surface wave. The layered Green's function extracted is suitable for 3D IC or packaging applications.

3. PARTIAL INDUCTANCE AND CAPACITANCE IN PEEC

3.1. PARTIAL INDUCTANCE AND CAPACITANCE WITH LGF

The LGFs calculated from DCIM can be integrated in the PEEC mesh cells to calculate partial inductance and capacitance for the cells. As both LGF calculation and numerical integration in the PEEC cells are time consuming, special procedures are needed for fast calculations. The details of handling LGF in PEEC are illustrated in this section. Also, since the partial inductance and capacitance for the cells in PEEC for 3D IC/package systems is frequency-independent, analytical formulas are proposed to include complex image contribution in PEEC capacitance calculation.

Two bars are used here to illustrate the partial inductance and capacitance calculation to include LGF in PEEC [40][41][42]. The mesh settings for inductance and capacitance calculations are shown in Figure 3.1, Figure 3.2 and Figure 3.3 for the two bars. The mesh cells are cuboid for partial inductance calculations. For partial mutual inductance calculation, a bar is firstly meshed along cross-section to obtain filaments, as shown from Figure 3.2 (a). Then the filaments are meshed along longitude direction, as shown in Figure 3.2 (b). For partial capacitance calculation, the six surfaces of a bar is meshed into rectangular small cells, as shown from Figure 3.3 (a) to Figure 3.3 (b).

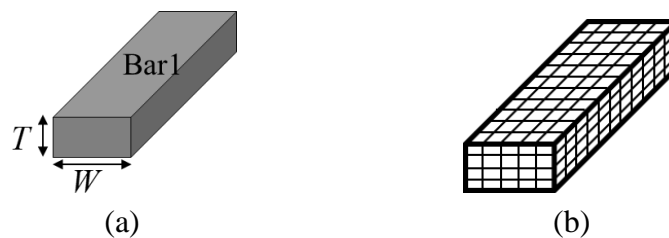


Figure 3.1. Cuboid mesh settings for partial self-inductance calculation. (a). A bar with the dimensions labeled. (b). The cuboid mesh for the bar in (a).

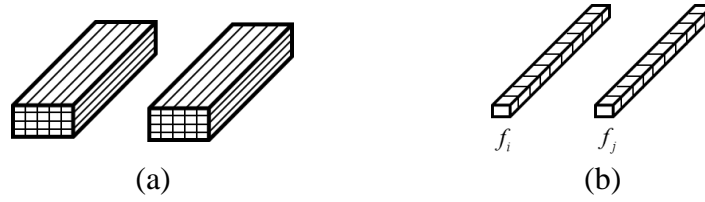


Figure 3.2. Cuboid mesh settings for partial mutual inductance calculation. (a). The filament settings for partial mutual inductance calculation. (b). Meshes on filaments.

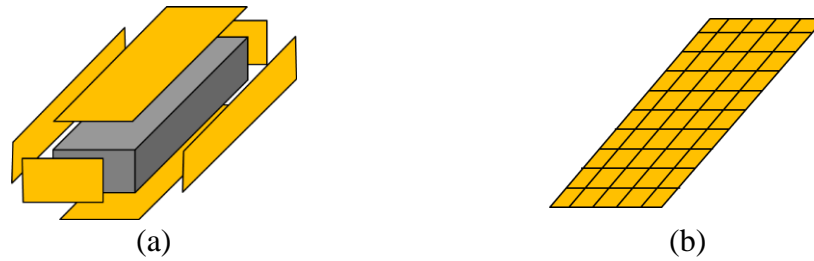


Figure 3.3. Surface mesh settings for six surfaces in a bar for partial capacitance calculation.

The PEEC formulation for the partial inductance and capacitance is illustrated here based on the cells shown in Figure 3.1 and Figure 3.3. The formulation for partial self-inductance calculation in PEEC [41] is

$$L_{pii} = \frac{1}{T^2 W^2} \int_{a_i} \int_{a_{i'}} \int_0^l \int_0^{l'} G(\bar{r}, \bar{r}') \left| d\vec{l}_i \cdot d\vec{l}_{i'} \right| da_i da_{i'} \quad (28)$$

Here, \bar{r} and \bar{r}' are the observation and source locations. $G(\bar{r}, \bar{r}')$ is the Green's function. a_i and $a_{i'}$ are the cross-section of i^{th} and i'^{th} inductance mesh cells for source and observation. l and l' are the longitude length of i^{th} and i'^{th} inductance mesh cells. In (28), the Green's function has singularity when $\bar{r} = \bar{r}'$. To handle the singularity using

Duffy method [43], the surface integration along the cross-section surface is considered directly and explained later. Applying Legendre-Gauss Quadrature along the longitude direction of a bar to (28), the partial self-inductance calculation is changed to

$$L_{pii} = \frac{1}{T^2 W^2} \sum_{a_i} w_{a_{xi}} w_{a_{yi}} \sum_l w_l \int_0^{l'} \int_{a_i'} G(\bar{r}, \bar{r}') dl' da_i' \quad (29)$$

Here, $w_{a_{xi}}$, $w_{a_{yi}}$ and w_l are Gaussian weights along x , y (cross-sectional coordinates) and longitude for the i^{th} inductance mesh cell. The formulation for partial mutual inductance calculation is defined as

$$L_{pij} = \frac{1}{a_i a_j} \int_{a_i} \int_{a_j} L_{pfi j} da_i da_j \quad (30)$$

Here, the partial filament $L_{pfi j}$ inductance [41] is defined as

$$L_{pfi j} = \frac{\mu}{4\pi} \int_{b_i}^{c_i} \int_{b_j}^{c_j} G(\bar{r}, \bar{r}') |d\vec{l}_i \cdot d\vec{l}_j| \quad (31)$$

Where, a_i and a_j are the cross-section of i^{th} and j^{th} inductance mesh cells for source and observation. l_i and l_j are the longitude length of i^{th} and j^{th} inductance mesh cells. Applying Legendre-Gauss Quadrature to (8) along three directions, the partial mutual inductance can be calculated as

$$L_{p_{ij}} = \frac{\mu}{4\pi T^2 W^2} \sum_{a_i} \sum_{l_i} w_{a_{xi}} w_{a_{yi}} w_{l_i} \sum_{a_j} \sum_{l_j} w_{a_{xj}} w_{a_{yj}} w_{l_j} G(\bar{r}_{a_i l_i}, \bar{r}_{a_j l_j}) \quad (32)$$

Here, $w_{a_{xi}}$, $w_{a_{yi}}$ and w_{l_i} are Gaussian weights for the i^{th} inductance mesh cell. And $w_{a_{xj}}$, $w_{a_{yj}}$ and w_{l_j} are Gaussian weights for the j^{th} inductance mesh cell. The partial capacitance is calculated from sub-coefficients of capacitance c_s . And c_s is calculated as $c_s = ps^{-1}$. Here ps is the coefficient of potential matrix [42], and is defined as

$$ps_{ij} = \frac{1}{S_i S_j} \int_{S_i} \int_{S_j} G(\bar{r}, \bar{r}') ds' ds \quad (33)$$

Here, \bar{r} and \bar{r}' are the observation and source locations. $G(\bar{r}, \bar{r}')$ is the corresponding Green's function for capacitance calculation. S_i and S_j are the surface of i^{th} and j^{th} capacitance mesh cells for source and observation. The equation also has singularity when $\bar{r} = \bar{r}'$. For $\bar{r} \neq \bar{r}'$, Legendre-Gauss Quadrature can applied directly to (9), as

$$\int_{S_i} \int_{S_j} G(\bar{r}, \bar{r}') ds' ds = \sum_{S_i} \sum_{S_j} w_{s_i} w_{s_j} G(x_{s_i}, x_{s_j}) \quad (34)$$

Here, w_{s_i} and w_{s_j} are Gaussian weights for the i^{th} and j^{th} capacitance mesh cell. x_{s_i} , and x_{s_j} are the Gaussian nodes in the i^{th} and j^{th} capacitance mesh cell.

Duffy method [43] is used to handle singularity in formula (6) and (9), as shown Figure 3.4. In Duffy method, the rectangular integration is divided into four triangular with

the singularity point to be one vertices of the triangular and the other two vertices from the rectangular, Then the coordinates of the triangular in \bar{r} is mapped into a new domain (u - v).

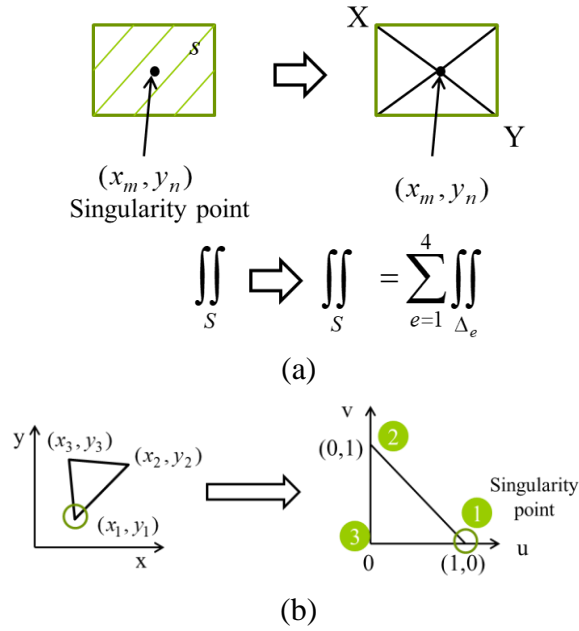


Figure 3.4. Duffy method to handle the singularity inside integrations. (a) Divide the integration in a rectangular to four triangular. (b). Domain mapping for the coordinates in a triangular.

Using Duffy method, formula (6) and (9) are changed to

$$\int_{a_i'} \int_0^{l_i'} G(\bar{r}, \bar{r}') dl' da_i' = \sum_{l'} w_l' \sum_{a_i'} w_{a_i'} \int_{a_i'} G(\bar{r}, \bar{r}') da_i' \quad (35)$$

$$\int_{S_i} \int_{S_j} G(\bar{r}, \bar{r}') ds' ds = \sum_{S_i} w_{S_i} \int_{S_j} G(\bar{r}, \bar{r}') ds' \quad (36)$$

The formulation of the procedure for (12) is shown as

$$\begin{aligned}
\int_{S_i} \int_{S_j} G(\bar{r}, \bar{r}') ds' ds &= \int_0^1 \int_0^{1-u} \int_{S_j} \frac{e^{-jk|\bar{r}(u,v,z) - \bar{r}'(x,y,z)|}}{\sqrt{(p(u,v) - x_j)^2 + (q(u,v) - y_j)^2 + (z - z_j)^2}} ds' dudv \\
&= \int_0^1 \int_0^1 \int_{S_j} \frac{(1-u)e^{-jk|\bar{r}(u,v,z) - \bar{r}'(x,y,z)|}}{\sqrt{(p(u, (1-u)s) - x_j)^2 + (q(u, (1-u)s) - y_j)^2 + (z - z_j)^2}} ds' dudv
\end{aligned} \tag{37}$$

3.2. COMPLEXITY REDUCTION

Both LGF calculation and numerical integration in the PEEC cells are time consuming. And numerical integration using LGF in every mesh cells can lead to high computational cost. To include the layered media impacts in PEEC model, several acceleration treatments are used. The first one is to avoid calculating LGF repeatedly. The LGF calculation procedure is divided into two steps. The first one is to find surface wave and complex image information. And when it comes to the use of Green's function in PEEC integration, the surface wave and complex image information can be used to form the spatial domain Green's function. The second one treatment is to separate singularity term and use the PEEC analytical formulas calculated from free space Green's function to calculate partial inductance and capacitance. From the LGFs analysis shown in Section II, for 3D IC/package systems, G_{xx}^A is dominated by the direct coupling. And G_{φ} is dominated by direct coupling and complex images. For partial inductance calculation, the analytical formulas using free space Green's function without retardation can be used for partial inductance calculation. The formulas used for partial inductance calculation are included in. For partial capacitance calculation, to include the contribution of complex images, (9) can be changed to

$$\begin{aligned}
p_{S_i S_j} &= \frac{1}{S_i S_j} \int_{S_i} \int_{S_j} \left[\frac{1}{4\pi r} + \sum_{N_p} \frac{1}{4\pi r_i} \right] ds' ds \\
&= \frac{1}{S_i S_j} \int_{S_i} \int_{S_j} \frac{1}{4\pi r} ds' ds + \frac{1}{S_i S_j} \int_{S_i} \int_{S_j} \sum_{N_p} \frac{1}{4\pi r_i} ds' ds \\
&= \frac{1}{S_i S_j} \int_{S_i} \int_{S_j} \frac{1}{4\pi r} ds' ds + \frac{1}{S_i S_j} \frac{1}{4\pi} \sum_{N_p} \int_{S_i} \int_{S_j} \frac{a_i}{r_i} ds' ds
\end{aligned} \tag{38}$$

Here, $r_i = \sqrt{(-jb_i)^2 + \rho^2}$, The second term in (14) is similar to the first term. Analytical formulas can be derived to include the complex image contribution in (9). Here, b_i is always along z direction and ρ is along x and y directions.

Coordinates rotation can be used to derive analytical formulas to include the complex image contribution in the coefficient of potential matrix calculation. For capacitance mesh cells, the direction is defined as the direction perpendicular to the surface of the cells. For two mesh cells in bars, the direction of two cells has nine combinations, with 3 cases (zz , xx , yy , which represent the first sheet are along z direction and the second sheet along z direction, both along x and x direction, both along y and y direction, respectively) when the two cells are parallel, and 6 cases (xy , xz , yx , yz , zx , zy) when the two cells are perpendicular.

Two cases are shown in Figure 3.5 and Figure 3.6 to illustrate the coordinate rotation and how to change the analytical PEEC formulation derived using free space Green's function. In Figure 3.5 and Figure 3.6, the image for the first sheet is shown here for illustration. The location of the image should be decided using LGF. The coefficient of potential for two cells in parallel using the free space Green's function is

$$4\pi\epsilon_0\epsilon_r p s_{ij} = \frac{1}{f_a f_b s_a s_b} \sum_{k=1}^4 \sum_{m=1}^4 (-1)^{i+j} \left[\frac{b_m^2 - C^2}{2} a_k \ln(a_k + \rho) + \frac{a_k^2 - C^2}{2} b_m \ln(b_m + \rho) - \frac{1}{6} (b_m^2 - 2C + a_k^2) \rho - b_m C a_k \tan^{-1} \frac{a_k b_m}{\rho C} \right] \quad (39)$$

Where,

$$\rho = (a_k^2 + b_m^2 + C^2)^{1/2},$$

$$a_1 = a_{ij} - \frac{f_a}{2} - \frac{s_a}{2}, \quad a_2 = a_{ij} + \frac{f_a}{2} - \frac{s_a}{2}, \quad a_3 = a_{ij} + \frac{f_a}{2} + \frac{s_a}{2}, \quad a_4 = a_{ij} - \frac{f_a}{2} + \frac{s_a}{2},$$

$$b_1 = b_{ij} - \frac{f_b}{2} - \frac{s_b}{2}, \quad b_2 = b_{ij} + \frac{f_b}{2} - \frac{s_b}{2}, \quad b_3 = b_{ij} + \frac{f_b}{2} + \frac{s_b}{2}, \quad b_4 = b_{ij} - \frac{f_b}{2} + \frac{s_b}{2}.$$

And the coefficient of potential for two cells in parallel using the free space Green's function is

$$4\pi\epsilon_0\epsilon_r p s_{ij} = \frac{1}{f_a f_c s_a s_b} \sum_{k=1}^4 \sum_{m=1}^4 \sum_{l=1}^2 (-1)^{l+m+k+1} \cdot \left[\left(\frac{a_k^2}{2} - \frac{c_l^2}{6} \right) c_l \ln(b_m + \rho) + \left(\frac{a_k^2}{2} - \frac{b_m^2}{6} \right) b_l \ln(c_l + \rho) + a_k b_m \ln(a_k + \rho) - \frac{b_m c_l}{3} \rho - \frac{a_k^3}{6} \tan^{-1} \left(\frac{b_m c_l}{a_k \rho} \right) - \frac{b_m^2 a_k}{2} \tan^{-1} \left(\frac{a_k c_l}{b_m \rho} \right) - \frac{a_k c_l^2}{2} \tan^{-1} \left(\frac{a_k b_m}{c_l \rho} \right) \right] \quad (40)$$

Where, ρ and a_k are defined as above and additionally,

$$b_1 = b_{ij} + \frac{s_b}{2}, \quad b_2 = b_{ij} - \frac{s_b}{2}, \quad c_1 = c_{ij} + \frac{f_c}{2}, \quad c_2 = c_{ij} - \frac{f_c}{2}.$$

To include the complex image contribution, the distance between the image sheet and the second sheet is $-jb_i$ along z direction for every image. Then the definition of a few parameters in (39) and (40) can be changed to represent the contribution of the i^{th} image to the coefficient of potential calculation. For the two sheet along zz direction, as shown in Figure 3.5, C can be changed to $-jb_i$ and then the weight of every image a_i is multiplied on the right side of (39) calculate the ps_{ij} due to the i^{th} image. For the two sheet along zy directions, c_{ij} is changed to $-jb_i$ and then the weight of every image a_i is multiplied on the right side of (40) calculate the ps_{ij} due to the i^{th} image. The details of the changes to (39) or (40) for the nine cases to include the contribution of the i^{th} image is listed in Table 3.1.

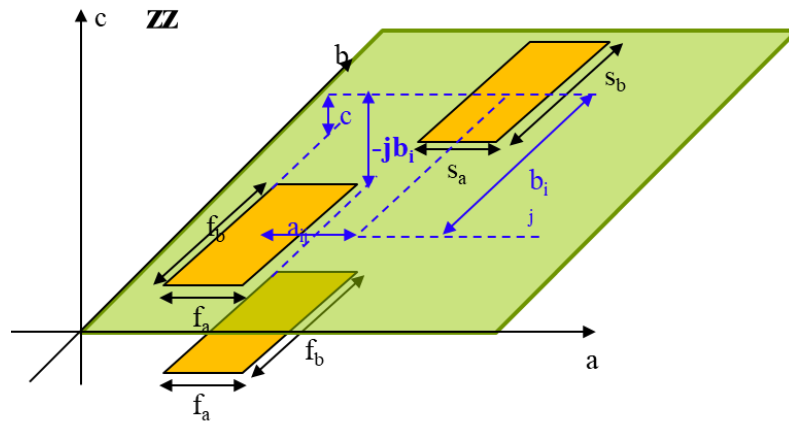


Figure 3.5. Potential coefficient calculation to include the contribution of complex images for two parallel rectangular conduction sheets.

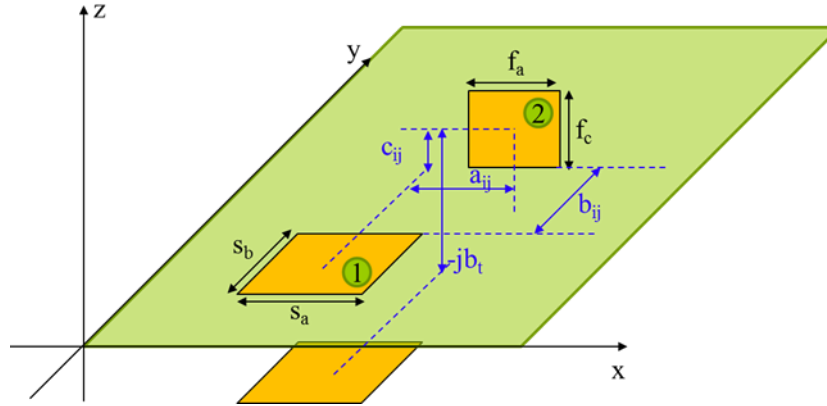


Figure 3.6. Potential coefficient calculation to include the contribution of complex images for two orthogonal rectangular conducting sheets.

Table 3.1. Formula change for two conducting sheets along different directions.

1 st sheet	2 nd sheet	Formula change
z	z	C changes to $ -jb_i $ in (39)
x	x	b_{ij} changes to $ -jb_i $ in (39)
y	y	a_{ij} changes to $ -jb_i $ in (39)
z	y	c_{ij} changes to $ -jb_i $ in (40)
z	x	c_{ij} changes to $ -jb_i $ in (40)
x	z	b_{ij} changes to $ -jb_i $ in (40)
x	y	a_{ij} changes to $ -jb_i $ in (40)
y	z	b_{ij} changes to $ -jb_i $ in (40)
y	x	a_{ij} changes to $ -jb_i $ in (40)

3.3. PARTIAL INDUCTANCE AND CAPACITANCE VALIDATION

A two bar geometry is used to validate the partial inductance and partial capacitance calculation to include LGF in PEEC. Q3D is used to validate the formulation proposed in the previous sections. Even though the partial inductance is dominated by the direct

coupling for 3D IC/packing systems, boundary condition impact is not negligible. The partial inductance from PEEC using LGF for two bars is compared with the simulation results from Q3D and a good match is observed.

The comparison of partial inductance results is shown in Table 3.2 for three cases, free space case, half space case with a ground plane 1 μ m under the two bars, and IC environment with silicon interposer and ground plane under the two bars. For the third case, the distance between the bars and the silicon interposer is 1 μ m and the thickness of the silicon interposer is 100 μ m. The distance of ground plane to the bars is 101 μ m. The partial inductance for the two bars above silicon interposer is similar to that in the free space, which validates the conclusion that G_{xx}^A is dominated by the direct coupling. And the partial inductance in the half space is smaller than that in the other two cases. For inductance calculation, the key factor is the location of ground planes. Either free space Green's function or half space Green's function is needed for partial inductance calculation in 3D IC/packing systems.

The comparison of partial capacitance results is shown in Table 3.3 for three cases, half space case with a ground plane 1 μ m under the two bars, loose coupling and tight coupling in IC environment with silicon dioxide, silicon interposer and ground plane under the two bars. The two bars to the first layer or ground plane is 1 μ m for all cases. The thickness of silicon interposer is 100 μ m. The thickness of silicon dioxide is 1 μ m. The partial capacitance from the LGF using (39) and (40) with Table 3.1 of the three cases compares well with the simulation results from Q3D.

Table 3.2. Partial inductance calculation in Q3D and PEEC with LGF for different stackups

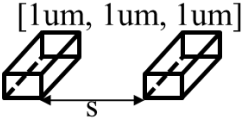
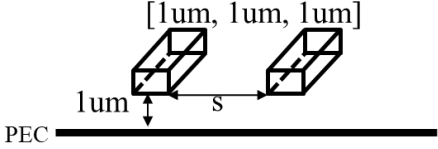
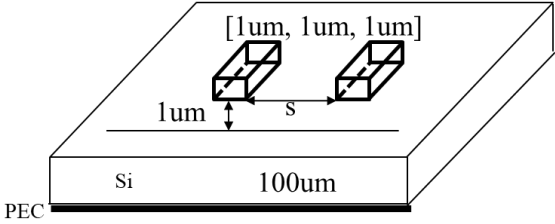
	Q3D	LGF
		
Self L	188.59 fH	191.56 fH
Mutual L	49.87 fH	49.91 fH
		
Self L	155.3 fH	158.2 fH
Mutual L	22.3 fH	22.2 fH
		
Self L	188 fH	191 fH
Mutual L	49.42 fH	49.41 fH

Table 3.3. Partial capacitance calculation in Q3D and PEEC with LGF for different stackups

	Q3D	LGF
Cs11	17.61 fF	17.89 fF
Cs12	-0.0120 fF	-0.0114 fF
Cs11	2.071	2.071
Cs12	-0.272	-0.273
Cs11	16.661	16.296
Cs12	-15.583	-15.201

4. CHIP PDN

Chip PDN is a grid geometry with many bars on different layers. The longitude directions for the bars in adjacent layer are perpendicular, as shown in Figure 4.1. Vias are used to connect the bars in the same net in different layers. Full wave simulation of chip PDN geometry can be time consuming since there can be large number of bars on many layers for an IC. With the layered media environment for 3D IC and packages, building an accurate model for chip PDN is challenging.



Figure 4.1. A 2-layer chip PDN geometry with bars in perpendicular directions for neighboring layers. Power and ground bars are placed alternating.

The PEEC modeling method with LGF can be used to extract the circuit model for the chip PDN geometry. The mesh settings for partial inductance and capacitance calculation in chip PDN is shown in Figure 4.2. The nodes are set to be the center of the crossing area of two perpendicular bars in adjacent layers. The inductance cuboid are between the nodes. The full capacitance cuboid has nodes in the middle along the longitude directions. And at the end of every bar, half cuboid are used for capacitance mesh.

The repeated structures in the chip PDN geometry can be used to reduce the horizontal complexity to extract the circuit model. For inductance calculation, there is no mutual inductance between two cuboid cells that are perpendicular to each other. Since the mutual inductance decreases with the increase of distance between two bars, only the

mutual partial inductance between the nearby bars are considered for the bars in the same layer. As shown in Figure 4.2 (a), for the cuboid 5, only eight mutual partial inductances are considered, as between cuboid 5 and cuboids 1, 2, 3, 4, 6, 7, 8 and 9. Also, as the mutual inductance is only relative locations, two cuboids with the same relative locations have the same mutual partial inductance. Thus, only eight values need to be calculated for the mutual partial inductance for the cuboids in the same layer. When the number of cuboids is large, the eight partial mutual inductances and one partial self-inductance can be used to construct the L matrix for the cuboids in the same layer regardless of the number of bars in the layer. For capacitance calculation, similar procedure can be implemented as well. But the partial mutual capacitance between the cuboids in the adjacent layers needs to be considered. The number of different cases is even larger since there are full cuboids and half cuboids in the mesh cells. The way to correctly use the method is to use the coefficient of potential matrix between two cuboids as unit matrix. The total coefficient of potential matrix is constructed by fill the different unit matrixes at the corresponding index. The loss included in the PEEC model is the resistance of every inductance cuboid calculated using

$$R = \frac{L}{\sigma S} \quad (41)$$

where L is the length of the cuboid along longitude direction. S is the cross-section area of the cuboid. σ is the conductivity of the conductor. An equivalent circuit model can be built following the net and geometry in PEEC [44].

A two layer chip PDN geometry shown in Figure 4.3 (a) is used to validate the proposed modeling method. There are ten bars on each layer. Power and ground bars are

placed in an alternating way between neighboring bars. A port and a short are set between the two nodes on the bottom layer circled in Figure 4.3 (a). The chip PDN is placed in free space, in half space with 5um above the ground plane, and 1um above silicon dioxide, silicon interposer and ground plane. The silicon dioxide thickness is 2.5 um. The thickness of the silicon interposer is 100 um. The input impedance comparison from PEEC with LGF and HFSS simulation is shown in Figure 4.3 (b) and Figure 4.3 (c). Good match is observed with some difference only the loss at the resonance frequencies.

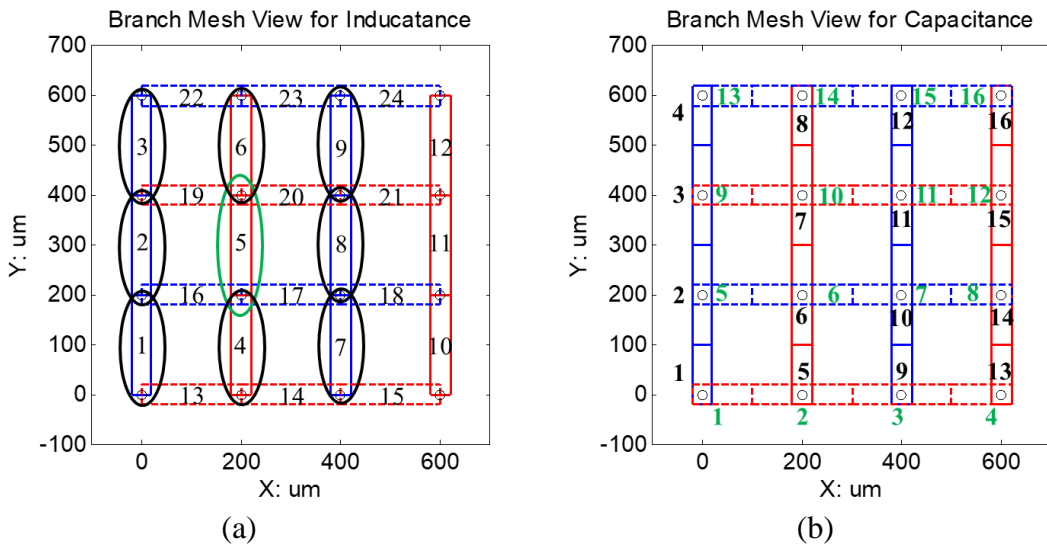


Figure 4.2. Top view of the chip PDN mesh settings for (a). Partial inductance calculation. (b) Partial capacitance calculation. Blue rectangular represents the ground bars. Red rectangular represents the power bar. Dashed line represents the bars are on the bottom layer. Solid line represents the bars are on the top layer.

The proposed method largely reduces the modeling complexity for 3D IC/packaging applications while maintaining the accuracy. Analytical formulas are used to include the complex image contribution in the partial capacitance calculation, which avoids

numerical integration and enables to use PEEC in complex 3D IC/packages to model the geometry quickly and accurately.

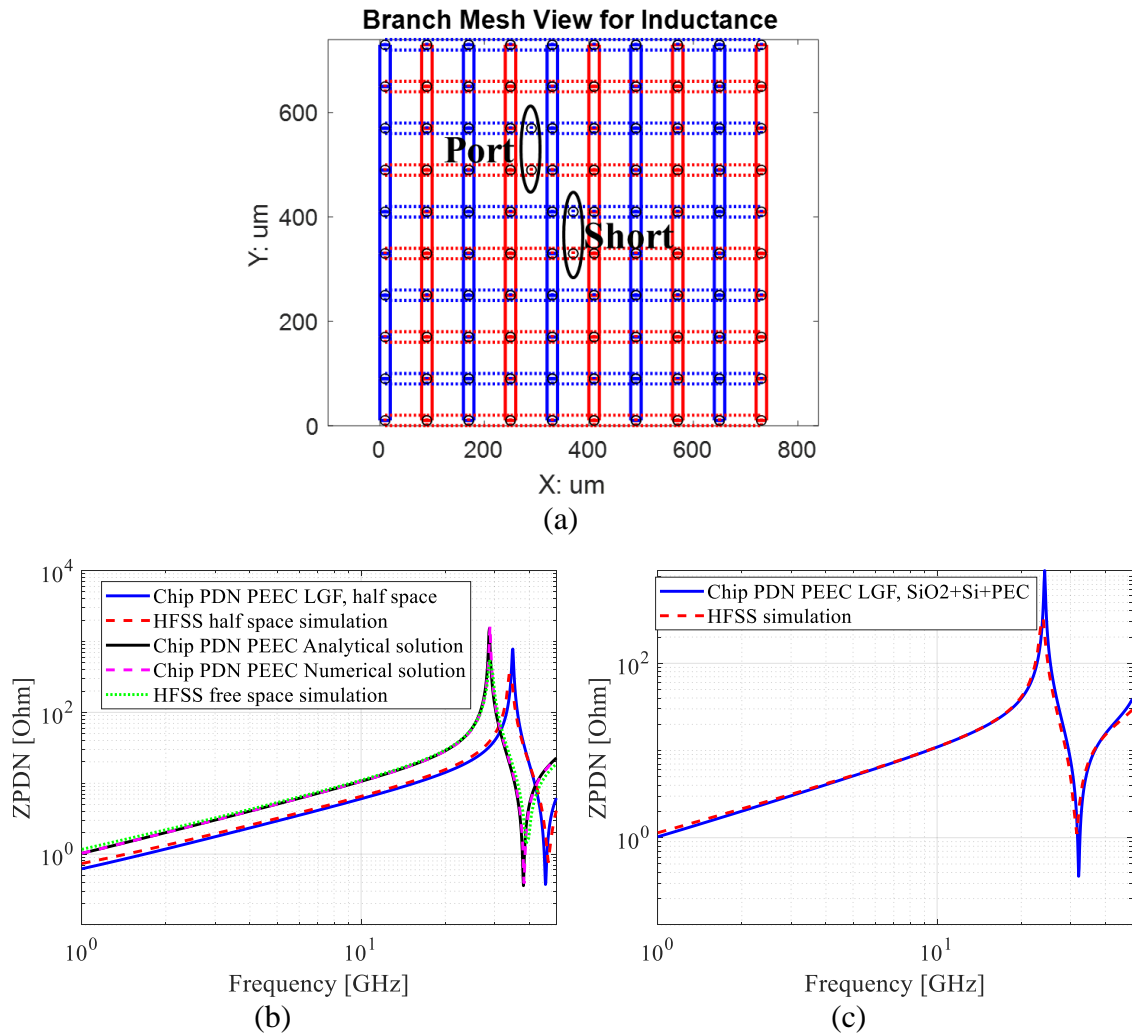


Figure 4.3. Chip PDN geometry and validation. (a) Top view of a chip PDN geometry with 10 long traces on the two layers. Port and short are added on the bottom layer as shown in the figure. (b) Input impedance looking from the port when the chip PDN is placed in free space and half space. (c). Input impedance looking from the port when the chip PDN is placed on chip, above silicon dioxide and silicon interposer.

Since the locations and coefficients of the complex images are from LGF, the accuracy of the method is ensured. Also, the treatment of obtaining the complex image

information for all Gaussian point pairs firstly avoided repeated calculations of LGF in PEEC cells. Further, by identifying the unit cells in the chip PDN, only several values need to be calculated for partial inductance and capacitance. Increasing the number of traces in the chip PDN will not increase the number of unit cells. The method is able to model large chip PDN geometries without increasing the computation cost too much.

Equivalent circuit model can be exported using PEEC to represent the system or to be used for further analysis. The value of partial capacitances and inductances can be tuned for different geometry changes to test out the effectiveness of various proposed improvements without modifying the geometry.

5. PHYSICS-BASED CIRCUIT MODELING METHODOLOGY

5.1. DIRECT CURRENT PATH

The objective of the PI modeling herein is to find an equivalent circuit to represent complex digital systems which consist of multi-core processors and multiple levels of packaging. The circuit model need to reflect the physical structures in the system, and can be used for further PDN design, discovery, and analysis.

The system of IBM z13 processor drawer is investigated herein [15][16][17]. The system includes an IC with eight cores, an organic PKG and a 44-layer PCB, as shown schematically in Figure 5.1. The IC is placed in the center of the PKG. On the top layer of the PKG, there are four 8-terminal decaps on one side of the IC, and three 8-terminal decaps on the other side. The PKG is 68.5 mm by 68.5 mm, including 7 build-up layers on the top, 7 build-up layers on the bottom and a two-layer core. The main power layer for the PKG decaps is the top core layer (Top-Layer-8). There are three power layers among the bottom 8 layers in the PKG, the bottom core layer (Bot-Layer-1), Bot-Layer-3 and Bot-Layer-7. On Bot-Layer-1, the plane is divided into power net area fill in the center, ring-shaped ground area fill around the IC region and power area fill on the edge. There is a gap between the power and ground area fills to isolate the vias in the IC region. Thus, the current from the IC region uses the power planes on Bot-Layer-3 and Bot-Layer-7 to reach the surrounding area in the PKG. The cross-section of the organic PKG is shown in Figure 5.2 (a). A top view of the PKG with chip and PKG decap locations highlighted is shown in Figure 5.2 (b) [15][16]. The PCB is roughly 590 mm by 470 mm. The layout of the electronic packaging components assembled on the z13 PCB is shown in [17] with six central processor chips and two system controller chips. Here, one of the systems with one

chip is analyzed. For the PCB PDN for a specific system, there are 153 decaps in size 0402 placed on the bottom layer under the IC, and 108 decaps in size 0805 placed around the IC with approximate 5 mm distance to the edge of the PKG on the top and bottom layers. Among the 0805 decaps, two are placed sharing one pair of power and ground vias on the top layer, and another two are placed sharing the same pair of vias on the bottom layer. Multiple power planes with different power nets are located near the top and the bottom of the stack-up on layers 3, 6, 7, 38, 39, 41 and 42 in the PCB, as shown in Figure 5.1. The power layers with the power net of interest are on Layer 3 and Layer 41.

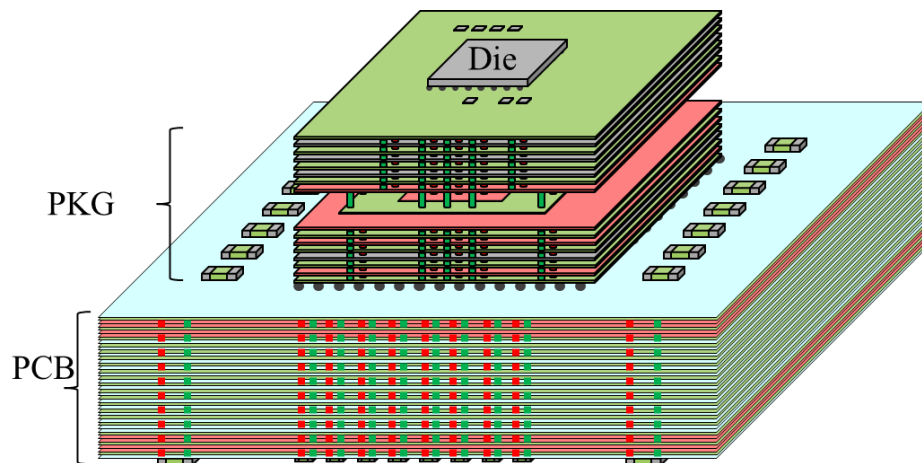


Figure 5.1. The schematically representation of IBM z13 processor drawer system with an 8-core IC, an organic PKG and a 44-layer PCB.

The overall aim of the system PDN is to keep the input impedance observed on the IC at the current draw terminals low for a frequency range from kHz to GHz range. The decoupling solutions for different levels of PDN, as on chip, PKG and PCB PDN, are different so that each level of the PDN design should be effective for a portion of the entire

frequency range. Together, the system PDN meets the requirement to achieve a low PDN input impedance across a wide frequency range.

There are two current paths within the PCB PDN. One is from the top layer of the PCB where the PKG is located, to the decoupling capacitors through the power net area fill and back to the power-return, as shown in [45]. The equivalent inductance of the total current path is denoted L_{PCB_EQ} . Another current path is from the PKG location on the PCB to the power net area fill and back to the power return through the plane capacitance without passing through the decoupling capacitors. The inductance of this path is defined as L_{PCB_IC} . In L_{PCB_EQ} , the inductance associated with the current crossing the power net area fill from IC region to the decap region is defined as L_{PCB_Plane} . The inductance of the interconnection from the decaps to the power plane through the vias is defined as L_{PCB_Decap} , and the parasitic inductance due to pad, trace, and ESL are defined as L_{above} . Herein, the L_{above} is included in the L_{PCB_Decap} during the inductance extraction since both terms are related to the decaps.

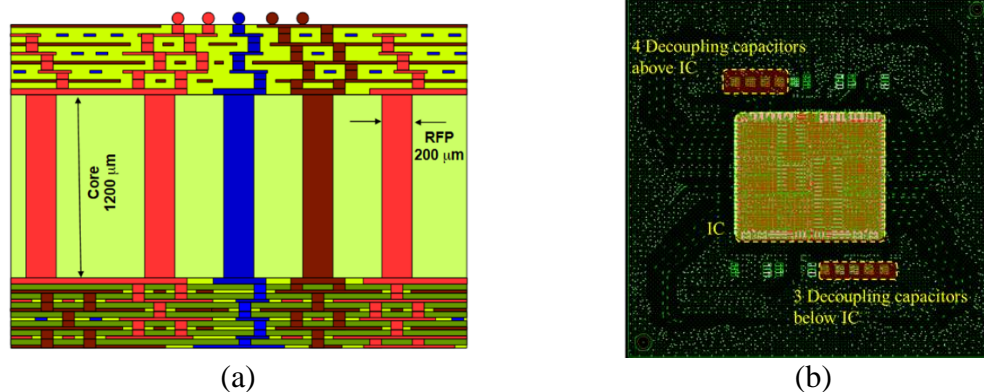


Figure 5.2. The organic PKG geometry in the system (a) Stack-up of the PKG PDN with 16 layers, (b) Top view of PKG PDN with IC placed in the center of PKG and seven 8-terminal SMT decoupling capacitors mounted on the top of the PKG around the IC [6].

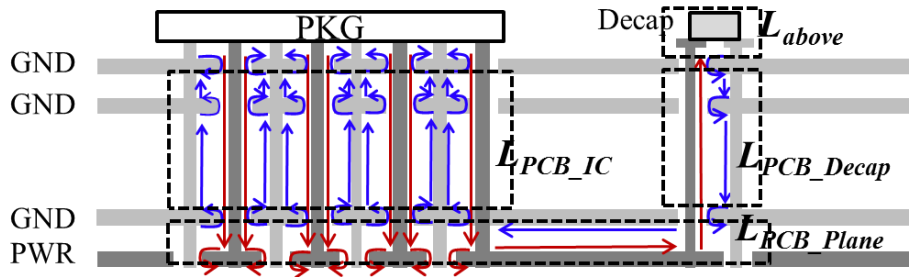


Figure 5.3. The current path in PCB from the PKG to the decoupling capacitors through the power net area fill.

There are two similar current paths in the PKG PDN. The current path from the IC core to the PKG decoupling capacitors through the power net area fill in the top layers of the PKG is shown in [46]. In the PKG PDN, the vias are not through-hole vias. The lateral connections between vias (dog-bones) in the PKG lengthen the current path. The equivalent inductance of this current path is defined as L_{PKG_EQ} . The second current path is from the IC core to the power net area fill and back to the power-return through the PKG plane capacitance. The path inductance is denoted L_{PKG_IC} . In L_{PKG_EQ} , the inductances L_{PKG_Plane} and L_{PKG_Decap} (L_{above} included) are defined similarly as those on the PCB, and are identified in Figure 5.4.

The PCB decaps have a large charge storage capacity with the largest equivalent inductance L_{PCB_EQ} , and the slowest charge delivery rate, and are effective in the low-frequency range, in the present case from 10 kHz to 500 kHz, and 2 MHz to 3.5 MHz. The PKG decaps are closer to the IC and are effective in a middle frequency range, here from 5 MHz to 10 MHz. The on-chip capacitance is used to suppress the high-frequency noise as it is closest to the current demand with minimal inductance. This difference in the capacitances and associated inductances leads to a frequency separation solution to lower the PDN input impedance over a wide frequency range, as shown in Figure 5.5.

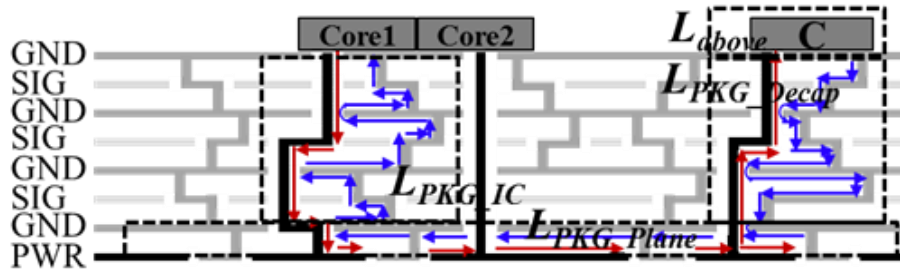


Figure 5.4. The current path in the PKG from the port to the PKG decoupling capacitors through the power net area fill in the top of the PKG.

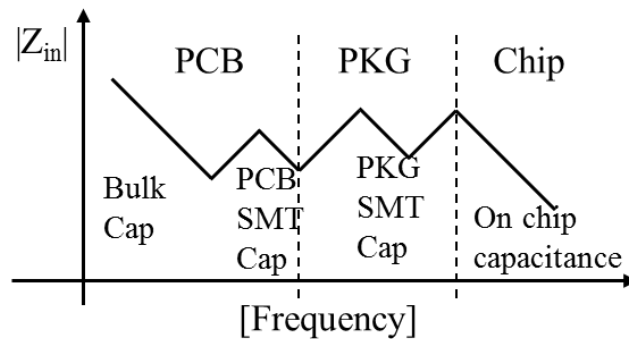


Figure 5.5. System PDN input impedance showing the frequency dependence of different levels of PDN design.

5.2. PHYSICS-BASED CIRCUIT MODELING METHODOLOGY

A physics-based circuit model is proposed herein based on the current paths and the geometric layout details. The physics-based circuit model is based on cavity model and plane-pair PEEC. The power net area fill of the PKG has lots of cut-outs and voids. Plane-pair PEEC can model this structure within 15mins with high accuracy, while it takes hours to simulate the power net area fill in SIwave. The combination of both methods enables quick calculation and maintains high accuracy. The approach can be used to compute the element values in the proposed impedance equivalent circuit model that improves upon the typical hierarchical model.

5.2.1. Cavity Model. The cavity model has a long history for solving the parts of the PDN structures which consist of multiple power and ground planes with vias [47][48]. Two thin metal layers separated by a small distance form a cavity. The distance between the two layers needs to be electric small. The cavity geometry is modeled as planar circuit based on the cavity model [49][50][51]. Due to the assumptions on the geometry, electromagnetic principles are used to build a model, which is called the cavity model, to characterize the electric and magnetic fields inside the cavity. Figure 5.6 shows the one cavity with four vias and the equivalent circuit model for this geometry with four vias being set as ports. The circuit model is based on the transfer impedance between the vias of rectangular cavity from the cavity model. The via and the plane around it in the cavity is represented as an inductor. The cavity capacitance is calculated as plane-pair capacitance. For multi-layered PCB PDN geometries, the circuit modelling rule can be extended to include the vias and cavities in the physics-based circuit model. The circuit model has one-to-one correspondence to the geometry, as shown in Figure 5.6, which can be used to link the PDN response to the geometry.

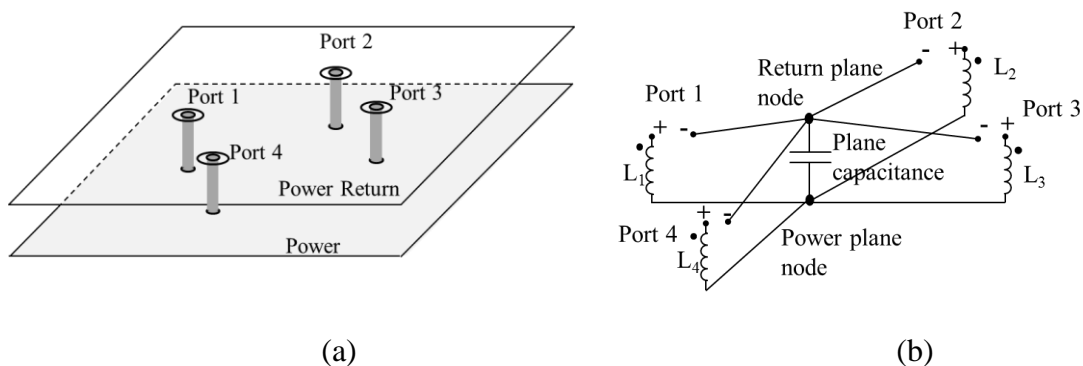


Figure 5.6. Cavity model. (a) An open plane-pair cavity with four vias; (b). The equivalent circuit mode based on the cavity model.

The formulation for component values in the equivalent circuit is explained below [16][45]. The impedance looking into a via i in a rectangular cavity when the source is placed at via j can be written as,

$$Z_{ij} = \frac{1}{j\omega C_p} + j\omega L_{ij}(\omega) \quad (42)$$

where, C_p is a parallel plate capacitance for the first cavity mode with $(m, n) = (0, 0)$ given by

$$C_p = \varepsilon \frac{ab}{d} \quad (43)$$

and the inductance is found using,

$$L_{ij} = \frac{\mu d}{ab} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \frac{(2-\delta_m)(2-\delta_n)}{k_{mn}^2 - k^2} f(x_i, y_i, x_j, y_j) \Big|_{(m,n) \neq (0,0)} \quad (44)$$

where,

$$\begin{aligned} f(x_i, y_i, x_j, y_j) = & \cos\left(\frac{m\pi x_i}{a}\right) \cos\left(\frac{m\pi y_i}{b}\right) \operatorname{sinc}\left(\frac{m\pi W_{xi}}{2a}\right) \operatorname{sinc}\left(\frac{m\pi W_{yi}}{2b}\right) \\ & \times \cos\left(\frac{m\pi x_j}{a}\right) \cos\left(\frac{m\pi y_j}{b}\right) \operatorname{sinc}\left(\frac{m\pi W_{xj}}{2a}\right) \operatorname{sinc}\left(\frac{m\pi W_{yj}}{2b}\right). \end{aligned} \quad (45)$$

Here,

$$k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2, \quad k^2 = \omega^2 \mu \varepsilon \quad (46)$$

And, a, b, and d: Dimensions of cavity along the x , y , and z directions, respectively,

(x_i, y_i) : Location of the i^{th} port,

W_{xi} , and W_{yi} : i^{th} Port dimensions along the x and y directions, respectively,

m , and n : Cavity mode indices in the x and y directions, respectively,

μ : permeability of the dielectric layer, and

ε : permittivity of the dielectric layer.

δ_m and δ_n : the Keronechker delta function.

The extracted inductance used in the model should be frequency dependence. But, it is found that the inductance value is relatively constant till 60% of the first cavity resonance frequency [45]. For low frequency approximation, it is acceptable to use a single inductance value at DC to find its contribution of the cavity impedance. The infinite summation can be truncated in practice as soon as target convergence is achieved. For the test structure used herein, the mode number $m=n=800$ is necessary to reach the target convergence within 5% [51].

For multi-layer PCB PDN geometry, the circuit can be built the same way as the single cavity for every cavity. And the equivalent circuit models for all cavities can be assembled together to form the equivalent circuit model for the entire geometry. The physics-based circuit model has one-to-one corresponding to the geometry.

5.2.2. Plane-Pair PEEC. The Plane-Pair PEEC (PPP) method is well suited for modeling the power net area fill. It is a special application of the partial element equivalent circuit (PEEC) method for the parallel planes in the PCB and PKG stack-up [52][53][54]. In the PPP method, orthogonal mesh cells are applied to subdivide the planes to form cell pairs for a single cavity. The voltage and current continuity is maintained at the nodes between cells.

It has been shown that PPP can be applied to very complicated structures such as irregular power net area fills with many voids and vias [53]. The inductance contribution of the current crossing the planes can be modeled quickly and accurately using PPP when the area fill is irregular and has thousands of voids. Compared to commercial tool simulations, the orthogonal mesh in PPP enables a fast calculation while maintaining the accuracy. In this work, the plane inductance of the PKG irregular power net area fill is quantified by using PPP.

5.2.3. Physics-Based Circuit Model for PKG and PCB. A physics-based circuit model is proposed based on the cavity model and PPP. The physics-based circuit model has a one-to-one correspondence with the geometry features. The current on every via segment in every cavity is represented as an element in the model.

There are several difficulties in applying the cavity model directly to the PKG PDN geometry [46]. There are partial planes for different power/power-return nets. The number of vias change layer by layer. Further, there are multiple partial power net area fills along the stack-up. Also, the vias in the PKG are not through-hole vias. And, finally, there are thousands of dog-bones along the stack-up. To solve the problem, a layered solution is applied to build a physics-based circuit model based on the cavity model for the PKG PDN

geometry. In the layered solution, the horizontal traces in the via-jog part along the layer is ignored.

The PKG region is divided into 20 small regions, as shown in Figure 5.7. Eight of them are in the IC region, corresponding to the 8 cores on the chip. For each cavity in the stack-up, every via segment is represented as an inductor, where the value is obtained from the cavity model (1). Then, the power vias and ground vias in the 8 core regions are merged separately and reduced as 8 pairs of power and ground vias. Then the eight pairs of power and ground vias are connected layer-by-layer following the physical connections of the cavities, as shown in Figure 5.8. The layer-by-layer topology also applies to the decap region and the surrounding 12 regions around the IC. There are 7 eight-terminal decoupling capacitors placed on the top layer of the PKG. Correspondingly, there are seven pairs of power and ground vias in each cavity along the stack up to represent all the power and ground vias for every decap, as shown in Figure 5.8. In the bottom layers, the surrounding 12 small regions are represented as 12 pairs of power and ground inductors similarly for each cavity.

There are two assumptions introduced during the via reduction process. One is that the vias of the same net are at equal potential for the small regions [16]. The other is that the layers in the small region form a cavity. The two assumptions are justified because the dimensions in each region are sufficiently small. The potential difference among each region can be neglected at the frequency range where the PKG PDN is effective. Also, even though the entire planes may not form a cavity, small regions in the planes can still be treated as a cavity structure.

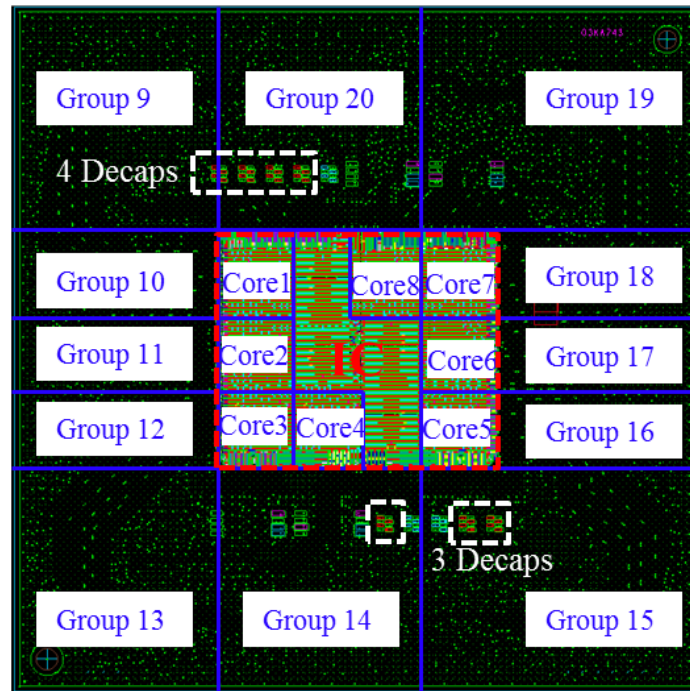


Figure 5.7. Region division setup in the PKG.

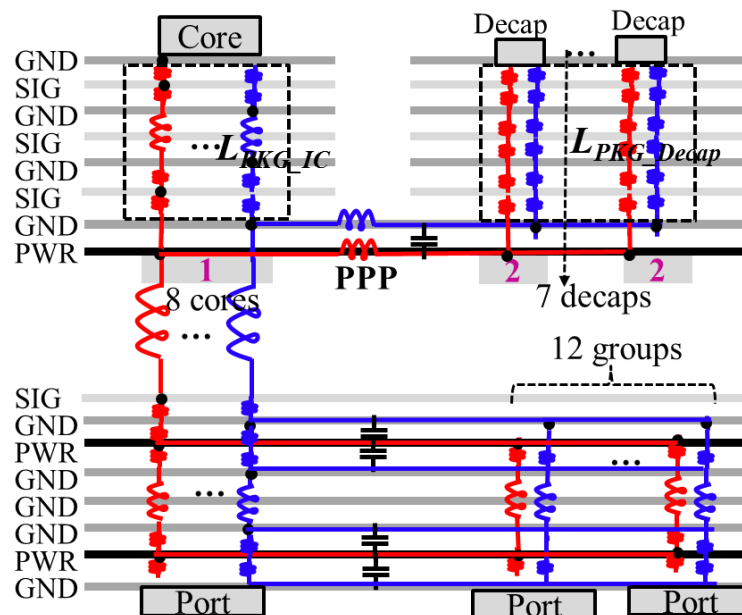


Figure 5.8. Schematic representation of the physics-based circuit model for the PKG PDN based on the cavity model and PPP.

The power net area fill in the PKG PDN is irregularly- shaped with thousands of voids primarily due to anti-pads. For the inductance associated with the current crossing the power net area fill, the current distribution the shape of the power net area fill, and the voids inside it. The resulting inductance is then higher than that of a solid rectangular power plane. This particular power cavity is modelled using PPP, and connected to the regions which are modeled using the cavity model, as shown in Figure 5.8. For the power net area fills in the bottom of the PKG, the shape is close to rectangular and there are few voids. The bottom part of the PKG is modelled using the cavity model directly. The full physics-based circuit model for the PKG is schematically represented in Figure 5.8.

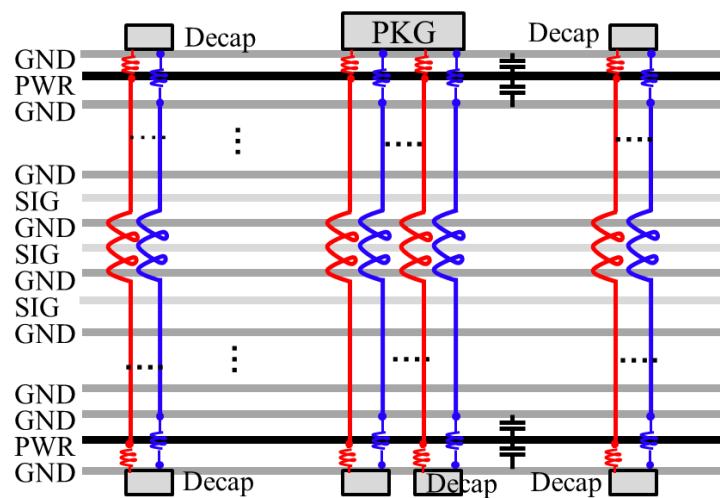


Figure 5.9. The physics-based circuit model for the PCB PDN.

The cavity model is applied directly to the PCB PDN geometry where the vias in the PCB are plated through-hole vias. Then circuit model reduction can be applied to simplify the physics-based circuit model [16]. The physics-based circuit model is shown

schematically in Figure 5.9. The method has been validated with simulations and measurements [55].

The proposed way of modeling the PKG and PCB PDN geometries maintains the one-to-one correspondence between the circuit and the geometry. Even though some of the inductors are merged and represented as a single inductor, the contribution of each via is still traceable in the modeling process. The use of PPP reduces the simulation complexity and time dramatically, while maintaining the accuracy for the power net area fill [53][[56]. The combination of the two methods provides a fast modeling methodology for PDN geometries with high accuracy.

5.2.4. System PDN Input Impedance. Commercial tool simulation is used to corroborate the results from the physics-based circuit model. The system PDN model was constructed using S-parameter cascading. The ports to connect the PCB, PKG and chip are carefully set in the commercial tool, according to the area definitions shown in Figure 5.7 following the physical connections. Eight ports in the IC region are added on the top layer of the PKG to connect the PKG to the IC. Twenty ports are added on the bottom layer of the PKG and in the PKG region on the top layer of the PCB to connect the PKG and the PCB. The system PDN input impedance from the physics-based modeling and the commercial tool is compared in Figure 5.10. and Figure 5.11.

The input impedance from the physics-based circuit model agrees favorably with that from the commercial simulation tool. The cavity model used here only includes dielectric loss, so the PDN input impedance from the commercial simulation tool has larger loss, which leads to high peaks at resonances in the physics-based model results. The resonances of the system PDN are correctly represented using the physics-based circuit

model. By comparing the PDN input impedance of different levels of the PDN from PCB, adding the PKG, and then including the chip, it is observed that the dominant part changes from PCB to PKG, and to chip PDN with increasing frequency range, as shown in Figure 5.10. It also shows that the on-chip capacitance can lower the system input impedance at higher frequencies. However, there are frequency ranges where two levels of the overall PDN design have an effect over the same frequency interval. That is, there is an overlapping interaction between frequency ranges without a clear boundary of frequency separation.

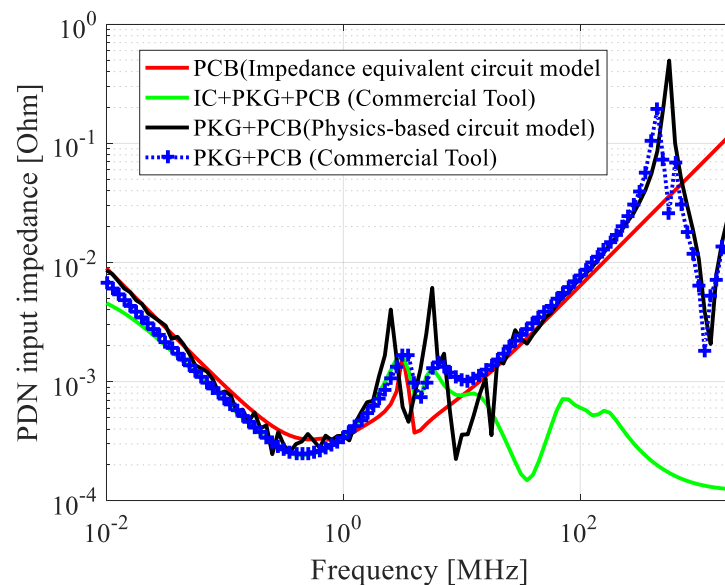


Figure 5.10. The comparison of the system PDN input impedance from the physics-based circuit model and the commercial simulation tool with PCB PDN and PKG PDN connected.

The simulation time of the physics-based circuit is significantly reduced as compared to the commercial tool. The simulation time of the circuit model depends on circuit simulation time, which only needs a few seconds to minutes. The most time-

consuming part in the setup is the L_{ij} calculation from (1) for all the via segments in the different cavities. For the PKG used, a maximum time of 1-2 hours was observed using a local desktop. The L_{ij} matrix can be saved and reused. With a decap location changed, only corresponding rows and columns of the L_{ij} matrix related to the decap vias need to be recalculated [46], which is fast. The modeling of the power net area fill using PPP also reduces the simulation time and complexity. For the power net area fill in the PKG used here, it takes 10-15 minutes to include all the voids and cut-outs in the irregular power net area fill with conductor losses, the skin effect included. However, 2.5D simulation of the entire PKG using a commercial tool takes days to finish on a server due to the complexity of the PKG PDN geometry.

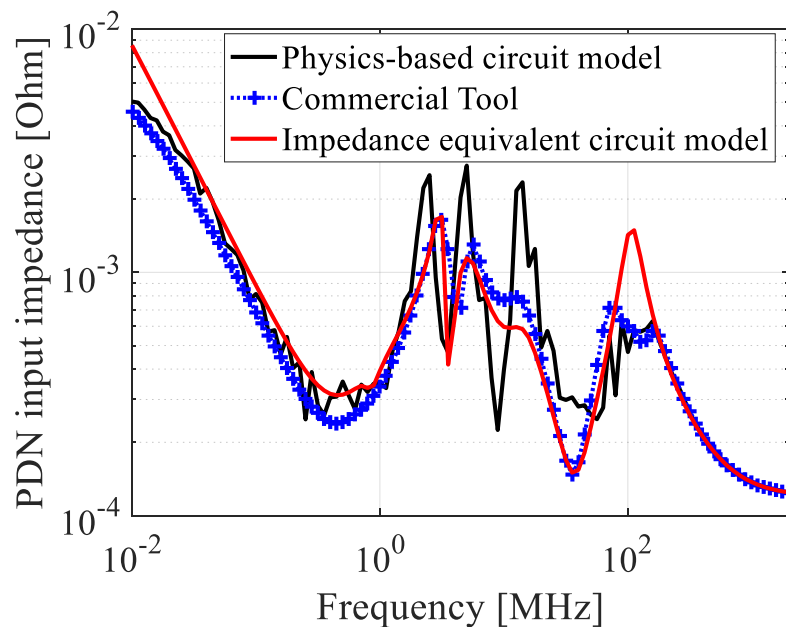


Figure 5.11. The system PDN input impedance with the complete physics-based circuit model of the PCB, PKG and chip PDN compared with the commercial simulation tool result.

5.3. SYSTEM INTERACTIONS

The number and proximity in frequency of the poles and zeros in the impedance response are indications that there are interactions in the system. Apart from the direct current paths within the same level of PDN, there are current paths in the system PDN that connect different levels of PDN as a complete system and there are interactions between the different levels of PDNs and components. The one-to-one correspondence of the physics-based circuit model can be used to identify the interactions of the related current paths to the geometry in the system.

An impedance equivalent circuit model is proposed herein to represent the system PDN input impedance by tracing all the current paths in the system. The impedance equivalent circuit model maps the inductance contributions of different blocks of the geometry to the response. The zeros and poles are also represented clearly in the circuit.

5.3.1. Interaction Between IC and PKG. The IC used in the example system has eight cores. When the IC is connected to the PKG, the eight cores are connected through the PKG power layer. At very high frequencies, each core is dependent on the nearest on-chip capacitance in the same core region. While, at lower frequencies, each core can use all on-chip capacitance through the interconnections on chip and in PKG, which leads to the interaction between PKG and IC.

The current path to explain the interaction in the PKG to connect the different IC cores is shown in Figure 5.12 (a). The current comes from the power pins of Core 1, goes through the vias under the IC in the PKG to reach the Top-Layer-8, and spreads across the power net area fill. Then, it reaches the on-chip capacitances of other cores, like Core 2, through the power via in the regions under other cores in the PKG. Then, it returns to the

power-return pins of the first core through the PKG power-return vias and plane. The current path involves both the PKG and IC, and is similar to the equivalent inductance current path with the on-chip capacitance of the other cores treated as decoupling capacitance for the first core. Due to this interaction, the total on-chip capacitance can be used from 5MHz to 35MHz in this case.

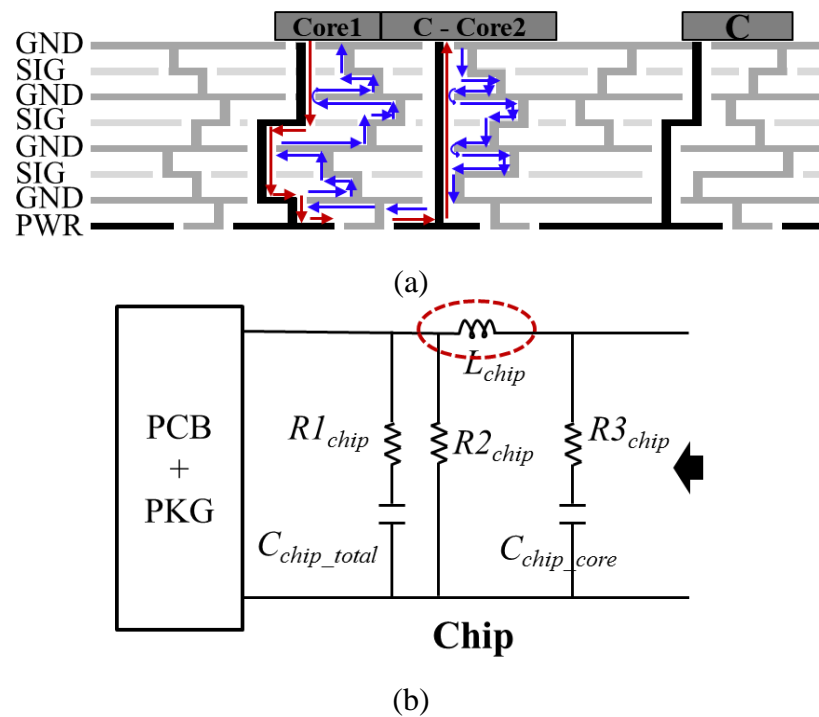


Figure 5.12. Current path and circuit model for the interaction. (a). The current path in the PKG from one core to the on-chip capacitance in another core through the PKG. (b). The chip PDN part in the impedance equivalent circuit model.

The corresponding inductance from the interaction is shown in Figure 5.12 (b). The chip model is modified to two branches to explain the interaction. The branch with C_{chip_core} is related to the high-frequency when only the on-chip capacitance inside the core is used, and the branch with C_{chip_total} is related to the lower frequencies when the total on-chip

capacitance is used through the PKG. The equivalent inductance of the current path in Figure 5.12 (a) is represented as L_{chip} in Figure 5.12 (b). The resistance $R1_{chip}$, $R2_{chip}$ and $R3_{chip}$ are from the chip modeling tools to account for the loss on chip. Here, L_{chip} is in the PKG, and is extracted using the physics-based circuit model for the PKG.

5.3.2. Interaction Between PKG and PCB. The PKG also serves as a connection between the PCB PDN and the IC. As shown in Figure 5.13 (a), the current starts at the IC and passes through the top layers of the PKG and its core vias. Then it spreads to a wider region through the power planes, Bot-Layer-3 and Bot-Layer-7, in the bottom layers of the PKG. Then it connects to the current path of either L_{PCB_EQ} or L_{PCB_IC} , depending on the frequency range. After that, it returns to the IC through the PKG. This connection contributes to the series inductance between the PCB PDN and IC, and the inductance value depends on the design of the bottom layers of the PKG.

The PKG PDN part in the impedance circuit model is shown in Figure 5.13 (b). The four PKG decaps on one side of the IC and the three decaps on the other side are represented separately using two branches. The inductance $L_{PKG_EQ_3Decap}$ and $L_{PKG_EQ_4Decap}$ are from the L_{PKG_EQ} current path as shown in Figure 5.4, which includes L_{PKG_Decap} , L_{PKG_Plane} and L_{above} . Here, L_{PKG_via} represents the series inductance contribution from the PKG being the connection between the PCB and IC. The inductance value is extracted from the physics-based circuit model using the associated current path shown in Figure 5.13 (a). $C_{PKG_Plane_Top}$ and $C_{PKG_Plane_Bot}$ represent the plane capacitance in the top power-net build-up layers and bottom power-net build-up layers in the PKG, respectively. The plane capacitance can be calculated using the parallel capacitance formula. Resistors are added to account for the loss on the PKG.

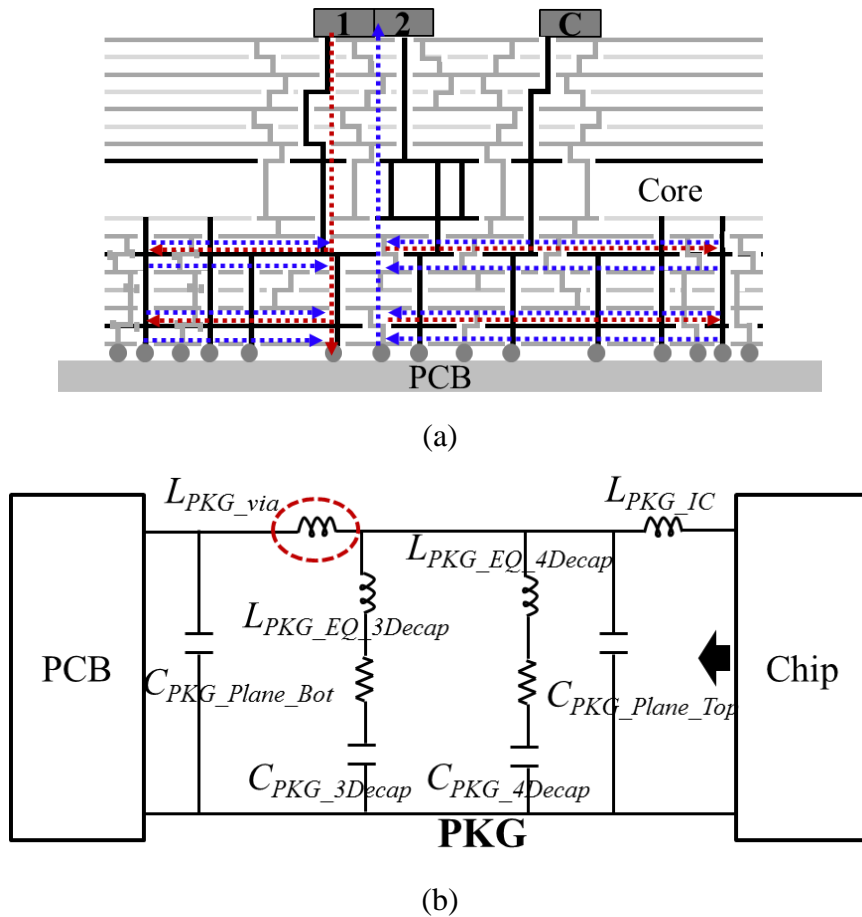


Figure 5.13. Current path and circuit model for the interaction. (a). The current path in the PKG from the IC to the PCB through the PKG. (b). The PKG PDN part in the impedance equivalent circuit model.

5.3.3. Interaction on PCB. The physics behind the segmentation of the geometry is based on the current paths in the PCB PDN. The current distribution along the planes of the geometry gives more intuitive understanding of how the geometry influences the mutual inductance between the vias in the cavity.

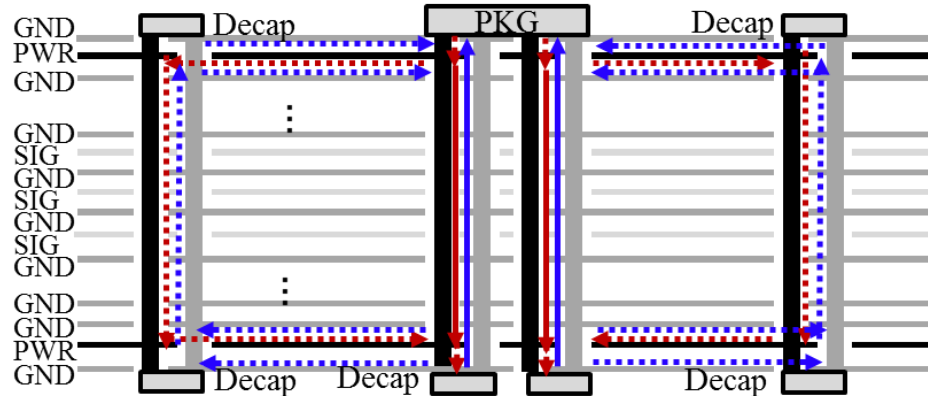
A single rectangular cavity formed by a power layer and a power-return layer with a power via and a shorting power-return via is used as the test geometry to illustrate the coupling mechanism in different situations [57], as shown in Figure 5.14. One of the via is defined as a port and the other via is shorted to both plates of the cavity. The comparison

is designed to show how the distance of the vias influence the coupling between them. The two vias are placed close (5mm) in one case, and are placed far away (25mm) in another case. The circuit model for the geometry is shown in Figure 5.14, with the values of self and mutual inductance for the different cases. The surface current density for the cases in Figure 5.14 is shown in Figure 5.14.

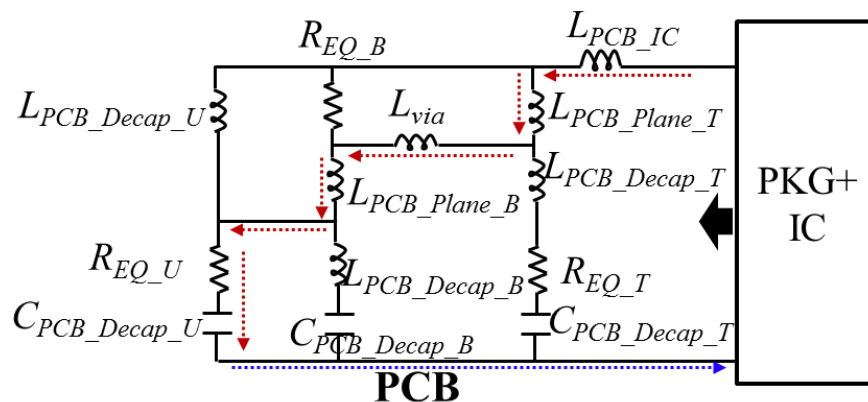
The last interaction of importance occurs between elements in the PCB PDN. A large number of decoupling capacitors can be placed on the top layer of the PCB, on the bottom layer away from the IC area, and on the bottom layer under the IC, as shown in Figure 5.14 (a). It is clear from Figure 5.14 (a) that different current paths are possible due to the multitude of possible capacitor and power plane locations. The current path for the decoupling capacitors placed on the bottom layer under the IC is usually from the IC port to the decaps through the vias in the IC region, and back to the IC port through the nearby ground vias, shown as a solid line in Figure 5.14 (a). This current path is applicable when the board is not too thick, and the power planes are in the middle of the stack-up. However, in the PCB PDN design considered here, which is used for large ICs with high current draw, two power net area fills are added at both the top and bottom parts of the PCB in the stack-up. The board is very thick with over 6.2 mm total thickness such that the inductance associated with the vias in the IC region is large. Additionally, many decoupling capacitors are added on both the top layer and the bottom layer around the IC. As a result, an extra parallel resonance is observed around 3MHz from the multiple decaps and power plane locations.

Sensitivity analyses were performed on the elements in the physics-based circuit model to identify the related current path and components which introduce the extra

parallel resonance in the input impedance. It can be identified to be the interactions between the capacitors at the three different locations through the two power planes in the stack-up, and the related current path is shown in dashed lines in Figure 5.14 (a). The current comes from the PKG, reaches the decaps on the top layer through the power plane at the top of the PCB, goes through the vias in the decap region to the decaps on the bottom layer away from the IC, and reaches the decaps under the IC through the power plane in the bottom of the PCB, then it returns through the power planes and vias correspondingly.



(a)



(b)

Figure 5.14. Current path and circuit model for the interaction. (a). The current path of the interactions between the decoupling capacitors at different locations in the PCB. (b). The PCB PDN part in the impedance equivalent circuit model.

The interaction between the decaps at different locations is not introduced by a large parallel capacitance element, but it behaves like so and introduces an additional parallel resonance. In [15], a large parallel capacitance was used to represent the impact in the lumped circuit model, though it does not correctly reflect the actual current path physics as shown herein.

The PCB PDN part in the impedance equivalent circuit model is shown in Figure 5.14 (b). The decaps on the top of the PCB, on the bottom layer of the PCB away from the IC, and on the bottom layer under the IC are represented as three separate branches. Resistors are added to account for the loss on the PCB. $L_{PCB_Decap_T}$, $L_{PCB_Decap_B}$ and $L_{PCB_Decap_U}$ represent the L_{PCB_Decap} value (including L_{above}) for the decaps on the top (T), on the bottom away (B), and under the IC (U). $L_{PCB_Plane_T}$, $L_{PCB_Plane_B}$ and $L_{PCB_Decap_U}$ represent the L_{PCB_Plane} value for the decaps at the three locations. The interaction between the decaps from the extra current path shown in Figure 5.14 (a) is marked in the circuit model in Figure 5.14 (b). L_{via} represents the inductance contribution from the top decaps to the bottom decaps through the vias.

5.3.4. Impedance Equivalent Circuit Model. The complete impedance equivalent circuit model for the system is shown in Figure 5.15. The topology of the impedance circuit model reflects all the current paths including the direct ones described in Section III and the interactions shown in Section IV.

The element values are extracted using the components in the physics-based circuit model according to the corresponding current path. Each inductor is the result of many parallel current paths of a large number of vias and interconnections. The elements in the circuit have physical meaning which can be related to geometry details. The comparison

of the impedance equivalent circuit model to a commercial tool simulation is shown in Figure 5.15. The comparison is favorable except a subtle resonance at 126 MHz is missed.

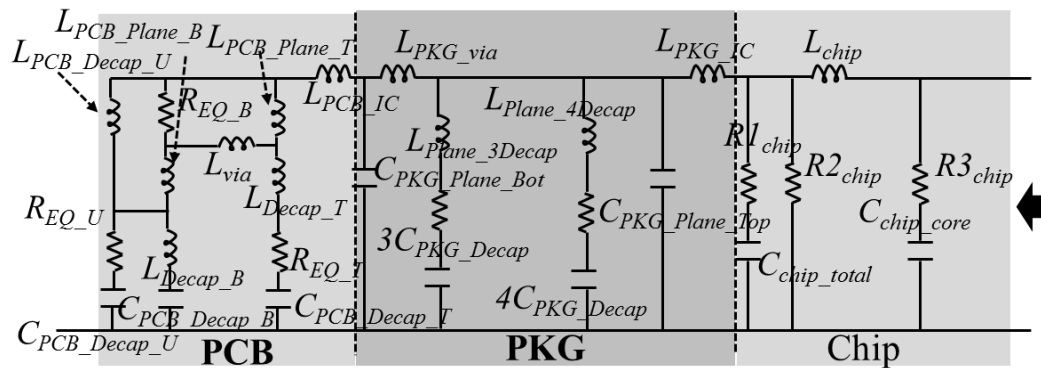


Figure 5.15. Impedance equivalent circuit model for the system shown in Figure 5.1.

The impedance equivalent circuit model has a wide range of applications. The circuit topology is simple, therefore the resonances in the PDN input impedance can be easily mapped to the related circuit elements, as shown in [15]. With the resonance information, the PDN design can be adjusted to avoid peaks in the current spectrum from the chip. A unique feature of the impedance equivalent circuit model here is that it maintains the geometrical correspondence. Thus, it can be used to explore possible design changes without changing the layout. Also, other types of simulations can be applied to the circuit and the circuit model itself can be combined with other components in the system to quantify the PDN impact on signal integrity, or EMC.

5.4. APPLICATIONS OF THE CIRCUIT MODELS

The one-to-one correspondence of the geometry to the physics-based circuit model and geometrical correspondence in the impedance equivalent circuit model can be used to

explore design options quickly with good accuracy. Any change in the physics-based circuit model can be mapped to the geometry change in the layouts without real layout changes, which is a key advantage of the physics-based equivalent circuit model. The impedance equivalent circuit model can also be used to map the geometry and resonances to the related components for PDN analysis.

The available on-chip area that can be used for on-chip decoupling capacitance is reduced with the increasing speed and complexity of the chips. Also, on-chip decoupling technology is changing with decreasing technology feature sizes. For example, the large value of on-chip capacitance achieved with deep trench capacitance is not available for technologies of 10 nm and smaller. Furthermore, the current draw on chip is increasing due to switching current increasing caused by function and power management as well as circuit density. Overcoming the impact of the reduction of on-chip decoupling capacitance on the PDN impedance is challenging.

The circuit models developed can be used to investigate design possibilities to compensate for the loss of on-chip capacitance. A few design changes have been investigated using the impedance equivalent circuit model and physics-based circuit model. The changes in the input impedance with decreasing on-chip capacitance and increasing PKG capacitance is shown in Figure 5.16. In the original design, the on-chip capacitance of each core is 2.5 μF and there are seven 2.2 μF decoupling capacitors on the PKG PDN. Reducing the on-chip capacitance increases the PDN input impedance substantially above 6 MHz. Increasing the PKG capacitance changes the input impedance from approximately 1 MHz to 16 MHz, but it cannot compensate for the impedance increasing in high frequencies.

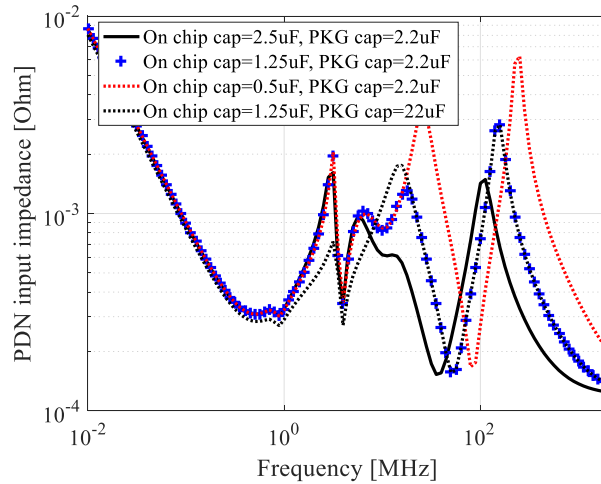


Figure 5.16. The PDN input impedance increases at high frequencies when the on-chip capacitance is reduced. The results are from the impedance equivalent circuit model.

Another option is to increase the effectiveness of the PKG decaps by moving the PKG decaps closer to the IC to reduce the series inductance of the current path from IC to the decaps. Decoupling capacitance can be added in the core region [59][60][61]. Two locations, Location 1 and Location 2, as shown in Figure 5.8, in the package core were investigated. Eight $1\ \mu\text{F}$ decaps are added at Location 1 under the IC, or seven $1\ \mu\text{F}$ decaps are added at Location 2 under the PKG decaps. The input impedance obtained from the physics-based circuit model is shown in Figure 5.17 (a). From Figure 5.17 (a), the comparison indicates adding decaps in the core region is not effective to reduce the input impedance at high frequencies to compensate for the on-chip capacitance reduction.

Another way to reduce $L_{\text{PKG_EQ}}$ is to move the power net area fill on Top-Layer-8 to Top-Layer-2. A large reduction of the input impedance is achieved in the higher frequency range, as shown in Figure 5.17 (b). Moving the power net area fill to the very top of the PKG can be a potential solution. Since the physics-based circuit model only includes dielectric loss, the peaks at the resonances are not well quantified. The input

impedance from the impedance equivalent circuit model provides better estimation with more accurate loss quantification.

When the power net area fill is moved to Top-Layer-2, the input impedance is lower than the original design, even with only half of the on-chip capacitance. By analyzing the inductance contribution of the blocks in the equivalent inductance path L_{PKG_EQ} , the mechanism related to the large impedance reduction at high frequencies is explained. From [46], the dominant part in L_{PKG_EQ} is the L_{PKG_Plane} . Moving the power net area fill to the top reduces the L_{PKG_IC} and L_{PKG_Decap} , but the L_{PKG_Plane} remains the same. The effectiveness of PKG decaps is not improved much by moving the power net area fill to Top-Layer-2. However, as L_{PKG_IC} becomes much lower, the frequency range in which one core can see the total on-chip capacitance is pushed to higher frequencies. And it leads to the compensation for the on-chip capacitance reduction in each core. Thus, to account for routing needs, instead of moving the power net area fill to the second layer, a small area of power net area fill can be added under the IC on the second layer to achieve the same improvement.

The layout of the PKG does not need to be updated or re-simulated for all the design options shown here. Only certain elements or the connections in the physics-based circuit model or in the impedance equivalent circuit model need to be changed to re-compute the corresponding PDN input impedance, with several seconds to minutes of circuit simulation time. The simulation setup and simulation time is significantly reduced as compared to the use of commercial tools. In this way, existing designs can be improved and updated quickly and accurately during the design process.

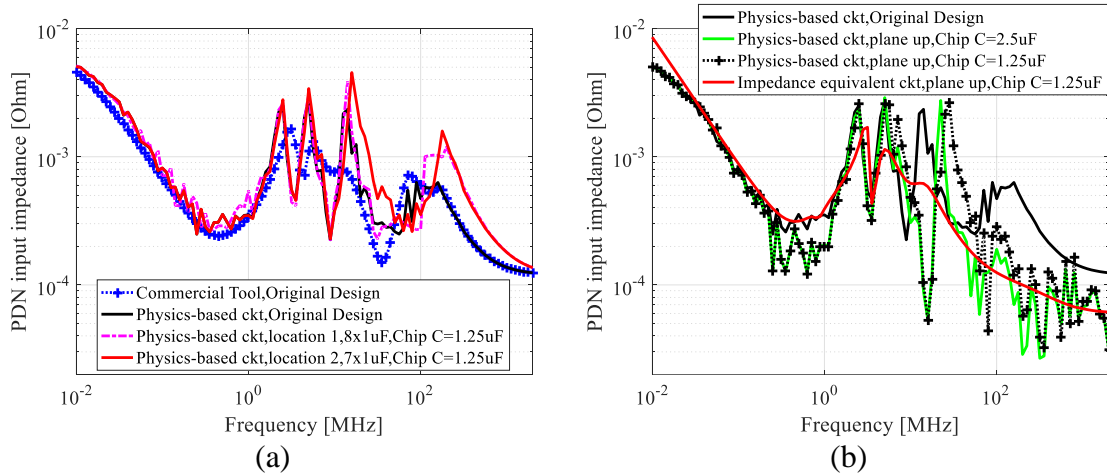


Figure 5.17. The system PDN input impedance from the physics-based circuit model (a) adding the decoupling capacitance in the PKG core under the IC and under the decoupling capacitors, and, (b) by moving the power area fill to the top of the PKG.

5.5. VOLTAGE RIPPLE

The ultimate objective in the PDN system design is to reduce the voltage ripple that can be transmitted over the PDN system. The physics-based circuit and impedance equivalent circuit models both can be directly used for time-domain simulation to obtain the voltage ripple with a specific current profile. Because the number of elements in the physics-based circuit model is relatively large, the impedance equivalent circuit model is used here for the time-domain evaluation. The functional variation in the voltage ripple with time can be readily related to elements in the impedance equivalent circuit model, and then to aspects in the geometry layout.

Many different current profiles can occur in a complex system due to different device operating states. To obtain the voltage ripple of the system, a current source is placed on the chip side of the impedance equivalent circuit model. An ideal VRM output voltage of 0.9 V is added on the PCB side of the circuit. The measurement and the simulation results of the voltage ripple when the clock stops on the chip are shown in Figure

5.18 and Figure 5.19. The current drops to 103.5 A from 133.75 A within 2-3ns, as shown in Figure 5.19. The voltage ripple measurement shows 22 mV and 24 mV for Core 0 and Core 5, respectively. The simulated voltage ripple for one core is 19 mV. Given the complexity of the full system and the measurement setup to probe the voltage on chip, the 20% agreement between modeling and measurements is acceptable for recommending design improvements and quantifying the sensitivity of a proposed optimization. Potential sources of discrepancy include inadequate representation of the geometry in the model, the assumption of uniform current distribution among the eight cores, and the probe effects in the measurements which may not have been well de-embedded due to lack of rigorous calibration standards.



Figure 5.18. Measurement results of the voltage ripple of a clock stop for two cores of the 8 core chip.

Another current waveform where the current ramps up and down by steps with a high-frequency component riding on the low-frequency component is used for the voltage ripple simulation to evaluate the system performance, as shown in Figure 5.20 (a). A high frequency 5GHz switching noise is superimposed on a low frequency component (4MHz)

to form the switching current profile. The voltage ripple due to this current profile is shown in Figure 5.20 (b). The peak-to-peak value is 26mV, which is within the 10% tolerance of the voltage ripple on the 0.9V DC source.

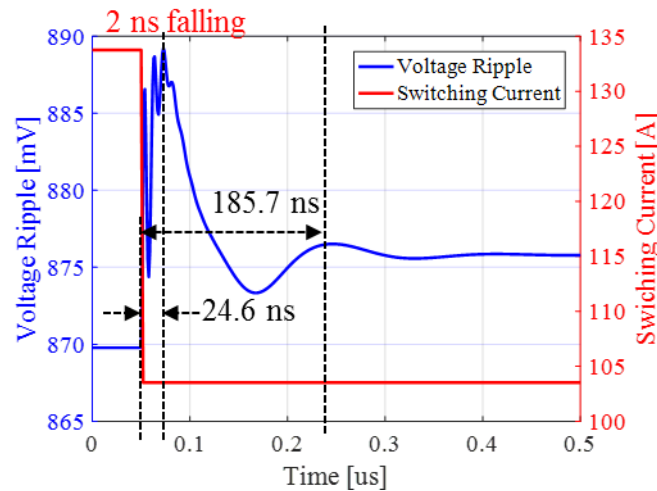


Figure 5.19. Voltage ripple simulation from the impedance equivalent circuit model and the switching current provided when the clock stops.

The voltage ripple with the power net area fill in the PKG moved to Top-Layer-2 is also included in Figure 5.20 with the on-chip capacitance reduced to 1.25 μF from 2.5 μF for each core. In Figure 5.20 (b), the reduction in the peak to peak voltage ripple is 5.4 mV, which is 20.7% reduction with only half of the on-chip capacitance. The voltage ripple from the applied high frequency 5 GHz triangular switching current with amplitude from -3 A to 3 A is shown in Figure 5.20 (c). The high-frequency voltage ripple is nominally reduced though only half of the on-chip capacitance is used.

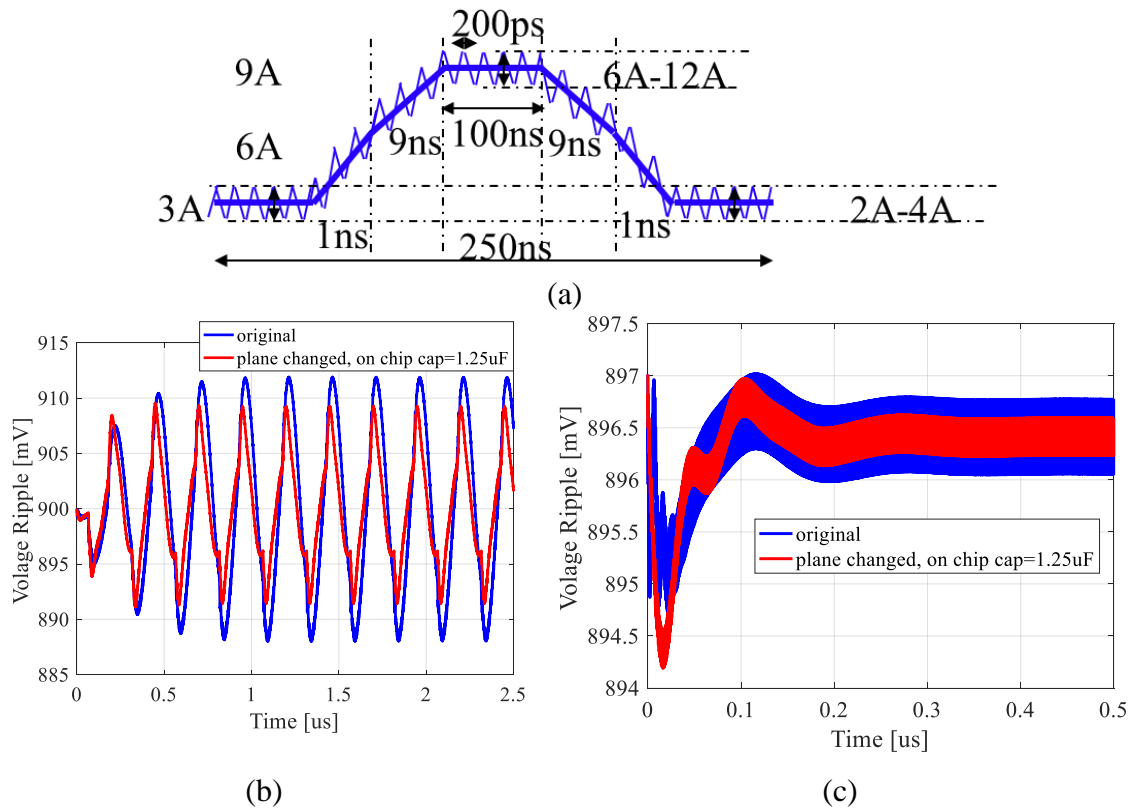


Figure 5.20. Voltage ripple simulation from the impedance equivalent circuit model. (a) The current source for the voltage ripple simulation includes a high-frequency ripple on an underlying lower-frequency waveform. (b). The total voltage ripple seen on chip with the switching current in (a). (c). The high frequency voltage ripple with 5 GHz triangular switching current with amplitude from -3 A to 3 A.

6. DISCUSSIONS AND CONCLUSION

A physics-based approach for PDN modeling was presented herein. The methodology has been demonstrated by using a complex commercial system. The PDN input impedance and the voltage ripple show a good match with the commercial tool simulation and measurements. Two circuit models have been obtained for PI analysis and design.

The methodology is based on identifying the current paths to fully understand the functionalities of the PDN system. The most important aspect of the approach is the one-to-one correspondence of the model elements to the geometry. This leads to a direct understanding of how the layout details affect the PDN response. Since the physics-based circuit model maintains the one-to-one corresponded to the geometry, any design changes can be quickly implemented by changing the elements in the circuit model. Also, the needed values for inductance and capacitance to meet specific requirements can be traced back to design a targeted change in the geometry. This feature enables engineers to improve designs in a more direct fashion.

The impedance equivalent circuit model is extracted from the physics-based circuit model and is dominated by the inductive behavior of the current paths. The impedance equivalent circuit model still maintains the physical correspondence to the geometry and can be used for quick design assessment. The components in the impedance equivalent circuit model can be related to the zeros and poles of the PDN input impedance. The circuit can also be used in other simulations, such as time domain simulation or signal integrity simulation, to represent the system PDN due to the simplicity of the model. The physical

connection carried by the circuit model can be useful to analyze the impact of the PDN on other system performance.

A physics-based circuit modeling methodology for 3D IC/package is proposed in this paper. The method is based on PPEC and LGF. The vertical complexity of the 3D IC/package systems is handled by LGF and the horizontal complexity is handled by PEEC.

The LGFs are calculated from DCIM with three terms, direct coupling, complex images, and surface wave, extracted to analyze the wave behavior. For stack-ups in 3D IC/package systems, G_A^{xx} is dominated by the direct coupling. And G_φ is dominated by direct coupling and complex images. Analytical formulas to include the contribution of complex images are proposed for partial capacitance calculation, with the complex image details from LGFs.

A chip PDN geometry is used to illustrate how to use PEEC to include geometric details in the horizontal direction and to validate the proposed method. A good match is observed between the input impedance from the proposed method and full wave simulation.

The loss calculation in the proposed method only includes the conductive loss of the traces. Loss from silicon interposer and dielectric loss are not included at this stage. The imaginary part of the LGFs can be used to include the silicon interposer loss and dielectric loss [22]. More work is needed to accurately quantify the loss. The method can also be extended to include TSV in 3D IC/packages. G_A^{zz} , G_A^{zx} and G_A^{zy} can be used similarly in PEEC to model TSV.

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