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SerDes channel crosstalk mitigation methodology with industrial implementation guidance

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SERDES CHANNEL CROSSTALK MITIGATION METHODOLOGY WITH INDUSTRIAL IMPLEMENTATION GUIDANCE

by

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ABSTRACT

With the increasing data rate of digital circuits, the differential crosstalk degrades the signal integrity performance in PCBs drastically. Usually, in the trace area, crosstalk can be isolated by stitching vias and adding shielding ground vias can also shield coupling in the ball gate array (BGA) and pin field area. The traditional way to mitigation crosstalk in the BGA and pin field area through adding more ground vias between signal pairs or increasing the spacing in between, it demonstrated us the efficiency on crosstalk cancellation efficiency but it also increases the size of products and it would be contradictory to the trend of the industry and market. The design of new channels with far less crosstalk but maintained or increased space efficiency is necessary.

The proposed pin patterns in this research mitigate the differential crosstalk dramatically, yet maintained or even increased the signal vias to ground vias ratio (S:G).（S:G is the ratio of signal vias to ground pins in a specific area of PCBs, it can represent the space efficiency). Crosstalk cancellated by using the principle of symmetry on two adjacent differential signal pairs in the BGA and pin field region. Except for the pin patterns, corresponding trace routing for the advance patterns also been researched and designed to maintain the crosstalk cancellation benefits in the pin field area. After all, interconnections between the chip package and the newly designed PCB have been studied and verified regarding industry capability and reliability.

This research proposed for the SerDes channel and the validating is under the SerDes operating circumstance.

ACKNOWLEDGMENTS

For all the time I spent on my master's program at Missouri S&T, first of all, I would like to express my heartfelt gratefulness to my advisor, Dr. Fan Jun. Thanks for all the instruction and support from him, I can only improve with his many valuable advice and patient guidance on me. Dr. Fan not only guided on my study and research but also influenced me in my life and my personality, always stay modesty and accommodating. I would like to thanks Dr. James. L. Drewniak's help and support on me, on my academic study and all different other things but important for me, without his help it would be harder for me to succeed. I am also grateful and thanks to Dr. Darly Beetner and Dr. Chulsoon Hwang's help in my research and many activities.

Thanks for my mentor, Bichen Chen, for all your leading in the project and detailed instruction and thanks to all our EMC members, we shared a wonderful time here I believe.

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1. INTRODUCTION

With the rapid increase of data rate in modern electronic devices and systems, signal integrity (SI) and electromagnetic compatibility (EMC) issues are also becoming more problematic [1] – [6]. In the SI problem, the increase in data rate can cause more severe crosstalk between high-speed channels, which can significantly degrade signal quality.

SerDes (Serial/Deserializer) is a type of high-speed data transportation solution. It conveys data between serial and parallel formats in each direction. SerDes has the advantage of minimize the number of I/O in each direction and can fully utilize the bandwidth of the SerDes channel.

However, increasing of date rate induces higher and higher crosstalk levels in the SerDes channel and it will degrade the signal integrity dramatically when the budget for the signal integrity became tighter and tighter, nevertheless, it will also affect the accuracy of signal postprocessing [7]-[13]. Separation or adding more ground vias between signal pairs can reduce crosstalk but the drawbacks are also apparent, it will sacrifice the more space and the manufacturing limitation can’t allow putting many ground vias in between [14]-[16].

In this research, new pin patterns developed to mitigate the crosstalk between differential vias while maintained or even increased the S:G ratio. The new pin patterns developed based on the symmetry principle. Except for the pin pattern design, the corresponding trace routing for the proposed advanced pin patterns also being research to maintain the crosstalk benefits in the pin field area. In the end, the industrial

implementation of the advanced layouts is studied regarding the expense, reliability and manufacturing capability. The specific realization scheme is presented.

Integrated crosstalk noise (ICN) has been introduced in the IEEE 802.3ba standard to evaluate the crosstalk in the high-speed PCBs as a replacement of the insertion crosstalk ratio (ICR) [17]. ICN is the weighted summation of crosstalk noise in the frequency domain concerning the power spectrum of the signal being transferred, it can integrate crosstalk from multiple pairs in the network. Herein, ICN is the assessment criteria for crosstalk evaluation, higher ICN indicates higher crosstalk at a specific data rate. The TDR, insertion loss and return loss will be confirmed to make sure the experimental group and control group are at a similar level to exclude the influence of other variables on the result.

2. REVIEW OF PRINTED CIRCUIT BOARD (PCB)

PCB is a kind of a board that provides electrical connection and mechanical support for chips and devices being mounted on, it can also help with heat dissipation. Figure 2.1 showed below is a typical PCB board with components mounted, various chips and components are mounted and being connected through vias, traces, and pads. Solder is the metal used to connect the PCB surface landing pad to the chip package, providing electrical connection and mechanical support. There are several signal nets and power nets inside the PCB for signal transportation and power delivery.

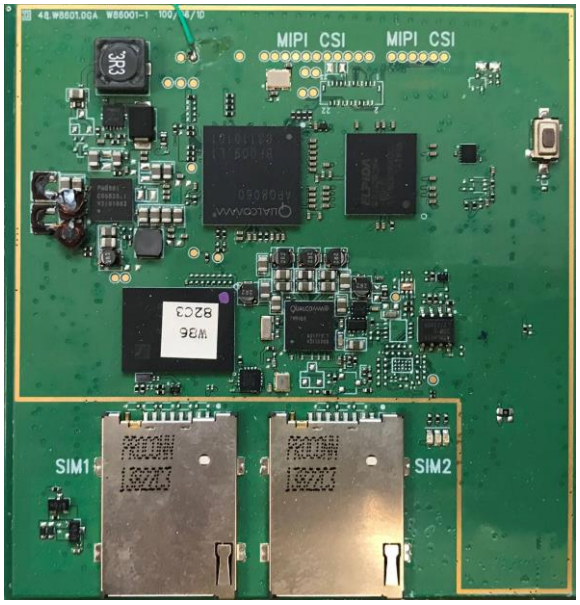


Figure 2.1. Typical PCB with chips and components mounted.

Figure 2.2 showed the main components of the PCB and there are the substrate, copper, solder mask, and silkscreen.

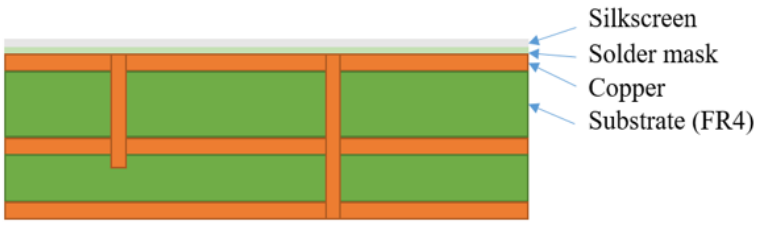


Figure 2.2. Main components of PCB.

The substrate is one of the base structures of PCB, it provides the frame of PCB and decides PCB thickness. It usually a fiberglass material and FR4 is the most commonly used material. Depends on the demands of PCB, according to the different environments it works and the requirement on signal and power its delivery, this material, and geometry can be changed.

Between substrates, there are several thin coppers foils laminated. These copper foil including signal, power nets and ground plans, providing horizontal electrical connections between components being mounted on PCBs. The thickness of copper foils represented by an ounce per square foot. 1-ounce copper is the most common foil thickness but when PCB needs to meet the more strict power requirement, the thickness can be increased to 2 to 3 ounce for the power plane. The layer number of copper foils decides the layer number of PCBs.

There are vias and pads also, vias provide vertical electrical interconnection and pads provide interconnection between PCBs and chip packages, through solder balls.

Soldermask is a thin layer at the top of PCB, it gives PCB different colors (mainly green or red). The main function of the solder mask is to prevent the solder flows from

one pad to another pad, preventing electrical short and mechanical issues. Figure 2.3 showed the PCB with a green solder mask.

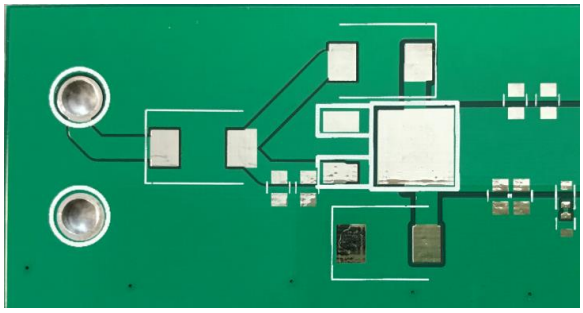


Figure 2.3. PCB with a green solder mask.

Silkscreen serves as the indicator of PCB. It is printed at the top of the solder mask. Any letters, numbers or pictures can be printed to help people know where is the chip exactly at and had a better understanding of PCB. The silkscreen is usually on write but it depends, other colors can be used also. Figure 2.4 shown a typical PCB with silkscreen printed.

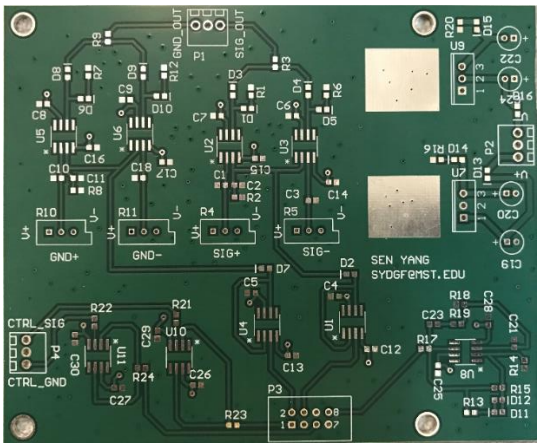


Figure 2.4. PCB with silkscreen printed.

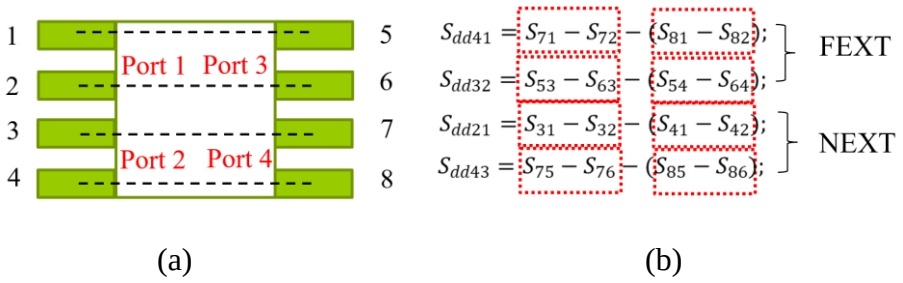
There are several other components inside PCB, like the annular ring, finger, panel and so on. These structures integrated PCB and make it provides efficient, convenient and reliable interconnections between components and chips being mounted on.

There are several signal and power nets inside PCB as mentioned previously, between each net, a signal in one net can be coupled to another net through mutual inductance and capacitance. In terms of signal integrity, a higher data rate causes higher crosstalk and high-level crosstalk in PCB hurts the time margin as well as the bit error rate (BER) however the budget for them goes tighter, optimization of crosstalk on networks is necessary to guarantee the efficiency and quality of high-speed communication.

3. THE METHODOLOGY OF DIFFERENTIAL CROSSTALK MITIGATION IN THE PIN FIELD AREA

The basic idea of crosstalk cancellation in the pin field area in this research is the symmetry principle. When two differential pairs put orthogonally to each other, theoretically, crosstalk between them would be zero since the coupling from P/N in one pair to individual P/N in another pair would canceling each other.

Figure 3.1 illustrated the single-ended port to differential port s parameters transformation. (a) showed the configuration of the single-ended ports to differential ports, (b) showed the single-ended ports to differential ports s parameter transfer functions.



(a) (b)

Figure 3.1. Single-ended to differential S parameters transformation.

Vias in red in Figure 3.2 are signal vias and blue vias are ground vias. Two differential pairs put orthogonal to each other, port configuration as it showed in the plot. When l1 equals to l2, coupling induced from via 1 to 3 would have the same amplitude but reversed-phase as coupling induced from 2 to 3, it is the same for the coupling from via 1 and 2 to via 4, based on this, the relation of the formula in the graph can be

established. Theoretically, the far-end and near-end crosstalk of this via pattern design are zero.

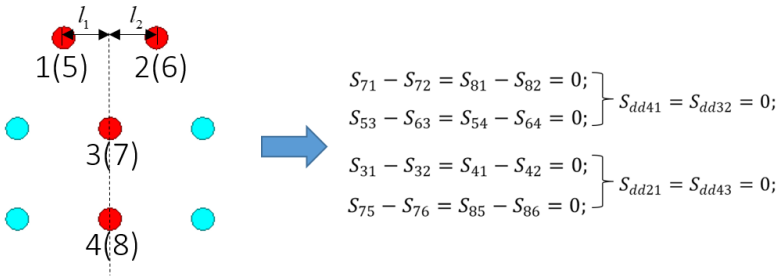


Figure 3.2. New via pattern design.

4. NOVEL PIN MAP PATTERNS DEVELOPMENT

4.1. REVIEW OF INTEGRATED CROSSTALK NOISE (ICN)

During this research, ICN is the crosstalk evaluation criteria. Herein, a brief review of ICN introduced.

As mentioned before, ICN has been introduced in the IEEE 802.3ba standard to evaluate the crosstalk in the high-speed PCBs as a replacement of the insertion crosstalk ratio (ICR). ICN is the weighted summation of crosstalk noise in the frequency domain concerning the power spectrum of the signal being transferred, it can integrate crosstalk from multiple pairs in the network.

The equation calculating ICN showed in Figure 4.1. ICN including far-end, near-end, and total ICN. There are 2 parts in ICN equations, one is the weighting function and another is multi-disturbers crosstalk function.

Weighting function Multi-disturbers crosstalk loss function

$$Near\ end:\ \sigma_{nx} = \left(2\Delta f \sum_{n} W_{nt}(f_n) 10^{-MDNEXT_{loss}(f_n)/10}\right)^{\frac{1}{2}}$$

$$Far\ end:\ \sigma_{fx} = \left(2\Delta f \sum_{n} W_{ft}(f_n) 10^{-MDFEXT_{loss}(f_n)/10}\right)^{\frac{1}{2}}$$

$$Total:\ \sigma_x = \sqrt{\sigma_{nx}^2 + \sigma_{fx}^2}$$

Figure 4.1. ICN equations.

Figure 4.2 showed the weighting function for both near-end and far-end ICN. It consists of three parts: power spectrum, transmitter filter, and receiver filter. For NRZ (no

return to zero) signals, where Ant and Aft are the near-end and far-end pulse amplitude of the signal, fb is the date rate, fr is the cut-off frequency for the receiving filter.

$$\textit{Near end:}\quad W_{nt}(f) = (A_{nt} / f_b)\sin c^2(f / f_b)\left[\frac{1}{1+(f / f_{nt})^2}\right]\left[\frac{1}{1+(f / f_r)^2}\right]$$

$$\textit{Far end:}\quad W_{ft}(f) = (A_{ft} / f_b)\sin c^2(f / f_b)\left[\frac{1}{1+(f / f_{ft})^2}\right]\left[\frac{1}{1+(f / f_r)^2}\right]$$

Power spectrum Transmitter filter Receiver filter

Figure 4.2. Weighting functions.

Figure 4.3 illustrates the multi-disturber crosstalk loss functions, Sv,ni and Sv, nj represent multi-disturber S parameters from near-end and far-end, v represents the victim port, n represents the aggressor port.

$$\textit{Near end:}\quad MDNEXT_{loss}(f) = -10\log_{10}(\sum_{1}^{i} | S_{v,ni} |^2)$$

$$\textit{Far end:}\quad MDFEXT_{loss}(f) = -10\log_{10}(\sum_{1}^{j} | S_{v,nj} |^2)$$

Figure 4.3. Multi-disturbers crosstalk loss function.

Figure 4.4 depicted the calculation flow of ICN at one frequency point. At a specific frequency point, s parameters decide multi-disturbers crosstalk, signal type decide power spectrum modulation and weighting function can be confirmed. After the integration of crosstalk noise at different frequency points in a frequency range regarding the power spectrum, far-end, near-end and total ICN for bandwidth can be calculated. It will be used to evaluate the crosstalk level of the newly designed models in this research.

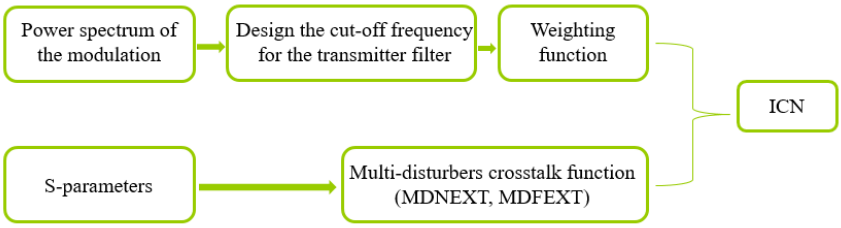


Figure 4.4. ICN calculation flow at a frequency point.

4.2. THE CONVENTIONAL PIN MAP DESIGN

The commonly-used pin map in the industrial community is the square pin map in Figure 4.5. Model 1 and 2 are 2 pin maps developed based on the square pin map. The difference between models 1 and 2 is model 2 has ground via between left side signal pairs and right side signal pairs. From model 1 to 2, the conventional way to mitigate crosstalk in the pin field is by increasing the spacing between signal pairs and adding more ground via for shielding. The shortage of this methodology is obvious, it will need more space and degrades the S:G in the PCB.

The area in the red rectangular markers is the unit cells. S:G can be calculated from each unit cells.

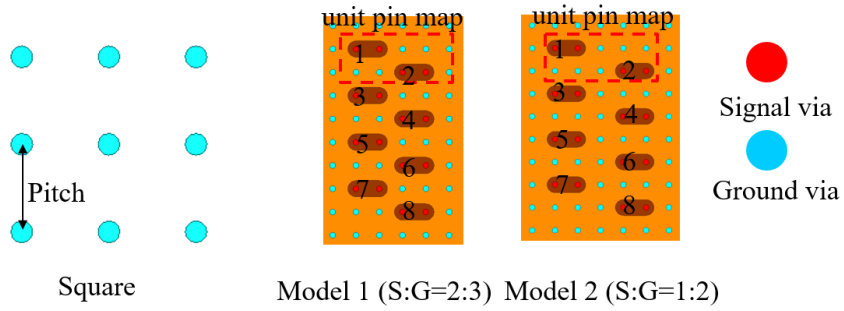


Figure 4.5. The conventional pin map design.

Model parameters:

- Via size: 10mils;
- Anti-pad: 28mils*40mils oblong;
- Pitch (via-to-via center spacing): 40mils;
- Dielectic: DK: 3.96; DF: 0.0175;
- Differential Characteristic Impedance: 95Ohm.

4.3. THE PROPOSED PIN MAP DESIGN

4.3.1. Advanced Unit Pin Maps. Based on the symmetry principle, two orthogonally put differential pairs can have zero crosstalk, the new unit pin map built in Figure 4.6. Conventional unit pin maps 1 and 2 are two unit cells cut from full conventional pin maps. Conventional unit pin map 2 has more ground vias between differential signal pairs and also the distance between signal pairs increased, this is the conventional way mitigating crosstalk and the efficiency will be verified. The new unit pin map will be compared to conventional unit pin maps 1 and 2 to verify the advantage of the new design and the crosstalk mitigation efficiency compare to the conventional way.

The characteristic impedance for all differential pairs has been tuned to a similar level. Figure 4.7 is the far-end, near-end and total ICN comparison for three unit cells up to 30Gbps. From the comparison, conventional unit pin map 2 has much lower ICN than 1, the conventional way canceling crosstalk work efficiently, the new unit pin map has much lower ICN than conventional unit pin map 1 and 2, even conventional unit pin map 2 has more ground vias for shielding and much spacing between signals, it can be

concluded that the new unit pin map is a better design on crosstalk cancellation and it works much more efficiency on crosstalk canceling than conventional way and it doesn't need more ground vias and much spacing.

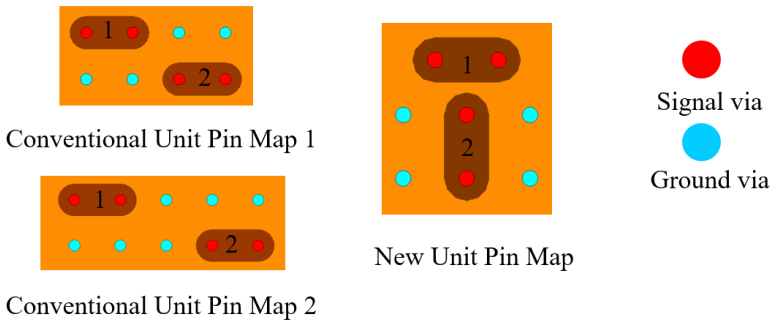


Figure 4.6. New unit pin map design.

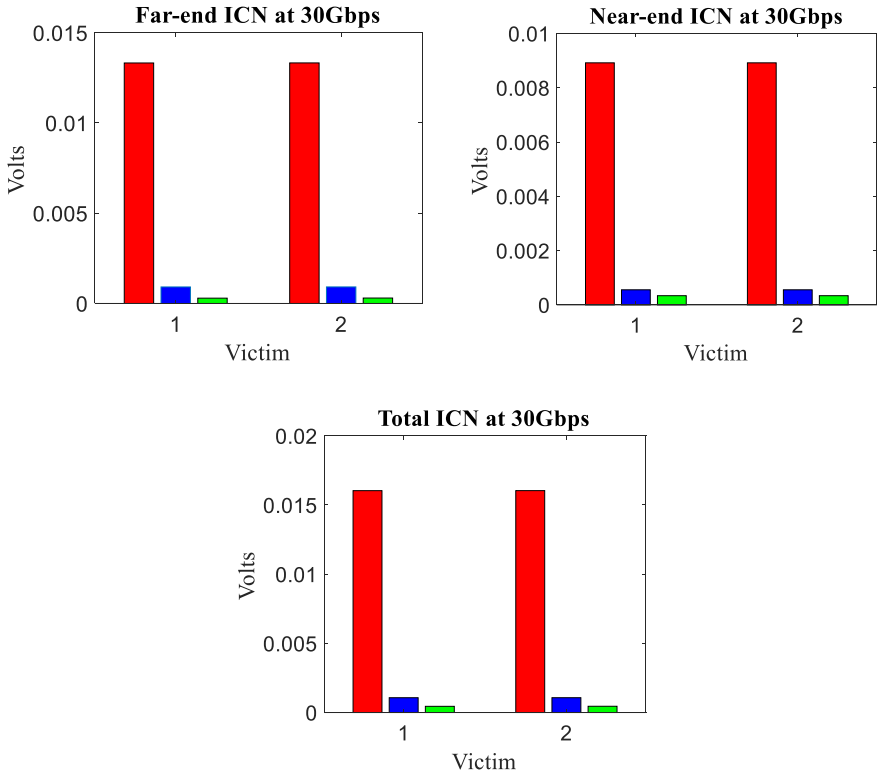


Figure 4.7. ICN comparisons of unit pin maps.

Figure 4.7. ICN comparisons of unit pin maps (cont.).

Model of variation can be developed like shown in Figure 4.8, pair 1 in the new unit pin map can be mirrored to the downside and model of variation developed. Symmetry principle applied to both the upper and downside in the variation model.

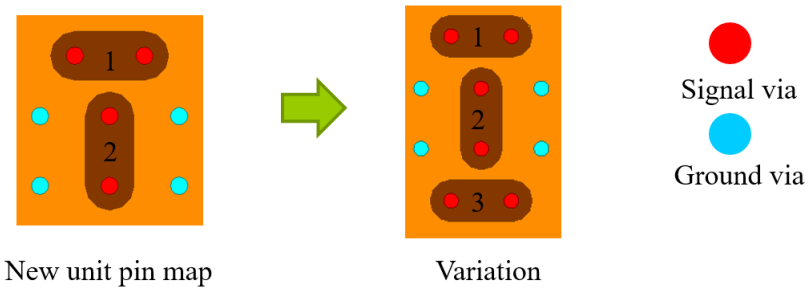


Figure 4.8. Variation of the new unit pin map.

4.3.2. Full Pin Maps Extension. There are more signal pairs than 2 in the real PCB, the new unit pin maps need to be extended and compared to the full conventional pin maps with the same or similar S:G.

The extension of the new unit pin map would be discussed first. Based on the new unit pin map, there are 2 kinds of full pin maps can be extended. Model 3 in Figure 4.9 extended through duplicate and move unit pin map rightwards and downwards, ground vias needed between pairs in the left and right side to prevent too much coupling between them. Other than model 3, model 4 has ground vias between pairs in the upper side and

downside, in this way, the coupling between upper side pairs and downside pairs can be isolated but it will decrease the S:G. Model 3 and model 4 will be compared to conventional models with similar S:G.

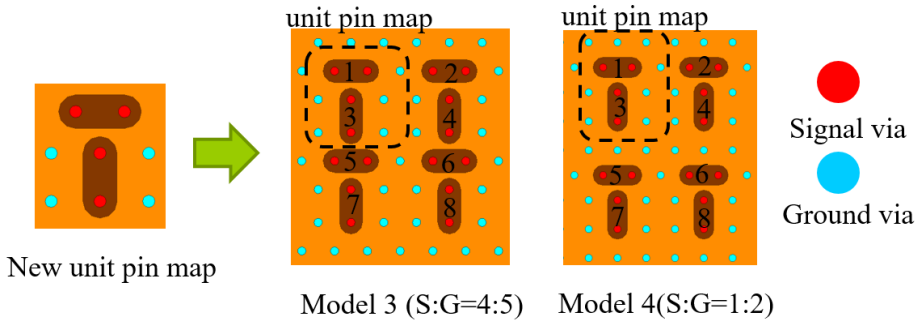


Figure 4.9. New unit pin map extension.

Model of variation can be extended to model 5 as it showed in Figure 4.10, extension methodology is the same as model 4 extension. Unit pin maps in the upper and downside must have ground vias in between, otherwise, there will be too much crosstalk between 4 signal pairs in the center of the pin map.

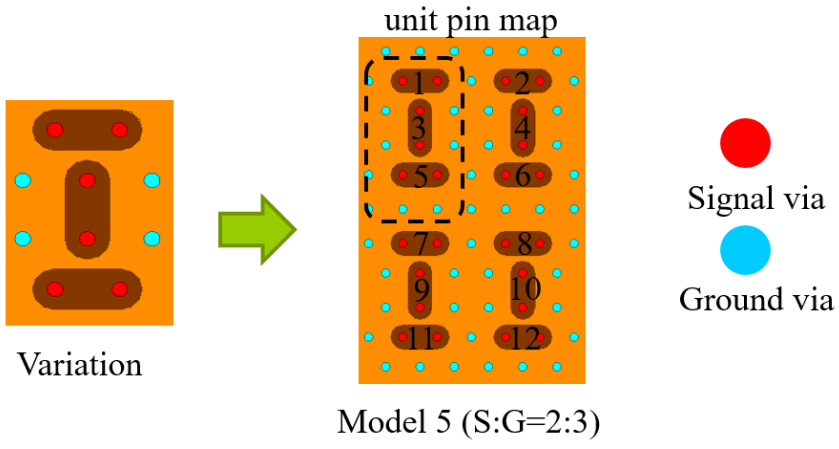


Figure 4.10. Model of variation extension.

4.4. ICN VALIDATION OF THE PROPOSED FULL PIN MAP

The TDR, insertion loss, and return loss of differential pairs in all models needs to be controlled and verified before validating ICN. Parameters mentioned above need to be controlled at a similar level to guarantee the pin pattern is the only variable that affects the ICN. Figure 4.11 showed the TDR of differential pairs in these models and there are on a similar level.

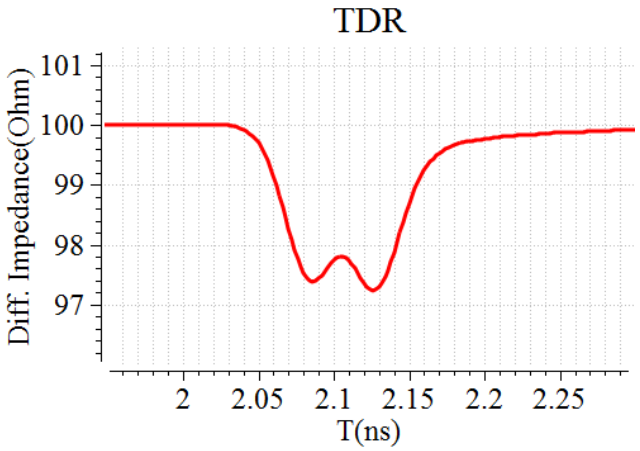


Figure 4.11. TDR verification.

Figure 4.12 showed the insertion and return loss of differential pairs. For different models, insertion loss and return loss of differential pairs are slightly different but close to the level showed below.

Before comparing the new designed full model to the conventional full model, here, comparing two conventional models with different S:G first verifying the efficiency of crosstalk cancellation of the conventional way in the fully extended pattern. Conventional full models with different S:G demonstrated in Figure 4.13.

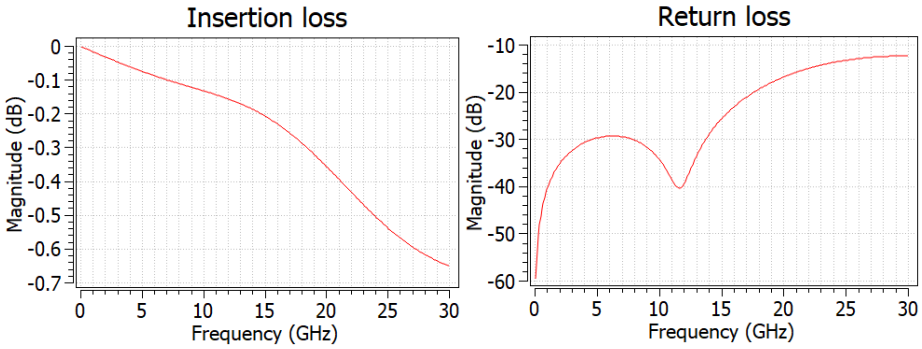


Figure 4.12. Insertion loss and return loss verification.

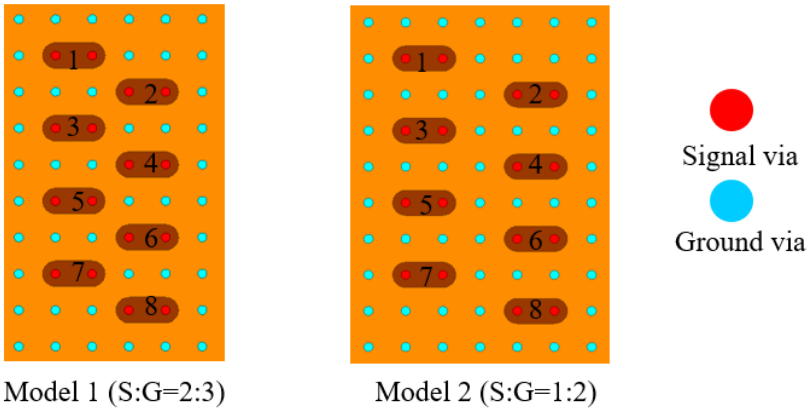


Figure 4.13. Conventional full pin maps.

Figure 4.14 is the ICN comparison results up to 30Gbps for two conventional full pin maps. Model 2 has a much lower ICN than model 1 as expected. Even for the extended full pin map, the conventional way mitigate crosstalk through adding space and ground via still works effectively.

After the evaluation of the traditional strategy, herein, verifying the crosstalk cancellation of the new design. They will be divided into two groups.

- Group1: Model 3, 5 vs. model 1;
- Group2: Model 4 vs. model 2.

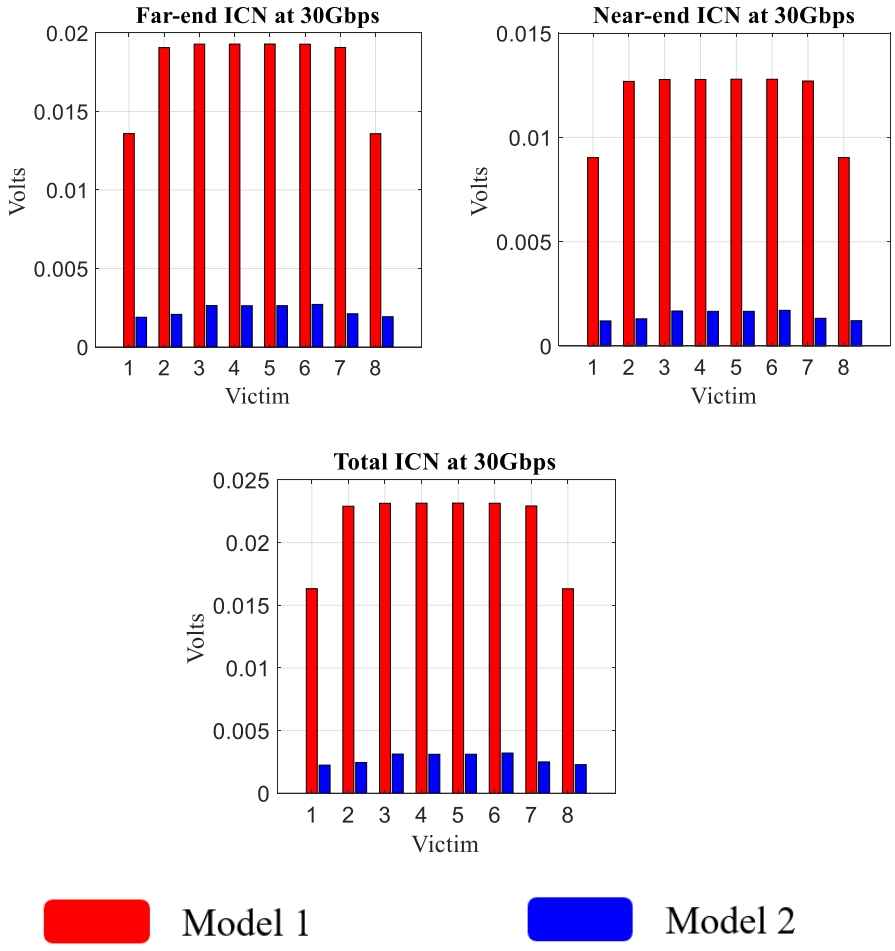
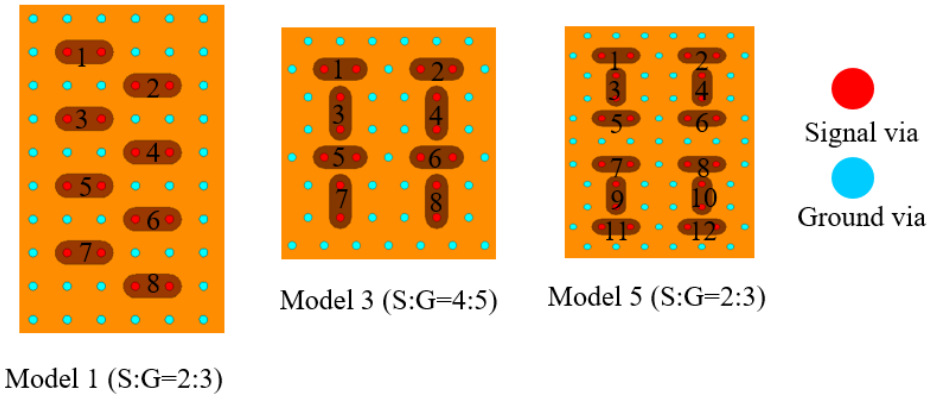


Figure 4.14. ICN comparisons of the full conventional pin map.

Model 3, 5 and 1 divided into the same group since the experimental group models 3 and 5 have higher or the same S:G ratio as model 1. Model 4 has the same S:G as model 2 and there are comparable. It is important to control variates in the experiment to have a rigorous result and conclusion.

Figure 4.15 depicted the model and ICN comparisons of the first group. Both model 3 and 5 have much less ICN than model 1, even model 3 has higher signal pin density. In the pin field area, two proposed full pin maps have much lower crosstalk than conventional pin map but maintained or even increased S:G has been developed.

From the ICN comparison, for model 1, pair 1 and 8 have lower ICN than others since comparing to other ports, they have less aggressor from the upper and downside individually. Pair 3, 4, 7, 8 in model 3 have much larger ICN since there are too close to being coupled by each other and there are no ground vias in between for shielding. In model 5, pair 5, 6, 7, 8 have larger ICN because there are close to each other.



(a)

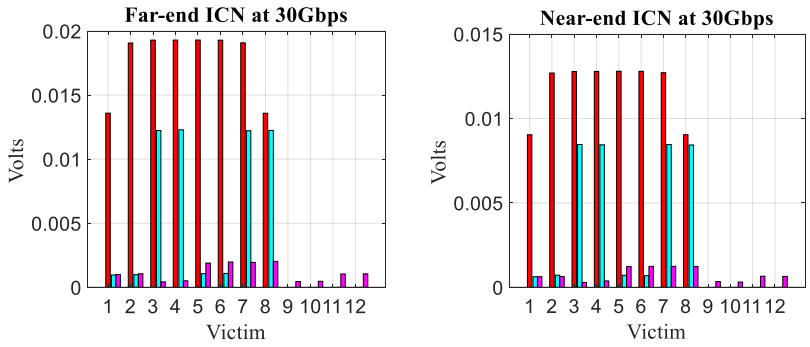


Figure 4.15. Comparisons of group 1: (a) models; (b) ICN.

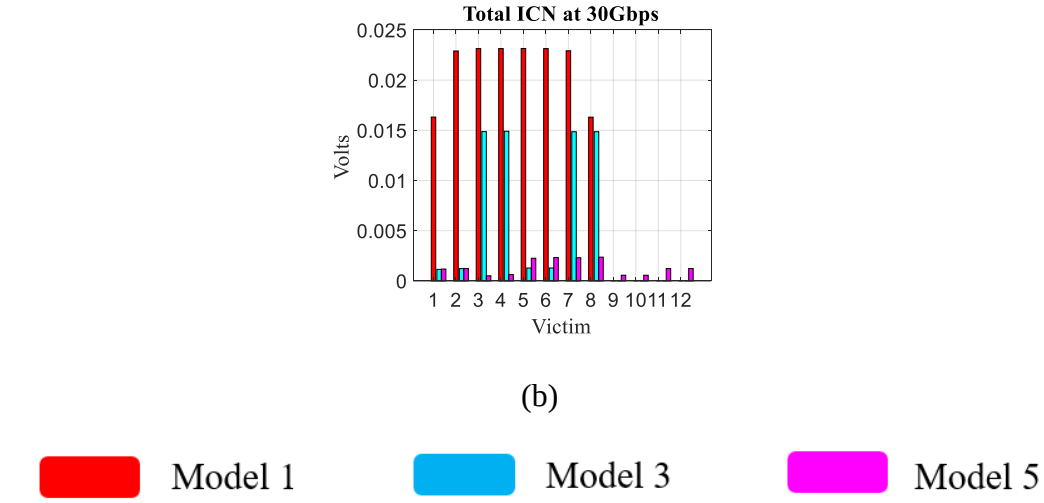
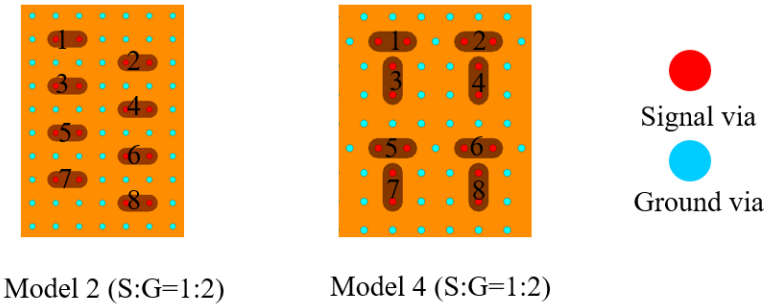


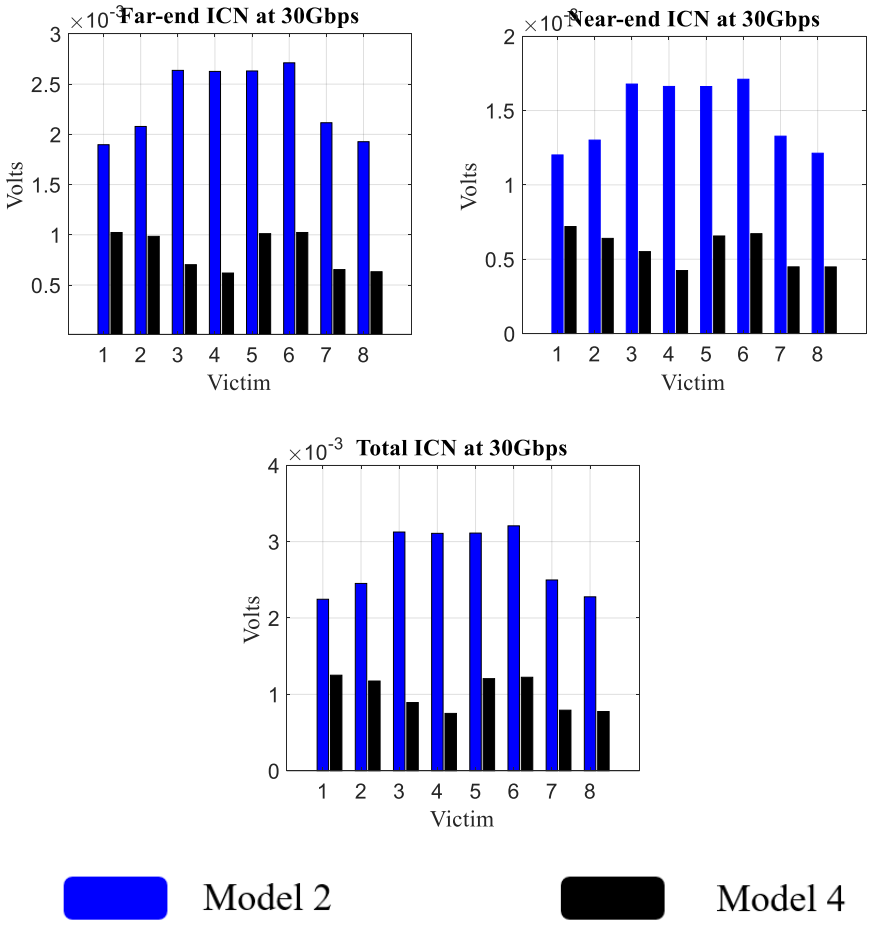
Figure 4.15. Comparisons of group 1: (a) models; (b) ICN (cont.).

For the second group comparison, model 4 is compared to model 2. (a) in Figure 4.16 showed models in group 2, from (b) ICN comparisons, model 4 has much lower ICNs than model 2 up to 30Gbps. In model 2, pair 1, 2, 7, 8 have less ICN since fewer signal pairs around and there will be fewer aggressors. In Model 4, ICN in pairs 3, 4, 7, 8 have been decreased after the separation and adding ground vias between signal pairs.



(a)

Figure 4.16. Comparisons of group 2: (a) models; (b) ICN.



(b)

Figure 4.16. Comparisons of group 2: (a) models; (b) ICN (cont.).

Table 4.1 showed the average ICN and Table 4.2 showed the worst-case ICN of all pin patterns. For each group, the newly designed pin patterns have much lower ICNs than the conventional design.

From unit pin maps to full pin maps extension, there are 3 new pin patterns proposed with much lower ICN than the conventional pin map but maintained or even increased the S:G. Models verified by ICN calculation regarding simulated s parameters from full-wave modeling. Other variates have been controlled at a similar level for the

comparison, like TDR, insertion loss and return loss. New proposed pin maps have far lower crosstalk without disturb any other signal integrity performances.

Table 4.1. Average ICN comparisons of full pin maps.

Model	1	2	3	4	5
S:G	2:3	1:2	4:5	1:2	2:3
Far-end (mV)	18.1	2.3	6.5	0.81	0.6
Near-end (mV)	11.8	1.5	4.5	0.58	0.5

Table 4.2. Worst-case ICN comparisons of full pin maps.

Model	1	2	3	4	5
S:G	2:3	1:2	4:5	1:2	2:3
Far-end (mV)	19.5	2.6	12.3	1.0	1.9
Near-end (mV)	12.7	1.7	8.3	0.71	1.4

5. THE CORRESPONDING TRACE ROUTING DESIGN FOR THE PROPOSED PIN MAP

5.1. TRACE ROUTING FOR THE ADVANCED UNIT PIN MAP

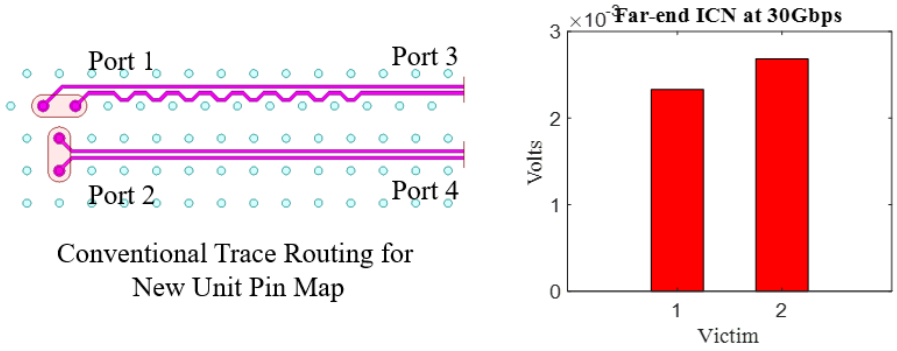
Trace routing in PCBs is for horizontal electrical interconnections between chips, components being mounted. For the proposed new pin map, trace routing should be studied and designed, differential signal pairs of proposed pin maps displaces differently, conventional trace routing can not be directly applied and it needs to be re-designed to route in the required direction, and also the trace routing should maintain the crosstalk benefit in the pin field area.

5.1.1. The Conventional Trace Routing on the Advanced Unit Pin Map

Verification. For the trace routing design, trace on a new unit pin map would be studied and optimized first, it would be compared to the conventional unit pin map with trace routing. The newly designed trace will be applied to the full pin maps and verified in the end.

In Figure 5.1 (a), the conventional trace routing has been applied to the new unit pin map. Bumps in pair 1 are for P/N skew compensation since crosstalk of orthogonal pin map is very sensitive to the P/N skew, large P/N skew in pair 1 can cause coupling from pair 2 to P/N in pair 1 has different phase in the far-end, at port 3, induced coupling at P/N have the same amplitude but different phase, far-end crosstalk induced. (b) showed the far-end ICN up to 30Gbps of the proposed configuration. This routing design will be decomposed analyzed to try to verify if it is a good design or to find a better design that has lower crosstalk.

Far-end ICN will be analyzed as the reference here for trace routing optimization.



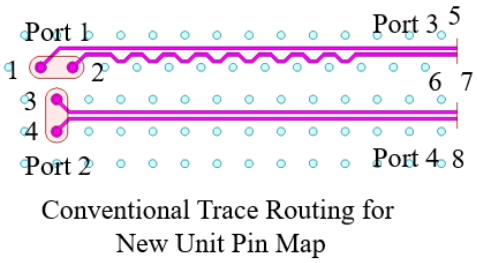
(a) (b)

Figure 5.1. New unit pin map with conventional trace routing: (a) model; (b) ICN.

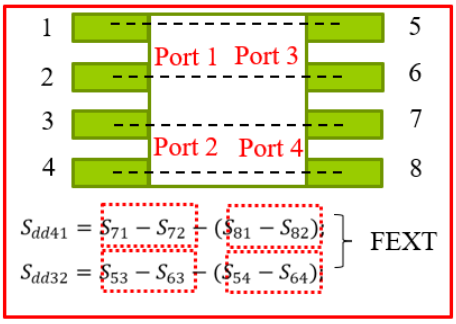
Figure 5.2 (a) is the signal-ended and differential port configuration of the new unit pin map with conventional trace routing, (b) showed the single-ended to differential far-end crosstalk s parameter transformation functions. For individual differential far-end crosstalk it can be decomposed into two parts as red rectangle marked and the decomposed s parameters plotted in (c), the gaps between red and blue lines are the crosstalk induced. The crosstalk level can still be improved, the level of the red line can be reduced to be close to the blue line. Physically, reduce the red line level is balance the coupling from channel 3 to channel 1 and 2.

Coupling from channel 3 to channel 1 and 2 in the proposed model is not balanced. Unbalanced coupling might come from 3 types of coupling below:

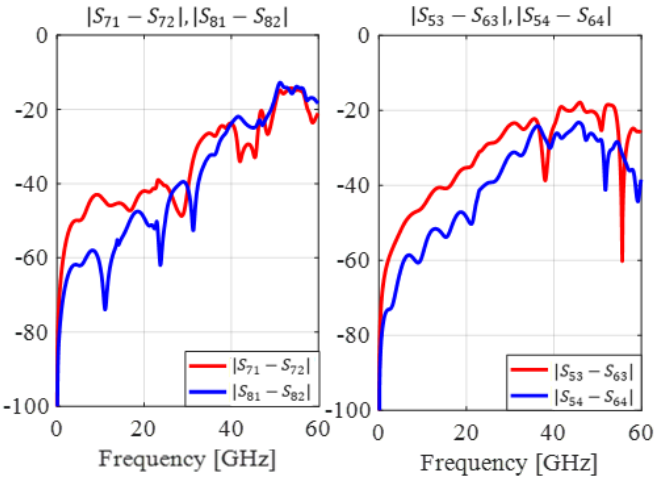
1. Via-to-via coupling;
2. Trace-to-trace coupling;
3. Via-to-trace coupling.



(a)



(b)

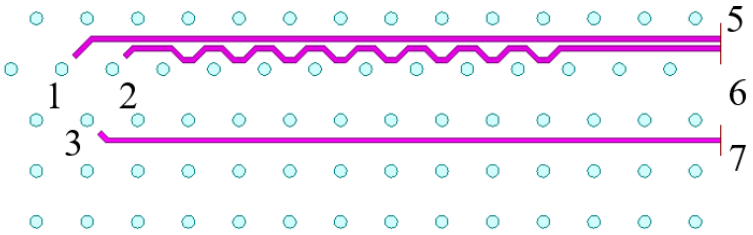


(c)

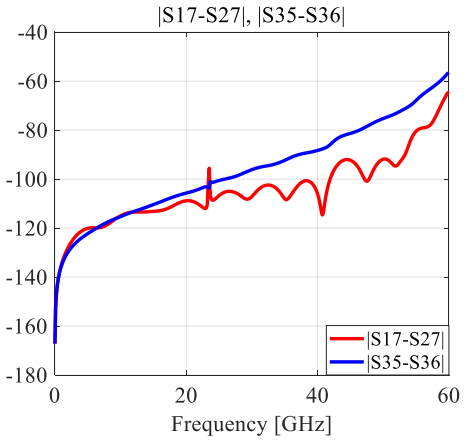
Figure 5.2. (a) New unit pin map with conventional trace routing; (b) single-ended to differential far-end crosstalk transformation; (c) far-end crosstalk decomposed analysis.

The unbalanced coupling does not likely come from via-to-via coupling, from previous research, the orthogonal pin map design has a few coupling. Another source is

the trace-to-trace coupling, to investigate that, traces in channels 1, 2, and 3 have been cut and have been full-wave simulated. Figure 5.3 (a) showed the simulation model. (b) showed the far-end coupling between channels 3 and 1, 2, parently, the differences maintained at a very low level, the unbalanced coupling does not likely come from the trace-to-trace coupling.



(a)



(b)

Figure 5.3. Crosstalk between traces verification: (a) model; (b) far-end crosstalk analysis.

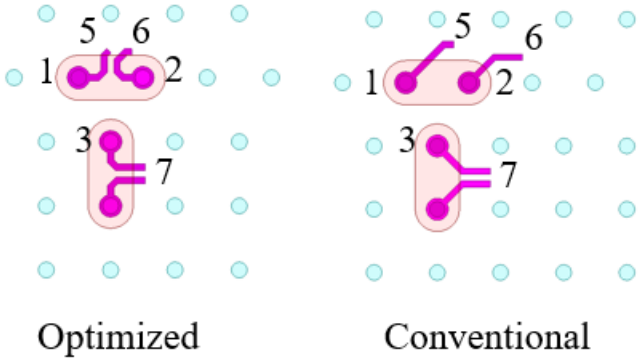
5.1.2. Design of the New Trace Routing. There is only one source left that is the via-to-trace coupling. To investigate the coupling from via-to-trace, vias and

interconnections between vias and traces have been cut and simulated. In Figure 5.4 (a), it is suspected that in the conventional model, coupling from via 3 to trace 1 and 2 are not balanced, via 3 has more coupling to trace 1 since there are closer, furthermore, trace 1 has more length in the anti-pad area than trace 2, wave velocity of traces in the anti-pad area is different than it has reference upper and downsides, this will cause phase skew in pair 1 and increased the far-end crosstalk from pair 2 to 1. Based on that, the optimized model designed, traces in the P/N of pairs routed to the center first then routed out, in this way, the coupling would be balanced and coupling transition in P/N of pair 1 would be the same too, theoretically, it can improve the crosstalk performance a lot. Pair 3 in the optimized model has the same design as pair 1 to avoid the unbalanced coupling from trace 3 to vias in pair 1. The model of optimized has been simulated with the same set up as the model of conventional.

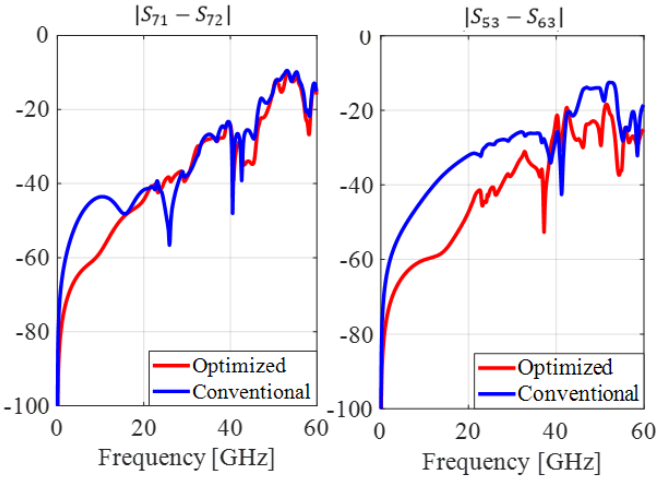
Figure 5.4 (b) demonstrated the improvement of crosstalk performance after optimization. The red line is the far-end crosstalk after the optimization and the level of it decreased a lot compared to the blue line, the far-end crosstalk of the conventional model. Unbalance coupling of the conventional routing specified new pin map comes from the via-to-trace coupling and better design is also presented.

In Figure 5.5 (a), full traces applied on both optimized and conventional model, reference is the conventional unit pin map with trace routing design. P/N skew in all pairs is tuned and all three models simulated under the same simulation setting. From far-end ICN comparison up to 30Gbps in (b), by comparing optimized routing to conventional routing, optimization of trace routing can decrease the crosstalk a lot, by comparing the reference to conventional and optimized routing, before optimization, new unit pin map

with trace routing has higher far-end ICN, after optimization, it has lower far-end ICN, the trace routing optimization is indeed, otherwise, the crosstalk benefit in the pin area is destroyed totally.

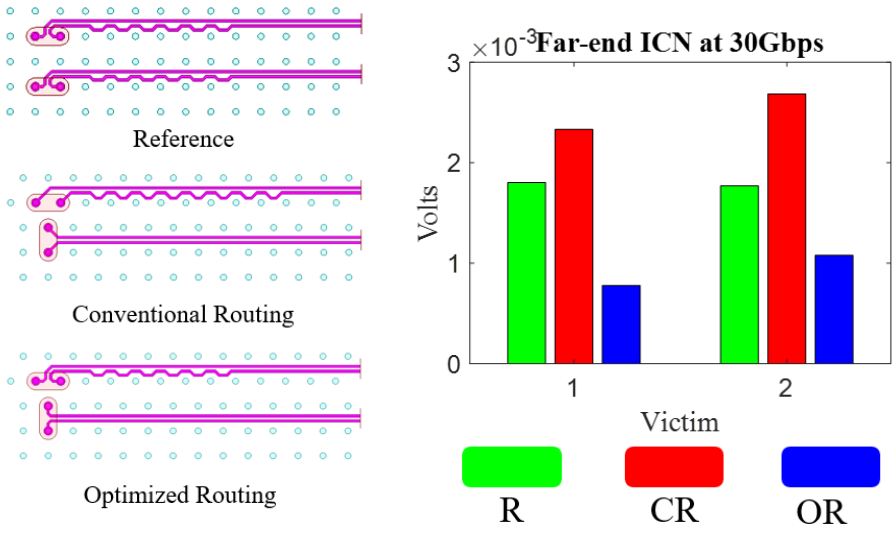


(a)



(b)

Figure 5.4. Optimized trace routing vs. conventional trace routing: (a) model; (b) far-end corsstalk.



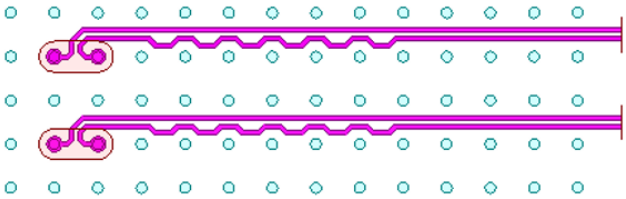
(a) (b)

Figure 5.5. Optimized routing vs. conventional routing vs. reference: (a) model; (b) far-end ICN comparison.

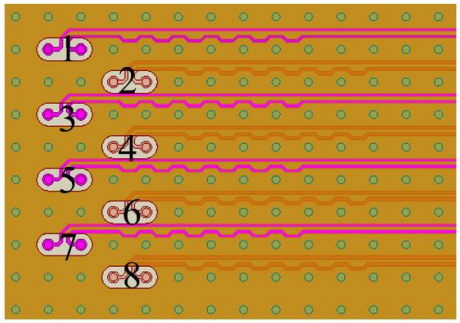
5.2. FULL PIN MAPS TRACE ROUTING IMPLEMENTATION

After the trace routing design for the unit pin map, the optimized trace routing needs to be applied to full pin maps and verified.

Trace routing for the conventional pin maps is studied first. Based on the model of reference, models 1 and 2 with trace routing developed. Model 1 and model 2 with trace routing can be developed by simply apply traces on the pin maps. The P/N skew of all pairs in model 1 and 2 are tuned to guarantee no other variables would be introduced to disturb the crosstalk level. Figure 5.6 (b)(c) showed models 1 and 2 with trace routing individually. All pairs in model 1 and model 2 can be routed in the same layer, for both model 1 and model 2, they have the same board width it means the introduced trace length is the same.



(a)



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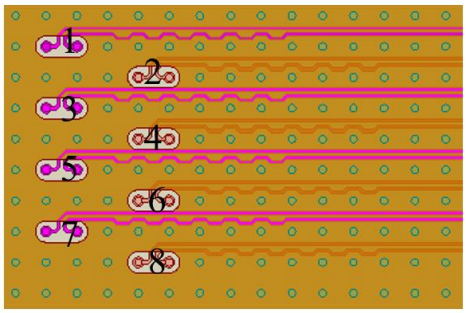


(c)

Figure 5.6. (a) Conventional unit layout; (b) model 1 with trace routing; (c) model 2 with trace routing.

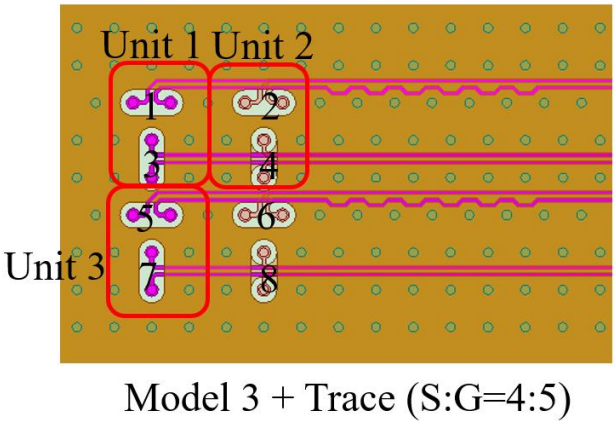
For the trace routing for proposed full pin maps, trace routing for model 3 discussed first. There are four unit cells in model 3, unit 1 directly applied optimized trace routing, from unit 1 to unit 2, it is worth to mention that unit 2 need to routing in a different layer.

The routing layer of unit 2 has been assigned above routing layer of unit 1 with 2 ground layer in between, and there are 2 reasons:

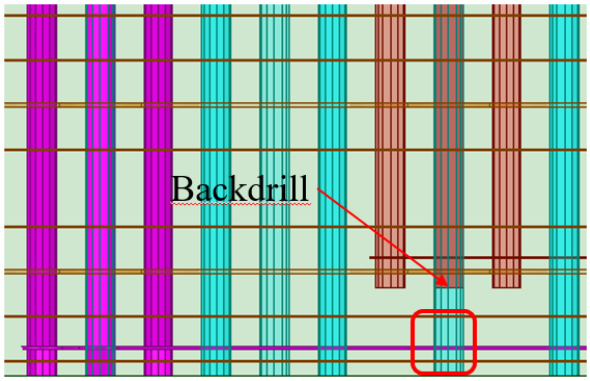
1. Avoiding overlap of traces with unit 1;
2. Unit 2 routing above to avoid coupling between vias in unit 2 and traces in unit 1.

Figure 5.7 (b) shown such methodology can avoid the undesired coupling.

From unit 1 to unit 3, traces in unit 3 can be directly duplicated from traces in unit 1. Model 3 with trace design showed in Figure 5.7.



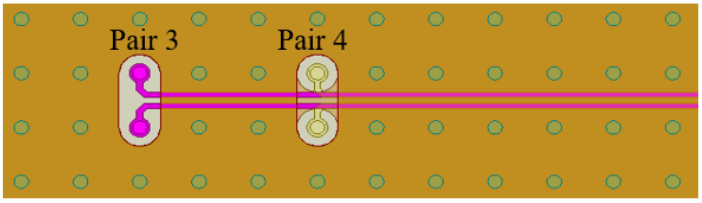
(a)



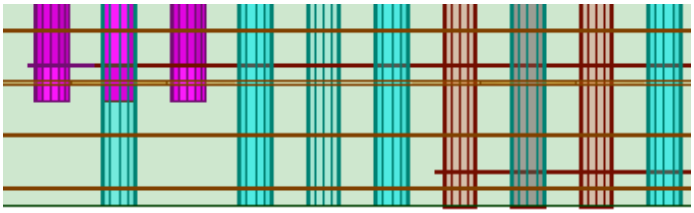
(b)

Figure 5.7. Model 3 with trace routing design: (a) top view; (b) frount view.

It is been verified that unit 2 needs to be routed above unit 1 and higher enough. In Figure 5.8 (a), pair 3 and 4 have been cut from model 3 with trace routing, (b) is the design of pair 4 routed below pair 3, (c) is the design of pair 4 routed above pair 3.



(a)



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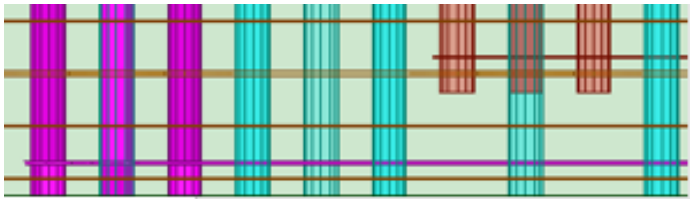


(c)

Figure 5.8. (a) Model of pair 3 and 4 cut from model 3; (b) pair 4 routing below; (c) pair 4 routing above.

Figure 5.9 demonstrated the ICN comparisons of two different designs up to 30Gbps. The model of pair 4 routing above has far fewer ICNs than the other design as expected. The reason why pair 4 routing below has much larger ICN is because of the coupling between traces in pair 3 and vias in pair 4, there are too close to each other and

the capacitive coupling between them makes the ICNs increased significantly. This situation avoided in the model of pair 4 routings above. Also, the routing of pair 4 needs to be higher enough, the coupling between traces and vias needs to be avoided.

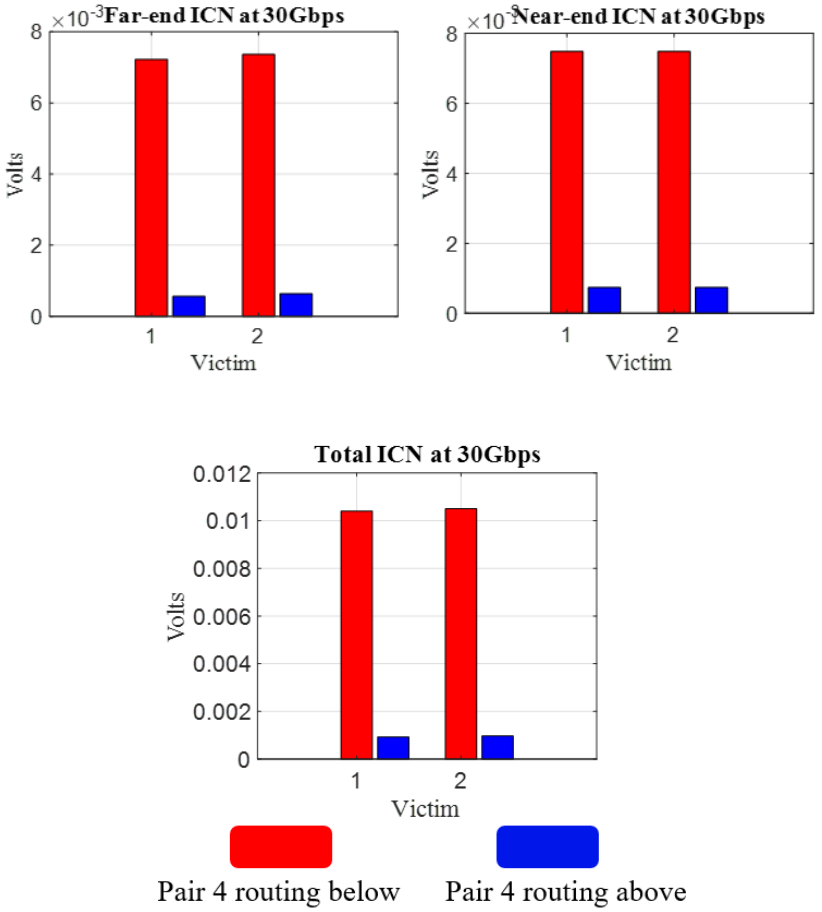
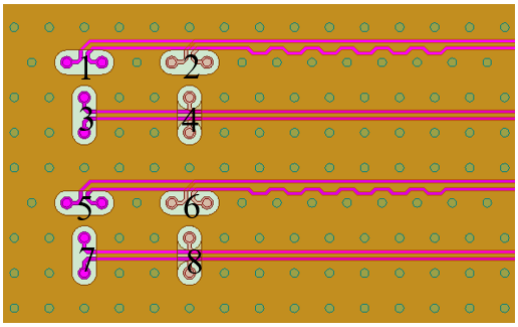
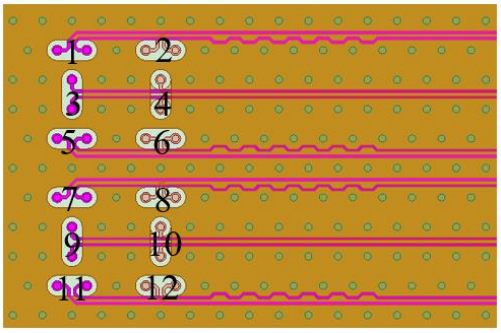


Figure 5.9. ICN comparisons of different routing strategies.

Based on the model of model 3 + trace, model 4 + trace and model 5 + trace extended. Figure 5.10 showed the trace routing for models 4 and 5. For the full-wave simulation of the three newly designed models, P/N skew of all pairs are tuned.



(a)



(b)

Figure 5.10. (a) Model 4 with trace routing; (b) model 5 with trace routing.

All 5 conventional and newly designed pin maps with trace design are full-wave simulated under the same simulation setting. ICNs are compared up to 30Gbps in Figure 5.11. The comparisons are divided into two groups regarding the S:G ratio, Figure 5.11 (a) – (c) showed the ICN comparisons for S:G=1:2 group and (d)-(f) showed the ICN comparisons for S:G=2:3 group. Basically, after the trace routing optimization for orthogonal layouts, the crosstalk cancellation in the pin field area is well maintained, orthogonal pin maps with trace routing design still have much lower crosstalk than conventional pin maps with trace routing design. For the implementation of the orthogonal layouts, there are 3 requirements for the trace routing:

1. The interconnection between via and trace needs to observe the symmetry principle also and it needs to be routed like mentioned above;
2. The P/N skew in the orthogonal layouts is required to be well controlled, the crosstalk of the orthogonal layouts is very sensitive to the P/N skew in differential pair;
3. To avoid traces overlap and more crosstalk induced, more routing layer is needed.

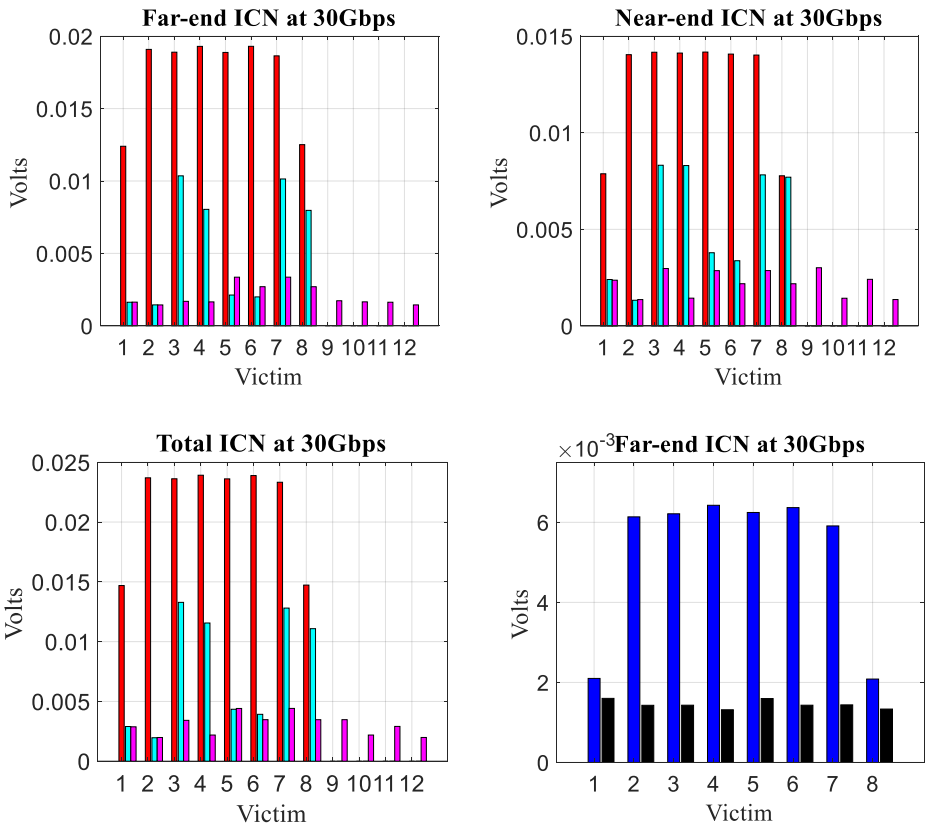


Figure 5.11. ICN comparisons after the newly designed trace routing introduced.

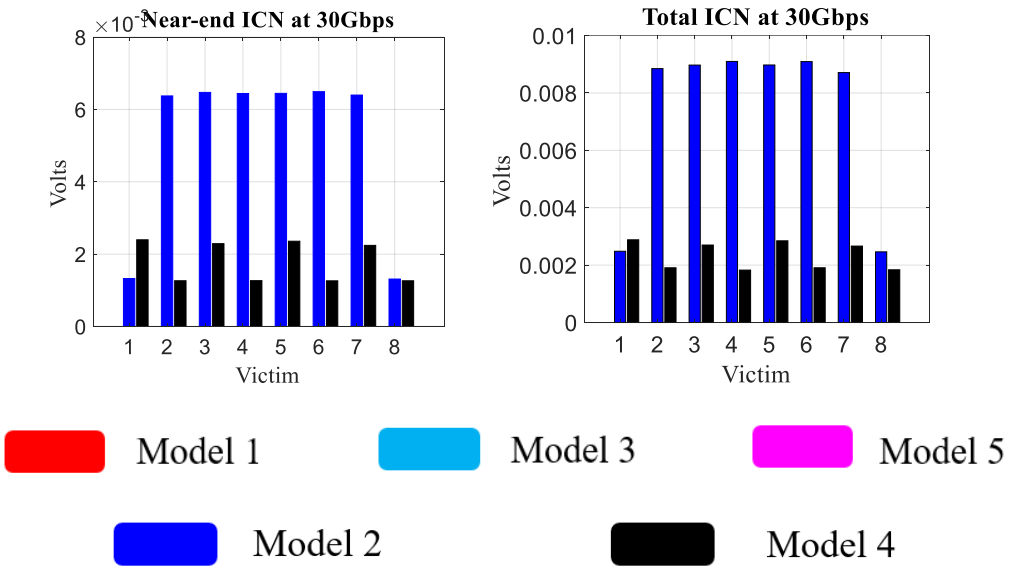


Figure 5.11. ICN comparisons after the newly designed trace routing introduced (cont.).

Comparisons of the average and worst-case ICN of all 5 models are demonstrated in Table 5.1 and Table 5.2. From the observation of more specific values. After the advanced trace routing introduced, the newly designed model still has a lower average and worst-case ICNs than the conventional model for each group. The proposed layouts have the advantages of crosstalk cancellation with maintained or even increased S:G.

Table 5.1. Average ICN comparisons of full pin maps with trace routing.

Model	1	2	3	4	5
S:G	2:3	1:2	4:5	1:2	2:3
Far-end (mV)	17.0	5.11	5.57	1.62	3.13
Near-end (mV)	12.6	5.13	5.25	1.65	2.10

Table 5.2. Worst-case ICN comparisons of full pin maps with trace routing.

Model	1	2	3	4	5
S:G	2:3	1:2	4:5	1:2	2:3
Far-end (mV)	19.3	6.35	10.3	1.71	3.70
Near-end (mV)	17.9	6.36	8.30	2.43	3.17

6. RESEARCH ON THE ORTHOGONAL LAYOUT INDUSTRIAL IMPLEMENTATION

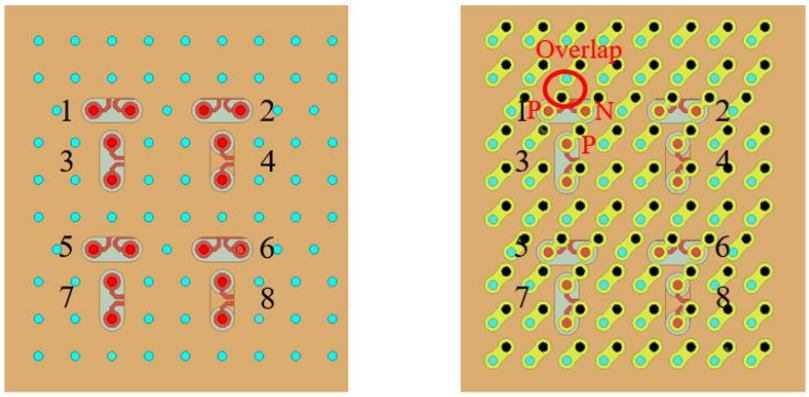
The previous study only contains the pin maps and the corresponding trace routing design. But in the real PCB product, between the chip package and the via, there are dog-bones, solder balls. The introduction of the dog-bone and solder ball may disturb the crosstalk cancellation in the advanced orthogonal layouts and it needs to be verified and improved. In the end, the whole structure of the conventional design and the advanced design underneath the package needs to be full-wave simulated and the crosstalk will be validated.

Except for interconnecting packages to vias by dog-bones, via in pad plated over (VIPPO) process can be an alternative too but regarding the high-expense of the VIPPO process, implementation of the dog-bone is mainstream in the industry. Herein, the application of the dog-bone will be discussed first, then come to the VIPPO.

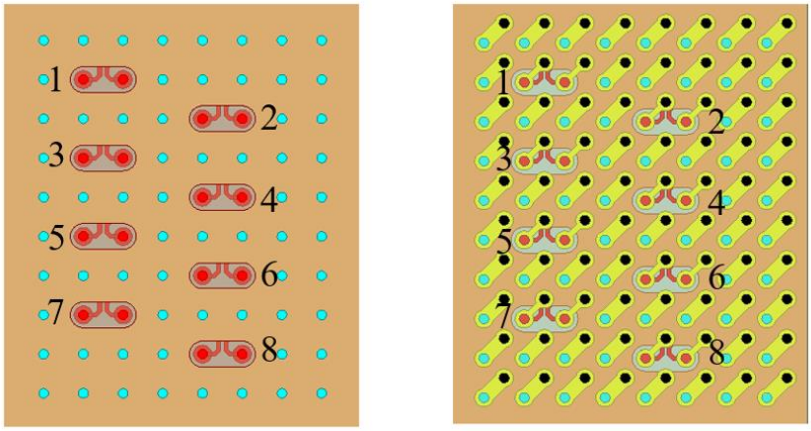
For the following research, a new stack up that has been widely used in the industry applied and it is been verified that the new stack up still maintained the crosstalk cancellation advantage of the orthogonal layout.

The conventional dog-bone design applied on model 4 with trace routing design first. Figure 6.1 (a) showed the implementation of the dog-bone and the solder ball on models 4. It is worth to mention that the standard length of the dog-bone does not apply to the pin pattern of model 4 since dog-bones will overlap with one and another due to the offset of pins. To overcome it, dog-bones swept from 23mils to 14mils, 23mils is the largest dog-bone length to avoid dog-bone overlap and with minimum metal-to-metal spacing. To do apple-to-apple comparisons, the conventional dog bone and solder ball

also applied to the conventional design model 2 with trace routing shown in (b). (c) depicted the front view before and after dog-bones and solder balls introduced. The thickness of the dog-bone and the solder ball is the standard thickness in the industrial community.

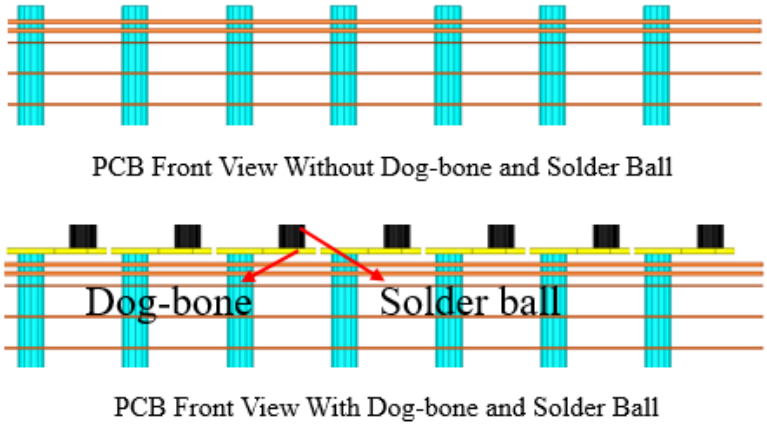


(a)



(b)

Figure 6.1. (a) Model 4 with dog-bone design; (b) model 2 with dog-bone design; (c) front view of PCB with dog-bone design.



(c)

Figure 6.1. (a) Model 4 with dog-bone design; (b) model 2 with dog-bone design; (c) front view of PCB with dog-bone design (cont.).

New models with dog-bones and solder balls are full-wave simulated and ICNs are compared up to 10Gbps as showed in Figure 6.2. From the ICN comparisons, shorter dog-bones will induce lower crosstalk in model 4 and the dog-bone length needs to be less than 14mils to maintain the crosstalk advantage compares to model 2 with dog-bones. From 14mils dog-bone to 23mils dog-bone, crosstalk increased significantly because longer dog-bones will disturb the coupling balance in the orthogonal unit cell. Taking pair 1 and 3 in model 4 with dog-bone for example, when dog-bone is long enough, P/N in pair 1 would have different length signal returns underneath, the wave speed would be different in P/N and this will cause crosstalk phase skew in the trace side, it will increase the crosstalk significantly, and also, P in pair 3 would have larger crosstalk to N in pair 1, through the pad to pad coupling, unbalanced coupling would increase the crosstalk also. 14mils is too short to be applicable. Also, the conventional dog-bone design on model 4 will need the chip vendors to change their chip package to

adopt the new BGA, this can be very expensive. Optimization of the dog-bone design for model 4 needs to be studied.

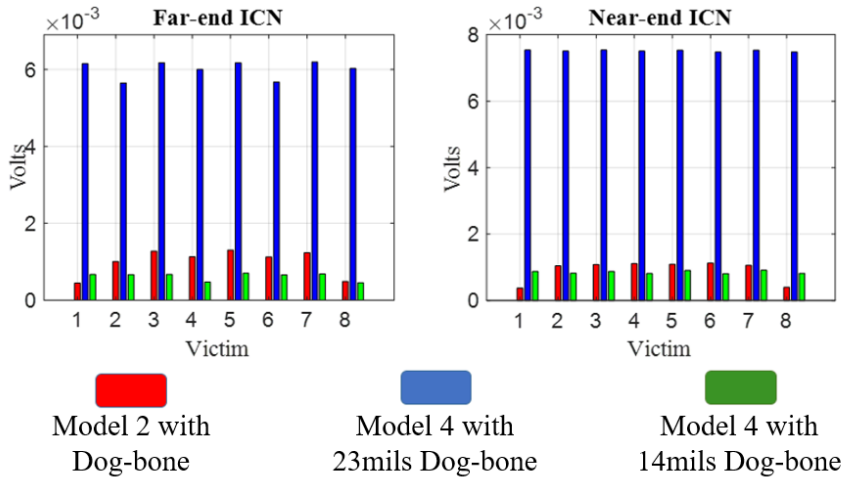


Figure 6.2. ICN comparisons after the conventional dog-bone design applied.

6.1. STUDY OF THE ORTHOGONAL LAYOUT INDUSTRIAL REALIZATION WITHOUT CHANGING CHIP PACKAGE

To satisfied the requirement mentioned above, the dog-bone is re-designed for model 4. Figure 6.3 depicted the newly dog-bone design. There are some rows applied dog-bones and the BGA relocated to the right side to align with other pins, other pins remains the same pattern by applying VIPPO. In this way, the chip package can fit with the new BGA and the dog-bone length will be enough. This design also intentionally kept the coupling and transition balance for parallelly placed differential pairs by the VIPPO process. Figure 6.4 showed the ICN comparisons between model 4 with the new dog-bone design and model 2 with dog-bone design. The relative crosstalk level of two models remained as the dog-bone and solder ball are not introduced as expected.

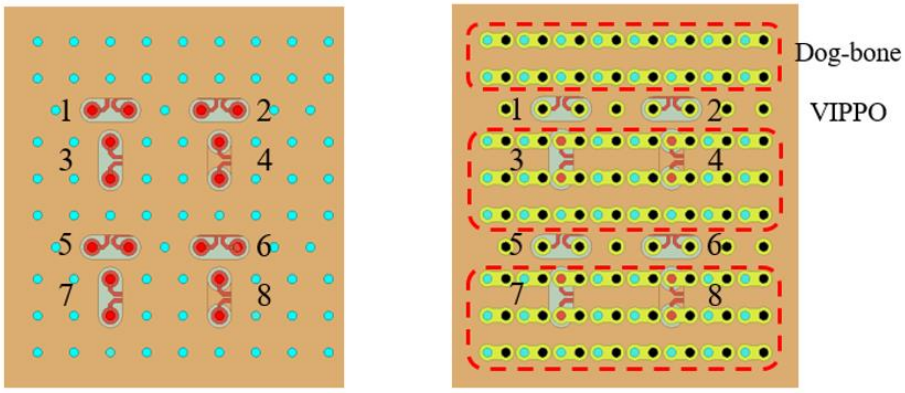


Figure 6.3. Model 4 mixed dog-bone and VIPPO design.

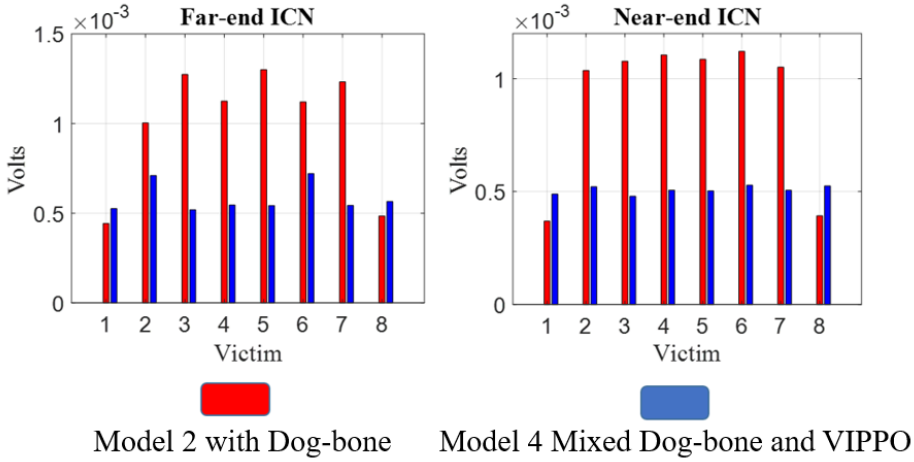


Figure 6.4. ICN comparisons after the mixed dog-bone and VIPPO design.

Even though the new method maintained the crosstalk level, satisfied the manufacturing and relocated the BGA but it still not applicable since the reliability problem. Mixed dog-bone and VIPPO design can cause mechanical problems after the reflow and soldering of chips. The mechanism is depicted in Figure 6.5. During the process of soldering chips on PCBs, due to the VIPPO vias has higher high thermal conductivity, solder balls above it will melt faster, in the same time, PCB underneath the

surface landing pad of dog-bone has a higher coefficient of thermal expansion (CTE) makes two sides lifted and a gap between the chip package and solder balls created. This means some channels will be in an open condition and it will cause some reliability problems. Mixed dog-bone and VIPPO is not preferable in the industrial community.

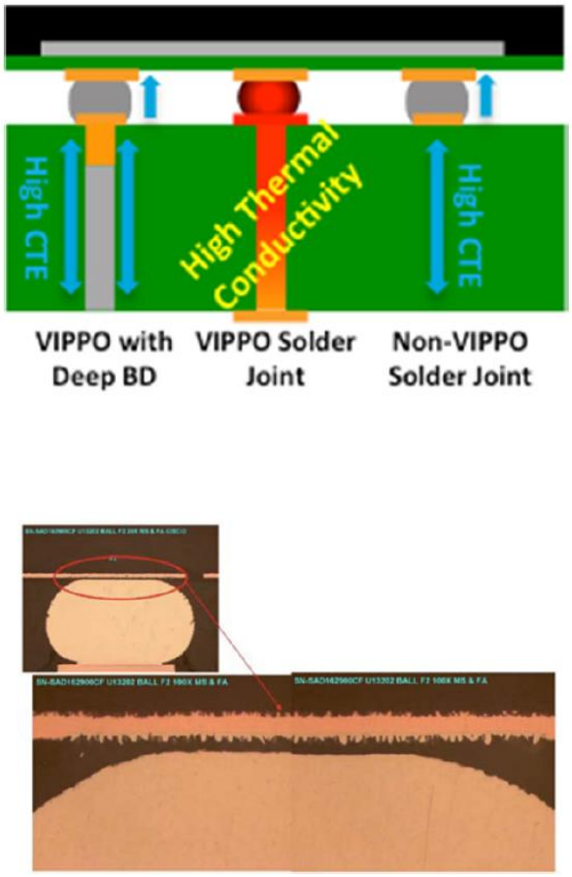
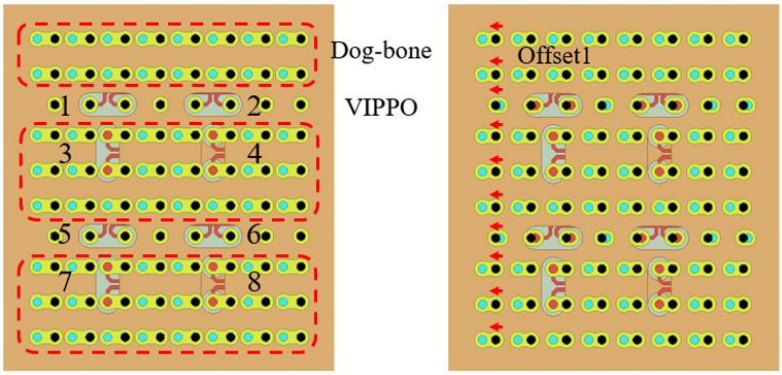


Figure 6.5. Reliability problem in the mixed dog-bone and VIPPO PCB.

There is one way that can solve the reliability issue. Methodology depicted in Figure 6.6 (a), BGA in the previous mixed model can be swept to the left side, in this way, previous VIPPO structure will become with dog-bone design, dog-bones already exists in the mixed model will be shorter, all vias can have dog-bone applied. There is

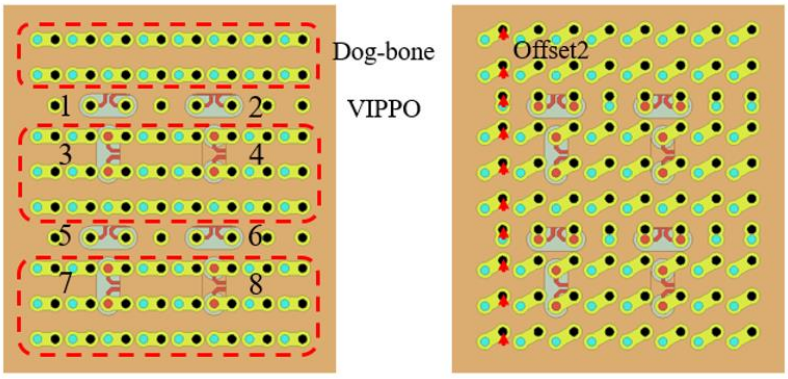
one shortage of this methodology, sweep dog-bones mounted on parallel placed differential pairs can disturb the coupling balance inside the unit cell and transition balance of this differential pair, when the offset goes longer, dog-bone on via 1 starts to has reference plane underneath and this will change the wave velocity and resulting phase skew in the receiver side when the phase skew goes larger, higher crosstalk would be induced, and also, via 3 would has higher coupling to dog-bone on via 2, this would disturb the symmetry principle also and causes increasing of ICN. To resolve this problem, another methodology introduced in (b), BGA can be upwards swept. Both offset 1 and 2 are swept to trade-off the dog-bone length and the ICN.

The ICN results in Figure 6.6 (c) showed the increase of the offset increases the crosstalk as expected. The ICNs also demonstrated 7mils is the breakpoint for both offset 1 and 2. The offset is not allowed to exceed 7mils to maintain the crosstalk cancellation advantage of the orthogonal layout.

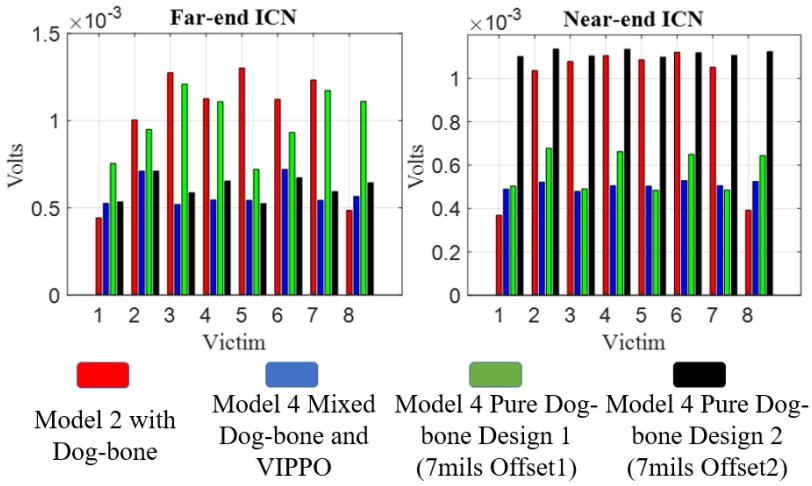


(a)

Figure 6.6. (a) Methodology 1 to solve realiability problem; (b) methodology 2 to solve realiability problem; (c) ICN validation.



(b)



(c)

Figure 6.6. (a) Methodology 1 to solve realiability problem; (b) methodology 2 to solve realiability problem; (c) ICN validation (cont.).

To realized the previous 2 methods means the minimum of 7mils dog-bone exists. 7mils dog-bones are too short to be applicable in this industry. Figure 6.7 showed the dog-bone size requirements from one of the vendors in the industrial community. It has minimum via capture size of 18mils and minimum BGA solder mask window is 20mils, finished hole size is 8mils and minimum via solder mask window is 14mil, the minimum

solder mask web is 4mils and after the mathematical calculation, the minimum dog-bone length is 21mils (20/2+14/2+4). Existing of solder mask web is for preventing solder flows from the landing pad to the finished hole of the via during the reflow process. The leaking of the solder will cause the loss of mechanical and electrical connections between the package and the PCB.

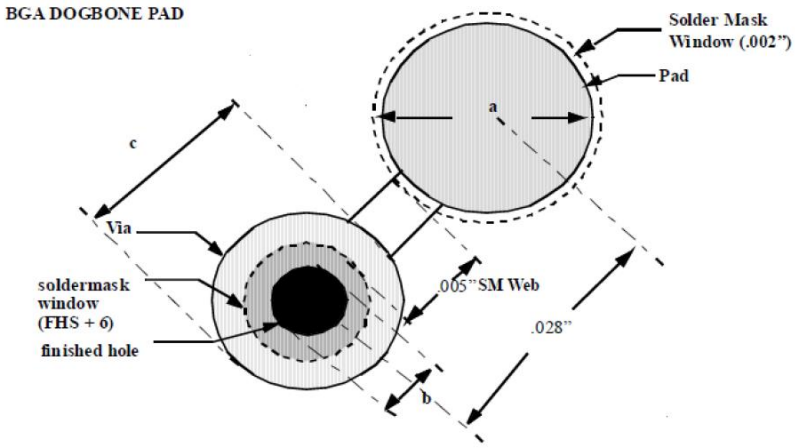


Figure 6.7. Dog-bone length limitation.

The previous study showed it is not realistic that implement the orthogonal layout without changing the chip package. There are different ways have been tried to relocate the BGA and satisfied the reliability, manufacturing when considering to keep the crosstalk cancellation advantages in the orthogonal layout. The fundamental problem preventing it from implementation is the pin offset of the unit cell, the location of two pairs of differential vias makes the pure dog-bone design that can relocate BGA can not pass the industrial manufacturing requirement. Since other orthogonal layouts have the same unit cells, the methods studied above are not applicable too.

6.2. IMPLEMENTATION OF THE ORTHOGONAL LAYOUT BY CHANGING THE CHIP PACKAGE

6.2.1. New Layout Conversion. In model 4, parallelly placed pairs have large crosstalk in between. Taking pair 1 and pair 2 as an example, there is a lot of crosstalk exist in between due to the short spacing. To avoid this, the placement direction of pairs on the right side can be reversed, pair 2, 4, 6, and 8 in model 4 can be reversed placed and model 6 can be developed. Figure 6.8 showed the transformation of model 6 from model 4. Theoretically, crosstalk between parallelly placed pairs can be reduced and the whole level of crosstalk inside model 6 can be less than it's in model 4.

Figure 6.9 showed ICN comparisons between model 4 and the new design model 6. As expected, model 6 has lower ICNs than model 4, ICNs of pair 1, 4, 5, and 8 reduced a lot, reversing of differential pairs placement decreases crosstalk between parallelly placed differential pairs. The conversion of model 6 still maintained the S:G as it is in model 4, spacing efficiency of these two models keeps the same.

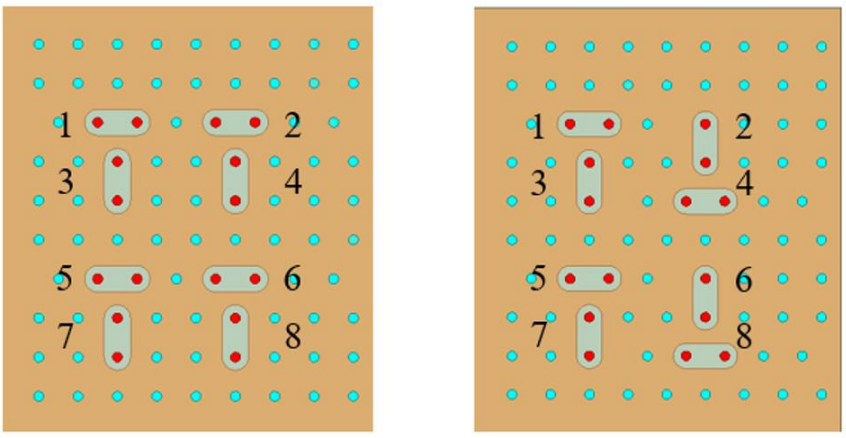


Figure 6.8. Model 6 conversion.

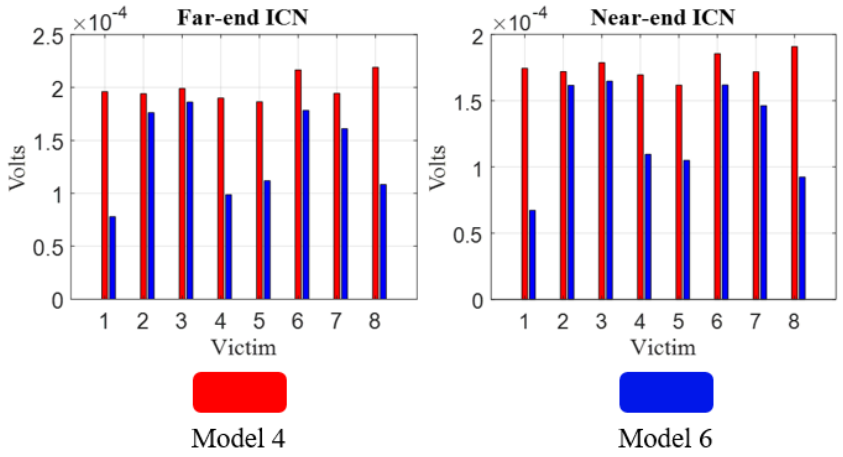


Figure 6.9. ICN validation of model 6.

It is worth to mention that the ground via placement in model 6 is critical for crosstalk cancellation. On the right side of Figure 6.10, it is the wrong via placement. Ground vias in the wrong via position disturb the crosstalk through disturbing the crosstalk of unit cells. Because of P/N in pair 1 have the different distance to ground vias, the coupling between P/N in pair 1 and P in pair 2 can not be balanced and it will significantly increase the crosstalk in the unit cell and will result in crosstalk increases of the full pin map. Figure 6.11 showed the ICN comparisons between the right and wrong via placement models. The wrong via placement model has much larger ICNs than the right one, it demonstrated us the critical of ground via placement to crosstalk in model 6 and this is the requirement to implement this the new layout.

6.2.2. Pure VIPPO Design for the Orthogonal Layout. There are 4 advanced orthogonal layouts developed in this research. Among all proposed models, model 6 has the lowest crosstalk inside. To explore the industrial implementation of the orthogonal

layout with changing the package, model 6 would be taken as an example of the pure VIPPO design validation for the orthogonal layout.

Theoretically, pure VIPPO design can maintain the crosstalk cancellation in the orthogonal layout. Introduced thin pads and solder balls maintain the same pin patterns and crosstalk cancellation in the pin field area can be retained.

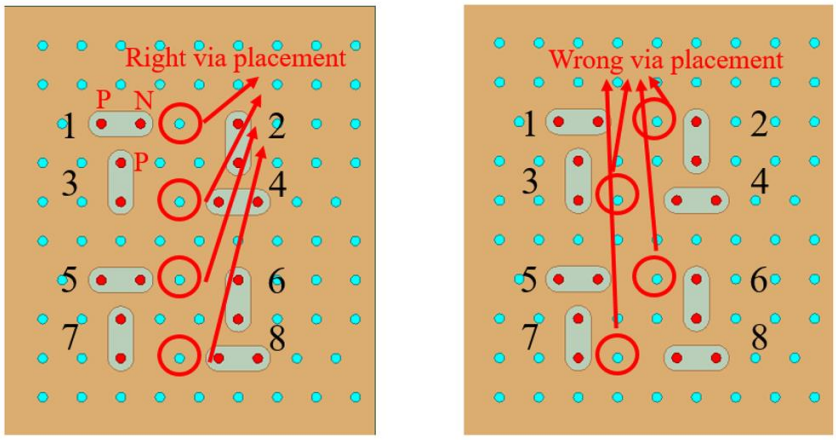


Figure 6.10. Ground via placement design for model 6.

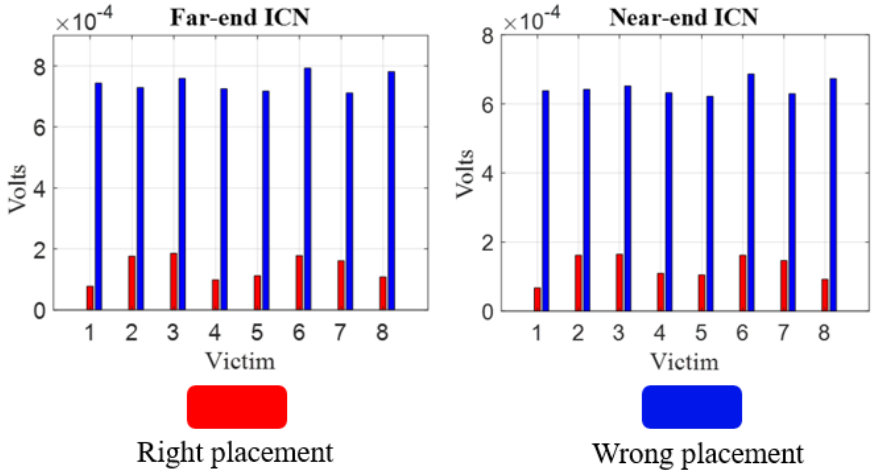


Figure 6.11. ICN evaluation of the ground via placement in model 6.

Figure 6.12 listed the VIPPO design for model 2 and model 6. Traces, pads, and solder balls all considered in the model and there are the structures just beneath the package. Such comparisons can validate the pure VIPPO design for the orthogonal layout and prove the industrial feasibility of the orthogonal layout.

Figure 6.13 showed the ICN comparisons between the conventional layout model 2 with pure VIPPO and the orthogonal layout model 6 with pure VIPPO. Model 6 with pure VIPPO design has much lower ICNs than model 2 with pure VIPPO design. Pure VIPPO design is the way for the orthogonal layout industrial implementation.

For the other 3 orthogonal layouts, pure VIPPO design can be the way for them for industrial implementation too. To realize the orthogonal layout in the industrial community, the chip package must be changed, and when the chip package can be changed, the pure VIPPO can be adopted as the schematic for orthogonal layouts implementation.

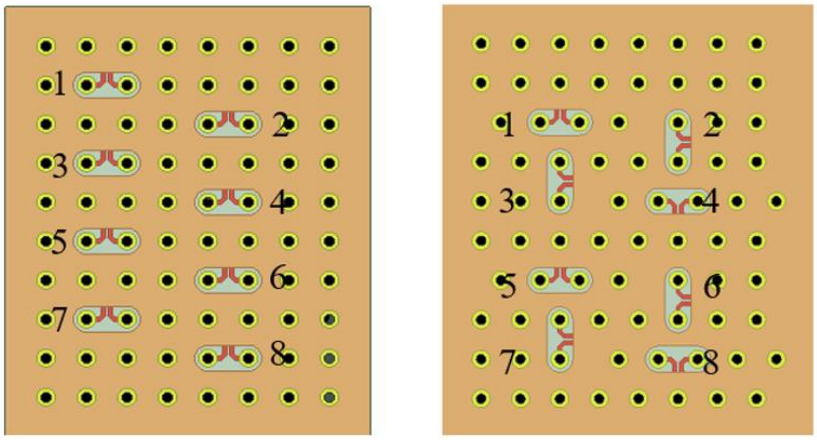


Figure 6.12. Pure VIPPO design for model 2 and model 6.

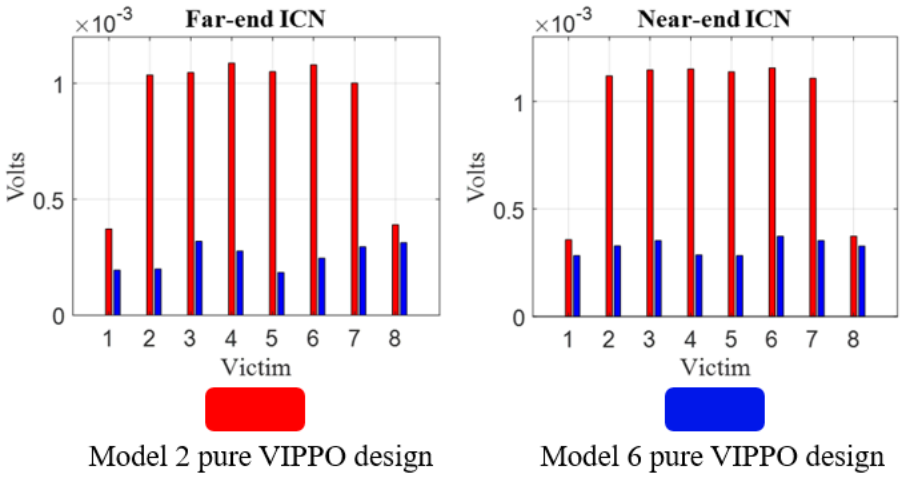


Figure 6.13. ICN validation of the pure VIPPO design for model 6.

7. CONCLUSION

During the research, there are 4 different advanced layouts proposed that have a large advantage on the crosstalk cancellation, also the industrial implementation of these layouts has been studied and the specific application scheme already been presented. The research is based on the symmetry principle of differential pairs in a unit cell, then full pin maps with different S:G ratio extended by the design of unit cells placement, the trace routing for unit pin maps has been studied and the advanced trace routing applied on differential pin maps and also the crosstalk of the advanced pin maps with trace routing models are verified. For the orthogonal layout industrial implementation research, implementation without changing the chip package is firstly researched because of its low expense, then implementation by changing the chip package is studied and the specific realization scheme is presented.

ICN has been introduced to be the crosstalk assessment index during the research, it can present crosstalk more intuitional and precise. Before the crosstalk evaluation of the proposed layouts, TDR, insertion loss, and return loss of differential pairs in all orthogonal models are control at the same level as there are in the conventional model to avoid crosstalk level effect by other variables and ensure crosstalk reduction won’t affect other signal integrity performances.

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