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Channel Mobility and Contact Resistance in Scaled ZnO Thin-Film Transistors

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ABSTRACT

ZnO thin-film transistors (TFTs) with scaled channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm exhibit increasing intrinsic channel electron mobility at a gate bias of 10 V (15 V) from 0.782 cm^2/Vs (0.83 cm^2/Vs) in the 10 μm channel length TFT to 8.9 cm^2/Vs (19.04 cm^2/Vs) for the channel length scaled down to 2 μm. Current-voltage measurements indicate an *n*-type channel enhancement mode transistor operation, with threshold voltages in the range of 8.4 V to 5.3 V, maximum drain currents of 41 μA/μm, 96 μA/μm, 193 μA/μm, and 214 μA/μm at a gate bias of 10 V, and breakdown voltages of 80 V, 70 V, 62 V, and 59 V with respect to channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm. The channel electron mobility (excluding contact resistance) is extracted by the transmission line method (TLM) from the effective electron mobility (including contact resistance). The contact sheet resistance of 4.6×10^5 Ω/sq extracted from the measurements, which is 3.5× larger than the contact sheet resistance of 1.3×10^5 Ω/sq obtained from the DFT calculation and the 1D self-consistent Poisson-Shrödinger simulation, largely limits the drive current in the scaled ZnO TFTs.

1. Introduction

ZnO is intensively studied as an alternative channel material for semiconductor TFTs due to its distinctive material properties having a direct wide band gap of 3.37 eV [1], an electron mobility in the range of 1-100 cm^2/Vs at room temperature, and a relatively large breakdown voltage in the range between 50 V-75 V [2]. The most appealing advantages of ZnO are low cost fabrication, low thermal resistance, low temperature processing, high resistance to radiation damage, piezoelectricity, and technological compatibility with Si [3]. Lately, ZnO was considered as a promising semiconductor material for complementary metal oxide semiconductor (CMOS) technology [4] and integrated circuits [5]. However, many challenges remain that hold back the actual implementation of this promising material. One of the major challenges is a low effective (including contact resistance) electron mobility as well as a low channel (excluding contact resistance) electron mobility in TFTs [5, 6]. Currently, there is no full comprehension of the physical mechanisms behind a relatively low electron mobility despite a known presence of high density of interface traps [7, 8].

In this paper, we study electrical characteristics of ZnO TFTs with scaled channel lengths (10 μm, 5 μm, 4 μm, and 2 μm) fabricated by a top-down approach, the remote plasma atomic layer deposition (ALD) [4]. Our ZnO TFTs exhibit an *n*-channel enhancement mode operation with a large drain current saturation in the range of 5–25 μA/μm. The set of scaled channel lengths allows us to extract a contact resistance, and effective (which includes an external resistance) and channel (which excludes an external resistance) electron mobility as a function of the gate voltage. The extracted intrinsic channel mobility is a better representative of device performance because a typically reported low electron mobility in ZnO TFTs using transconductance method [6] is due to a large contact resistance. Our study investigates the impact of the scaled channel length at two gate voltages on significant device parameters such as threshold voltage (V_{Th}), drain induced barrier lowering (DIBL), sub-threshold swing (SS), on-current (I_{On}), leakage current (I_{Off}), on/off ratio, contact resistance, and effective and channel electron mobility. Finally, physically based simulations using a new approach combining density functional theory (DFT) calculations with quantum transport simulations at the interface between metal and semiconductor predict a theoretical limit of the contact sheet resistance.

2. ZnO Thin-Film Transistors Fabrication Process

The ZnO TFTs are fabricated on a *p*-type silicon wafer acting as a back-gate as shown in Fig. 1(a). A 100 nm SiO_2 layer is grown by dry thermal oxidation as a gate insulator. ZnO is deposited at 190°C using remote plasma ALD by Oxford Instrument Plasma Technology (OIPT) Flex Al system with diethyl zinc as a precursor with a RF power of 100 W, a pressure of 80 mTorr, and an O_2 flow of 60 sccm as shown in Fig. 1(b). The advantage of using the remote plasma ALD technique compared to water-based oxidation [4] is the reduction of OH impurities which can increase film resistivity [4]. The ZnO thin film is defined by photo-lithography

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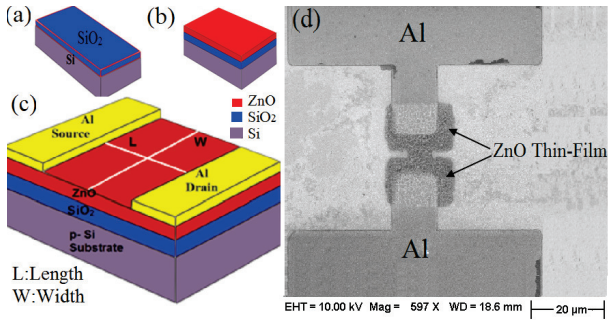

Figure 1: Top-down fabrication process of ZnO TFTs: (a) SiO_2 thermally grown through a dry oxidation with a thickness of 100 nm, (b) ZnO thin film deposited in the remote plasma ALD technique, (c) a 3D schematic structure of the fabricated ZnO TFT, (d) the SEM image of the ZnO TFT with Al pads which serve as contacts.

and anisotropic inductive coupled plasma (ICP) etching based on CHF_3 gas chemistry. Finally, a 500 nm thick Al metal electrode is deposited by an electron beam evaporation and lift-off as top source and drain contacts [4]. A scanning electron microscope (SEM) image of the fabricated device is shown in Fig. 1(d).

3. Device Characteristics and Mobility

Fig. 2 shows output (I_D-V_D) characteristics of ZnO TFTs with different channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm measured at room temperature. The devices exhibit an n-type operation mode in the range of V_D = 0-20 V [9]. The output characteristics show a well-distinguished linear region at a low drain bias and a saturation region at a high drain bias [10]. At the high gate bias (V_G = 10 V), the maximum drain current (I_D) increases proportionally to the decrease in a channel length (L_{ch}) from 10 μm to 2 μm. The maximum drain currents for 10 μm, 5 μm, 4 μm, and 2 μm are 40.5 μA/μm, 96.0μA/μm, 192.9 μA/μm, and 214.4 μA/μm, respectively, when the currents are normalised by a device width (W = 10 μm). As the source/drain voltage increases, the channel/drain depletion region shifts to the source side and electrons in the channel are quickly drifted to the drain. When the channel length of the ZnO TFTs is scaled down by decreasing the distance between the source and the drain, the electric field along the channel increases leading to an increase in acceleration of electrons by the electric field in the channel. Consequently, the injection of electrons from the source into the channel becomes a more efficient due to the same increase in electric field since the electrons gain a larger kinetic energy to overcome Schottky barrier height between the metal and the semiconductor by thermionic transport and tunnelling. This increase in the electron velocity accompanied by an increase in electron density in the channel, due to the more efficient electron injection from the contacts, increases the maximum drain current [9].

To study the impact of the channel length scaling on device performance, Fig. 3 illustrates the transfer characteristics (I_D-V_G) at a fixed drain bias of 5 V for different channel

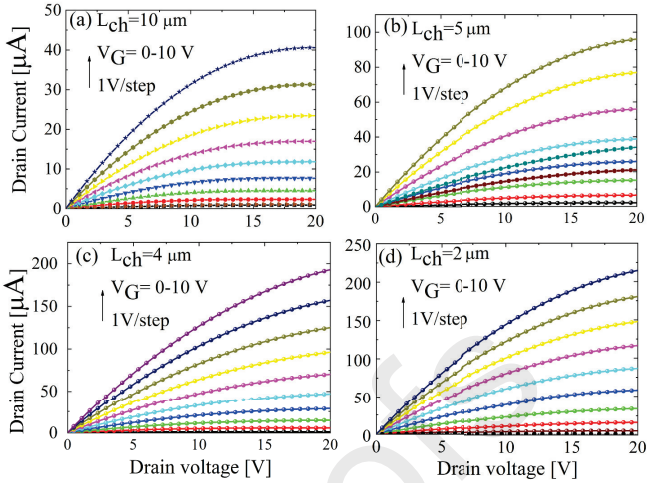

Figure 2: Output I_D-V_D characteristics from V_G = 0 V to 10 V with a step of 1 V for ZnO TFTs with different channel lengths (L_{ch}) of (a) 10 μm, (b) 5 μm, (c) 4 μm, and (d) 2 μm.

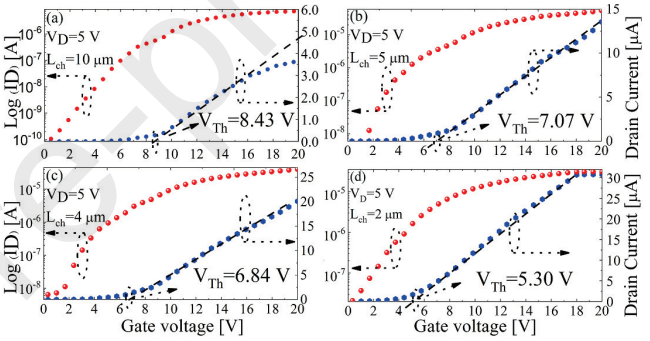

Figure 3: Transfer I_D-V_G characteristics under a fixed drain bias of 5 V for (a) 10 μm, (b) 5 μm, (c) 4 μm, and (d) 2 μm channel length ZnO TFTs. The width of the all TFTs is 10 μm.

lengths of L_{ch} = 10 μm, 5 μm, 4 μm, and 2 μm. The sub-threshold region exhibits approximately a linear behaviour of the drain current on logarithmic scale which indicates well behaved transistor characteristics with a small leakage current. Transistors with channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm have sub-threshold slopes of 1.67 V/dec, 0.75 V/dec, 0.57 V/dec, and 0.41 V/dec, respectively. These sub-threshold slopes are relatively large when compared to the ideal slope of Si MOSFET of 60 mV/dec at room temperature but will provide a relatively low leakage current and a good on/off ratio in low-power applications (with respect to the on-current and the breakdown voltage). The decrease in the sub-threshold slope follows the decrease in the channel length [9]. In the sub-threshold region, drain current (I_D) is dominated by a diffusion transport of carriers and is inversely proportional to L_{ch} [9]. To evaluate a performance of the scaled ZnO TFTs in circuits, the I_{On}/I_{Off} ratio is extracted by comparing the maximum drain current (I_{On}) as a function of the gate voltage (V_G) against the drain current (I_{Off}) at the gate voltage equal to zero (all the TFTs are enhancement mode). The I_{On}/I_{Off} ratios are 1.5 $\times 10^4$, 4.2 $\times 10^4$, 5.3 $\times 10^4$, and 8.3 $\times 10^4$ for channel lengths of

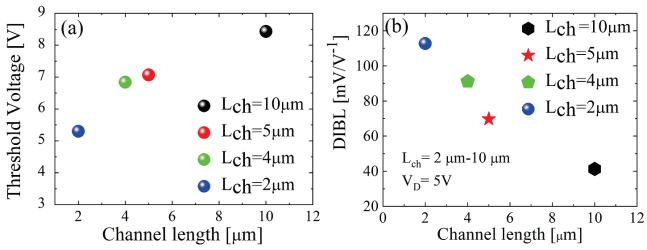

Figure 4: (a) Variation of threshold voltage (V_{Th}) as a function of the channel length. (b) The drain induced barrier lowering (DIBL) of ZnO TFTs versus the channel length of $L_{ch} = 10$ μm, 5 μm, 4 μm, and 2 μm.

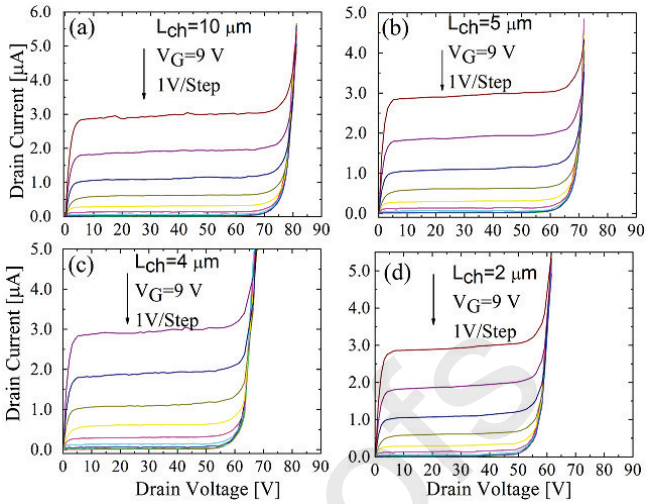

Figure 5: Output I_D-V_D characteristic of a ZnO TFTs with a channel length of $L_{ch} = 10$ μm, 5 μm, 4 μm, and 2 μm at fixed gate voltages starting from $V_G = 9$ V exhibiting a breakdown voltage of 79.91 V, 70.07 V, 64.68 V, and 58.85 V.

$L_{ch} = 10$ μm, 5 μm, 4 μm, and 2 μm, respectively, which provides solid on/off ratios for switching in digital and analogue low-power applications. The I_{On}/I_{Off} ratio decreases with the channel length decrease also because the threshold voltage shifts toward larger positive values [10]. Fig. 4(a) shows an extracted threshold voltage (V_{Th}) versus the channel length. The threshold voltage for the 10 μm and the 5 μm channel length ZnO TFTs are 8.43 V and 7.07 V, respectively. When the channel length decreases further to 4 μm and 2 μm, the threshold voltage decreases to 6.84 V and to 5.30 V, respectively. The decrease in the threshold voltage with a decrease in the channel length is caused by the increase in electron density in the channel. Thus, it becomes easier to create an accumulation channel for a given gate bias [11]. When the long channel length (10 μm) transistor is compared to the short channel length (2 μm) transistor, the threshold voltage decreases by 37 %.

The Schottky barrier height in the transistor channel is controlled by both the gate-to-source voltage (V_G) and the drain-to-source voltage (V_D). If the drain voltage is increased, the potential barrier in the channel decreases, leading to a drain-induced barrier lowering (DIBL).

The DIBL is determined using a transistor theory from the physics of semiconductor devices by the relation [10]:

$$\mathrm{DIBL} = \frac{V_{\mathrm{Th}}^{\mathrm{DD}} - V_{\mathrm{Th}}^{\mathrm{Low}}}{V_{\mathrm{DD}} - V_{\mathrm{D}}^{\mathrm{Low}}} \quad (1)$$

where $V_{\mathrm{Th}}^{\mathrm{DD}}$ is the threshold voltage measured at a supply voltage V_{DD}, and $V_{\mathrm{Th}}^{\mathrm{Low}}$ is the threshold voltage measured at a low drain voltage $V_{\mathrm{D}}^{\mathrm{Low}}$.

The experimental results for the DIBL versus channel lengths (L_{ch}) for 10 μm, 5 μm, 4 μm, and 2 μm of ZnO TFTs are plotted in Fig. 4(b). As the channel becomes shorter, the DIBL becomes more pronounced. By decreasing the channel length, the space charge at the drain will interact with that at the source which leads to a potential barrier lowering in a space between the source and the channel [11].

Finally, a breakdown voltage has been measured in carefully designed experiments to protect device functionality from unexpected burn out due to undue large applied bias [4]. In practice, the drain bias is increased in small steps until the drain current starts to quickly increase. This exponential-like increase in the drain current [13] results from the impact ionisation process taking place where the largest electric field occurs, typically close to the drain contact. The impact ionisation causes a very large generation of electrons in a chain-like reaction leading ultimately to the device breakdown. The results from the investigation of breakdown voltage are shown in Fig. 5. Devices with channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm have exhibited breakdown voltages of 79.91 V, 70.07 V, 61.68 V, and 58.85 V, respectively. These are relatively high breakdown voltages which are very promising for circuit applications with high drive voltage requirements such as a display panel and a diode [4].

The total resistance, R_{Tot}, has been extracted from the linear region of I_D-V_D characteristics for different channel lengths (L_{ch}) of 10 μm, 5 μm, 4 μm and 2 μm at two gate biases (10 V and 15 V). In order to normalise the total resistance, the value of R_{Tot} is multiplied by a device width ($W = 10$ μm) to obtain a value in $\Omega.\mathrm{cm}^2$. Fig. 6(a) shows the normalised total resistance for all transistors for the 10 μm, 5 μm, 4 μm, and 2 μm channel lengths at two gate biases of 10 V and 15 V which will be used in the transmission line method (TLM) [12] to extract carrier mobility. The normalised total on-resistance is found to be decreasing from 0.3659 $\Omega.\mathrm{cm}^2$ at $V_G = 10$ V to almost 0.297 $\Omega.\mathrm{cm}^2$ when compared to the one measured at $V_G = 15$ V. The normalised total resistance for the 10 μm channel length ZnO TFT is three times larger than the total resistance resistance for the 2 μm channel length device (the normalised total resistance becomes proportional to the channel length). When electric field increases in the channel region as the result of scaling down the source-to-drain distance or as the result of increase in the drain bias, electrons in the channel will gain a large kinetic energy. These electrons with a large kinetic energy will overcome Schottky barrier between metal and semiconductor by thermionic transport and tunnelling more efficiently

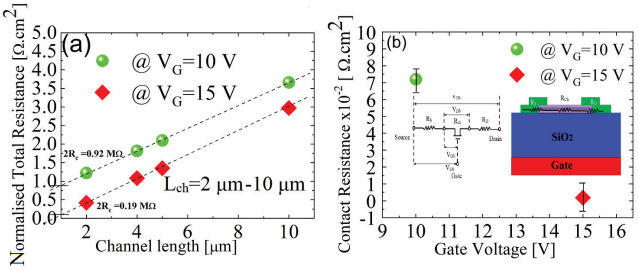

Figure 6: (a) Total and (b) contact resistances versus the gate voltage at two different gate biases (V_G = 10 V and 15 V). The inset schematics show a diagram of resistances by the contacts and the channel in the ZnO TFTs (left) and the resistances set over the device structure (right).

thus lowering access resistance [9, 14]. The lower access resistance leads to more electrons to contribute to the channel transport, increasing electron density in the channel.

The total resistance, R_{Tot}, can be expressed linearly with dependence on the channel length. The contact resistance R_{C} can be calculated using results from the TLM assuming that the normalised total resistance is independent of the potential drop across contacts at the source and the drain [14] and its change is only proportional to the channel length. Contact resistance per channel length presented in Fig. 6(b) is extracted from the slope of the drain current versus the drain voltage (I_{D}-V_{D}) at two different gate voltages (10 V and 15 V). The contact resistance is 7.2 $\times 10^{-2}$ Ω.cm^2 at a gate voltage of 10 V. When the gate voltage is increased to 15 V, the contact resistance reduces to 0.177 $\times 10^{-2}$ Ω.cm^2, a decrease of 106.78 %. When the gate voltage increases from 10 V to 15 V, injection of charge becomes a more efficient thanks to increased kinetic energy of electrons contribute into carrier transport along the channel [15, 16] as described before.

The effective mobility, μ_{eff}, is determined from the linear regime using the conventional equation for MOSFETs in the approximation when $V_{\text{D}} \ll (V_{\text{G}} - V_{\text{Th}})$ [9]:

$$I_D = \mu_{\text{eff}} C_{\text{Tot}} \frac{W}{L} \left[(V_{\text{G}} - V_{\text{Th}}) V_{\text{D}} - \frac{V_{\text{D}}^2}{2} \right] \tag{2}$$

Eq. (2) can be simplified in a linear region by neglecting a quadratic term as:

$$I_D = \mu_{\text{eff}} C_{\text{Tot}} \frac{W}{L} (V_{\text{G}} - V_{\text{Th}}) V_D \tag{3}$$

and then re-written as:

$$\mu_{\text{eff}} = \frac{I_{\text{D}}}{V_{\text{D}}} \frac{L}{W C_{\text{Tot}}} \frac{1}{(V_{\text{G}} - V_{\text{Th}})} \tag{4}$$

or:

$$\mu_{\text{eff}} = \frac{1}{R_{\text{Tot}}} \frac{L}{W C_{\text{Tot}} (V_{\text{G}} - V_{\text{Th}})} \tag{5}$$

where $R_{\text{Tot}} = \frac{V_{\text{D}}}{I_{\text{D}}}$ is the slope, W is the width of the device, L is the channel length, and C_{Tot} is the total gate capacitance per area. The total gate capacitance consists of two capacitances in series, the SiO_2 capacitance, C_{ox}, and the capacitance of the p-type Si substrate, C_{Si}. Therefore, the total gate capacitance for the device can be described as:

$$\frac{1}{C_{\text{Tot}}} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{Si}}} \tag{6}$$

where

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}} \epsilon_0}{t_{\text{ox}}} \quad \text{and} \quad C_{\text{Si}} = \frac{\epsilon_{\text{Si}} \epsilon_0}{t_{\text{Si}}} \tag{7}$$

where A is the area of the bottom gate, ϵ_r (r = Si, ox) is the relative static permittivity (also called the dielectric constant) of the material (for a vacuum, $\epsilon_r = 1$), ϵ_0 is the permittivity of vacuum, t_{Si} is the thickness of Si substrate and t_{ox} is the oxide thickness.

The effective electron mobility extracted at two different gate biases (10 V and 15 V) is plotted in Fig. 7(a) for 10 μm, 5 μm, 4 μm, and 2 μm channel length TFTs. The mobility increases with a decrease in the channel length at both gate biases of V_{G}=10 V and 15 V. When a gate bias increases from 10 V to 15 V, the effective electron mobility increases from 0.11 cm^2/Vs to 0.38 cm^2/Vs (about 71.05 %) for the 10 μm channel length TFTs as well as increases from 1.28 cm^2/Vs to 2.86 cm^2/Vs (about 55.24 %) for the 5 μm channel length, from 1.77 cm^2/Vs to 3.25 cm^2/Vs (about 45.54 %) for the 4 μm channel length, and from 2.9 to 4.04 cm^2/Vs (about 28.22 %) for the 2 μm channel length TFTs.

The channel electron mobility is obtained using the conventional MOSFET equation for channel mobility [9]. The total resistance has two contributions from the contact resistance and the channel resistance as [9]:

$$R_{\text{Tot}} = R_{\text{C}} + R_{\text{ch}} = R_{\text{C}} + \frac{L}{W C_{\text{Tot}} \mu_{\text{ch}}} \frac{1}{(V_{\text{G}} - V_{\text{Th}})} \tag{8}$$

where the channel resistance R_{Tot} in Eq. (5) is replaced by the channel resistance R_{ch} and the effective electron mobility μ_{eff} is replaced by the channel electron mobility μ_{ch}. Since the contact resistance can be determined at a channel length of zero ($L = 0$) as plotted in Fig. 6(b), the channel electron mobility (μ_{ch}) can be expressed by re-arranging Eq. (8) as:

$$\mu_{\text{ch}} = \frac{L}{W} \frac{1}{Q_{\text{inv}} (R_{\text{Tot}} - R_{\text{C}})} \tag{9}$$

where Q_{inv} is the inverse charge in the channel region. When $V_{\text{G}} \gg V_{\text{Th}}$, the inverse charge is given by:

$$Q_{\text{inv}} = C_{\text{Tot}} (V_{\text{G}} - V_{\text{Th}}). \tag{10}$$

Fig. 7(b) shows that the extracted channel electron mobility of ZnO TFTs, which is also summarised in Table 1, increases with the decreasing of the channel length. The channel mobility also increases when comparing values at gate biases of 10 V and 15 V. The channel mobility will increase from 0.782 cm^2/Vs to 0.83 cm^2/Vs by about 6 % in the 10 μm channel length TFT, from 8.28 cm^2/Vs to 9.86 cm^2/Vs in the 5 μm channel length TFT by about 16 %, from 8.30 cm^2/Vs to 10.25 cm^2/Vs (about 13 %) in the 4 μm channel length

Table 1
Effective and channel electron mobility extracted using Eq. (9) at two different gate biases of V_G=10 V and 15 V.

L_{ch}	10μm	5μm	4μm	2μm
μ_{eff} @ V_G=10 V (cm^2/Vs)	0.11	1.28	1.77	2.9
μ_{eff} @ V_G=15 V (cm^2/Vs)	0.38	2.86	3.25	4.04
μ_{ch} @ V_G=10 V (cm^2/Vs)	0.78	8.28	8.30	8.9
μ_{ch} @ V_G=15 V (cm^2/Vs)	0.83	9.86	10.25	19.04

TFT, and from 8.9 cm^2/Vs to 19.04 cm^2/Vs (around 53 %) in the 2 μm channel length transistor. The increase of the channel electron mobility during the channel scaling is indicative of a less frequent scattering due to the increase in kinetic energy of electrons resulting from the increase in electric field along the channel [8, 17]. Overall, this channel electron mobility in the ZnO TFTs is improved or equal to the previously reported values of a field-effect electron mobility for such devices [21, 22, 23, 24, 25]. Our intrinsic channel electron mobility, especially in the smallest 2 μm gate length TFT, compares favourably with the typically reported field-effect carrier mobility which frequently overestimates the intrinsic channel carrier mobility because the field-effect carrier mobility is extracted at a high electric field [26].

Since electron scattering occurs close to the conduction band edge, the increase in the applied bias (from 10 V to 15 V) will result in the increased kinetic energy of electrons which will be able to move effectively along the channel. Therefore, the channel electron mobility observed in the 2 μm channel length TFT at 15 V is more than one time larger than the mobility at 10 V. This relatively large electron mobility can be further increased by a surface passivation which can mitigate a large density of traps at the surface of ZnO TFTs. The increase in kinetic energy of electrons also leads to a more efficient de-trapping of electrons from surface traps [8]. The electrons trapped at a surface act as scattering centres that interact with the flow of mobile carriers in the channel due to remote Coulomb scattering.

4. DFT Calculations of ZnO Electron Effective Mass and Density of States

Density functional theory (DFT) is used to calculate electron band structure of hexagonal ZnO using a software package QuantumATK by Synopsys [27]. In the calculations, lattice constants are set to a = 3.249 Å and c = 5.207 Å. The meta generalised gradient approximation (MGGA) [28] is selected to obtain a material band gap instead of a more common generalised gradient approximation (GGA). The band gap between the maximum of the valence band (the green line in Fig. 8(a)) and the minimum of the conduction band

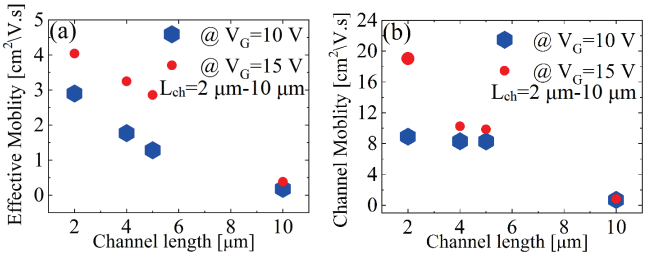

Figure 7: Effective (a) and channel (b) electron mobility extracted using the TLM versus the channel length at two different gate biases of V_G = 10 V and 15 V. The channel mobility excludes a contact resistance.

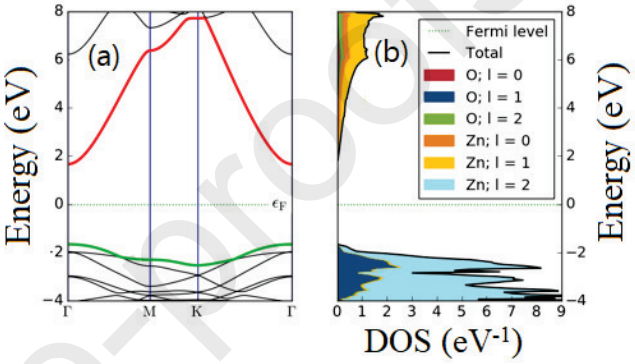

Figure 8: (a) A band gap structure of ZnO with indicated minimum of the conduction band (red line) and maximum of the valence band (green line). (b) The density of states (DoS) obtained from the DFT calculations. Fermi level (ϵ_F) is set at zero energy.

(the red line in Fig. 8(a)) is calculated to be 3.32 eV, which is close to the experimental value of 3.37 eV [1]. The density of states (DoS) is shown in Fig. 8(b), where angular quantum numbers $0, 1, 2$ correspond to s, p, d orbitals, respectively. Effective electron mass at the Γ point is calculated to be 0.25 m$_0$ using a hybrid functional, where m$_0$ is the free electron mass. This extracted effective electron mass in ZnO will be used in the next section to calculate a sheet resistance of the Al contact to the ZnO thin film as schematically shown in Fig. 9(a).

5. 1D Transport Simulation of the ZnO Source-Drain Contact

The sheet resistance of the Al contact to the ZnO thin film is schematically illustrated in Fig. 9(a). Carrier transport through the structure is simulated using self-consistently coupled 1D Poisson-Shrödinger equations (PS) [29]. The layer structure considered in the simulations is chosen to match the size and the composition of the experimental structure [4]. The thicknesses of the layers, depicted in Fig. 9(a), are collected together with doping concentration, energy band gap, conduction band offset, mobility, effective electron mass, and permittivity of the materials in Table 2. Fig. 9(b) shows the conduction and valence bands, and Fermi level from the

Table 2
ZnO, SiO_2 and Si material parameters: layer thickness, *n*-type doping, band gaps, conduction band offset, electron mobility, effective electron mass, (m_0 is the electron mass in vacuum), and relative material permittivity used in the modelling of the source/drain contact.

Material	Thickness [nm]	*n*-type doping [cm^3]	E_G [eV]	ΔE_C [eV]	μ [cm^2/Vs]	m_e [× m_0]	ε_r [%]
ZnO	80	1×10^{17}	3.37	0.25	50	0.25	8.5
SiO_2	100	1×10^{16}	8.9	0.75	2500	0.33	8.0
Si	625,000	1×10^{16}	1.12	0.35	450	0.17	11.9

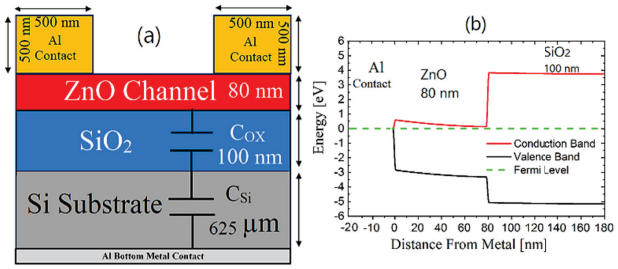

Figure 9: (a) Cross-section of Al/ZnO/SiO_2/Si layer structure for the ZnO TFTs indicating thicknesses of the layers. (b) Conduction and valence band profiles of the reduced Al/ZnO/SiO_2 layer structure at equilibrium as considered in the simulations of sheet resistance of the Al contact. The interface between the Al contact and the 80 nm ZnO layer is located at zero.

solution of 1D PS equations, of the reduced Al/ZnO/SiO_2 layer structure at equilibrium because the *p*-type Si substrate below the 100 nm SiO_2 layer has a negligible contribution to the overall sheet resistance of the source/drain. We assume a metal work function of Al (4.28 eV) and calculate Schottky barrier height (SBH) as the potential difference between the metal work function and the electron affinity [30]. The effective electron mass is extracted from the DFT calculations shown in Fig. 8(a).

The 1D PS simulations assume that the contact sheet resistance of the ZnO TFTs is determined by electron transport through the top source and drain contacts into the ZnO thin film channel. Therefore, only the Al/ZnO layer structure is considered in the simulations of a sheet source/drain contact resistance. The calculated contact sheet resistance is 1.286×10^5 Ω/sq. This value is smaller (3.5× smaller) than the contact sheet resistance of 4.6×10^5 Ω/sq obtained from experimental measurements by the TLM. The simulated smaller sheet resistance is the result of assumption of ideal Schottky contact which neglects any traps or voids at the metal-semiconductor interface. However, the simulated sheet resistance is still in a close order of magnitude of the measured one.

6. Conclusions

ZnO TFTs have been fabricated by a top-down approach using the remote plasma ALD technique with different channel lengths (2 μm, 4 μm, 5 μm, and 10 μm). Current-voltage measurements have demonstrated an *n*-type channel enhancement mode transistor operation, with threshold voltages in the range of 8.4 V to 5.3 V, the maximum drain currents of 41 μA/μm, 96 μA/μm, 193 μA/μm, and 214 μA/μm at $V_G = 10$ V and breakdown voltages of 80 V, 70 V, 62 V, and 59 V with respect to channel lengths of 10 μm, 5 μm, 4 μm, and 2 μm, respectively. We have also observed a decrease in the sub-threshold slope from 1.67 V/dec to 0.75 V/dec, 0.57 V/dec, and 0.41 V/dec with channel lengths of 10 μm to 5 μm, 4 μm, and 2 μm, respectively.

The total contact resistance has decreased with increasing of a gate voltage from 10 V to 15 V. The effective electron mobility (μ_{eff}) has increased with the scaling of the source-to-drain distance. The channel electron mobility (μ_{ch}) increased from 0.78 cm^2/Vs to 8.28 cm^2/Vs, 8.30 cm^2/Vs, and 8.9 cm^2/Vs at $V_G = 10$ V (from 0.83 cm^2/Vs to 9.86 cm^2/Vs, 10.25 cm^2/Vs, and 19.04 cm^2/Vs at $V_G = 15$ V) with the decrease in a channel length from 10 μm to 5 μm, 4 μm, and 2 μm, respectively. The increase in the effective mobility causes also an increase in I_{On}. The I_{On} in the ZnO TFT with a channel length of 2 μm is larger by 82 % than the I_{On} in the TFT with a channel length of 10 μm because of a larger channel electron mobility.

Finally, we have also calculated a contact sheet resistance using 1D self-consistent PS simulations. The electron effective mass in these PS simulations has been extracted from the ZnO band structure obtained from DFT calculations. The contact sheet resistance from the simulations is 1.286×10^5 Ω/sq which is smaller than the sheet resistance of 4.6×10^5 Ω/sq obtained experimentally by the TLM measurements. This suggests that a lowering of the source/drain contact resistance would bring a large benefit [31] into an increase in the drain current of the ZnO TFTs.

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