Suppression of Surface Leakage Currents in InAs Avalanche Photodiodes via Sputtering of High-k Dielectric Layers

Zhongming Cao, Ivona Z. Mitrovic (Senior Member IEEE), and Ian Sandall (Member IEEE)

***Abstract*— The effectiveness of a range of alternative high-k dielectric layers as potential passivation layers for InAs avalanche photodiodes has been investigated. The suppression of surface leakage currents is investigated by analysing the current-voltage performance of differently sized mesa diodes passivated with each oxide layer. Three potential passivation layers, ZnO, Al_2O_3 and MgO, have been identified, all of which enables suppression of surface leakage in smaller sized devices of a radius of 50 μm and at lower temperatures of 175 K compared to a reference SU8 device. The influence of repeated temperature cycling on these layers has also been investigated with Al_2O_3 passivated devices, exhibiting no change in performance after multiple cooling and heating cycles.**

***Index Terms*— high-k dielectric, InAs, avalanche photodiodes, leakage currents.**

I. Introduction

The ability to detect mid-infrared light efficiently is increasingly important for a range of applications, such as communications, security, medicine and metrology [1-4]. Conventional semiconductor photodiodes have limited sensitivity, especially in photon-starved and high-speed applications such as free-space optical communication and remote sensing. In these applications, avalanche photodiodes (APDs) are often the preferred optical detectors, due to their internal gain mechanisms.

Currently, most applications operating in this wavelength region utilize Cadmium Mercury Telluride (CMT) [5, 6]. However, CMT is an expensive and difficult semiconductor to grow and fabricate, limiting both the price and quantity of devices that are available. Other semiconductor based materials, which have successfully demonstrated as photodetectors operating in the wavelength of 2 – 3 μm range, include GaAsSb/InGaAs Type-II superlattices [7, 8]. Photodiodes utilizing the bulk semiconductor InGaAsSb have also been realized over this wavelength range [9, 10]. However, the growth and fabrication of this material are still at a very early stage.

Over recent years, InAs has been demonstrated to operate as an excellent APD over this spectral range with single carrier multiplication and low excess noise [11, 12]. This has more recently led to the demonstration of a linear array of InAs APDs [13], as well as single diodes demonstrating room temperature gains in excess of 100 [14] and APDs capable of detecting down to near single photon levels [7].

However, despite these achievements, the commercial uptake and development of InAs based APDs have not yet occurred. One of the primary reasons for this is that the surface passivation of these devices is a non-trivial matter. Mesa etched diodes, fabricated from narrow bandgap semiconductors are particularly susceptible to surface leakage currents. For InAs it has been reported that the etched surface of InAs results in electron accumulation which leads to the fermi level being pinned above the conduction band minimum and providing an efficient conduction path [15, 16]. In other compound semiconductor systems (for example GaAs and InGaAs) surface passivation techniques to block parasitic current paths, are typically realized by depositing a layer of dielectric such as silicon nitride over the semiconductor surface [17, 18]. However, such techniques have proved unsuccessful when applied to InAs, most likely due to the small bandgap and the

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The authors are with the Department of Electrical Engineering and Electronics, University of Liverpool, Brownlow Hill, Liverpool L69 3GJ, U.K. (zmc506@liverpool.ac.uk; Ivona@liverpool.ac.uk; Ian.Sandall@liverpool.ac.uk).

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relatively high deposition temperatures required to achieve a high-quality dielectric layer.

This has led to polymer-based dielectrics being utilized in the best performing InAs devices reported to date. However, these polymers are highly sensitive to their deposition conditions (temperature, relative moisture), making repeatable and reliable manufacture difficult, these layers can also degrade over time. A further disadvantage of making use of these polymer layers is that while they supress surface leakage currents at room temperature in moderate sized diodes (i.e. mesa's with diameters > 100 μm), surface-based currents remain present at low temperatures and in smaller devices [19], limiting the potential size of pixel elements in array-based systems. A final issue with such passivation layers is that they can be difficult to obtain good adhesion for electrical bond pads.

A potential alternative passivation route may be to utilize so-called 'high-k' dielectrics to act as the surface passivation layer. This class of dielectrics possess a high dielectric constant, which could provide much greater surface passivation, particularly on narrow bandgap materials. Possible dielectrics such as aluminium oxide (Al_2O_3) and hafnium oxide (HfO_2) are now utilized in the production of CMOS circuits and as such are a well-characterized and understood class of materials [20, 21]. They can also be deposited using a low temperature and high throughput techniques such as atomic layer deposition (ALD) and radio frequency (RF) sputtering. A recent example [22] investigated the passivation of surface contamination on InAs(100) by removing the native oxide using annealing in ultra-high vacuum (UHV) under a flux of atomic hydrogen and growing a stoichiometrically controlled oxide (thermal oxide) in UHV, prior to ALD of an Al_2O_3 high-k layer. Capacitance-voltage measurements confirmed a reduction of the interface trap density compared with an untreated sample, however such work is yet to progress beyond analysing the material interface layer into device applications.

These high-k dielectrics and in particular Al_2O_3 have been investigated in recent years for the potential suppression of leakage currents in various III-V semiconductor-based devices [23-27]. For example, He *et al.*[27] have investigated the effect of Al_2O_3 passivation layer on the interface electrical properties of MOS capacitors fabricated using HfTiO as the dielectric on InGaAs, resulting in low leakage current of 1.17 x 10^{-5} A/cm^2 at an applied gate voltage of 1 V. There have also been a handful of studies on utilizing these passivation layers on other narrow bandgap photodetectors, such as Type-II superlattices [28, 29], however to date, there are no reports of high-k based dielectrics being used in the passivation of InAs photodetectors. In this paper, we present a systematic investigation of the use of sputtering different dielectric layers as potential passivation layers for InAs APDs. By utilizing the same device structure and deposition technique for the passivation layer, we are able to make direct comparisons in terms of the effect of different dielectric layers on suppressing surface leakage currents.

II. Experimental Details

The epitaxial wafer was grown by Metal Organic Chemical Vapour Deposition (MOCVD) on a 2" n doped InAs substrate. The epitaxial structure consisted of a 1.5 μm n^+ doped InAs (1 x 10^{18} cm^{-3} of Si) layer followed by 4 μm of nominally undoped InAs and then a 3.5 μm p doped layer (with a linearly graded doping profile extending from 1 x 10^{16} to 1 x 10^{18} cm^{-3} of Zn) which was then capped with a 0.5 μm p^+ doped layer (1 x 10^{18} cm^{-3} of Zn).

The wafer was then fabricated into circular mesa diodes (with radii ranging from 50 to 600 μm) using standard mask lithography process and were then etched using preferred chemical etching procedures for InAs of a 1:1:1 (phosphoric acid: hydrogen peroxide: de-ionized water) etch, followed by a finishing etch of 1:8:80 (sulphuric acid: hydrogen peroxide: de-ionized water) [11, 12]. The wafer was then cleaved into a series of approximately 2 cm x 2 cm pieces for passivation. For deposition of high-k layers, the samples were placed in a Moorfields NanoPVD RF Sputter system and in total 4 different dielectric layers were deposited: Zirconium Oxide (ZrO_2), Zinc Oxide (ZnO), Aluminium Oxide (Al_2O_3) and Magnesium Oxide (MgO). The schematic diagram of InAs APD shows in Figure 1.

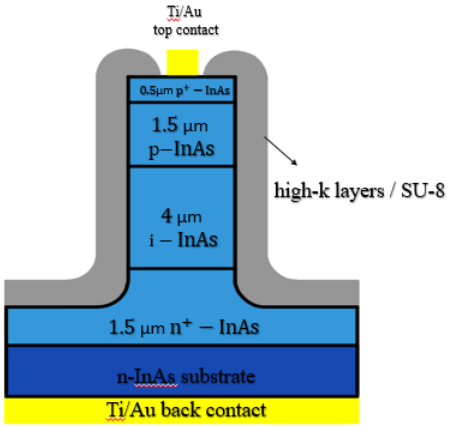

Figure 1 - The schematic diagram of InAs with the passivation layer

To determine the optimum deposition conditions for each dielectric, a series of initial layers were deposited for each material on planar InAs substrates under different deposition conditions (RF power, argon flow rate and deposition temperature). The sheet resistivity was measured for each layer using a 4-point probe technique, and the conditions resulting in the highest resistance were determined to be optimum.

The selected optimum conditions were then utilized to deposit the dielectric passivation layers onto the etched mesa diodes. The details of the deposited layers and the associated conditions are listed in Table 1. After dielectric deposition, the samples were patterned utilizing standard lithography, and an appropriate wet etch was used to remove the dielectric from the electrical contacts and optical window of the device. A reference sample was also realized by passivating one of the samples with SU8, using standard literature based procedures [12].

Dielectric Material	Layer Thickness (nm)	Deposition Temperature (°C)	RF Power (W)	Argon Flow (sccm)	Sheet Resistance (Ω/□)
ZnO	50	25	45	3	$3.2 \pm 0.6 \times 10^{11}$
Al_2O_3	50	25	45	0.5	$3.5 \pm 0.7 \times 10^{10}$
MgO	50	25	45	0.5	$6.3 \pm 0.6 \times 10^{12}$
ZrO_2	50	25	60	3	$1.6 \pm 0.4 \times 10^{12}$

Table 1 - Deposited high-k dielectric layers and their associated deposition conditions

Current-voltage (IV) measurements were performed by an Agilent Technology B1500A Semiconductor Device Analyser with a current compliance limit of 5 mA. At room temperature, the devices were directly probed via a probe station, while for temperature dependant measurements the samples were mounted onto suitable headers and wire bonded, before being placed into a liquid nitrogen cooled cryostat.

III. Results and Discussion

The room temperature current density versus voltage (JV) curves for differently sized mesa diodes are shown for all passivation materials in Figure 2. The reference device (passivated with SU8), shows good agreement between the larger sized diodes, however as the radius of the mesa's is reduced the current density increases, indicating the presence of significant surface leakage currents in these devices.

The samples passivated with ZrO_2, Al_2O_3 and MgO exhibit excellent agreement between different sized mesa's, even down to the smallest radius used in this study (50 μm). This indicates that each of these dielectric layers provides sufficient passivation to suppress any measurable surface leakage currents at room temperature. The ZrO_2 has much poorer performance than the other three high-k dielectrics used, as observed in Figure 2; the resultant devices exhibit a rapid rise in current as the reverse bias is applied, indicating near short circuit behaviour. The reasons for this are not immediately clear, however the deposition of this layer does require significantly higher RF power as detailed in *Table 1*, than the other dielectrics. One possible cause of the degradation in performance is due to this higher power causing significant surface damage to the InAs as the ZrO_2 is initially deposited.

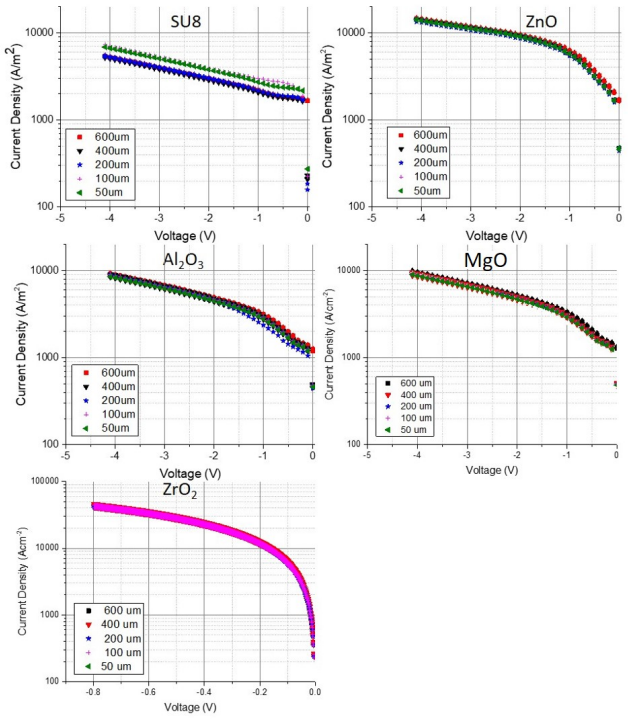

Figure 2 - Room temperature current voltage (JV) curves for InAs APDs of varying sized radius, passivated with different dielectric layers.

To further evaluate the passivation properties of these different layers, temperature dependant IV measurements were undertaken for the ZnO, Al_2O_3 and MgO samples. Due to poor room temperature performance, the ZrO_2 sample has been discounted for any further investigation in this work. For each passivation layers diodes with radii of 600, 200 and 100 µm have been measured as a function of temperature to enable the current density to be compared for each. The resultant curves for all samples at various temperatures are shown in Figure 3. For the SU8 passivated sample, as the temperature is decreased, there is an increasing divergence in the performance of differently sized devices, indicating the increase of non-bulk leakage current mechanisms as the temperature is decreased. This result indicates that as the temperature is decreased, surface leakage currents become more dominant.

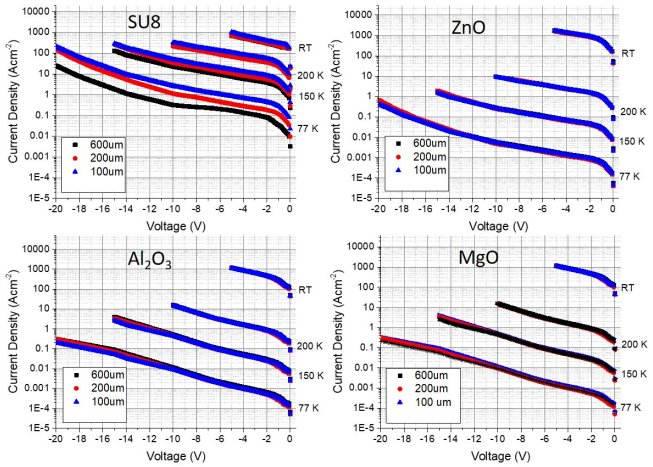

Figure 3 - Temperature dependant JV curves for InAs APDs, passivated with different dielectric layers

In contrast, for the three high-k passivated samples, a much better agreement can be seen for all samples and at all temperatures. This indicates that these layers can provide much better suppression of surface leakage currents, even at low temperatures, with only a slight deviation in current densities occurring at high voltages and the lowest temperatures.

To further investigate the temperature dependence of these leakage currents, we have performed an Arrhenius analysis. Figure 4, plots the dark current density for devices with a radius of 200 µm at an applied reverse bias of 0.2 V, plotted against 1000 / T, where T is the temperature.

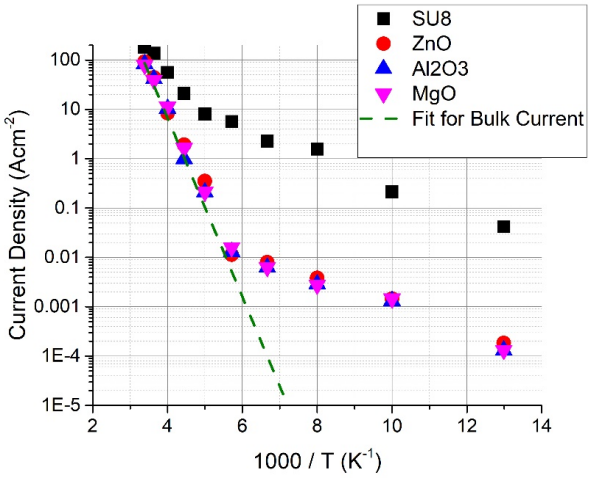

Figure 4 - Comparison of dark current density for devices with a radius of 200 µm at a reverse bias of 0.2 V, for different passivation layers

From Figure 4, a clear difference between the SU8 passivated sample and the high-k passivated samples can be seen across all temperatures. At higher temperatures only, a slight reduction in dark current is noticed for the high-k passivated samples, and however as the temperature is decreased, this reduction becomes much larger.

Despite the reduced dark currents for the samples passivated with high-k layers, there are still two distinct slopes and regimes in the Arrhenius plots. A sharp reduction in the dark current as a function of decreasing temperature occurs between room temperature and at approximately 175 K, after which a much slower reduction of the dark current takes place for further reductions in the temperature.

If the dark current was dominated by the diffusion of carriers from the cladding layers [30], then the observed current would be expected to follow a simple Arrhenius plot given by:

$$J = C\exp\left(\frac{-E_A}{kT}\right), \quad (1)$$

where C is a fitting constant and E_A is the activation energy, which we have set to 0.36 eV (the bandgap of InAs). The resultant fit is shown by the dashed line in Figure 4 and it shows an excellent agreement with the experimental data over the higher temperature region between 300 to 175 K. As expected, the fit then gives poorer agreement in the lower temperature region due to the onset of surface leakage currents, where generation and recombination of carriers at the surface of the mesa begins to dominate.

The effects of surface leakage seem to be supressed by high-k passivation at high temperature, however, even for the high-k passivated samples, there are still significant (although less compared to the reference SU8 sample) surface leakage currents at lower temperatures. These surface leakage currents are also present in Figure 3, where deviations in the current densities for the differently sized devices can be observed at higher voltages. The currents at lower voltages appear to show a better agreement due to the scale of the plots.

These results show that a variety of high-k dielectric layers can be deposited via sputtering and act as passivation layers with superior performance compared to more standard polymer-based passivation layers.

Another potential drawback from utilizing polymer-based passivation layers is that due to the mismatch in the thermal properties of the polymer layers and the underlying semiconductor layers after repeated temperature cycling, the performance of the device begins to degrade. The most likely cause of such degradation is the difference in thermal expansion and contraction of the InAs and SU8 (4.5×10^{-6} and 1.0×10^{-4} K^{-1} respectively) causing the SU8 to deform and crack, and hence degrading the passivation properties of the layer. A secondary potential advantage of utilizing high-k based passivation layers is improved temperature robustness, due to a lower mismatch in the thermal properties of these layers. ZnO, Al_2O_3 and MgO exhibit coefficients of expansion of 4.8×10^{-5} [31], 1.4×10^{-5} [32]and 1.1×10^{-5} K^{-1} [33] respectively.

To investigate the thermal robustness of these passivation layers, we have performed thermal cycling tests on each sample. For this, we have measured the room temperature IV characteristics and then cooled the sample to a temperature of 77 K at a rate of approximately 5 K per minute; the devices are then held at this temperature for 15 minutes before being heated back to room temperature at the same rate. The room temperature IV characteristics are then measured again before another temperature cycle takes place; up to 10 temperature cycles were undertaken for each sample. The resultant IV plots for devices with a radius of 200 μm, taken between temperature cycling runs, are shown in Figure 5.

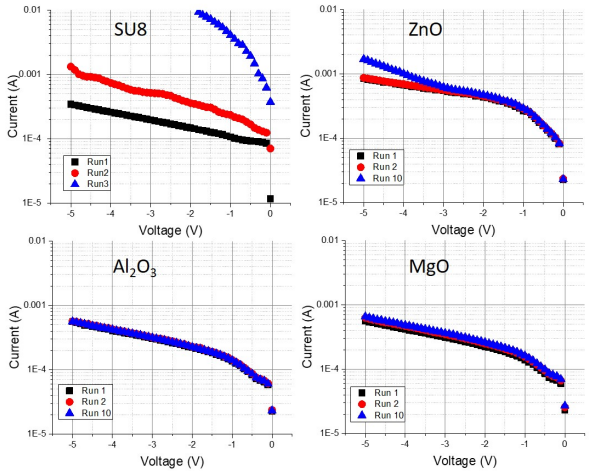

Figure 5 - Room temperature IV characteristics of passivated InAs, taken between temperature cycles

From Figure 5, it can be seen that for the reference SU8 passivated sample, after one temperature cycle, there is a significant degradation in the electrical performance of the device. After a 2nd temperature cycle, the device has undergone significant further degradation and is exhibiting near short-circuit behaviour. For all of the high-k passivated samples, a significant reduction in the degradation after each temperature cycle is observed, with good performance still be maintained even after 10 temperature cycles. For the ZnO passivated sample, no observable difference in the IV characteristics occurs after a single temperature cycle, however, after 10 such cycles an increased current is observed at the highest voltages suggesting some degradation in the layer and onset of some surface leakage current, particularly at higher bias. For the Al_2O_3 passivated sample, no degradation in performance is observed even after 10 temperature cycles. The MgO sample shows a very slight degradation in performance after each temperature cycling, resulting in almost a 10% higher current at a constant voltage after 10 temperature cycles. These results indicate that all of the high-k layers exhibit improved temperature robustness compared to the more standard SU8 passivation technique, with the best performance being obtained for the sample passivated with Al_2O_3. As previously noted, Al_2O_3 has the closest coefficient of thermal expansion to InAs, which could be the reason for its excellent behaviour under repeated thermal stress.

IV. Conclusion

We have evaluated the use of four alternative passivation layers for InAs avalanche photodiodes based on high-k dielectrics deposited via sputtering technique. We have demonstrated that ZnO, Al_2O_3 and MgO offer enhanced passivation properties compared to the more standard SU8 layers used previously in the literature. Devices passivated with these layers exhibit bulk dominated dark currents down to smaller sized mesa diodes and at lower temperatures than those passivated with SU8. We have also investigated the robustness of these layers after temperature cycling and showed that high-k passivation layers demonstrate improved performance compared to SU8.

V. References

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