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High Performance Gallium Tin Zinc Oxide Thin Film Transistors By Rf Magnetron Sputtering

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Biographical Sketch

Ngoc Huu Nguyen was born in Vietnam on March 27, 1989 to Tot Thi Duong and Lam Van Nguyen. He came to the United States in 1996 with his parents and three brothers to start a new life and a brighter future. He graduated from high school at Southwest Guilford High in May 2007 and began his professional education in August 2007 attending Guilford Technical Community College in Pre-Engineering program. In August 2010 he transferred to North Carolina Agricultural & Technical State University and received his Bachelor of Science degree in Electrical Engineering in December 2012. With his lust for learning he is currently pursuing his Master of Science at North Carolina Agricultural & Technical State University.

Dedication

This work is dedicated to my family

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μ	Mobility
AMLCD	Active Matrix Liquid Crystal Display
AOS	Amorphous Oxide Semiconductor
Au	Gold
CB	Conduction band
CBM	Conduction band minimum
C_{ox}	Oxide capacitance
D_{it}	Density of interface traps
DOS	Density of states
E_C	Conduction band energy
Ga	Gallium
GSZO	Gallium tin zinc oxide
GZO	Gallium zinc oxide
I_D	Drain current
IGZO	Indium Gallium Zinc Oxide
In	Indium
I_L	Leakage Current
I_{OFF}	Off current
$I_{ON/OFF}$	On/off current ratio
IZO	Indium zinc oxide
N_2H_2	Forming gas

NBS	Negative Bias Stress
NBIS	Negative Bias Illumination Stress
O	oxygen
O_2	Oxygen Gas
POA	Post Oxygen Annealing
PR	Photoresist
q	charge
RF	Radio Frequency
RT	Room Temperature
SCCM	Standard cubic centimeter per minute
Si	Silicon
SiO_2	Silicon Dioxide
Sn	Tin
SS	Sub-threshold swing
SZO	Tin zinc oxide
TAO	Transparent Amorphous Oxide
TCO	Transparent conducting oxide
Ti	Titanium
TFT	Thin Film Transistor
UV	Ultra violet
V_G	Gate voltage
V_{DS}	Drain to source voltage
V_o	Oxygen vacancies

V_T	Threshold voltage
W/L	Width / Length ratio
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction
Zn	Zinc
ZSO	Zinc Tin Oxide

Abstract

With the growing need for large area display technology and the push for a faster and cheaper alternative to the current amorphous indium gallium zinc oxide (a-IGZO) as the active channel layer for pixel-driven thin film transistors (TFTs) display applications, gallium tin zinc oxide (GSZO) has shown to be a promising candidate due to the similar electronic configuration of Sn^{4+} and In^{3+}. Post deposition annealing at 450 °C of the films in air was found to lead to a high atomic concentration of Sn^{4+} in the films as ascertained by x-ray photoelectron spectroscopy, which is one of the prerequisites for improved performance of the device. In this work a systematic and detailed study of GSZO TFTs with the channel annealed at 450°C has been carried out, and different effects have been investigated, including: oxygen flow, deposition contacts, further annealing in different ambients and presence of passivation layer on the TFT performance. The electrical and optical stability of the GSZO TFTs have also been the subject of study. These studies provided a more insight into the role of surface and interface states on the TFT performance and its degradation mechanism under stress. Improved device performance with V_{ON} of -3.5 V, I_{ON}/I_{OFF} of 10^8, $\mu_{FE} = 4.36\ V^{-1}\ s^{-1}$, and sub-threshold swing (SS) of 0.38 V/dec has been achieved, which is close to those of industrial standard IGZO TFTs. Thus, this work demonstrates GSZO based TFTs as a promising and viable option to the IGZO TFTs.

CHAPTER 1

Introduction

1.1 Overview

One of the most advanced discussed topics for a wide range of device applications today is the amorphous oxide semiconductor (AOS) electronics. Oxide semiconductors, especially amorphous materials with zinc oxide (ZnO) based alloys, such as indium gallium zinc oxide (IGZO), zinc tin oxide (ZSO), and gallium tin zinc oxide (GSZO) are promising thin film transistors (TFTs) that have shown tremendous progress in the display applications, challenging silicon (Si) not only in conventional applications but also new and innovative areas like paper electronics. Compared to amorphous silicon (a-Si), common thin film transistors devices use in active matrix liquid crystal displays (AMLCD) typically exhibit field effect mobility (μ_{FE}) values lower than 1 cm^2/V-s and have instability against electric stress and photo-illumination. A higher performance can be obtained with amorphous oxide semiconductor, the major advantage is that it can exhibit high optical transparency, high electron mobility of more than 5 cm^2/V-s, and have amorphous microstructure. One other major advantage of oxide semiconductor materials is it can be deposited by conventional process such as sputtering at room temperature, and have their amorphous structure enabling it to have uniform device properties over large areas for ultra-high definition display [1-3].

1.2 AOS Films and its Structure

Amorphous oxide semiconductors (AOSs) are becoming one of the most new promising semiconductor materials for active-matrix thin film transistor based backplane due to their high electrical performances and better uniformity over large areas, when comparing to conventional amorphous silicon and polycrystalline silicon TFTs [4]. Table 1 shows some of the performance

semiconductor as the active channel materials [5]. The mobility of the TFT is representative of how mobile are the carriers (i.e. electrons, holes) moving through a piece of silicon. The sub-threshold voltage swing (SS) is the measure of the required voltage to increase the drain current (I_d) an order of magnitude and the leakage current (I_O) is the current flow when the device is in the "off" state. Both amorphous oxide and poly-Si are more superior in performance than traditional a-Si, with very high mobility, low SS, I_O, and better stability performance..

As much of a greater performance from poly-Si its drawback is their unacceptable variation of electrical properties due to the grain boundary problems and inhomogeneous laser crystallization over a large area (long-range non-uniformity). With the drawback of low mobility and instability of a:Si and poor uniformity of poly-Si TFTs which is why it is not possible for AM-LCDs production of large area [5]. However, the emergence of AOS has bring new possibilities with good electrical performances which are more superior to a:Si. Furthermore, one major advantage of amorphous oxide material over a-Si and poly-Si is that the deposition can be done at room temperature for fabrication onto plastic substrate for flexible applications.

Table 1

Comparison of a-Si:H, poly-Si, and amorphous oxide TFTs.

	a-Si:H	Poly-Si (LTPS/HTPS)	Amorphous oxide
Mobility ($cm^2V^{-1}s^{-1}$)	<1	30-100	1-20
Subthreshold swing (V/decade)	0.4-0.5	0.2-0.3	0.1-0.6
Leakage current (A)	$1x10^{-12}$	$1x10^{-12}$	$1x10^{\wedge-13}$
Cost/yield	Low/high	High/low	Low/high
Stability	Poor	Good	Superior to a-Si

Table 1

Cont.

Process Temp.(°C)	150-350	250-550	RT-400(600)
Substrate	Glass, metal	Glass, metal	Glass, metal, plastic

The advantage of AOS is the origin of the high mobility, which is attributed to the electronic orbital structure of the material, as shown in Fig. 1.

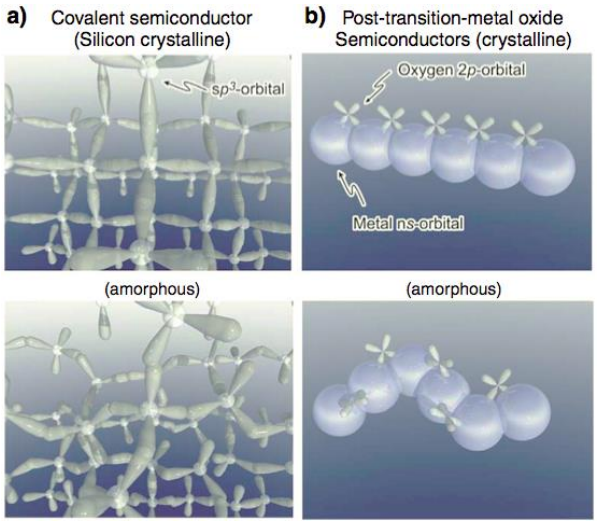

Figure 1. Schematic orbital structure of the conduction-band minimum in Si and ionic oxide semiconductor [2].

The direct overlap between the neighbor metal s orbitals occurs forming a conducting path for the free electrons. The spherical symmetry of the 5s orbital in the post-transition-metal oxide semiconductor is not susceptible to structural deformation, and the semiconductor maintains its high mobility even in the amorphous state. This is a very promising material for switching or driving element for future display technology [2]. A common alloy of ZnO semiconductor used in TFT today is IGZO. However, one of the major problem with using indium is that indium is

becoming scarce and more expensive to produce. Thus, a replacement is needed for AOS TFT applications.

1.3 Motivation

With the high demands in flat panel display technology, IGZO is one of the most promising candidate for application that requires large area of greater than 70 inches, ultra-high definition of 4000x2000, and faster frame rate of >240 Hz AMLCD panels [2]. Because of the incorporation of gallium (Ga) that aids in the stability and combining it with indium (In) together improves the device field effect mobility greater than 10 cm^2/V-s. [6]. However, despite these performances the demand and scarcity of indium (In) has introduced risk in procurement and increase in cost of production. As In availability is becoming limited (In is a by-product of mining ores from other metals, such as zinc, copper, lead, and tin existing in the earth's crust) and is more expensive, replacing In is more preferable [4]. With the need for less expensive AOS material, tin (Sn) has shown promising performances from various studies and have been reported that Sn has similar electronic configuration as In. Little work has been reported for GSZO TFTs, but it has been reported to have characteristics close to IGZO. For example, Fortunato, Elira M.C. [5] have reported device with threshold-voltage (V_T) = 4.6 V, I_{on}/I_{off} = $8x10^7$, and a sub-threshold swing (S) = 0.45 V/decade. The strong motivation from this research is the ability to fabricate GSZO TFTs and have it electrical performance comparable to IGZO.

1.4 Objectives

In this study, GSZO thin films have been investigated as an active channel for thin film transistors. The focus of this work is to improve the electrical performance of GSZO by replacing indium. Indium, like mentioning earlier, is very scarce and limited in nature, which makes it expensive for mass production. Because of the common problem associated with ZnO

based amorphous oxide in their high level of carrier traps due to various defects in the hexagonal wurtzite structure between the GSZO channel and gate oxide, this research will give an insight into the effect of various deposition parameters and post annealing techniques to improve upon the electrical performance of GSZO TFTs

The following chapters will outline this thesis. First, chapter 2 will give a literature review to AOS TFTs, mainly IGZO and GSZO and the published literatures of various parameters that were investigated with their performances. Chapter 3 will go over the experimental setups and the characterization tools used to fabricate and test the performance of the TFTs. In chapter 4 the experimental results are presented and discussed. Finally, chapter 5 provides the summary of the research work and discusses areas of further investigation for future work.

CHAPTER 2

Literature Review

2.1 Introduction

This chapter will highlight some of the published works on AOS TFTs, especially IGZO and GSZO as the replacement candidate. As mentioned in chapter 1, there has been a great interest in adapting AOS to meet the performance for display application. The main focus is to replace indium because of its high cost that is associated with scarcity, with something that is more cost efficient and have the same electron configuration as indium, hence tin is being explored for replacing indium. The following literature review will report some of the published works done on AOS materials, mainly IGZO, GSZO, and tin zinc oxide (ZSO).

2.2 IGZO

Indium gallium zinc oxide has been known for its semiconductor properties since 2003 [1]. When fabricated on thin film transistor, it has electron mobility that is one order higher than a:Si TFT. Hence, many institutes and research companies focused on this material system as a part of their research and development effect in their application for flat panel displays and other electronic devices [7].

2.2.1 Deposition temperature. Jie et al. [8] have investigated the effect of deposition temperature on the electrical performance of amorphous IGZO TFTs. Inverted coplanar TFTs was fabricated on alkali-free glass substrate with a 300 nm thick Al/Mo as the gate electrode. A gate dielectric of silicon nitride film with thickness of 300 nm was deposited by plasma-enhanced chemical vapor deposition (PECVD). The electrodes was sputtered with 300 nm thick Mo/Al/Mo. The active channel thickness was deposited by radio-frequency (RF) sputtering with a thickness of 30 nm IGZO. For the deposition temperature experiment, the temperature was

controlled by heating the substrate and was intentionally set to room temperature (RT), 150 °C, 200 °C, 250 °C, and 300 °C respectively. Finally, the TFTs were annealed in air at temperature from 150 to 350 °C. From their experiment it was investigated that the highest mobility (μ_{FE}) was at deposition of 150 °C with a value of 5.56 $cm^2/(V\text{-}S)$ and the lowest μ_{FE} of 1.6 $cm^2/(V\text{-}S)$ at deposition temperature of 250 °C. It was evident that the μ_{FE} increases with increasing IGZO deposition temperature from RT to 300 °C. For the SS and I_{off} values the RT sample exhibit the best with 0.6 V/decade and 10^{-9} A respectively.

Further investigation [8] was done on the effect of deposition temperature on the structural and composition of the films using x-ray diffraction (XRD), atomic force microscopy (AFM), and x-ray photoelectron spectroscopy (XPS) experiment. It was confirmed by XRD that IGZO thin films exhibit amorphous structure. Surface morphology of the IGZO film was studied by AFM in the range of 10x10 μm^2, where a smooth surface could be observed for all the samples. From the test all the as-deposited samples has surface roughness of less than 0.6 nm with a trend that slightly increases with increasing deposition temperature. This has been explained by the higher kinetic energy of sputtered atoms at higher substrate temperature and since the surface is smooth and shows little change with deposition, IGZO surface morphology is not responsible any observed variations in the electrical performance with IGZO as active layer channel. XPS measurements were performed to study the quantitative and qualitative chemical properties and bonding states of IGZO. XPS results revealed that the deposition temperature affects the atomic ratio and the O1s spectra, which leads to variation of carrier concentration and the I_{off} current in the devices. Based on the studies it was determined that the variation in performance with IGZO deposition temperature is due to the trap states at the front channel interface rather than IGZO bulk layer.

2.2.2 Annealing temperature. Lin et al. [9] reported on IGZO TFTs annealed at 250 °C, 300 °C, 350 °C, and 400 °C. From their research V_T is significantly shifted negatively as the annealing temperature increases to 400 °C. The negative shift in V_T at higher annealing temperature is attributed to the increase in the concentration of oxygen vacancies which is a source of more free electrons.

Hwang et al. [10] presented the effect of annealing temperature on solution-processed IGZO TFTs. The IGZO active layer was performed by sol-gel method. The gel film were annealed at various temperature in the range from 300 to 600 °C in air for 3 hours to form homogenous oxide thin films. The V_T of the TFTs decrease from 13.6 to -37.7 V as the annealing temperature increased from 300 to 600 °C. This negative shift is most likely due to the increase in the number of native defects, especially in the oxygen vacancies, with ZnO based oxide semiconductor that are known to be mainly attributed to the generation of oxygen vacancies. The oxygen vacancies in ZnO based oxide are generated by the following equation.

$$0_0^x = \frac{1}{2}0_2(g) + V_o + 2e^- \tag{2.1}$$

2.2.3 Electrical and optical stability. It is well reported [11] for thin film transistors materials that prolonged gate bias application on the TFT can cause deterioration of the current-voltage (I-V) characteristics. This can degrade the device performance which is why it is necessary to study the effect of electrical and optical stability to understand the degradation behind this bias stress effect. Dao et al. [12] reported on the positive bias stress. The DC bias conditions were V_G= +25 V and V_D=V_S= 0 V. All of the samples showed a common behavior in which there is a positive shift direction in the I_D-V_G transfer curve. This shift was due to the generation of defects originating from the creation of dangling bonds or electron trapping near the gate insulator interface.

Fuh et al. [13] investigated the roles of oxygen in IGZO TFT for device ambient stability. The inverted staggered IGZO TFT was fabricated on Si substrate with SiO_2 as the gate dielectric layer. The channel was deposited by DC sputtering with a thickness of 50 nm. The argon (Ar) has a flow rate of 10 sccm under the pressure of $3x10^{-3}$ Torr at RT. Finally, the samples were thermally annealed with N_2 gas flow rate of 10 l/hr at 350, 400, and 450 °C for one hour. To test the ambient stability of the TFT device, a stress reliability test was preformed to accelerate the oxygen absorption/desorption at the back surface of the active channel layer. After being subjected to positive gate bias stress (PGBS) with an electric field of 1 MV/cm for 180 minute at the atmosphere, the threshold voltage shifted towards the direction of positive voltages, and the variation of V_T decreased for the IGZO TFT annealed at higher annealing temperatures. This is reported that the absorption process of oxygen species from the atmosphere can capture electrons in the channel layer and generate negatively charged species ($O_{2(s)}^-$), as described by the following chemical reaction:

$$O_{2(g)} + e^- \leftrightarrow O_{2(s)}^- \tag{2.2}$$

where e^- denotes electrons, and $O_{2(g)}$ and $O_{2(s)}^-$ representing the neutral and charged oxygen molecules, respectively, in the IGZO channel layer. Under PGBS, more electrons are induced in the channel and formed negatively charged species,$O_{2(s)}^-$, which repelled conduction electrons in the channel and cause the positive threshold voltage shift. This degradation can be released by raising the annealing temperature to 450 °C. This higher annealing temperature can effectively improve the IGZO film quality and reliability of the TFTs.

Chung et al. [14] observed the hole current of IGZO under illumination. Two different gate dielectrics were used; 192 nm SiO_2 and 300 nm thick SiN_x with both having a 40 nm thick IGZO film which was deposited by RF sputtering. It was determined that there were holes in the

oxide semiconductor layer when the device is under illumination. TFTs subjected to stress conditions in the dark and under light illumination showed a negligible difference in V_T shift at wavelength longer than the threshold wavelength. This clearly point out that hole trapping is indeed the major cause of negative bias illumination temperature stress (NBITS).

2.2.4 Deposition pressure and gas flow. Chiu et al. [15] investigated the effect of oxygen partial pressure on the electrical performance of IGZO samples which were prepared at three different oxygen partial pressure (0.1%, 0.14%, and 0.2%). It was shown by XPS that the binding energies at 0.1%, 0.14%, and 0.2% were 529.43, 529.22, and 529.18 eV respectively. With these decreases in binding energy with increasing oxygen partial pressure, it is reported that polymeric dielectric exhibit a large hysteresis containing a significant number of hydroxyle groups. Furthermore, when the hydroxyl groups are present in the dielectric, the electron trapping related to the hydroxyl groups increases, resulting in large gate leakage current. These characteristics are attractive for nonvolatile thin film memory applications.

Jung et al. [16] reported on the electrical and optical characteristics of IGZO under various gas flows. The IGZO thin film was deposited on glass substrate by rf magnetron sputtering with a pressure at 0.13 Pa, and a film thickness of ~200 nm. The film was deposited as a function of different flow of Ar, Ar-4% H_2, O_2/Ar + O_2, and O_2/Ar-4% H_2 + O_2 at RT. Another sample was fabricated with 100 nm SiO_2 gate insulator with a 100 nm Ti film on the backside as gate electrode. For the channel, a 50 nm IGZO was deposited by rf magnetron with the same various gas flow at RT. The optical transmittance under Ar-4% H_2 was at 40%, while all the films that deposited under O_2/Ar + O_2 and O_2/Ar-4% H_2 + O_2 revealed high transmittance above 90%, irrespective of the oxygen flow rate. This difference is attributed to the deterioration of the film transparency due to the addition of hydrogen gas, which reduced the amount of oxygen. As

for the electrical properties the TFT fabricated under Ar-4% H_2 shows promising performance with V_T of 0.34 V, μ_{FE} of 3.2 $cm^2V^{-1}s^{-1}$, on/off ratio of 10^6, and SS of 0.04 V/dec.

2.2.5 Active layer thickness. Cho et al. [17] investigated the effect of channel thickness on the bias stress instability of IGZO TFTs. This electrical bias stress test is very crucial for commercial applications. The IGZO TFTs has a staggered bottom gate structure with a 200 nm SiN_x as gate insulator and a channel with thickness 40, 50, and 60 nm thickness. The devices were stressed at a gate-source voltage (V_{GS}) of 20 V with the I_{DS}-V_{GS} curve shifts to the positive direction as the stress time are increased with no change in the SS value. This is due to the carrier trapping in the channel/insulator interface or/and in the insulator bulk region or/and in the deep acceptor-like traps channel with negligible creation of defect states. The positive ΔV_T shift is explained by the trapping of carriers in the defect states.

Ding et al. [18] reported on the performance of IGZO with different channel layer thicknesses from 25 to 120 nm that were deposited on RF sputtering with Al_2O_3 as the gate insulator deposited by atomic layer deposition (ALD). The morphology of the TFTs root mean square (RMS) roughness (R_{rms}) was 0.6 to 0.77 nm with increasing channel thickness from 25 to 120 nm. Also, the grain size increases slightly with increasing thickness; however, the surface is smooth and uniform. Performance wise the relatively optimum TFT was obtained with the IGZO channel layer around 58 nm thick, with a V_T of 2.1 V, I_{on}/I_{off} ratio of $6.4x10^7$, and a SS of 0.6 V/decade.

2.3 GSZO

2.3.1 Deposition temperature. Fortunato et al. [19] reported on the performance of GSZO TFTs by RF magnetron co-sputtering using gallium zinc oxide (GZO) and Sn targets. Two series of transistors are produced, S1 and S2. For S1, GSZO film was deposited at RT with

S2 was produced at 150 °C. Both transistors were annealed in nitrogen, at 150, 200, 250, and 300 °C for 1 hour. The results from structural and morphological after annealing does not present any variations concerning the structure of the films. Electrical properties was not presented in the research, but are influenced by the deposition temperature along with annealing temperature. Result from XPS data have indicate that the number of hole traps in the sample decrease with the annealing temperature with a segregation of Ga^{3+} and specially in Sn^{4+} at the surface from by annealing. For the two series, S2 has a slightly improved performance with SS of 0.45 V/dec and I_{on}/I_{off} of $8x10^7$ when annealed at 300 °C.

2.3.2 Annealing temperature. Kim et al. [20] investigated the effect of post-annealing on GSZO films with different Ga contents. The films were deposited by rf sputtering at RT with a thickness of 300 nm. The films were than annealed in ambient condition for 1 h at temperatures of 200, 300, and 400 °C. The film with the low Ga doping exhibits significant changes in its electrical properties according to the annealing temperature. XPS analyses revealed that the post annealing induced the transition to a higher oxidation state for each cation and the surface enrichment in Zn resulted in changes of surface composition of GSZO films, so the doping of Ga are acting as the carrier suppressor, contributing to the stability of GSZO films.

Ogo et al. [21] reported on the effect of post annealing GSZO TFTs at temperature of 200 through 700 °C for 1 h in air. From the experiment the amorphous structure of GSZO is stable up to 600 °C, and then the chemical composition of GSZO does not have a stable crystal at thermal equilibrium at higher annealing temperature. When annealed at 300 °C, the output characteristic shows pinch-off at $V_{DS} > 10$ V, with on/off current ratio $<10^3$. At 500 °C annealed, it improves the TFT characteristics significantly, with an on/off ratio of $\sim10^6$. Also, the threshold voltage increases to positive values on increasing annealing temperature as well as the sub-threshold

voltage swing is also improved especially at temperature greater than a critical value of 400 °C. This critical annealing temperature, which the TFTs have significantly improved, is related to the incorporation of Sn and/or Zn ions. Furthermore, all the TFTs exhibit clockwise hysteresis >2V suggesting the existence of electron traps around the gate insulators. It was found that the higher-quality annealed sample exhibits an Urbach tail region below the Tauc region. The as-deposited film has the strongest subgap absorptions, which would come from defect states formed by incorporation of Sn ions. This subgap states including the Urbach tail was reduced by the annealing, which suggested the improvement of the TFTs.

2.3.3 Electrical and optical stability. Jeong et al. [22] have generated a novel AOS-TFT that has excellent bias-stress stability using solution-processed GSZO as the channel. The studied was compared with a tin-doped ZnO (ZTO) layer that lacks gallium. By photoluminescence, x-ray photoelectron, and electron paramagnetic resonance spectroscopy, it was found that the GSZO layer had a significantly lower oxygen vacancy, which acts as trap sites, than did the ZTO film. Both of the devices show similar TFT characteristics with on/off current ratio of $1x10^6$, and subthreshold slope of 1.5 V/dec. The threshold voltage was at 3 V, which means that both TFTs are operated in enhancement mode. This indicates that doping with Ga ions had no significant impact on the resulting electrical performance. With bias-stressing, the doped Ga ions had a large difference between the two devices with ΔV_T = 2 V for GSZO and ΔV_T = 8 V for ZTO from their initial transfer curves. After applying the gate bias at 20 V for 60 minutes the GSZO device had a small ΔV_T of ~4 V, while the ZTO had a ΔV_T of ~13 V. This indicates that the GSZO transistor has a bias-stress stability with minimal hysteresis and a threshold voltage shift. This difference in threshold voltage was ascribed to temporal charge trapping at the interface and/or in the channel region. It was suspect that oxygen vacancies may act as trap states. It was observed

that gallium suppressed the generation of oxygen vacancies, and the control of oxygen vacancies in sol-gel-processed ZnO-based TFT films was essential to bias-stress stability.

2.3.4 Deposition pressure & gas flow. Liang et al. [23] reported on the performance of GSZO thin films as a function of various oxygen gas content levels in the sputtering gas ambient (0, 3.8, 7.4, and 10.7%) during deposition. The deposition pressure of the chamber was below 0.53 Pa, flowing Ar and O_2 mixed gas and the RF power was at 100 W. The deposition rate of GSZO was decreased from 15.9 nm/min to 7.5 nm/min with increasing oxygen gas content. The final film thickness was around 250 nm. The resistivity of the GSZO film decreased from 78 to 19.5 Ωcm when the oxygen content was decreased from 10.7 to 0%. The carrier concentration significantly decreased from 1.81×10^{17} cm^{-3} to 5.98×10^{15} cm^{-3} when the oxygen was increased from 0 to 10.7%. This change in carrier concentration is due to the free carriers originate from oxygen vacancies. The incorporated oxygen vacancies can act as double donors when two trapped electrons are activated to the conduction band. This mechanism is as follow:

$$V_O^x \leftrightarrow V_O^{\cdot\cdot} + 2e' \tag{2.3}$$

where V_O^x is a neutral oxygen vacancy, $V_O^{\cdot\cdot}$ is an ionized oxygen vacancy, and e' is a free electron. The mobility of the device also increases rapidly with increasing oxygen pressure with a value of 13.3 cm^2 $cm^2V^{-1}s^{-1}$ at a carrier concentration of 5.98×10^{15} cm^{-3}.

2.3.5 Active layer thickness. There has been no published literature reporting on the effects of channel thickness on GSZO TFTs.

2.3.6 Prior Work from Our Group. Tanina [24] fabricated GSZO TFTs on Si substrate to optimize the performance for flexible device applications. The effects of deposition and post-deposition parameters on the film properties were investigated. Film properties were examined by x-ray diffraction (XRD) and transmission measurements on deposited films. The GSZO film

exhibit amorphous structure with transparency >80% was observed. GSZO TFTs demonstrated good electrical characteristics with $I_D = 10^{-6}$ A, V_T = -3 V, SS = 1.3 V/dec, and $I_{ON}/I_{OFF} = 10^6$. Furthermore, stable TFT was achieved under electrical and optical stress at 250 °C annealed, with ΔV_T = ~0.5 V for 3 hour under a gate bias of 1.2 and 12 V.

Robert [25] reported on low annealing temperature GSZO TFT at 140 °C for flexible substrate applications. It was found that GSO TFT annealed <140 °C have oxygen deficient films which led to porous films, with a high trap density, shallow oxygen vacancies and Zn interstitial state. On the other hand, films with rich oxygen exhibit smooth surface and denser films with Sn in the Sn^{4+} state. In addition, Robert demonstrated the first successful fabrication of bottom-gate GSZO TFTs on polyethylene naphthalate (PEN) substrate with $I_D = 10^{-7}$ A, V_{ON} = 0 V, SS = 0.7 V/dec, $I_{ON}/I_{OFF} = 10^5$ and μ_{FE} = 0.7 cm^2/V s.

Briana [26] studied the effect of electrical and optical stability of GSZO TFTs. It was found that post annealing of >350 °C shows a reduction of deep and shallow traps, which explains the superior performance over low annealing temperature at 140 °C. Electrical stability was observed with more stable device in the 450 °C annealed than the 140 °C TFTs. Optical stress at 650, 550, and 410 nm wavelengths was also investigated. Like electrical, 450 °C showed little changes in the transfer curves, with high shifting of V_{ON} for the 140 °C TFTs.

2.4 ZSO

2.4.1 Deposition temperature. There has been no published literature reporting on the effects of annealing temperature on ZSO TFTs.

2.4.2 Annealing temperature. Chiang et al. [27] investigated the annealing of 300 and 600 °C on ZSO TFTs. The ZSO TFTs are fabricated using staggered bottom gate configurations, the first being a glass substrate for fully transparent device and the second employing a doped Si

wafer with SiO_2 gate dielectric layer via thermal oxidation. The devices were annealed in air at 300 and 600 °C for 1 hour following ZSO deposition. In unannealed and annealed temperature up to 600 °C XRD result does not indicate any grain formation in the sample and show no observable differences. The optical transmittance shows a 84% transmittance at 400-700nm wavelength for the device. The annealed sample at 600 °C has a turn-on voltage (V_{on}) of -5 V and a on/off current ratio of ~10^7-10^8. As for the mobility, it was observed to be 20-50 $cm^2V^{-1}s^{-1}$.

2.4.3 Electrical and optical stability. Chen et al. [28] investigated the effects of bias-induced oxygen adsorption on the electrical characteristic instability of ZSO TFTs in different ambient oxygen partial pressures. Bottom gate ZSO TFTs with a 80 nm thickness was deposited by spin-coating at RT and atmospheric pressure, and then baked in a furnace at 350 °C for 1 hour to improve the film quality. After photolithography and wet etching, the sample were annealed at 350 °C for 1 hour in ambient oxygen. The stress condition was 10 V applied to the gate while the source and drain contacts were grounded. The I_D-V_G curve shifts in the positive direction with tiny variations in sub-threshold swing and turn-on current. This is suggested due to electron trapping in the pre-existing traps located at the interface or in the gate dielectric. After the stress, the gate bias was switched to ground to observe the recovery behavior. During the 1000 s recover, the I_D-V_G curve shifted in the negative direction. This recovery behavior is associated with de-trapping of the previously trapped charges. To further investigate the influence of oxygen, the stress were performed under different oxygen partial pressure of 10, 120, 400, and 760 torr. The threshold voltage shift seems to be closely related to the amount of surrounding oxygen molecules.

2.4.4 Deposition pressure and gas flow. There has been no published literature reporting on the effects of deposition pressure on ZSO TFTs.

2.4.5 Active layer thickness. There has been no published literature reporting on the effects of deposition pressure on ZSO TFTs.

2.5 Summary

This chapter has examined the literature published work done on IGZO, GSZO, and ZSO. Their electrical properties as well as electrical and optical stability have been discussed. For GSZO TFTs there has not been much research done on the active layer thickness at this time as well as the cause and effect of different deposition parameters and annealing. More research and experiment have to be done and examine to get the performance as close to the current IGZO TFTs as possible for next generation display technology.

CHAPTER 3

Methodology

3.1 Introduction

The following chapter is a description of the preparation of the GSZO TFTs; the deposition process, the fabrication of the TFTs, and information regarding the characterization techniques used. The RF magnetron sputtering system was used for the deposition process as well as the equipment used to anneal the film and the deposition of metal contact. The complete procedure for fabrication of the GSZO TFTs is discussed which include from a bare n^+ Si wafer to the lift-off of the metal for contacts.

3.2 GSZO TFT Configuration

The bottom-gate TFT configuration is fabricated, consisting of a 130 nm n^+ Si that acts as the bottom gate electrode followed by a thermally grown 130 nm SiO_2 dielectric on top of the Si wafer. The GSZO film was than deposited by RF magnetron sputtering and photolithography is process to make the TFTs. Following photolithography, the metal contacts are deposited using electron-beam evaporation consisting of Al or Au/Ti contacts that are the source and the drain of the device. A 3-D view of the GSZO TFT is shown in Figure 2.

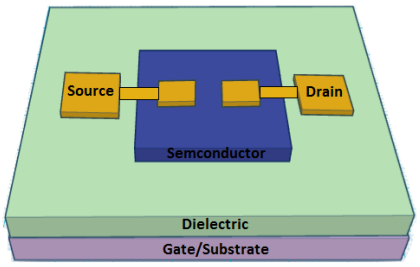

Figure 2. 3-D view of GSZO TFT (dimensions not to scale).

3.3 SiO_2 Oxidation

Prior to the deposition of the GSZO film, thermally grown SiO_2 is grown on the Si wafer as an insulator (dielectric). This oxidation process is performed within a furnace by heating the silicon wafer to a temperature of 1100 °C in the presence of pure oxygen. This oxidation process lasted for one hour, until a 130nm thickness is formed. This SiO_2 is formed through a chemical reaction occurring at the silicon surface. This dry oxidation process is identified as:

$$Si\ (solid) + \ O_2(vapor) \rightarrow SiO_2(solid) \qquad (3.1)$$

The silicon surface is consumed as the oxide grows; resulting in the final oxide layer being approximately 54% above the original surface of the silicon and 46% below the original surface. Figure 3 shows the formation of SiO_2 on the surface of the Si wafer.

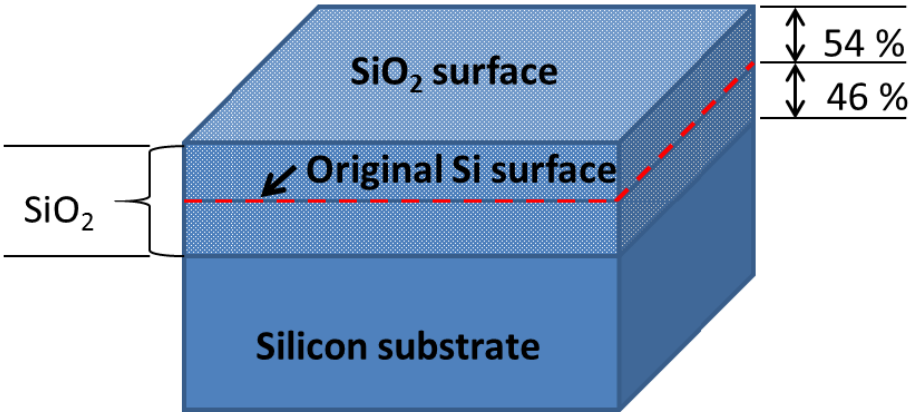

Figure 3. SiO_2 formation on Si wafer.

3.4 Film Deposition by RF Magnetron Sputtering

The deposition of the active channel layer is performed by RF magnetron sputtering technique. This process was performed in the Edwards ESM Sputtering Tool. The substrate holders are located on the lid of the chamber when opened. The substrate holders are both connected to the anode of the system while the target form the cathode. A motor to rotate the substrate is located above the lid of the chamber. Figure 5 shows the two substrate holder.

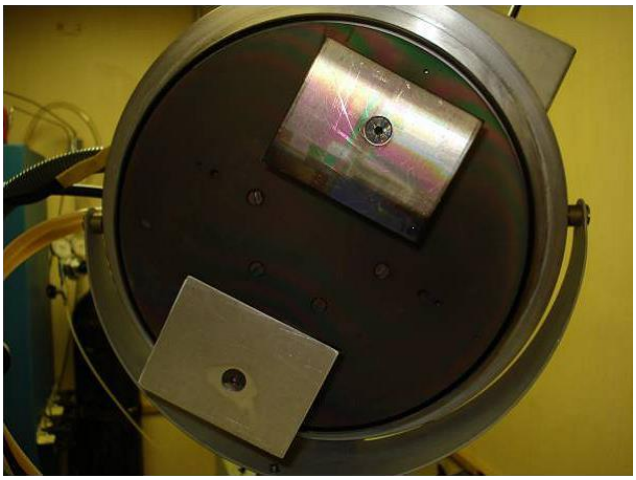

Figure 4. Substrate holders of Edwards ESM sputtering tool.

The target of the system has a diameter of 4" located approximately 90 mm away from the substrate when the lid is closed. The composition of the GSZO target used for this is ZnO (88%), Ga_2O_3 (5%), 9.9% pure SnO_2 (7%). The target's elemental atomic concentration was calculated to be 51.5, 44.4, 2.2, 1.9 % O, Zn, Ga, and Sn, respectively. Figure 5 shows the GSZO target for the experiment.

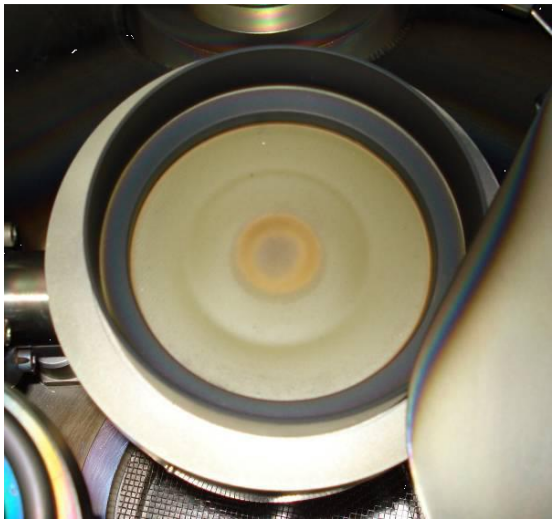

Figure 5. GSZO target.

The deposition of the GSZO film was conducted at either room temperature (RT) or elevated temperature (ET). For ET, a radiant heater is used to increase the temperature inside the

chamber. The heater is controlled by a Watlow temperature controller and a thermocouple is used to measured the temperature. Figure 6 shows the radiant heater inside the chamber for ET deposition.

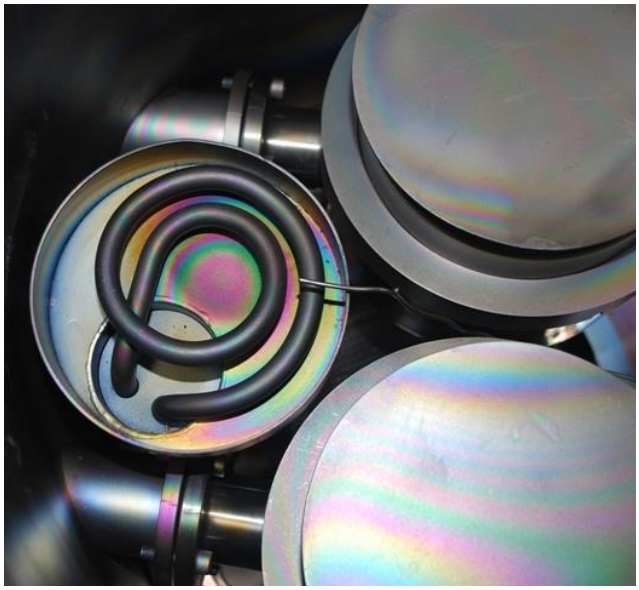

Figure 6. Radiant heater used for ET deposition.

3.5 Post Deposition Annealing

Annealing of the device was performed in an in-house built single zone annealing furnace, as shown in figure 7. The system consists of an Au coated quartz tube, sample-loading boat, and K-type thermocouples used for temperature monitoring. Annealing ambient, duration and temperature were varied. Effect of annealing temperatures and ambient will be discussed in chapter 4.

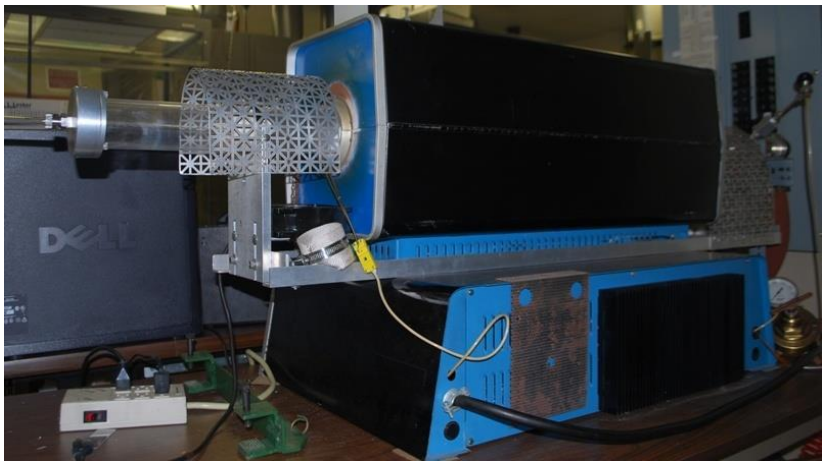

Figure 7. Annealing furnace system.

3.6 TFTs Fabrication

After deposition of the channel and annealing in the furnace, the samples undergo a series of process to achieve the bottom-gate TFTs. The TFT fabrication process consisted of the photolithography, metal contacts deposition, lift-off, and gate formation which are described below.

3.6.1 Photolithography. After annealing the sample are ready for photolithography. To begin, the sample is cleansed in acetone and propanol in an ultrasonic bath for 5 minutes each to clean the surface of any debris or contamination. After air-drying the sample, a thin coat of hexamethyldisilazane (HMDS) is spun on the GSZO at an rpm of 3000 for 30 seconds to promote adhesion of positive photoresist (PR), Microposit s1818. The sample is then baked on a hot plate for 1 minute at 90 °C and loaded back onto the spin coater for the positive PR. After baking the sample for another minute at 90 °C, the sample is then transferred to the mask aligner for exposure to ultraviolet (UV) to form the channel of the TFTs. Figure 9 shows the mask aligner station and the mask layout of the channel and source/drain design.

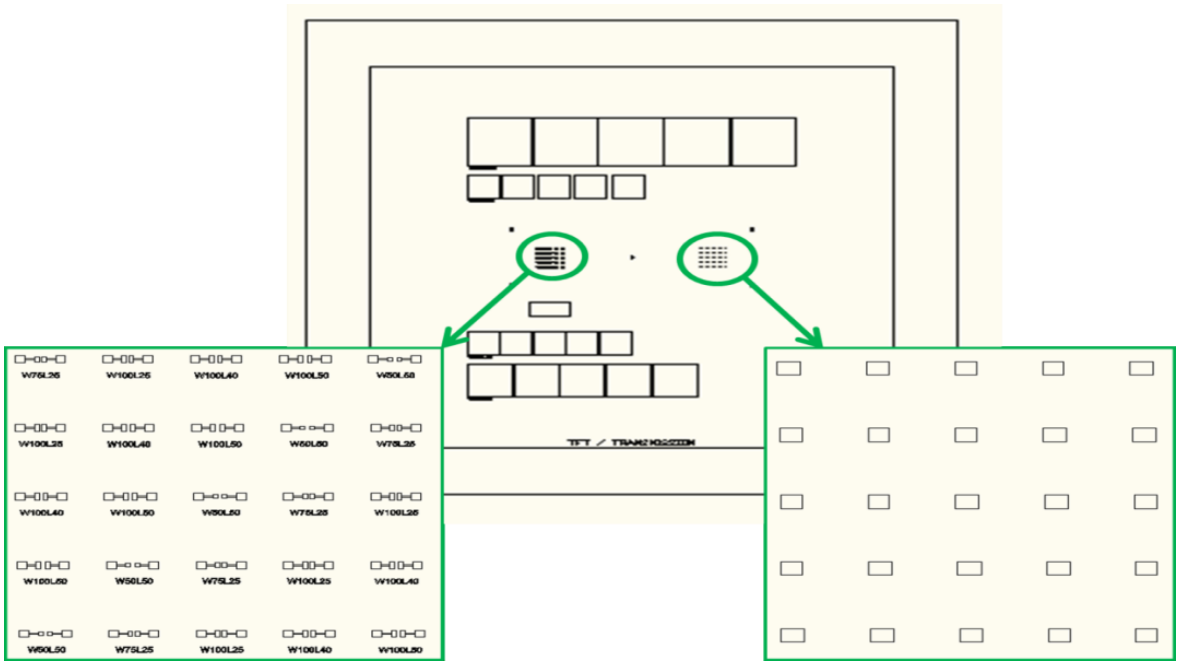

Figure 8. Mask layout design for the channel and source/drain.

After exposing the positive PR to UV lights, the sample is than hard baked at 90 °C for 1 minute and placed in positive developer to remove the unmasked portion of positive PR. At this point the unwanted regions of the GSZO film are unshielded by the positive PR. The sample is clean with deionized water (DI water) and is placed in a 500:1 DI water and hydrochloric acid (HCL) solution for approximately 8-10 seconds. This removes the unshielded GSZO and creates isolated GSZO channels on top of the SiO_2 layer. The sample is then placed in acetone and propanol to remove any remaining positive PR and cleaned for the next step. The negative PR, NFR-016D2, is used for the patterning process of the source/drain. The steps are very similar for the positive PR, but only differ in the mask aligner step where the source/drain patter must be aligned to ensure the placement atop of the channel. The UV exposure is followed hard baking at 90 °C for 90 sec and 20 sec in the negative developer. The complete photolithography process is illustrated in figure 9.

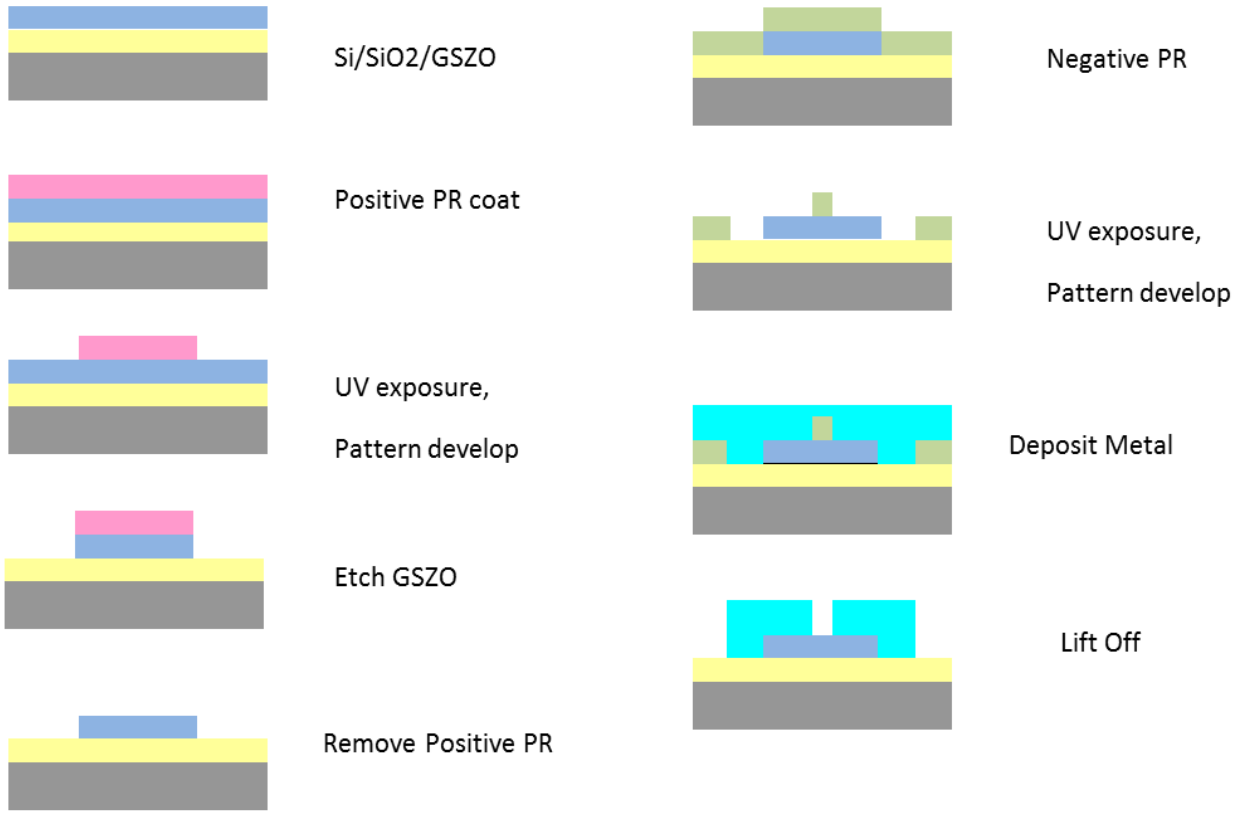

Figure 9. Photolithography process for bottom-gate GSZO TFTs.

3.6.2 Electron-beam deposition (E-Beam). The Kurt J. Lesker PVD75 (Figure 10) system is used to deposit the metals for the source/drain contacts. In this work Al and Ti/Au are used. The Al thickness is 100 nm and Ti/Au is 20/100 nm. Following deposition, the source/drain contacts are patterned by lift-off technique by placing the sample in acetone bath in a sonicator and thereafter cleaned with propanol.

Figure 10. Kurt J. Lesker PVD75 deposition system.

3.6.3 Gate formation. The Si substrate was used as the common gate for the GSZO TFTs. This is done by dispensing a tiny drop of hydrofluoric acid (HF) onto a corner of the sample to etch off a small area of SiO_2 and exposing the Si underneath.

3.7 Material Characterization

Various characterization techniques used to analyze the GSZO TFTs are introduced. This section will examine the electrical properties of the TFTs such as I-V, C-V and also electrical and optical stability. All GSZO films were deposited at 45 W in Ar/O_2 plasma ratio of 10:1.

3.7.1 Ellipsometry. To determine the thickness of our GSZO films, ellipsometry measurement was done. This contactless optical technique measures the complex refractive index and thickness of thin films. The polarization change is dependent upon the optical constants of the substrate, incidence angle of the light, the optical constants of the film, and the film thickness. A requirement of the film being measured is that it is homogenous and isotropic. Films with thickness ranging from a single atomic layer to a few angstroms can be analyzed with great accuracy.

The Rudolph Research Auto EL II model ellipsometer used to conduct ellipsometry measurements is shown in Figure 11. A He/Ne laser operating at a wavelength of 632.8 nm was used to penetrate the GSZO films and reflected to a sensor for analysis. The system displays the amplitude and phase of the reflected light wave, Ψ and θ respectively. Along with the system, the software "Rudolph Research Double Absorbing Films Calculations" is used for the conversion of the Ψ and θ values to determine the thickness of the films.

Figure 11. Rudolph Research Auto EL II Ellipsometer.

3.7.2 Current-voltage measurements. The Keithley 4200- Semiconductor Characterization System (Figure 12) and SemiProbe LA-150 probe station were used to characterize the performance of the GSZO TFTs. The electrical characteristics of the devices were plotted with the transfer and output curves. The following parameters were used to determine the device performance.

The turn-on voltage, V_{on} is defined when the corresponding gate voltage starts to increase sharply or when the drain current (I_D) is roughly equal to $5x10^{-12}$ A. Figure 13 illustrate the extraction of V_{on} along with the on-off ratio (I_{on}/I_{off}), and the threshold-voltage (V_T).

Figure 12. Keithley 4200-S system used for current-voltage measurements.

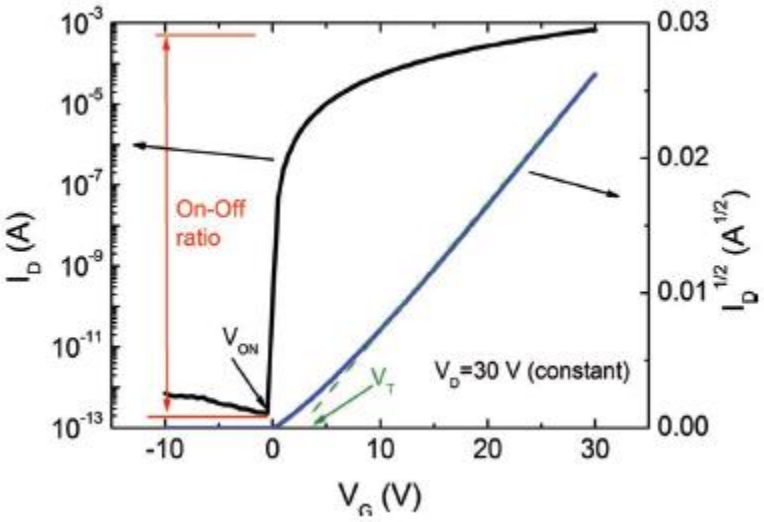

Figure 13. Transfer characteristics of TFT device.

The field-effect mobility (μ_{FE}) and sub-threshold swing (SS) was also investigated in the device performance using equation 3.2 and 3.3 respectively. The μ_{FE} is determined from the linear region of the I_D vs. V_{GS} plot with a low drain-source voltage (V_{DS}) of 0.5 V.

$$\mu_{FE} = \frac{g_m}{\frac{W}{L} C_{OX} V_{DS}} \tag{3.2}$$

where g_m is the transconductance ($g_m = dI_D/dV_{GS}$), W/L are the channel wide and length ratio, C_{OX} is the gate insulator capacitance per unit area (2.8×10^{-8} F/cm^2), and V_{DS} is fixed at 0.5 V. SS gives a measure of the increase in gate voltage required to switch the transistor from an off-state to an on-state by an order of magnitude. SS is extracted at the steepest slope in the $I_D - V_{GS}$ plot and is given by:

$$SS = \frac{\Delta V_D}{\Delta log I_D} \tag{3.3}$$

The SS values can also provide the density of total trap states (N_T) near the channel/insulator interface by the equation:

$$N_T = \left(\left(\frac{SS log(e)}{\frac{kT}{q}} \right) - 1 \right) \frac{C_{OX}}{q} \tag{3.4}$$

where e is the Euler's number, k is Boltzmann constant, T is the absolute temperature, and q is the charge of an electron.

3.7.3 Capacitance-voltage measurement. C-V measurement was also carried out on the GSZO TFTs. For this purpose, the HP 4284 LCR meter was used. Figure 14 shows the configuration set up for this experiment. This consist of a stainless steel platform with high-sensitivity probes placed on the contacts of the device under testing (DUT) connected to a triaxial cables which are connected to the HP 4284 LCR device. An in-house programmed software is used to control thee LCR meter which supplies the DC voltage and AC current to the DUT. The schematic diagram of the configuration is shown in figure 15 and table 2 shows the values used for the C-V experiments.

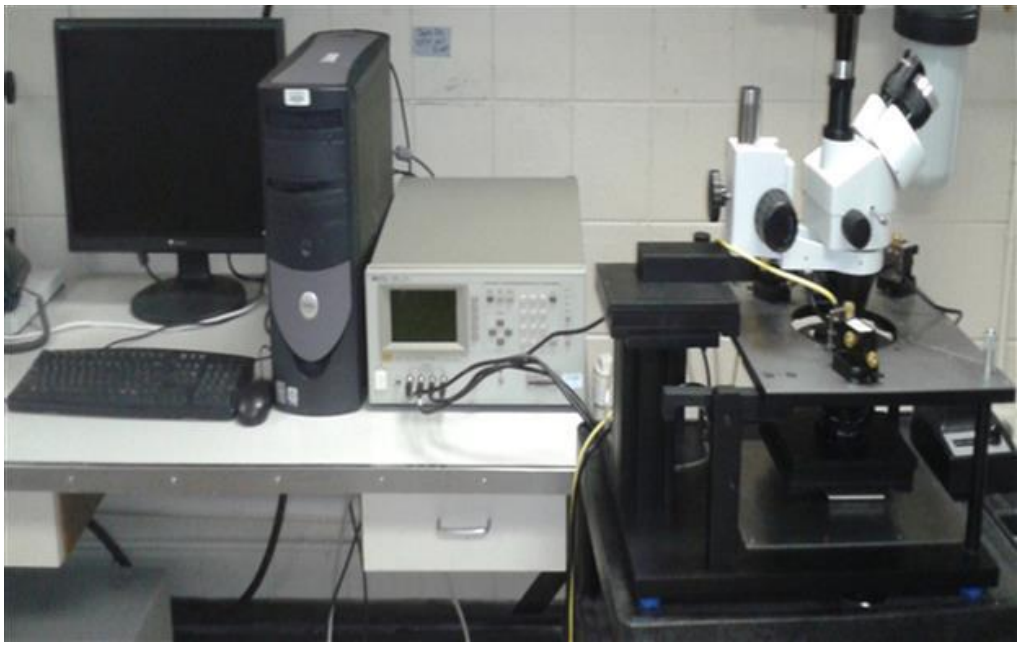

Figure 14. C-V experiment set up.

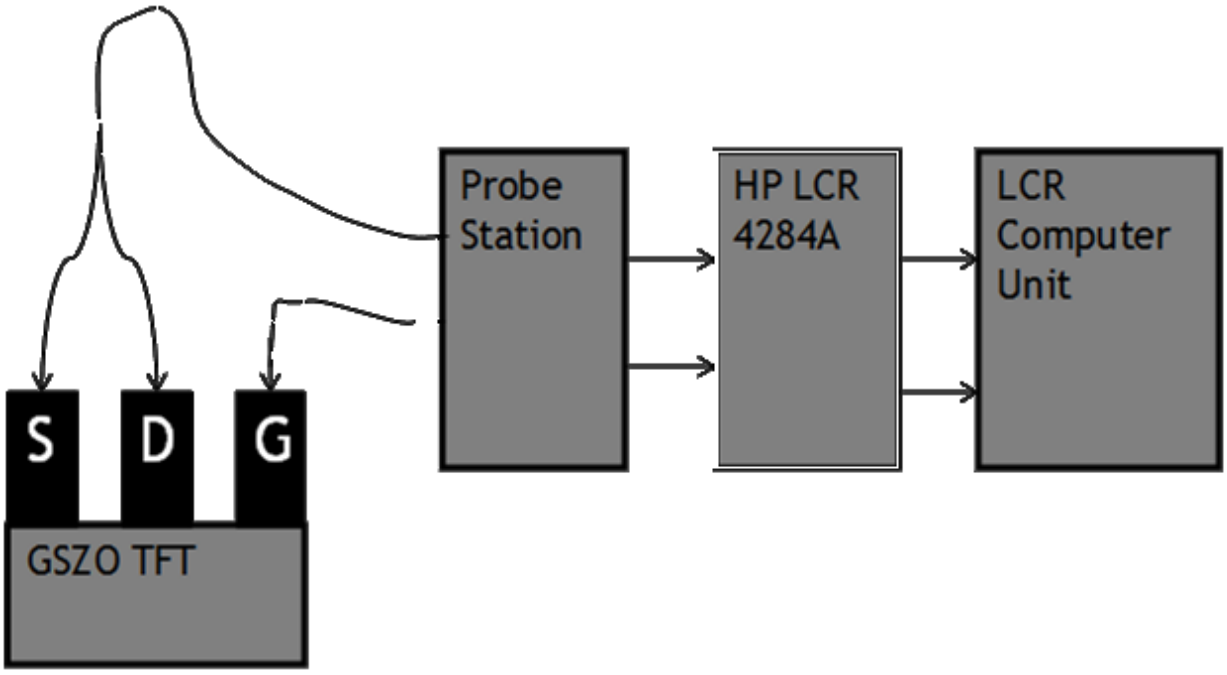

Figure 15. Schematic diagram of CV measurement.

Table 2

C-V experimental values.

AC Voltage	10 mV
Gate Voltage	-20 to 20 V
Drain/Source Voltage	Ground
Frequencies	250 – 1M Hz

3.8. Stability Procedure

3.8.1 Electrical stress. The transfer characteristics at initial state and after applying a gate bias voltage was investigated for the electrical stability to understand the degradation mechanism of the TFTs. Negative bias stress (NBS) was applied to the gate at a voltage of -20 V

at 300, 600, 1800, 5400, and 10800 seconds while shorting the source and drain electrodes during this period. The transfer characteristics were measured at a V_{DS} = 0.5 V while sweeping the gate voltage from -20 to +20 V. An unstressed TFT was used for each stressing condition.

3.8.2 Optical stress. Optical stability tests were also done to understand the optical state of the device as well as determining the energy levels of charges trapped in V_O's and the trapping mechanism within the channel/insulator interface. Photo-excitation was provided by a MicroHR Monochromator and a white halogen lamp coupled to the device channel by an optical fiber. Optical measurement were carried out in an isolated shielding box from external light, as shown in Figure 16. It was found that little variation was observed for $\lambda > 500$ nm, according to research done by our previous group [26]. For this study wavelengths 410 nm (3.02 eV) UV was investigated. For measuring the illumination stress, the channel was exposed to the wavelength with no bias and with negative bias with a time of 300, 600, and 1800, 5400, and 10800 seconds. Degradation of the device characteristics was checked by measuring the transfer characteristics at initial state, during the illumination, and after illumination at V_{DS} = 0.5 V. The analysis of the optical stability is also verified with the corresponding C-V measurement.

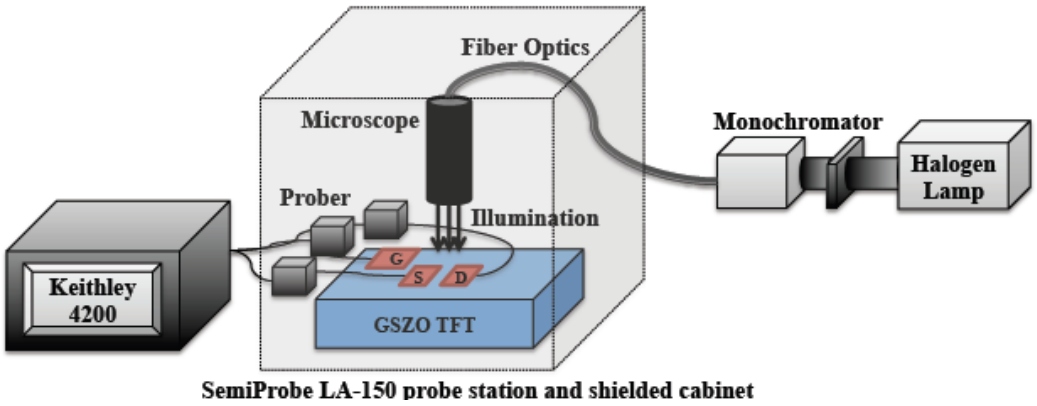

Figure 16. Optical stress configuration schematic set up.

CHAPTER 4

Results

This chapter presents the results of various experiments and characterizations on GSZO TFTs. These experiments include the effect of annealing temperature up to 450 °C, different deposition contacts mainly Al and Ti/Au contacts, the effect of oxygen flow, and the decrease in the active layer thickness. Further enhancement of the GSZO TFTs was also investigated to improve the performance of the device. These post treatment include: post oxygen annealing, exposing the device to N_2+H_2 and adding a passivation layer. Also, the stability of the device were also analyzed.

4.1 Annealing Temperature

Previous work done by our group [25] on low annealing temperature at 140 °C have shown overall poor GSZO TFTs performance, while this study will focus on the high temperature of 450 °C which have a drastic improvement in the characteristic performance of the device. The I-V plot has been plotted in Figure 17. Table 3 summarizes the electrical characteristics of the TFTs with the low and high temperature annealing. At higher temperature annealing of 450 °C, the drain and the on/off ratio has increased by 2 orders of magnitude, SS has decreased by 5 times along with a negative shift of V_{ON}. These are clear indicative of increased carrier concentration in the channel at higher annealing temperature.

Table 3

Comparison between low and high temperature annealing.

Annealing Temperature	I_D (V)	Ion/Ioff	Von (V)	SS (V/dec)
140 °C	10^{-8}	10^6	-2	1.1

Table 3

Cont.

450 °C	10^{-6}	10^{8}	-3.5	0.38

From Robert's dissertation [25] XPS characterization performed on the films to examine the effects of the annealing temperature are reproduced in this thesis (Table 4-6). XPS shows that there are slightly less O-rich oxide surface layer with annealing temperature reduction, however more O-rich in the bulk of the film. From Table 5, the O_I, O_{II}, O_{III}, are attributed to the oxygen bound with cations, to O^{2-} ions in oxygen-deficient regions, and to the presence of loosely bound oxygen on the surface of the GSZO film belonging to specific species, respectively. These species can be –CO, adsorbed H-O or adsorbed O within the amorphous film [29]. For the low annealing temperature the O_{II} at.% has decreased which shows in increase in oxygen vacancies (V_O). These Vo's can be shallow defect locations (V_O^{2+}) which can capture electrons from the conduction band and degrade the device performance as seen with low annealing temperature. XPS also show a higher density of Sn^{4+} in the 450 °C sample than the 140 °C annealed device. It is well known that Sn^{4+} is created by the migration of O atoms to nearby Sn^{2+} ions [30] and higher annealing temperature provides sufficient thermal energy for occurrence of this migration. This explains the presence of higher concentration of Sn^{4+} observed at higher annealing temperature. It is noted that higher valency Sn^{4+} configuration is the desirable configuration to replace In^{3+}.

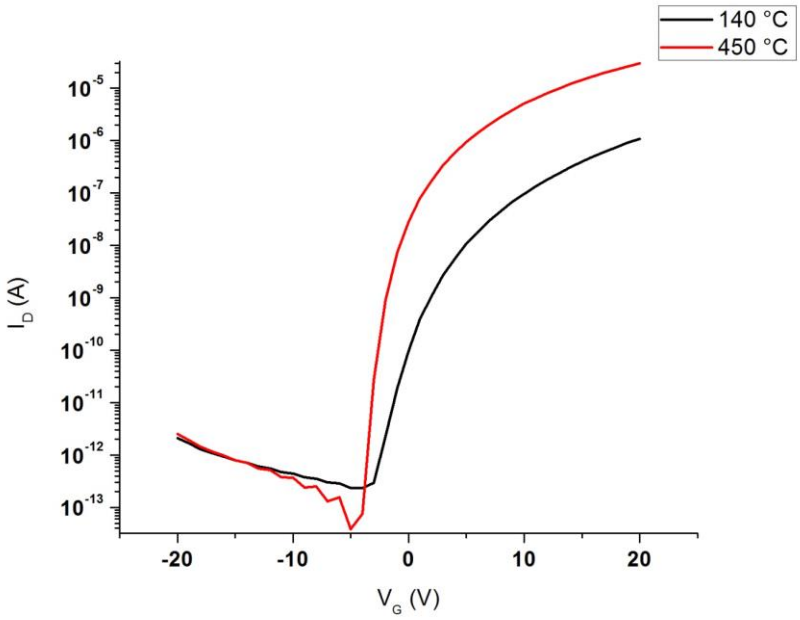

Figure 17. I-V plot for 140 °C and 450 °C annealed films.

Table 4

Atomic percentage of 15nm GSZO films annealed at 140 °C and 450 °C.

Annealing Temperature	O-(Zn,Ga,Sn)	C_l	Zn	Ga	Sn
140 °C Surface	53.6	1.0	41.1	2.2	2.2
140 °C Sputtered	47.7	0.1	46.6	4.6	1.0
450 °C Surface	58.7	0.3	37.0	1.6	2.3
450 °C Sputtered	43.6	0.0	50.8	4.3	1.3

Table 5

O-1s relative percentage of 15nm GSZO films annealed at 140 °C and 450 °.

Annealing Temperature	O Relative %			Binding Energy (eV)		
	O_I	O_{II}	O_{III}	O_I	O_{II}	O_{III}
140 °C Surface	61	34	5	530.2	531.7	532.7
140 °C Sputtered	76	24	0	530.3	531.7	532.7
450 °C Surface	58	35	7	530.3	531.8	532.7
450 °C Sputtered	86	14	0	530.3	531.7	532.7

Table 6

Sn relative percentage of 15nm GSZO films annealed at 140 °C and 450 °C.

Annealing Temperature	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
140 °C Surface	14.1	85.9	0	486.2	486.8	0
140 °C Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
450 °C Surface	28.1	71.9	0	486.2	486.8	0
450 °C Sputtered	42.6	57.4	0	486.2	486.8	0

4.2 Transistor Performance

4.2.1 Effect of deposition contacts. The effect of different S/D contacts, which were deposited by E-Beam on the performance of the GSZO TFTs were investigated. Two contacts were used: Al and Ti/Au with a thickness of 100 nm and 20/100 nm respectively. The I-V plot, output plot, and electrical characteristics are illustrated in Figure 18, Figure 19 and Table 7 respectively. Both TFTs exhibit good overall performance with Al contact slightly better drain current, Ion/Ioff ratio, V_{ON} and a field-effect mobility of 3.37 cm^2/Vs. The output characteristics of the two devices also exhibit good ohmic contact property and current saturation behaviors. The amount of I_D has also increased with Al contact. This increase in I_D can be understood in the same manner as conventional metal-oxide-semiconductor transistor structures, which is the reduction of parasitic contact resistance between the electrode and channel layer [31].

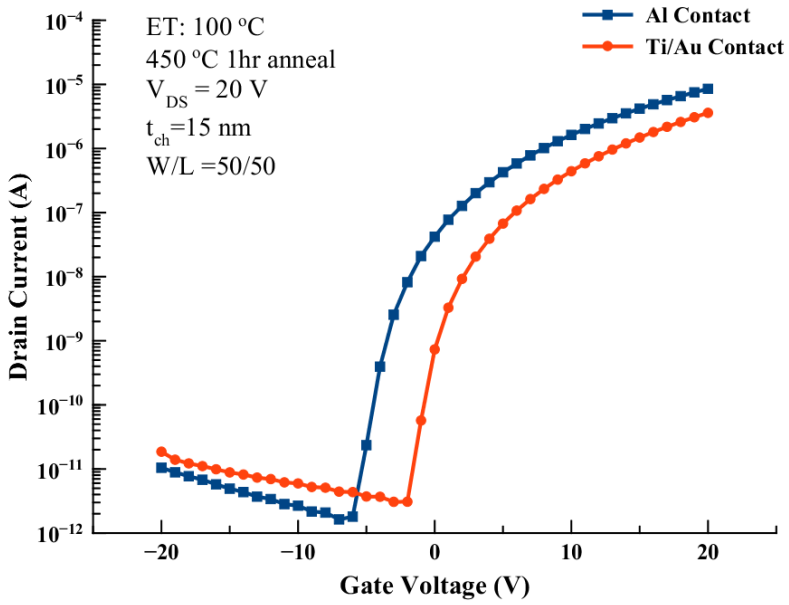

Figure 18. I-V charactersitics with Al and Ti/Au contacts.

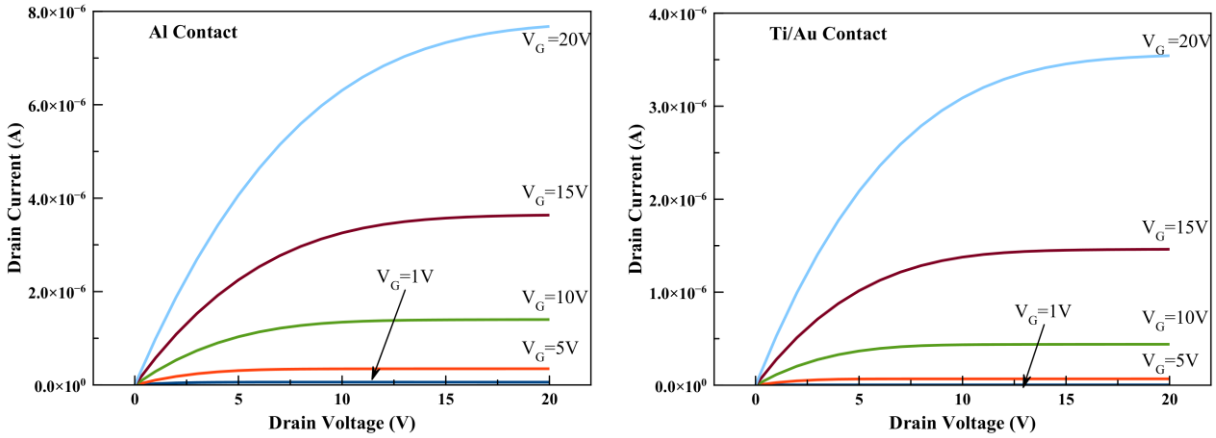

Figure 19. TFT output characteristic plots with Al and Ti/Au contacts.

Table 7

TFT characteristics with Al and Ti/Au contacts.

Contact	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/dec)	μ_{FE} (cm^2/V-s)
Al	$8.5x10^{-6}$	$4.7x10^{6}$	-6	0.8	3.37
Ti/Au	$3.5x10^{-6}$	$1.1x10^{6}$	-2	0.78	1.94

4.2.2 Effect of oxygen flow. The influence of oxygen incorporation in the deposition process has been investigated. During this experiment TFTs were produced with 2 and 10 sccm oxygen flow. For both TFTs the GSZO channel was 15 nm and was annealed in air at 450 °C for 1 hr. The electrical performance of these devices is shown in Figure 19, Figure 20 and Figure 21. Table 8 shows the electrical performance of both the TFTs. Here it is observed that with increasing oxygen flow there is a positive shift in V_{ON} from -6 to -2 V. The I_{OFF} current has also reduced in the 10 sccm TFT. The sub-threshold remains the same for both samples at 0.8 V/dec and the field-effect mobility has reduced from 3.37 to 2.7 cm^2/Vs with increasing oxygen flow.

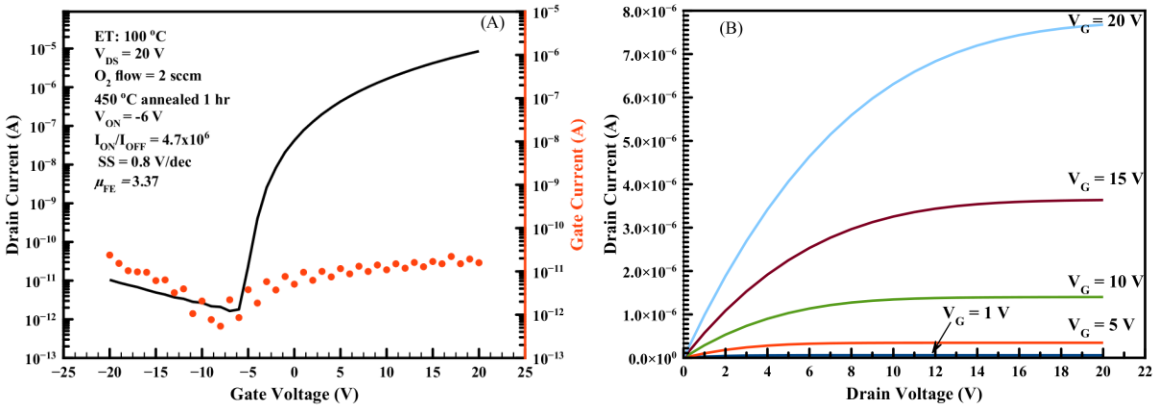

Figure 20. ET 450 °C annealed 2 sccm O_2 TFT (a) transfer and (b) output characteristics.

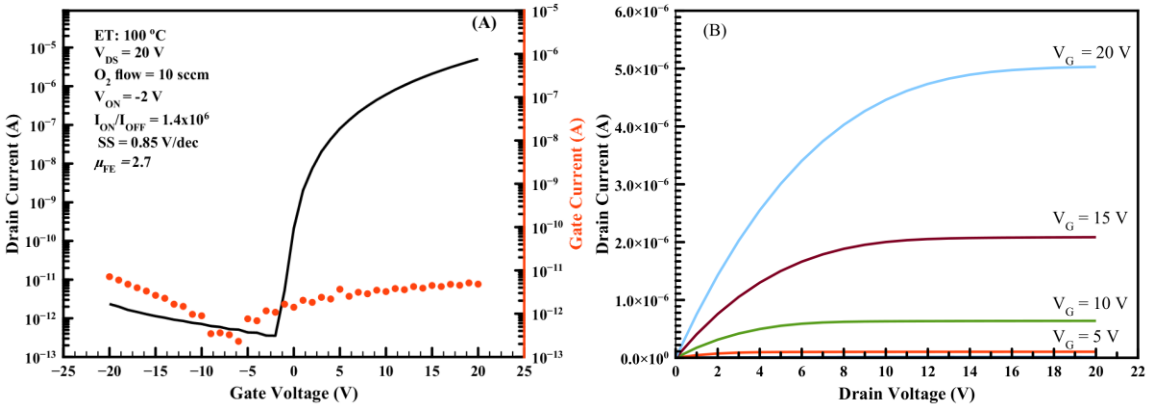

Figure 21. ET 450 °C annealed 10 sccm O_2 TFT (a) transfer and (b) output characteristics.

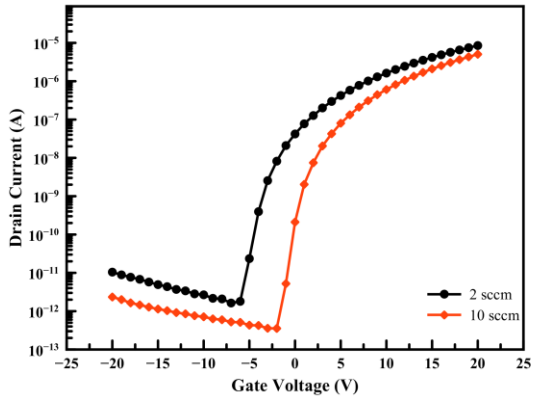

Figure 22. Transfer characteristic comparison between 2 and 10 sccm O_2 flow.

Table 8

Comparison between TFT performance with 2 and 10 sccm O_2 flow.

Oxygen Flow (sccm)	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
2	$8.5x10^{-6}$	$4.7x10^{6}$	-6	0.8	3.37
10	$5.00x10^{-6}$	$1.4x10^{7}$	-2	0.85	2.7

From previous work done by our group [24] it was found that the elemental at.% concentrations were slightly varied as O_2 was increased during the deposition of GSZO film. The differing trends of O_2 flow and oxygen at.% is attributed to both a reduction in surface point defects and chemisorption of O_2 molecules onto the films surface. Surface defects are reduced with increased O_2 during deposition, thereby reducing the dangling bonds available to induced chemisorption [32]**.** The positive change in V_{ON} and the reduction in the field-effect mobility as shown in Figure 22 may be caused by the disorder that produces tail states in the vicinity of the band edge and leads to the reduction of the band gap (E_g)**.** The optical band gap was not conducted for this research, but Shin et al. [33] has reported that with increasing oxygen flow the E_g decreases. Therefore, μ_{FE} degrades gradually with increasing oxygen content. Also, from Tanina's dissertation [24] as the Ga/O_I ratio increases the carrier concentration in the film is decrease because Ga is considered as scavenger of oxygen vacancies due to its strong bonding with oxygen. This is verified again in Figure 22 with V_{ON} shifting in the positive direction. Thus, a higher gate voltage is required to turn on the TFT at higher oxygen concentration.

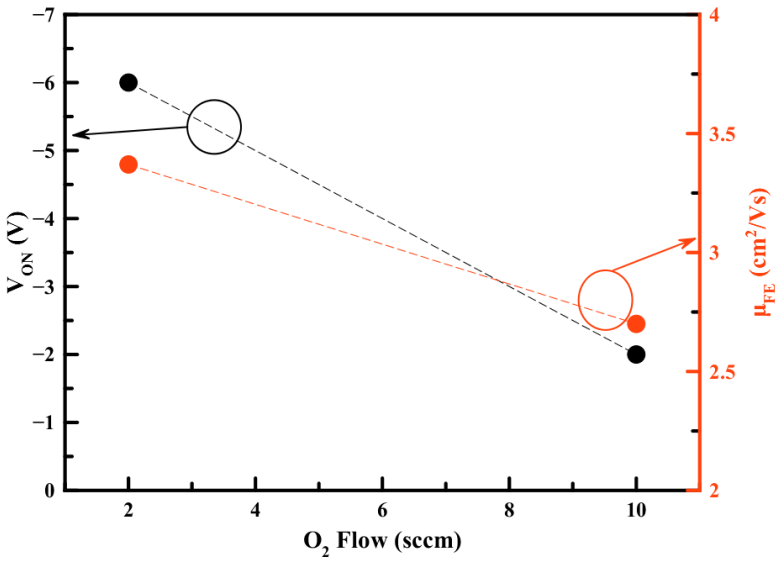

Figure 23. Turn-on voltage and field-effect mobility as a function of O_2 flow.

4.2.3 Active layer thickness. The channel thickness of GSZO was varied to examine the effect on the electrical properties of the devices. The transfer characteristic of 15 and 8 nm channel devices are plotted in Figure 23 – Figure 25 with Figure 26 comparing the SS, V_{ON}, and μ_{FE} as a function of channel thickness. Their electrical properties are shown in Table 9. Both I_{ON} and I_{OFF} decrease with decreasing channel thickness, with on/off ratio slightly better with the 8 nm channel. Von has largely shifted in the positive direction from -9 V to 1 V with the 8 nm device. SS also improves significantly from 0.91 to 0.3 V/dec with reduction in channel thickness, however, the field-effect mobility has decreased from 4 to 0.87 cm^2/Vs.

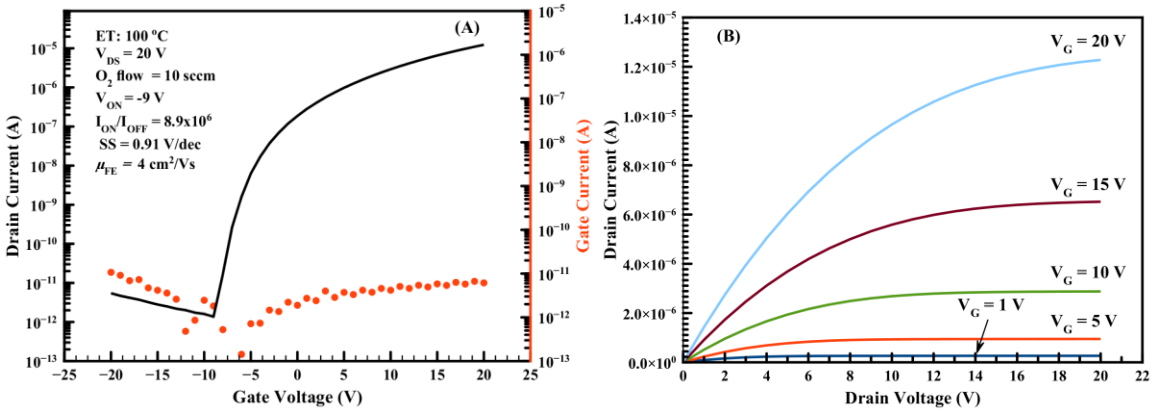

Figure 24. ET 450 °C annealed 15nm (a) transfer and (b) output characteristic.

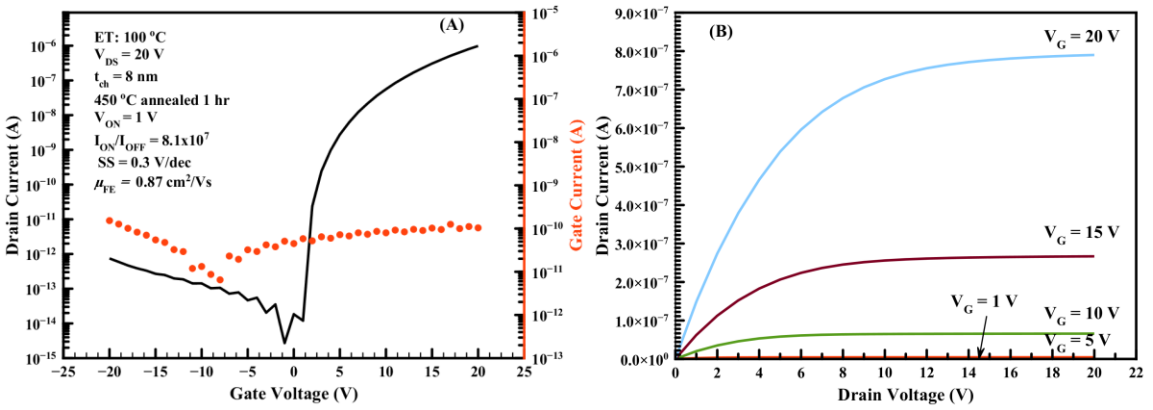

Figure 25. ET 450 °C annealed 8 nm (a) transfer and (b) output characteristics.

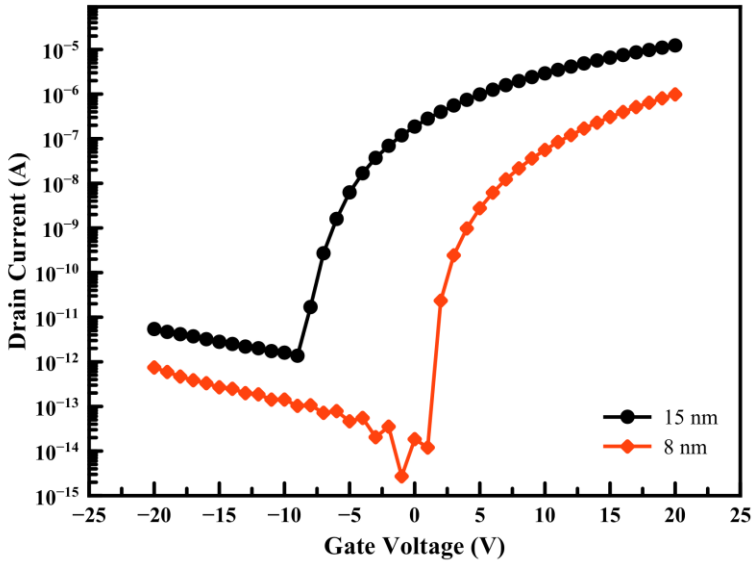

Figure 26. Channel layer thickness transfer characteristic comparison between 15 nm and 8 nm.

Table 9

Electrical characteristic comparison for 15 nm and 8 nm channel thickness.

Channel Thickness (nm)	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)	Density (g/cm^3) [25]
15	$1.2x10^{-5}$	$8.9x10^{6}$	-9	0.91	4	~5.9
8	$9.8x10^{-7}$	$8.1x10^{7}$	1	0.3	0.87	~7

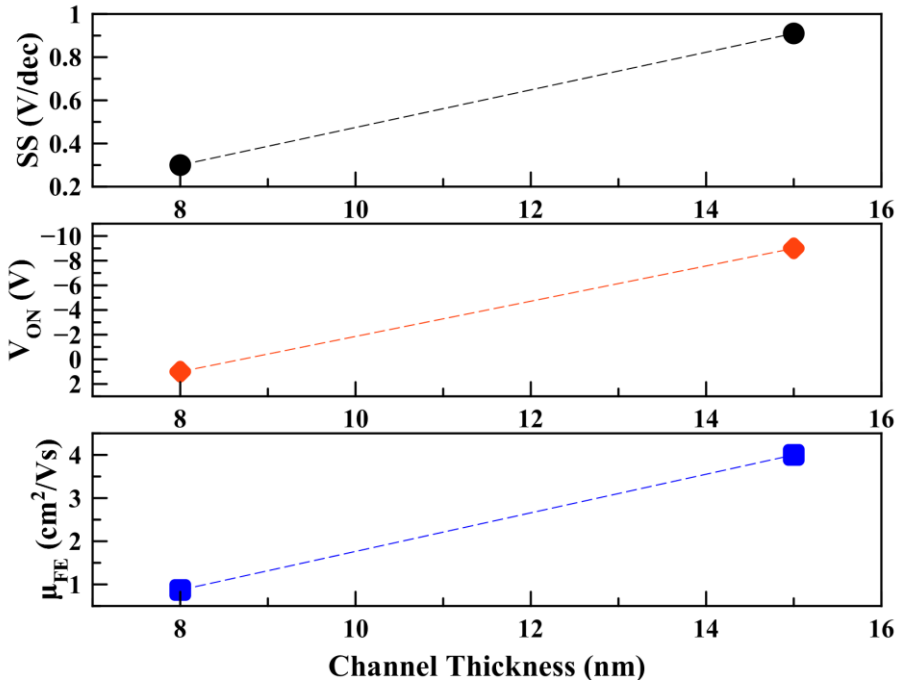

Figure 27. The changes in sub-threshold swing, voltage threshold, and field-effect mobility as a function of channel thickness.

With the reduction in the active layer thickness, the TFT electrical performance has improve significantly. This improvement in the performance is attributed to: (i) The active channel layer thickness extends only a couple of nm from the SiO_2/GSZO interface and (ii) the thinner channel layer is denser and exhibit smoother interface, as given in Table 9, giving rise to a better SS value. The thicker channel layer impacts negatively the TFT performance by contributing to the background carrier concentration resulting in the negative V_{ON} shift with increase in I_{OFF}. The increase in I_{OFF} is directly proportional to the channel thickness, from Equation 4.1 [34].

$$I_{OFF} = \frac{\sigma W t_{CH}}{L} V_{DS} \tag{4.1}$$

where t_{CH} is the channel thickness, W/L are the width and length of the channel, σ is electrical conductivity, and V_{DS} is drain source voltage.

To explain the positive shift in V_{ON} and the decrease in I_D, the surface of the channel is sensitive to the oxygen adsorption from the ambient forming different bonded negative ionic species such as O^{2-}, O^- and aids in creating the depletion region at the surface. A significant portion of the depletion region occupies the channel for the thinner channel, which restricts the channel conductivity and gives rise to the decrease in drain current, as observed in the 8 nm channel. Also, the fully depleted region has already formed in the 8 nm channel when a small positive gate voltage is applied which leads to a positive V_{ON} at 1 V. Thus, the reduction in channel thickness is more advantage in improving the performance for GSZO TFT.

4.2.4 Annealing ambient. Following the fabrication of the GSZO TFTs post treatment was done to the TFTs to investigate their effect on the TFT characteristics. These post treatment include post oxygen annealing (POA), exposing the TFTs to forming gas, and forming a passivation layer to help enhance the TFTs performance.

After fabrication of the GSZO TFTs the sample was annealed in oxygen at 200 °C for 5 min for two set of samples, 2 and 10 sccm oxygen flow. The transfer and output characteristic are plotted in Figure 27 - Figure 30 and Figure 31 compares the 2 and 10 sccm I-V characteristic behavior. The electrical properties are given in Table 10.

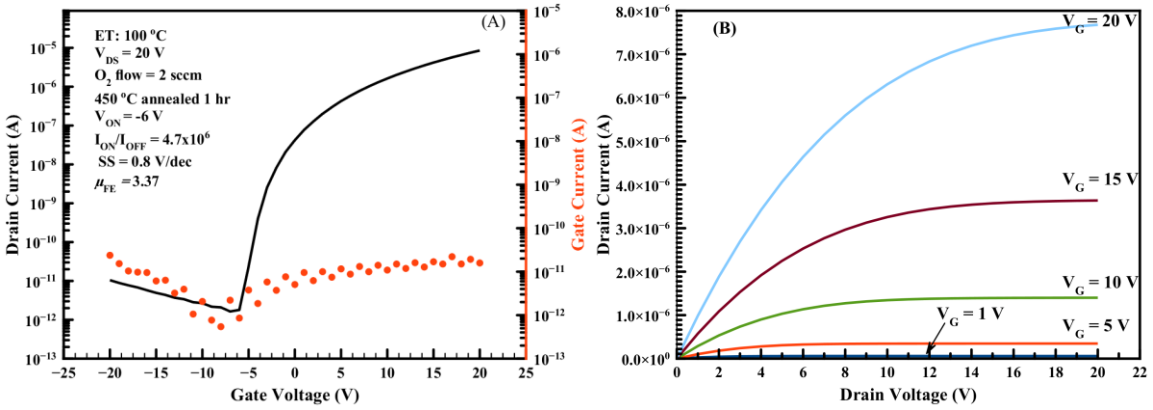

Figure 28. As-deposited with 2 sccm O_2 flow: (a) transfer and (b) output characteristics.

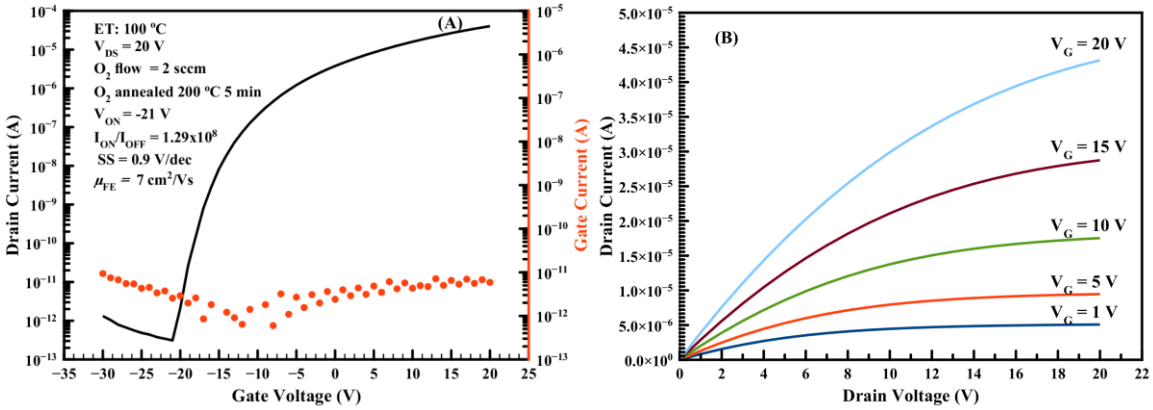

Figure 29. 200 °C annealed with 2 sccm O_2 flow: (a) transfer and (b) output characteristics.

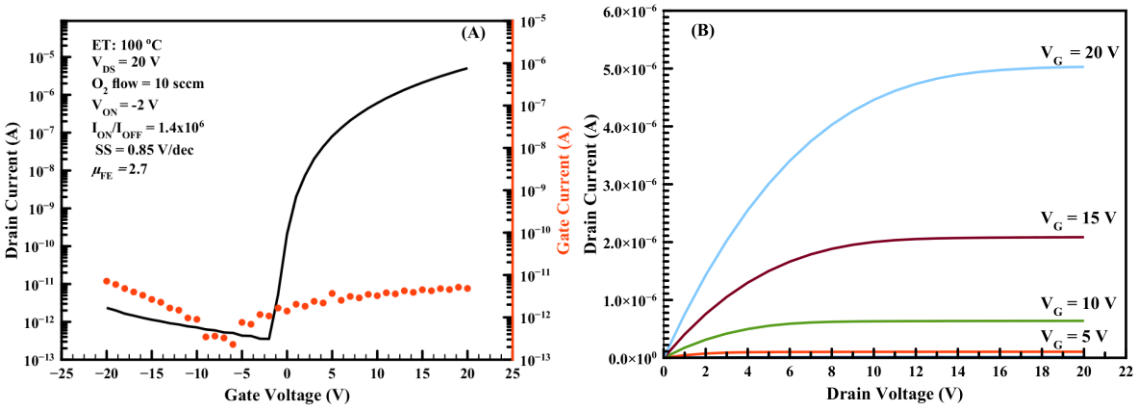

Figure 30. As-deposit film with 10 sccm O_2 flow: (a) transfer and (b) output characteristics.

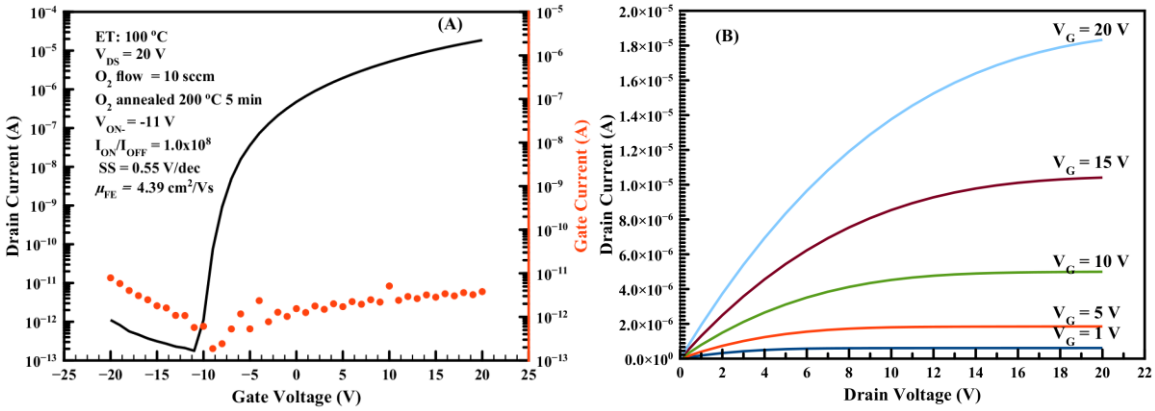

Figure 31. 200 °C O_2 annealed 10 sccm (a) transfer and (b) output characteristics.

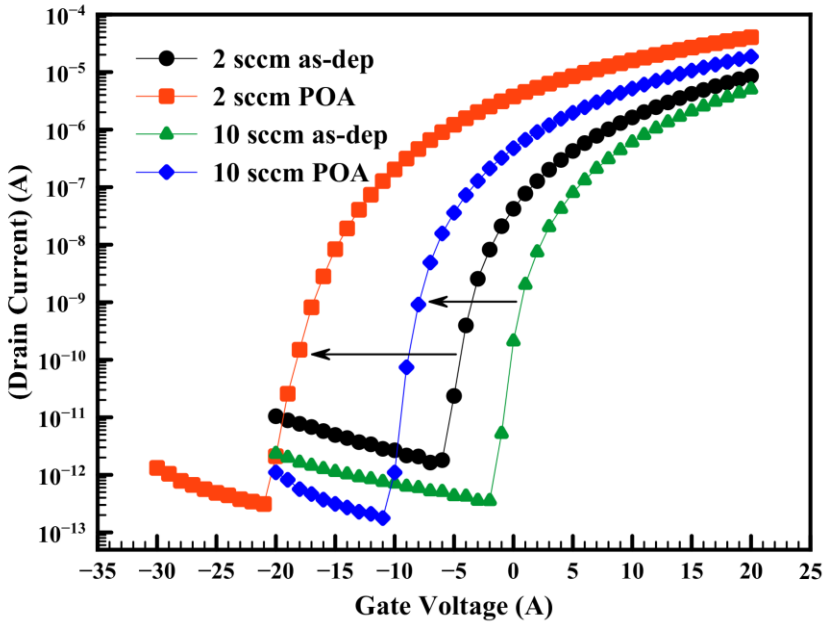

Figure 32. Effect after POA I-V showing V_{ON} shifted negatively.

Table 10

POA electrical performance.

Condition	O_2 flow (sccm)	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
As-dep.	2	$8.5x10^{-6}$	$4.7x10^{6}$	-6	0.8	3.37
	10	$5.0x10^{-6}$	$1.4x10^{7}$	-2	0.85	2.7
POA	2	$4.0x10^{-5}$	$1.29x10^{8}$	-21	0.9	7
	10	$1.8x10^{-5}$	$1.0x10^{8}$	-11	0.55	4.39

After POA both devices show overall improvement in their electrical characteristic. I_D has increase for both O_2 flow from $8.5x10^{-6}$ A to $4.0x10^{-5}$ A for 2 sccm and from $5.0x10^{-6}$ A to $1.8x10^{-5}$ A for the 10 sccm device with a corresponding increase in on/off ratio for both TFTs. μ_{FE} also improve from 3.37 to 7 cm^2/Vs and from 2.7 to 4.39 cm^2/Vs for both 2 and 10 sccm TFTs, respectively. It is observed in both O_2 flow cases V_{ON} after POA has shifted negatively. Figure 31 illustrates the shifting of the I-V characteristics and V_{ON} change.

After POA, further investigation was done to both POA devices by exposing the sample to forming gas to find out if there is any further improvement to the TFTs performance. Figure 32 shows the I-V characteristic compared with as-deposited and subsequent POA in forming gas ambient. Table 11 summarizes the electrical characteristics result. From the I-V graph it is observed that there is a large negative shift of V_{ON} to -26 V. I_D has a small increase to $6.4x10^{-5}$ A with I_{OFF} remaining invariant at 10^{-13} A range.

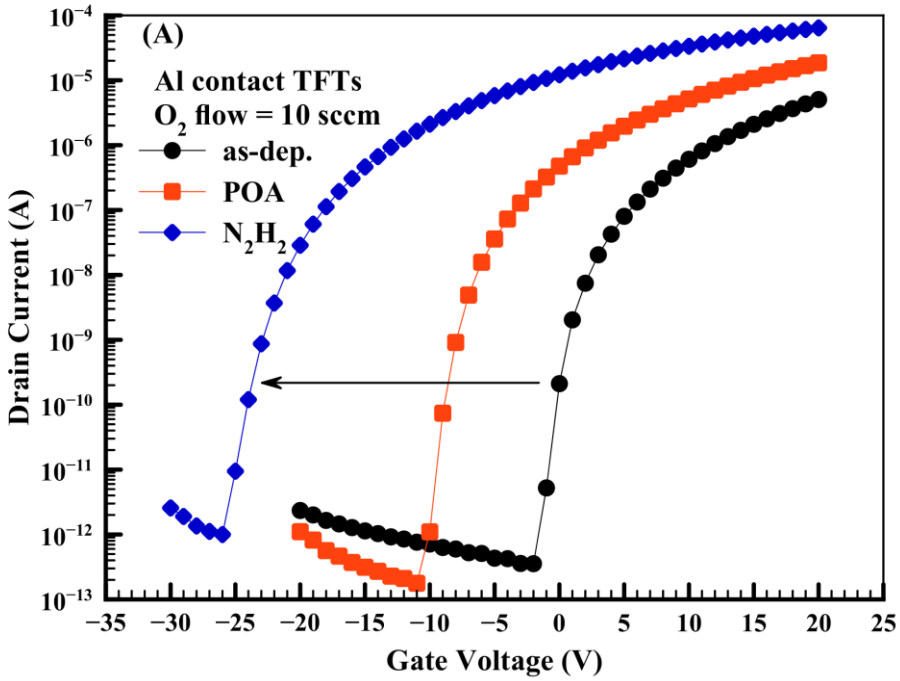

Figure 33. I-V characteristic after exposing to forming gas.

Table 11

Electrical performance after exposing to forming gas.

Condition	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
As-dep.	$5.0x10^{-6}$	$1.4x10^{7}$	-2	0.85	2.7
POA	$1.8x10^{-5}$	$1.0x10^{8}$	-11	0.55	4.39
N_2H_2	$6.4x10^{-5}$	$5.7x10^{7}$	-26	0.9	7.2

4.3 Effect Passivation Layer on GSZO TFTs

The effect of forming a passivation layer was investigated on the performance of GSZO TFTs. SU-8 2100 epoxy-based negative photoresist was used for this experiment. The process flow for the passivation layer of SU-8 is shown in Figure 33. After the fabrication of the GSZO

TFTs, SU-8 is spin-coated at 3000 rpm for 30 sec with a thickness of approximately 100 μm and prebaked on a hot plate at 95 °C for 30 min. After that the film was then exposed to UV light in hard contact mode. Immediately after exposure the GSZO TFTs are baked on a hot plate at 95 °C for 15 min and then developed in SU-8 developer. Finally the device is cleaned in isopropanol and rinsed with DI water and dried with nitrogen. Control device, without any passivation layer was also fabricated. The device was hard baked (annealed) in air at 200 °C for 1 h after forming the passivation layer. Transfer characteristics of TFTs measured at V_D=20 V are presented in Figure 34 – Figure 37 and C-V plots are shown in Figure 38. Table 12 shows the electrical characteristics performance of the devices. The pertinent growth and device parameters for the devices fabricated are 10 nm GSZO film, 130 nm SiO_2 layer, 5 mtorr and 10 sccm.

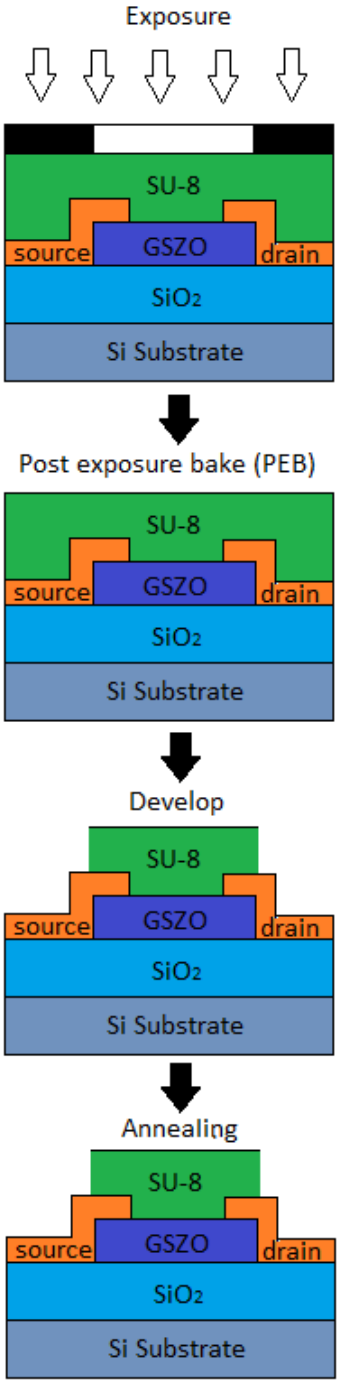

Figure 34. Process flow of SU-8 passivation layer.

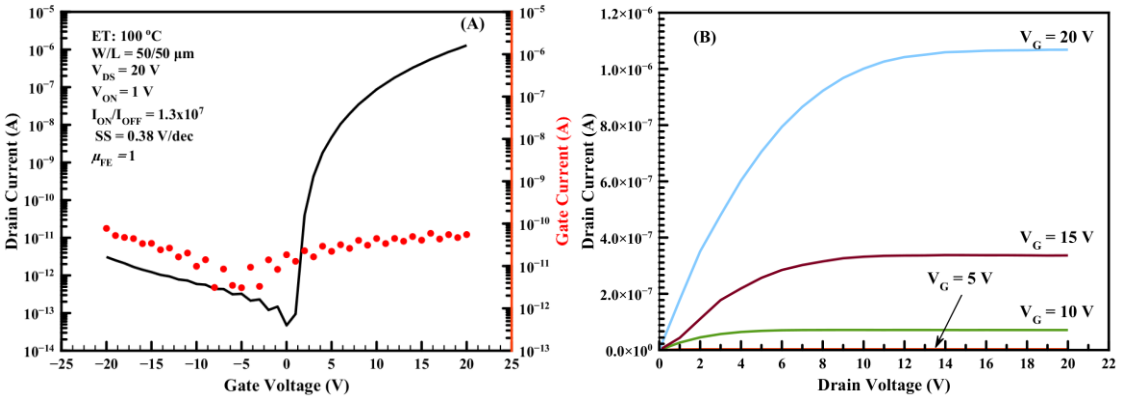

Figure 35. References TFT without any passivation layer: (a) Transfer characteristic unpassivated and (b) its output characteristics.

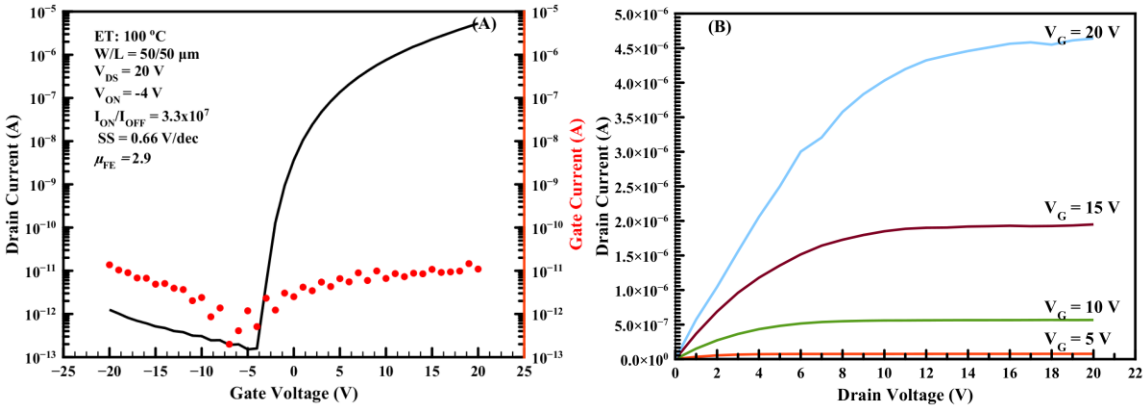

Figure 36. (a) Transfer characteristic of passivated non-annealed, and (b) its output characteristics.

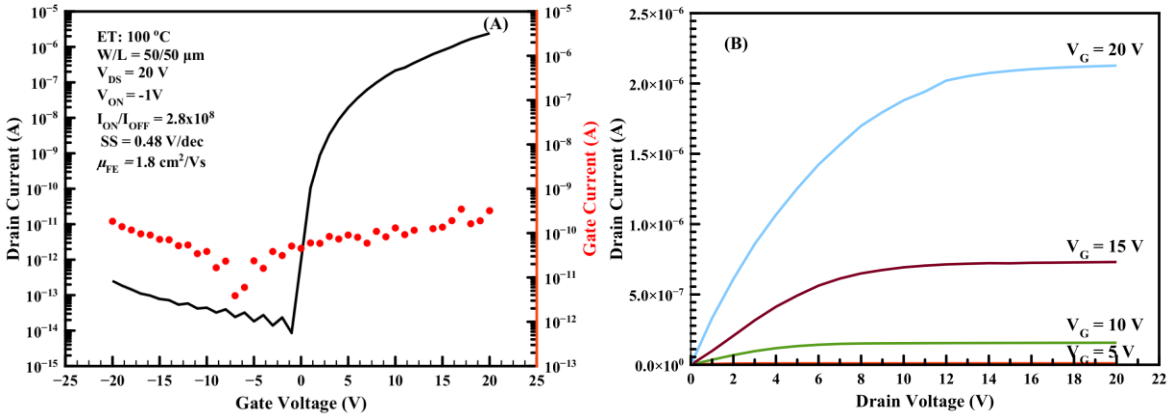

Figure 37. TFT annealed at 200 °C for 1h and passivated: (a) Transfer and (b) its output characteristics.

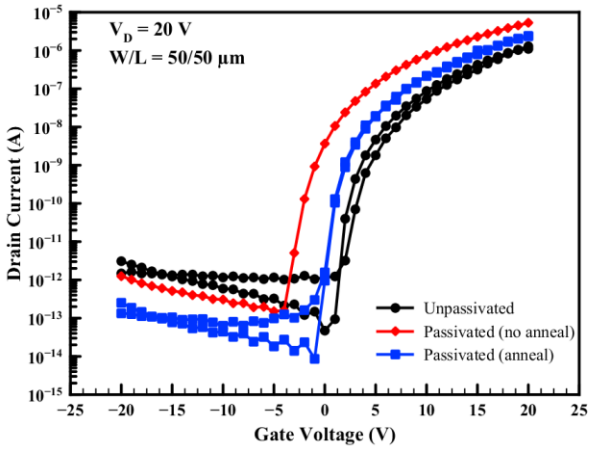

Figure 38. Transfer characteristics of unpassivated and passivated TFTs.

Table 12

Electrical characteristics performance of unpassivated and passivated TFTs.

Condition	I_D (A)	I_{ON}/I_{OFF}	V_{ON} (V)	SS (V/decade)	μ_{FE} (cm^2/V-s)
Unpassivated	$1.29x10^{-6}$	$1.4x10^7$	1	0.38	1

Table 12

Cont.

Passivated	$5.3x10^{-6}$	$3.3x10^{7}$	-4	0.66	2.9
Passivated (annealed)	$2.4x10^{-6}$	$2.8x10^{8}$	-1	0.48	1.8

The unpassivated device, have a turn-on voltage of 1 V, a field effect mobility of 1 cm^2/Vs, an ON/OFF ratio of $1.4x10^7$, and a sub-threshold slope of 0.38 V/dec. The passivated TFT without annealing presented good electrical characteristics, though V_{ON} has shifted negatively to -4 V, and SS has increased to 0.66 V/dec. After annealing in air at 200 ^oC for 1 h, helps to recover from the negative shift and additionally leads to a lower off-current by nearly two orders of magnitude, Von = -1 V, ON/OFF = $2.8x10^8$. This result has showed that the use of passivation layer, specifically SU-8 spin-coated, provides a good electrical characteristics that does not degrade the TFT operation, unlike passivation layer deposited by sputtering or e-beam techniques [1] which resulted in the bombardment of the substrate occurring during sputtering can break weak metal cation-oxygen bonds, generating oxygen vacancies. In addition, vacuum deposition techniques result on the largest negative shifts of V_{ON} after passivation, since some oxygen from GSZO's back surface can be removed during pump down time [35]. SU-8 is an epoxy-based negative photoresist that is used for fabrication of high aspect ratio features [36]. This improvement in the device is related to the non-vacuum deposition technique without physical substrate bombardment.

After passivation the device has shifted negatively, this suggests that the carrier concentration in the semiconductor has increased compared to the unpassivated device. This

negative shift has been shown to be related to the concentration of adsorbed oxygen on the semiconductor surface [37, 38]. As mentioned earlier in the unpassivated device the oxygen is physisorbed at the back surface, creating acceptor-like surface states that attract electrons from the semiconductor giving rise to a depletion region in the semiconductor that can extend from the GSZO surface to the SiO_2/GSZO interface [1]. However, with the help of the SU-8 passivation layer, the GSZO surface is no longer in contact with the atmosphere and oxygen adsorption is no longer taking place. The negative shift in the transistor can also be explained by the lack of fresh oxygen to feed the physisorption process in the previously adsorbed oxygen that have already bonded with the GSZO surface during the photolithography process.

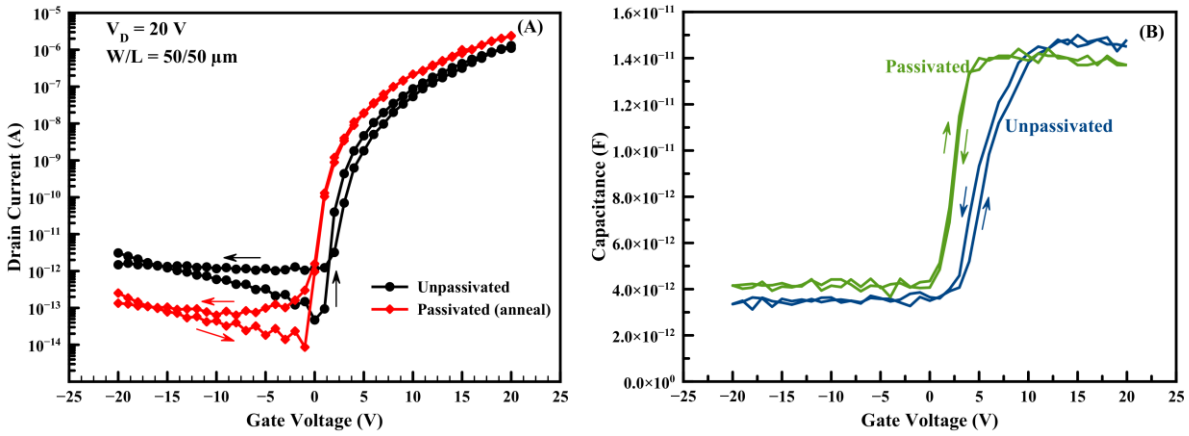

Figure 39. (a) Hysteresis transfer characteristics and (b) capacitance-voltage plot for unpassivated and passivated TFTs.

The hysteresis is almost vanished in the passivated device in comparison to the unpassivated, as shown in Figure 38(a). This hysteresis is always clockwise, being consistent with the typical and reversible charge trapping phenomena at or close to the insulator/semiconductor interface [39]. Likewise, C-V measurements also support this in Figure 38(b) showing lack of hysteresis in the passivated TFT. Fourier transform infrared (FTIR)

spectroscopy was not performed on this experiment but Olziersky et al. [39] has done similar experiment using SU-8 to observed the changes in the structure of the film before and after annealing. The analysis showed that after photolithography the SU-8 is not fully cross-linked, but after annealing at 200 ^{o}C the cross-linking has increased causing a large polymer network, which gives rise to a high stability and electrical resistivity. As observed from the Figure 37(b) after annealing V_{ON} has shifted positive to -1 V closed to the original control device (V_{ON}=1 V) and also a lower I_{OFF} current. This can be explained by photoacid generator (PAG), which is a photosensitizer when exposed to radiation, a strong acid is produced that initiates and catalyzes the cross-linking reactions. When the cross-linking is complete H^+ is not occupied in the catalyzation anymore and some of the cations that are found close to the GSZO/SU-8 interface can bond to the surface of GSZO by capturing electrons. This is verified by the positive shifting of V_{ON} after annealing. When this happen the anions of the acid (SbF_6^-) act as an excess fixed negative charge in the passivation layer, since there is a lack of H^+ to fix a zero net charge. This has been shown to only affect the off-state current [40]. This charge is negative and gives rise to a lower I_{OFF} current which is consistent with our observation.

4.3.1 Effect of negative bias electrical stability. Stability of the unpassivate and passivated devices was conducted for its stability mechanism. Negative bias gate stress was performed on the unpassivated and passivated annealed TFTs to investigate the degradation mechanism. Figure 40 shows the transfer characteristic of non-passivated and passivated TFTs when stress for 300, 600, 1800, 5400, and 10800 s.

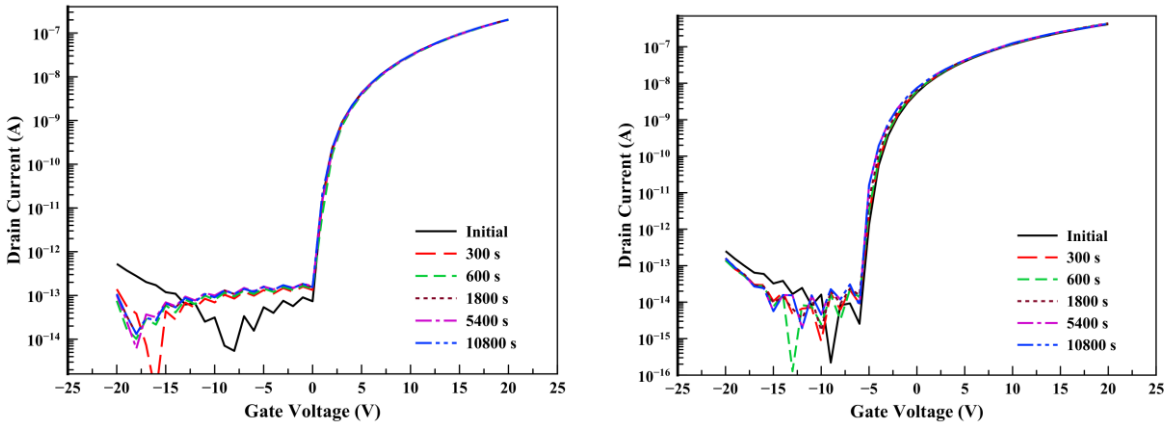

Figure 40. Negative bias stress test on (a) unpassivated and (b) passivated TFTs

The variation in the different device parameters during negative bias stress is observed in Figure 41. The V_{ON} of GSZO TFTs under dark condition was invariant after applying a negative gate bias stressing for 10,800 s. SS and μ_{FE} as well have negligible changes after stressing. Negative gate bias stressing is often reported to result in negligible changes in V_{ON}, SS, and μ_{FE} when the TFTs are stressed in the dark [41]. This indicates that under negative bias is applied to the gate, the transistor channel is depleted of electrons at the channel/dielectric interface and no mobile charges are available for the charge trapping and tunneling process [11]. For the passivated device the change in SS is smaller than the unpassivated device. This is plausible to say that the passivated TFTs charge trapping are at the insulator/semiconductor interface. It is to say that the passivated devices should have a low concentration of mobile ions, which is also consistent with the small or negligible hysteresis as verified in Figure 39.

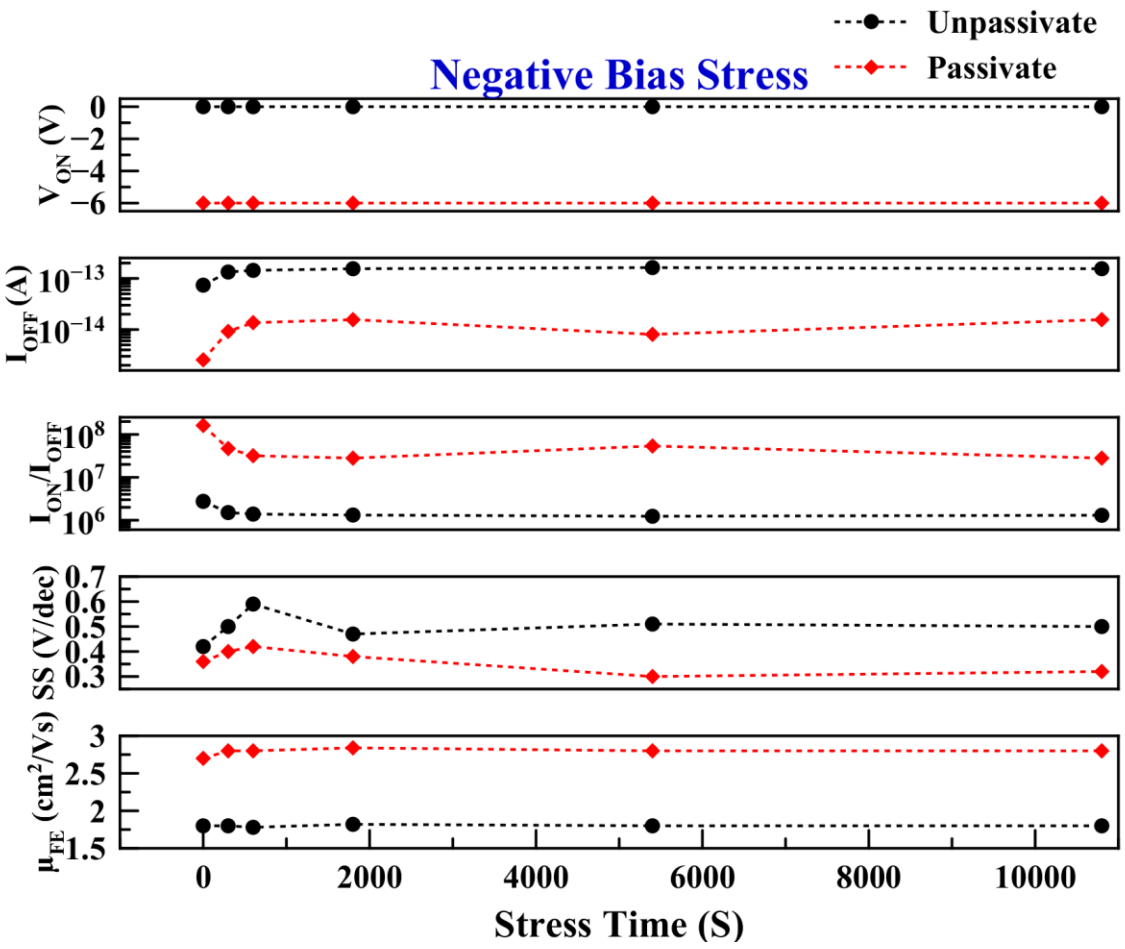

Figure 41. Variations of pertinent device parameters of unpassivated and passivated TFTs under negative gate bias stress.

To help further understand the mechanism of NBS, the energy band diagram is shown in Figure 42. At initial state, the energy bands are assumed to be flat-band as shown in Figure 42a. When a negative bias is applied at the gate, Figure 42b, the electrons in the channel are depleted of carriers for the charge trapping, thus creating a region of positive charges resulting in a upward band bending of the energy bands towards the interface.

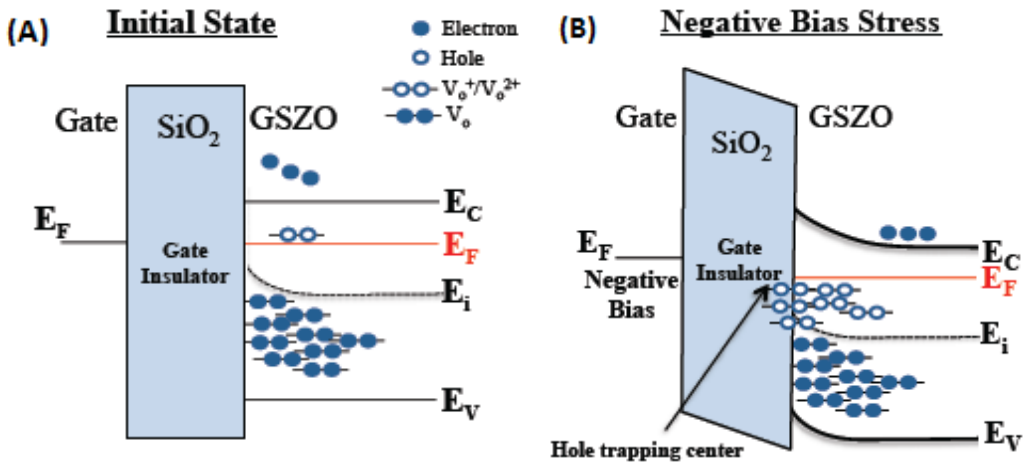

Figure 42. Illustrations of energy band diagram of GSZO TFTs at (a) initial and (b) NBS states.

4.3.2 Optical Stability

4.3.2.1 Effect of 410 nm wavelength stress. As previous mentioned in section 3.8.2 there were only small variations in the electrical performance in unpassivated device when the wavelength exceeds 500 nm and most photo-induced degradation of GSZO TFTs occurs under near ultraviolet illumination λ <500 nm, due to electron-hole pairs that are created by the photo-excitation originating from the valence band tail states as shown in Figure 43. Hence, the photo-induced degradation was carried out only for 410 nm to observe the effect of the unpassivated layer if any are present. Figure 44 shows the transfer characteristics when exposed to 410 nm wavelength for 3 hrs stress.

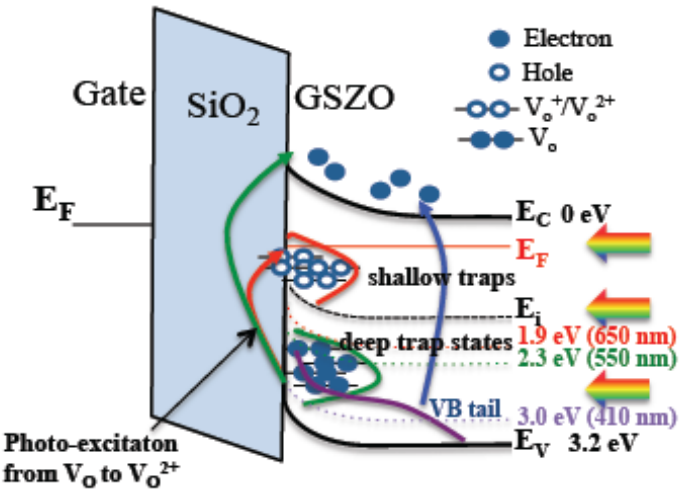

Figure 43. Schematic diagram of photo-excitation of electrons from V_O and VB tails state under illumination and creation of Vo^{2+} states.

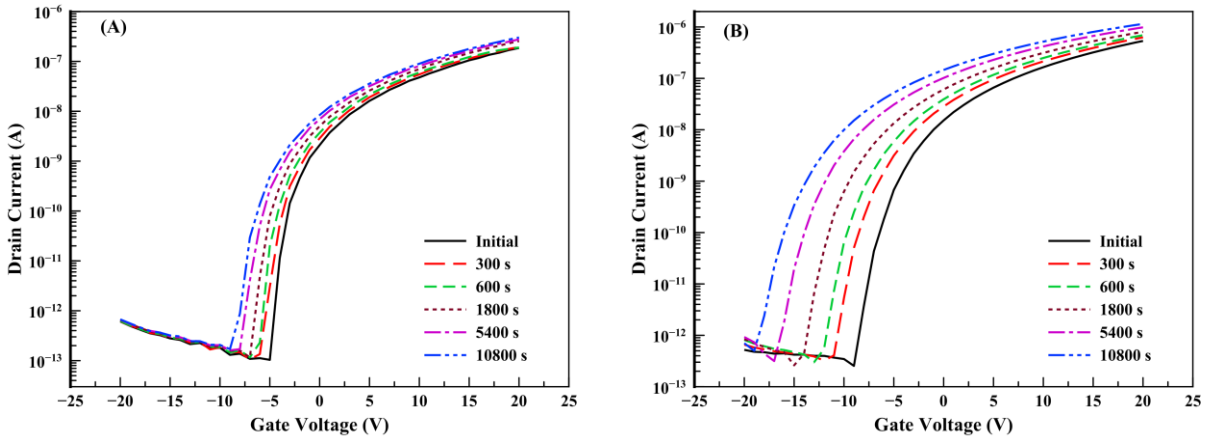

Figure 44. Transfer characteristics of 410 nm wavelength stress on (a) unpassivated and (b) passivated TFTs.

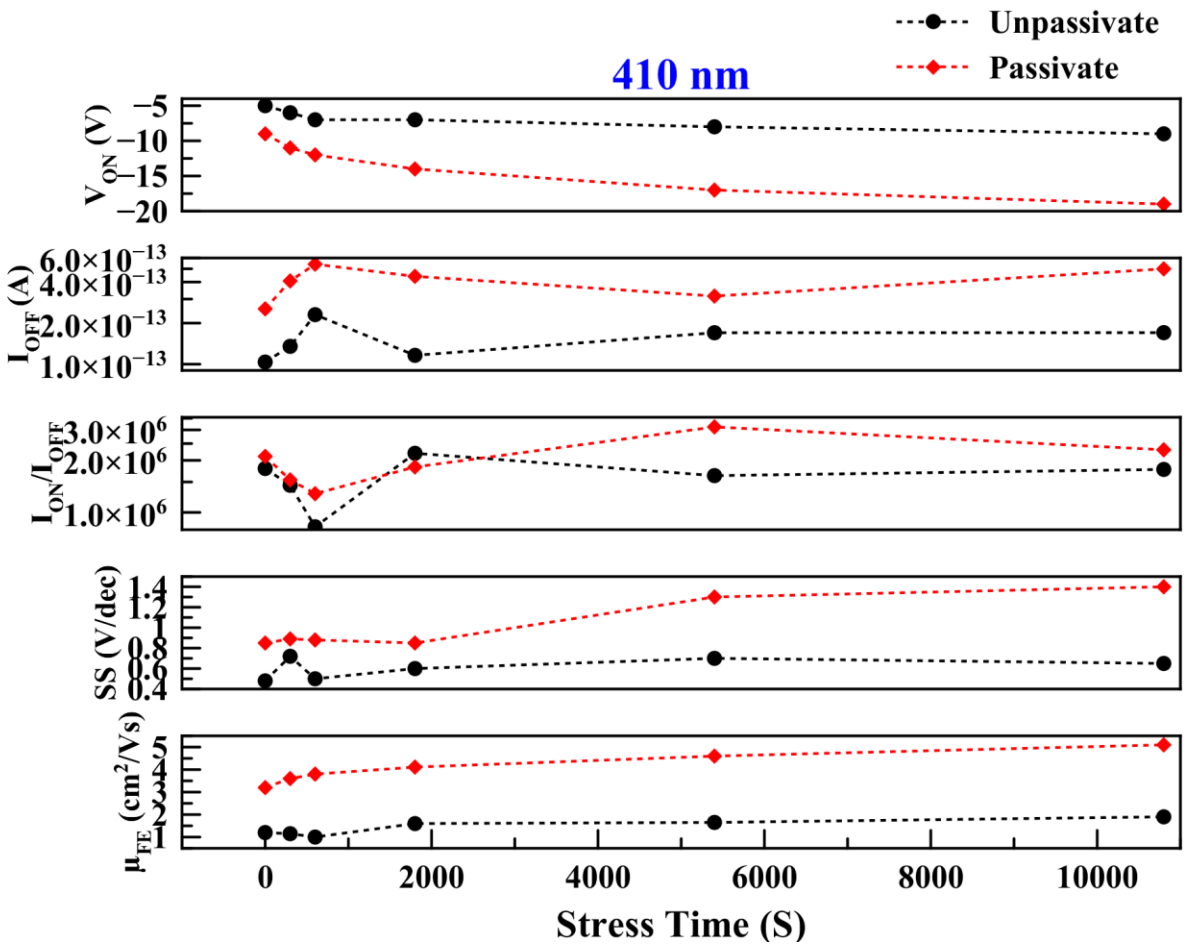

Figure 45. Influence of 410 nm wavelength on GSZO TFTs.

There was significant negative shifting of V_{ON} for both devices due to increased in carrier concentration in the channel accompanied by a large change in SS and μ_{FE}. As pointed out previously and previous work done by our group, this is not only due to a large density of deep traps, but also of valence band tail state because the photon energy, hυ = 3.02 eV, is in the valence band tail states region. The increased in I_{OFF} is also consistent with this fact for unpassivated and passivated TFTs as shown in Figure 45. This increase is speculated to the trapped positive charges (hole trapping) within the channel or/and at the SiO_2 /GSZO interface which is responsible for the increase in $I_{OFF.}$

4.3.2.2 Effect of negative bias illumination stress. The transfer characteristics of GSZO TFTs exposed to 410 nm wavelength with bias of -20 V is severely shifted negatively for both unpassivated and passivated GSZO TFTs as shown in Figure 46.

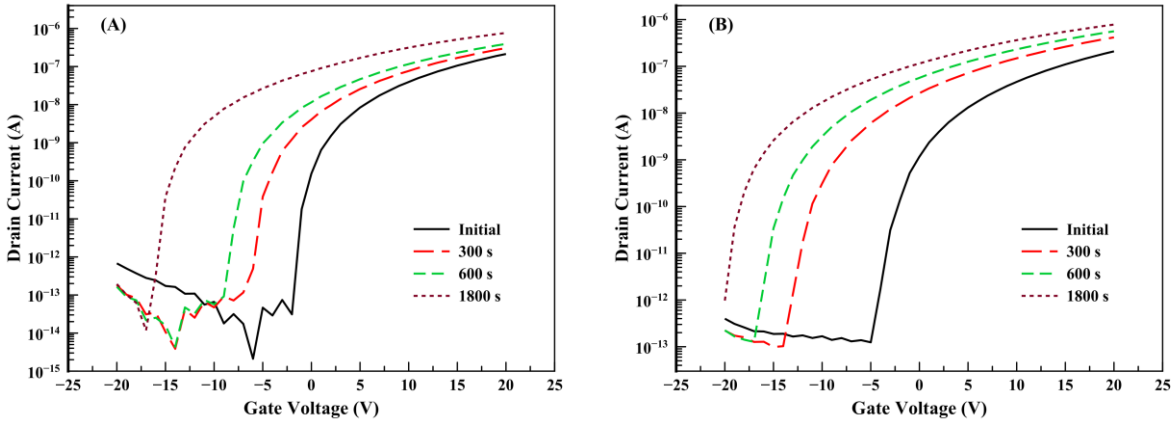

Figure 46. Transfer characteristics under -20 V bias with 410 nm illumination stress on (a) unpassivated and (b) passivated TFTs.

As observed in Figure 47, V_{ON} has shifted negatively for both devices being larger for the passivated device and is attributed to hole trapping in the gate insulator or at the gate insulator/channel interface [42], which resulted in the negative shift of the transfer characteristics. The illumination of light plays a critical role in hole trapping due to creation of excess electron-hole pairs and in the absence of losing the electrons to the bonding at the surface, all the electrons created contribute to the channel conductivity resulting in a larger negative shift in V_{ON} in the passivate device. All the other device parameters remained invariant unlike the unpassivated device.

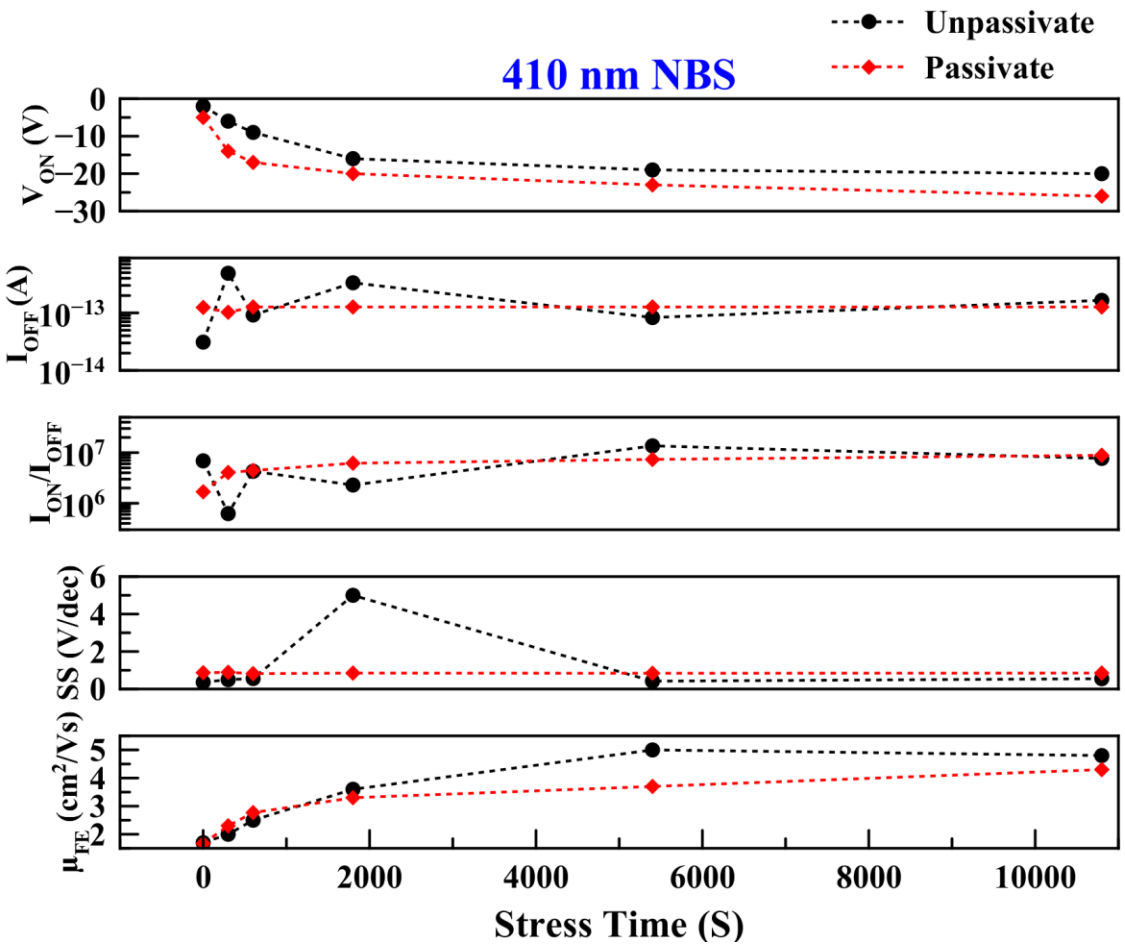

Figure 47. Influence of NBIS on GSZO TFTs.

4.3.2.3 Effect of 410 nm illumination stress on CV. The I-V measurements are complemented by the C-V charactersitics. The evolution of C-V curves to the 410 nm wavelength, NBS, and NBIS are plotted in Figure 48. All illumination stress test show a parallel negative shift in the C-V plot with NBIS showing largest shift. TFTs that were passivated with SU-8 show very small hysteresis loop compared to unpassivated TFTs for all illumination stress. This small hysteresis is clear indicative of reduction in the trap density present in this TFT.

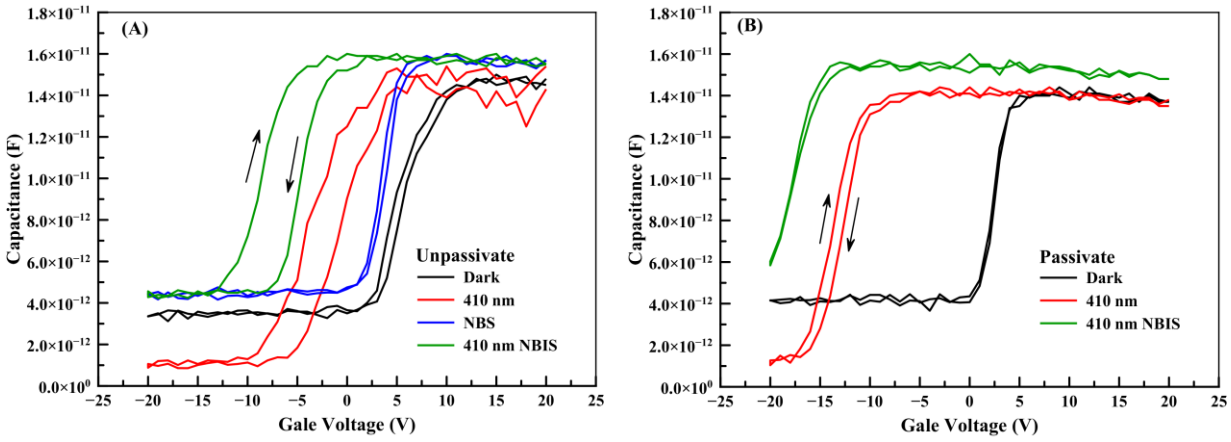

Figure 48. C-V measurements for (A) unpassivated and (B) passivated TFTs under various illumination stress.

There are salient differences between the C-V characteristics of the two devices. The passivated devices exhibit sharper transition from completion depletion to accumulation regions, which is consistent with the I-V data and are signatures of conductive channel. The parallel shift of the I-V and C-V characteristics under all wavelengths, except at 410 nm, are clear indicative of the traps states being predominantly located at the interface. The decrease in depletion region at 410 nm for both devices could be due to experiment error.

The most prominent difference between the two devices is the hysteresis. As observed in Figure 45, both devices showed a negative shift within 300s with degradation in both I_{OFF} and SS due to increase in carrier concentration. This is reflected in Figure 48 C-V measurement in the unpassivated devices with large density traps, indicated by the large hysteresis. There are clear reductions of hysteresis observed in the passivated devices under all wavelengths, which is indicative of less density traps cause by the passivated layer on the GSZO surface preventing the adsorption of oxygen.

CHAPTER 5

Discussion and Future Research

5.1 Discussion

In this work, the effect of oxygen flow, deposition contacts, forming gas, passivation layer and its electrical and optical stability have been studied to examined the performance of GSZO TFTs at 450 °C annealed. The following list examined the contribution from this research.

1. Increased in the annealing temperature from 140 °C to 450 °C showed a drastic improvement in the overall electrical performance due to lower density defects resulting in higher quality film with better semiconductor/insulator interface along with a higher density of Sn^{4+} in the 450 °C sample which is a contributing factor for the superior performance.
2. Both Al and Ti/Au electrode contacts showed good ohmic contact property and current saturation behaviors. Al contact has slightly better electrical performance in I_D, V_{ON}, and $\mu_{FE.}$ This increased in I_D with Al contact is attributed to the reduction of parasitic contact resistance between the electrode and channel layer.
3. Variations in oxygen flow from 2 to 10 sccm have shown a positive shift in V_{ON} with increasing oxygen flow along with reduction in I_D and μ_{FE}. This positive shift and reduction in μ_{FE} are suggested to be caused by the disorder that produces tail states in the vicinity of the band edge which was reported with increasing oxygen content the band gap decreases. Also, as Ga/O_I ratio increases the carrier concentration in the film is decreased because Ga is considered as scavenger of oxygen vacancies due to its strong bonding with oxygen. This was also consistent with the positive shifting of V_{ON}.

4. Reduction in the active layer thickness from 15 to 8 nm resulted in much performance improvement with V_{ON} improving (-9 V → 1V), SS decreasing (0.91 V/dec → 0.3 V/dec) and I_{OFF} decreasing ($1.3x10^{-12}$ → $1.1x10^{-14}$ A). This is all indicative of a decrease in defect density with decreasing channel thickness also supported from C-V data (not shown) showing a sharper slope from depletion to accumulation region. Furthermore, since the thinner channel is only a few nanometers thick, the surface depletion region forms a significant portion of the channel and hence the fully depleted region formed with the application of only a small gate voltage. This result in a positive shift in $V_{ON,}$ decrease in I_{OFF} and improvement in SS. However, I_D decreased by two orders of magnitude after reducing the channel thickness which is due to the presence of interfacial electron trap which becomes more significant thus capturing more free carriers.
5. Post oxygen annealing test have shown overall improvement in the electrical characteristics with an increased in both I_D and μ_{FE} and decrease in SS for both 2 and 10 sccm oxygen flow. In both cases it was observed that V_{ON} has shifted in the negative direction after exposing to oxygen with an increase in mobility. This is attributed to the reduction in the oxygen vacancies in the oxygen ambient, leading to a better I_D and improvement in SS.

   Exposing the samples to forming gas after POA presents degradation in the electrical performance with V_{ON} shifted heavily to the left to -26 V and no noticeable improvement in the electrical device.
6. Passivation layer using SU-8 presented good electrical performance, but V_{ON} shifted in the negatively at -4 V and SS has increased to 0.66 V/dec from the unpassivated device of V_{ON} = 1 V and SS = 0.38 V/dec. Annealing the passivated device in air at 200 °C for 1

h, helps to recover from the negative shift and leads to a better I_{OFF} by nearly two orders of magnitude, Von = -1 V, ON/OFF = $2.8x10^8$ and SS = 0.48 V/dec. C-V measurement also exhibited negligible to no hysteresis compared to unpassivated devices. Thus significant improvement achieved in the presence of the passivation layer is attributed to the lack of oxygen present in the ambient which is responsible for the degradation mechanism in these TFTs.

7. During NBS, there were no changes in V_{ON}, SS, or μ_{FE} for both unpassivated and passivated devices consistent with the reports in literature [41]. When a negative bias is applied to the gate, the transistor channel is depleted of electrons at the channel/dielectric interface and no mobile charges are available for the charge trapping and tunneling process. Compared to the unpassivated samples, the SU-8 passivation TFTs the change in SS is smaller. It is plausible to say that the passivation GSZO charge trapping are at the insulator/semiconductor interface. Also, the passivation devices should have a low concentration of mobile ions, which is also consistent with the negligible hysteresis as observed in the I-V characteristics.
8. From C-V characteristics, the passivated devices exhibit sharper transition from completion depletion to accumulation regions, which is consistent with the I-V data and are signatures of conductive channel. The parallel shift of the I-V and C-V characteristics under all wavelengths, except at 410 nm, are clear indicative of the traps states being predominantly located at the interface. The decrease in depletion region at 410 nm for both devices could be due to experiment error. Reductions in hysteresis are also observed for passivated devices for all wavelengths, indicative of lower density of traps, due to the passivation layer on the GSZO surface.

9. For NBIS, both non and passivated devices V_{ON} has shifted negatively which is suspected due to hole trapping in the gate insulator or at the insulator/channel interface. The illumination of light plays a critical role in hole trapping because it generate electron-hole pairs with the help of the subgap states. Unlike unpassivated devices, SU-8 passivation TFTs SS as well as I_{OFF} observe no changes which is reflected by C-V measurement showing sign of no hysteresis. The presence of passivation layer prevents further adsorption of oxygen at the GSZO surface.
10. Our data on the 8 nm thick obtained from this study (Table 13) with V_{ON} close to 0 V, $I_{ON}/I_{OFF} = 10^8$ and a good SS = 0.38 V/dec compares well with the best IGZO published work by Kawamura et al. [43] with V_{ON} = 0 V, SS = 0.082 V/dec, I_{ON}/I_{OFF} ratio of 10^8 and mobility of 3.1 cm^2/Vs obtained on a top-contact 6 nm thick IGZO TFTs with 100 nm PECVD-SiO_2 gate insulator. Thus, this work demonstrates GSZO based TFTs as promising viable option to the IGZO TFTs by further tailoring the film composition and relevant processing parameters.

Table 13

This study compared with best IGZO data.

	V_{ON} (A)	I_{ON}/I_{OFF}	SS (V/decade)	μ_{FE} (cm^2/V-s)
This Study	-3.5	10^8	0.38	4.36
Kawamura et al.	0	10^8	0.082	3.1

5.2 Future Work

Good electrical performance with stable optical stability test have been achieved in GSZO TFTs. Further investigation is required to achieve the level of performance comparable to current IGZO technology if GSZO is going to be the replacement in the future. Using SU-8 spin-coated as a passivation layer has greatly improved our overall device performance. Further investigation of using passivation layer is required to enhance the electrical and stability performance of the GSO TFTs devices. Further exploration of defect states should be explored through an in-depth photo-excitation analysis. Pulsed gate bias stress stability can also be investigated to further explore the degradation for GSZO TFTs in switching devices because the turn-off duration is much longer than the turn-on duration in periodic cycles of the gate pulse. Control over the deposition parameters is key part in improving the performance of GSZO TFTs as well as exploring different annealing ambient techniques. The addition of Sn concentration is another vital part in the GSZO target that would further tune the atomic concentration to improve the device performance. There are still many unexplored areas and issues remained to be explored. Overall, the fabrication of high performance TFTs using GSZO as the channel have been successful fabricated and tested and there is a bright future for the next generation GSZO devices display technology.

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Appendix

Publication & Presentations

N. Nguyen, B. McCall, R. Alston, W. Collis, S. Iyer, "*The Effect of Annealing Temperature on the Stability of Gallium Tin Zinc Oxide Thin Film Transistors*", to be submitted to Journal of Crystal Growth.

N. Nguyen, S. Iyer, "*High Performance Gallium Tin Zinc Oxide Thin Film Transistors by RF Magnetron Sputtering for Display Applications*" 4th Annual COE Graduate Student Poster Competition at North Carolina Agricultural and Technical State University, April 2015.

N. Nguyen, S. Iyer, "*Transparent Amorphous Gallium Tin zinc Oxide Thin Film Transistors by RF Magnetron Sputtering Deposition for Display Applications*" 2014 MRS/ASM/AVS Joint Symposium at North Carolina State University, November 2014.

N. Nguyen, B. McCall, R. Alston, J. Li, S. Iyer, "*A Comparison of the Stability of Low and High Temperatures GSZO TFTs*" 3rd Annual COE Graduate Student Poster Competition. North Carolina Agricultural and Technical State University, April 2014

N. Nguyen, B. McCall, R. Alston, J. Li, S. Iyer, "*Improved Characteristics & Bias Stress Stability of GSZO Thin Film Transistors on Annealing*" Poster Sessions at NAS Committee on Review of ARL Programs for HBCU/MI, North Carolina Agricultural and Technical State University, February 2014.

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