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Design And Implementation Of Millimeter Wave Frequency Multiplier In 65Nm Rf Cmos Technology

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Miss Sebsebie's thesis, *Design and Implementation of Millimeter Wave Frequency Multiplier in 65nm RF CMOS Technology*, was supervised by Dr. Numan Dogan.

To my loving parents, Mestewat Bekele and Sebsebie Waketola and

to my beloved Sister, Dagmawit. I'm forever in your debt

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Abstract

In this thesis, the design and implementation of frequency multipliers in 65nm CMOS was explored for millimeter wave oscillators and optimized to achieve higher output power and better rejection of the fundamental frequency. Several types of frequency multipliers are discussed. Transformers for AC-coupling used in the frequency multipliers were also explored. The design and optimization of the circuits was performed using Sonnet, Cadence, and ADS software tools.

In this work the design of a frequency multiplier which takes in a 12.5GHz signal and outputs 100GHz at the output is achieved. Three transformers are used for three stages of a frequency doubler to achieve a multiplication by eight. High isolation is achieved between the input frequency and the output. The output power level is –4dBm. The fundamental rejection is above 35dB. The power consumed by this frequency multiplier is 18mW. While multiplication of up to 4 is achieved in CMOS devices in other works, we are able to achieve a frequency multiplication of 8 in this work.

CHAPTER 1

Introduction

This thesis explores designing frequency multipliers in 65nm CMOS technology and how to reach the various figures of merit for the best design. In this chapter, the importance and purpose of frequency multipliers, as well as why CMOS technology is better than other technologies, is explained. Also, an overview of how and why frequency multipliers work is presented.

1.1 Motivation

As lower frequency bands become more and more congested, there is a push to explore the untapped higher frequency bands. These under-utilized bands are the terahertz frequencies that lie between the millimeter wave and infrared light, and range between 0.1 to 10THz. This frequency band is attractive for wireless communications because of the high bandwidth that can be obtained, potentially solving the problem of high mobile traffic and addressing the demand for ultrafast communication systems while meeting the ever growing demand for spectral resources [1], [2]. It also promises high data rates of above 10 Gbps [3]. In accordance with Edholm's law of bandwidth, over the last two decades, the demand for bandwidth has doubled every 18 months for short range communication [2]. As shown in Figure 1 according to Edholm, someday soon wireline communication will be a thing of the past [2], [4].

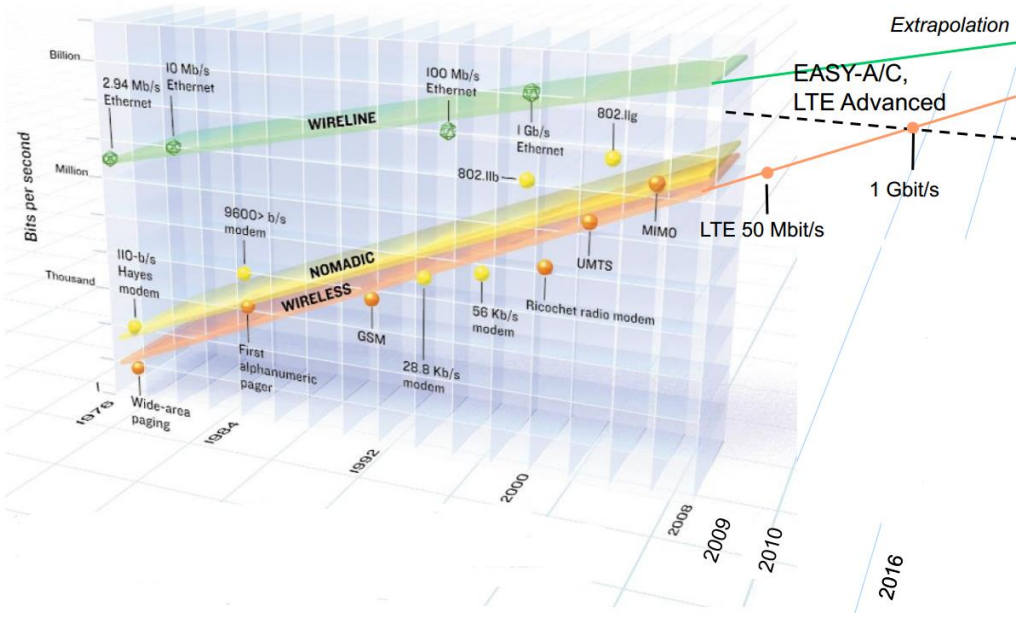

Figure 1. Edholm's law very similar to Moore's Law [2], [4]

Besides wireless communication, other applications demand high frequencies. One such application is in imaging and spectroscopy. High frequencies produce sharper images. The medical field is another arena for the application of these high frequencies since they are not harmful to soft tissue and would provide an alternative to X-rays and other imaging systems.

While their advantages are numerous, high frequencies are hard to achieve in electronics and research is on-going to bridge the gap between theories that have already been developed for high frequencies to the tools needed to realize high frequency applications. There are limitations in semiconductor devices which prevent hardware design for ultra-high frequencies but because the demand for high frequencies persist, research groups continue to develop new designs to achieve electronic devices that can facilitate high frequency applications.

To meet this demand, Electrical Engineers have attempted to use various means of achieving high millimeter wave and terahertz frequencies. Although optoelectronic devices,

quantum cascade lasers (QCL) and other Nano-devices have been explored to produce these high frequencies, they do not possess the advantages of silicon devices [1]. Silicon devices are cheap and readily available. They are not as bulky as some of the alternative devices and they can function fairly well in uncontrolled environments [1]. Additionally, as frequency increases, implementation of oscillators becomes plagued by phase noise and instability. Cascading a low frequency oscillator with a frequency multiplier is a way to solve this problem [5].

1.2 Overview of Frequency Multipliers

Frequency multipliers are devices that utilize the innate non-linear characteristics of semiconductors to realize frequency multiplication [6]. These nonlinear characteristics can be understood by examining the following power series as presented in [6]:

$$I = a_0 + a_1V + a_2V^2 + a_3V^3 + \cdots \tag{1}$$

Assuming *V* is the input signal,

$$V = V_1 cos(\omega_1 t) \tag{2}$$

the currents resulting from the power series are:

$$i_1(t) = a_1V = a_1V_1 cos(\omega_1 t) \tag{3}$$

$$i_2(t) = a_2V^2 = a_2V_1^2 \cos^2 \omega_2 t = \frac{1}{2}a_2V_1^2(\cos 2\omega_1 t + 1) \tag{4}$$

$$i_3(t) = a_3V^3 = a_3V_1^3 \cos^3 \omega_1 t = a_3V_1^3 \left(\frac{3}{4}\cos \omega_1 t \ + \frac{1}{4}\cos 3\omega_1 t\right) \tag{5}$$

As can be seen from these current equations, the harmonics begin to emerge as we continue in the power series. The role of the frequency multipliers is to extract the desired harmonic of the fundamental and deliver it at the output while suppressing all other frequencies.

Frequency multipliers have an input at a low frequency f_0 produced by an oscillator and by their non-linear characteristics are able to produce Nf_0 frequency. The output frequency is a

harmonic of the fundamental frequency f_0. Ideally the fundamental frequency is suppressed by the circuit such that only the desired frequency is seen at the output. A spectrum analysis will show that this does not happen in reality as the unwanted fundamental frequency is not cancelled out entirely. One of the goals of design is to achieve a high fundamental frequency rejection. Additionally, frequency multipliers introduce phase noise to the circuit since they actually multiply phase of a signal to achieve higher frequencies [7, 8]. The more frequency multipliers placed in cascade, the higher the phase noise as can be seen from the so called carrier to noise (CNR) degradation for an ideal frequency multiplier given as

$$\Delta\, CNR = 20\, log_{10}(n) \tag{6}$$

where n is the multiplication factor [7].

There are two categories of multipliers that we can use; passive multipliers and active multipliers. The passive multipliers make use of passive components and devices while active multipliers use active components. Passive devices that can be used are resistive diodes such as Schottky barrier diodes, nonlinear capacitance diodes such as varactors and step recovery diodes while active components include bipolar transistors and FETs [8].

Another component that is essential in the implementation of many multiplier topologies are transformers and inductors. Since they are passive components, inductors and transformers need to be modelled and simulated accurately for the best inductance, quality factor and self-resonant frequencies [9]. Transformers are modelled in Sonnet and parasitic extraction is performed in ADS using fitting techniques with a network of resistor, inductor, capacitance and conductance (RLCG) models. These values are then used in Cadence to model the behavior of the transformers with a circuit chosen to characterize different geometries and topologies. This enables us to identify which geometry will be the best to use in our multipliers.

By analyzing the topology of the circuit, the category, active or passive, and the transformer geometries we attempt to achieve the best multiplier that is possible and design it in 65nm CMOS technology. Although other technologies have been pursued in other research (GaAs, QCL), CMOS technology remains the cheapest way to implement high frequency circuits [1]. What remains is finding the best design that will reach the advantages of the alternatives while enjoying the low cost of CMOS devices.

1.3 Thesis Organization

Chapter 2 looks at the passive and active circuit components for the two different categories of frequency multipliers and their analysis. Chapter 3 explores the transformer geometries and their corresponding models. In chapter 4 multi-stage doublers are presented. Finally, chapter 5 discusses our conclusions and further work.

1.4 Summary

In this chapter the motivation behind designing frequency multipliers in 65 nm CMOS technology is presented. Since demand for higher bandwidth persists and increases in accordance with Edholm's law, devices are needed that can facilitate high frequencies. Frequency multipliers can be used to achieve such devices. Additionally, an overview of how frequency multipliers function was also given. They work mainly because semiconductor devices are non-linear and give rise to harmonics which can be extracted to multiply the frequency of a signal.

CHAPTER 2

Frequency Multipliers: Active and Passive

There are two main categories of multipliers that can be used, namely, active and passive. Active multipliers use active circuit components while passive components are used in passive multipliers. There are advantages and disadvantages that are encountered in both. A discussion of both categories is presented in this chapter.

2.1 Passive Frequency Multipliers

Passive multipliers make use of the non-linear behavior of passive circuit components. In this category, diodes and varactors are used to accomplish frequency multiplication. Passive multipliers are expected to have high-order multiplication, low noise and broad bandwidths and are either resistive multipliers or capacitive multipliers [8]. Passive devices that we will look at include resistive diodes (Schottky-barrier diodes) and nonlinear capacitors (varactors).

2.1.1 Resistive Frequency Multipliers

A resistive diode distorts a sinusoidal waveform generating harmonics; the higher the distortion, the higher the number of harmonics that result from the circuit [8]. Figure 2 shows a Schottky diode frequency doubler that takes 100GHz and outputs 200GHz. The resulting waveform is shown in Figure 3.

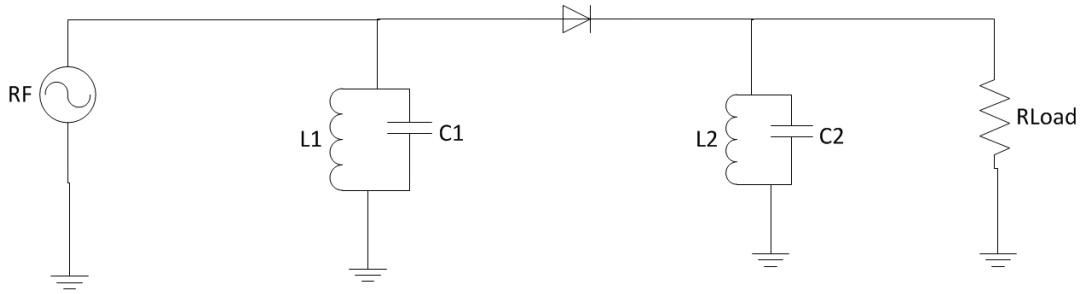

Figure 2. Schottky barrier diode as a frequency doubler schematic.

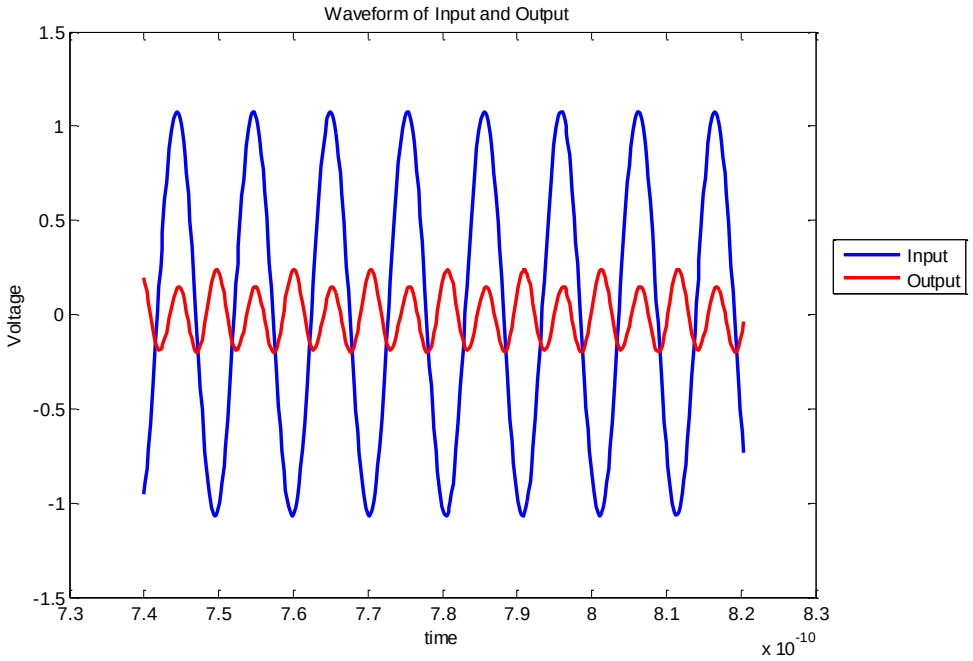

Figure 3. Output of the doubler circuit.

The diode in Figure 2 is flanked by two LC tanks that are tuned to the appropriate frequencies. The first LC tank near the input is tuned to the fundamental frequency and the other LC tank is tuned to double the fundamental frequency. The LC tanks are shorts for every other

frequency except for the frequencies that they are tuned to. This ensures that other harmonics of the fundamental frequency do not go into the diode or appear at the output.

The conversion loss of a resistive doubler as can be seen from the waveforms is quite high. The optimum efficiency of a resistive passive multiplier is to the order of $1/n^2$ where n is the harmonic number [8]. For a doubler, the conversion loss is therefore 6 dB. Although they are inefficient, resistive diodes exhibit higher bandwidth than capacitive diodes.

2.1.2 Varactor Multipliers

The nonlinear reactances of capacitive diodes (varactors), which have a voltage controlled depletion capacitance, distort sinusoidal signals. Varactor multipliers exhibit higher efficiency and higher power output compared to resistive multipliers but they are narrowband and extremely sensitive to circuit parameters which makes them tedious to implement [8]. Varactors can only generate second harmonics in an efficient manner and are therefore successful in only achieving doublers and need idler circuits to realize other multiplications of the fundamental frequency [8]. The chief reason that varactors are still in use today is the fact that they generate very little noise compared to the more popular GaAs MESFET multipliers [7]. However, they still have the high conversion loss that passive components are rejected for.

2.2 Active Frequency Multipliers

Active multipliers have several advantages over passive multipliers. Firstly, they have much high conversion gain and are therefore more efficient [7]. In addition, they are broadband and power efficient in dc to RF conversion [7]. The non-linear active components used are FETs and BJTs. They realize efficient multipliers and dissipate very little heat in comparison with the

passive components. We examine class B implementation of active multipliers where we do not necessarily have an output that is high power. The objective is to obtain the high frequency and amplifications can be obtained after this stage.

A simple active frequency multiplier consisting of a MOSFET and RLC tank is illustrated in Figure 4 below to outline how it works.

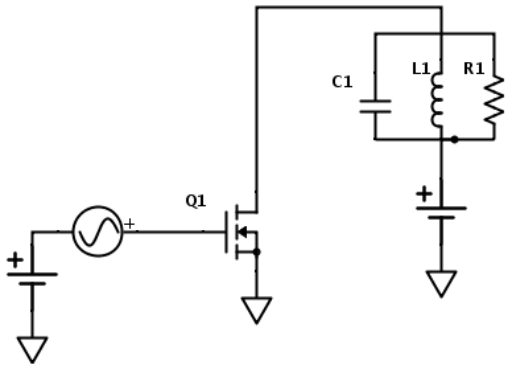

Figure 4. Simple Active Frequency Multiplier

The gate bias is kept close to the threshold voltage of the transistor so that it is operating close to the cutoff region. As the signal swings up and down, the transistor will turn on and off at the frequency of the signal. When the transistor turns on the capacitor is charged up and when the transistor turns off when the signal goes below the threshold voltage, the capacitor discharges through the resistor, creating additional swings at the drain of the transistor. The frequency of the output wave depends on frequency that the RLC tank is tuned to.

$$f_n \approx \frac{1}{2\pi\sqrt{LC}} \tag{7}$$

The non-linearity of the transistor creates harmonics from the pure sine wave input and the RLC tank acts as a short of all other frequencies except the one that it is tuned to. The frequency of interest which is a multiple of the fundamental is also a harmonic. This is multiplication via harmonic extraction.

Another method is illustrated using Figure 5 where the transistors act as switches and the result is a doubling of the frequency at the output.

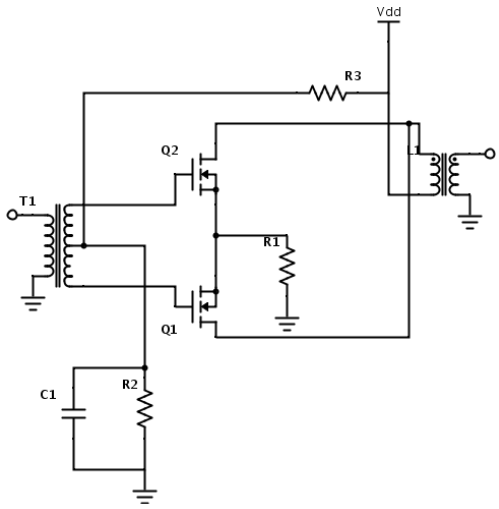

Figure 5. Frequency doubler in push-push configuration [10].

The input signal is at the transformer node and is coupled to the two transistors. When the voltage at Q2 is high, the input at Q1 is low. This means that the transistors switch on and off at different times but since their drains are connected to the top of the output transformer, their currents push through in the same direction in the inductor coil they are tied to. For this reason, the frequency seen at the output is twice the frequency at the input. This particular configuration ensures that all odd harmonics including the fundamental are suppressed [10].

2.3 Summary

In this chapter, we looked at the two different categories of multipliers, namely, passive multipliers and active multipliers. While passive multipliers make use of diodes and varactors, active multipliers use MOSFET's and BJT's for their non-linear elements. We examined the merits and demerits of each category to demonstrate why we choose to use active multipliers.

Although passive multipliers have greater bandwidth, they are found to have low conversion gain. Active multipliers on the other hand are efficient and dissipate less heat than passive multipliers. Our implementation makes use of active multipliers.

CHAPTER 3

Modelling Transformers

Transformers are essential in various integrated RF circuits and are used as impedance matching networks, for DC biasing and AC coupling [11]. They are also used to convert from single ended to double ended outputs [11]. They are used in power amplifiers, mixers and oscillators. To implement our frequency multipliers, we use transformers for AC coupling and single to differential transformation [5].

In this chapter we examine the transformers to be used in our frequency multipliers. We study the figures of merit for different geometries and show the EM simulation of their layout. The transformer layouts are designed in Sonnet simulation software using 65nm TSMC technology substrate stack. Coils of the transformer occupy the two topmost metals, Metal 8 and Metal 9. A 3D EM simulation is performed and transformer characteristics are plotted and examined. Transformers are then optimized for the figures of merit such as high transmission gain, high Q-factor and the required self-resonant frequencies desired for the final design.

To design and simulate the frequency multipliers we require a circuit model of the transformer. Several transformer circuit models exist in the literature as found in [12, 13, 14] that can be used but we choose one that is suitable for the frequencies that we are targeting. A circuit model as described in [11] is used where the parasitic resistances, inductances and capacitances (RLGC) are obtained by calculations based on the geometric and technological parameters of the transformer. Since this model is suitable for operations of up to 110 GHz, and our target for the design is to achieve a multiplier that can get to 100 GHz, we can use it successfully. Once RLGC values are obtained, they are tuned further to fit the S-parameter plots of the transformer's EM simulations.

As mentioned earlier, the parameters of importance are the quality factor of the transformer, the inductance, the transmission gain and the self-resonant frequency. Different factors lead to losses that degrade these parameters and various ways are used to ensure that they are minimized. One factor is the geometry of the transformer. For instance, rectangular transformers experience power loss due to the sharp turns which results in lower Q-factor [5]. For this reason, we limit ourselves to octagonal transformers. We also use a stacked structure because it enables stronger magnetic coupling between the primary and secondary coil [11]. Stacking also reduces the area occupied by the on-chip transformers which is desirable in integrated chips [11]. In the next section we examine transformer layouts with different radii and width and their corresponding characteristics.

3.1 Transformer Structure

The layout of the transformer is performed in Sonnet Software and appears as shown in Figure 6 below. The secondary coil has a center tap for biasing the circuit. The primary coil is implemented on Metal 9 while the secondary coil is implemented in Metal 8. We examine transformers with inner radii of 100um, 60um, and 50um. For the transformer with radius 50um we look at different widths, 10um, 15um and 20um.

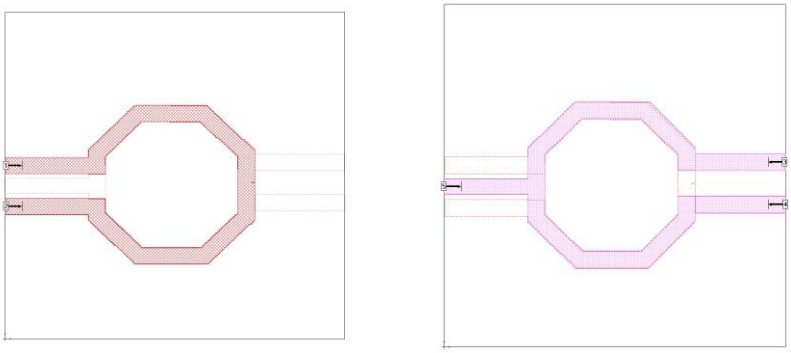

Figure 6. Octagonal stack structure a) Primary coil b) Secondary coil with center tap

3.1.1 Effect of Increasing Inner Radius.

In Figure 7 below we see how self–resonant frequencies (SRF) change with radius. This means that the choice of the transformer size is highly dependent on the frequency of operation desired. As the frequency of operation increases, the transformer size needs to decrease in radius. Beyond the self-resonant frequency, the transformer's capacitive coupling is stronger than the magnetic coupling and the transformer will no longer be reliable. Thus it is crucial to ensure that the SRF be higher than the frequency at which the transformer will be operated. The SRF can be found by plotting the return loss or transmission gain and finding the frequency corresponding to the maximum return loss or transmission gain. The transformers and the SRF of each are summarized in the table below. A trend that is seen here is that as the transformer increases in size, the SRF decreases.

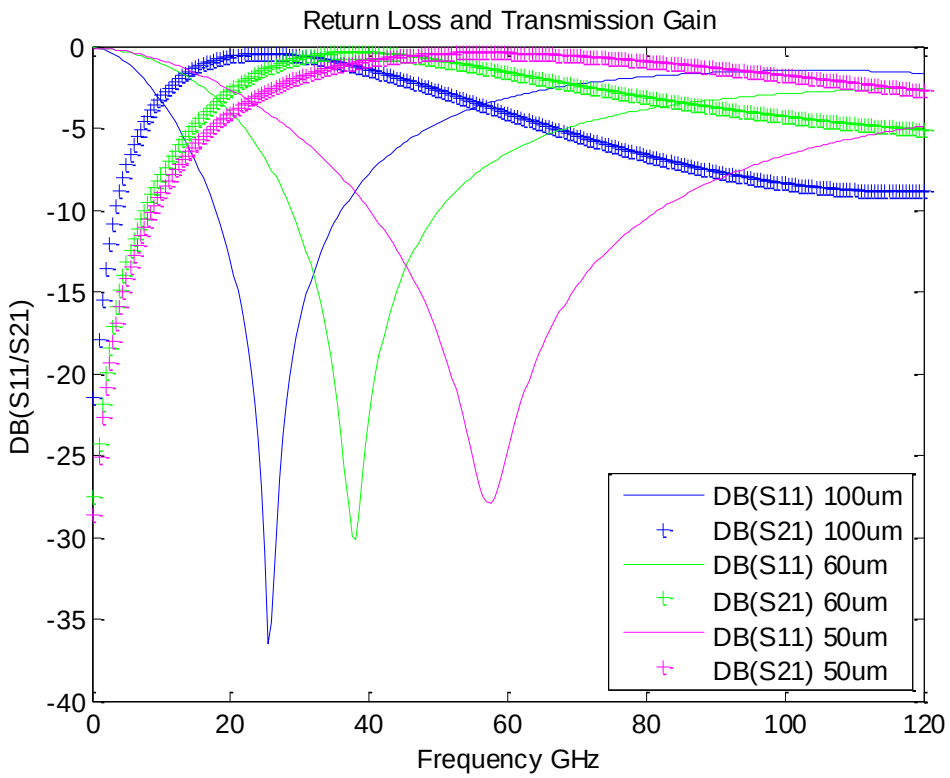

Figure 7. S-parameter plots showing the SRF of the different transformers

Table 1

Transformer and corresponding SRF

Inner Radius	Self-Resonant Frequency SRF
100 um	25.5 GHz
60 um	38.5 GHz
50 um	57.5 GHz

We also examine another figure of merit, the Q-factor of the transformers with increasing inner radius. While there is no trend that can be seen in Figure 8, the biggest transformer does exhibit higher Q-factor values than the smaller two transformers. Q-factor will generally decrease with increase in frequency in on-chip transformers.

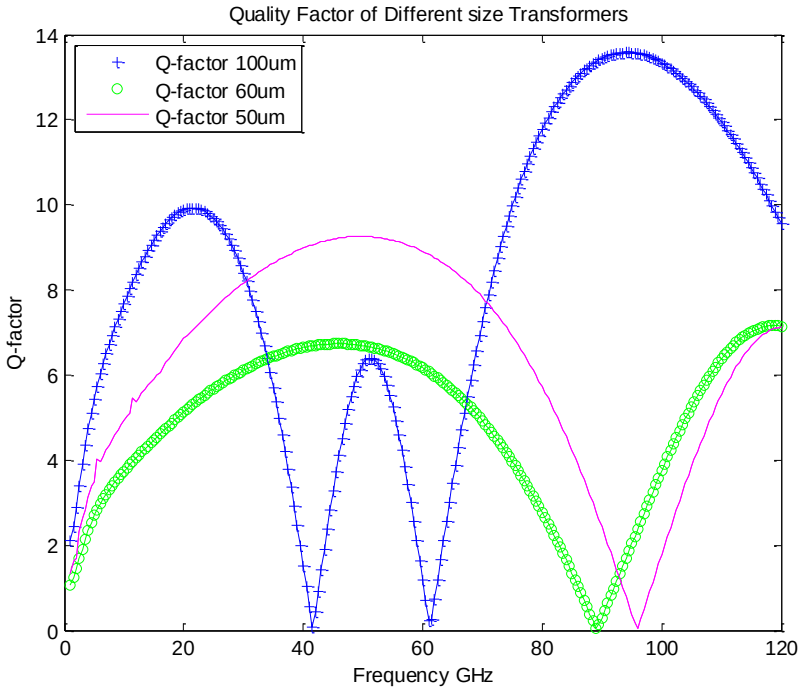

Figure 8. Q-factor plots of the different size transformers

3.1.2 Effect of Varying Width

Using the transformer with IR, 50um, we examine the change in characteristics of the transformer with width. We first look at the SRF of different width transformers. Figure is a plot of the transformers with different widths.

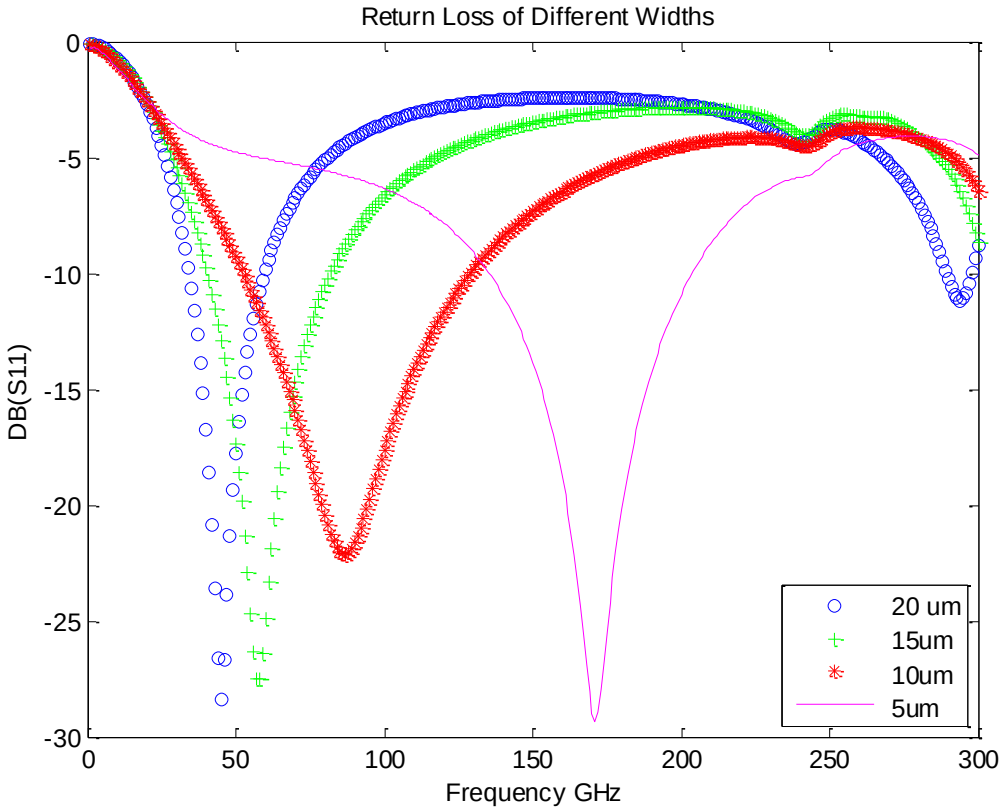

Figure 9. S-parameter plots showing the SRF increasing with decrease in width.

As we can see from the plots above, the SRF of the transformer increases with decrease in width. The formula for approximating SRF is shown in equation below.

$$f_{SRF} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \tag{7}$$

Therefore an increase in inductance and/or capacitance will result in a higher SRF. Looking at the inductance plots in Figure 10 gives insight into the validity of the trend with SRF as well. The plots show that as width of the transformer is increased, the self-inductance of the transformer decreases for the bandwidth that we are interested in which up to about 100 GHz.

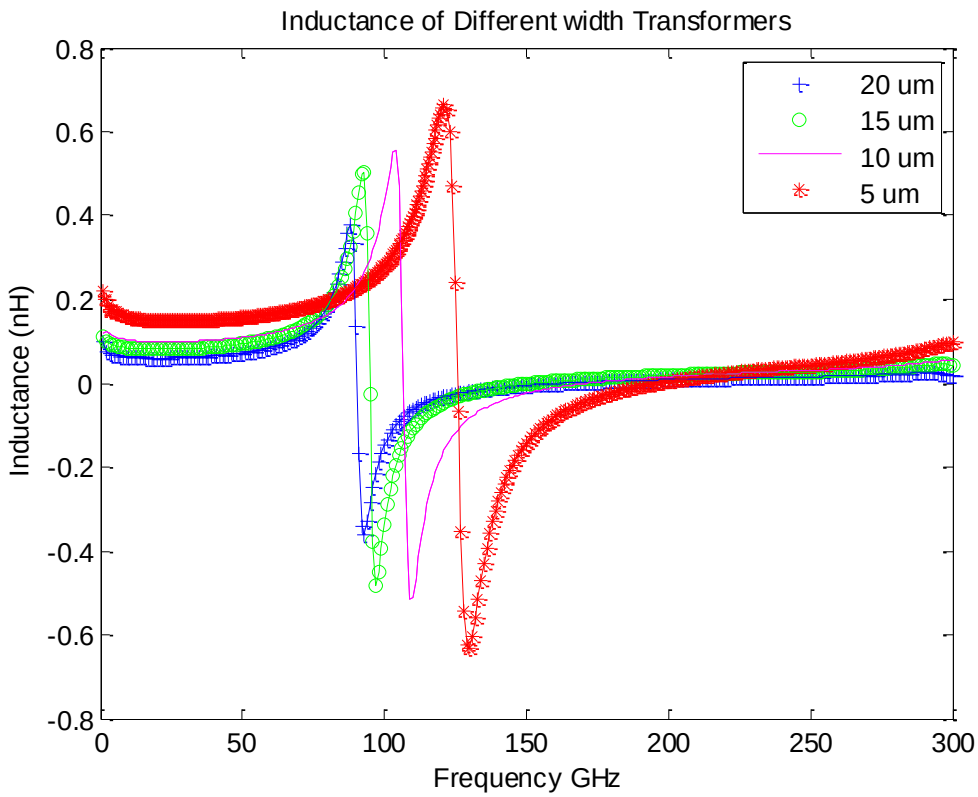

Figure 10. Inductance of the transformers showing a trend with increase in width

3.2 Transformer Circuit Model

In order to simulate these transformers in multiplier circuits, it is essential to get a model that most closely approximates them. While there are several models that exist in literature, very few models can fit the parasitic network of a transformer at high frequencies. Looking at the work in [11], we adopt the circuit model proposed and implement it since it shown to work up to 110GHz. Physics based equations are used to obtain a close approximation of all the elements in the circuit [11] and will be explored here. The model is shown in Figure 11.

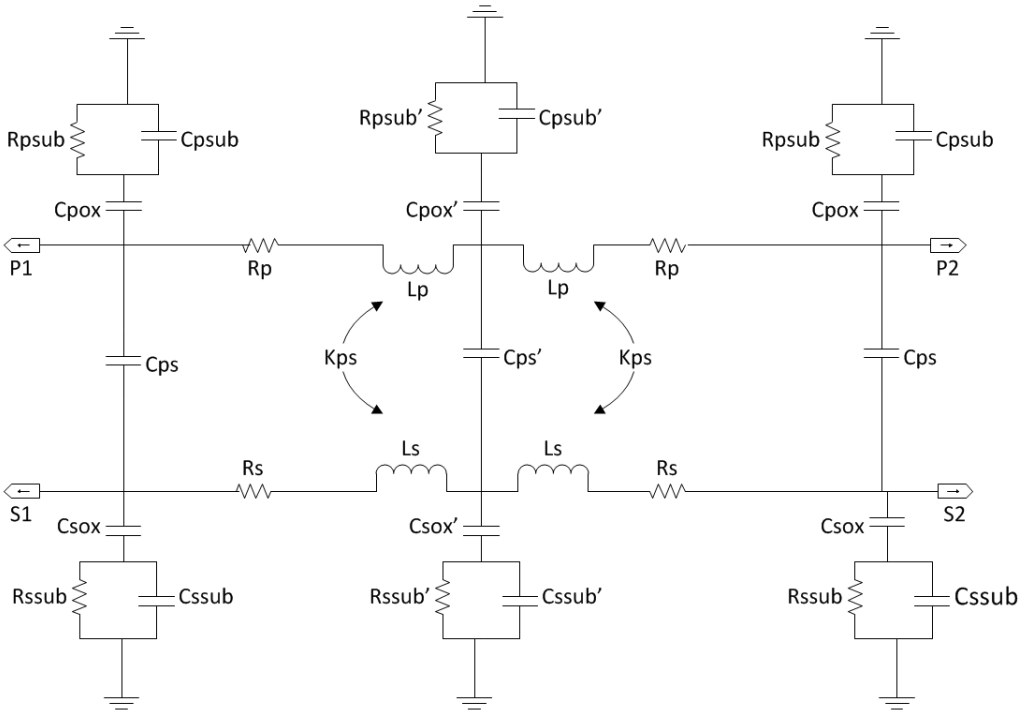

Figure 11. Circuit model diagram as proposed in [11]

As shown in Figure 11 and as discussed in [11], we have the series elements, R_p, R_s, L_p and L_s, the substrate branches, R_{sub}, C_{sub} and C_{ox}, and the coupling elements, C_{ps} and K_{ps}. The technological and geometrical parameters used to determine these values are given in *Table 2*. The equations used to calculate the parasitic elements proposed in [11] are summarized below.

$$L_p = Ind(l_p) - Mut(feed_{intP}) - Mut(d_{intP}) \tag{8}$$

$$L_s = Ind(l_s) - Mut(feed_{intS}) - Mut(d_{intS}) \tag{9}$$

$$Ind(l, W, t) = \frac{0.42 * \mu_0}{\pi}\, l \left[ln\left(\frac{2l}{GMD(W,t)}\right) + \frac{GMD(W,t)}{l} - 1 \right] \tag{10}$$

Table 2

Geometric and Technological Parameters

l_p	Length of primary coil	t_p	Thickness of the primary coil
l_s	Length of secondary coil	t_s	Thickness of secondary coil
W_p	Width of primary coil	t_{si}	Thickness of substrate
W_s	Width of secondary coil	d_{ps}	Distance between primary and secondary
A_p	Primary area	ε_{oxP}	Permittivity of dielectric between substrate and primary
A_s	Secondary area	ε_{oxS}	Permittivity of dielectric between substrate and secondary
A_{ps}	Area overlap between primary and secondary coil	ε_{oxPS}	Permittiveity of dielectric between secondary and primary
h_p	Distance between substrate and primary coil	ε_{si}	Permittivity of substrate
h_s	Distance between substrate and secondary coil	ρ_{MP}	Primary metal resistivity
t_p	Thickness of the primary coil	ρ_{MS}	Secondary metal resistivity
		ρ_{Si}	Substrate resistivity

$$GMD(W,t) = 0.2235\ (W + t) \tag{11}$$

Series resistance values are calculated as shown below where the resistances due to the geometry of the conductor as well as the skin resistance are considered.

$$R_p = R_{Pdc} + R_{Pac}\,, \qquad R_s = R_{Sdc} + R_{Sac} \tag{12}$$

$$R_{Pdc} = \frac{\rho_{MP} l_p}{W_p t_p}, \qquad R_{Sdc} = \frac{\rho_{MS} l_s}{W_s t_s} \tag{13}$$

The skin resistance which is frequency dependent is calculated as shown below.

$$R_{Pac} = \frac{k_{Rac}\,\rho_{MP}\,l_p}{\left(1+\frac{t_p}{W_p}\right)\delta_p[1-exp\left(-\frac{t_p}{\delta_P}\right)]}, \qquad R_{Sac} = \frac{k_{Sac}\,\rho_{MS}\,l_s}{\left(1+\frac{t_s}{W_s}\right)\delta_s\left[1-exp\left(-\frac{t_s}{\delta_s}\right)\right]} \tag{14}$$

The branch parasitic capacitances and resistances are calculated as shown below. The variables $\mathrm{Cap_{par}}$ and $\mathrm{Cap_{fr}}$ are parallel and fringe capacitances respectively.

$$C_{pox} = k_{cap}\left[\,Cap_{par} + \left(\frac{A_p - A_{PS}}{A_p}\right) Cap_{fr}\right] \tag{15}$$

$$C_{sox} = k_{cap}\left[\,Cap_{par} + Cap_{fr}\right] \tag{16}$$

$$R_{Psub} = \frac{k_{rsub}\,W_p\,\rho_{Si}}{l_p\,t_{Si}}, \qquad R_{Ssub} = \frac{k_{rsub}\,W_s\,\rho_{Si}}{l_s\,t_{Si}} \tag{17}$$

$$C_{Psub} = \frac{\varepsilon_{si}\rho_{Si}}{R_{Psub}}, \qquad C_{Ssub} = \frac{\varepsilon_{si}\rho_{Si}}{R_{Ssub}} \tag{18}$$

The coefficient *k* with various subscripts is a model weighting factor [11]. The coupling elements are calculated as follows.

$$C_{ps} = k_{cap}\,Cap_{par} \tag{19}$$

$$M = k_M[Mut(primary, Secondary)] \tag{20}$$

The variable $Mut(i,j)$ is the mutual inductance calculated by considering the dimensions and positions of the conductors of the transformer [11].

To implement our frequency multiplier we use the transformer with 100 um radius for the first stage, 50 um for the second stage and 40 um for the third stage. The width of each transformer is 20 um, 15 um and 8 um respectively. Since we are using only one turn transformers, some of the equations shown are modified from the original for a single turn stacked transformer. Once the parasitic RLCG values for each transformer are obtained, an S-parameter fitting is done in ADS software. While the model approximated the transformers well, the error margins were high and a modification was done to have a circuit model that would fit better. This modification took into consideration the eddy current losses in the substrate modeled in a resistor and inductor loop as shown in the Figure 12 below [13].

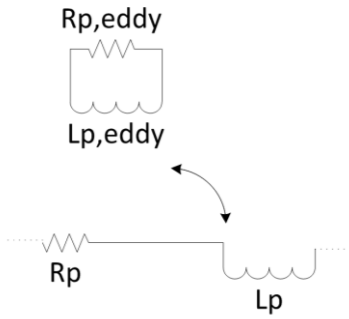

Figure 12. Eddy current loss model

Addition of the eddy current model in Figure 12 gives a complete representation as it signifies the eddy current losses that occur at high frequencies. Eddy current losses become significant especially at higher frequencies and should be included in the model. The final transformer model with both the 2π model and eddy current elements is shown in Figure 13.

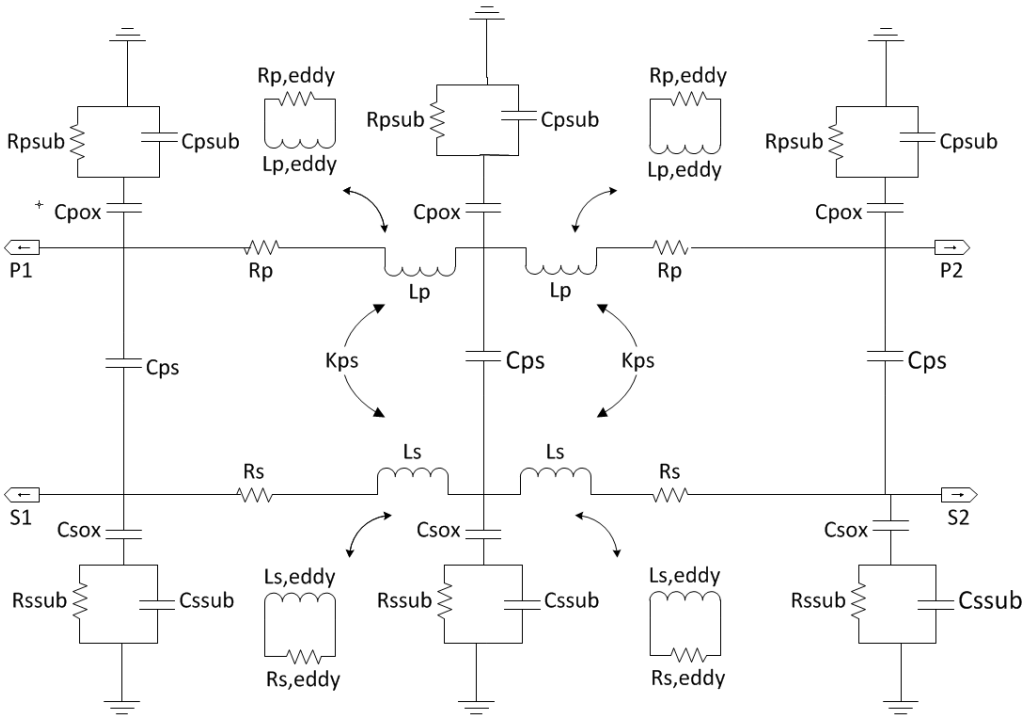

Figure 13. Final Transformer Model with eddy current loss circuit modification

The model in Figure 13 is used as a representation of the transformer in the circuits that are set up for simulation and optimization of the frequency multiplier.

Using the EM simulation results of the transformer from Sonnet Software, optimization of the model in Figure 14 is performed in ADS. The first stage transformer which is 100 um in radius and has a width of 20 um is used to illustrate the fitting. The S-parameter plots exhibiting return loss (S11), isolation (S12), and transmission (S14, S13) are shown in Figure 14. The plots in Figure 14 verify that our model is satisfactory and can be used in place of the transformer in the frequency multiplier circuits for simulation and design purposes. Fitted plots for the other two stages are in the Appendix.

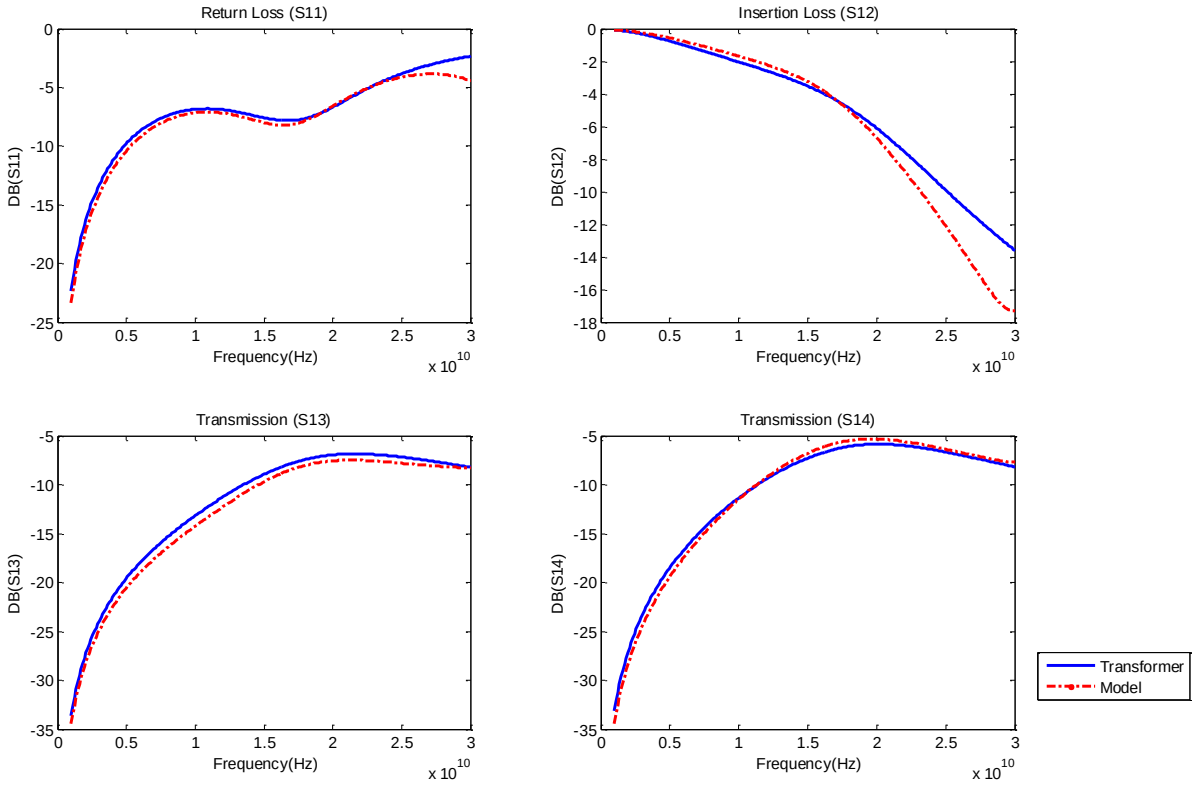

Figure 14. Fitted S-parameter plots of the model and transformer for the first stage

3.3 Summary

In this chapter, we looked at transformer characteristics and the structures in use. Octagonal, stacked structure is chosen for its merits of low loss (compared to rectangular) and high magnetic coupling. Effects of varying radius and width were shown. Higher radius is attributed to increases in SRF and increase in width to decreased SRF. The transformer size chosen for the multiplier's first stage is 100um in radius and 20um in width. The second stage uses one with radius of 50um and width 15um while the last stage uses one with radius 40um and width 8um.

CHAPTER 4

Multi-stage Doubler Frequency Multiplier

In this chapter we examine the Cadence simulations of a three stage doubler and analyze it for several figures of merit. Fundamental frequency and odd harmonics are also to be eliminated at the output with a good rejection ratio. A two stage doubler is implemented in [5] which takes in a 25GHz input and has an output up to 100GHz. The task here is to implement a three stage frequency multiplier with good design for 12.5GHz to 100GHz.

4.1 Transformer Model

The stack octagonal transformer with a center tap is chosen to achieve the frequency multiplier and appears at the input of each stage.

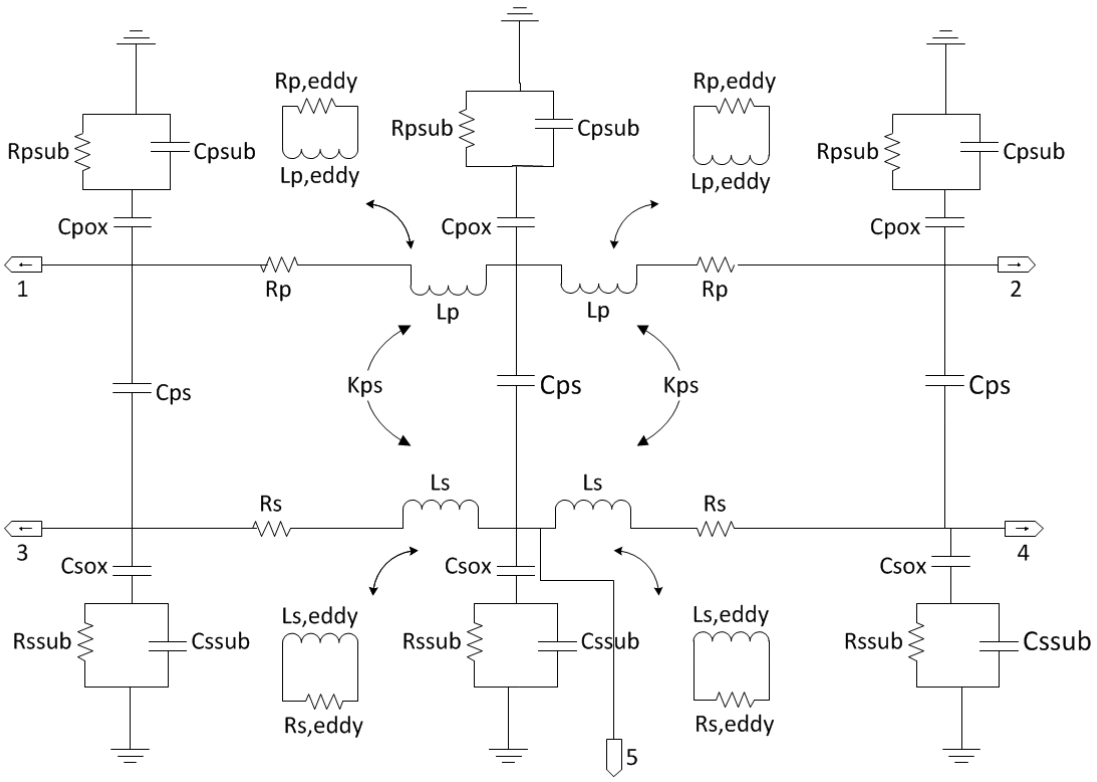

Figure 15. Model Transformer with 5 ports

Table 3

Transformer model circuit values

	First Stage Transformer IR = 100um W = 20um	*Second Stage Transformer* IR = 50um W = 15um	*Third Stage Transformer* IR = 40um W = 8um
R_p	0.332	1.72E-5	1.5E-4
R_s	1.52	1E-5	1.47
R_{pedd}	0.020	1.795E-5	0.019
R_{seddy}	0.010	1E-3	3.02
R_{ssub}	1.122E3	1E4	2.0E5
R_{psub}	8.0E3	4.9	1.1E3
L_p	3.93E-12	1.786E-10	1.86E-10
L_s	3.74E-10	1.67E-10	2.4E-10
L_{peddy}	5.8E-9	4.237E-8	8.69E-8
L_{seddy}	5.0E-7	1E-6	8.1E-9
C_{pox}	4.5E-13	1.26E-13	5.5E-14
C_{sox}	1.1E-10	1E-9	7.17E-10
C_{psub}	4.3E-13	9.4E-13	1.245E-12
C_{ssub}	2.82E-13	1.04E-13	2.01E-15
C_{ps}	4.17e-14	1.49E-19	1.5E-14
K_{ps}	0.802	0.77	-0.634
K_{pedd}	0.01	0.146	0.01
K_{sedd}	0.01	0.025	0.02

Three circuits representing the three transformers with the values shown in the table above are inserted into the three stage frequency multiplier in Cadence for simulation and optimization. In the following sections we will examine the multipliers implemented using the transformer model circuits.

4.2 Doubler Circuit

A push-push topology has good harmonic rejection and is the configuration implemented to realize a doubler. The circuit schematic for the doubler is shown in Figure 16. The circuit as shown consists of a transformer, three transistors, two in parallel with differential inputs and the third as the buffer to the output, an LC tank tuned to the frequency desired and power sources.

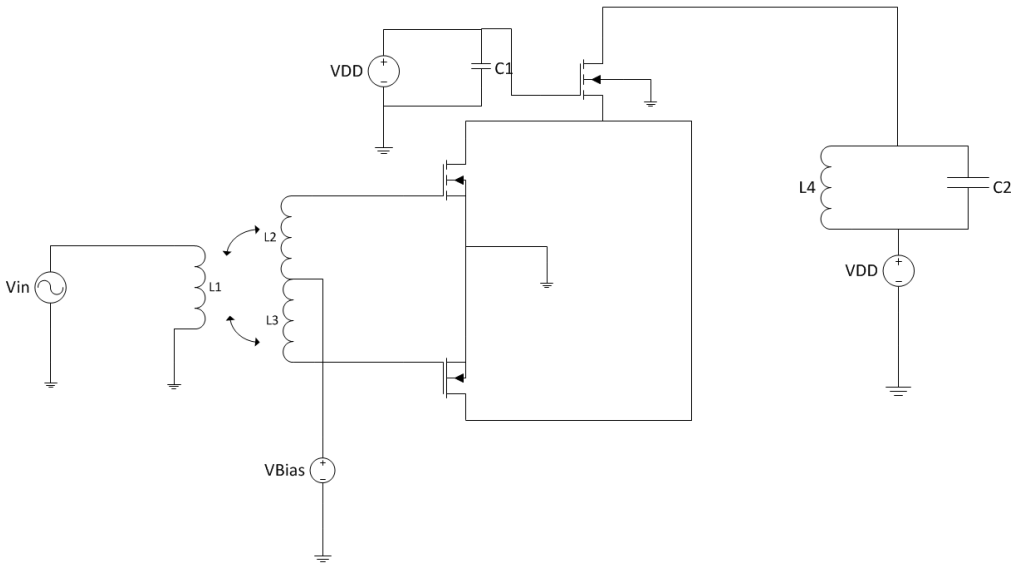

Figure 16. Frequency doubler circuit

4.2.1 First Stage as a Doubler

The circuit is configured as shown in Figure 16. The transformer used here is 100um in radius and 20um width. It has a resonance frequency at 25.5GHz and will operate reliably at 12.5GHz. The rest of the parameters of the circuit are shown in Table 4 and the resulting waveforms in Figure 21.

Table 4

First Stage Doubler Parameters

Input Signal	12.5GHz, 1V pk-pk	M1/M2 W/L	32um/60nm
V_{DD}	1.2V	M3 W/L	32 um/60nm
V_{bias}	0V	L4	200pH
C1	1nF	C2	170fF

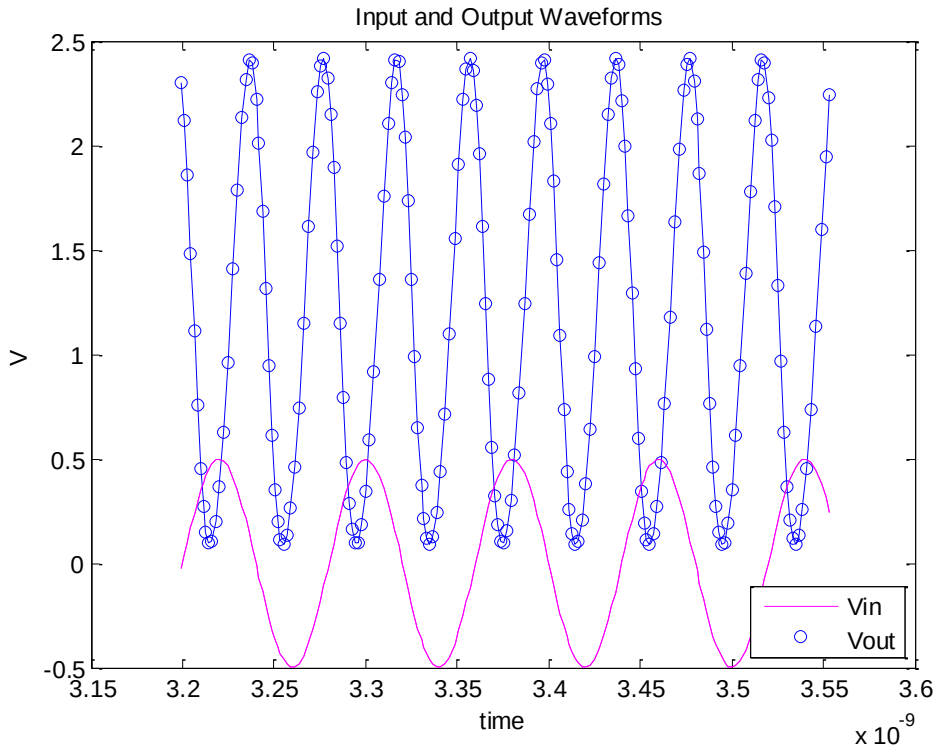

Figure 17. Waveforms of the first stage doubler

Figure 17 shows the input and output waveform of the first stage doubler with the parameters shown in Table 4. The output waveform is 2.2V peak-to-peak while the input is 1V peak-to-peak. The LC tank at the output is tuned to 25GHz and is a virtual short for every other frequency. This ensures a high fundamental frequency rejection.

The figures of merit, namely, conversion gain, power and bandwidth are analyzed for this frequency multiplier. An analysis of the conversion gain is plotted in Figure 18. As seen from the plot, the maximum conversion gain occurs at an input of 20dBm for this doubler. The conversion gain at that point is -17.28dB. In the figure 19, a plot of the output power depicting the fundamental rejection and harmonic rejection is shown. Fundamental rejection for this doubler is above 60dBm. The output signal is at 1.15dBm and the fundamental is at -65dBm. By sweeping a range of frequencies around 12.5GHz the bandwidth of the doubler is tested. The output frequencies are shown in Figure 20. As can be seen in the figure, the bandwidth of the doubler is narrow and spans from about 23GHz to about 27GHz.

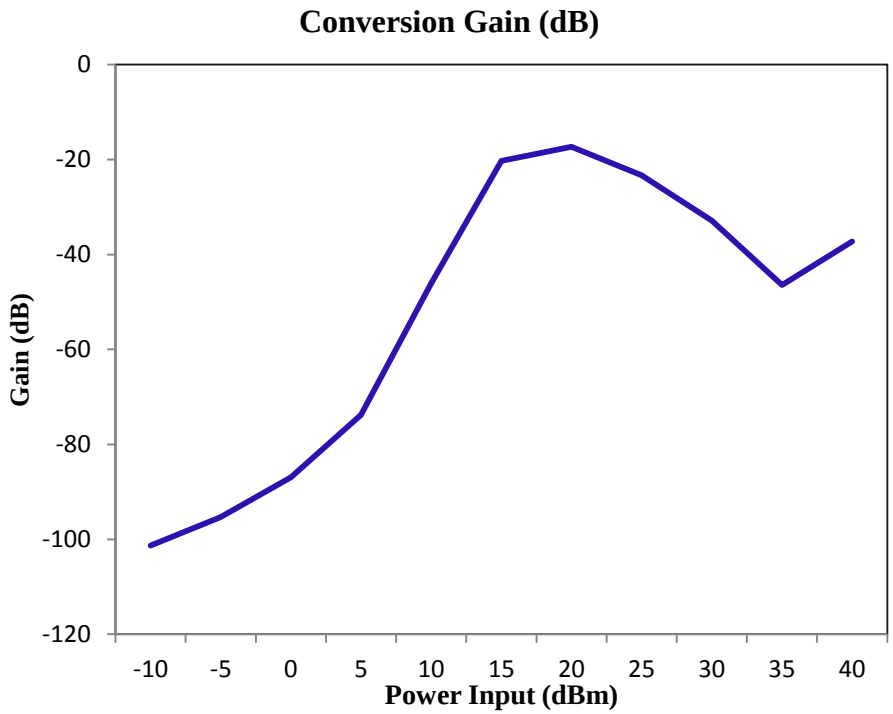

Figure 18. Conversion gain of the first stage doubler.

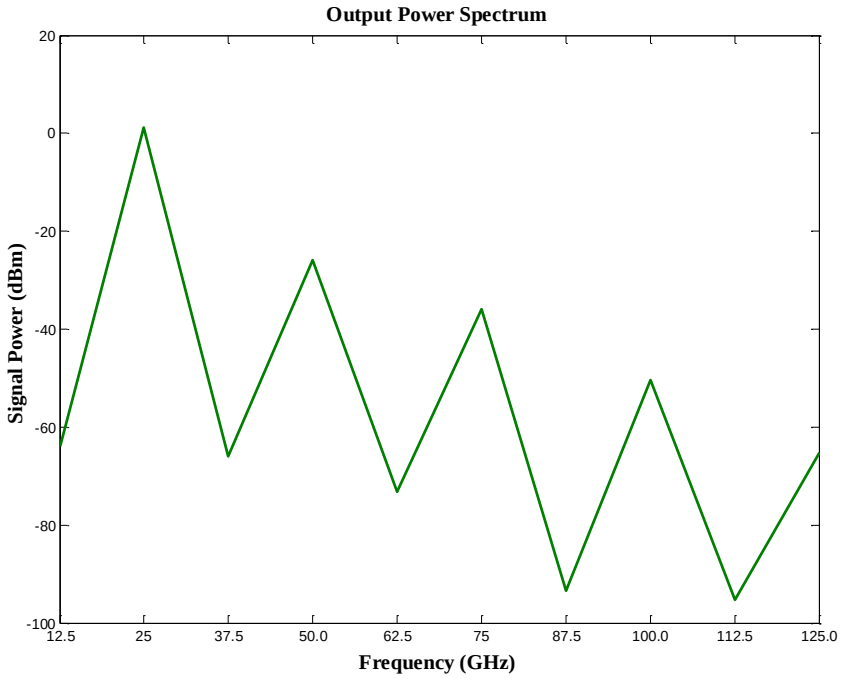

Figure 19. Power output spectrum of the first doubler

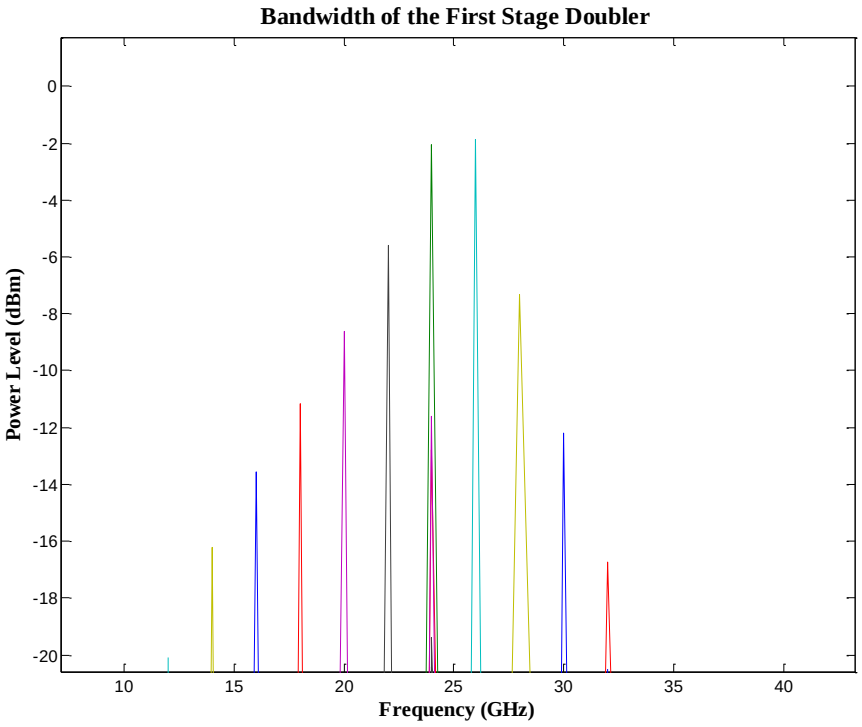

Figure 20. Power spectrum showing the bandwidth of the doubler.

4.2.2 Second Stage as a Doubler

The topology of this circuit is identical to the first stage doubler shown in Figure 16 except for circuit parameters and the transformer in use. The transformer in this doubler is 50um in radius and 15um in width. This transformer has a resonance frequency of about 57.5GHz. The other circuit parameters are listed in Table 5. The waveforms of the second stage acting as a doubler are given in Figure 21. The frequency of the output is 50GHz and is 1.01V peak-to-peak. The LC tank is also present in this doubler is tuned to 50GHz and attenuates other frequencies.

Table 5

Second Stage Doubler Parameters

Input Signal	25 GHz, 1V pk-pk	L4	175pH
V_{DD}	1.2V	C2	34fF
V_{bias}	550mV	M1/M2 W/L	44um/60nm
C1	1 pF	M3 W/L	28 um/60 nm

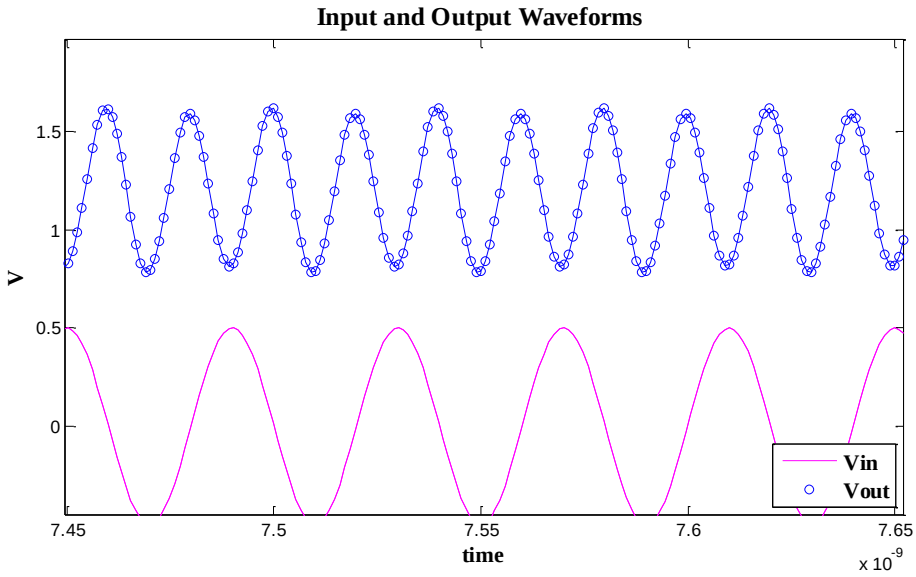

Figure 21. Input and Output waveforms of the second stage as a doubler

An analysis of the conversion gain is plotted in Figure 22 shown below. Maximum conversion gain occurs at an input of 20dBm for this doubler. This conversion gain is -14.98dB. In Figure 23 a plot of the output power depicting the fundamental rejection and harmonic rejection is shown. Fundamental rejection for this doubler is about 20dBm. The output power is -8.04dBm at the output frequency of 50GHz. Sweeping the input frequency from 20GHz to 30GHz, the bandwidth of the second stage doubler is obtained at the output. The spectrum plot below shows the bandwidth of the doubler. The bandwidth of the doubler as can be seen from the figure goes from about 45GHz to about 55GHz.

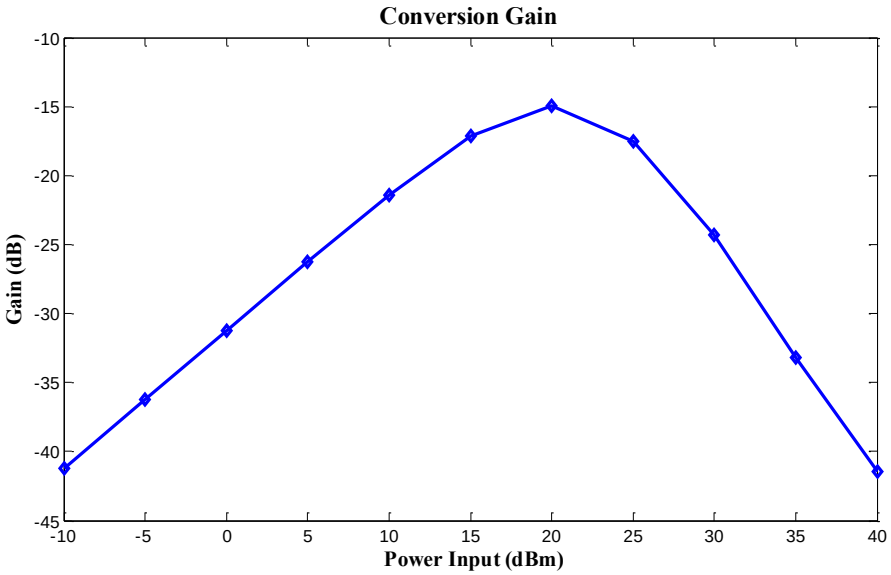

Figure 22. Conversion gain of the second stage doubler.

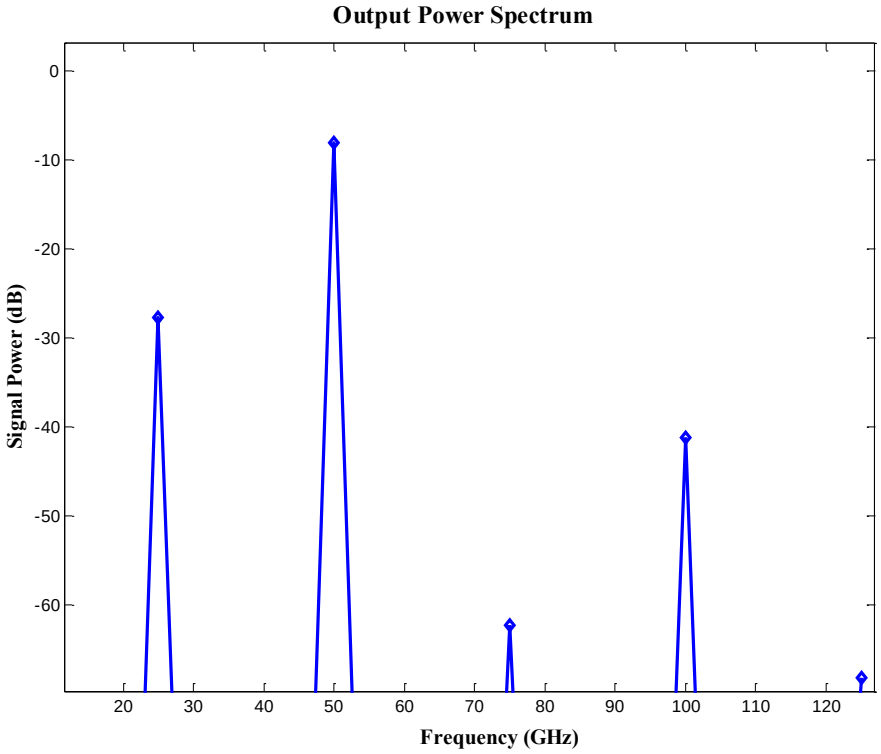

Figure 23. Power output spectrum of the second doubler

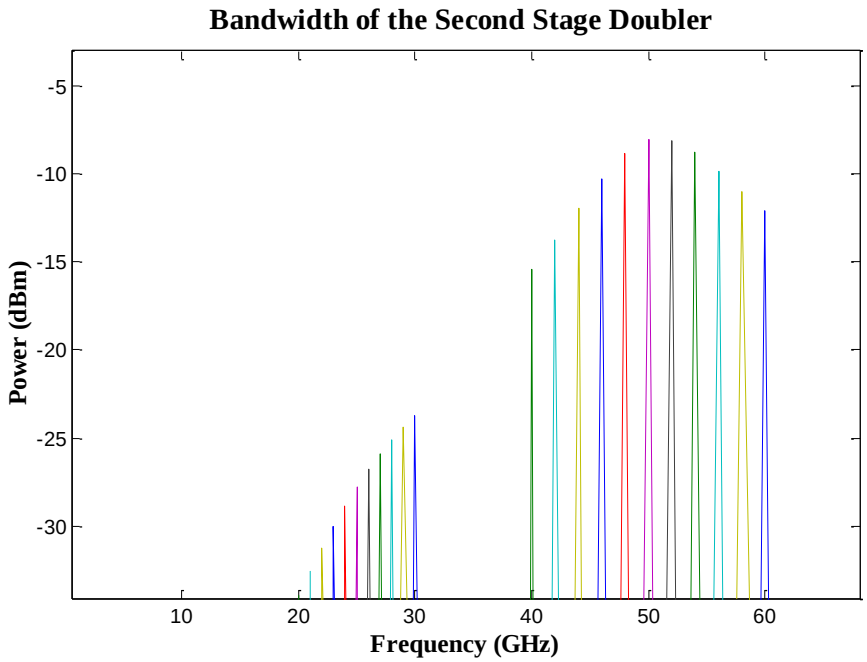

*Figure 24.*Bandwidth of the second stage doubler.

4.2.3 Third Stage as a Doubler

Using the same topology as the other doublers but changing again the circuit parameters and the transformer, we are able to use the third stage as a stand-alone doubler. The transformer here has a radius of 40um and a width of 8um. The resonant frequency for this transformer is 133GHz. The rest of the parameters are given in Table 6. The input and output waveforms are shown in Figure 25. The third stage doubler has an output of 100GHz frequency which is 455.4mV peak-to-peak. There is a loss between input and output in this doubler. The input is 1 V peak to peak at 25GHz frequency.

Table 6

Third Stage Doubler Parameters

Input Signal	50 GHz, 1V pk-pk	L4	42 pH
V_{DD}	1.2 V	C2	30 fF
V_{bias}	500 mV	M1/M2 W/L	40 um/60 nm
C1	1 pF	M3 W/L	40 um/60 nm

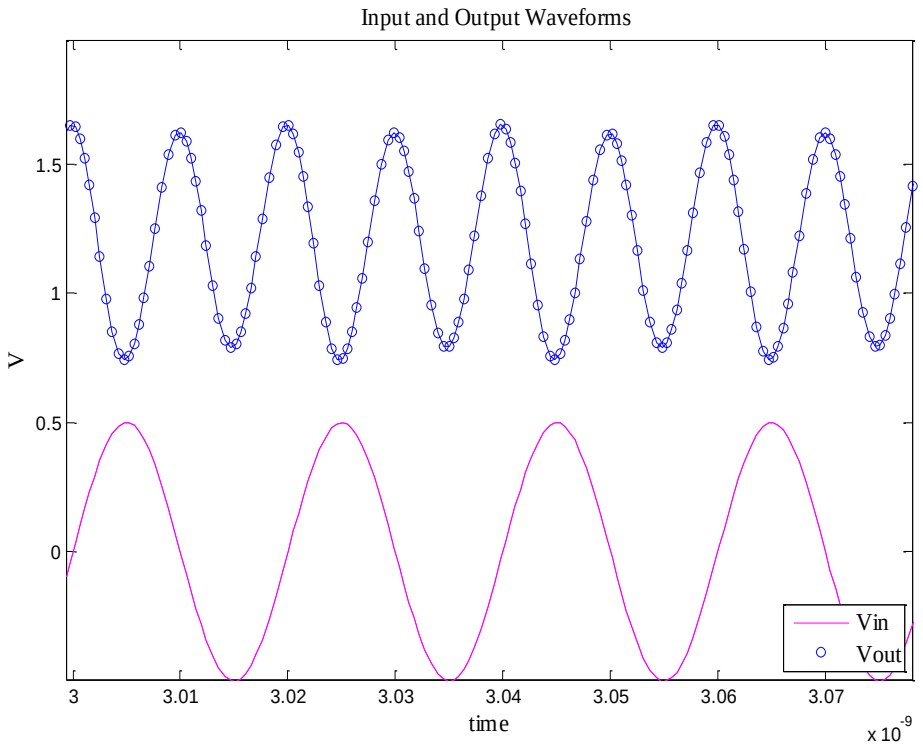

Figure 25. Input and output waveforms of the third stage as a doubler.

An analysis of the third stage doubler is performed and figures of merit are shown in the figures that follow. The conversion gain is shown in Figure 26. Maximum conversion gain occurs at an input of 35dBm for this doubler. This conversion gain is -30.6994dBm. In Figure 27 a plot of the output power depicting the fundamental rejection and harmonic rejection is shown. Fundamental rejection for this doubler is about 4dBm. The output power is -10.2dBm for the

output signal frequency of 100GHz. Sweeping the input frequency from 45GHz to 55GHz the output is plotted as a spectrum shown in Figure 28. As seen in the figure, the bandwidth spans from about 92GHz to about 110GHz. The maximum power of -8.1dBm is at 106GHz.

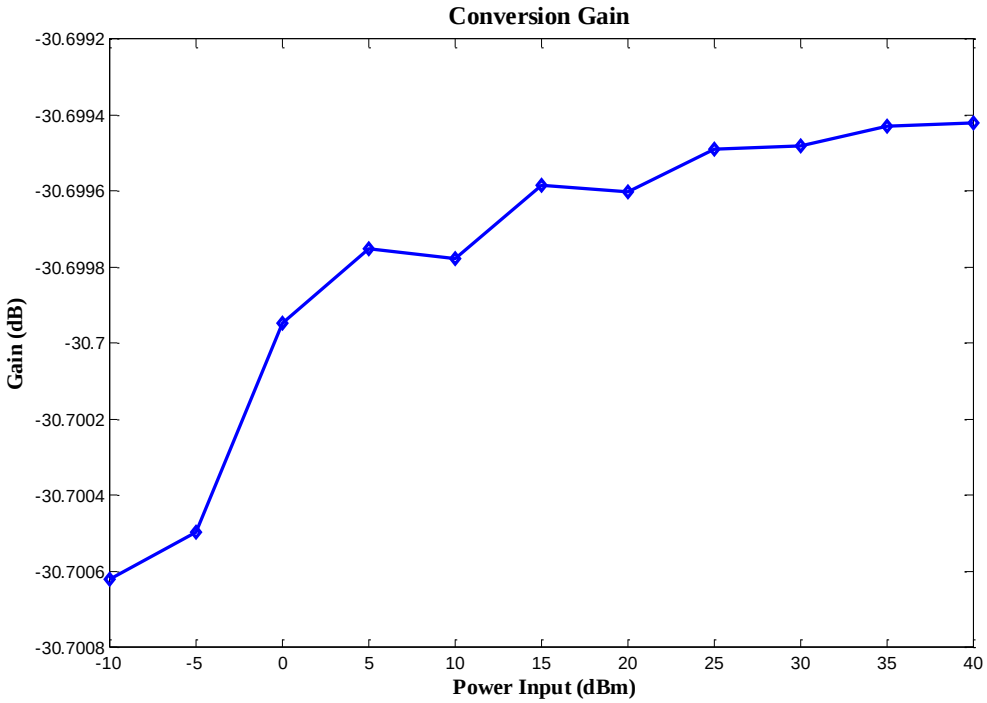

Figure 26. Conversion gain of the third stage doubler.

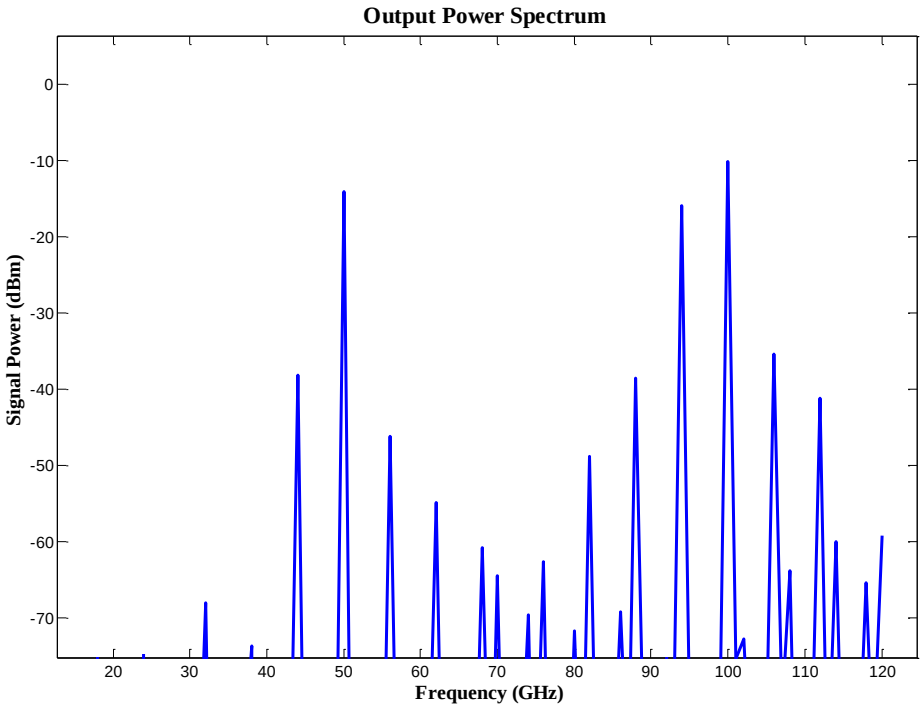

Figure 27. Power output spectrum of the third stage doubler

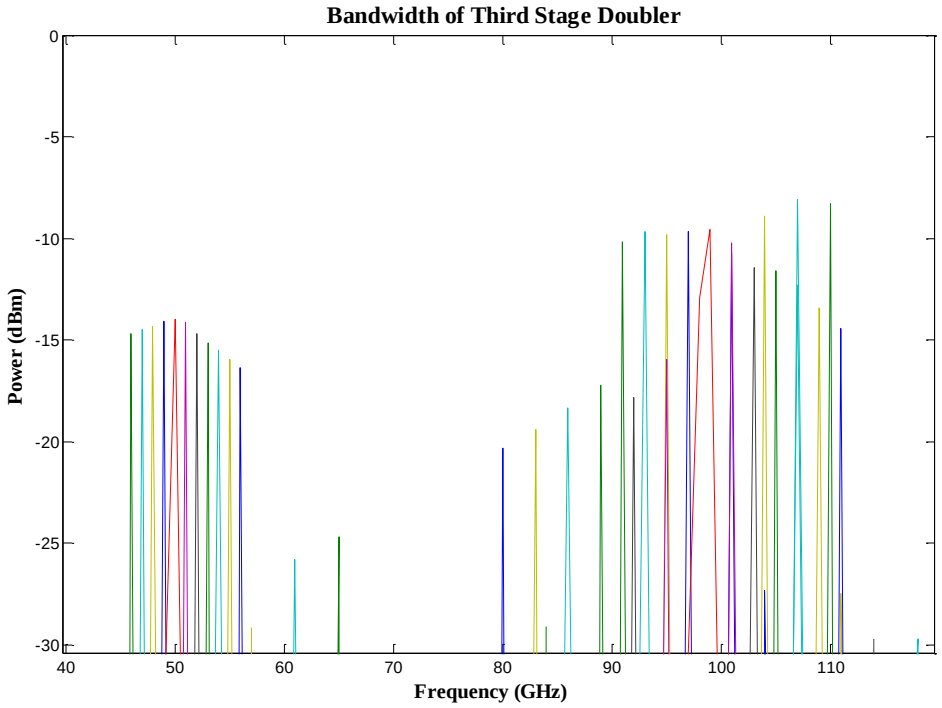

Figure 28. Bandwidth of the third stage doubler.

4.3 Two Stage Doubler X4 Multiplier

Here we examine the implementation of a two stage frequency doubler shown in Figure 29 The LC tank at every stage is matched to a resonance of the frequency desired there. The two stage multiplier is implemented in two different ways. The first and second stage transformers are used to go from 12.5GHz to 50GHz and then the second and third stage transformers to go from 25GHz to 100GHz.

4.3.1 First and Second Stage Doublers Cascaded

The two stage frequency multiplier as shown in Figure 29 is implemented here using the second and third stage whose transformers are of size 100um and 50um respectively. Figure 38 shows the waveform of the frequency multiplier realized. At the output of the first stage, the signal is 25GHz in frequency and 656mV peak-to-peak. The output of the second stage is 50GHz in frequency and 361mV peak-to-peak. The input signal is 1V peak-to-peak. The values chosen for the various capacitors and transistor sizes are shown in Table 7. These are values that were tuned to increase the gain of the multiplier while maintaining the multiplication of the input at the output of the first stage and second stage. Figure 39 shows the output waveforms.

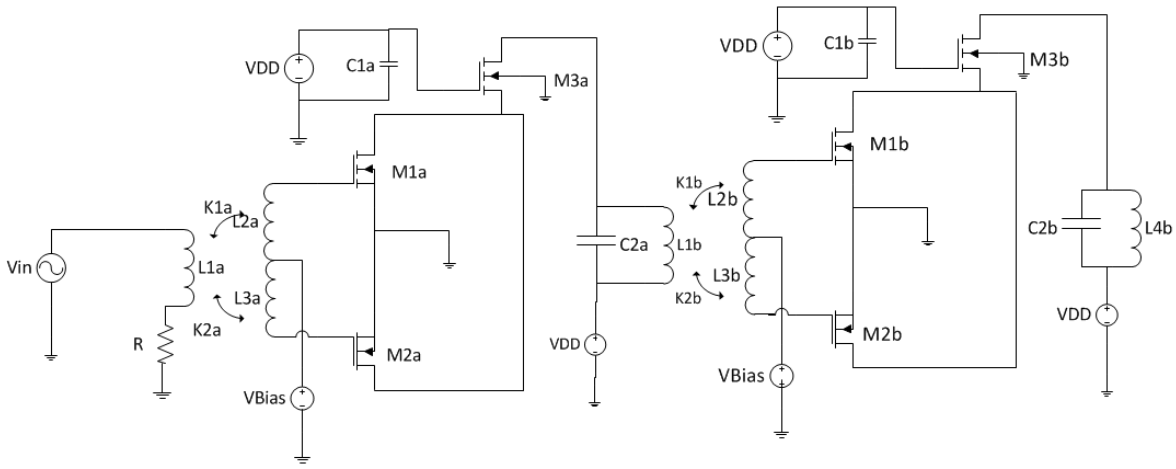

Figure 29. Frequency multiplier circuit configuration

Table 7

Frequency Multiplier Parameters

C1a	1 nF	M3b W/L	28 um/60 nm
C2a	150 fF	C1b	1 pF
M1a, M2a	44 um/60 nm	C2b	34 fF
M3a W/L	52 um/60 nm	L4b	175 pF
M1b, M2b W/L	44 um/60 nm		

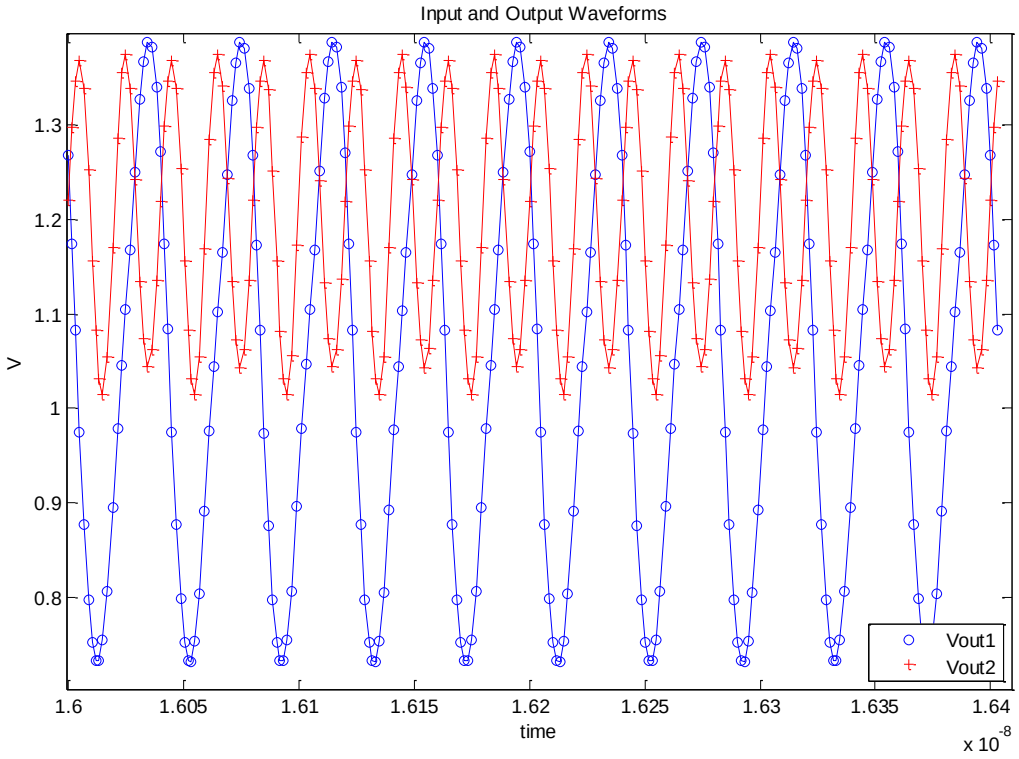

Figure 30. Output and Input waveform of the two stage frequency multiplier.

An analysis of the conversion gain is plotted Figure 31. Maximum conversion gain occurs at an input of 20dBm for this doubler. The maximum conversion gain is -38dB. In Figure 32 a plot of the output power depicting the fundamental rejection and harmonic rejection is shown. Fundamental rejection for this doubler is above 80dBm. The second harmonic suppression is 20dBm. The output power at the output frequency of 50GHz is -21dBm.. Input frequency is swept from 5GHz to 20GHz and the output plotted in a spectrum as shown below. The bandwidth spans from 50GHz to about 60GHz. The maximum power of -18.25dBm is at 54GHz.

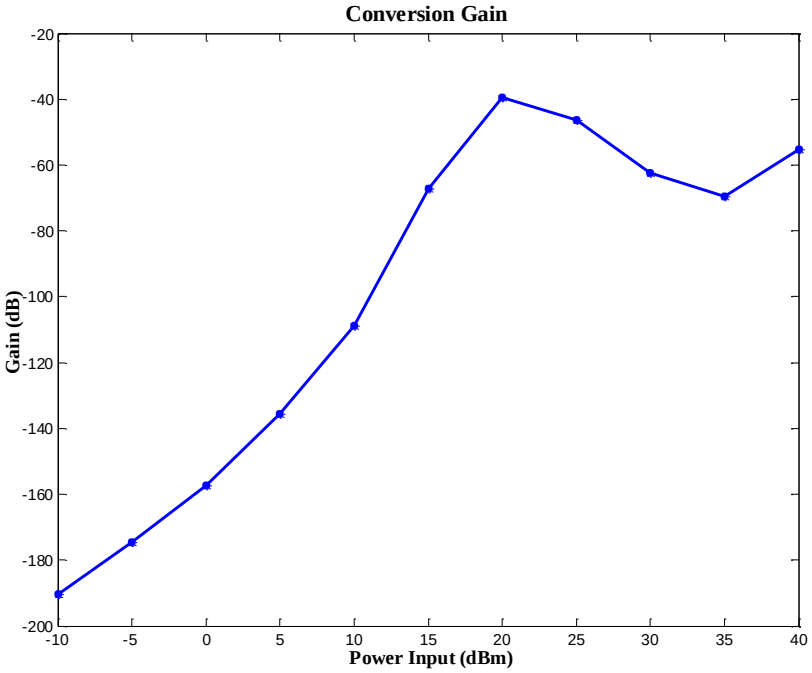

Figure 31. Conversion gain of the x4 frequency multiplier.

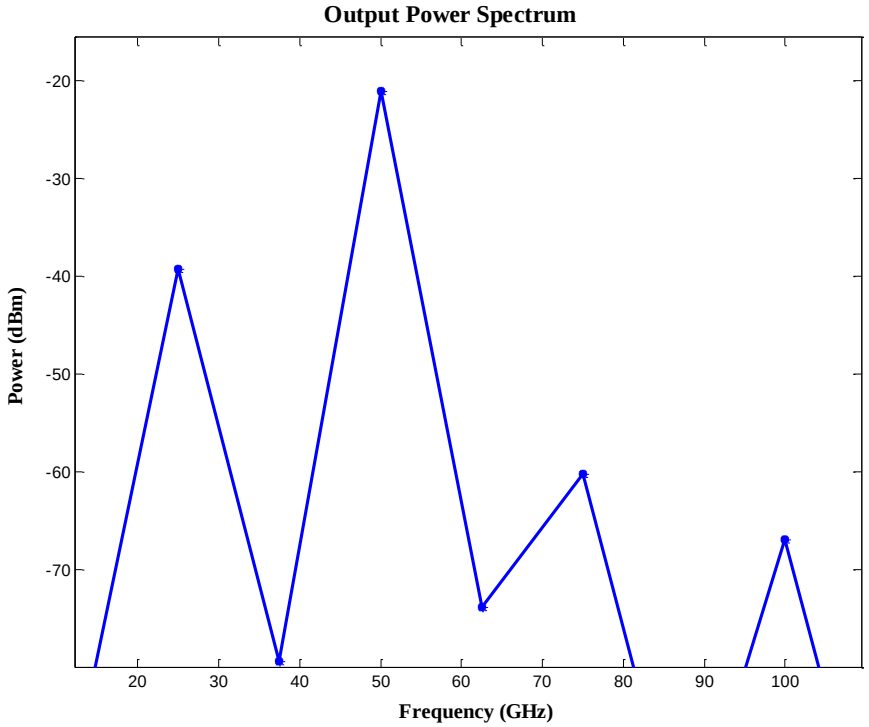

Figure 32. Power output spectrum of the x4 frequency multiplier.

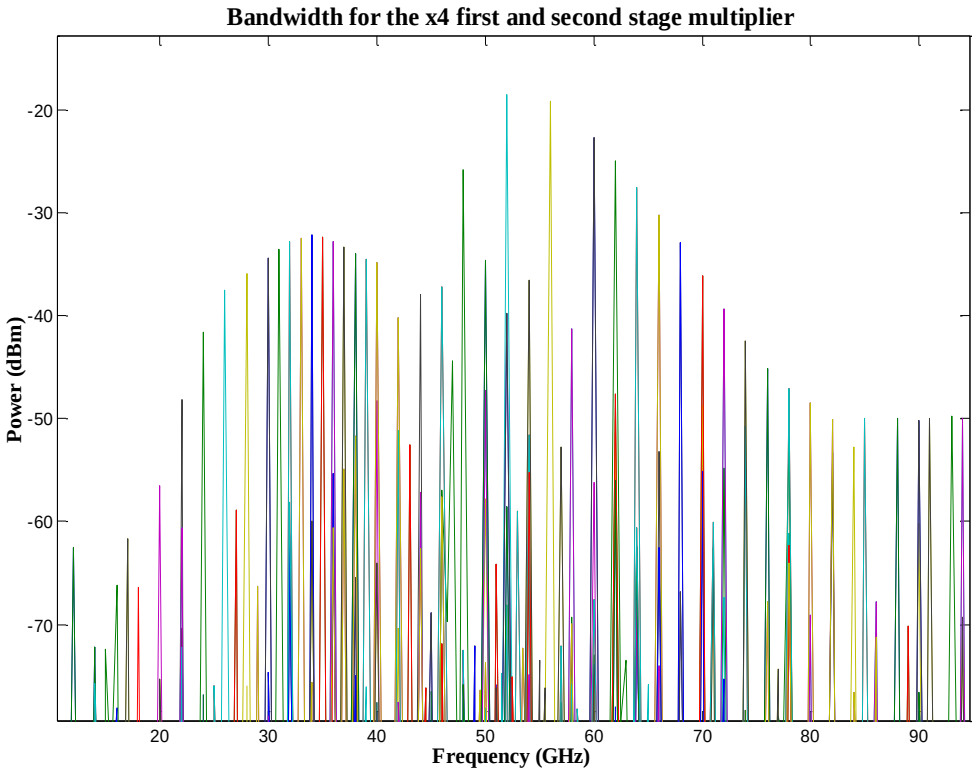

Figure 33. Bandwidth of the x4 Frequency multiplier

4.3.2 Second and Third Stage Cascaded

The two stage frequency multiplier as shown in Figure 29 is also implemented using the second and third stage whose transformers are of size 50um and 40um respectively. Figure 38 shows the waveform of the frequency multiplier realized. As seen from the figure, there is amplitude noise but we get the desired frequencies at both outputs. The first output is 463mV peak-to-peak, while the second is 435mV peak-to-peak. The input voltage used is 1.5V in amplitude.

Table 8

Frequency Multiplier Parameters

C1a	1 pF	M3b W/L	44 um/60 nm
C2a	28.9 fF	C1b	1 pF
M1a, M2a	48 um/60 nm	C2b	31 fF
M3a W/L	40 um/60 nm	L4b	42 pF
M1b, M2b W/L	22 um/60 nm		

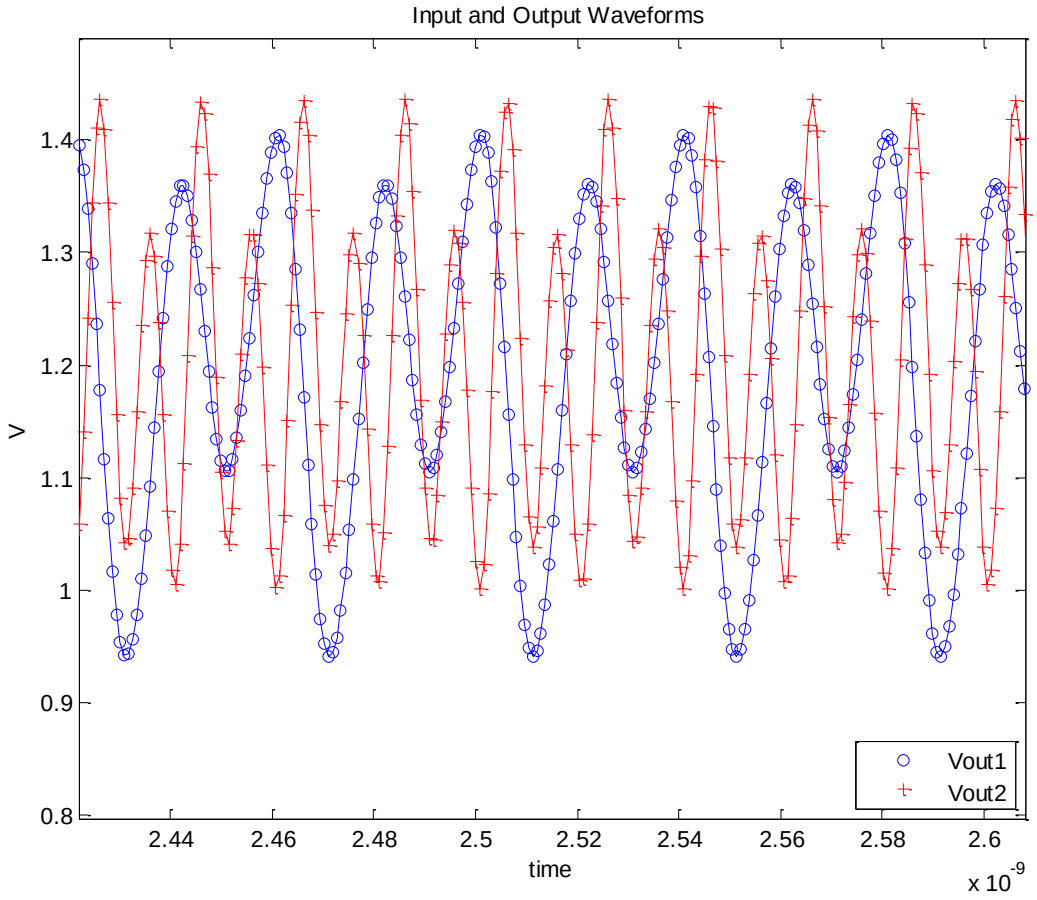

Figure 34. Output and Input waveform of the two stage frequency multiplier

An analysis of the conversion gain is plotted in Figure 35. Maximum conversion gain occurs at an input of 25dBm for this doubler. The conversion gain at this point is -30dB. In

Figure 36 a plot of the output power depicting the fundamental rejection and harmonic rejection is shown. Fundamental rejection for this doubler is above 25dBm. The second harmonic rejection is about 3dBm. The target frequency 100GHz is at a power of -18dBm. The bandwidth of this multiplier as shown in Figure 37 spans from 100GHz to about 110GHz with the highest power of -18dBm at 107GHz.

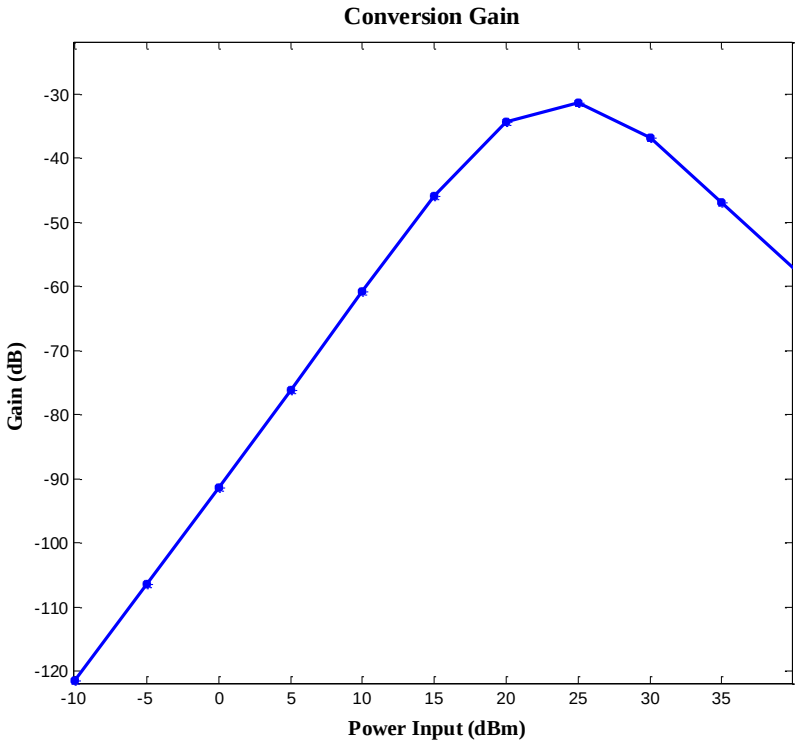

Figure 35. Conversion gain of the x4 frequency multiplie

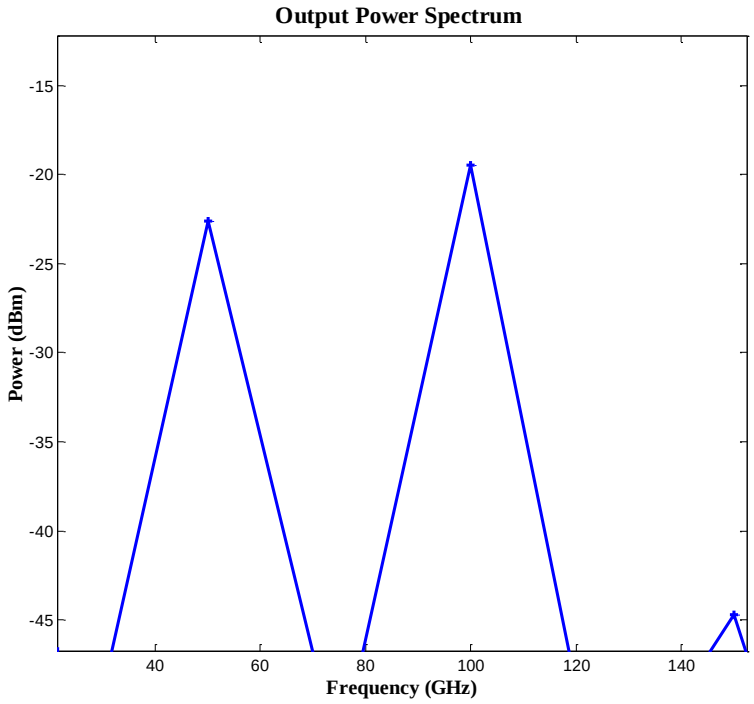

Figure 36. Power output spectrum of the x4 frequency multiplier

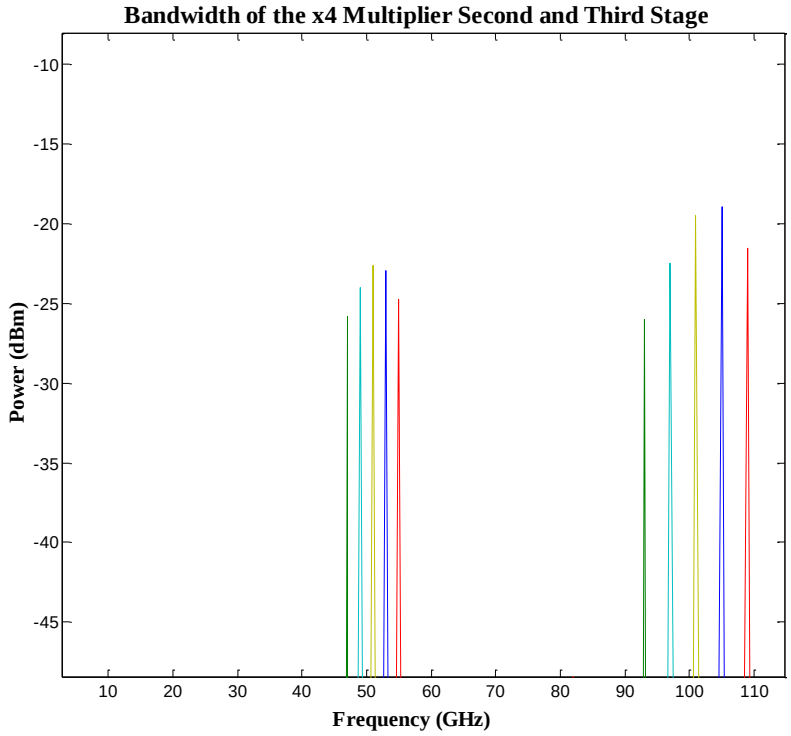

Figure 37. Bandwidth of the x4 multiplier using the second and third stage.

4.4 Three-stage Doubler x8 Frequency Multiplier

By cascading another doubler at the output of the second stage, we are able to achieve a three-stage doubler and multiply the input frequency to obtain 100GHz at the output. The output waveforms of the three stage doubler are as shown in Figure 39. The values of the parameters used in the three stage doubler of Figure 38 are listed in Table 9. The bias voltage is given in the order of stages. The waveforms of the outputs at the three stages are shown in the waveform plot of Figure 39.

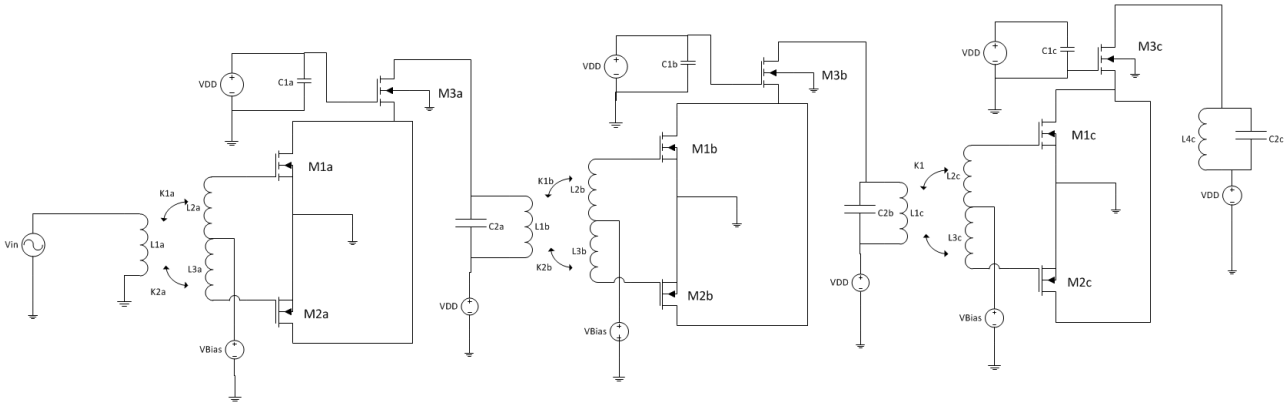

Figure 38. The three stage frequency multiplier

Table 9

Parameters of the three stage doubler frequency multiplier

Input Signal	12.5 GHz, 1V	M1b/M2b W/L	32 um/60 nm
V_{DD}	1.2 V	M3b W/L	24 um/60 nm
V_{biass}	0 mV, 500 mV, 800 mV	C2b	5 fF
C1a	1 nF	M1c/M2c W/L	40 um/60 nm
M1a/M2a	44 um/60 nm	M3c W/L	16 um/60 nm
M3a	52 um/60 nm	L4c	42 pF
C2a	100 fF	C2c	31 fF
C1b	1 pF		

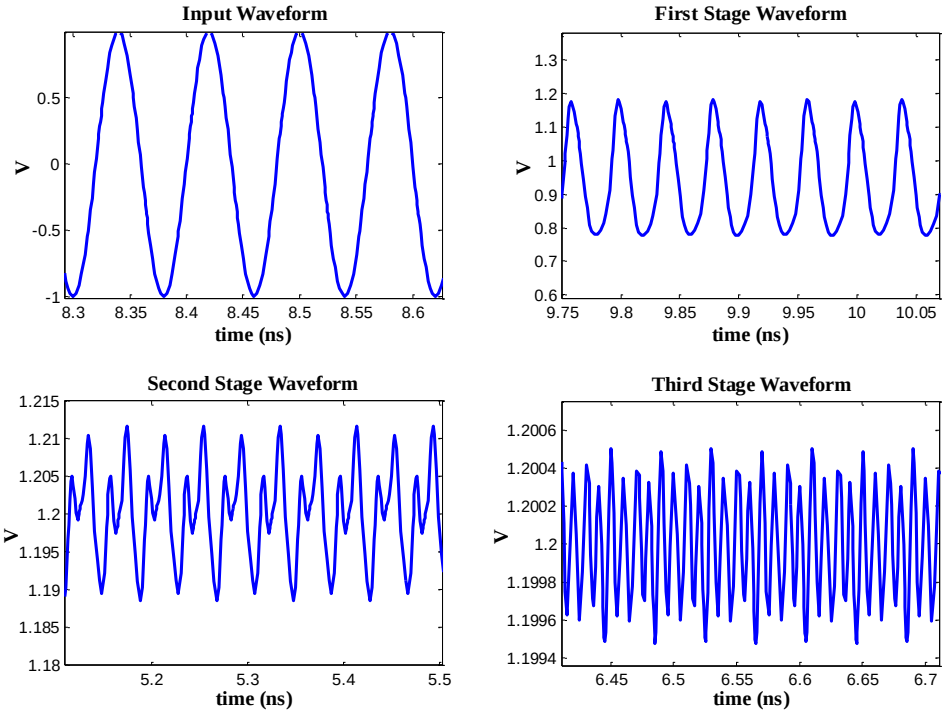

Figure 39. Output waveforms for the three stage doubler

At the output of the first stage, the frequency of the waveform is 25GHz and 508mV peak to peak. The output of the second stage has a waveform of 50GHz and a peak to peak value of 23.2mV. The final output of the three-stage doubler is 100GHz with a peak-to-peak voltage of 1.2mV peak to peak.

In a plot of the output power depicting the fundamental rejection and harmonic rejection is shown in Figure 40. Fundamental rejection for this doubler is above 35dB. The second harmonic rejection is about 10dB. The target frequency 100GHz is at a power of -4dBm. For an input of 25dBm, conversion gain is approximately -30dB.

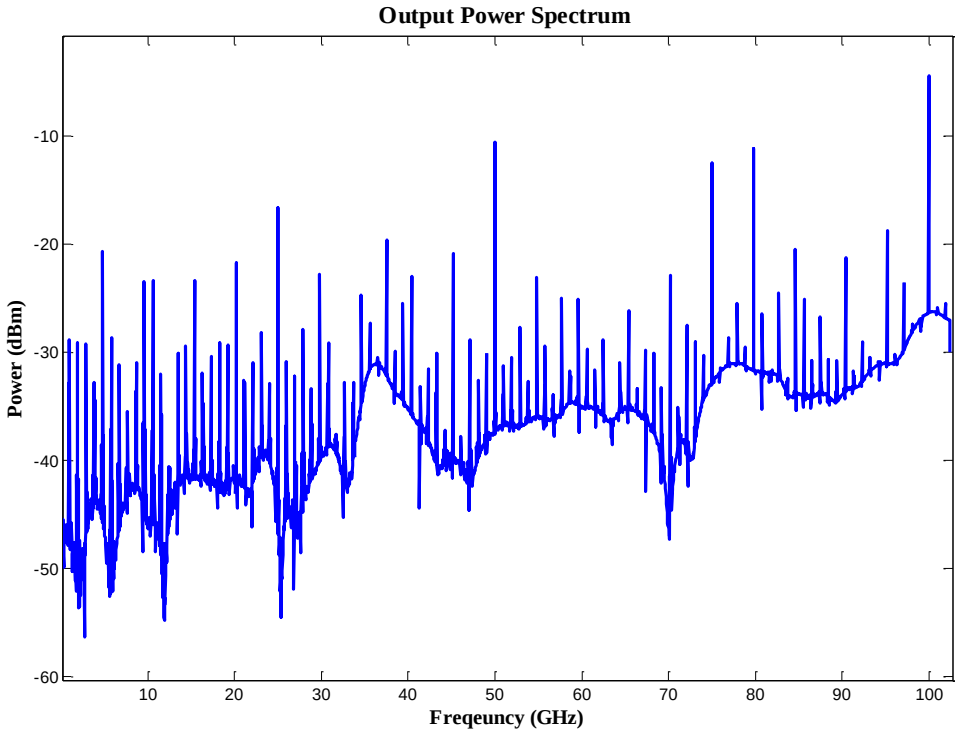

Figure 40. Power Output of the 3-stage doubler frequency multiplier

4.5 Summary

In this chapter we have examined various multiplier circuits and looked at their waveforms. We looked at single stage doublers using the three different transformers and at three different input frequencies. We also looked at two-stage doubler multipliers and finally the three stage doubler frequency multiplier. The input and output waveforms illustrate that they do perform the function of extracting the higher harmonics of the fundamental frequency.

CHAPTER 5

Conclusion

Using the transformers in frequency multipliers enables us to achieve higher frequencies into the terahertz range. Modelling the transformers and choosing an appropriate geometry is essential in achieving a good behavior in the frequency multiplier. The different transformer geometries have different Q-factor, inductance and self-resonant frequency (SRF). Careful selection of a transformer with the appropriate Q-factor and SRF is essential in having a good performance multiplier.

5.1 Results

We are able to design a frequency multiplier which takes in a 12.5GHz signal and outputs 100GHz at the output. The output is -4dBm in power level and the conversion gain is -81.5dB. For a multiplication of eight of a fundamental frequency, this is an acceptable power level. The power spectrum of each frequency at the end is illustrated by the graph shown below. We can see that the input fundamental frequency and other harmonics below 100GHz are highly attenuated at the output with a fundamental rejection greater than 35dB. With a DC bias level of 1.2V, power consumption is 18mW. These values are summarized in Table 10 and compared with other works.

Table 10

Comparison with Literature

References	[15] 2008	[16] 2010	[17] 2010	[5] 2012	This Work
Technology	90nm CMOS	65nm CMOS	0.13um CMOS	65nm CMOS	65nm CMOS
Bandwidth	56-64	85-95.2	94-108	75-110	88-104
Multiplication	3	3	2	4	8
Fundamental rejection ratio	n/a	>14dB	>30dB	>30dB	>50dB
Power (dBm)	-22	-13.5	-8.7	-14.3	-4
Conversion Gain (dB)	-23	-17.5	-21	-24.3	-30
Power Consumptiom	23.8mW	19.8mW	n/a	16mW	18mW

5.2 Future Work

Frequency multipliers are possible in the high frequency bands as considered in this thesis. Working on perfecting the transformer model for higher frequencies is fundamental to the design of multipliers. Also, designing amplifiers that will work well with frequency multipliers without deteriorating the purity of the output signal is essential to get the power levels higher than was achieved here or in other literature.

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Appendix

The fitting data between the model and the second and third transformer are shown in Figure 41 and Figure 42. The S-parameter plots of the transformer model are well within 10% of the EM-simulation S-parameter plots. The model therefore gives a good approximation of the transformer behavior in a circuit.

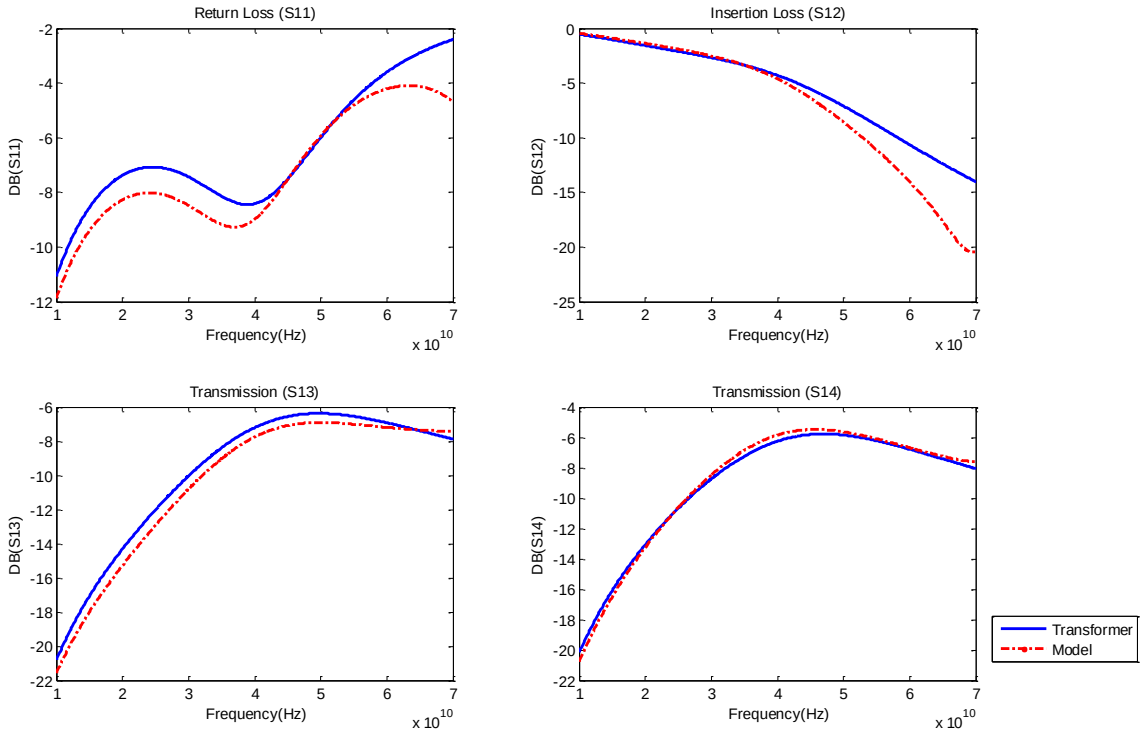

Figure 41. S-parameter fitting curves of EM simulation and model for stage 2.

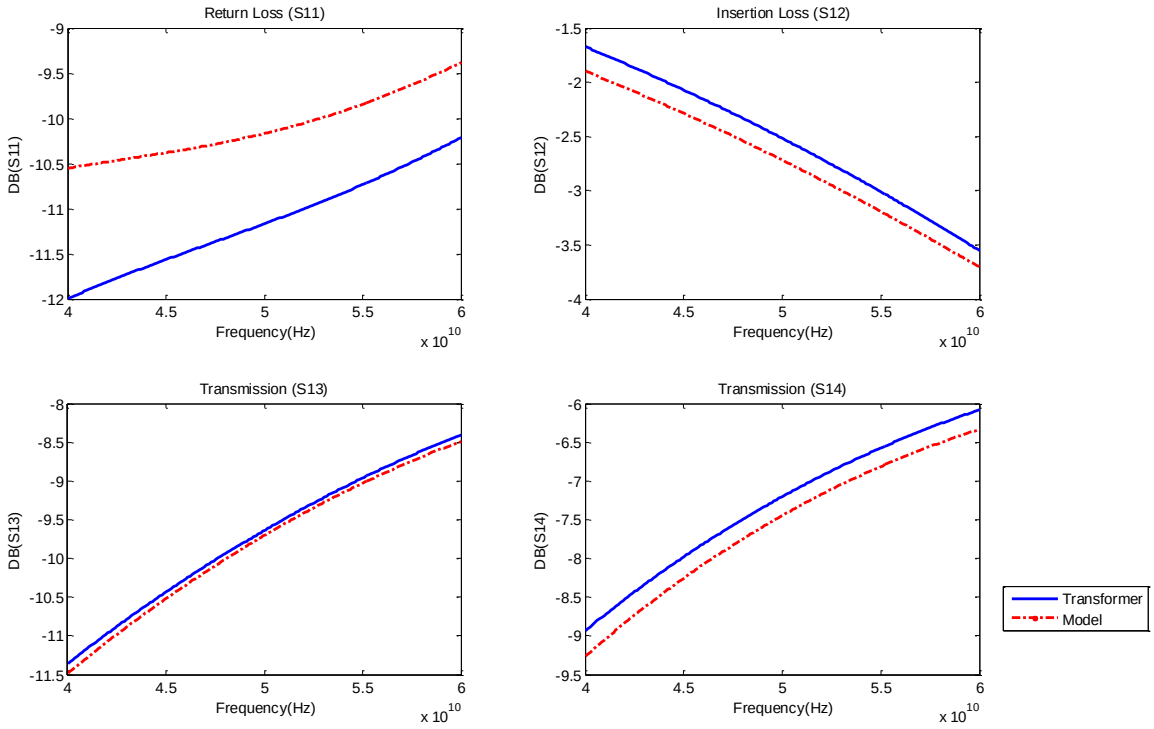

Figure 42. S-parameter fitting curves of EM simulation and model for stage 3.

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