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Characterization, Modeling And Implementation Of Esd Protection Of An Rf Circuit

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Characterization, Modeling and Implementation of ESD protection of an RF circuit

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Biographical Sketch

Abid Mehmood was born in Attock, Pakistan on October 26 1984. He did his undergraduate studies in Electrical Engineering at North Carolina A&T State University from January 2009 to December 2011. He joined the Department of Electrical and Computer Engineering at North Carolina Agricultural and Technical State University, Greensboro, North Carolina, in fall 2012 for the Master of Science degree in Electrical Engineering. He worked as teaching assistant and research assistant during his master study. He has been advised by Dr. Zhijian Xie of master study in A&T University and supervised by Dr. Nathaniel Peachey and Scott Parker of his internship in RF Micro Device since 2013.

Dedication

This work is dedicated to my advisor, supervisor, committee members, and all ESD group members of RFMD for their prayers and unflinching support through my years of education.

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First of all I would like to thank Allah (GOD) for making this achievement possible. Many people have contributed to this thesis in diverse ways. To all these people, I would like to express my genuine thanks and gratitude. First, my gratitude goes to North Carolina A&T State University for providing me a good environment to study. Secondly, I would like to express my deepest gratitude to my advisor, Dr. Zhijian Xie for his expertise to help me complete this work. His insightful contributions and suggestions have helped me to better understand the research problems of this work. During my master study life he encouraged and educated me patiently. I want to thank my supervisor Dr. Nathaniel Peachey and Scott Parker. They provided me a good research environment and shared their experiences with me.

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List of Symbols

ESD Electrostatic Discharge

TLP Transmission Line Pulse

RFIC Ratio Frequency Integrated Circuit

IEEE Institute of Electrical and Electronics Engineering

DUT Device under Test

HBM Human Body Model

CDM Charged Device Model

MM Machine Model

EOS Electrical Over Stress

POD Point of Distribution

CMOS Complementary Metal Oxide Semiconductor

LC Inductor Capacitor

SOI Silicon on Insulator

Abstract

In this research an attempt has been made to fully characterize a diodes array in shunt configuration as ESD protection circuit in order to maximize ESD performance of the products in IBM SOI 0.18um technology. For full characterization of ESD protection of RF circuit, HBM and TLP tests and simulation have been conducted and discussed in detail. Test results for HBM and TLP are summarized and grouped according to their stack number. Simulations on HBM and TLP were carried out using Cadence Spectre environment and compared to the tests for HBM and TLP obtained using Celestron I. To consider the RF part, small signal analysis and large signal analysis are done in Advanced Design System. Small signal extracts the black box capacitance using S-parameter in ADS and compares with test results obtained using Murray Microwave system. Also large signal analysis is carried out to see the nonlinearity of the ESD protection device. In large signal analysis input power is swept and output power is observed on different harmonics caused by the inherent nonlinearity of the device. Again large signal simulation results were compared with test results obtained from Murray Microwave System. Lastly, this research has been conducted to fully characterize the diodes array as ESD protection in shunt configuration and to produce a predictive ESD model.

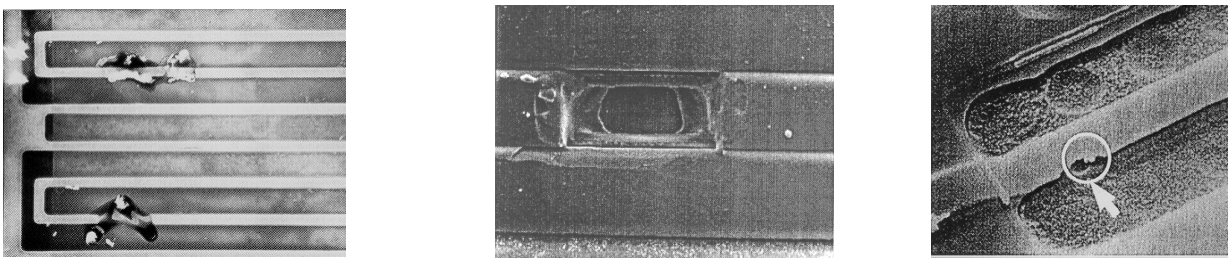
CHAPTER 1

Introduction

1.1 Background

EOS stands for Electrical Overstress. When a device or integrated circuit (IC) is exposed to a current or voltage level which is beyond its maximum limit is called electrical overstress. ESD stands for electrostatic discharge. ESD is subset of EOS. ESD happens between two bodies or surfaces at different electrostatic potential [1]. ESD is a single event in which a quick transfer of electrostatic charge between two bodies takes place when these two bodies at different potential difference come in contact with each other. ESD can also occur when a high electrostatic field is developed between the two bodies very close to each other. ESD failures are one of the most important failures in semiconductor devices industry causing millions of dollars in lost.

Electrostatic charge builds up on the surface of a material due to imbalance of surface electrons, and such charge build up create electric field that is noticeable on the other objects close to it. This process of electrons transfer resulting from two charged bodies coming in contact with one another and then separating is called 'triboelectric charging'. The process of triboelectic charging results one object gaining electrons and therefore becoming negatively charged and other object losing electrons and therefore becoming positively charged [2].
ESD event lasts only for 0.2ns-200ns but it gives a fatal damage to IC's devices because it involves a very high voltage usually several kilo volts and very high current stress usually range from 1A to 10A. Figures given below can be the best example to show the ESD failures in IC's world, e.g. junction breakdown, metal damage, and gate oxide damage.



(A) (B) (C)

Figure 1 ESD Failure in IC's: (A) Junction Breakdown. (B) Metal Damage. (C) Gate Oxide Damage [3].

Besides these apparent damages to IC's devices minor damages could also happen due to ESD that can appear later on and affect the functionality of devices [3].

1.2 ESD Stress Model and Test Methods

ESD can happen due to many different kinds of charged sources and thus could be modeled depending upon the nature of the ESD source. Several models exist to best describe ESD events for example, Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) etc. [3]. These models are discussed below.

1.3 Human Body Model

HBM is based on assumption a charged human body discharging through a grounded IC. This model assume that when an initially charged human body touches the IC causes an ESD current transfer between charged human body and the device (IC). When there is no protection circuit hooked up to the device, this huge amount of current can instantly burn the device [4].

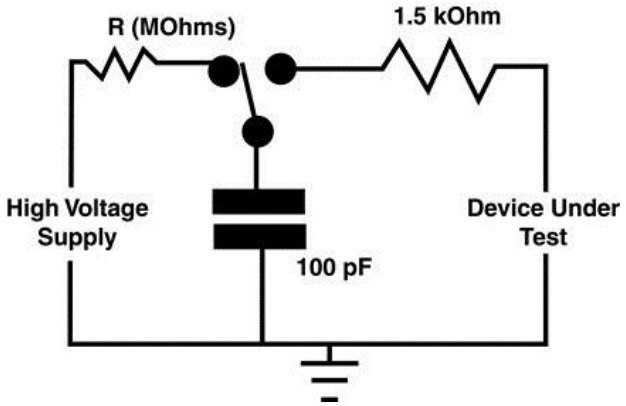


Figure 2 HBM Model Circuit.

A simplified HBM circuit is shown in above figure. A 100pF capacitor charges through high voltage to a certain limit and then discharges by switching component into the device that is being under the test [5].

1.4 Transmission Line Pulse

Transmission Line Pulse (TLP) is one of the most useful tools that an IC industry has been using to characterize an ESD protection structure. In this test, very short ESD pulses are applied to the device under test (DUT) and current through DUT and voltage build up across the DUT can be measured to obtain the DUT's I-V characteristics. A TLP set up is shown in the figure below [6].

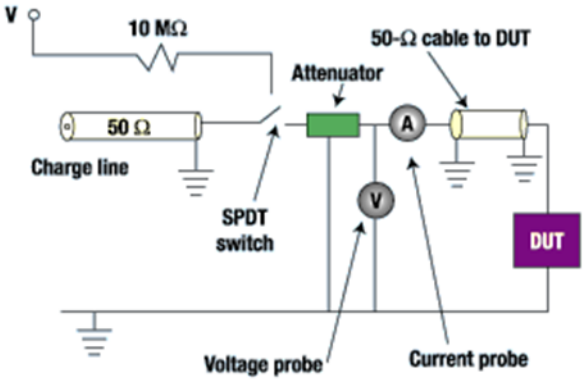


Figure 3 TLP-50: a constant impedance 50 ohm TLP system

In this test, a 50Ω- transmission line is charged initially to a certain voltage level, and then it is discharged to the DUT through constant matching impedance provided by another 50Ω transmission line as shown in the figure above. When stress is applied to the DUT, leakage DC current is measured after each stress applied. The applied ESD stress voltage is increased according to the stress plan and I-V curve of the DUT under ESD stress is obtained and then failure level can be determined from the breakdown point and DC leakage avalanche threshold.

1.5 Charged Device Model

Charged Device Model (CDM) simulates ESD event occurring in production and assembly lines. In this model, charges transfer from ESDs devices to contact metal [7]. A perfect example for CDM is, a device may charge from sliding down the feeder of an automated assembler. When this charge body contacts with any other metal which has lower potential then a rapid transfer charge happens from the device to the contact metal. CDM is found to be more destructive as compare to HBM for some devices. Several different methodologies have been employed to simulate real world CDM model. Current work in this field is focused on two separate CDM test methods; one termed as CDM that best replicates real charged device ESD event and the other explains the devices that are inserted in sockets and then charged and discharged in the socket. This second method is called socket discharge model. A typical test circuit that is used to test CDM is given below [8].

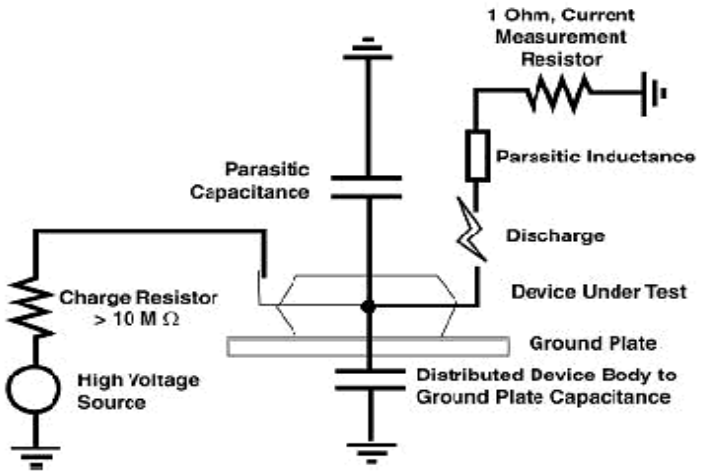


Figure 4 Charged device model.

1.6 RF ESD Protection

RF application in electronic continues to increase and providing ESD protection for such RF circuits is forcing additional complexities into design. In order to apply ESD protection to RF circuits, protection should be designed in such a way that it should not affect the signal under normal operating conditions. A simple ESD protection is shown below [9].

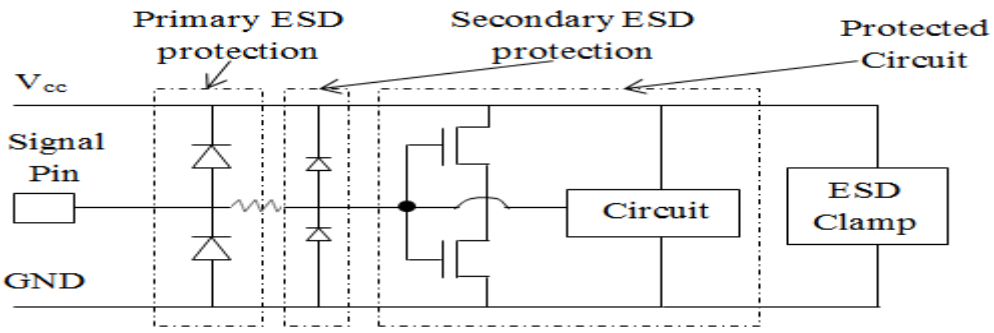


Figure 5 A Simple ESD chip level protection circuit.

The primary ESD protection diodes are used to carry ESD current and voltages to supply rail and then shunt them to ground through the ESD clamp. Whereas secondary protection diodes are used to limit the voltage below failure level to protect the gate oxide of input receiver.

During the normal operating conditions these protection devices add resistance and capacitance to the signal which is not good thing for high frequency applications because capacitances becomes a short for the signal. Therefore protection device has to be designed very carefully otherwise it can cause impedance mismatch and reflect the signal back at high frequency and also can cause inefficient power transfer [10]. Some parameters are very important to consider when designing RF ESD protection. These parameters are given in "RF ESD Design Parameter" section of this chapter.

1.7 RF ESD design parameters

Reflection Coefficient:

Reflection coefficient is a function of characteristics and load impedance as given below.

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0) \quad (1)$$

Where Z_L is load impedance and Z_0 is characteristics impedance.

The above equation can also be written in term of admittance, $Y_0 = 1/Z_0$

$$\Gamma = (Y_0 - Y_L)/(Y_0 + Y_L) \quad (2)$$

Normalized Reflection Coefficient:

Reflection coefficient can be normalized with characteristics impedance is called Normalized Reflection Coefficient. It is written as follow.

$$\Gamma = ((Z_L/Z_0) - 1)/((Z_L/Z_0) + 1) \quad (3)$$

Return Loss:

It is given as follow:

$$RL\ (dB) = -10 \log \left| \Gamma \times \Gamma \right| = -20 \log \left| \Gamma \right| \quad (4)$$

Voltage Standing Wave Ratio:

Voltage Standing Wave Ratio (VSWR) is defined ratio of maximum voltage and minimum voltage.

$$VSWR = V_{MAX} / V_{MIN} \quad (5)$$

We can also express gamma (Γ) as a function of VSWR as follow.

$$\Gamma = (VSWR - 1) / (VSWR + 1) \quad (6)$$

Missmatch Loss:

The loss of signal from one terminal, usually source terminal to the other terminal, usually load terminal is called Missmatch Loss. It just tells the ability to deliver power from source to load.

$$ML = (\left| 1 - \Gamma_S \Gamma_L \right|^2) / [(1 - \left| \Gamma_S \right|^2) (1 - \Gamma_L \left|^2 \right.)] \quad (7)$$

If the source characteristics impedance is Z_0, and reflection coefficient is zero i.e $\Gamma = 0$ ML can be written as:

$$ML = 1 / (1 - \left| \Gamma_L \right|^2) \quad (8)$$

Quality Factors (QF):

Quality factor is defined as ratio of the desired to the undesired electrical characteristics. For any physical element there is always an undesirable parasitic that degrades the functionality of the element, for example, an inductor has a parasitic resistance associated to it. These parasitic changes the ideality of the elements and hence functionality from ESD prospective.

In the series expression, QF is defined as ratio of series reactance, X_S and the series resistance, R_S as follow:

$$Q = X_S / R_S \quad (9)$$

For a parallel configuration;

$$Q = R_P / X_P \quad \text{or} \quad Q = B_P / G_P \tag{10}$$

Where B_P is susceptance and G_P is conductance of the equivalent parallel circuit.

Noise Figure:

The noise figure is ratio of actual noise power to the thermal noise power.

$$NF\ (dB) = 10 \log[P_N /(KT)B] \tag{11}$$

Where P_N is noise power, T is temperature, B is bandwidth, and K is Boltzmann's constant [11].

Device Geometry:

Geometry of the device also has a very important role in the design of an ESD RF circuit. The device that is used in this work is diode. This eight fingers diode has length 460nm and has width of 23.12u. This work is done in 0.18u SOI technology.

1.8 S-Parameter Analysis

Scattering parameters or S-parameters are used to describe behavior of linear network in steady state. Characteristics of a network can be represented by S-parameter matrix for an RF system. At a very high operating frequency the wavelength of the signal becomes comparable to the device dimensions. In such a case we cannot ignore the wave nature of the signal. At the same time, it becomes hard to calibrate the network by doing pure open and short loads at higher frequency because of the small parasitic can greatly affect the network impedances [12].

S-Parameters are very important in RF design. Also it is easy to work with S-Parameters at higher frequencies as compared to any other two port network. These parameters are simple and can give detailed insight into measurements and problem modeling. These parameters are linear by default to represent the linear behavior of a network [13].

The linear equations describing two-port network is given below.

$$b1=S11*a1+S12*a2 \quad (12)$$

$$b2=S21*a1+S22*a2 \quad (13)$$

S11, S12, S21, and S22 are S-Parameters and they are defined as below.

$$S11=b1/a1\ |_{a2=0} \quad (14)$$

$$S12=\ b1/a2\ |_{a1=0} \quad (15)$$

$$S21=\ b2/a1\ |_{a2=0} \quad (16)$$

$$S22=\ b2/a2\ |_{a1=0} \quad (17)$$

Here S11 is input reflection coefficient when a2 is set equal to zero and $Z_L=Z_o$ by terminating out pout port and load match. S22 is output reflection coefficient when input port is terminated, setting Vs=0. S21 is forward transmission gain when output port is terminated in a perfect Z_0 load. S12 is representing reverse transmission gain when input port is terminated in a matched load [14].

1.9 Harmonic Balance analysis

When designing ESD Protection devices, it is very important to consider any distortion that we can get in our RF signal. Our goal is to keep that distortion in RF signal at minimum level. Therefore, harmonic balance is very important tool to measure all such distortion in RF signal.

Harmonic balance is very attractive steady state frequency domain analysis for simulation of non-linear circuit and system. It is best choice for simulating, RF and Microwave problems because they are handled in frequency domain. Harmonic balance has several advantages over a conventional time domain steady state analysis. Using harmonic balance we can calculate frequency domain voltages and currents by directly calculating the steady state spectral content of voltages and currents of a circuit [15].

Harmonic balance is very handy when it comes to nonlinear circuits. Harmonics generated by the nonlinearity in some circuits are very important because they determine the performance of the circuit. Harmonic balance can analyze these undesirable distortions that cause harmonics and help minimizing them. The way that harmonic balance work is, the actual is circuit is partitioned into two sub-circuits, one is linear sub-circuit and other is non-linear sub-circuit and are connected through a number of ports. We can choose state variables such as port voltages represented by frequency domain complex phasors at all frequencies of interest. The linear sub-circuit is evaluated in frequency domain and non-linear sub-circuit is in the time-domain. Then these responses are converted by using Fourier transform into frequency domain. Given below is the set of harmonic balance equation.

$$F(V) = I_{NL}(V) + I_{L}(V) = 0 \tag{18}$$

Where V is used to represent state variables, I_{NL}, and I_L are representing the responses of nonlinear and linear sub circuits respectively. The nonlinear part of harmonic balance equations are solved by using Newton iterations and by optimization. Starting point is very crucial for the convergence so these convergence problems are overcome by continuation method [16].

CHAPTER 2

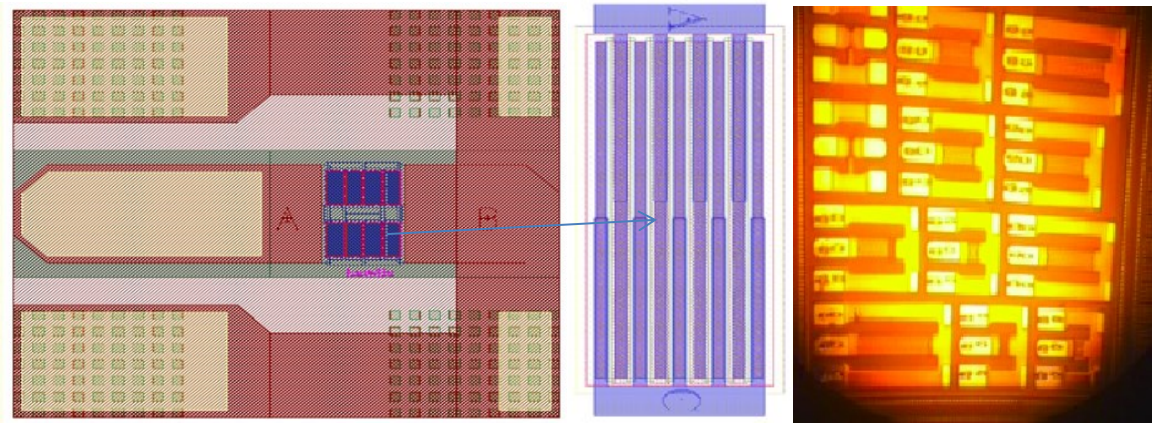
Experimental Test

2.1 SOI 0.18 um Technology

For this research, IBM SOI 0.18um technology is used. This technology has a very high resistivity substrate and it is very appealing technology in manufacturing industries nowadays. Due to its high resistivity substrate it can provide better isolation between laterally build devices. Some of the key advantages of this technology are better stability, linearity and reliability of the structures as compare to some other technologies [17].

2.2 Experimental Test Procedure

The experiments part includes testing using Celestron I and Murray Microwave system. HBM and TLP testing were done using Celestron I while RF testing's were done using Murray Microwave Network Analyzer and Agilent Parametric Analyzer. A simple test structure used for experiments is in ground signal ground format for 4x4 diode stack is shown figure 6 (A). Also a single diode is shown in figure 6(B) in exploded view. A picture is also taken to show how the structures look like under a microscope that is being test given in figure 6(C).



(A) (B) (C)

Figure 6 (A) Test Structure 4x4; (B) A Single Diode; (C) Test Structure under Microscope

2.3 TLP Test

For TLP testing the adopted test plan includes a start voltage, stop voltage and step voltage of the applied pulse. A test plan for TLP is given in the table below.

Table 1

Experimental TLP Test Plan

TLP Test PLAN	
Start Voltage	1V
Step Voltage	2V
Stop Voltage	200V
Current Constraints	2.2A

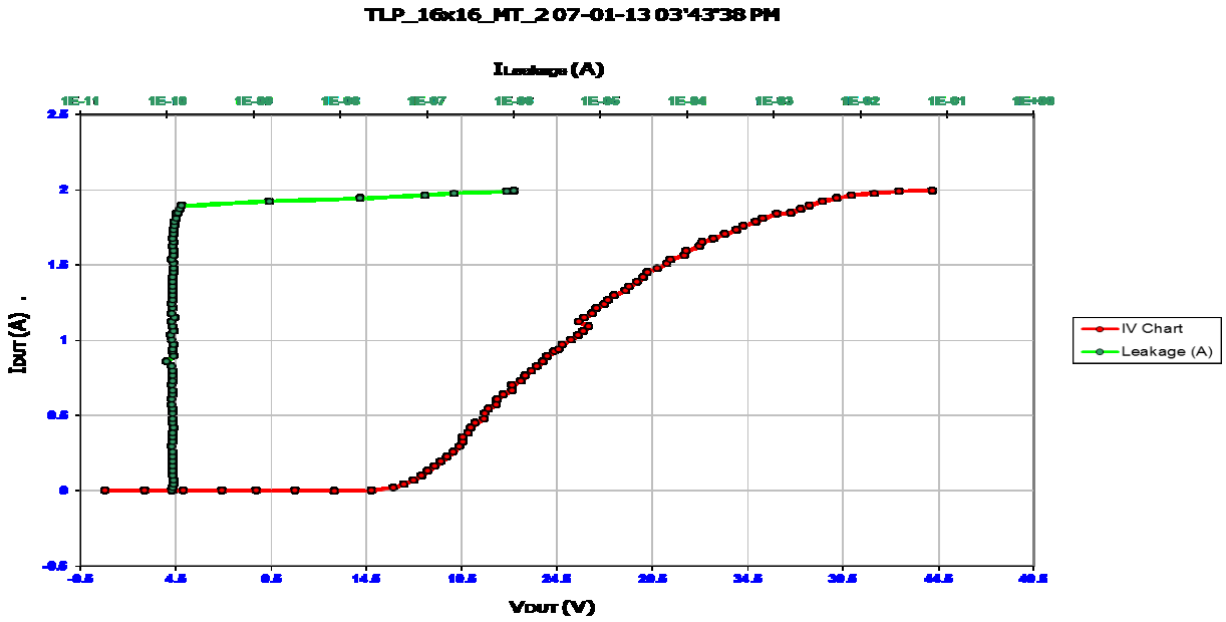


Figure 7 Experimental TLP test result of Stack 16x16.

2.4 Individual Structure TLP Test Data

The figure 7 shows the experimental test curve obtained from test structure (Stack 16x16). It is very clear from the Leakage data that observed device is failed at close to 1.9A TLP current. The plot shows that failing current is 1.89A at voltage 37.78V while applied pulse voltage was 147V. So the maximum peak current for the stack 16x16 is 1.89A and maximum

peak voltage is 37.78V. Any increase in voltage beyond this point leads to the permenant damage to the device. Therefore withstand volatage for the stack 16x16 is 37.78 V.

2.5 Grouped TLP IV Curves

The test diodes structure varies from stack 4x4, 12x12, 16x16, 20x20, 24x24, and 28x28. The figure 8 shows that almost all the diode stack failing at 2A TLP current. But the withstand voltage for each diode stack is different which is very clear from the figure.

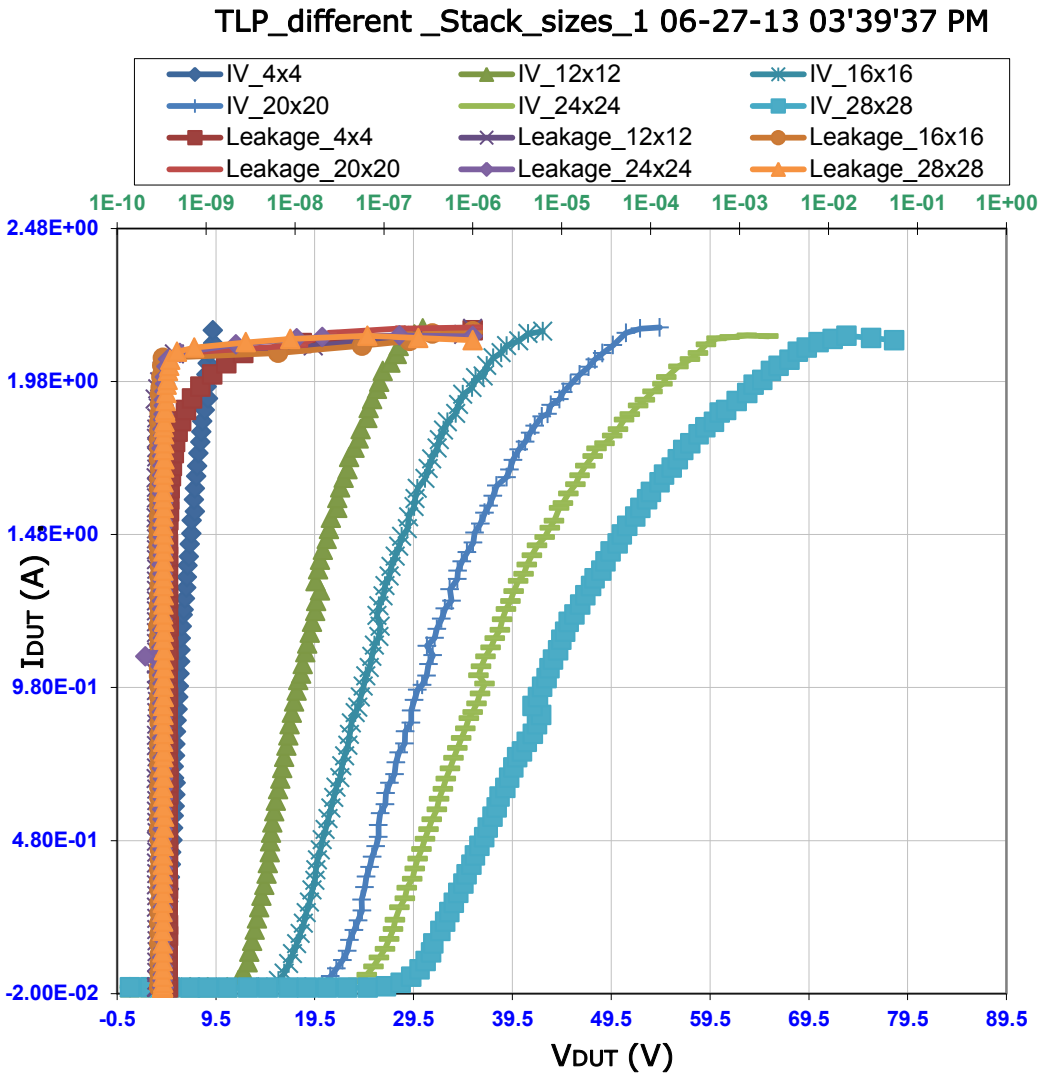


Figure 8 TLP IV curves for all structures

Table 2

TLP withstand Voltages and Withstand Current for all stacks

Stack Size	Withstand Voltage (V)	Withstand Current(A)
4x4	8.58	2.002
12x12	27.84	2.069
16x16	37.58	2.056
20x20	48.616	2.07
24x24	58.293	2.07
28x28	69.32	2.09

To better see the withstand voltages and withstand current for each diode stack, a table is given below which contains all withstand voltages and currents against their diode stack.

2.6 HBM Test

For HBM, adopted test plan includes a start pulse voltage, a stop pulse voltage and step size. A test plan for HBM testing is given in the following table.

Table 3

Experimental HBM Test Plan

HBM Test Plan	
Start Voltage	50V
Stop Voltage	4000V
Step Size	49V
Voltage Constraint	4000V

2.7 Individual Structure HBM Test Data

For HBM testing, positive ESD pulses were applied to different sizes of diodes stack. According to the test plan first pulse is set to 50V and then increased with step size of 49V until 4000V or until the structure failure. After each applied pulse a leakage current was taken which determines the structure failure. Figure below is the curve obtained from the Celestron I for HBM test for the diode stack size 16x16. This curve shows the device completely failed at almost 3800V.

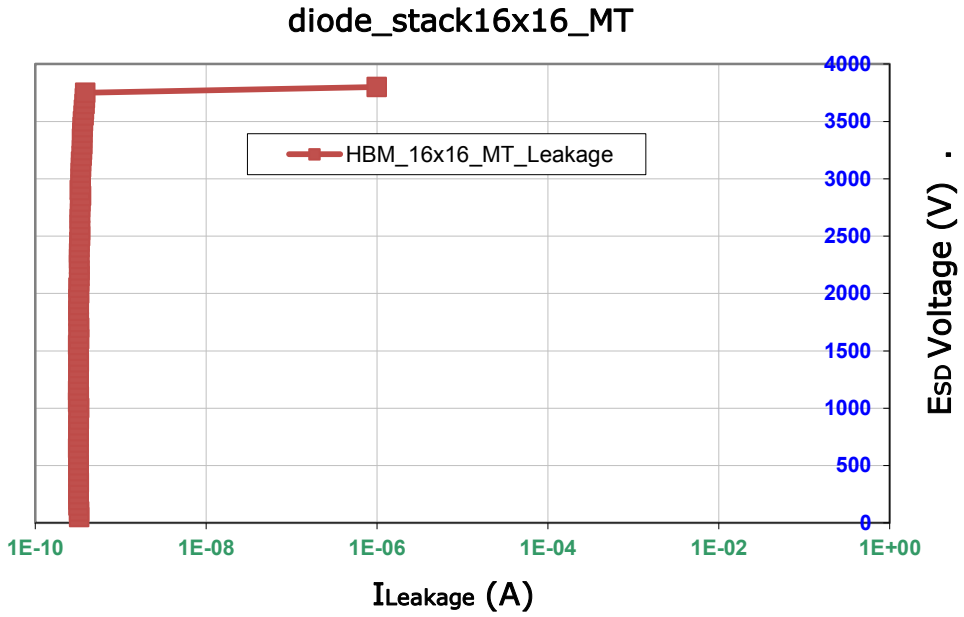


Figure 9 Experimental HBM Test Result for Stack 16x16.

From the table below it is easy to see that leakage current was between 3.2901x10^(-10)A to 3.876x10^(-10)A for an applied voltage range of 50V to 3750V. This leakage current was very small on a very wide range but then leakage current shoots to 9.999x10^(-7) at an applied voltage of 3800V resulting in complete device failure.

Table 4

HBM Test Result for Stack 16x16

Test Pulse (V)	Leakage (A)
50	3.2901E-10
100	3.29915E-10
150	3.23329E-10
……	…….
3650	3.78989E-10
3700	3.84269E-10
3750	3.87261E-10
3800	9.99997E-07

2.8 Grouped HBM Leakage Curves

HBM test was done on diodes stack size 4x4, 12x12, 16x16, 20x20, 24x24, 28x28. For each HBM test for given structure, leakage current curve and test pulse data was obtained. Following is the plot for all the HBM leakage curves together. Individual plots are given in the appendix. It is very obvious from the figure that almost all the structures are failing at an applied voltage of 4000V but a soft failure has happened between 2500V to 3000V.

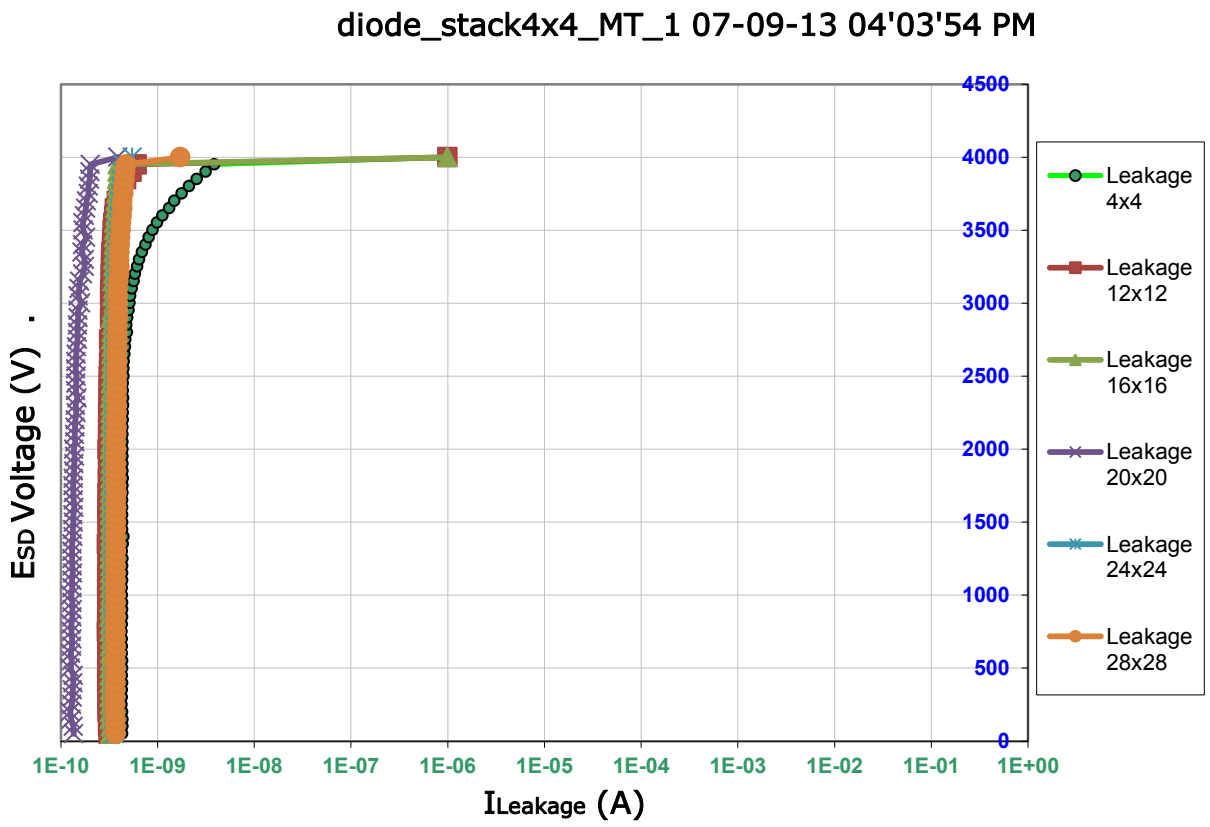


Figure 10 HBM Test Leakage curves for all structures.

2.9 Small Signal Analysis

Small signal analysis was done using Murray microwave system. In this experiment, capacitance of the diode stack is measured against the frequency for all stacks 4x4, 12x12, 16x16, 20x20, 24x24, and 28x28. For this experiment, frequency is swept from 0.5GHz to10 GHz and capacitance is measured which is oscillating on very negligibly small range. It is very important for a design engineer to know how much capacitance a black box contains. In this case, diode stack is seen as black box and ignoring what is inside it and capacitance is measured. From the figure below, we can read capacitance for each stack of diode. The capacitance for diode stack 4x4 is almost 48fF, for 12x12 diode stack is 18fF, and for 16x16 diode stack is 16fF and so on. We see that capacitance has decreased for higher stack number because we are putting

more and more diodes in series which means more and more capacitances in series. Capacitances add up inversely in series which causes a significant decrease in capacitance for higher order stack. Also we see that capacitance for diodes stack 20x20, 24x24, and 28x28 is almost same showing the system has reached minimum capacitance measurement limitation. Therefore we will see a significant difference for higher order stack between simulated results and experimental results in next chapter, data analysis.

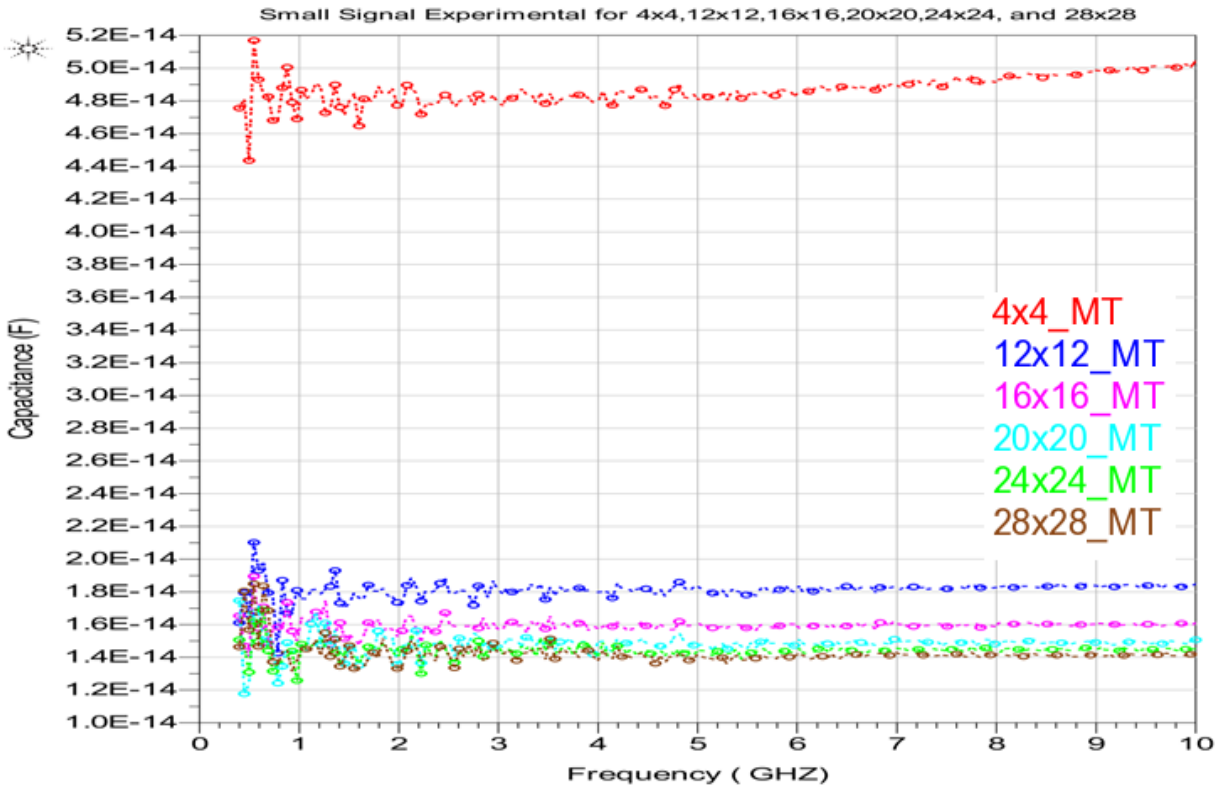


Figure 11 Small Signal Test results for all structures

2.10 Large Signal Analysis

Large signal analysis was done using network analyzer. In large signal analysis input power is swept from 10dbm to 40dbm and output is obtained on 1 through 5 harmonics due to nonlinearity of the device. Large signal analysis was done on diode stacks 4x4, 12x12, 16x16,

20x20, 24x24, and 28x28. Following figure shows the experimental results obtained for the large signal for diode stack 16x16. We can see there are five harmonics. The first harmonic is called fundamental harmonic, we see most of the power is delivered on the first harmonic. We also see 2^{nd}, 3^{rd}, 4^{th} and 5^{th} harmonics; these harmonics are produced due to nonlinearity of the device. From the below figure we see that our device is pretty much in linear region from 10dbm to 20dbm because these harmonics are very close to floor level of noise which in this case is -85dbm. But these harmonics start contributing more and more for the higher power from 20dbm to 40dbm in this case. This nonlinearity is caused by several different reasons which we will see in chapter 4 in very detail. Experimental large signal data are given in appendix for other all other stacks.

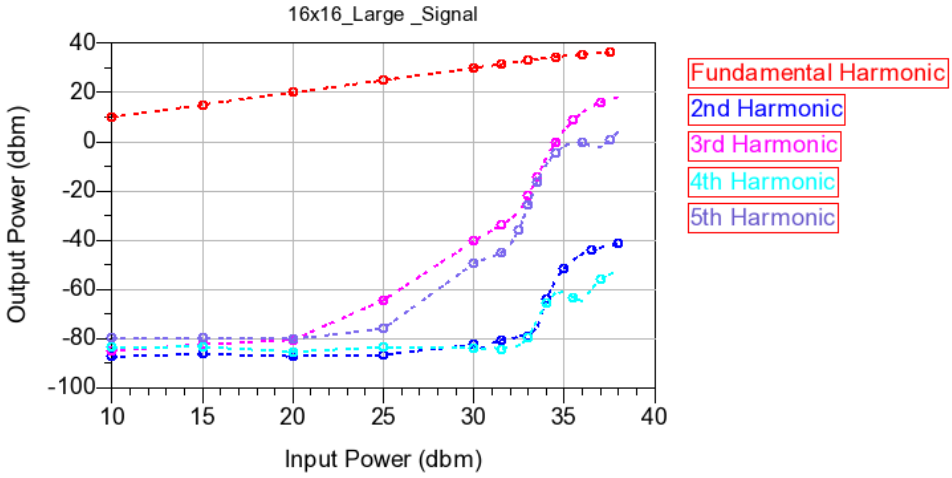


Figure 12 Large Signal Test for 16x16 structure

CHAPTER 3

Simulation Results

3.1 HBM Simulations

Human Body Model (HBM) is model to describe the ESD event when a charged human body touches and discharges to IC. Since resistance and capacitance of a human depending on so many different things so it can vary from person to person. An average resistance of 1500 Ohms and 100pf capacitance is chosen to simulate this model. A test bench is made in Cadence spectre to simulate this model is given below. In this case, symbol (box) is representing the diode stack which is the protection device. In following case symbol contains a diode stack of 4x4. A variable voltage source is also used to supply a pulse voltage. We supply some voltage from voltage source and measure the voltage drop against device under test (DUT) and current going through the DUT.

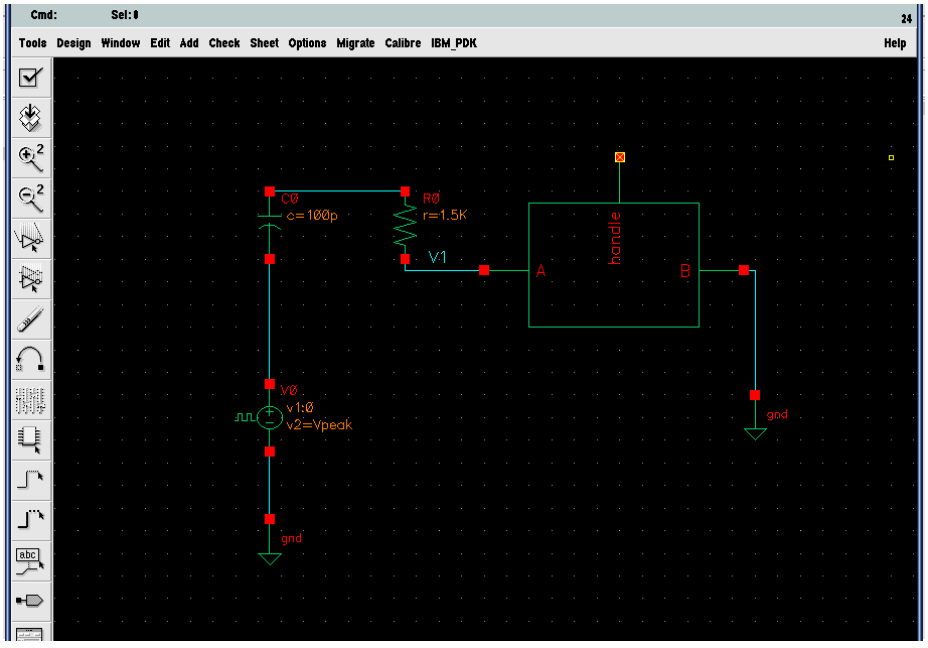


Figure 13 Test Bench for HBM Model

For better explanation diode stack of 4x4 is shown in the figure below. In this figure we can see four diodes are directed downward and same number of diodes directing upward. When a sinusoidal signal is incident on port A or port B, one half of cycle goes through downward directed diodes and other half cycle goes through from other side. Such arrangement was made to avoid the diode reverse biasing because in reverse diodes act as open circuit.

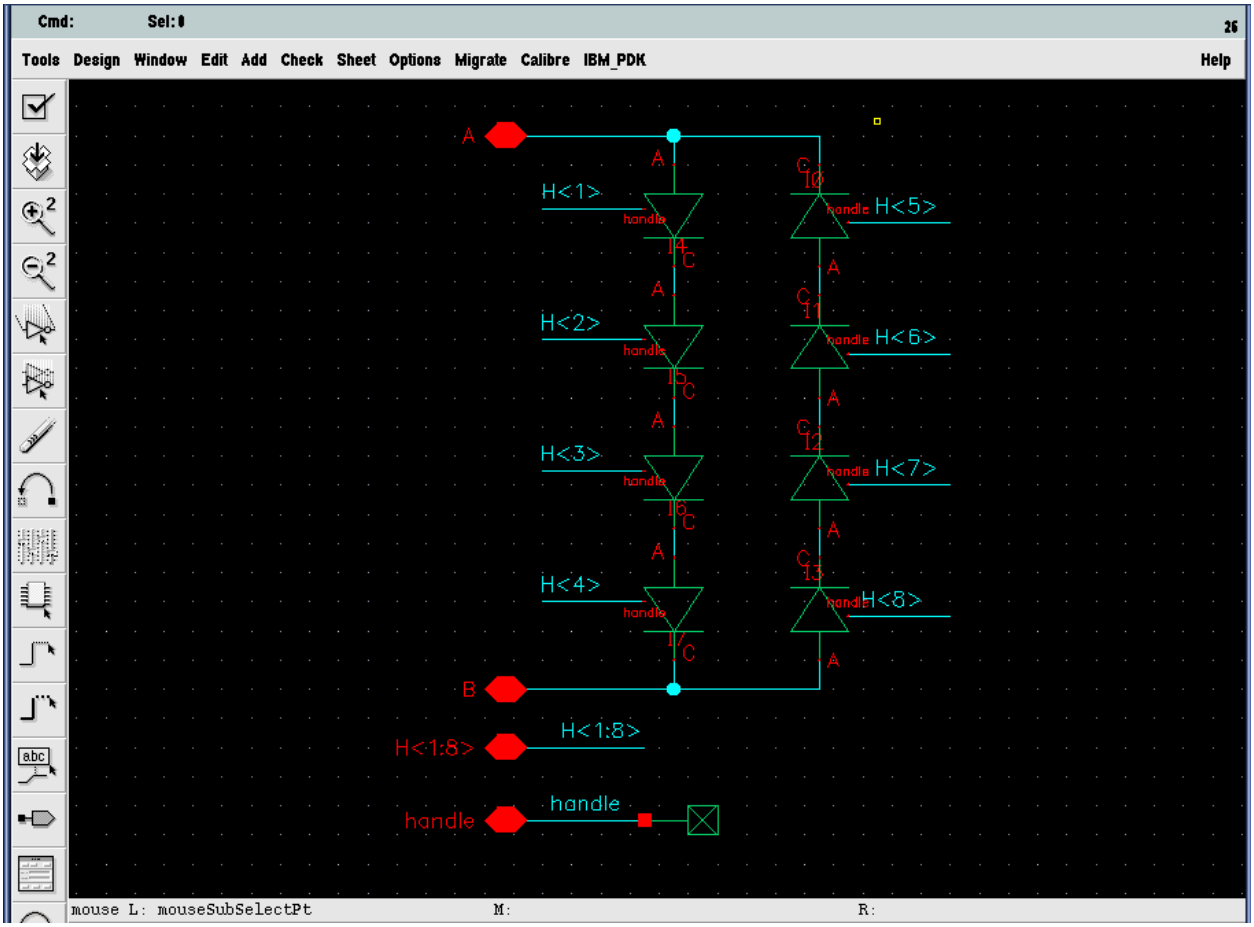


Figure 14 Diode Stack of 4x4

A voltage has supplied ranging from 100V until the signal shows structure has damaged. A table containing applied pulse voltage, HBM terminal voltage against the DUT and HBM current through the DUT is also given below for a diode stack 4x4. Following figure is a snapshot for an applied voltage of 400V to a diode stack of 4x4. It shows that HBM voltage is almost 4.5V and HBM current is almost 0.25A at supplied pulse voltage of 400V.

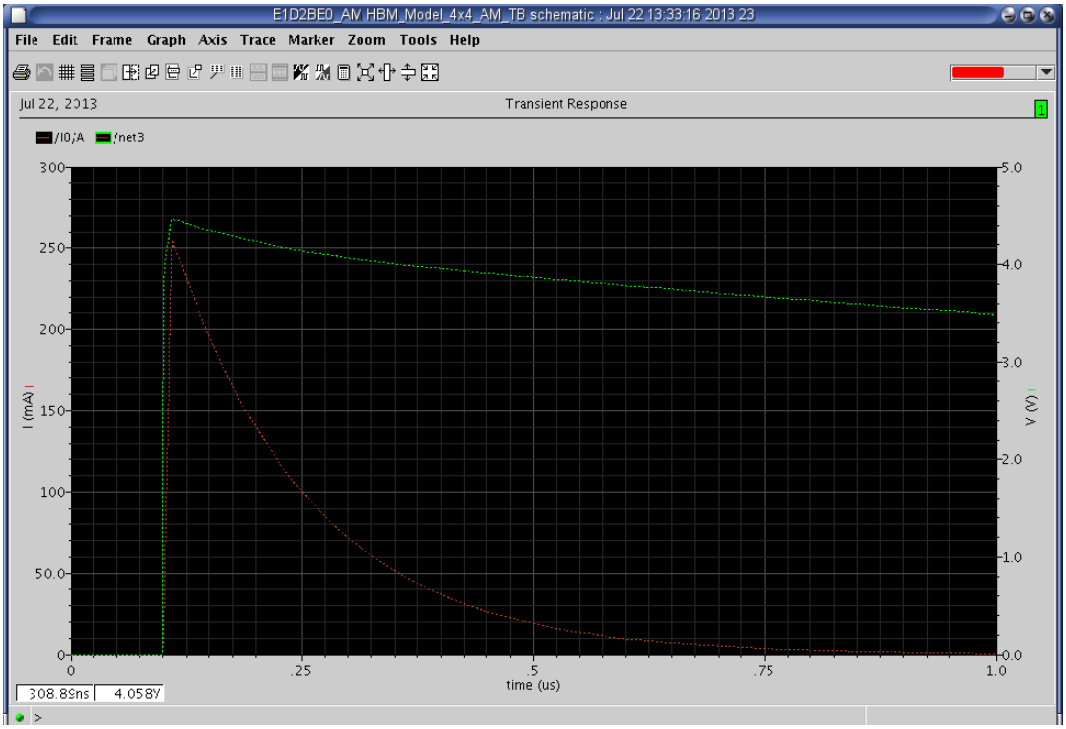


Figure 15 HBM Voltage and Current

Below is the table for HBM data for the diode stack of 4x4. This table shows supplied pulse voltage, HBM voltage drop against the diode stack, and HBM current going through the diode stack of 4x4. Similarly I have recorded the HBM data for all rest of diode stack and 0given in the appendix.

Table 5

Simulation results for diode stack 4x4.

HBM 4x4		
Pulse Voltage(V)	HBM Voltage(Terminal)(V)	HBM current(terminal)(mA)
100	4.04	61.84
200	4.2	126.35
300	4.34	190.76
400	4.47	254
500	4.59	319.5
1000	5.21	641.66

3.2 TLP Simulations

To characterize the protection device TLP model is used. In this model, a transmission line is charged through a voltage source and then discharged through DUT which is explained in detail in chapter 1. A transmission line is made up of inductors and capacitors, LC cells cascaded. For this simulation 19 LC cells are used to implement the transmission line. I have chosen the value of L to be 2.5 nH and value of C to be 1pf which results characteristics impedance to be 50ohms as obtained from below equation.

$Z_o = \sqrt{L/C} = 50\ \Omega$ (19)

There are 19 LC cells cascaded. Only few LC cells are shown and rests are represented by dotted lines in the figure below. A voltage source is used to charge the transmission line and an ideal switch is used to connect and disconnect the transmission line to DUT. When the switch

is opened transmission line is charged and when switch is closed transmission line discharged through the DUT. In this case ideal switch is handled with a separate pulse voltage source, which is operating at 0V and 5V. When this pulse source is at 5V then switch is closed and when it returns to 0V the switch turns open. TLP test schematic is shown below.

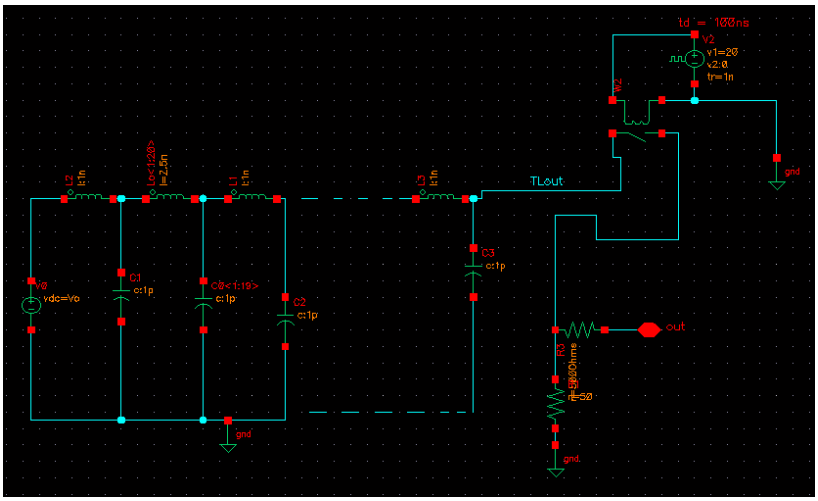


Figure 16 TLP test Schematic

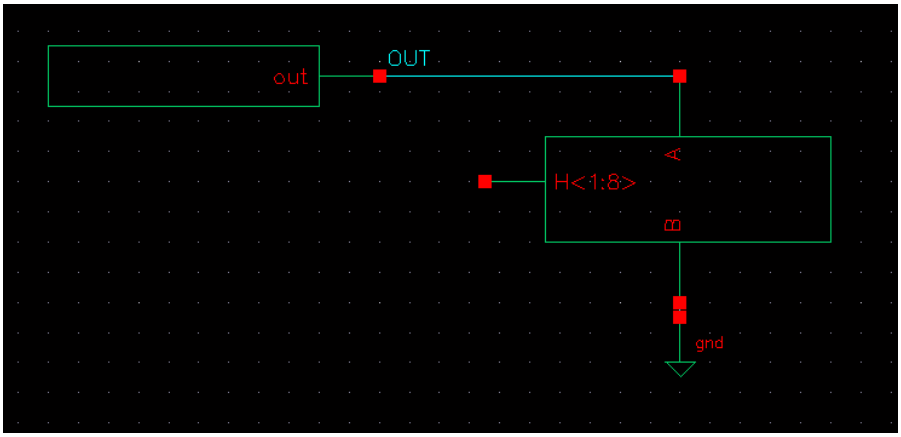


Figure 17 TLP Testbench

In above TLP testbench first symbol on the left represents the TLP test structure of the figure above it and the other symbol represents the diode stack. For diode stack symbol “A” and “B” represents simply IO ports while H<1:8> representing substrate handles of diodes which are floating in this case.

Through the variable voltage source, we supplied pulse voltage according to the test plan and obtained TLP voltage and TLP current against the DUT. The following figure is showing a snapshot of TLP voltage and TLP current at applied pulse voltage of 100V to diode stack of 16x16.

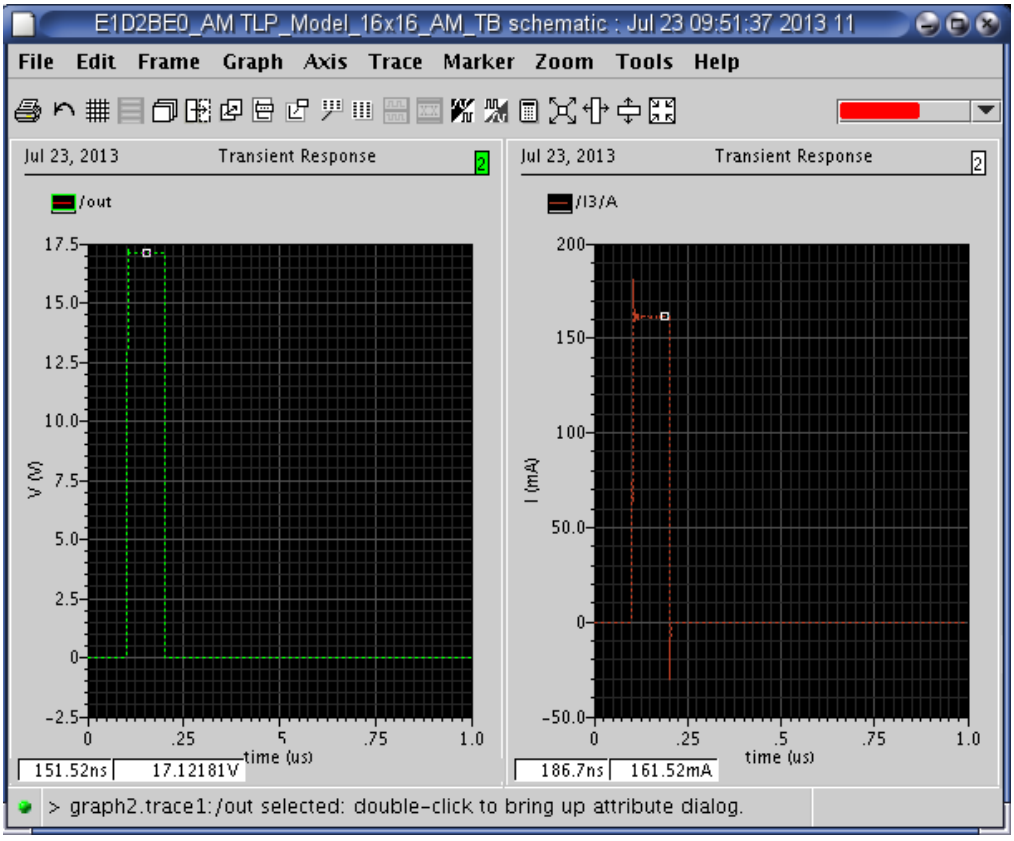


Figure 18 TLP Voltage and Current at pulse voltage of 100V

It is easy to see from the figure that TLP voltage drop against the diode stack of 16x16 at applied pulse voltage of 100V is 17.12V and TLP current is 161.52mA. The bandwidth of the signal is designed to be100ns. The applied pulse voltage started from 20V and increased until TLP signals are fully distorted showing device failure. A table for the TLP current and TLP voltage is given below for the diode stack of 16x16. All rest of data obtained for TLP for different stack sizes are given in appendix. Using this obtained simulated data we plotted IV curve for the each test structure and compared against the experimental data obtained from the Celestron I in the next chapter in detail.

Table 6

TLP Simulation Results for 16x16

TLP 16x16		
Pulse Voltage(V)	TLP Voltage(Terminal)(V)	TLP Current(Terminal)(A)
20	15.1	0.009014
40	15.97	0.04642
60	16.41	0.08464
80	16.78	0.12315
100	17.12	0.16168
150	17.89	0.25785
200	18.62	0.35383
300	20.09	0.54757
500	23.26	0.931174
600	25.05	1.124

Table 6

(Cont.)

700	26.98	1.315
800	29.16	1.508
900	31.46	1.698
1000	34.12	1.887
1100	37.1	2.077

Based on the above tabulated data, we draw an IV curve using TLP voltage and TLP current. We can see the withstand voltage is 37.1V and withstand current is 2.077A for the diode stack of 16x16. Any voltage increase after this voltage, results in device non-recoverable failure. We will see from experiments that soft failure happens before this voltage. This is just simulation which is predicting device failure and it is experimentally verified in chapter 2 and compared again in chapter 4.

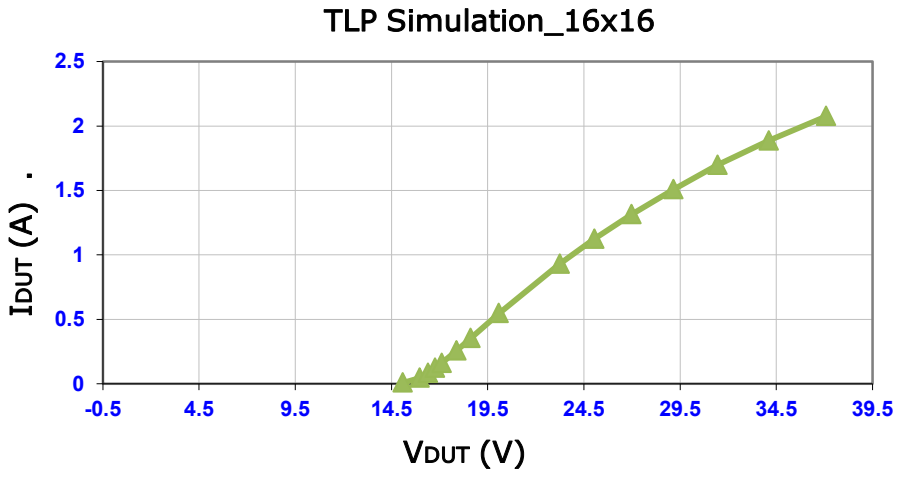


Figure 19 TLP I-V Simulation curve for a diode stack of 16x16

3.3 Small Signal Simulations

For small signal analysis, simulations were done using Advanced Design System (ADS). All the structures were built in cadence environment and then imported in ADS using dynamic link. A testbench for the small signal used is given below.

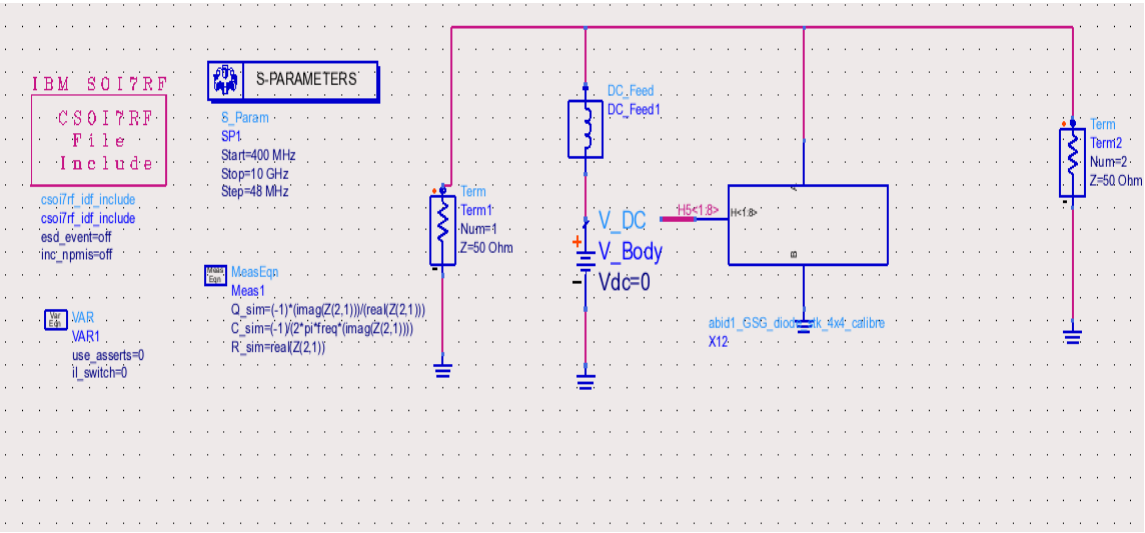


Figure 20 Small Signal Testbench

Two terminations were used to do two port S-parameter simulations. The impedance for both terminations was set to 50ohms. For simulation, frequency is swept from 400MHz to 10GHz with a step size of 48 MHz in S-parameter simulator. In a small signal analysis, the device is seen as black box and capacitance is extracted because it is very important to see how much capacitance is device can present without looking what's inside it. In above testbench 4x4 diode structure is hanging in shunt configuration. To find the capacitance it is assumed that R and C are simply connected in series topology and then two port Z-parameters is used to extract capacitance using equation given below.

$$Z_c = \frac{1}{j \cdot \omega \cdot C} \tag{20}$$

$$C = \frac{1}{j \cdot \omega \cdot Z_c} \tag{21}$$

We can rewrite above equation for two port network by assuming series RC as

$$C = \frac{-1}{\omega \cdot Img(Z_{21})} \tag{22}$$

Where $\omega = 2\pi f$,So

$$C = \frac{-1}{2\pi f \cdot Img(Z_{21})} \tag{23}$$

Also the quality factor is found using Z parameter which is given below.

$$Q = 1 / (\omega\ C\ R) \tag{24}$$

Replacing

$$C = -1 /(2\pi f \cdot \text{Img}(Z_{21})) \tag{25}$$

And

$$R = \text{real}\ (Z_{21}) \tag{26}$$

We get equation for quality factor for two port network is

$$Q = -1 * \text{Img}\ (Z_{21}) / \text{real}\ (Z_{21}) \tag{27}$$

Small signal simulations for the stack size 4x4 , 12x12, 16x16, 20x20, 24x24, and 28x28 on the same grid is obtained which is given below. In this simulation capacitance is obtained as a function of frequency for various stack sizes of diodes. For these simulation substrate handles of all diodes are simply floating and are not connected to anything.

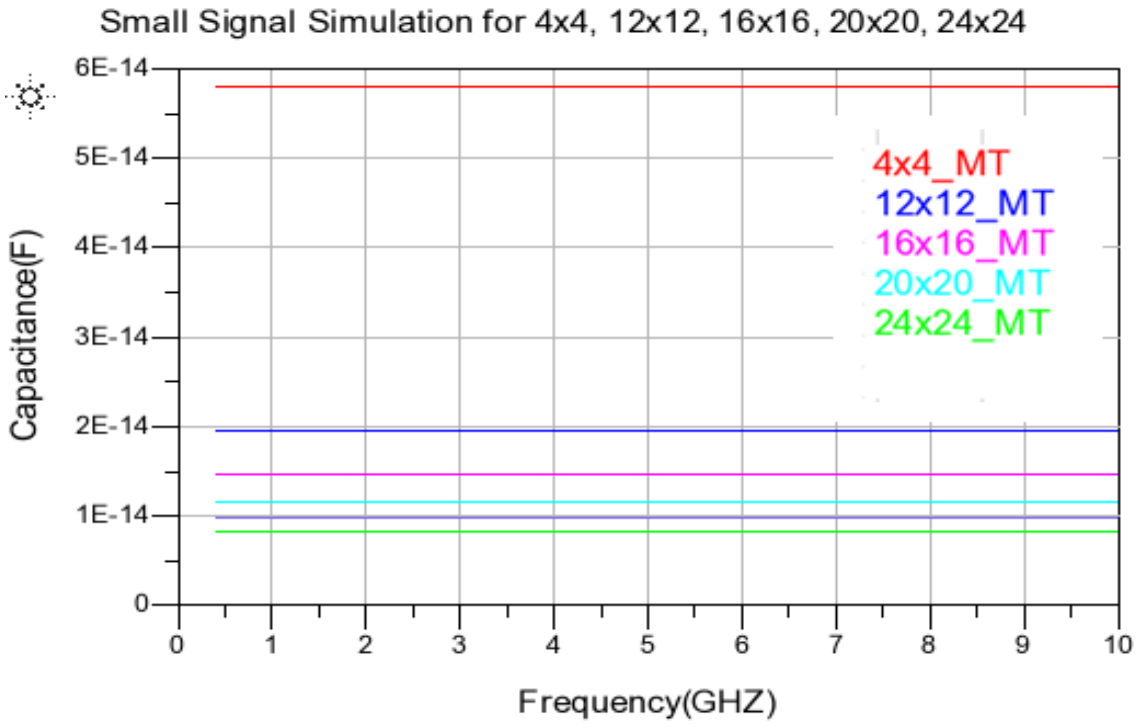


Figure 21 Small Signal Simulation Results for all Structures

We can see that capacitance curves are straight lines meaning that our RC topology in series for two port network fits best. Also it is easy to read capacitances for all different stacks. Capacitance for the stack 4x4 is almost 59fF, for 12x12 is 20fF and 15fF for 16x16 and so on and so forth. We see that capacitance is decreasing as stack is going up because we are putting more and more number of diodes in series which decreases capacitance as capacitance adds up inversely for the capacitors in series. That's why we see huge drop in capacitance for high order stack of diodes.

3.4 Large Signal Simulations

Large Signal analysis was also done in Advanced Design System. All structures were built in Cadence and were imported to ADS using dynamic link available in cadence to do large

signal simulations. A testbench for large signal is shown below. The box is symbol for our diode stack which is hanging in shunt configuration between two terminations each has 50 ohms impedance. For the simulation purpose, input power is swept from 10dbm to 40dbm with a step size of 1dbm and frequency was set to 900 MHZ.

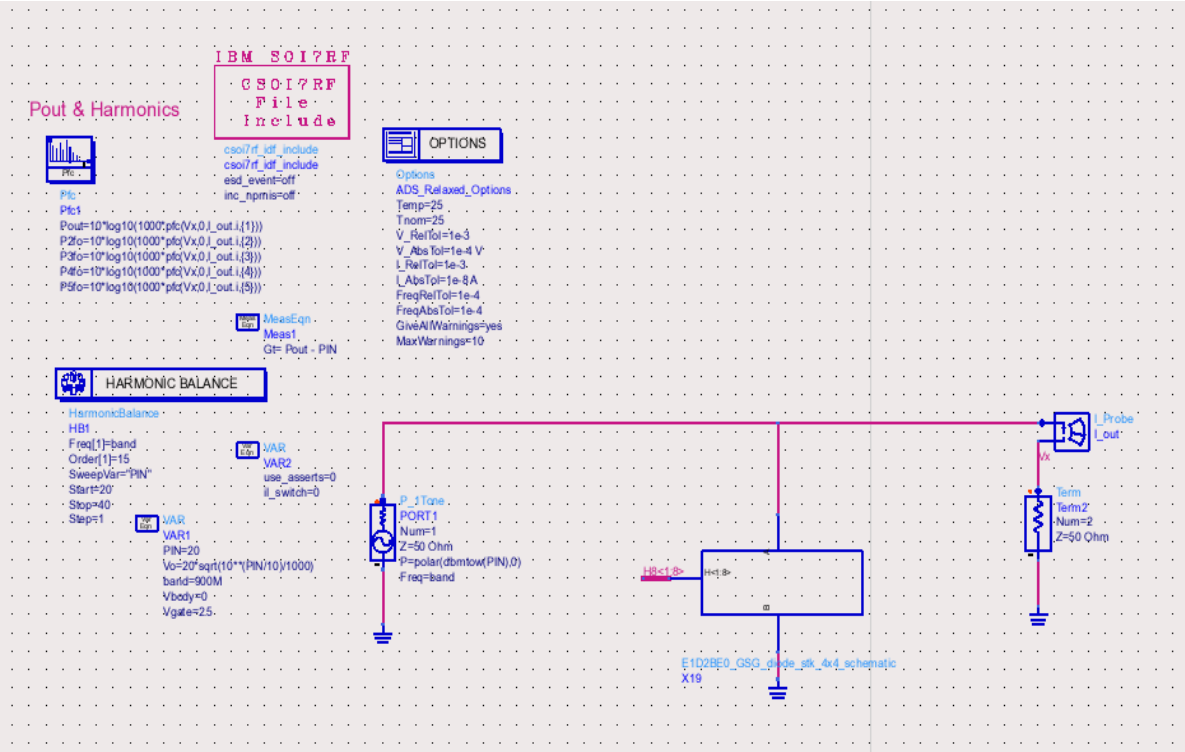


Figure 22 Large Signal Testbench

A simulation result for large signal analysis for diode stack 4x4 is shown in the figure below. Fundamental harmonic or first harmonic delivers most of the output power but some of the power is also delivered on the 2nd, 3rd, 4th, and 5th harmonics due to nonlinearity. The noise floor level is -85dbm and everything is below considered as noise. We can see that 3rd and 5th harmonics (odd harmonics) are above -85dbm and are very significant while 2nd and 4th harmonics (even harmonics) are far below -85dbm which are just considered as noise in this

case. Even harmonics are very far below the noise floor level because out device seems to be very symmetric and even harmonics due to one side of device canceled by the even harmonics produced from the other side of device. In reality, even harmonics are not 0 which is already shown in chapter 2. That's mean we have discrepancy in the nonlinearity or asymmetry of our device. To overcome this discrepancy, modeling has been done on the device which is discussed in great detail in chapter 4, data analysis.

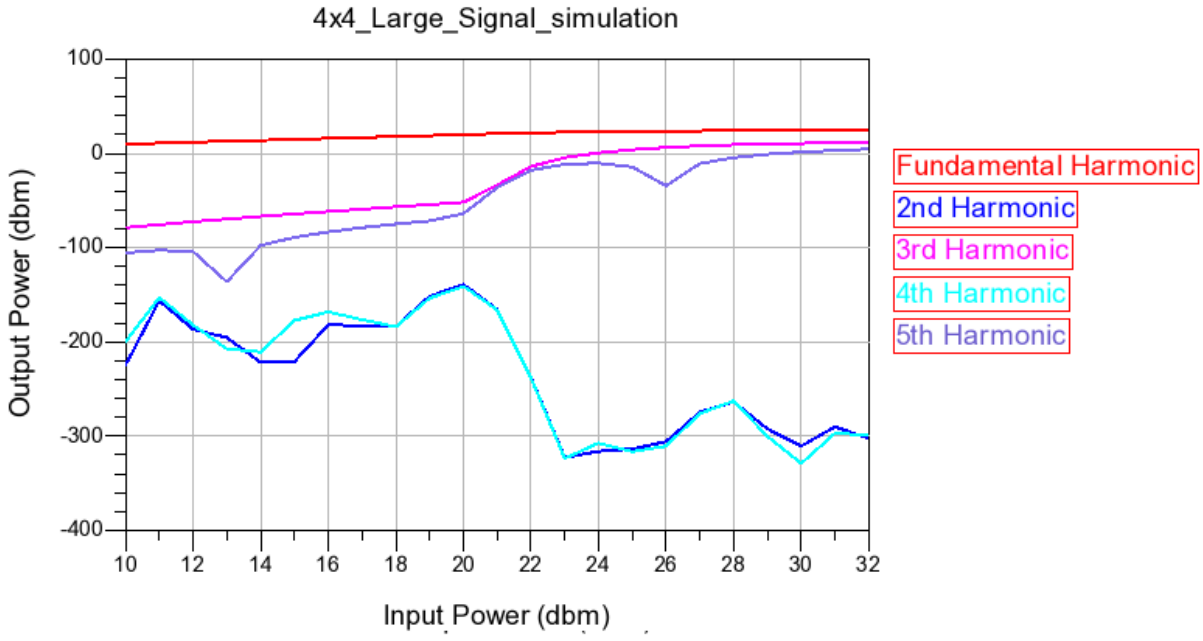


Figure 23 Large Signal Simulation for 4x4 Structure

CHAPTER 4

Data Analysis

This chapter more focuses on comparison between experimental data and simulated data for ESD tests and small signal and large signal analysis. In this chapter, we will show simulated data closely follow experimental data and if not, what steps has been taken to model it better. Any discrepancy between simulations and experiments will be discussed in detail. Most of the discrepancies have been corrected by taking number of steps and any uncorrectable discrepancy has been explained with number of reasons.

4.1 TLP Comparison

The main simulated and tested data for TLP is already given in chapter 2 and chapter 3 and rest of simulations and tests are given in appendix. In this chapter, focus is to compare the obtained results for TLP simulation and TLP test to see if there is any consistency or discrepancy. In order to do so, simulation data and test was plotted on the same figure using Excel program. The test data plot was obtained from the Celestron I and simulation data plot were obtained using Excel based on the simulation data obtained from the Cadence. Following is the figure for TLP I-V curve for both experiments and simulation for the structure 16x16. It is clear from the figure that simulation data curve is almost overlapping experimental data curve and no parasitic need to be added.

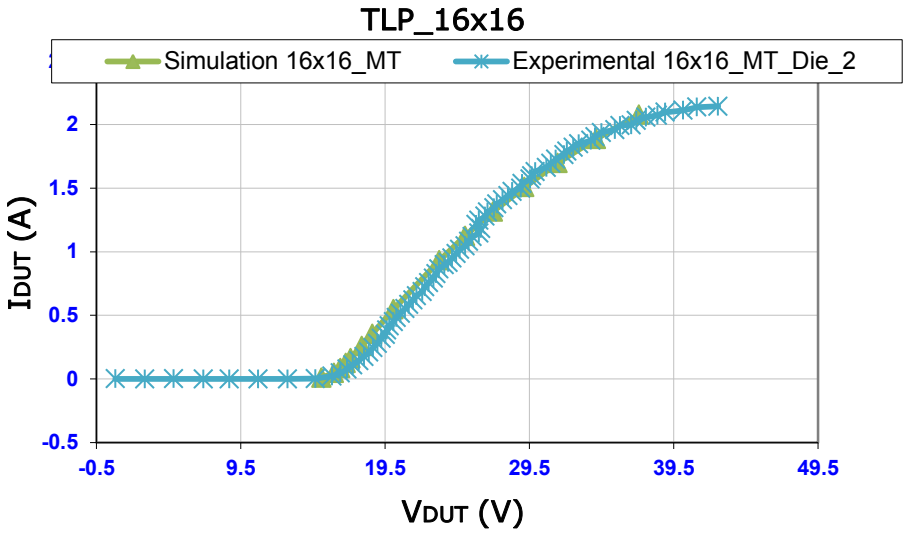


Figure 24 TLP comparison for 16x16

A figure below also attached to show a good experimental and simulation match for TLP for the diode structure of 12x12. The experiment was repeated twice just to see if there is any process variation from stack to stack. It can be seen that simulation curve lies between two experimental curves very closely. Similarly, all the rest experimental and simulation curves were compared against each other and showed a very good match without adding any parasitic All the rest comparisons for TLP test are given in appendix at the end.

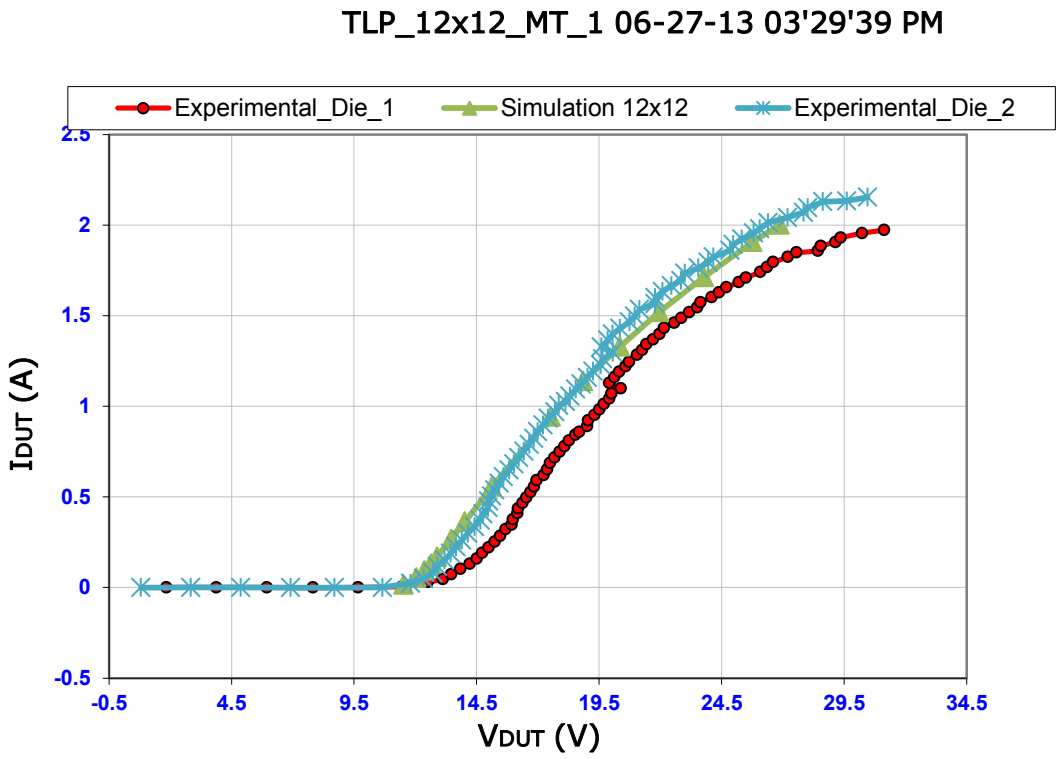


Figure 25 TLP comparison for 12x12

4.2 Small Signal Comparison

The experimental and simulation data for small signal analysis is also listed in chapter 2 and chapter 3 respectively. In order to compare simulation and experimental data, first experimental data was imported into ADS and then plotted on the same figure with simulation in ADS. Small signal analysis was done just on simple diode structure without adding any parasitic capacitance or resistance. From the figure below it is easy to see that there is a huge discrepancy between simulated and experimental data. Simulation data shows very high capacitance for structures and experimental curves are far below than simulations.

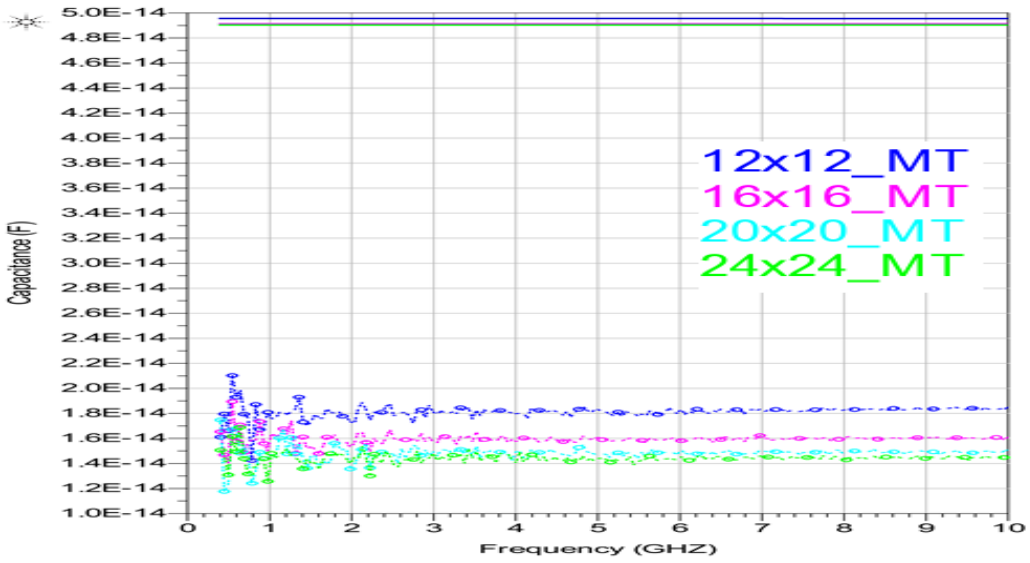


Figure 26 Small Signal Comparison

4.3 Simulation with lateral coupling, "sxmodel"

Simulations in the above figure were done without taking "sxmodel" into consideration. The purpose of sxmodel is to capture coupling effect between any two lateral devices. IBM CSOI7RF model reference guide was used to correctly model lateral coupling effect between two devices. Lateral coupling depends on the geometry of the given devices and separation between them.

The figure given below is a picture of diode cross section with sxmodel. This figure shows vertical sxmodel and lateral sxmodel. The vertical sxmodel is already taken care of by IBM when simulations are conducted but lateral sxmodel requires adding "sxmodel" instance to our schematic and feeding geometrical parameters of the device to the instance.

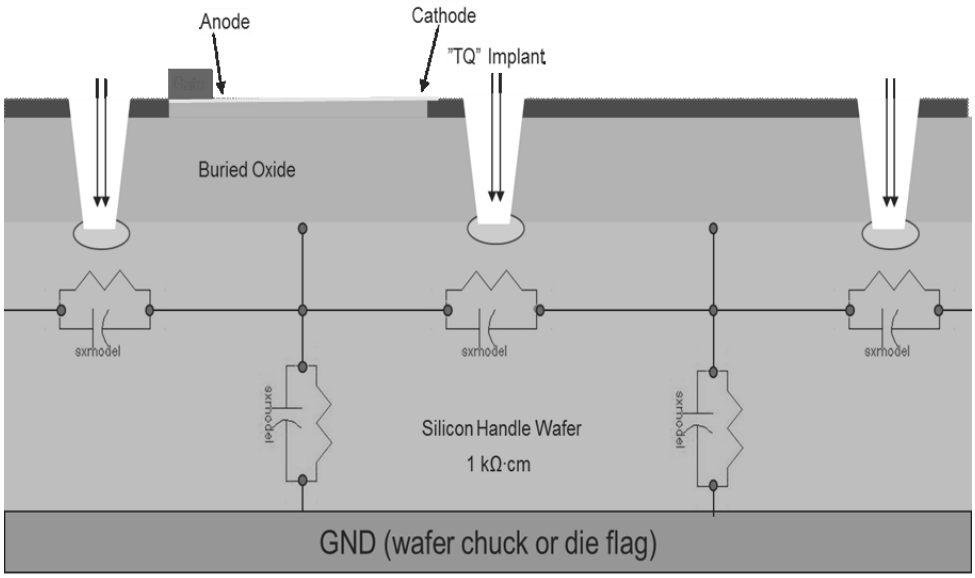


Figure 27 Diode Cross Section including sxmodel

The lateral coupling sxmodel is modeled as R-C parallel circuit as long as substrate is homogenous and has linear behavior. Equations based on IBM reference guide model that were used to model lateral capacitance are given below whereas R derived from relaxation frequency principle.

$$C_{sx} = C_{main} + C_{dw} \quad (28)$$

$$C_{main} = (3.84/x).e_0.e_{si}.W.\ln(1+0.086Y) \quad (29)$$

$$C_{dw} = 0.63.\ e_{0.}\ e_{si}\ \ln(1+dw) \quad (30)$$

Where, (31)

$Y = (L1 + L2) / 2 + x$

$dw = abs\ (W1-W2),\ W= max\ (W1, W2)$

e_0 is permittivity of free space

e_{si} is Silicon permittivity and L1, L2, W1, W2, and x are geometrical parameters.

$$R= 1/ (2*pi*F_r C) \quad (32)$$

Where F_r is relaxation frequency.

The lateral coupling sxmodel instance was added to the schematic between every two adjacent devices to capture lateral coupling effect and small signal analysis was repeated. The

figure below shows the comparison between experimental and simulation after adding sxmodel to structure to capture lateral coupling effect.

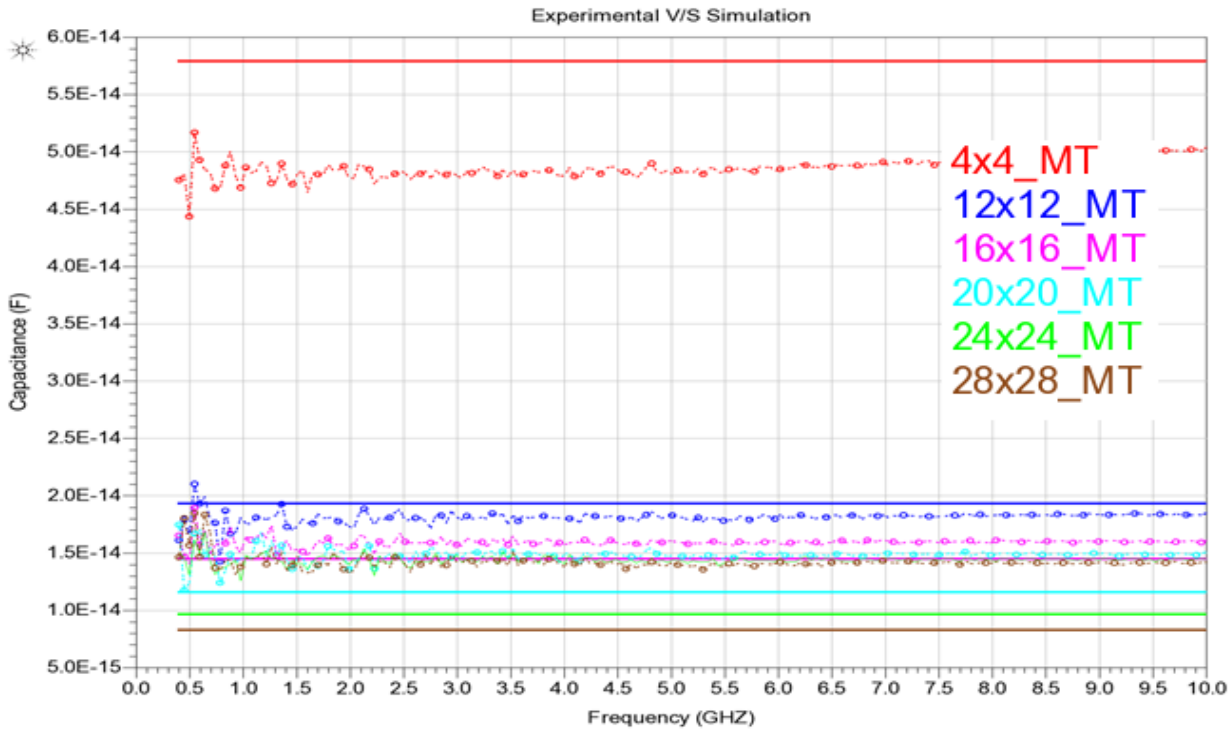


Figure 28 Small signal comparison with sxmodel

It is easy to see that simulation data lines are very close to the experimental curves and structure is better modeled with including lateral coupling effect. For small stack number 4x4, 12x12, and 16x16 experimental and simulation data is matching closely. For higher stack number 20x20, 24x24 and 28x28 experimental curves are just not changing and showing minimum capacitance measuring limitation of the system.

4.4 Large Signal Comparison

In order to analyze any consistency or discrepancy between simulation and experimental data for large signal, harmonic curves for experiments and simulations were plotted on the same figure in ADS. In order to obtain experimental curves in ADS to plot with simulation,

experimental data was stored in .ds file and then imported into ADS. First of all, simulations were done on simple diode stack structure without including any sxmodel and any other capacitance parasitic. In the figure below odd harmonics from simulation were compared against odd harmonics from experimental test.

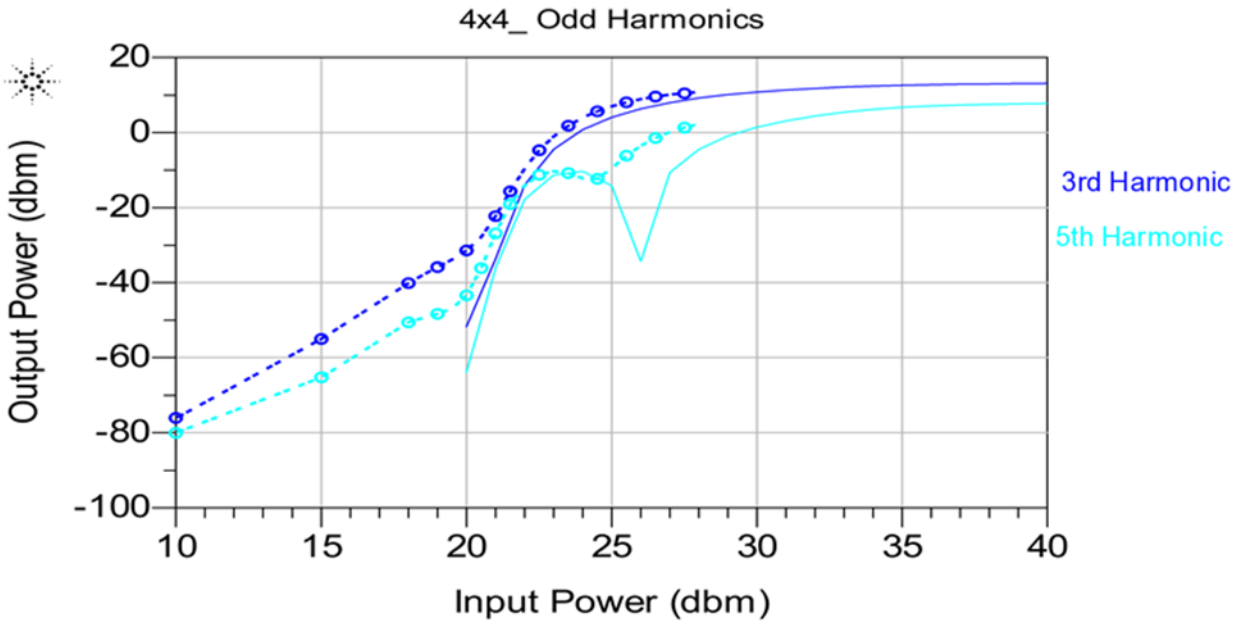


Figure 29 Large signal Odd Harmonics Comparison

The above figure shows odd harmonics for simple diode stack 4x4. It is easy to see that these odd harmonics 3rd and 5th are very close to each other without adding any sxmodel or any other parasitic. In the figure below even harmonics were from experimental test and simulations were compared.

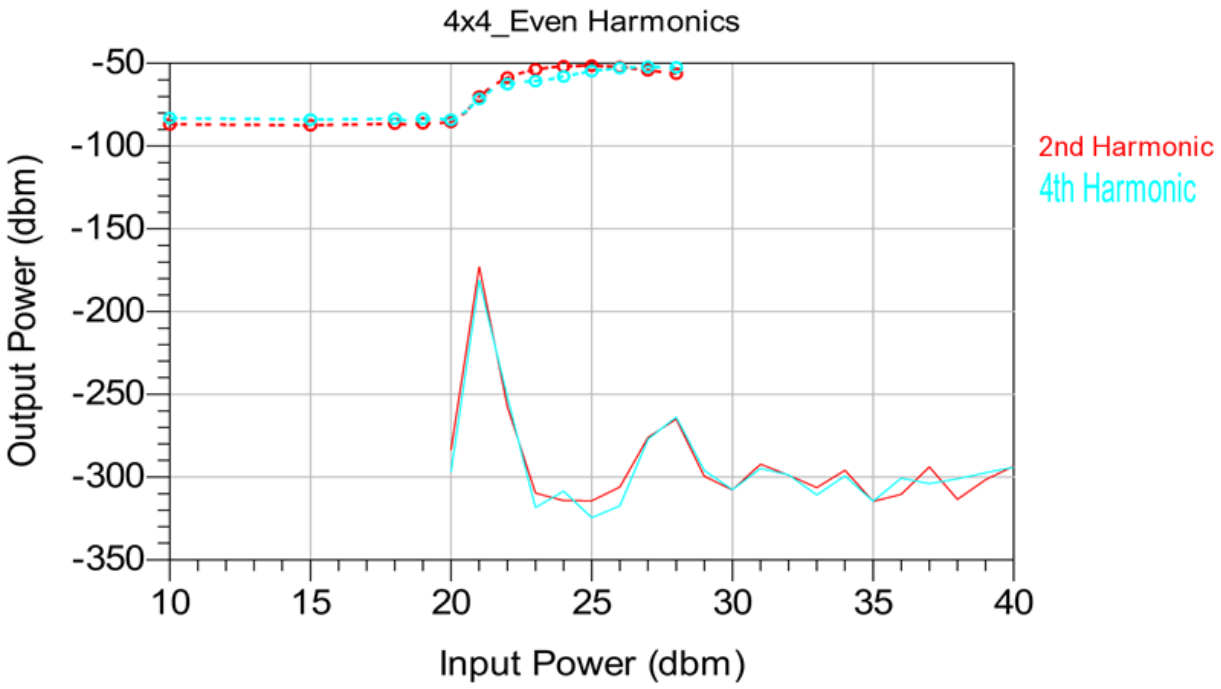


Figure 30 Large Signal Even Harmonics Comparison

From the figure, it can be seen that even harmonics from experiments are very higher than simulated even harmonics. The noise floor level is at -85dbm so simulated even harmonics are far below -85dbm and can be considered as noise, whereas even harmonics for experiments are in significant range and showing a huge discrepancy. Similarly even and odd harmonics were drawn for all other structure 12x12, 16x16, 20x20, 24x24, and 28x28 and observed odd harmonics matching very close and even harmonics were observed way off. A lot of work has been done to model the diode stack to match even harmonics without distorting the odd ones since those are matching pretty close. Several methodologies like modeling variable buried oxide capacitance, sxmodel of lateral coupling, and asymmetric diode geometry were employed in order to capture even harmonics and it was observed that these all have some effect on the nonlinearity of the diode structure but asymmetric diode geometry was very significant than

other. Therefore, an attempt was made to model the diode structure well to capture the nonlinearity through diode asymmetry.

4.5 Simulation with Geometrical Asymmetry

Variation in even harmonics can be caused due to asymmetry in diodes. This asymmetry could be difference in diode's length, diode's width, or doping concentration variation in fabrication process. For this project, asymmetry was emulated using diode's width change. Since Small signal was modeled with lateral coupling sxmodel so in order to be consistent lateral coupling sxmodel is also used for large signal along with emulated geometrical asymmetry of diodes. To emulate asymmetry in diode geometry width of one array of diode of structure 4x4 changed from 23.12um to 23.32um and simulated in ADS and compared against experimental data curves. The figure given below is for diode structure 4x4 with emulated diode asymmetry by width change of diode.

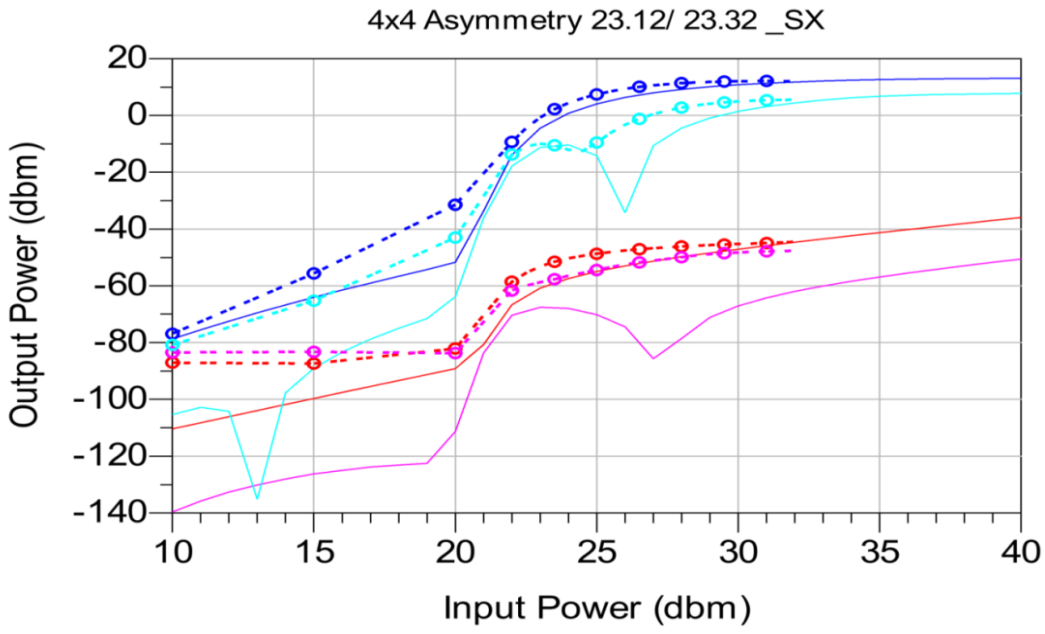


Figure 31 Large Signal comparison with consider sxmodel and asymmetry

It can be seen from the figure that emulating diode asymmetry and sxmodel does not change much odd harmonics but it corrects even harmonics. The noise floor level is -85dbm output so all harmonic values below that are not meaningless and nothing to worry about. It is very clear from the figure that all harmonics have a closer match above -85dbm output power. Similarly, geometric asymmetries for all other diode stacks were emulated by width change and compared against experimental curves and showed a closer match. Comparison curves for large signal analysis for all rest of diode stacks are shown in the appendix. A table given below is made to clear that how much asymmetry is emulated for each diode stack to model the nonlinearity better.

Table 7

Diode stacks and Asymmetries

Diode Stack	Sizes Fwd/Bwd	Asymmetry (um) per Finger	Total Asymmetry	Relative Asymmetry	% Asymmetry
4x4	23.12/23.32	0.20	6.40	0.00865	0.86
12x12	23.12/23.19	0.07	6.72	0.00302	0.30
16x16	23.12/23.19	0.07	8.96	0.00302	0.30
20x20	23.12/23.18	0.06	9.60	0.00259	0.26
24x24	23.12/23.17	0.05	9.60	0.00216	0.22
28x28	23.12/23.17	0.05	11.2	0.00216	0.22

This particular diode was an 8 finger diode. From the table we can see asymmetry per finger is decreasing as diode stack number is increasing and on the other hand, total asymmetry per diode stack is increasing as diode stack number is increasing. Also the relative asymmetry also decreases as diode stack number goes up. For diode stack 4x4, relative asymmetry is 0.8% and for diode stack 28x28, relative asymmetry is 0.2% only which shows a significant drop in relative asymmetry going from lowest diode stack to highest diode stack. A graph is drawn based on the above data to see well. The graph is given below.

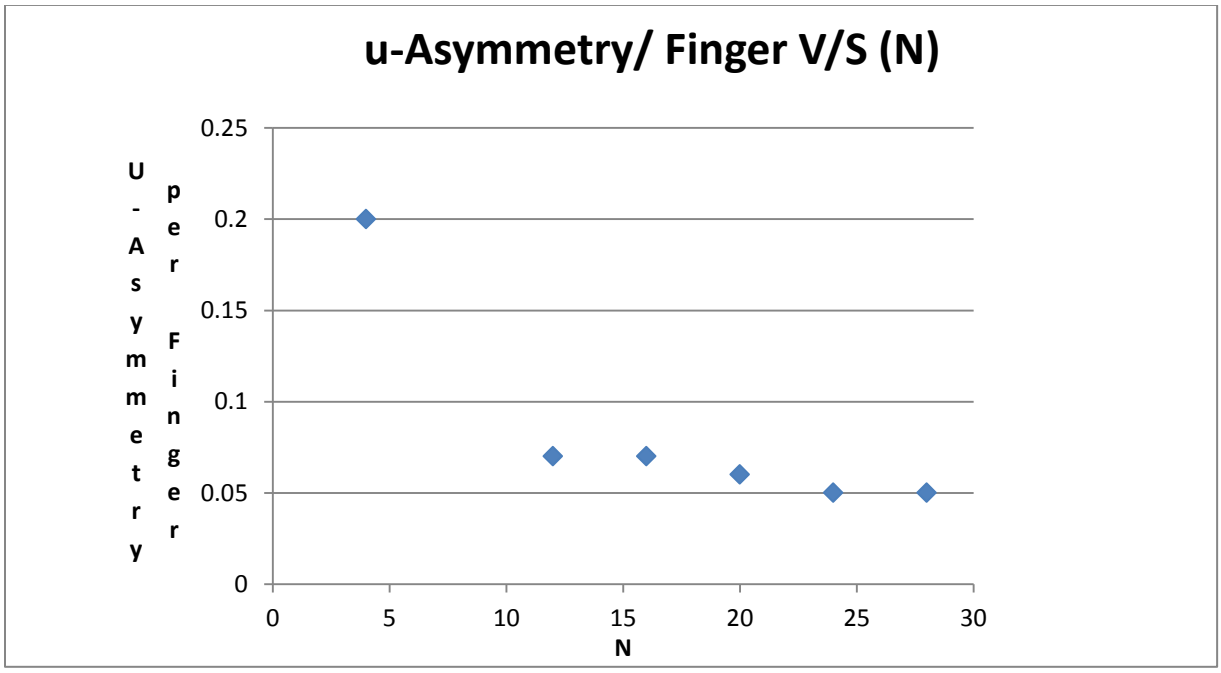


Figure 32 A graph between Diode stack number and asymmetry per finger

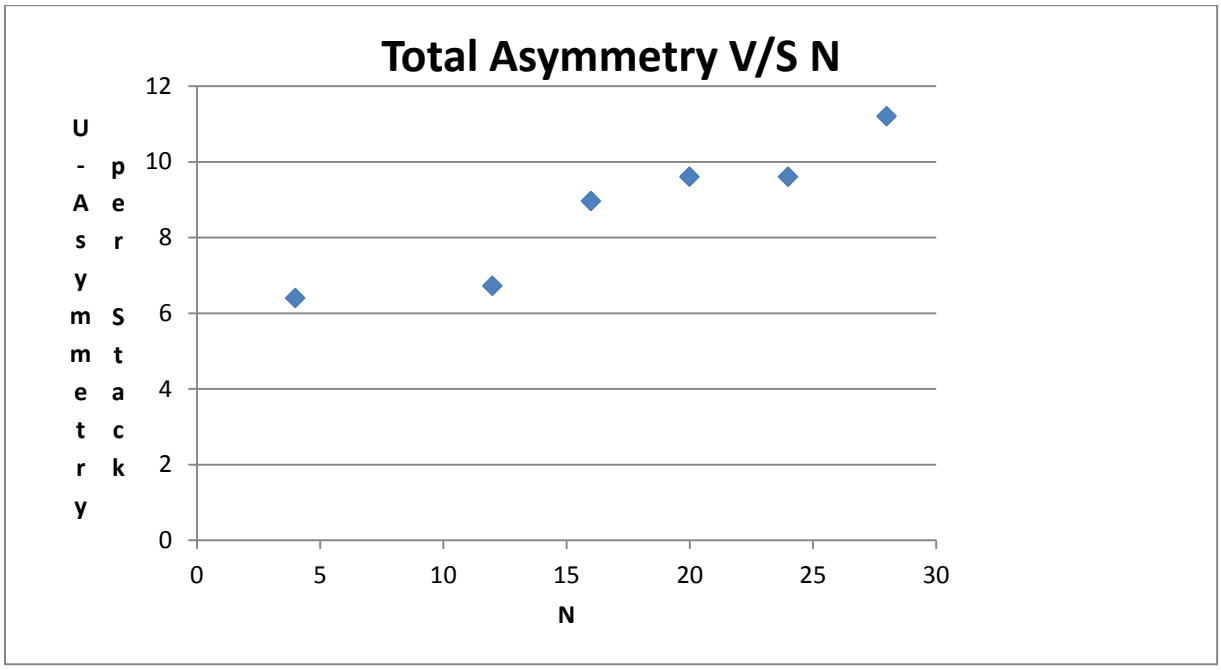


Figure 33 Total asymmetry per stack vs. stack number

The figure 33 shows total asymmetry of diode stack against stack number. It is increasing curve showing total asymmetry increases as stack number increases.

A graph is also drawn between total asymmetry per stack and square root of stack number which shows the significant statistic relationship between stack number and total asymmetry per diode stack.

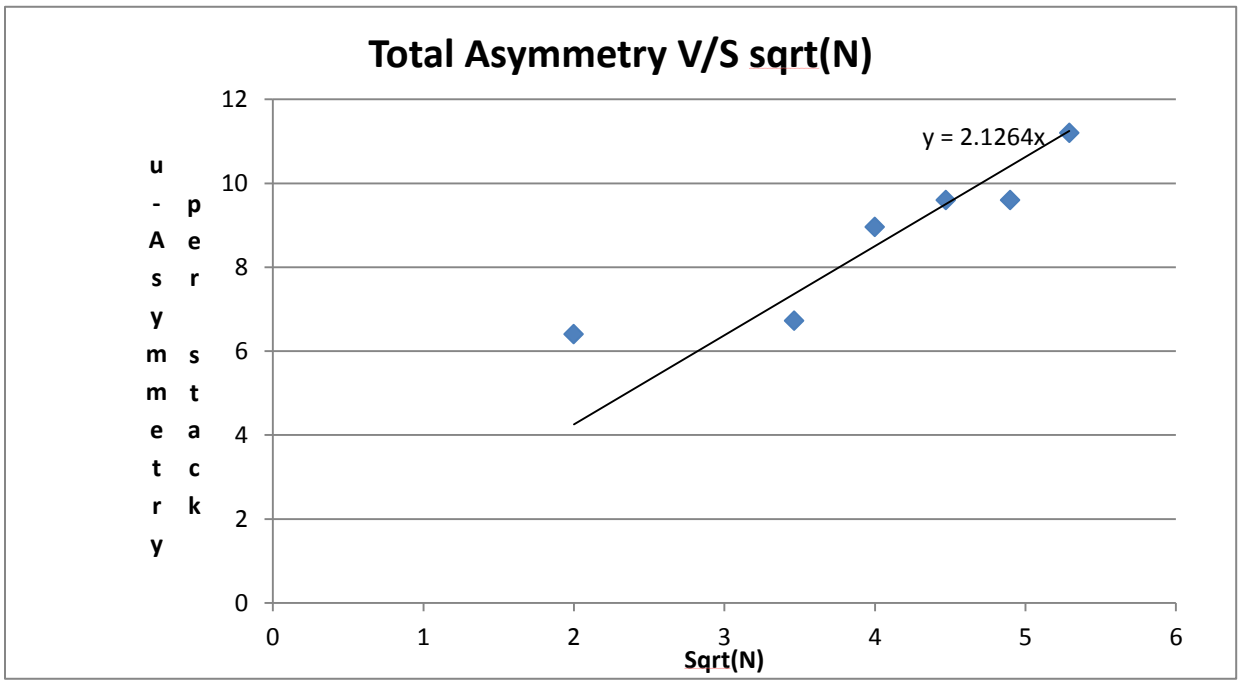


Figure 34 Total asymmetry per diode stack vs. square root of stack number

Above is graph for total asymmetry against square root of N. A linear trend line is drawn and all the data is lying close to the line which is very significant statistically, showing that standard deviation is proportional to the square root of the sample. In this case asymmetry is proportional to the square root of stack number N. This statistic variation is due to build in semiconductor fabrication process variation.

CHAPTER 5

Conclusion

5.1 Completed Research

The main purpose of this study was to fully characterize the diodes array as ESD protection for RF circuits. An extensive research is done for full characterization of the protection circuit. The research includes experimental tests and simulations. Celestron I was used to do HBM and TLP tests for ESD failure and RF small signal and large signal tests were done using Murray Microwave and Spectrum Analyzer equipment available in RF Micro devices. Simulations for HBM and TLP were done in Cadence environment and small signal and large signal simulations were done in Advanced Design System through dynamic link in Cadence. Some of the results obtained from tests and simulation were used in the main text of the thesis report to explain major outcomes and rest of results are given in the Appendix.

5.2 Problem Solved and Academic Achievements

A diode array as ESD protection circuit has been fully characterized in this research as proposed. There were few achievements have been made that are quite useful for the ESD design engineers when sizing the device. Through research we can conclude that almost all stacks can handle a current of 2A and a different withstand voltage depending upon the size of the stack which is also important for ESD protection circuit design engineer. Also from large signal analysis it can be seen that higher stacks has more total asymmetry causing more nonlinearity in the system. From small signal analysis we see it is important to model substrate correctly. The model that was used did not take care of the lateral coupling that exists between two adjacent devices. This lateral coupling effect was captured using “sxmodel” instance which was comprised of R and C value. The capacitance C depends on the geometry of the adjacent active

regions and spacing between them. After calculating C we calculated resistance R through relaxation frequency relation to model lateral coupling accurately. From the large signal analysis it is found that there is some kind of asymmetry exists in our protection device. This asymmetry could be due to several different reasons like change in width, change in length, or some variation in fabrication process. For this research the asymmetry was emulated through the change in width to capture the asymmetric effect in our large signal.

5.3 Future Work

This research contributed to the characterization of the protection circuit by itself and DUT was considered to be an open circuit. More future work is required to see how this protection circuit would have interference when put against a core circuit that is being protected. For this research asymmetry was captured through emulating width change but in future we can model asymmetry with buried oxide capacitor for more accuracy. Also this research did not consider any heating effect so work need to be done with consideration of heating effect to model protection circuit more realistically because disadvantage of the SOI technology is it has heating effect.

References

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Appendix A

Additional data for this work on measurement and simulation

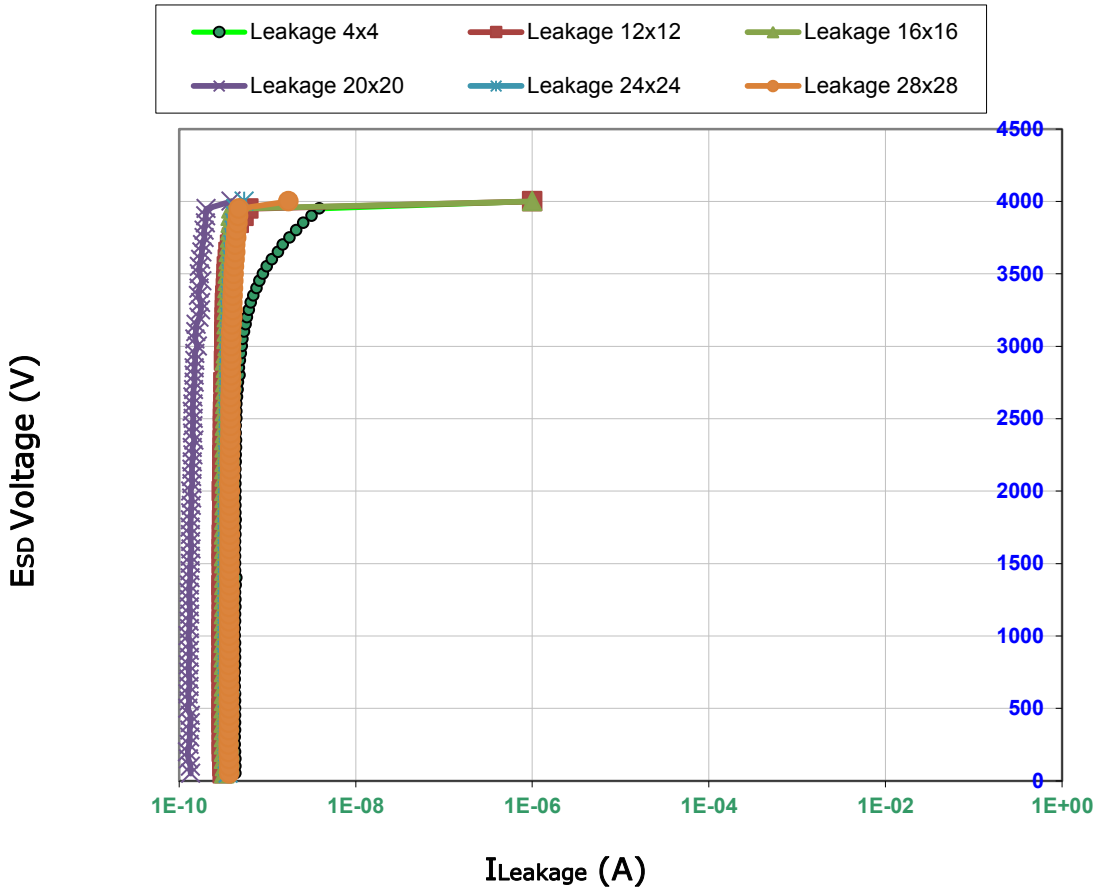

Figure A.1. HBM Leakage Curves for stacks 4x4, 12x12, 16x16, 20x20, 24x24, and 28x28.

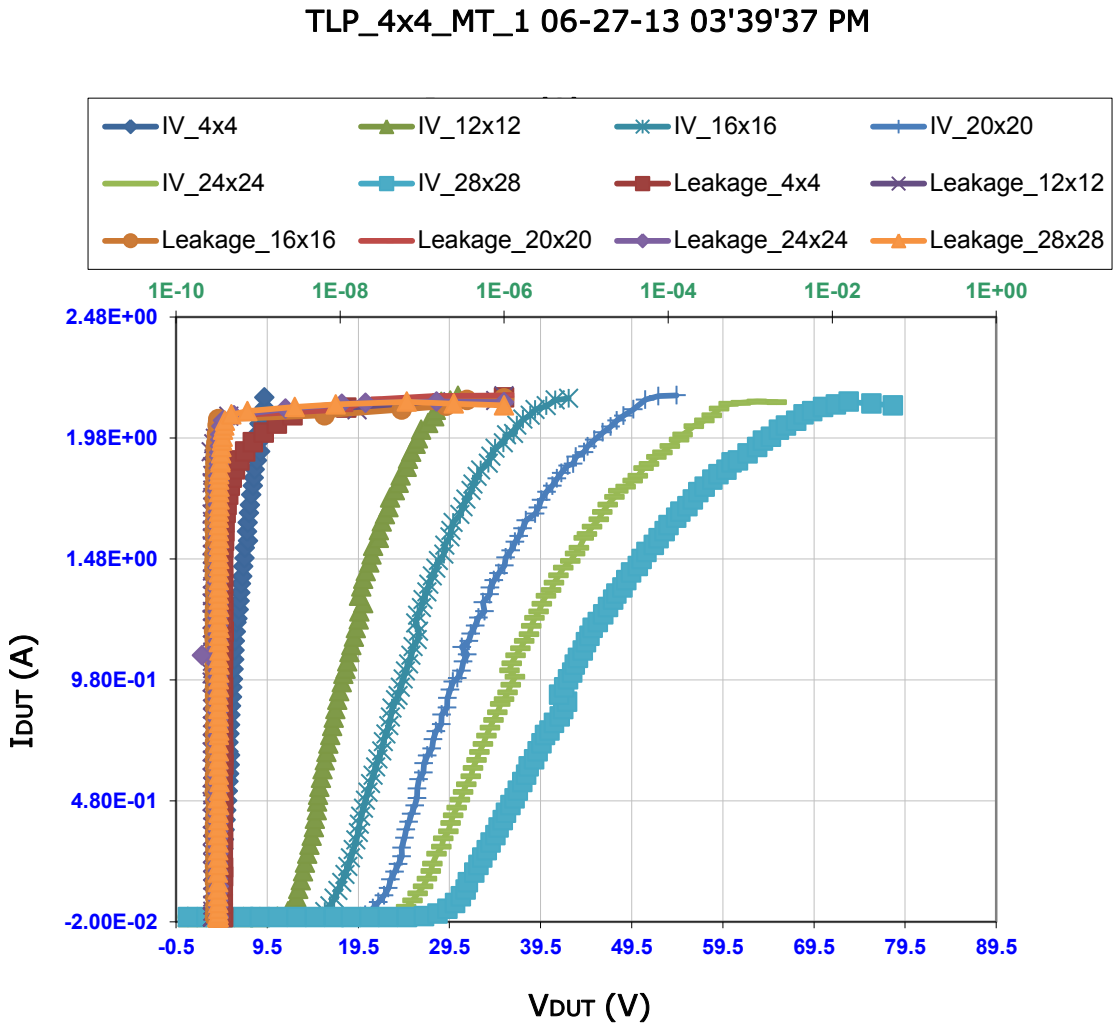

Figure A.2. TLP IV and Leakage Curves for stacks 4x4, 12x12, 16x16, 20x20, 24x24, and 28x28

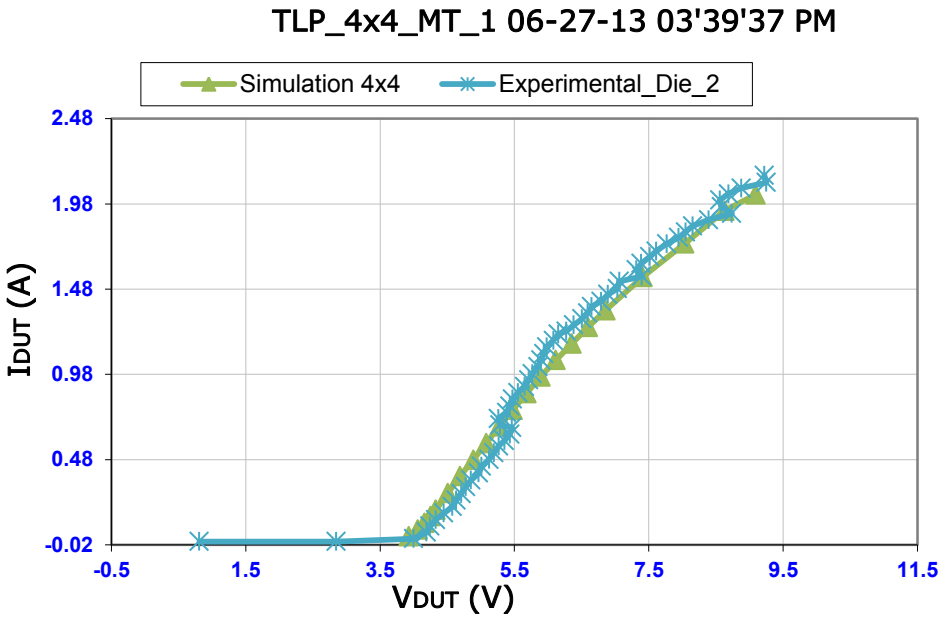

Figure A.3. TLP Comparison for 4x4 without adding any parasitic.

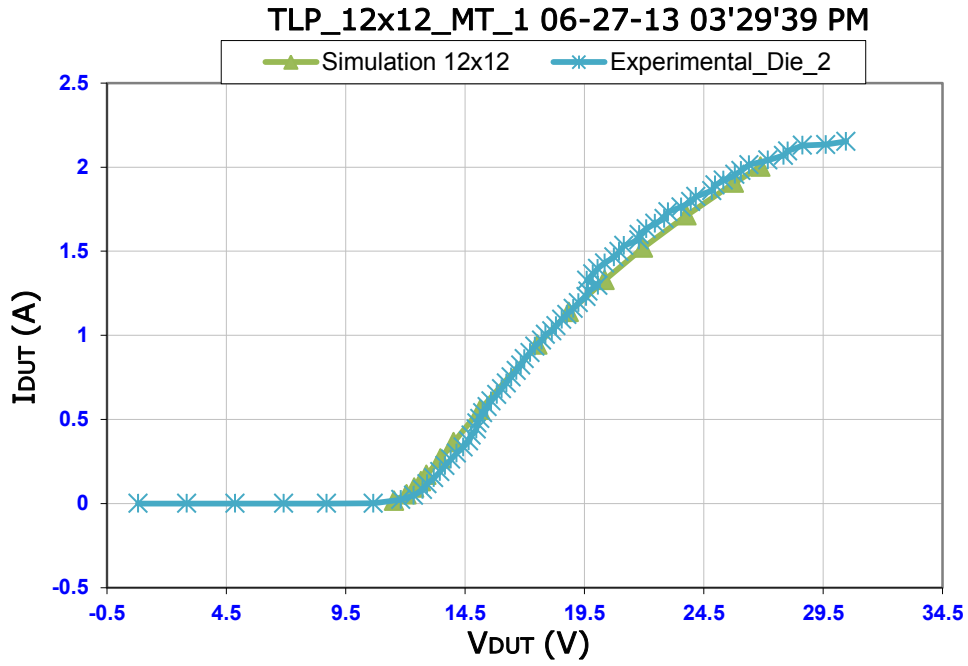

Figure A.4. TLP Comparison for structure 12x12 without adding any parasitic.

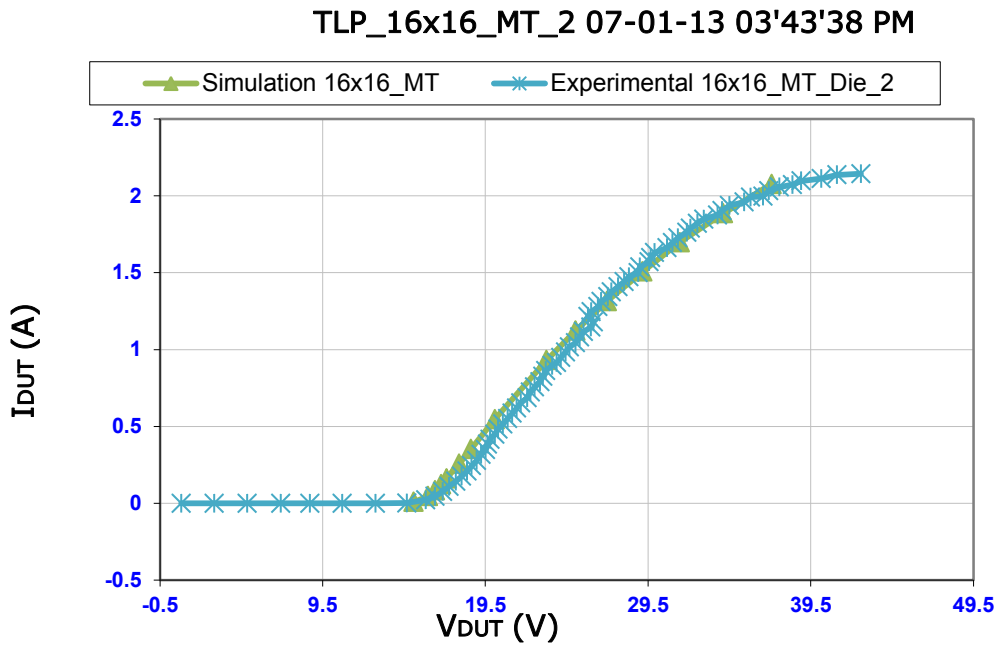

Figure A.5. TLP Comparison for stack 16x16 without adding any parasitic

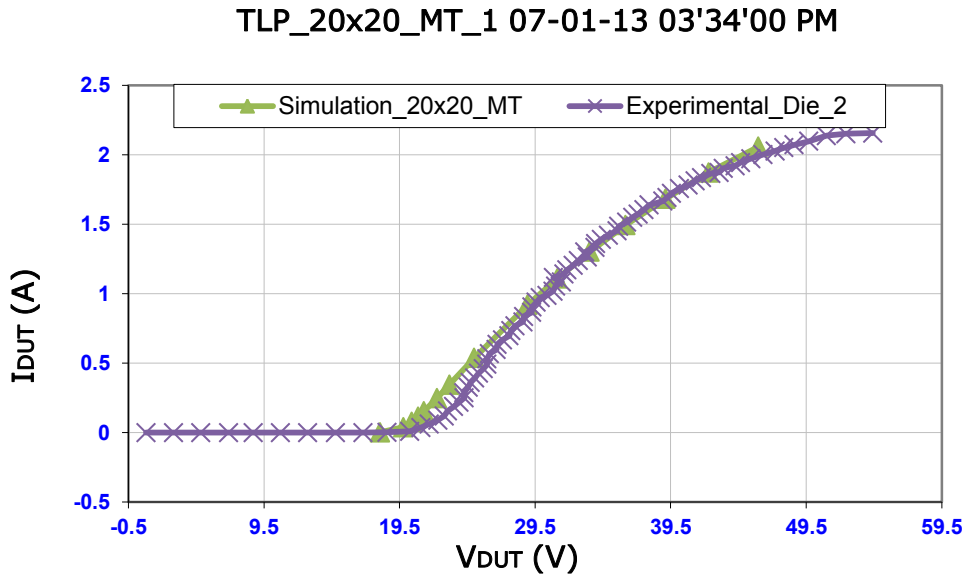

Figure A.6. TLP comparison for stack 20x20 without adding any parasitic

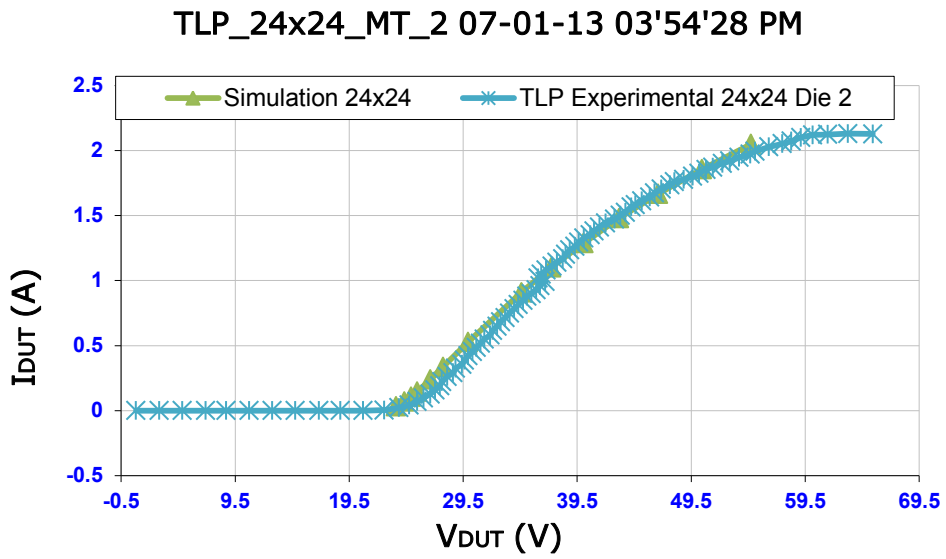

Figure A.7. TLP Comparison for stack 24x24 without adding any parasitic

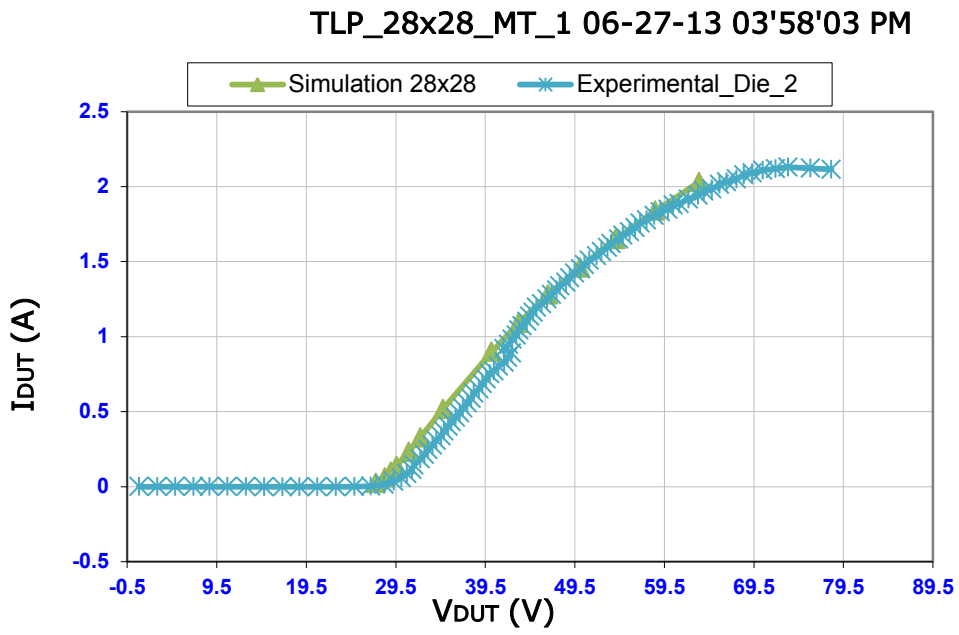

Figure A.8. TLP Comparison for stack 28x28 without adding any parasitic

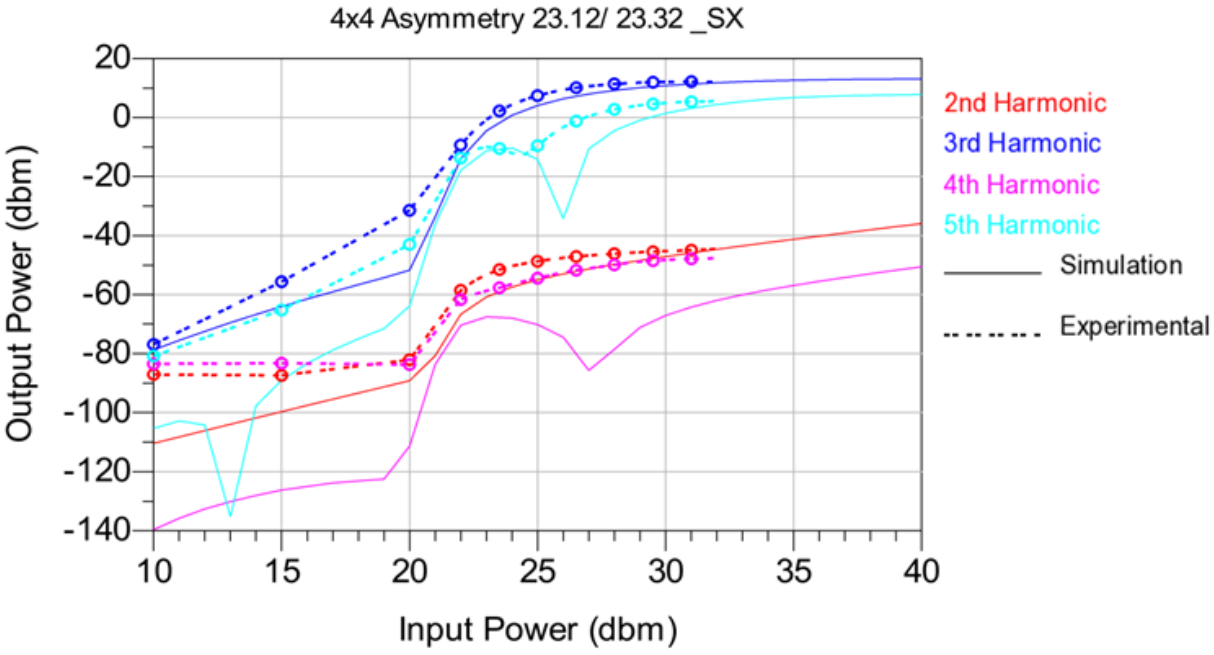

Figure A.9. Large Signal Comparison for 4x4 with considering asymmetry.

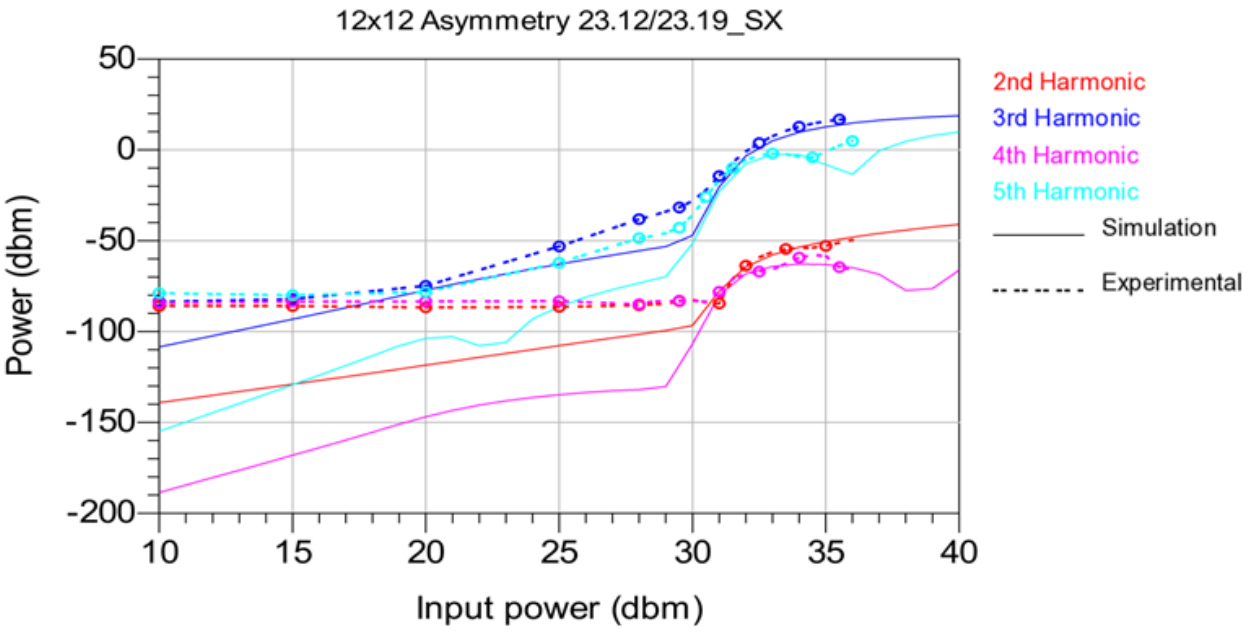

Figure A.10. Large Signal Comparison for 12x12 with considering asymmetry

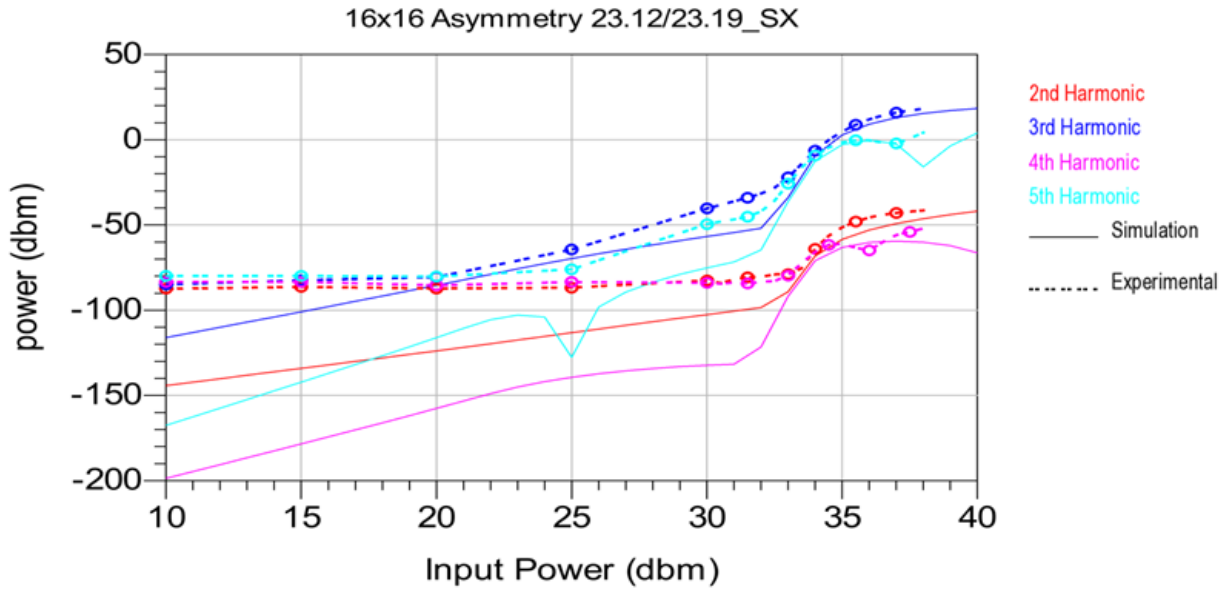

Figure A.11. Large Signal Comparison for 16x16 with considering asymmetry

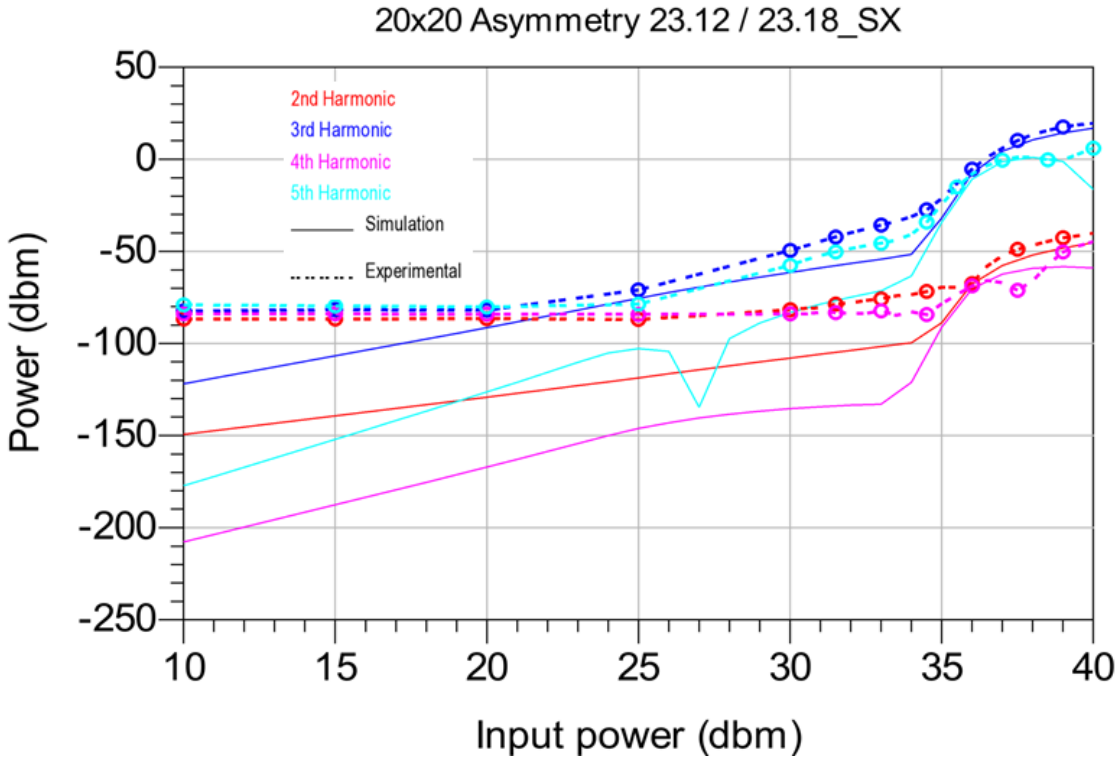

Figure A.12. Large Signal Comparison for 20x20 with considering asymmetry

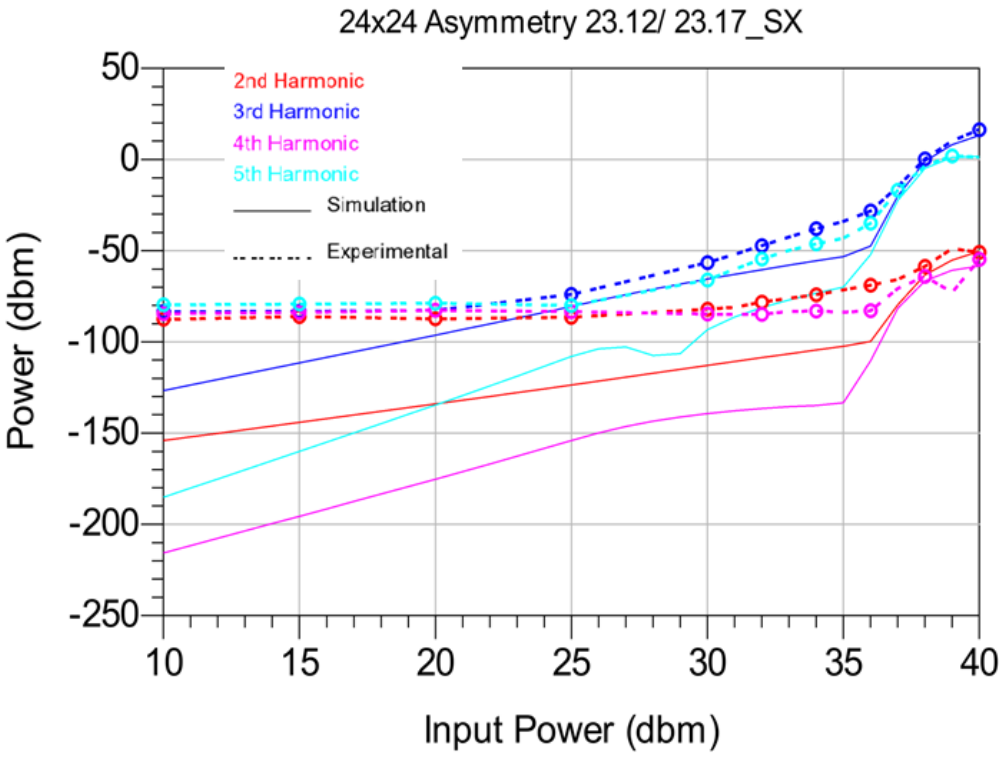

Figure A.13. Large Signal Comparison for 24x24 with considering asymmetry

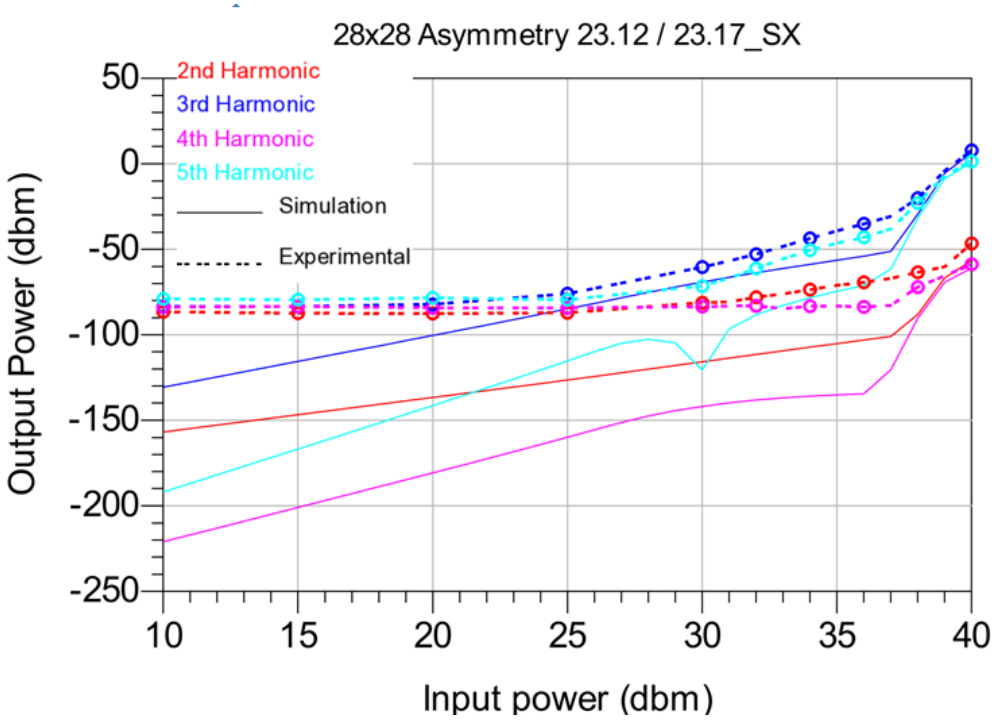

Figure A.14. Large Signal Comparison for 28x28 with considering asymmetry