A Novel Differential Ramp Generator Circuit with PVT Compensation Structure

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***Abstract*— Applications like counter ADC demanded accurate ramp signal with low power dissipation. This paper presents a novel approach of low power differential ramp generator with negative feedback for the compensation of the variations in process, voltage, and temperature (PVT). The derived equations of the proposed ramp generator circuit show that PVT compensation is enhanced significantly. Additionally, the circuit design and simulations were done in TSMC 0.18-µm CMOS technology. The Monte Carlo simulation results and corner analysis show that the linearity of the ramp signal is about 9-bit while power dissipation of the circuit is about 2.61µW.**

Index Terms—Counter ADC; Differential Ramp Generator; PVT Compensation; Single Slope.

I. INTRODUCTION

Recently, scientists have shown great interests in single slope analog to digital converters (SS-ADCs), or counter ADCs, because of the reducing channel length in new technologies [1-3]. In the past, SS-ADCs were not proper for high sampling rate applications, as counters sampling frequency was limited; but nowadays SS-ADCs are more useful because of the existing high sampling rate, low power, and digital counters [4,5]. The ramp generator block defines the resolution of SS-ADC; so stable linear ramp generators are significantly required for this purpose [6]. Also, linear ramp voltages are used in applications such as buck converter [7], proportional–integral–derivative (PID) controller system test [8], and ADC test [9]. On the other hand, the ramp generator circuit must be stable with variations in process, voltage, and temperature (PVT) for these applications; so a low power, linear ramp generator circuit, which is very useful for applications like SS-ADCs, is presented in this paper

Numerous attempts are made for the improvement of PVT compensation in ramp generators [9-11]. Snoeij et al., 2007 used a resistor ladder digital to analog converter, for making ramp voltages, which are utilized in a 10 bit ADC [12]. As the resistor ladder divides the supply voltage and generates the output ramp in this structure, it shows robustness against supply voltage variations; however, the proposed structure is not differential. Danesh et al., 2013 proposed a similar structure for counter ADC that used a differential ramp generator using the resistor ladder [13]. To decrease the number of resistors in the ramp generator structure, they used a low pass filter. Generating differential ramps using resistor ladder has been proposed previously by Danesh et al.. Additionally, Sordo et al., 2014 proposed a calibration method for PVT compensation of a single-ended ramp generator [11].

The differential ramp generator has smore merits than the single-ended ramp generator [13]. Further, current source ramp generator has less complexity and switches than the resistor ladder ramp generator [4, 13-15]; therefore, in this paper, we present a differential ramp generator structure using two current sources. The current sources are calibrated continually by a negative feedback loop, which makes the proposed structure very stable with variations in the process, voltage, and temperature. For instance, 50 percent mismatch between the capacitors does not change the linearity of the ramp voltages predominantly. For proving the robustness of the proposed structure, the mathematical representation of this model is expressed and a ramp generator with 9-bit linearity is designed and simulated in TSMC 0.18-µm CMOS technology. The operation of the proposed ramp generator circuit is illustrated in the following section.

II. PROPOSED RAMP GENERATOR

Figure 1 shows the proposed differential ramp generator schematic. The ramp circuit consists of two linear current sources, two charging capacitors (C0 and C1), and two feedback loops for compensation of the current sources. The feedback loops include eight transmission gates (TGs), four capacitors (C2, C3, C4 and C4), two analog multiplexers and one op-amp; TGs are used as switches in this structure. The proposed circuit works as follows. First, the I_{CSp} current charges the C0 capacitor linearly, to make positive ramp voltage (V_{rp}). Simultaneously, discharging the C1 capacitor with the I_{CSn} produces negative ramp voltage (V_{rn}). Furthermore, the two negative feedbacks in this structure adjust the desired slopes of output ramps. Ideally, the slope errors of differential ramp voltages (V_{rp} and V_{rp}), is zero if the maximum ramp voltage ($V_{ramp\ Max(Ideal)}$) and minimum ramp voltage ($V_{ramp\ Min(Ideal)}$) have constant values. For this purpose, bandgap voltage reference or external constant voltages must be used. If the maximum voltage of V_{rp} is more than the ideal voltage, then the V_{rp} of the next cycle increases using the negative feedback and vice versa; the negative feedback changes I_{CSp} current with varying V_p voltage. Negative ramp voltage slope is also modified by changing V_p voltage in the negative feedback loop.

As shown in lower part of Figure 1, two negative feedback loops were used. Both of the feedbacks work in odd and even cycles by "Select" controlling voltage, that results in the use of one op-amp for two feedback loops. In this figure M3, M4 and M8, M9 transistors are used as current sources, while M1, M2, and M6, M7 transistors are use as the two transmission gates. Further, M0 and M5 transistors are used for discharging of the C0 and C1, respectively.

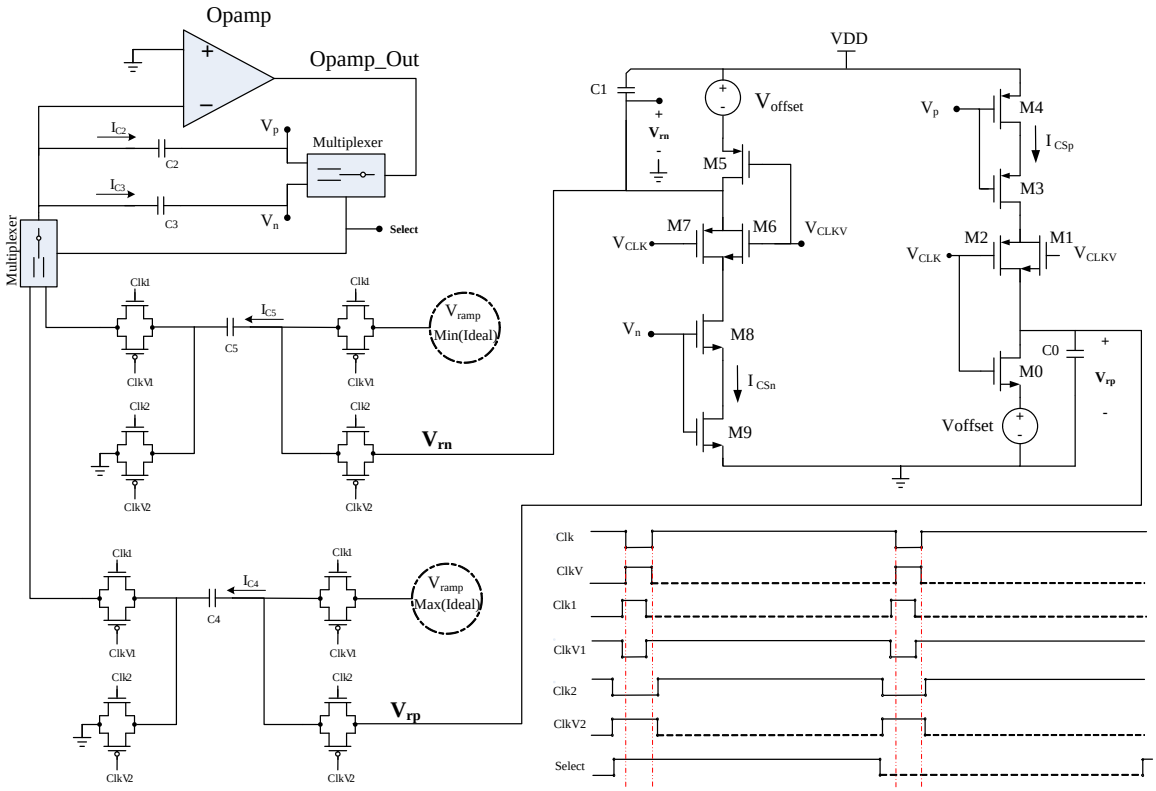


Figure 1: Proposed structure of the ramp generator with PVT compensation feedbacks

The differential ramp voltages for the SS-ADCs must have the same voltage ranges [13]. For that reason, offsets are vital for the proposed ramp generator because the current sources must be in the saturation region. Further, an offset (V_{offset}) that is equal to 0.45V is used for both of the ramp voltages.

Following the mathematical equations of the feedback loop, a ramp generator the charging current (I) is equal to:

$$I = C\frac{\Delta V}{\Delta T} \tag{1}$$

In this equation, C is the charging capacitor, ΔV and ΔT are the voltage and time differences, respectively. By considering the clocks from Figure 1 and neglecting the negative input current of the op-amp, we have the following equations for the charging currents of the capacitors:

$$I_{C2} = I_{C4} \tag{2}$$

$$I_{C3} = I_{C5} \tag{3}$$

According to (1), (2), (3) and Figure 1, by substituting I_{C2}, I_{C3}, I_{C4}, and I_{C5}, the following equations are achieved:

$$C_2\frac{0-V_p}{\Delta t} = C_4\frac{V_{RMIp}-V_{RMp}}{\Delta t} \tag{4}$$

$$C_3\frac{0-V_n}{\Delta t} = C_5\frac{V_{RMIn}-V_{RMn}}{\Delta t} \tag{5}$$

In these equations, V_{RMp}, V_{RMn}, V_{RMIp} and V_{RMIn} are the maximum positive ramp, the minimum negative ramp, ideal value of the maximum positive ramp and the ideal value of the minimum negative ramp, respectively. Integrations of (4) and (5) yields:

$$V_p = V_{p(0)} - \frac{C_4}{C_2}\left(V_{RMIp} - V_{RMp}\right) \tag{6}$$

$$V_n = V_{n(0)} - \frac{C_5}{C_3}\left(V_{RMIn} - V_{RMn}\right) \tag{7}$$

$V_{p(0)}$ and $V_{n(0)}$ in these equations are the initial values of V_p and V_n. These equations reveal the negative feedback effects on V_p and V_n. In fact, according to (6) and (7), V_p and V_n change, until V_{RM} and V_{RMI} become equal. To consider these periodic manners, the following equations are derived from (6) and (7):

$$V_{p(i)} = V_{p(i-1)} - \frac{C_4}{C_2}\sum_{i=1}^{\infty}\left(V_{RMIp} - V_{RMp(i)}\right) \tag{8}$$

$$V_{n(i)} = V_{n(i-1)} - \frac{C_5}{C_3}\sum_{i=1}^{\infty}\left(V_{RMIn} - V_{RMn(i)}\right) \tag{9}$$

These equations reveal the gradual variations of V_p and V_n for satisfying the circuit conditions to reach the ideal ramps slopes. More information about (8) and (9) are available in Figure 3. By considering V_n, the start time of Figure 3 (b), equals to 0.9V, while V_{RMIn}, $V_{RMn(1)}$, C3 and C5 equal to 0.45V, 0V, 0.951pF and 57fF, respectively. According to (9), for i equals to 1, $V_{n(1)}$ will be achieved at 873mV. This calculation is well matched with the simulation results from Figure 3, and it can be continued to reach the V_n steady. Similarly, the V_p steady can be calculated using (8). Also according to (8) and (9), the settling times of V_p steady and V_n steady decrease by increasing the C4/C2 and C5/C3, respectively, leading to the increasing slope errors of the final ramps

III. SIMULATION RESULTS

The proposed ramp generator is designed in TSMC 0.18-µm CMOS. The size of the transistors and capacitors of the proposed differential ramp generator is given in Table 1. The ramp generator is designed for 1.8V differential range; this means that each positive and negative ramp has an output range of 0.9V. Figure 2 depicts the integral non-linearity (INL) of the positive ramp (INLp), negative ramp (INLn) and differential ramp (INLt). The differences of the positive ramp and negative ramp yield the differential ramp. As illustrated in this figure, INLt is less than 3.5mV. Moreover, Figure 3(a) and 3(b), respectively show thevariations of controlling voltages V_p and V_n to reach the stable values. Also, Figure 3(c) and 3(d) show the positive and negative ramp voltages, respectively, in whin both ramps have the same ranges between 0.45V and 1.35V.

Table 1
Size Of Transistors And Capacitors Of The Proposed Ramp Generator

Transistor	W/L µm	Capacitor	fF
M0, M5	0.4/0.18	C0, C1	570
M1-M4	1.0/1.0	C2, C3	951
M6-M9	1.0/1.0	C4, C5	57

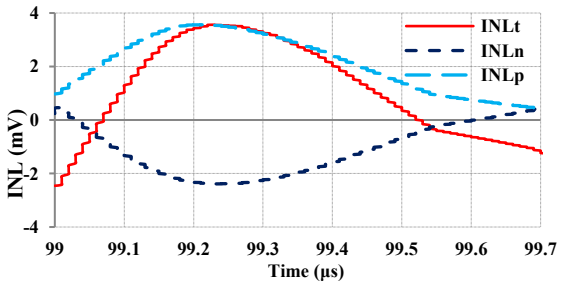
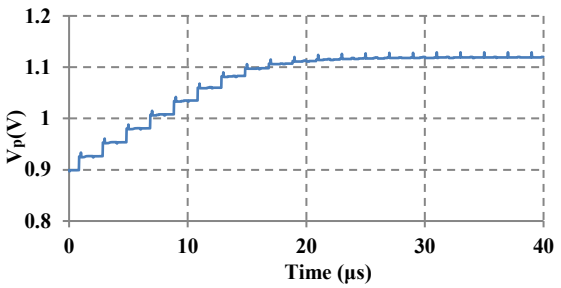
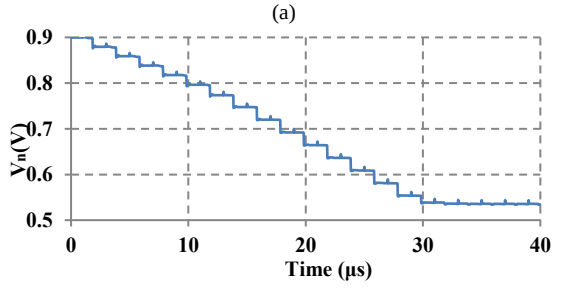


Figure 2: INL simulation results of the proposed differential ramp generator



(a)



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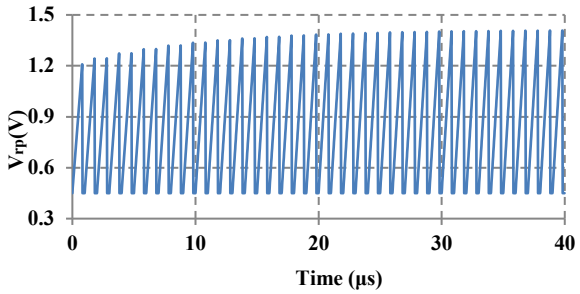

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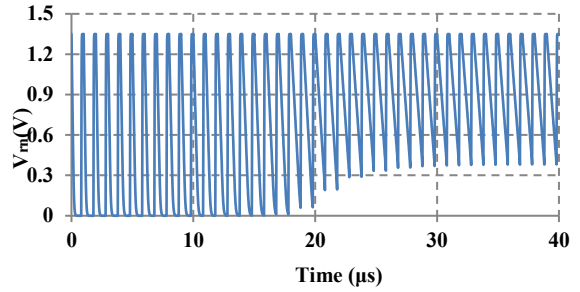

(d)

Figure 3: Simulation results of the proposed ramp: (a) V_p, (b) V_n, (c) V_{rp}, and (d) V_{rn}.

Table 2 shows the corner analysis of the proposed ramp generator. Linearity, V_p steady and V_n steady are investigated in these simulations. Corner TT shows the best result for linearity parameter, while corner FF shows the worst case.

Table 2
Corner Analysis of the Proposed Ramp Generator

Corner	TT	FF	SS	FS	SF
Ramp INL +/-	3.5mV	4.5mV	4.05mV	4mV	4.1mV
V_p Steady (V)	1.118	1.164	1.074	1.085	1.154
V_n Steady (V)	0.536	0.493	0.579	0.502	0.569

In the conventional ramp generator circuit, the INL variations in different corners are mostly due to the deviations of the charging current (I_{CS}). For a better understanding of the variations of this current, ΔI_{CS} is written as:

$$\Delta I_{CS} = \left(\frac{I_{CSI} - I_{CS}}{I_{CSI}} \right) \times 100 \qquad (10)$$

In this equation, I_{CS} is the value of the charging current and I_{CSI} is the ideal value of charging current that can be calculated from (1)Δ. In this case, I_{CS} is represented as a percentage of I_{CS} variations. A comparison of ΔI_{CS} between the conventional and proposed ramp generator circuit was made, and the results are shown in Table 3. It is worth mentioning that, while the proposed ramp circuit generates two ramp voltages, its power consumption is less than the conventional ramp circuit due to the removal of the circuit in the the proposed structure[4]. Charging capacitor and transistors of the conventional ramp circuit were chosen

similar to the charging capacitor and the transistors of the proposed circuit. Additionally, the conventional ramp generator was simulated with the same technology of the proposed circuit. The full scale of the conventional ramp generator is 1.16V, while the maximum INL of the output ramp is 4mV and the power consumption of the circuit is about 3.6µW. Table 3 shows a better comparison of the proposed and conventional ramp generators in different corners.

Table 4 shows the capacitor mismatch analysis of the proposed ramp generator. As indicated in this table, the proposed ramp generator tolerates the mismatches between capacitors. This mismatch is due to the existing negative feedback that changes the ramp slope to reach the ideal ramp voltages. The simulation results also show that while 50 percent mismatch between the capacitors in the proposed ramp generator leads to maximum INL deviations of 1mV; this mismatch for the conventional ramp generator leads to more than 550mV INL deviations.

Table 3
Conventional Ramp Generator And The Proposed Ramp Generator Comparison

Corner	FF	SS	FS	SF
Conventional ΔI_{CS}	+4.4%	-5.6%	-4.8%	+4.2%
Proposed ΔI_{CS}	+0.4%	-0.3%	-0.35%	+0.3%
Conventional INL +/-	4.5mV	4.05mV	4mV	4.1mV
Proposed INL +/-	42mV	64mV	51mV	47mV

Table 4
Performance of the Proposed Ramp Generator with Capacitor Mismatches

CMOS Technology	0.18-µm		
Supply (V)	1.8		
Ramp frequency (KHz)	1000		
Ramp full range differential (V)	1.8		
C0 (fF)	570	285	570
C1 (fF)	570	570	798
C2 (fF)	951	1902	570
C3 (fF)	951	951	951
C4 (fF)	57	57	57
C5 (fF)	57	57	112
Ramp INL +/-	3.5mV	3.95mV	4. 5mV
Power (Watt)	2.61µ	1.95µ	2.90µ

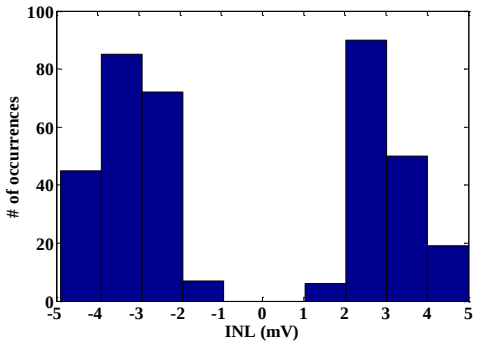

Figure 4: Monte Carlo simulation results of the proposed ramp generator

Figure 4 depicts the Monte Carlo analysis results of the proposed ramp generator with PVT compensation structure. The channel length modulation, device mismatches, variations of the threshold voltage and temperature are considered in the Monte Carlo analysis. As shown in Figure 4 the INL variations are between -5mV and +5mV.

IV. CONCLUSION

In this paper, a new technique for increasing the robustness of the ramp generator is proposed. The proposed method generally can be used for PVT compensation of the similar cases; analytic formulas of this technique were derived to determine the constraints that should be used for optimizing the output ramp. Further, by combining and sharing the two current source ramp generators, a fully differential ramp generator circuit, which can be used for counter ADCs, is invented. The results of a simulation that considers capacitor mismatches verified good performances in all corners. The power dissipation of the proposed circuit is about 2.61µW for 1MS/s differential output ramp, while it has 9-bit resolution. The analysis and simulation results of the proposed method show that this technique is completely general, and therefore it can be used in processes below 0.18-µm.

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