Technical Disclosure Commons

Defensive Publications Series

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FLEXIBLE PCI EXPESS BANDWIDTH EXTENSION ON EMBEDDED DISCRETE GPU

HP INC

Flexible PCI Express Bandwidth extension on embedded Discrete GPU

Abstract:

- On Intel platform that is supporting Switchable/Hybrid Graphics feature, a discrete GPU can be connected to either PCIe Graphics interface (PEG) inside CPU or PCIe controller inside PCH. The maximum link width is up to 16 lanes (x16) on PEG. But the maximum link width is up to 4 lanes (x4) per one PCIe controller on PCH.

- For both AMD and Nvidia graphics cards, the PCIe link width can support x8 or x16 lanes. However, if a discrete graphics card is designed behind PCH PCIe controller, the PCIe link width is limited to x4 lanes on system.

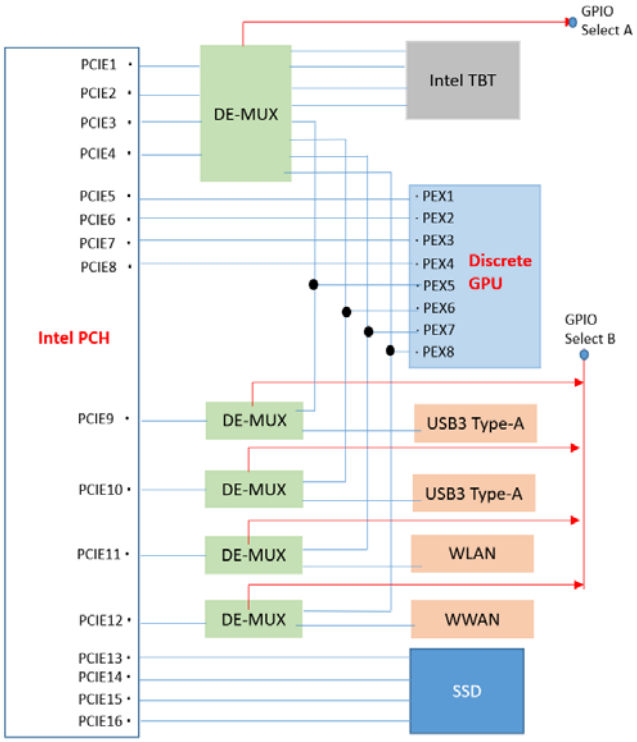
- SBIOS provides setup options to enable/disable certain PCIe devices, such as Intel Thunderbolt devices, WLAN, WWAN and USB3 ports. Once these PCIe devices are disabled, these free PCIe lanes can be used by discrete GPU ideally.

- With De-Mux PCIe switching solution, SBIOS can use GPIO to control output PCIe lanes to either Discrete GPU or other PCIe devices. So PCIe lanes can be fully utilized on discrete GPU when certain PCIe devices are disabled.

Design Construction:

- HW: De-Mux IC are required to route the output PCIe lanes to either Discrete GPU or other PCIe devices.
- SW: No SW need
- BIOS: If BIOS setup options are configured to disable certain PCIe devices, BIOS start to control GPIO state to select the output PCIe lanes source between discrete GPU and other PCIe devices.

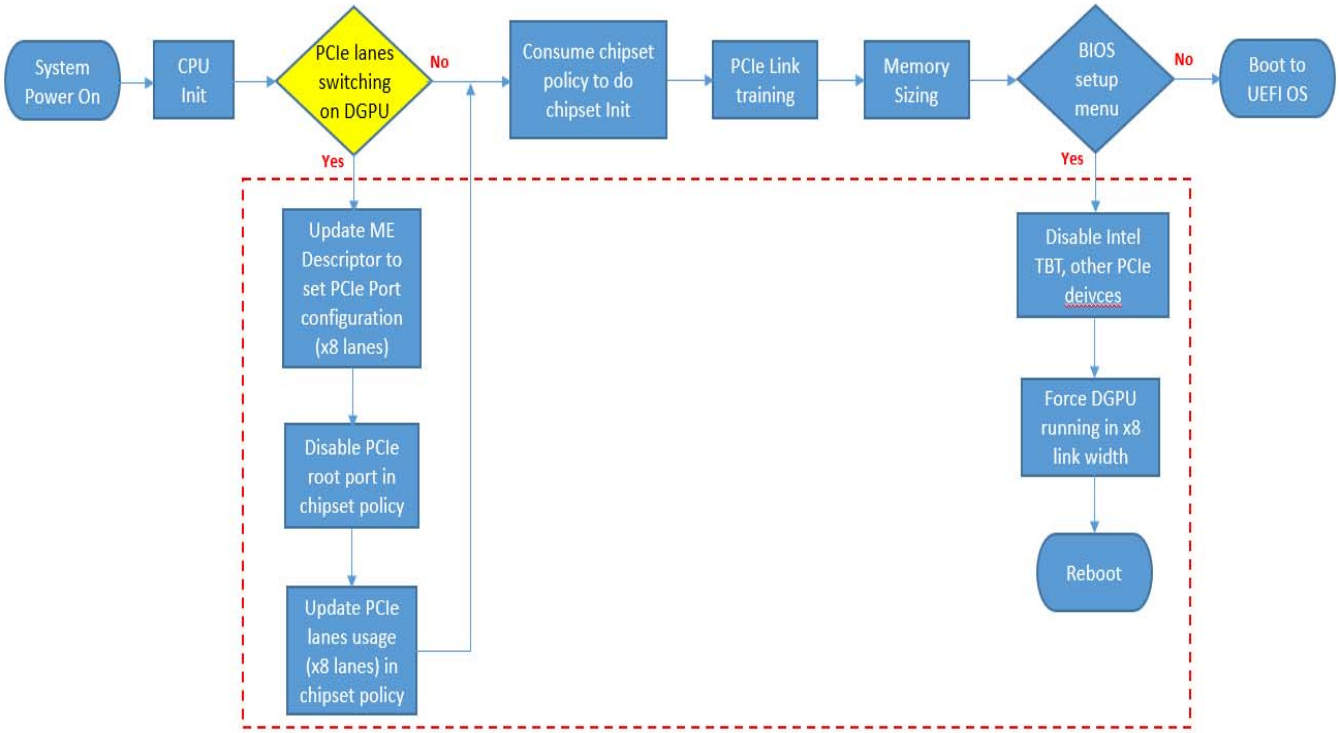
< Solution>



- The Discrete GPU is x4 link width. The PCIe lane# 5, 6, 7 , 8 from PCIe host bridge is connected to PEX1, PEX2, PEX3, PEX4 on Discrete GPU.
- The concept is to utilize the unused PEX5, PEX6, PEX7, PEX8 on Discrete GPU to achieve x8 link width.
- From HW design perspective, the key point is to put PCIe devices closed to discrete GPU. But under the premise that we should have BIOS setup options to enable/disable these PCIE devices.
- From chipset design, the maximum PCIe lanes on 1 PCIe controller is x4. Thus, chipset vendor have to support x8 link width across 2 PCIe controllers.
- The GPIO select A controls the De-Mux to routed PCIE lane # 1, 2, 3,4 to either Intel TBT or Discrete GPU.
- The GPIO select B controls the De-Mux to routed PCIE lane # 9, 10, 11, 12 to either onboard PCIe devices or Discrete GPU.
- In BIOS setup menu, BIOS provide 2 options to control GPIO select A and GPIO select B individually to allow discrete GPU running x8 link width.
- If GPIO select A is set to route PCIE lane # 1~4 to discrete GPU, Intel TBT will be disabled automatically. But if user disable Intel TBT in BIOS setup menu manually, BIOS will control GPIO select A to let discrete GPU running x8 link width.
- If GPIO select B is set to route PCIE lane # 9~12 to discrete GPU, onboard PCIE devices will be disabled automatically. But if user disable USB ports, WLAN and WWAN in BIOS setup manually, BIOS also control GPIO select B to let discrete GPU running x8 link width.

Discrete GPU Link width	GPIO Select A	GPIO Select B	PCI Express Lane #
x4	0	0	5, 6, 7, 8
x8 (Option 1)	1	0	1, 2, 3, 4, 5, 6, 7, 8
x8 (Option 2)	0	1	5, 6, 7, 8, 9, 10, 11, 12

<Flow Chart>


System Power On
CPU Init
PCIe lanes switching on DGPU
No
Yes
Consume chipset policy to do chipset Init
PCIe Link training
Memory Sizing
BIOS setup menu
No
Yes
Boot to UEFI OS
Update ME Descriptor to set PCIe Port configuration (x8 lanes)
Disable PCIe root port in chipset policy
Update PCIe lanes usage (x8 lanes) in chipset policy
Disable Intel TBT, other PCIe deivces
Force DGPU running in x8 link width
Reboot

- **Business Strategy/Advantages**

    1. The PCIe link width of discrete GPU that is behind Intel PCH will not limit to x4 lanes only.
    2. If certain PCIe devices are disabled via BIOS setup options, BIOS can control De-Mux IC to rout these free PCIe lanes to Discrete GPU. So discrete GPU link width can up to x8 lanes.
    3. With De-Mux PCIe switching solution, system can route unused /free PCIe lanes to other in use PCIe devices to increase the link bandwidth.
    4. Limit Discrete GPU to x2 link width as default. System can route unused/free 2 PCIe lanes to support additional PCIe devices that uses x1 lane link width. But discrete GPU can still support x4 link width via De-Mux PCIe switching.

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