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HIGH FREQUENCY COMMON-MODE NOISE IN SERDES CIRCUITS' OPTIMIZED INTERCONNECTIONS

Roxana Vladuță[1,2], Lidia Dobrescu[2], Nicolae Militaru[2], Dragoș Dobrescu[2]

[1]ESilicon Romania, Bucharest – District 1, Romania
[2]Faculty of Electronics, Telecommunications and Information Technology, University POLITEHNICA of Bucharest, Romania

Abstract. *According to the requirements imposed by the new four-level pulse amplitude modulation (PAM4) standard for high-speed data transfer and processing, electrical constraints and manufacturing tolerances in integrated electronic packages impose accurate electromagnetic simulations and new S-parameters analysis, saving time and financial resources for next-generation switches, routers or data centers circuits implementation. The complexity of the advanced networking class circuits' encapsulation substrates massively increases due to the large number of differential signals that it integrates. Differential signaling has replaced single-ended transmission in high-speed circuits due to their many advantages, including increased immunity to crosstalk and electromagnetic interference, but common-mode noise due to timing skew or amplitude unbalance differences can still affect them. This work tests five different models, identifies and optimizes the 45° bends, structures that commonly affect the reflections in a differential stripline. Then it studies differential transmission lines in stripline topology, implemented in a 12-layered flip-chip package, using S-parameters, inspecting and comparing the common-mode noise. In this way, the paper combines microwave theory with a real chip packaging design in an innovative way, using finite element analysis of electromagnetic field simulation and mixed-mod scattering parameters of differential topologies, towards an optimized structure design.*

Key words: *common-mode noise, differential signaling, electromagnetic interference, finite element analysis model, flip-chip package, multilayer circuit board*

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Corresponding author: Lidia Dobrescu
Faculty of Electronics, Telecommunications and Information Technology, University POLITEHNICA of Bucharest, Romania.
(E-mail: lidia.dobrescu@electronica.pub.ro).

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1. INTRODUCTION

The increasing number of devices connected to Internet and modern Cloud storage impose a growing need to move more data much faster [1]. Serializer/Deserializer solution, also known as SerDes, is used to convert parallel data into serial data, without increasing the number of pins. IEEE standards define fast data rates that impose four-level pulse amplitude modulation (PAM4) signaling [2]. The price that is paid consists in PAM4 sensitivity to noise and increasingly susceptibility to electromagnetic crosstalk problems in high-speed designs. Advanced packaging styles and a constant reduced area increase the complexity of the designing and verifying processes. Next-generation switches and routers impose power scaling, larger I/O bandwidth and a flexible and optimized architecture.

1.1. Differential Signaling

Differential signaling is a modern implementation method that enhances high-speed data carrying using two signals, each in its own conductor. A stripline is a transversal electromagnetic (TEM) transmission line which uses a flat strip of metal between two parallel ground planes insulated in a dielectric bulk. The advantages of the planar microwave fabrication process impose parallel-stripline for many other applications such as microwave sensors [3].

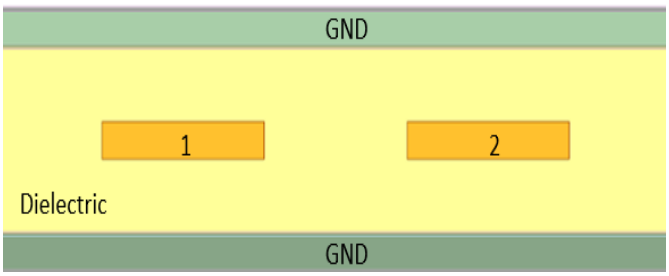


Fig. 1 Stripline transmission in differential topology

The common method to increase noise immunity in a stripline is to replace the single-ended topology with a differential one as shown in Fig. 1, where there are two electromagnetically coupled conductors between the ground planes. High bandwidth differential signals can be transmitted if a uniform cross section down its length ensures constant impedance. The greater the coupling, the more robust to ground bounce noise picked up from environment [4]. The ground plane allows a common mode of propagation to exist together with the desired differential mode signaling, requiring a mixed theoretical approach.

1.2. Chipset Encapsulation

Integrated circuits (IC) encapsulation structure, called package, has both electrical and structural roles. In fact, it is a passive component that adapts the IC conductive elements dimensions to printed circuit boards (PCB) specific ones. It also enables the redistribution of the signals to facilitate the connection of several components on the PCB. The complexity of the IC encapsulation substrate is due to the large number of differential signals that it integrates, thus realizing the interconnection between the integrated circuit and the printed circuit board. The interconnection paths can be seen and analyzed as differential paths. They cannot be realized in the form of straight lines since they will have elements of bypass or they must connect non-aligned structures, so many bends are required.

1.3. Propagation Issues

Common-mode reflections generated in differential transmission lines as strip line or microstrip type are due to the route bends and asymmetries, therefore causing signal degradation. The signal integrity issues of bend discontinuities in a high-speed interconnect design can be investigated using circuit simulators.

Shiue, Guo and Lin [5] deal with 45° angle instead right-angle bends for common-mode noise reduction. The length of the routes of the differential pair is conventionally measured as a midline of the route. Thus, for any bend of the differential pair, the outward path will have a longer length, whereby the propagated signal will have a greater delay [6]. Skew is the deviation of propagation delay due to length differences and electrical loading. Practical ways of compensating skew have been developed and a parallel-plate patch metal can act as a compensation capacitance [5]. Other technological aspects as discontinuities, layer-to-layer variation of the dielectric constant or skew due to glass weave can be also considered [7].

1.4. Paper Structure

Section 1 provides a quick view on interconnections paths from the substrate of an IC package, analyzed as stripline differential topology. It announces specific propagation problems such as common-mode reflections, noise and delays that can be simulated using specific software and can usually be compensated by length matching. This section outlines the structure of the paper in the end. It offers a short overview on this paper subject and topics.

Section 2 presents transmission lines modeling principles and characterization. Mixed-mode *S*-parameters, as a theoretical base of modeling, are shortly described using electromagnetic-field simulations.

Section 3 presents Ansys HFSS simulation methodology and its modeling principles.

Section 4 shows layout routing rules for package and signal integrity requirements.

Section 5 presents simplified structures evaluations.

Section 6 demonstrates optimized structures for common-mode noise reduction.

Section 7 summarizes the salient points of this work and the state-of-the-art advancements are highlighted.

2. Transmission Line Modeling and Characterization

Different approaches can be used for modeling the electromagnetic phenomena within the differential transmission line.

2.1. Traditional Distributed-Element Circuits Models

In order to model the differential transmission line (see Fig. 2), the lumped-element models with conventional passive electrical elements, exemplified in texts by Gray and Meyer [8], are replaced with other models containing distributed circuit elements per unit length. In this case, a complex distributed circuit analysis is required [8]. The distributed resistance, inductance, capacitance, and conductance, primary line constants, can model the transmission line as an infinite series of two-port cells, using so-called telegrapher's equations.

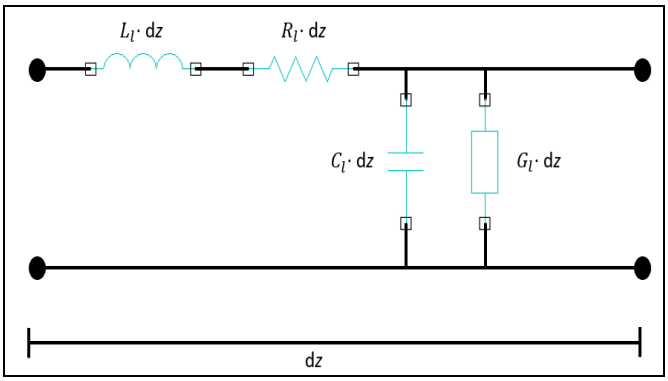


Fig. 2 Equivalent circuit with distributed elements per unit length

Although these models were initially developed for microwaves, where concentrated constants are difficult to be implemented, Bockelman affirms [9] that this method remains still difficult to be applied for measurements or tests in RF and microwave frequency range.

2.2. Models Using *S*-parameters

Scattering parameters (*S*-parameters) are more suitable for characterizing high-speed circuits at RF and microwave frequencies. Mixed-mode *S*-parameters [9] theory allows a real-mode measurement system and offers a solid based for electromagnetic field simulation.

A coupled line pair, Line A and Line B, over a common ground plane is analyzed. The four ports are not physically ports, but they can be seen as conceptual tools (see Fig. 3).

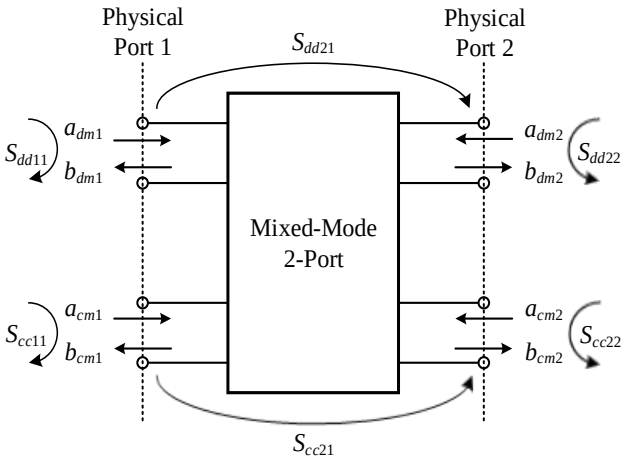


Fig. 3 Mixed-mode two-port device

When the *S*-parameter indices are the same (S_{11} or S_{22}), this indicates a reflection, because the input and output ports are the same.

The mixed *S*-parameters matrix becomes:

$$\begin{bmatrix} b_{dm1} \\ b_{dm2} \\ b_{cm1} \\ b_{cm2} \end{bmatrix} = \begin{bmatrix} S_{dd_{11}} S_{dd_{12}} & S_{dc_{11}} S_{dc_{12}} \\ S_{dd_{21}} S_{dd_{22}} & S_{dc_{21}} S_{dc_{22}} \\ S_{cd_{11}} S_{cd_{12}} & S_{cc_{11}} S_{cc_{12}} \\ S_{cd_{21}} S_{cd_{22}} & S_{cc_{21}} S_{cc_{22}} \end{bmatrix} \cdot \begin{bmatrix} a_{dm1} \\ a_{dm2} \\ a_{cm1} \\ a_{cm2} \end{bmatrix} = \begin{bmatrix} [S_{dd}] & [S_{dc}] \\ [S_{cd}] & [S_{cc}] \end{bmatrix} \cdot \begin{bmatrix} a_{dm1} \\ a_{dm2} \\ a_{cm1} \\ a_{cm2} \end{bmatrix} \quad (1)$$

where:

a = direct wave (incident on the port);

b = reverse wave (reflected from the port);

*dm*1 and *dm*2 = differential mode at port 1 and port 2;

*cm*1and *cm*2 =common-mode at port 1 and port 2;

S_{dd} = differential mode *S*-parameters;

S_{cc} = common-mode *S*-parameters;

S_{dc} = *S*-parameters describing the conversion of common-mode waves into differential-mode waves;

S_{cd} = *S*-parameters describing the conversion of differential-mode waves into common-mode waves.

The differential mode voltage is the difference between two voltages, establishing a signal that is no longer referenced to the ground. The common-mode voltage in a differential topology is the average voltage at a port, so common-mode voltage is the half of the sum of the two voltages. The common-mode current is the sum of the currents and the return current for the common-mode signal flows through the ground plane. Mixed-mode *S*-parameters can be measured with a special designed practical system [9].

Usually a channel must match only the characteristic impedance (50Ω), but for high-speed transmissions the waveform at the connector output is degraded and only *S*-parameters complex matrix show Reflection/Transmission characteristics (Amplitude/Phase) in the frequency domain. Mixed-mode *S*-parameters also cover mode conversions [10].

This theory using mixed-mode *S*-parameters can fully characterize a differential circuit, including coupled line systems and it will be used in the electromagnetic field simulation for optimizing the interconnection paths in the IC substrate. It will allow the evaluation of a transmission line both in differential transmission and in common transmission mode, as a main output of a simulated process, in the next section of the paper.

2.3. Odd and Even Propagation Mode

In a stripline, the useful differential signal is applied at the end of a pair of coupled lines as a potential difference between the two signal conductors and propagates oddly. The presence of the ground conductor, serving as the current return path, makes propagation of the transmission common mode possible. The even-mode signal, also called the common-mode signal, can be expressed as the average of the two amplitudes applied at the end of the coupled lines [4].

2.4. Common-Mode Return Loss

High-speed SerDes, in wire bond package applications, have clearly specified S_{cc11} parameter, common-mode return loss, and other requirements. Common-mode return loss is related to common-mode noise.

Na, Arseneault *et al*. [11] shows that for a differential pair, common-mode return loss is a measure of common-mode signal reflection from mismatch of common-mode impedance in differential pairs. Electromagnetic interference emissions and noise coupling is not strongly related to common-mode return loss. Better isolations and better decoupling of power supply noise on reference plans are good solutions to limit electromagnetic interference (EMI) caused by common-mode noise.

Many transmission protocols impose clear limits for both differential- and common-mode reflection. Common-mode noise mainly affects the jitter, which has very small margins for PAM4 modulation. Also, in the case of long reach channels where the signal must be amplified by the receiver, the amplified common-mode noise can cause high overshoot voltages at sensitive receivers. Any asymmetries in a differential transmission line produce a common signal that propagates through the device. This mode conversion is a main source of electromagnetic interference (emission/radiation). The electromagnetic compatibility compliance testing is a new condition for next-generation routers and switches at the end of the design cycle [10].

3. Electromagnetic-Field Simulations

3.1. 2D Electromagnetic-Field Simulators

ANSYS 2D Extractor uses an automatic mesh refinement in order to obtain a high-accuracy solution over broadband frequencies. It uses the finite element method, dividing the whole 2D geometry into arbitrary-sized triangle elements, as shown in Fig. 4.

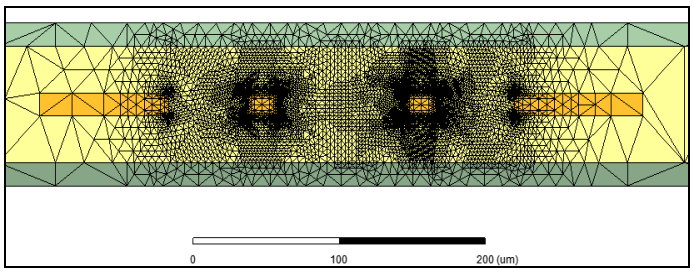


Fig. 4 Meshes for a differential stripline in an electromagnetic-field simulation

When modeling structures with nonlinear characteristics, non-uniform meshes are generally used. This software allows smaller size cells in areas that are physically small but very important regarding electromagnetic field, and bigger cells in less complex regions [12], using an adaptive algorithm towards specific desired convergence criteria [13].

In order to identify a differential stripline that respects the adopted principle, 2D electromagnetic software that models its cross section is used. For every mesh element, the Maxwell laws are applied in order to calculate the electric passive elements of the line per unit length. The boundary conditions on the interface between two elements of the geometry are automatically applied. Based on these conditions and within the desired frequency range, the 2D structure is analyzed electromagnetically. The convergence criterion of the simulation is defined as a tolerance of the error imposed by the user, in this paper having a value of 0.5%.

The main result of this 2D simulation is the characteristic impedance of the stripline structure that will be detailed in Section 5.

3.2. 3D Electromagnetic-Field Simulators

The evaluation of differential stripline transmission lines from the common-mode reflections point of view can be accurately performed using 3D electromagnetic field simulation software that implements the finite element method.

Ansys HFSS (High Frequency Structure Simulator) software is a 3D electromagnetic-field simulation tool for designing and simulating high frequency electronic products. The software is recognized for its accuracy by both academia and industry [14], generally used for analysis of three-dimensional microwave structures [15].

In this paper, the working method of Ansys HFSS simulator is based on the discretization of geometry in a tetrahedron network of arbitrary dimensions according to the geometry to be analyzed, as shown in Fig. 5.

Fig. 5 Simulated interconnects

The electromagnetic field is calculated by applying Maxwell's laws to a FEA (Finite Element Analysis) model. The automatic process adapts the mesh in consecutive steps, refining it so that it correctly captures the gradient of the electromagnetic field quantities and the process continues until the *S*-parameters or other user-defined quantity, change between two consecutive adaptive steps less than the convergence criterion imposed by the user. The frequency response of the geometry is calculated within a frequency range defined by the user. The *S*-matrix describing the analyzed multiport can be then post-processed by ANSYS HFSS as a matrix of mixed-mode *S*-parameters, allowing the evaluation of the transmission line both in differential and in common transmission mode.

4. INTEGRATED CIRCUITS LAYOUT DESIGN

The package (PKG) with electrical and structural roles can be realized in wire-bond or flip-chip technology [16]. Wire-bonding is a robust technology and its cost is a major advantage. Flip-chip's advantages regard lower-inductance power distribution network, reduced switching noise and ground bounce and lower parasitic elements due to the replacement of the highly inductive wire bonds with smaller solder balls to interface the package with the IC. Both technologies coexist due to continuous improvements.

4.1. Substrate Layers

The encapsulation of an application-specific integrated circuit (ASIC) has evolved from wire-bond to flip-chip technologies, the laminated substrate of the capsule acts like a mini-PCB with a surface of up to 60 mm × 60 mm, having between 12 and 16 metal layers.

Interconnects between the package and the silicon die serve both for electrical connection and as a method of attaching the IC to the substrate, giving it structural stability.

The package substrate is a printed wiring harness with the following laminated structure:

- The core, a middle dielectric layer with the greatest thickness, ensuring rigidity to the printed wiring.
- Metallic layers deposited on both sides by the core, as a rule from copper, in which the geometry of the elements of interconnection of the electrical circuit is realized by corrosion: signal paths and power plans.
- The build-up dielectric layers deposited to separate the metal layers. The dielectric filling of the corroded copper areas is realized from the same material.
- VIA (Vertical Interconnect Access), vertical elements used to make the connection between the metallic states. A VIA is made by laser or mechanical drilling of the

metal and dielectric layers, through which the connection must be made, followed by the plating of the cylinder thus formed or its filling with conductive material – usually copper.

- A thinner dielectric layer, called solder-mask is applied over the outer metal layers, which protects copper against oxidation and accidental short-circuiting.
- In the connection areas with the IC and the PCB, the solder-mask layer is not applied, thus allowing the bumps and the balls to be joined.

The stack of metal and dielectric layers that make up the structure of the printed circuit called substrate, which is the subject of this work, are disposed in 2 solder masks of 20 µm, 12 copper layers of 15 µm and 11 intermediary dielectric build-ups of 30 µm. For differential pairs routing, the first 3 metal layers will be used. The signal leads – paths are created on layer 2 and the reference plane uses layers 1 and 3. Frequency modeling of the electric properties of the dielectric, in ANSYS electromagnetic-field simulation programs integrates the Djordjevic-Sarkar mathematical model that allows the extrapolation of electrical properties over an entire frequency range starting from the known values at a single frequency point.

4.2. Routing Rules

The correct execution of electronic circuits involves more than their simulation using an Electrical Computer Aided Design (E-CAD) software environment. It is mandatory to consider the manufacturing process from the design stage as well. Although the technology to produce printed circuits is advanced and structures of the order of microns can be manufactured, certain rules are imposed for the dimensions and spacing of the conductive elements. These layout routing rules, as shown in Fig. 6, differ from one manufacturer to another, depending on manufacturing methods accuracy or on manufacturing equipment.

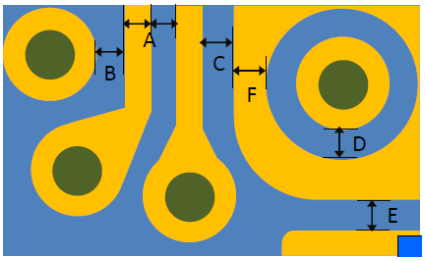


Fig. 6 Routing rules

The tolerance of the manufacturing processes translates into a percentage by which the physical dimensions of the topology elements of a printed circuit may vary from the nominal ones, required by the engineer that performs the routing. The lower the manufacturing tolerance and the greater the accuracy of the electrical circuit geometry dimensions are, the more expensive the manufacturing and assembly process will be. In the highly competitive environment of the electronic device market, balancing design effort and manufacturing cost becomes critical.

In order to achieve the differential stripline lines in a substrate manufactured with advanced technologies, the following manufacturing rules are required:

- Minimum width of a path (A): 14 µm;
- Maximum width of a route: 89 µm;
- Elements with a constant width greater than or equal to 90 µm are considered planes (F);
- Minimum spacing between paths (noted A): 14 µm;
- Minimum spacing between paths and planes (C): 40 µm.

4.3. Signal Integrity Rules

The signal integrity refers to the quality of the electrical signals as amplitude and synchronization. As most digital systems use variable or even programmable frequency data transfers, the passive elements that make up the transmission environment are required to comply with signal integrity conditions across the frequency range. For the same reason, the signal integrity requirements for a segment of the transmission channel, in this case the package of an IC, are expressed in the frequency domain, the requirements expressed in the time domain being used to validate the entire transmission channel.

For the IC proper functioning, the rules of signal integrity are provided by its designer. Considering only the transmission of differential signals, the rules of signal integrity are expressed using five main terms:

1. Characteristic Impedances

The ratio of the amplitudes of voltage and current of the wave propagating along a transmission line, up to 15 GHz frequency domain is simulated as characteristic impedance. The value of differential-mode impedance is twice the value of odd-mode impedance and the value of common-mode impedance is half the value of even-mode impedance. Two parallel traces in a PKG substrate are coupled and characteristic differential impedance of 100 Ω will be used in simulations of SerDes signals. Common-mode impedance will be 25 Ω for noise.

2. Insertion-Loss (IL)

For a transmission line, the signal power loss due to device loss is usually expressed in dB. Differential attenuation introduced by the package must not exceed 15% of the signal amplitude up to the first spectral component of the highest frequency useful signal of 15 GHz. The insertion *S*-parameters (S_{21}) should not decrease below -1, 4 dB at frequencies lower than 15 GHz in SerDes circuits simulations [17].

3. Return-Loss (RL)

For a transmission line, the power loss in a signal returned/reflected by a discontinuity, usually due to a mismatch of the terminated load or impedance discontinuity across the conductive path is also expressed in dB. Further referred to as signal reflection, it is expressed by an element of the differential parameter *S*-matrix (S_{dd11}), tolerated if they fall below a frequency-dependent limit.

Typical RL values could range from –15 to –60 dB. Many designers target –10 dB as the critical value and try to keep Return Loss lower than –10dB at the desired signal speeds. In most cases, –60 dB is more desirable [18].

4. Crosstalk (XTalk)

Crosstalk is the mutual influence of two parallel, nearby routed traces. As an undesired phenomenon (an inductive and a capacitive coupling) crosstalk is the effect created in a specific circuit (victim) by the signal transmitted in another circuit (aggressor). It is expressed by specific elements of the differential parameter *S*-matrix and it has frequency dependent limits in simulations [19]. XTalk perceived as a path-based approach for identifying pairs of pathways that may crosstalk, is used in computation [20], [21].

5. Common Mode Return-Loss (CMRL)

Reflections of the common mode signal, expressed by the commonly used *S*-parameter S_{cc11}, are tolerated if they fall below a specific limit, frequency dependent, in SerDes circuits' simulations [19].

5. Simplified Structures Evaluations

Inserting guard traces into a simplified structure (see Fig. 7), the cross talk is reduced by coupling the electromagnetic waves to the guard trace.

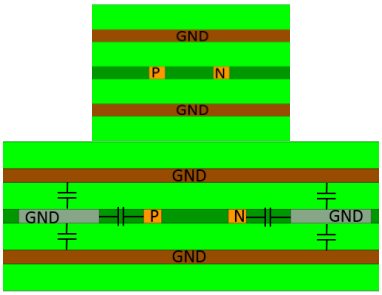


Fig. 7 Guard traces added to a simplified structure

The elements' dimension for a simplified structure are shown in Table 1.

Table 1 Routing Rules

Parameter	Dimension [µm]
Metal layer width	15
Dielectric width	30
Trace width	21
Trace separation	90
Separation between trace and guard trace	55
Guard trace width	90

Using the simulation software based on Maxwell's equations in the frequency range (1-15) GHz, the capacitance, inductance, and characteristic impedance values are calculated and the parameters of the maximum length of the 10 mm paths and the signal growth time of 14 ps are defined.

5.1. Characteristic Impedance for Stripline Topology

As shown in Fig. 8, characteristic impedance is frequency dependent.

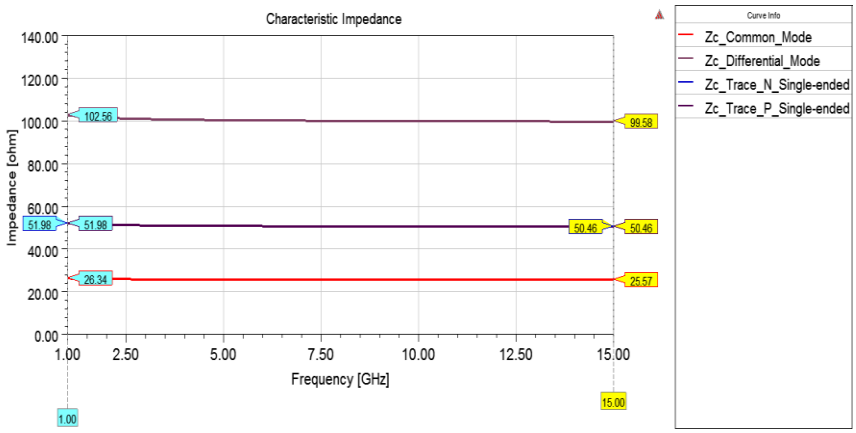


Fig. 8 Simulated characteristic impedance

At 15 GHz, the wavelength becomes twice time greater than the differential pair's length, so it becomes very important to match the characteristic impedance here, using Ansys 2D Extractor, in good agreement with the common-mode values and differential-mode impedances from Integrity Rules given in the previous Section.

5.2. Noise in a Differential Pair Evaluation

A mixed-mode multiport, according to Fig. 3, is defined by ports placed at the end of each signal path of the differential pair, considering the input IN at the end where the signal is applied and output OUT the end where the signal is transmitted. The ports used in simulation are placed as SE (Single-Ended) ports of 50 Ω standard impedance and the reference to the GND conductor. In order to highlight the effect of the bends of a differential pair in a package's structure, the conversion of the differential signal into a common signal is evaluated due to discontinuities introduced in signal propagation path. The common mode signal generated by a discontinuities (bends in this case) will propagate through the conductive structure in the two main directions: once as a commonly reflected signal having the opposite direction to the source differential signal that will be referred as RCD (Reflected Common-mode signal by conversion from Differential mode) and as a common mode signal transmitted in the same direction as the source differential mode signal that will be referred as TCD (Transmitted Common-mode signal by conversion from Differential mode). Since data transmission through a SerDes interface is purely differential, both at the transmitter and at the receiver, it can be considered the commonly generated signal by differential conversion as a noise that will be referred as CMN (Common Mode Noise). In this paper, the CMN is evaluated due only to the package structure as a sum of RCD and TCD.

5.3. Evaluation of a Differential Pair with Bends

The stripline structure can reduce the common-mode noise using a practical routing scheme, based on the same velocity of even-mode and odd-mode signals [5]. Using dual back-to-back coupled bends with different angles, keeping the same routing rules for the matched impedance of the stripline differential pair, the same trace length without the significant skew can be maintained [5]. A right angle in a trace is not desired because the capacitance increases in the region of the bend, and the characteristic impedance changes. This impedance change causes reflections. So, right-angle bends in a trace are avoided and they are replaced with at least with two 45° bends, as shown in Fig. 9.

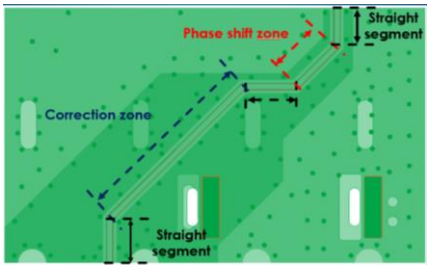
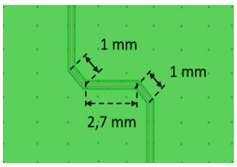
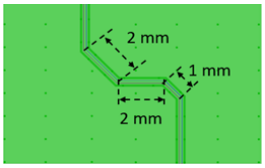


Fig. 9 Noise compensation zones in bends

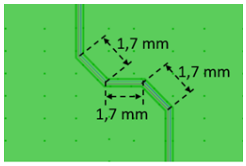
Based on this principle, four test models with four bends were developed to evaluate the effect of 45˚ bends on the common reflections. In order to facilitate the presentation of the simulation results, the four models, designed as shown in Fig. 10, are presented besides the straight model. They will be further referred as A, B, C and D models. The four models with bends are simulated using the same materials, boundary conditions and excitations for the entire frequency range between the DC point and the maximum frequency of the highest spectral component of 45 GHz.



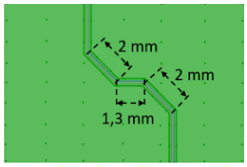
Model A 1-2.7-1



Model B 2-2-1



Model C 1.7-1.7-1.7



Model D 2-1.3-2

Fig. 10 Examples of different models with bends investigated

5.4. Differential Pair without Bends as Reference Model

Using an initial 3D simulation for a straight basic structure without bends, the first three *S*-parameters IL, RL and CMRL can be extracted as reference, as shown in Fig. 11.

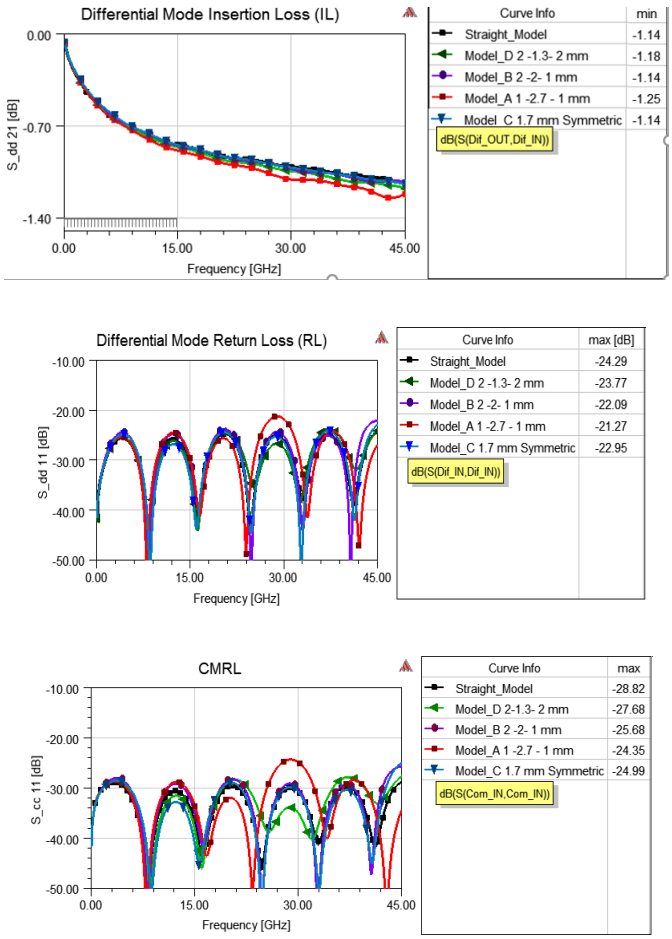


Fig. 11 Differential- and common-mode evaluation for the tested models

The commonly used reflection attenuation limit (CMRL) also depicted in Fig. 11 describes the common mode reflections generated by a common mode signal. It assumes the condition to be a non-ideal signal, containing both the differential mode component and a common mode noise due to the IC output stage, transmitted through the package. In differential pair structure simulations in frequency domain, outside noise is not determined and the CMRL cannot be interpreted as an effect of the differential pair bends, although in practice they will negatively influence the CMRL.

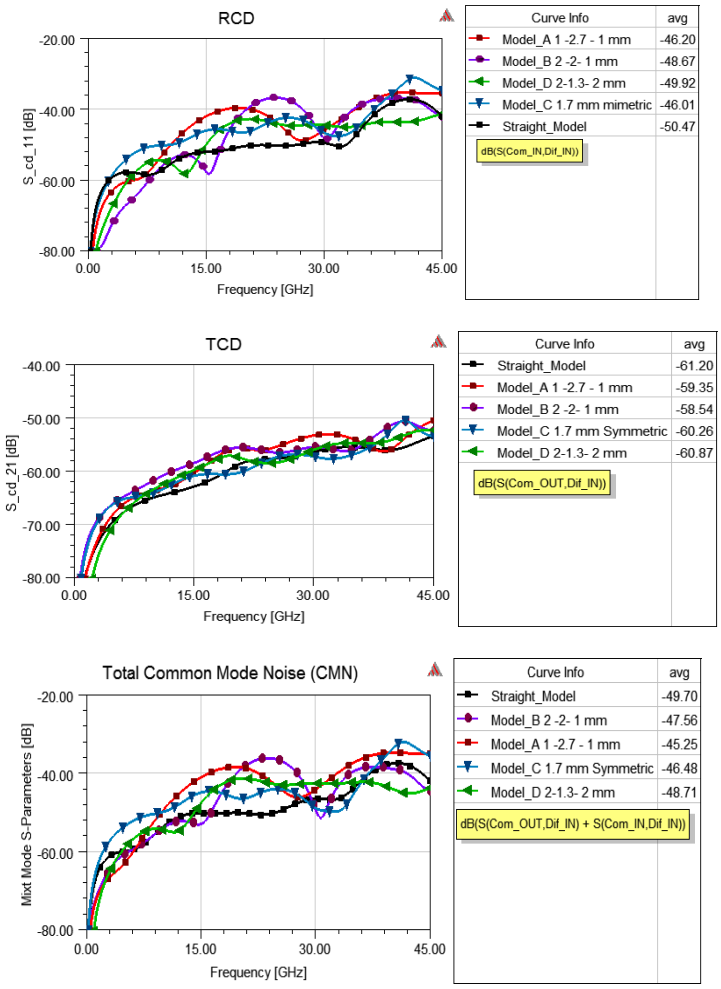


Fig. 12 Mixed-mode evaluation for the tested models

The results of common-mode reflected signal converted from differential-mode signal (RCD), common-mode transmitted signal converted from differential-mode signal (TCD) and total common-mode noise generated (CMN) are shown in Fig. 12.

In the package RCD signal is critical due to its direction into the integrated circuit affecting the entire output buffer, more than TCD signal, seriously attenuated in communication channel consisting of three minimum elements: the IC package that emits the signal, the PCB and the IC receiver package, the most attenuating part remaining the PCB element.

5.5. Differential-Mode Parameters Evaluation

The IL and RL, or S_{dd21} and S_{dd11} parameters, of all four models with bends are similar to the ones of the straight model, because the differential attenuation is mainly influenced by the equivalent resistance of the differential pair and while keeping the impedance controlled routing, length matching between the pair traces is enough to keep reflections below the necessary level. The Insertion Loss (IL) for the first model is slightly different at high frequencies because it has the largest distance (2.7mm) between the phase shift and the correction area. In conclusion, for an IC encapsulation circuit, 45° bends can affect differential transmission if the distance between the phase area and the correction area is closed to the wavelength [22].

5.6. Common-Mode Parameter Evaluation

The higher the maximum value of CMRL is, the lower the transmission performance through this model will be. By evaluating the results of the CMRL attenuation versus frequency in Fig. 11, all four tested models with 45° bends have a more unfavorable behavior than the straight model. The key decision factor in their overall evaluation is the maximum value over the whole analyzed frequency range. On the graph, the maximum CMRL values are periodically repeated after 8.25 GHz, due to the dimensions of the GND plane of each model corresponding to the quarter of the wavelength of the frequency resonance, finally 6 frequency areas can be delimited on the graph from Fig. 11, mainly linked to the distance between the phase shift and the correction areas. The greater the distance between the two zones becomes, the more the reflections increase, a strong effect is in case of the A model, as the most unfavorable case tested. The most favorable behavior has the C model, with perfect symmetry and an average distance between the two zones, and D model, with a small distance between the zones, although the phase shift and correction segments have the largest length of the tested ones.

5.7. Mixed-Mode Parameters evaluation

Mixed-mode *S*-parameters, RCD and TCD, S_{cd11} and S_{cd21} parameters describe signal conversion from differential- to common-mode. The signal resulting from this conversion is added to the noise that can be generated by the IC output stage, triggering a negative chain reaction, which disrupts the useful signal. From Fig. 12, the C model has greater RCD values only at high frequencies, above 38 GHz where spectral components have lower amplitude, and the A model can be considered as the worst case. The main elements that can worsen common mode generated reflections are the phase shift zone length and the distance between the two zones. Although common mode reflections focus the IC output stage transmitting the signal through the package, the common mode transmitted signal due to the differential conversion affects the IC input stage that receives it as an additional input signal. Thus, the two mixed *S*-parameters values, RCD and TCD are equally important for a proper functioning of a communication channel through the SerDes PAM4 interface.

According to the classification of the average TCD results, the main factor influencing the conversion of a differential signal into a common-mode signal is the distance between the phase shift area and the correction area [23]. The shorter this distance is, the generated phase shifted noise has a shorter propagation time and the less TCD becomes, therefore

preferable, noticing that if the two zones do not have equal lengths, the results will be more unfavorable, even if the distance between them is smaller than in the asymmetric case. The total noise commonly generated by the 45˚ bends in the differential conversion is calculated as the sum of RCD and TCD and are depicted in Fig. 12 and summarized in Table 2.

Table 2 CMN Models Classification

Model	Phase Zone [mm]	Distance [mm]	Corr. Zone [mm]	CMN Average [dB]
Straight	-	-	-	–49.70
D	2	1,3	2	–48.71
B	2	2	1	–47.56
C	1.7	1.7	1.7	–46.48
A	1	2.7	1	–45.25

As the average TCD values are generally lower, the same rule about the distances between the two zones stays as the main element that influences the total common noise (CMN) generated by conversion from a differential signal. In conclusion, limiting the attenuation of reflection, CMN reduction, can be achieved in two ways:

- Common impedance matching, in order not to generate common mode noise reflections inserted into the package and further into the transmission channel by the IC output stage;
- Optimization of the zones with impedance discontinuity, in printed circuits, that means the 45˚ bends optimization.

The bends optimization can be done considering the three main zones: the phase shift zone, the correction zone and the distance between them. In order to limit common-mode noise generation by differential conversion, which overlaps the common-mode noise inserted by the IC, it is primarily intended that the distance between the two zones to be as small as possible and their lengths to be as close as possible or even the same.

6. Common Mode Noise In Optimized Interconnects Paths

The conclusions of previous Section are verified for a real package case, shown in Fig. 13. The medium-sized package has 17 mm sides and the stack up previously described in Section 4. The package can encapsulate a 4 mm side IC and performs the interconnection between the IC and the PCB of 24 SerDes PAM4 channels with a 56 Gbps per channel rate. The package geometry has been designed using E-CAD software, Allegro Package Designer and then automatically recognized in electromagnetic-field simulation software, preserving the accuracy of the geometric details. The differential pair in the real package requires 45˚ bends both to reach its connection to the PCB, a point that is not aligned with the differential signal output IC area and to bypass passive components assembled on the package such as decupling capacitors symbolized using the C letter in Fig. 13.

Besides limiting the space where the differential pairs can be designed due to the passive components mounted on the package surface, the routes are conditioned to bypass the groups of VIAs that link the passive components mounted on the package and the power distribution network (PDN) on the lower metal layers, usually below the dielectric core.

In the real package paths electromagnetic simulation, the signal conductors' geometry and the GND conductor that serves as a reference plane for the routes are identically maintained. A major simplification consists in keeping only the coplanar guard elements from the metallic layer, where the paths of the differential pair are realized in, to highlight the main effect of the bending technique on the common-noise.

In Fig. 14 the real routing has a length of 7.12 mm, indicating the signal traveling through the IC package, from input (IN), towards the PCB, (OUT).

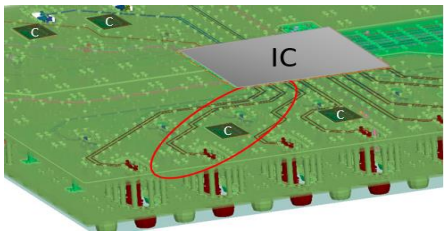


Fig. 13 Real package

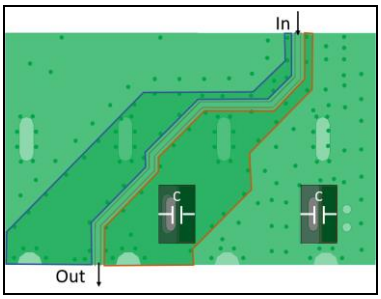


Fig. 14 Initial stripline routing

This simplified model will be referred as Initial in the electromagnetic-field simulations shown in Fig. 15 and in Fig. 16, in contrast with the optimized real model which is named PKG. The Initial model is also depicted in Fig. 17, where the phase shift zone and the correction zone are identified. Initial model's greater number of 45˚ bends compared to all simplified structures from Section 5, disturbs the Insertion Loss linear trend versus frequency, as shown in Fig. 15. The 45˚ bends have no negative effect on reflection as differential RL shows. Due to the reduced length compared to the five models from Section 5, the CMRL have similar values. In Fig. 16, RCD has greater values till 20 GHz and TCD has higher values than the equivalent model, but low enough to be attenuated along the transmission channel. Noting that the negative effect of 45˚ bends on total noise is commonly pronounced at frequencies up to 20 GHz, the differential pair optimization becomes a true necessity.

The initial pair, shown in Fig. 17 is optimized in Fig. 18. This consists in changing the dimensions of several zones in order to reduce the common reflected signal and transmitted by differential conversion. The initial differential pair dimensions are shown in Table 3 and they are compared with the final dimensions of the optimized structure shown in Fig. 18. By this optimization it was intended that the differential pair should have the smallest distance between the phase shift area and the correction area and a smaller number of bends of 45˚. In order to reduce the number of 45˚ bends, a compromise was needed with respect to the length of the correction area segment, which became longer.

Table 3 Real Package Bends Zones Dimensions

Element	Initial dimensions [mm]	Optimized dimensions [mm]
Straight segment	0.9	0.7
Phase Shift D1	0.8	1.0
D1 – C1 distance	1.4	0.9
Correction zone C1	1.4	3.3
Straight segment	0.3	0.8
45˚ bend – D2	–	–
D2 – C2 distance	1.5	–
Straight segment	0.82	–

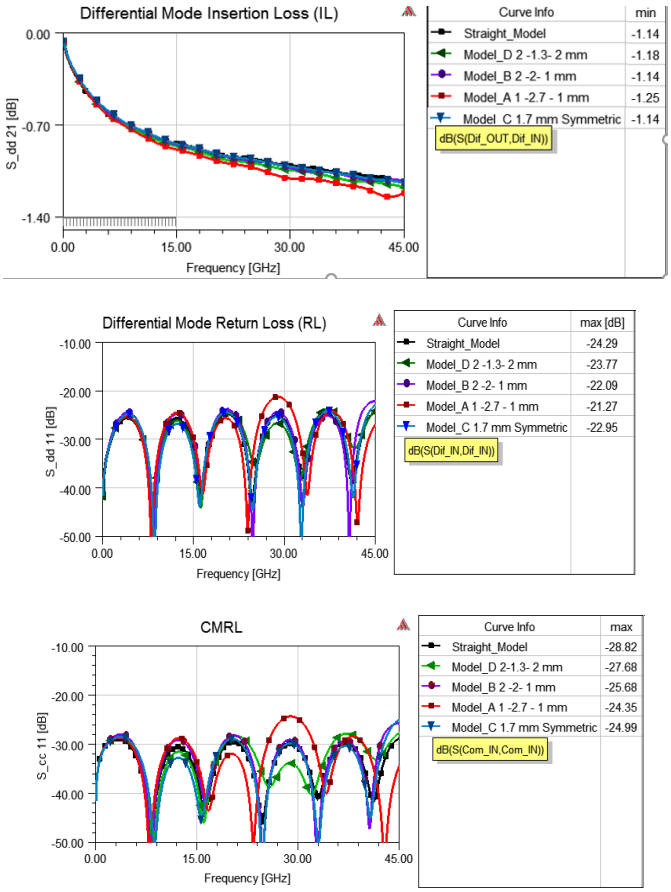


Fig. 15 Differential and common mode evaluation for the Initial and real package

Due to the changes made to optimize the differential pair, the length of the pair changed to 6.7 mm.

The improvement of the behavior of the differential pair in frequency was noticed only in terms of the common and mixed mode *S*-parameters.

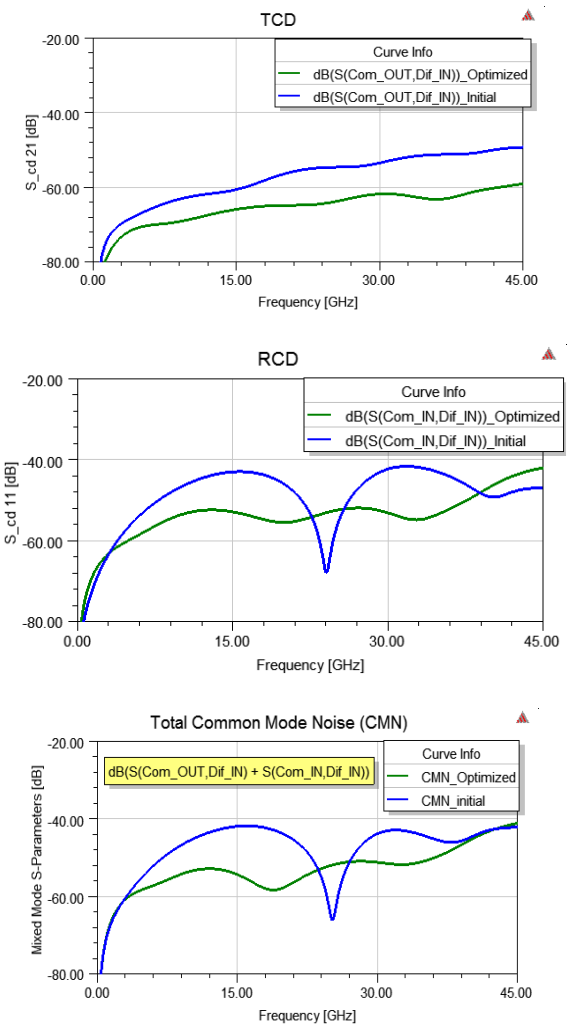


Fig. 16 Mixed-mode evaluation for the Initial and real package

From the point of view of transmitting a signal or a common-mode noise, the common-mode reflections are improved at high frequencies, over 38 GHz, in the optimized case compared to the original case as shown in the last graph in Fig. 16. Because the distance between the phase shift and correction zones was smaller after optimization, the RCD was reduced. The common mode signal CMN transmitted in the same sense as a source

differential mode signal, TCD, is greatly attenuated due to the optimization of the number of bends that the source differential signal encounters in its path (see Fig. 18).

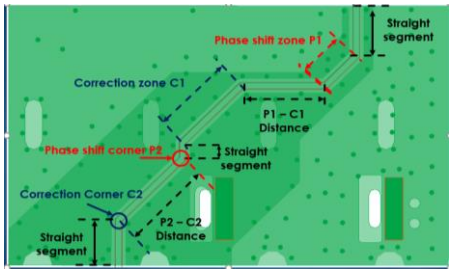


Fig. 17 Initial Structure for real stripline routing

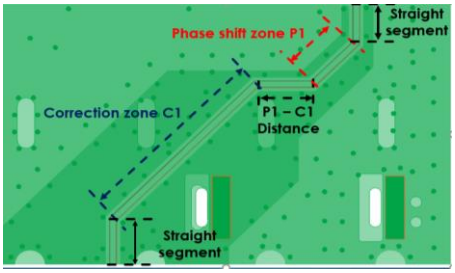


Fig. 18 Optimized Structure

7. CONCLUSIONS

The paper analyzed the common-mode noise effects due to 45˚ bends in differential transmission lines. The study focused the stripline differential transmission lines, from an IC encapsulating circuit, for high-speed data flow transmitted through a SerDes PAM4 interface. The 45˚ bends are mandatory in package design to interconnect the integrated circuit with the PCB, linking points that cannot be aligned, bypassing passive components, decoupling capacitors, mounted on the surface of the package.

Up to 15 GHz in order to ensure the signals integrity, it was enough to balance the differential pair routes lengths, neglecting the signal conversion from differential to common mode. This conversion between the two transmission modes is a negative effect introduced by discontinuities in the differential pair.

The study started by identifying a differential pair structure with coplanar elements and adapted differential impedance, using electromagnetic modeling and simulation. Using previously identified dimensions for the stripline structure with impedance adaptation, five differential pairs test models on average length about 10 mm in flip-chip encapsulation circuit have been designed: a straight model as reference and four different models including 45˚ double bends with three focused main zones: the phase shift zone, the correction zone and the distance between them. The five test models were analyzed in frequency domain using 3D electromagnetic simulation. Differential, common-mode and mixed-mode *S*-parameters frequency dependence, as graphical results, were compared with operating requirements according to the IC manufacturer up to 45 GHz. These models were also evaluated from common-mode noise generated by 45˚ bends perspective, expressed as mixed-mode parameters: common-mode reflections due to a differential mode source signal, S_{cd11} or RCD, and as common-mode signal transmitted in the same sense as the source differential mode signal, S_{cd21} or TCD. Their sum, the total common noise CMN was also investigated. Comparing the results for the five test models it was concluded that the main factor that negatively influences the generation of a common mode noise by conversion from differential mode is the large distance between the phase shift zone and the correction zone. The next factor is the symmetry between them. This generated common-mode noise, CMN, propagating along the differential paths has an unfavorable behavior at high frequencies.

These conclusions were verified by optimizing a stripline differential pair from a real package with a length of 7.12 mm. The total generated common noise, CMN, has been evaluated by comparing the results of its 3D electromagnetic simulations with the results of the initial model. Because the noise generated by the bends is predominantly reflected towards the IC output buffer, it was decided to optimize the differential pair by reducing the distance between the phase shift and the correction zones and by reducing the number of bends, from 6 to 4 bends.

Comparing the initial model results versus the optimized solution in a real package, an improvement in terms of the total common noise generated by differential conversion over the entire frequency range up to 45 GHz has been obtained.

Future developments will focus 45˚ bends effects on the crosstalk between the different pairs on the adjacent metal layers. In designing multi-layered flip-chip packages, although the output and the input signals are placed on different layers, they share a metal layer that serves as a reference plane for both classes of differential signals. Thus, the common noise generated by the bends in the differential pairs by the un-attenuated output signals can be electromagnetically coupled through the common ground panel with the input signals that have been attenuated due to the transmitted channel.

REFERENCES

[1] A. Mutschler, *Higher performance helps smooth the gap between analog and digital, but it adds a number of new twists*. Available: https://semiengineering.com/wrestling-with-high-speed-serdes/.
[2] IEEE Electronics Packaging Society, Heterogeneous Integration roadmap. 2019, Available: https://eps.ieee.org/images/files/HIR_2019/HIR1_ch02_hpc.pdf.
[3] D.A. Nesic, I. Radovic, "Parallel-Strip Line Stub Resonator for permittivity Characterization", Facta Universitatis, Series: Electronics and Energetics, vol. 33, Nno. 1, pp. 61–71, March 2020.
[4] E. Bogatin, Signal and Power Integrity – Simplified. New Jersey: Prentice Hall, 2009, pp. 475–553.
[5] G.H. Shiue, W.D. Guo, C.M. Lin and R.B. Wu, "Noise Reduction Using Compensation Capacitance for Bend Discontinuities of Differential Transmission Lines", *IEEE Trans. Advanced Packaging*, vol. 29, pp. 560–569, August 2006.
[6] E. Kunz, J.Y. Choi, V. Kunda, L. Kocubinski, Y.Li, J.R. Miller, G.J. Blando and I. Novak, "Sources and Compensation of Skew in Single-Ended and Differential Interconnects", *Signal Integrity Journal*, April 2017.
[7] S.C. Thierauf, *Understanding Signal Integrity*. Artech House, 2011, pp. 88–89.
[8] P.R.Gray and R.G.Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd. ed. New York: Wiley, 2009, pp. 291–292.
[9] D. E. Bokelman, "Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation," *IEEE Trans. Microw. Theory and Techn.*, vol. 43, pp. 1530–1539, July 1995.
[10] KEYSIGHT Technologies, "*S*-Parameter Measurements, Basics for High-Speed Digital Engineers". Available: http://literature.cdn.keysight.com/litweb/pdf/5991-3736EN.pdf, May 2019.
[11] N. Na, M. Arseneault, K. Yonehara, H. Hu, D. Zwitter, E.M. Wolf, K. Srinivasan, C. Cox and R. Anderson, "Common Mode Return Loss Consideration in Wirebond Packaging for High Speed SerDes Links", In Proceedings of the IEEE Electrical Performance of Electronic Packaging, Scottsdale, AZ, USA: World Scientific, 2006.
[12] M. Kostic, N. Doncov, Z. Stankovic, J. Paul, "Numerical Compact Modeling Approach of Dispersive - Magnoelectric Media Based on Scattering Parameters", Facta Universitatis, Series: Electronics and Energetics, vol. 33, no. 1, pp.73–82, March 2020.
[13] Ansys, "2D Extractor Solver Option". Available: https://www.ansys.com/products/electronics/option-2d-extractor-solver.
[14] Ansys HFSS, Available: https://www.ansys.com/products/electronics/ansys-hfss, July 2019.
[15] A.S. Tatarenko, D.V. Snisarenko, M.I. Bichurin, "Modeling of MagnetoElectric Microwave Devices", Facta Universitatis, Series: Electronics and Energetics, vol. 30, no. 3, pp. 285–293, September 2017.

[16] L. Ammann, "The Package Interconnect Selection Quandary", EETimes, 2003, Available: https://www.eetimes.com/the-package-interconnect-selection-quandary/#.
[17] D. R. Stauffer, J. Trinko Meckler, M. Sorna, K. Dramstad, C. R. Ogilvie, A. Mohammad and J. Rockrohr "High Speed Serdes Devices and Applications", Springer, 2008.
[18] Timbercon, "Connector return Loss", Available at: https://www.timbercon.com/resources/glossary/connector-return-loss/.
[19] 58G & 112G PAM4 & NRZ DSP-Based Long-Reach SerDes Family in 7nm, Available at: https://www.esilicon.com/products/high-performance-networking-computing-ip/serdes.
[20] A.N. Tegge, N. Sharp and T.M. Murali, "Xtalk: a path-based approach for identifying crosstalk between signaling pathways", *Bioinformatics*, vol. 32, no. 2, pp. 242-251, January 2016.
[21] Freescale Semiconductor, "High Speed Layout Design Guidelines, Application Notes", Available at: https://www.nxp.com/docs/en/application-note/AN2536.pdf.
[22] Z. Popovic and E.F, Kuester, "Principles of RF and Microwave Measurements", 2017, pp. 1, Available at: https://ecee.colorado.edu/~ecen4634/4634-Lectures-Labs.pdf.
[23] Texas Instruments, "High speed Layout Guide, Texas instruments Application Report", 2017, Available at: http://www.ti.com/lit/an/scaa082a/scaa082a.pdf.