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DESIGN OF EFFICIENT DELAY BLOCK FOR LOW FREQUENCY APPLICATION

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Abstract. *In recent years researchers have been focusing on the design of low power and small size oscillator for emerging areas of interest such as the internet of things (IoT) and biomedical applications. In this paper a new delay block for ring oscillator is proposed using CMOS inverter cascaded with inverted current starved inverter (CICSI). The designed delay block provides approximately 50% more delay with a smaller number of transistors than the conventionally designed circuits. Furthermore, a ring oscillator and a non-overlapping clock (NOC) generator are designed using it. The designed circuits can be used in switched capacitor (SC) circuits, analog mixed signal circuits to meet the need for low frequency portable biomedical applications. The designed circuits are simulated on Generic 90nm 1.2V Process Design Kit (GPDK90) using Cadence Virtuoso Design Environment. The simulation result shows the delay of the CICSI delay block is 592ps. The ring oscillator using 101 stages of delay block is designed and it is shown that it operates at a frequency of 17MHz with a power consumption of 420µW.*

Key words: *CMOS inverter, Inverted current starved inverter, NOC*

1. INTRODUCTION

In modern CMOS VLSI design, the researchers focus on switched capacitor (SC) technique to implement the design due to its enormous advantages like less power, smaller area, higher precision, and easy implementation on chip [1-3]. The optimal realization of SC circuits depends upon the efficient designing of a non-overlapping clock (NOC) generator. The traditional NOC consists of a Ring oscillator, NOR gate, and cascaded delay blocks. There are several methods reported for the generation of delay block, which is further used to design the ring oscillator and NOC [4-14]. For low frequency applications, the delay bock should provide more delay. The most efficient and easiest way to design the delay block is using CMOS inverter and current starve inverter [15-16]. Different techniques are reported to increase the delay of the delay block by implementing a voltage scaling technique [6], transmission gate method [7], and inverted inverter [17, 18].

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Cascaded inverter with an inverted inverter is used to get more delay compared to conventional delay blocks reported by A.K. Mal et all [17]. The drawback of the delay block is that two or more inverted inverters cannot be cascaded due to logic level restoration problem [6, 17]. So, to improve the delay without having logic level restoration problem inverted current starved inverter (ICSI) is used in place of an inverted inverter. The proposed cascaded inverter with inverted current starved inverter (CICSI) delay block consists of a CMOS inverter cascaded with an ICSI for a single delay block. The CICSI delay block has more delay mainly due to three reasons. First, the output voltage swing of the CICSI is not rail to rail. Second, the transistors of ICSI are not allowed to turn off during the transition of the input signal, so delay due to switching increases. Third, the current flowing through the CICSI is smaller compared to previously reported work [17]. The CICSI circuit produces higher delay with a fewer number of transistors, so that it can be used in low power and low frequency applications.

This paper is organized as follows: in Section 2, the delay block, ring oscillator, and NOC are discussed. Section 3 gives a detailed analysis of the delay calculation of the delay block. Section 4 presents the results and analysis, finally, Section 5 draws the conclusions of the work.

2 CICSI Structure

The previously reported delay block using an inverted inverter circuit has more delay but it shows a two-stage problem [17]. To improve the delay further, a CMOS inverter cascaded with inverted current starved inverter (CICSI) delay block as shown in Fig.1 is proposed in this paper. The inverted current starved inverter is designed by swapping PMOS with NMOS, and NMOS with PMOS, and shorting the gate terminal of all NMOS and PMOS transistors. The CICSI has two stages. The first stage is normal CMOS inverter and the second stage is a modified current starved inverter which acts as a cascaded pass transistor [1]. In the second stage, the drain terminal of NMOS (M3) as shown in Fig.1 is connected to V_{DD}, and the source is connected to the drain terminal of NMOS (M4). A logic '1' input activates the gate of both M3 and M4. The drain of PMOS (M6) is grounded and source is connected to drain of PMOS (M5). A logic '0' input activates the gate of both M5 and M6. By applying the concepts of cascaded pass transistor logic [19], when the second stage of CICSI is given logic '1', then the M4 pass gate is turned ON and the output will be $\approx V_{DD}-V_{Tn}$. Similarly, when a logic '0'is applied to the second stage then M5 is turned ON the output will be $\approx |V_{Tp}|$, where V_{Tn} and $|V_{Tp}|$ are the threshold voltage of the M4 and M5 transistors respectively. For GPDK 90 nm process, with V_{DD} = 1.2 V, and V_{Tn0} and $-V_{Tp0}$ are approximately 0.15V. The output voltage of the CICSI is from 0.15 V to 1.05 V.

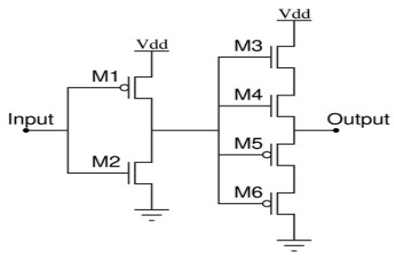

Fig. 1 CICSI delay block of NOC

The output voltage swing of the inverted current starved inverter is smaller by one threshold voltage on both sides as per the principle of cascaded pass transistor logic. So, the combination of CMOS inverter followed by inverted current starved inverter's output signal swing is not rail to rail. When this output is fed to the next stage inverter, the output is not affected much due to the fact that the basic CMOS inverter provides an excellent gain in between voltage levels V_{IL} and V_{IH} [19]. The output voltage swing of the next CMOS inverter is not affected as the input to the CMOS inverter is either less than V_{IL} or more than V_{IH}. The delay of the inverter circuit is inversely proportional to the current flowing through it [19]. In the proposed CICSI block, smaller amounts of current flow as compared to the conventional circuit.

Ring oscillators are realized by cascading an odd number of inverters [4, 17-19]. The ring oscillator using the CICSI block is shown in Fig.2. The frequency of oscillation for a ring oscillator is given by

$$f_{osc} = \frac{1}{2\,n\,\tau_p} \tag{1}$$

where 'n' is the number of inverter stages and 'τ_p' is the average propagation delay of a single CICSI delay block. As the frequency of oscillation depends on the delay introduced by each inverter stage, so for low frequency applications the total delay must be large at the output.

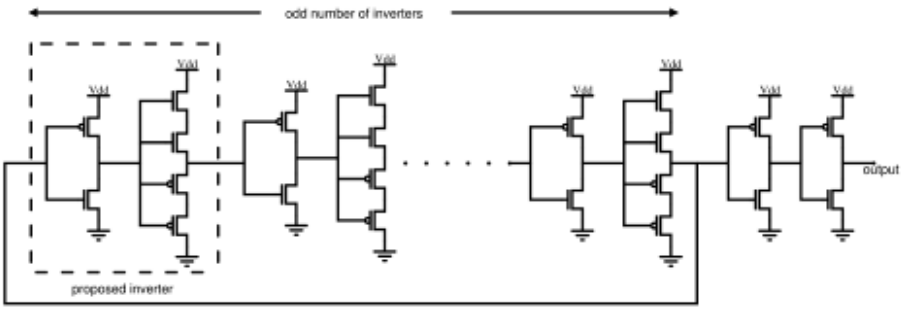

Fig. 2 Ring oscillator using CICSI delay block

The block diagram of the basic non overlapping clock (NOC) generator is shown in Fig. 3. An even number of delay blocks is connected in series in NOC generator [1]. The different non overlapping clock period can be obtained by suitably choosing number of cascaded delay blocks. The total non-overlapping clock period is given by $N \times \tau_p$, where 'N' represents the number of CICSI delay block and 'τ_p' represents the average propagation delay of single CICSI delay block.

The NOC output does not have a rail to rail swing, so two CMOS inverters are connected in series (as buffers) at the end of the delay block to make the output signal swing rail to rail.

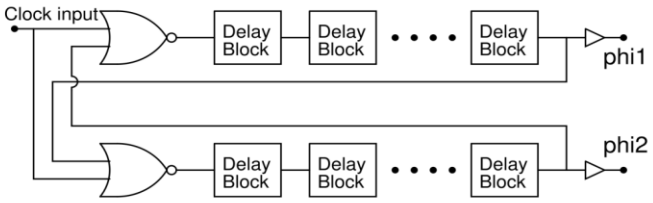

Fig. 3 NOC block

Fig. 4 shows the voltage transfer characteristic (VTC) of the CMOS inverter, inverted inverter [17], and the proposed inverter (CICSI). In the figure CMOS inverter shows rail to rail swing (0 - 1.2 V) but inverted inverter does not show rail to rail output. The VTC of the CICSI though not having rail to rail swing does not degrade from the inverted inverter. From the VTC of the CMOS inverter it is found that the transition region extends from 0.328 V to 0.6 V. So the input below 0.328V and above 0.6V is considered as perfect logic '0' and logic '1' respectively. For GPDK 90nm process $V_{Tn} = -V_{Tp} = 0.15$ V, the output swing of the CICSI is between 0.15 V to 1.05V (approximately) and it is recovered by the next stage CMOS inverter. In these three designs minimum transistor sizing ratio (W/L=120nm/100nm) with a voltage supply of 1.2V are used.

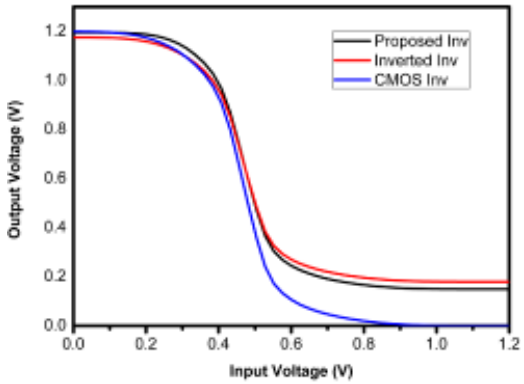

Fig. 4 VTC Curve

3. DELAY ESTIMATION

In this section the delay of the CICSI delay block consisting of a CMOS inverter and ICSI is calculated. The delay of the cascaded block is calculated one by one and then combined to get the final delay. Then the frequency of a ring oscillator which is designed using an odd number of such delay blocks is estimated.

The delay of CMOS inverter is calculated in two steps. When the output of CMOS inverter changes from logic '1' state to logic '0' state, the delay is defined as propagation delay (high to low) which is denoted by τ_{pHL}. Similarly, when the output of CMOS inverter changes from logic '0' state to logic '1' state, the delay is defined as propagation delay

(low to high) which is denoted by τ_{pLH}. Combining both the delays, the total propagation delay [17] (high to low) is expressed as

$$\tau_{pHL} = \frac{C_{load}}{k_n(V_{DD} - 2V_{Tn})}\left[\frac{4V_{Tn}}{V_{DD} - 2V_{Tn}} + \ln\frac{V_{DD}}{3V_{DD} - 4V_{Tn}}\right] \tag{2}$$

Similarly, the propagation delay [17] (low to high) is estimated as

$$\tau_{pLH} = \frac{C_{load}}{k_p(V_{DD} - 2|V_{Tp}|)}\left[\frac{4|V_{Tp}|}{V_{DD} - 2|V_{Tp}|} + \ln\frac{V_{DD}}{3V_{DD} - 4|V_{Tp}|}\right] \tag{3}$$

The next objective is to model the delay of ICSI in terms of the MOS process parameters. The behaviour of the ICSI circuit is the same as the cascaded pass transistor [19]. When the input of the the ICSI is high (V_{DD}), the NMOS transistor is ON and acts as a cascaded pass transistor to transfer the logic input to the output. Thus, during logic 1 transfer the charging of the capacitor is done through NMOS transistor. To simplify our analysis, we neglect the substrate bias effect at this point. Thus, when input changes from 0 to V_{DD} then transistors M3 and M4 are ON state and in saturation mode up to output voltage ηV_{DD} where η is $0 < \eta < 0.5$ and M3 in saturation and M4 in linear for output voltage ηV_{DD} to $0.5V_{DD}$.

$$\begin{aligned}\tau_{i1LH} &= \frac{2C_{load}}{k_n}\int_{V_{Tp}}^{\eta V_{DD}} \frac{dV}{(V_{DD} - V - V_{Tn})^2} \\ &= \frac{2C_{load}}{k_n}\left[\frac{1}{V_{DD}(1-\eta) - V_{Tn}} - \frac{1}{V_{DD} - |V_{Tp}| - V_{Tn}}\right]\end{aligned} \tag{4}$$

$$\begin{aligned}\tau_{i2LH} &= \frac{2C_{load}}{k_n}\int_{\eta V_{DD}}^{0.5V_{DD}} \frac{dV}{2(V_{DD} - V - V_{Tn})(V_{DD} - V) - (V_{DD} - V)^2} \\ &= \frac{C_{load}}{k_n V_{Tn}}\ln\left[\frac{V_{DD}(V_{DD} - \eta V_{DD} - 2V_{Tn})}{(V_{DD} - 4V_{Tn})(V_{DD} - \eta V_{DD})}\right]\end{aligned} \tag{5}$$

Here, V represents the output voltage of ICSI delay block, τ_{i1LH} is the time required to charge the load capacitor from V_{Tp} to ηV_{DD} and τ_{i2LH} is the time required to charge the load capacitor from ηV_{DD} to $0.5V_{DD}$. So total time (τ_{iLH}) required to charge load capacitor from V_{Tp} to $0.5V_{DD}$ is calculated as follows

$$\tau_{iLH} = \tau_{i1LH} + \tau_{i2LH} \tag{6}$$

In similar ways, during Logic 0, transfer high to low delay (τ_{iHL}) is calculated as

$$\tau_{iHL} = \tau_{i1HL} + \tau_{i2HL} \tag{7}$$

The total delay of the CICSI delay block $\tau_{LH}(tot)$ [or $\tau_{HL}(tot)$] is the sum of the delay of CMOS inverter τ_{pLH} [or τ_{pHL}] and delay of ICSI τ_{iLH} [or τ_{iHL}]. It is expressed as

$$\begin{aligned}\tau_{LH}(tot) &= \tau_{pLH} + \tau_{iLH} \\ \tau_{HL}(tot) &= \tau_{pHL} + \tau_{iHL}\end{aligned} \tag{8}$$

4. Result and Discussion

This section presents the simulated results that were carried out in Cadence using CMOS 90nm (GPDK 90nm) process of delay block and NOC, and its characterization for the proper functioning. In all the designs transistor sizing ratios (W/L=120nm/100nm) are used with a voltage supply of 1.2V.

Fig. 5 shows the plot of input and output voltage of CICSI. When the input is fed to the CICSI then the first stage gives the inverted output which is rail to rail. The output of the first stage is applied as input to the second stage (inverted current starved inverter). The output of the second stage is not rail to rail.

The V_{IL} and V_{IH} of the CICSI are 0.32V and 0.6V which is shown in Fig. 4. The output of the second stage inverted current starved inverter is less than 0.32 V and more than 0.6V. When this output is applied to the next stage of the CICSI, it is considered as perfect logic 0 and logic 1.

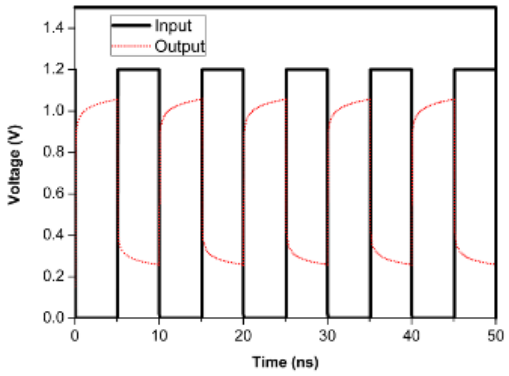

Fig. 5 Input and output voltage level of CICSI delay block

Fig. 6 shows the plot of the ring oscillator output with and without buffer. The ring oscillator output shows the output ranges from 0.25V to 1.05V which is not rail to rail. When the buffer is added at the output then the signal level is restored from 0 to 1.2V, as shown in Fig. 6.

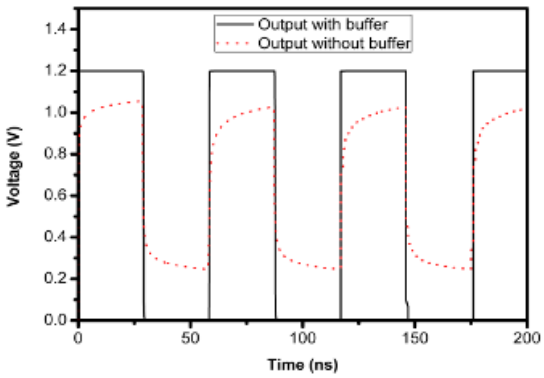

Fig. 6 Ring oscillator output with and without buffer

Fig. 7 shows the plot of transistor count versus the frequency variation for inverted inverter and CICSI. The graph shows for same number of transistors, CICSI produced less frequency compared to the inverted inverter. The variation shows the slope of CICSI is smaller compared to the inverted inverter. This shows that the proposed CICSI design has less variation in frequency (307MHz-68MHz) for the same number of transistors as compared to the inverted inverter (737MHz-145.9MHz).

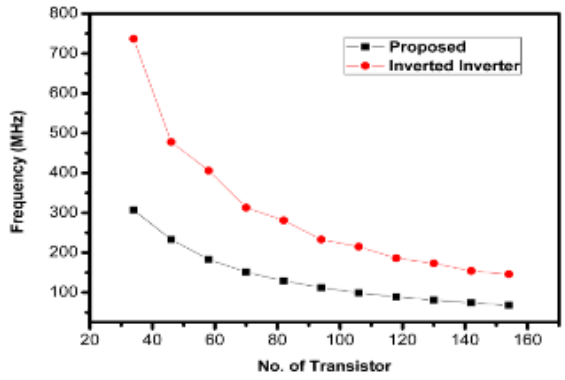

Fig. 7 Number of transistors vs frequency

Fig. 8 shows the plot temperature versus frequency of the CICSI. The CICSI shows the duty cycle is 50% for almost all ranges of temperature. The CICSI has tested from -40°C to 100°C, which shows minimal change (9.85MHz to 21.82MHz) in the frequency compared with the other oscillator in Table 1.

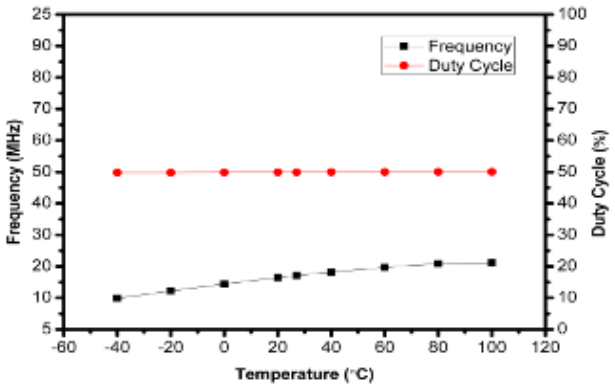

Fig. 8 Frequency vs temperature

Fig. 9 shows the output of the NOC block. The CICSI gives more delay compared to other delay circuits like inverted inverter [17]. The increased delay is helpful in saving number of transistors. In this work 2.59ns non overlapping clock period is achieved using 48 transistors in the delay chain.

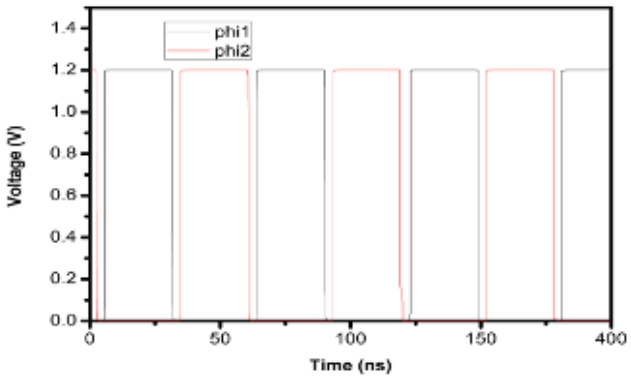

Fig. 9 NOC Delay

Fig. 10 shows the variation of the number stages of the oscillator with the frequency of oscillation obtained from simulation and analytical model. Based on Fig.10, the delay is calculated and the frequency is obtained.

Table 2 shows the comparison between an oscillator using CICSI block and the existing oscillator which shows the improved performance like reduced number of stages so that the power is reduced by nearly 50%. In Table 3 there is the comparison for different processes showing frequency of the oscillations for different oscillators. Table 4 shows that using a smaller number of transistors, a higher NOC period can be obtained with a CICSI block. The NOC and oscillators are an integral part of switch capacitor circuits used in the filter, EEG and ECG applications [20, 21]

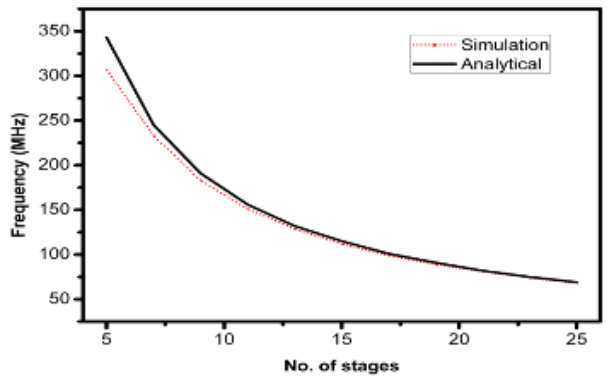

Fig. 10 Analytical & Simulated delay

Table 1 Comparison of frequencies of different oscillators for different temperatures

Temperature (°C)	Frequency of CICSI ring oscillator (MHz)	Frequency of 1CMOS inverter and 1inverted CMOS inverter (MHz)
-40	9.85	13.26
-20	12.22	14.82
0	14.44	15.98
20	16.45	16.97
27	17.08	17.15
40	18.20	17.92
60	19.69	18.24
80	20.87	18.64
100	21.82	18.88

Table 2 The important parameters of different oscillator blocks

	CICSI oscillator	1 CMOS inverter and 1 inverted CMOS inverter
Frequency	17.08 MHz	17.15 MHz
No. of Stages	101	313
Transistor Count	610	1256
Power	419.2µW	822.94 µW

Table 3 The comparison of the frequency of different oscillators for different processes

Process	Frequency of CICSI Ring oscillator (MHz)	Frequency of 1 CMOS inverter and 1 inverted CMOS inverter (MHz)
FS	4.59	5.63
SS	12.05	11.92
NN	17.08	17.15
FF	20.85	21.77
SF	31.56	26.81

Table 4 The comparison of NOC period of different delay blocks

No. of Transistors	T_{NOC} of CICSI block (ns)	T_{NOC} of 1CMOS inverter and 1inverted CMOS inverter (ns)
24	1.41	0.69
48	2.59	1.23
72	3.74	1.79
96	4.91	2.35
120	6.05	2.91

5. CONCLUSION

This paper presents a delay block which generates a higher delay with an equal number of MOS transistors as reported earlier. The delay expression for the proposed CICSI circuit is formulated. The delay block is used in a ring oscillator circuit and simulation results show its power and area efficiencies. Finally, a two phase non overlapping clock is generated using NOC generator which shows improvement in terms of area.

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REFERENCES

[1] P. E. Allen, E. Sanchez-Sinencio, *Switched Capacitor Circuits*, Van Nostrand Rienhold, 1984.
[2] Roubik Gregorian, Gabor C. Temes, *Analog MOS & Integrated Circuits for signal processing*, John WileySons, 1986.
[3] David A. Johns, Ken Martin, Analog Integrated Circuit Design, *John Wiley & Sons*, 1997.
[4] B. Razavi, "The Ring Oscillator [A Circuit for All Seasons]", in *IEEE Solid-State Circuits Magazine*, vol. 11, no. 4, pp. 10-81, Fall 2019.
[5] G. Jovanovic, M. Stojcev, "A Method for Improvement Stability of a CMOS Voltage Controlled Ring Oscillators", In Proceedings of the ICEST2007, Ohrid, June 2007, vol. 2, pp. 715–718.
[6] R. S. S. M. R. Krishna, G. L. Madhumati and A. K. Mal, "Design of substantial delay block using voltage scaled CMOS inverter and transmission gate blend", In Proceedings of the 2016 International Conference on Microelectronics, Computing and Communications (MicroCom), Durgapur, 2016, pp. 1–6,
[7] Meng-LiehSheu, Ta-Wei Lin, Wei-Hung Hsu, "Wide frequency range voltage controlled ring oscillator based on transmission gates", *ISCAS 2005*, vol. 3, pp. 2731–2734, May 2005.
[8] T.Jiang,J.Yin,P.Mak and R.P.C.Martins, "A 0.5-V 0.4-to-1.6-GHz 8-Phase Bootstrap Ring-VCO Using Inherent Non-Overlapping Clocks Achieving a 162.2-dBc/Hz FoM", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 2, pp. 157-161, Feb. 2019.
[9] F. Pepe and P. Andreani, "An Accurate Analysis of Phase Noise in CMOS Ring Oscillators", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 8, pp. 1292–1296, Aug. 2019.
[10] B.J. V. T. Ferreira and C. Galup-Montoro, "Ultra-low-voltage CMOS ring oscillators", *Electronics Letters*, vol. 55, no. 9, pp. 523–525, 2 5 2019.
[11] B. S. Salem, H. Zandevakili, A. Mahani and M. Saneei, "Fault-tolerant delay cell for ring oscillator application in 65 nm CMOS technology", *IET Circuits, Devices & Systems*, vol. 12, no. 3, pp. 233–241, 2018.
[12] B.X. Yu, Y. Fang and Z. Shi, "2.5 mW 2.73 GHz non-overlapping multi-phase clock generator with duty-cycle correction in 0.13 μm CMOS", *Electronics Letters*, vol. 52, no. 14, pp. 1261–1262, 2016.
[13] P. Angelov, M. Nielsen-Lönn and A. Alvandpour, "Ring-oscillator-based timing generator for ultralow-power applications", In Proceedings of the 2017 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Linkoping, pp. 1–4, 2017.
[14] B.Nowacki, N. Paulino and J. Goes, "A simple 1 GHz non-overlapping two-phase clock generators for SC circuits", In Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013, Gdynia, pp. 174–178.
[15] B.L. Minati*et al*., "Current-Starved Cross-Coupled CMOS Inverter Rings as Versatile Generators of Chaotic and Neural-Like Dynamics Over Multiple Frequency Decades", *IEEE Access*, vol. 7, pp. 54638–54657, 2019.
[16] B.C. Q. Liu, Y. Cao and C. H. Chang, "ACRO-PUF: A Low-power, Reliable and Aging-Resilient Current Starved Inverter-Based Ring Oscillator Physical Unclonable Function", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 12, pp. 3138–3149, Dec. 2017.
[17] A.K. Mal, R. Thodani,"Non overlapping clock (NOC) generator for low frequency switched capacitor circuits", In Proceedings of the students Technology symposium 2011 IEEE, pp. 226–231.
[18] A. K. Mal and R. Todani, "Non Overlapping Clock generator for switched capacitor circuits in Bio-Medical applications", In Proceedings of the 2011 International Conference on Signal Processing, Communication, Computing and Networking Technologies, Thuckafay, 2011, pp. 238–243.
[19] S.M. Kang, Y. Lebebici, CMOS Digital Integrated Circuits,Analysis and Design, *McGraw-Hili Publishing Company LImIted*, 2003.
[20] N. N. Singh and P. P. Bansod, "Switched-capacitor filter design for ECG application using 180nm CMOS technology", IN Proceedings of the 2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE), Bhopal, 2017, pp. 439–443.
[21] A. Karimi-Bidhendi et al., "CMOS Ultralow Power Brain Signal Acquisition Front-Ends: Design and Human Testing" *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 5, pp. 1111–1122, 2017.