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ABSTRACT

Off-state leakage current of AlGaN/GaN high-electron-mobility transistors (HEMTs) with implant and mesa isolation was studied. Comparison of isolated pad structures with HEMTs shows that isolation leakage flowing through contact pads is the major leakage source in the studied GaN-based HEMTs whose gate finger is connected to an Ohmic contact pad. Then, circular metal-oxide-semiconductor field-effect-transistor devices were used to identify this isolation leakage path as surface isolation leakage at the SiN/nitride interface rather than bulk leakage in the buffer layer or implanted region. The temperature-dependent measurement shows that the two-dimensional variable range hopping mechanism dominates both the implant and mesa isolation leakage current. Mesa isolation results in a larger hopping probability and isolation leakage current than implant isolation. The isolation leakage current through gate and drain contact pads results in a non-zero switch of gate current in rectangular devices with either a Schottky gate or a metal-oxide-semiconductor gate, which is not observed in circular devices. Gate voltage for the switch of gate leakage current is linearly correlated with drain bias voltage, and the slope of the linear model represents the influence of drain bias on gate leakage current. This empirical model is independent of the fabrication process, provided that the same layout is used. With an increase in the source–drain distance from 4 μm to 10 μm, the ratio of gate–drain isolation resistance to gate–source isolation resistance increases from 1.38 to 2.33, leading to a decrease in the slope of empirical lines from 0.42 to 0.30.

Off-state leakage current in semiconductor devices is of vital importance due to the major influence on power consumption, reliability, and long-term failure. Because of the wide bandgap semiconductor materials and two-dimensional electron gases (2DEG) formed at the heterostructure interface, GaN-based high-electron-mobility transistors (HEMTs) are promising candidates for high-frequency power amplifiers,[1,2] high-speed power switches,[3] and anti-radiation digital circuits applications.[4] The off-state leakage current of GaN-based HEMTs plays a critical role in device performance such as noise figure,[5] power added efficiency,[6] and sub-threshold characteristics,[7] which is obviously paid much attention to.

Among several potential leakage sources, vertical gate leakage current in GaN-based HEMTs flowing through the barrier layer has been widely studied in previous reports.[8–12] This leakage current may be dominated by different conduction mechanisms such as temperature-dependent Poole–Frenkel (PF) emission current, Fowler–Nordheim (FN) tunneling current under a high electric field, and trap-assisted tunneling current. Surface leakage current in the gate–drain access region is another critical leakage path, which has a major effect on current collapse. It was extracted by using a dual-gate or gate-guarded test structure,[13,14] showing the conduction mechanism via PF emission,[14] variable-range hopping (VRH),[15] or space charge-limited current.[16] In addition, device isolation is also highlighted for Si technology and integrated circuits.[17] With the suppression of other leakage paths,[7,14,15,18,19] the isolation leakage in GaN technology cannot be neglected, which, therefore, is desirable to be further investigated. The mesa isolation of

GaN-based HEMTs has been analyzed with the help of a ridge-furrow structure,[20] and the improvement was demonstrated by filling dielectrics.[21] However, previous reports were focused on the mesa edge or sidewalls for the process with mesa etching isolation.

In this work, leakage current flowing through the whole isolation area was studied, which led to the isolation leakage between contact pads. To identify the major leakage current path among several possible sources, devices with a gate finger connected to Ohmic contact pads were studied and compared with isolated contact pads. Surface isolation leakage current was found to dominate the off-state leakage current of the studied GaN-based HEMTs; even a small leakage current of 10^{-5} mA/mm was found when implant isolation was used. The isolation leakage current is dependent on both gate and drain bias voltage, causing a non-zero switch of gate current between negative and positive signs. The gate voltage at the gate current switch point has a linear correlation with drain voltage, giving an empirical model varying with the device layout. The temperature-dependent measurement with isolated structures shows the presence of a VRH conduction mechanism for both implant isolation and mesa isolation.

Figure 1 shows the schematic layout and cross section of rectangular AlGaN/GaN HEMTs used in this work, including several potential leakage current sources. Metal-oxide-semiconductor field-effect-transistors (MOS-FETs) were also studied to investigate the fabrication process and layout influence on isolation leakage current. AlGaN/GaN epitaxial layers were grown on SiC substrates by metal-organic chemical vapor deposition, consisting of a 180 nm AlN nucleation layer, a 1.3 μm unintentionally doped GaN layer, and a 21 nm $Al_{0.22}Ga_{0.78}N$ barrier layer from bottom to top. The Hall measurement at room temperature shows a sheet carrier density of 9.85×10^{12} cm^{-2}, a mobility of 2304 cm^2/V s, and a sheet resistance of 275 Ω/□.

The Ohmic contacts were fabricated by e-beam evaporation of Ti/Al/Ni/Au (stack thickness ~260 nm), the lift-off process, and rapid thermal annealing at 840 °C in N_2 for 30 s. Two types of device isolation processes were studied in this work. Mesa isolation was achieved using Cl_2 plasma etch with a depth of 125 nm, while nitrogen ion implantation was carried out with an energy of 150 keV and a dose of 5×10^{14} cm^{-2}. Surface passivation of 120 nm SiN was grown by plasma-enhanced chemical vapor deposition. Then, the SiN layer within the T-shaped gate foot area was removed by inductively coupled plasma etch, defining a gate length of 0.25 μm and a gate–source distance of 1 μm. For MOS-FETs, the AlGaN barrier layer within the gate area was fully etched using Cl_2/BCl_3 plasma, followed by atomic layer deposition of 20 nm Al_2O_3. Finally, gate metallization was achieved by e-beam evaporation of 160 nm Ni/Au/Ni stack and the lift-off process. Note that the gate finger in Fig. 1(a) is connected to an Ohmic contact pad for the probe measurement. One reason is that Ohmic contacts fabricated on the native surface have good adhesion, which can withstand large probe pressure or high temperature during the measurement. In addition, the Ohmic metal stack is thicker than gate metal, which will provide lower probe contact resistance and enhance the speed.

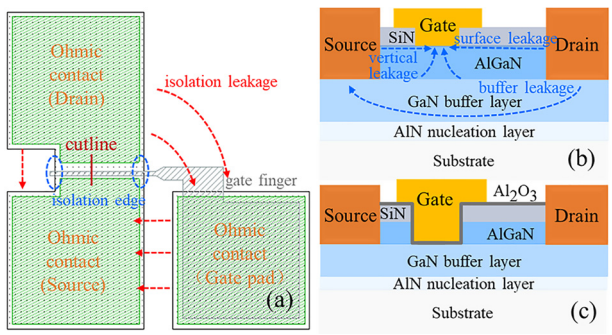

FIG. 1. (a) Top view layout of rectangular devices. (b) and (c) show the schematic cross section of GaN-based HEMTs and metal-oxide-semiconductor field-effect-transistors (MOS-FETs) used in this work. Dashed arrows and circles denote the possible off-state leakage paths.

The transfer sweep results of GaN-based HEMTs with the implant isolation and source–drain distance (L_{sd}) of 4 μm are shown in Fig. 2(a). With an increase in drain voltage (V_d) from 0.1 V to 15 V, there is an increase in off-state leakage current by one order of magnitude, causing an increase in the sub-threshold slope and a negative shift of threshold voltage. Note that the switch point of gate current from the negative sign to the positive one is not at 0 V, which is caused by the drain bias influence on gate current. The gate voltage (V_g) at the switch point is defined as V_{g0}, showing a linear dependence on drain bias. The non-zero switch of gate current is also observed for the output measurement with a gate bias step (V_{step}) of 1 V, as shown in Fig. 2(b).

Analysis of isolated Ohmic contact pads with a HEMT-like layout shows a leakage current of 10^{-5}–10^{-4} mA/mm and a non-zero switch, as shown in Fig. 3(a). Figure 3(b) shows the gate bias vs drain bias when gate current reaches zero for three terminal contact pads with and without the active HEMT region. Comparing V_{g0}–V_d and V_{d0}–V_g obtained from transfer sweep and output sweep in Fig. 2, we find that all pairs of voltage follow the same linear relationship. The data derived from Fig. 3(a) also exhibit a similar linear trend. Apparently, the non-zero switch of gate current is independent of the active region, and isolation leakage current between contact pads makes major contribution to the off-state leakage current of GaN-based HEMTs before the gate turns on. Therefore, the non-zero switch phenomenon of HEMTs in this work should be attributed to the isolation leakage current rather than vertical leakage and surface leakage in the access region. However, this cannot directly distinguish between the leakage path on the surface of the isolated area and that in the bulk of epitaxy layers.

MOS-FETs with a circular layout as shown in Fig. 4 were used to distinguish surface leakage and bulk leakage current paths. The drain contact pad is surrounded by the gate finger and source contact,

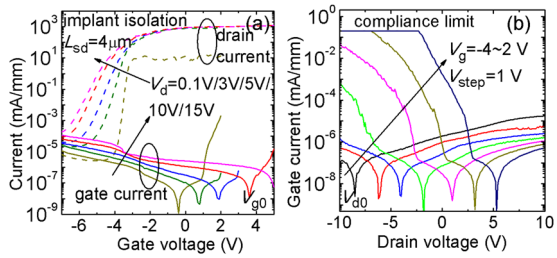

FIG. 2. (a) Transfer sweeps and gate current curves of AlGaN/GaN HEMTs with different drain bias voltages. (b) Gate current vs drain voltage curves with different gate bias voltages.

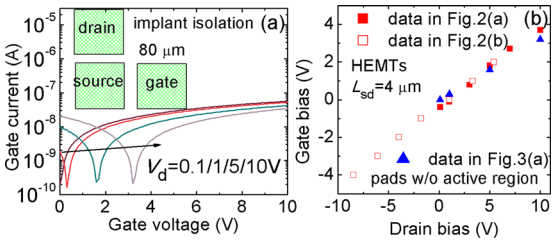

FIG. 3. (a) "Gate" current vs voltage curves with different "drain" bias voltages for the three-terminal isolated pad structure as shown in the inset. (b) Gate bias vs drain bias at the current switch points for pads with and without the active HEMT region.

blocking the surface isolation leakage current flowing between the gate and drain contact pads. The use of the Al_2O_3 gate insulator suppresses the vertical gate leakage, allowing a larger positive gate swing to observe the gate bias behavior. Mesa isolation causes higher leakage current than implant isolation in rectangular devices (not shown), and circular devices have a smaller off-state leakage current than the rectangular ones, as seen in Fig. 4(b). However, the key difference is that the rectangular devices show a drain bias-dependent current switch, whereas the circular devices show no dependence of the switch. If there were a leakage path through the bulk under the circular gate, a drain voltage dependence of the leakage current would be observed. This is clear evidence that the leakage path causing the switch in the sign of the gate leakage is associated with leakage at the SiN/nitride interface in the isolated region and not due to source to drain leakage through the bulk.

The above analysis suggests that gate leakage curves of rectangular HEMTs and MOS-FETs are highly dependent on not only gate voltage but also drain voltage. This is because the gate leakage current includes isolation leakage from source and drain contact pads. An empirical model of linear plot fits well with the correlation of gate voltage with drain voltage at gate current switch points, as shown in Fig. 5(a) for implant isolated HEMTs. The intercept is close to the origin, and the slope represents the influence of drain voltage on gate leakage current. With an increase in L_{sd} from 4 μm to 10 μm, the pad layout becomes more asymmetric and the drain voltage influence on gate leakage current is reduced. Therefore, there is a decrease in the slope of linear curves from 0.42 to 0.30. For the asymmetric devices with a high drain bias, the contribution of gate–drain pad isolation leakage to the total gate leakage current tends to decrease, causing the

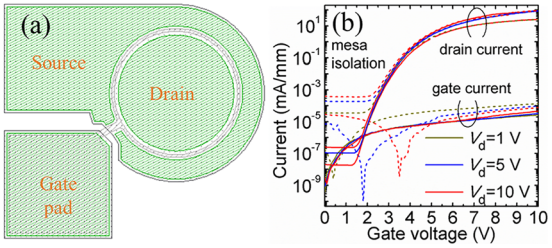

FIG. 4. (a) Layout of circular devices. (b) Gate and drain current curves of mesa isolated MOS-FETs with the circular (solid lines) and rectangular (dashed lines) layout.

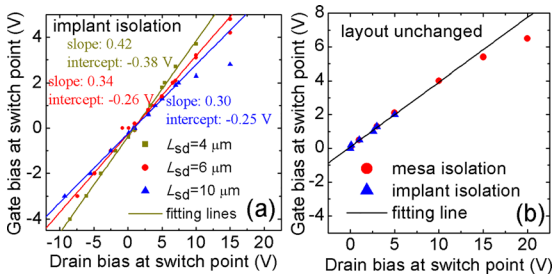

FIG. 5. Influence of (a) layout and (b) fabrication process on the gate voltage vs drain voltage at the switch points of gate current for rectangular GaN-based devices.

deviation of experimental data from fitting lines. Devices with mesa isolation show a similar empirical model when using the same layout, as shown in Fig. 5(b). This indicates that the empirical linear model for isolation leakage current developed in this work is independent of the fabrication process.

To determine the conduction mechanism of isolation leakage, the temperature-dependent current–voltage (I–V) measurement was carried out with an isolation structure, as shown in Fig. 6 for the implant isolation case. With an increase in temperature (T) from 25 °C to 200 °C, there is an accelerated increase in isolation leakage by over two orders of magnitudes. The isolation leakage curves obey Ohm's law at low fields. This is consistent with variable range hopping (VRH) conduction, which describes the carrier transport in the disordered semiconductor or amorphous solid by hopping through localized states (hopping sites).[22–24] The logarithmic conductance ln(G) of the isolation structure calculated using Ohmic fitting is proportional to $T^{-1/3}$ for both implant and mesa isolation processes, as shown in Fig. 7. This indicates that the isolation leakage arises from two-dimensional (2D) VRH assisted by the SiN/nitride interface electronic state, whose temperature-dependent conductivity [$\sigma(T)$] is given by the following formula:[15]

$$\sigma(T) \propto \exp\left[-(1/T)^{1/3}\right]. \quad (1)$$

The VRH hopping probability (P) depends on the range between two sites expressed as follows:[24]

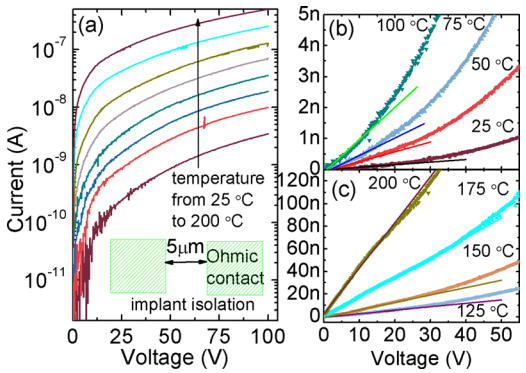

FIG. 6. (a) Temperature-dependent I–V curves of isolated Ohmic contacts with a 5 μm gap distance as shown in the inset. (b) and (c) show the Ohmic fitting at low voltage.

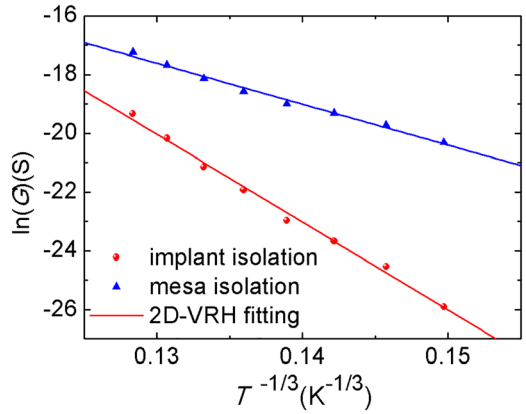

FIG. 7. Conductance of isolated Ohmic contacts and the 2D-VRH fitting for implant and mesa isolation processes.

$$P \propto \exp\left(-2\alpha R - \frac{W}{kT}\right), \tag{2}$$

where α^{-1} is the attenuation length for a hydrogen-like localized wave-function, R is the spatial separation, and W is the energy separation. Therefore, the difference in the slope of VRH fitting lines between two isolation processes results from the energy separation change. A reasonable explanation is that mesa etch causes some defects on the GaN surface, which will decrease both the spatial and energy hopping separation, leading to a larger leakage current with mesa isolation than that with implant isolation.

With the VRH mechanism, the empirical linear models in Fig. 5 can be explained. Because VRH leakage current is proportional to voltage at low fields, the isolation between the gate and source/drain pads can be equivalent to resistors with resistances of r_{gs} and r_{gd}. At the gate current switch point, the following equation holds:

$$\frac{V_g}{r_{gs}} = \frac{V_d - V_g}{r_{gd}}, \tag{3}$$

which gives the relationship of resistance ratio (r_{gd}/r_{gs}) with the slope (S) of empirical model as follows:

$$r_{gd}/r_{gs} = (1 - S)/S. \tag{4}$$

Therefore, the isolation resistance ratios are estimated to be 1.38, 1.94, and 2.33 for HEMTs with L_{sd} values of 4 μm, 6 μm, and 10 μm, respectively. The isolation resistance ratio gives quantitative evaluation of isolation leakage, which is Ohmic and geometry dependent but independent of the fabrication process.

In conclusion, isolation leakage current and the mechanism in AlGaN/GaN HEMTs were studied in this paper. Isolation leakage through contact pads dominates the off-state leakage current of rectangular-layout devices, leading to a non-zero switch point of I_g–V_g and I_g–V_d curves. The gate voltage at the gate current switch point shows a linear correlation with drain voltage, revealing an empirical model independent of the fabrication process. The temperature-dependent I–V measurement with isolated structures indicates that the 2D-VRH mechanism dominates both the implant and mesa isolation leakage. HEMT processes using dielectric isolated gate pads may misinterpret the off-state leakage current as a bulk leakage. Here, it is shown that this leakage is in fact due to pad-to-pad surface leakage in the isolated region.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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