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Improvement of Electron Transport Property and On-Resistance in Normally-Off Al_2O_3/AlGaN/GaN MOS-HEMTs Using Post-Etch Surface Treatment

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***Abstract*—Post-etch surface treatment technique was developed for normally-off recess-gate Al_2O_3/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs). By removing the residues and smoothing surface morphology after plasma etch, the diffusion-controlled interface oxidation (DCIO) and wet etch in MOS-HEMTs leads to a decrease in interface traps from 1.04×10^{12} cm^{-2} to 6.3×10^{11} cm^{-2} with filling voltage of 12 V. Field-effect mobility extracted in the linear region is 48 cm^2/V·s for MOS-HEMTs with an optimized post-etch surface treatment process, 33% larger than the case with conventional chemical clean process. Due to the increased electron mobility and decreased sheet resistance beneath the gate by over 30%, normally-off MOS-HEMTs with DCIO and wet etch exhibit a remarkable increase in output current by about 29% and an increase in peak transconductance from 35 mS/mm to 41 mS/mm. The optimized post-etch surface treatment method also enhances blocking voltage from 120 V to 230 V, by suppressing the leakage current resulting from gate soft breakdown. Dynamic characterization shows that the normalized on-resistance is increased by double with drain stress up to 80 V, and various post-etch surface treatment process has little effect on current collapse. Two types of threshold voltage shifts caused by interface trapping and border trapping are observed in the normally-off MOS-HEMTs, which keeps stable with an increase in temperature up to 125 °C.**

***Index Terms*—AlGaN/GaN, interfacial engineering, metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs), normally-off, post-etch surface treatment.**

I. Introduction

OWING to the superior properties such as high power density, high efficiency, low on-resistance, and compact size, GaN-based high-electron-mobility transistors (HEMTs) are promising candidates for high-speed power electronics. [1]-[3] Conventional GaN-based HEMTs are normally-on devices due to the very strong polarization effect. [4] Normally-off operation, however, is preferred for practical circuits, which possess inherent advantages including low power consumption, enhanced system safety, and simple circuit configuration. [2] Among various approaches to realizing GaN-based normally-off devices, metal-oxide-semiconductor HEMTs (MOS-HEMTs) with recessed gate have attracted increasing interest [5]-[7] because of the low leakage current, large gate swing, and high breakdown voltage.

Even though with outstanding features, GaN-based MOS-HEMTs suffer from a poor interface between gate dielectric and polarized nitride layers, which can cause serious device degradation or reliability problems, such as threshold voltage (V_{th}) instability and electron scattering. [8]-[10] It is commonly thought that the poor-quality native oxide layer makes a major contribution to the high-density interface charges, and there are two types of solutions to improving the interface quality. The one includes nitridation plasma pre-treatment or wet etching using acid solutions to effectively remove the native oxide layer. [11]-[14] The other one is surface pre-passivation of nitride materials with oxidation plasma or alkaline solutions. [15]-[21] The interface issues will become even worse for the gate-recess devices, where a large amount of surface damage and residues (e. g. photoresist, $AlCl_x$, and $GaCl_x$) may be left after dry etch process. [6] Therefore, interface engineering is much more critical to GaN-based gate-recess MOS-HEMTs.

In this work, normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs were realized by using fully recessed gate and post-etch surface treatment. The post-etch surface treatment process includes wet clean and surface oxidation after dry etch, which was demonstrated to improve the nitride surface morphology and reduce the impact of etch induced surface damage. The optimized post-etch surface treatment method consists of chemical clean in $NH_3{\cdot}H_2O$ (1:6) at 55 °C, pre-deposition of a diffusion-control interlayer, diffusion-controlled interface oxidation (DCIO) treatment, [21] and wet etch in 1:5 HCl solution. Compared to the conventional surface oxidation and wet etch method, the improved oxidation process in this work is controlled by the very slow oxidant diffusion through Al_2O_3 interlayer, which is beneficial to the complete reaction of oxidant with etched nitride surface.

DCIO treatment followed by wet etch demonstrated better surface morphology than the conventional method, which was then adopted for device fabrication. Thanks to the improved

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surface morphology and channel transport property, the post-etch surface treatment by DCIO treatment and wet etch results in a significant increase in output current, a decrease in on-state resistance, reduced voltage hysteresis, suppressed off-state leakage current, and enhanced breakdown property.

II. Post-Etch Surface Treatment and Fabrication of Recess-Gate GaN-Based MOS-HEMTs

AlGaN/GaN epitaxial layers used in this work were grown on 3 inch sapphire substrates by metal-organic chemical vapor deposition, consisting of 180 nm AlN nuclear layer, 0.8 μm carbon doped GaN buffer layer, 1 μm unintentionally doped (UID) GaN channel layer, 0.6 nm AlN interlayer, 21.6 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and 2.9 nm GaN cap layer from bottom to top, as shown in Fig. 1 (a). Hall measurement at room temperature shows a sheet carrier density of 9.78×10^{12} cm^{-2}, a mobility of 1675 $cm^2/V\cdot s$, and a sheet resistance of 381 Ω/□.

The source and drain Ohmic contacts were fabricated with e-beam evaporation of Ti/Al/Ni/Au, lift-off process, and rapid thermal annealing at 880 °C in N_2 for 50 s. Ohmic contact resistance about 50 $m\Omega\cdot mm^2$ was derived using transmission line method. Then mesa isolation of active areas was carried out with inductively coupled plasma (ICP) etch in Cl_2/BCl_3 mixed gas, followed by 100 nm SiN passivation with plasma enhanced chemical vapor deposition (PECVD). Before gate recess etch of nitride layer in mixed BCl_3/Cl_2 plasma, the gate foot area was defined by removing SiN layer with ICP etch in CF_4 plasma. The gate recess etch is time-controlled rather than selective process. To optimize the etch recipe and time, some pieces of un-passivated AlGaN/GaN epilayer samples were loaded into the ICP system to be etched with recess mask. Fig. 1 (b) and (c) give the atomic force microscopy (AFM) surface morphology and step profile across the gate recess for one sample with recess depth of 25 nm. Step profile gives an etched recess about 1 μm wide, which corresponds to the designed foot length of T-shaped gate. During device fabrication, however, process variation will affect the precise control of etch depth, so in-process measurement of open-gate structures developed in Ref. [22] was adopted to re-check the end-up point.

Interface quality between gate oxide and etched nitride layer is critical to GaN-based MOS-HEMTs, so the surface treatment after gate recess etch is of vital importance. The post-etch surface treatment process was optimized among four different solutions, as shown in Table I. Following organic solutions clean, soak in $NH_3\cdot H_2O$ (1:6) at 55 °C for 5 min was used to clean the surface contaminant and residual photoresist. Wet etch in 1:5 HCl solution for 3 min was used to remove the native oxide layer prior to the *in situ* pre-treatment and gate oxide deposition in atomic layer deposition (ALD) system. Process C and D present two different oxidation and wet etch methods, where the O_2/N_2 plasma assisted oxidation was carried out in ALD system for 30 min with sample temperature at 300 °C.

Different from the conventional oxidation and wet etch method as process C, 1 nm Al_2O_3 was pre-deposited before the plasma assisted oxidation for process D. During the following oxidation step, the time-dependent thickness of oxide layer

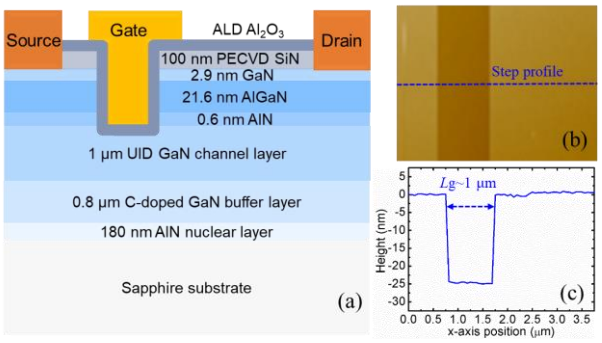

Fig. 1 (a) Schematic cross section of recess-gate Al_2O_3/AlGaN/GaN MOS-HEMTs fabricated in this work. (b) and (c) give the AFM surface morphology and step profile of Cl_2/BCl_3-etched AlGaN/GaN sample using the gate recess mask.

Table I. Post-etch surface treatment process prior to gate dielectric deposition for Al_2O_3/AlGaN/GaN MOS-HEMTs

Process sequences and RMS	**Optimization of post-etch surface treatment**			
	Process A	***Process B***	***Process C***	***Process D***
1:6 $NH_3\cdot H_2O$	YES	YES	YES	YES
Al_2O_3 pre-deposition	NO	NO	NO	YES
Plasma assited oxidation	NO	NO	YES	YES
Wet etch with 1:5 HCl	NO	YES	YES	YES
In situ pre-treatment	YES	YES	YES	YES
RMS within 6.5×6.5 μm²	0.59 nm	0.75 nm	0.50 nm	0.30 nm

should be determined by two issues: the diffusion of oxidant through Al_2O_3 layer and the chemical reaction at Al_2O_3/GaN interface. [21], [23] Because of the low oxygen permeability of Al_2O_3, [21], [24], [25] the oxidant diffusion is much slower than oxidation reaction process, which is then called as diffusion-controlled interface oxidation and will be beneficial to the complete reaction of oxidant with etched nitride surface. Noted that the oxide layer formed during diffusion-controlled reaction was defective due to the damaged surface and residues after ICP etch, which was then removed by soak in HF solution, with damage-free GaN surface left. Fig. 2 gives the comparison of AFM surface morphology for samples with different post-etch surface treatment process. Large number of nano particles (white dots) are observed on etched surface even after wet clean in organic and $NH_3\cdot H_2O$ solutions, resulting in a root-mean-square roughness (RMS) of 0.59 nm within the area of 6.5×6.5 μm^2. The following treatment in HF solution leads to an increase in RMS by 0.16 nm, because it may cause defect corrosion after completely removing the surface oxide layer. For the samples with process C and D, RMS of 0.50 nm and 0.30 nm were obtained, respectively.

Apparently, surface treatment with process D demonstrated the optimized surface morphology, which is, therefore, adopted for the fabrication of high performance GaN-based MOS-HEMTs. Devices without oxidation treatment and wet etch (process A) were also prepared for comparison. MOS-HEMTs with process B or C were not fabricated in this work, so there is a lack of discussion on their electrical performance. After the post-etch surface treatment and *in situ* NH_3/N_2 plasma pre-

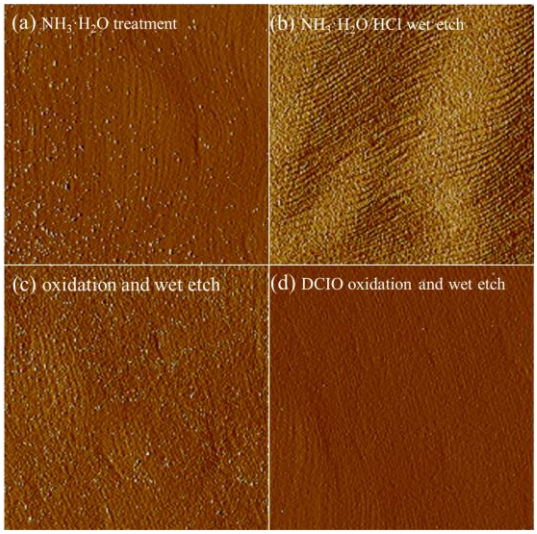

Fig. 2 AFM surface morphology (area: 6.5×6.5 μm^2) of Cl_2/BCl_3-etched AlGaN/GaN samples with different post-etch surface treatment process, showing that the DCIO oxidation followed by wet etch using HCl solution resulting in the optimized surface morphology.

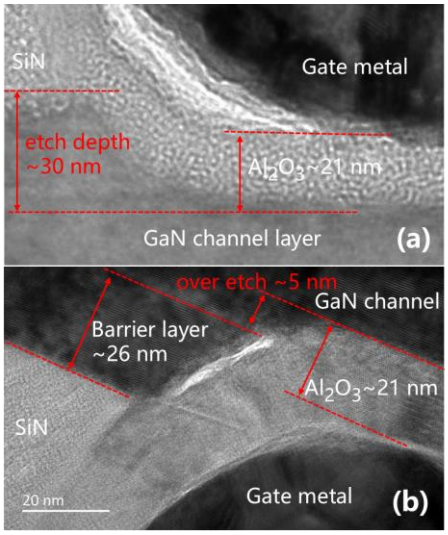

Fig. 3 Cross-sectional TEM views of recess-gate Al_2O_3/AlGaN/GaN MOS-HEMTs with post-etch surface treatment using (a) process A and (b) process D.

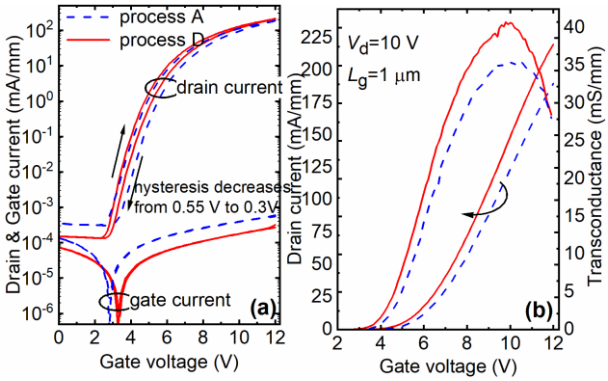

Fig. 4 Influence of post-etch surface treatment process on the transfer characteristics of normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs in (a) semi-logarithmic and (b) linear coordinate systems.

treatment, 20 nm Al_2O_3 was deposited in ALD, followed by fabrication of Ni/Au/Ni gate metallization using lift-off process. Finally, post-metallization annealing in O_2 at 450 ℃ for 5 min was carried out to further improve the interface quality.

III. Characterization Results and Discussion

The plasma etch rate of nitride might be dependent on the materials and process variation, so the recess-etch depth of as-fabricated MOS-HEMTs was confirmed using transmission electron microscope (TEM), as shown in Fig. 3. The total thickness of GaN/AlGaN/AlN stack layers is about 26 nm, very close to the result of 25.1 nm determined by optical method. The time-controlled BCl_3/Cl_2 plasma etch leads to an extra depth of 4 nm into GaN channel layer for the devices using process A surface treatment, while DCIO treatment and wet etch causes a deeper recess by 1 nm. The gate dielectric thickness in both devices is determined to be 21 nm.

Fig. 4 gives the impact of post-etch surface treatment process on the transfer characteristics with drain voltage (V_d) of 10V for Al_2O_3/AlGaN/GaN recess-gate MOS-HEMTs with gate length (L_g) of 1 μm, gate width (W_g) of 50 μm, gate-source distance (L_{gs}) of 2.5 μm, and gate-drain distance (L_{gd}) of 6.5 μm. The threshold voltage defined at drain current of 10 μ A/mm are 3.1 V and 2.8 V for devices with post-etch surface treatment process A and D, respectively. DCIO treatment and wet etch after ICP etch leads to an increase in peak transconductance from 35 mS/mm to 41 mS/mm and a decrease in hysteresis voltage from 0.55 V to 0.30 V with filling gate voltage (V_g) up to 12 V. The interface trap density (ΔN_{it}) was then calculated by using the following formula, $\Delta N_{it}=\Delta V_{th} \cdot C_{ox}/q$, where q is the magnitude of electron charge. DCIO treatment following by wet etch results in an increase in the capacitance of gate oxide (C_{ox}) in MOS-HEMTs from 303 nF/cm^2 to 336 nF/cm^2. With filling voltage of 12 V, the interface trap density for MOS-HEMTs with process A and D are estimated to be 1.04×10^{12} cm^{-2} and 6.3×10^{11} cm^{-2}, respectively.

The off-state leakage current at the order of magnitude of 10^{-4} mA/mm is similar to that of a test structure for isolation leakage current, so the leakage current of MOS-HEMTs in this work is dominated by isolation leakage flow between adjacent gate and source/drain contact pads. Note that the switch of gate leakage current (I_g) from negative sign to positive one is not at zero gate voltage, which is almost independent of trapping and de-trapping process. This is due to the drain bias influence on the gate leakage current. [26] With gate biased below the switch voltage, the contribution of isolation leakage from drain pad to gate pad results in the total gate current with negative sign. Further investigation shows that the switch point for gate leakage current is linearly dependent on drain bias, with a slope about 0.31. (not shown here) In contrast, a non-zero switch of gate current is not observed in circular-layout devices, where the drain contact is surrounded by gate finger and source contact, blocking the isolation leakage flow between gate and drain contact pads.

The output characteristics of normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs are shown in Fig. 5. To evaluate the output current capability of recess-gate MOS-HEMTs, gate voltage (V_g) steps up to 16 V, even interface and border trapping will

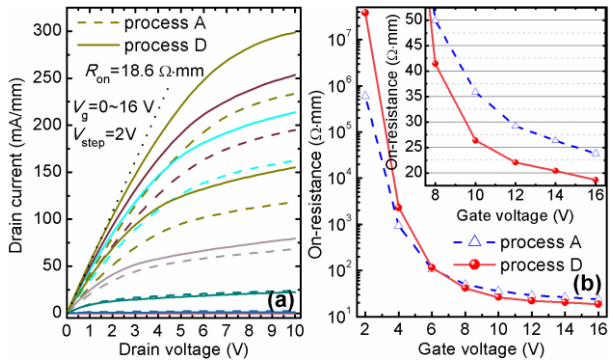

Fig. 5 (a) Family output curves and (b) on-resistance as a function of gate voltage for the normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs with two different post-etching surface treatment process. (Inset) The enlarged view of gate voltage dependent on-resistance in linear coordinate system.

cause V_{th} instability with an increase in gate bias stress. MOS-HEMTs with DCIO treatment and wet etch exhibit output current of 300 mA/mm, about 29% higher than the case with process A. The on-resistance (R_{on}) was derived from the linear region in output curves. DCIO treatment and wet etch causes a decrease in R_{on} by over 20% with V_g above 10 V. With V_g below 6 V, the smaller R_{on} for devices with process A is due to the larger leakage current.

It is obvious that the improved output properties by using DCIO treatment and wet etch are owing to the improvement of MOS-HEMTs channel, which is further investigated with gated transmission line model (GTLM). During the output curve sweeps with an increase in gate voltage, the step-by-step border trapping effect will keep depleting the electron in channel, which may affect the precise derivation of channel resistance. To avoid the step-by-step border trapping, GTLM devices were programmed with a high filling voltage of 15 V before output sweeps. The GTLM devices after program at 15 V have threshold voltage about 2.25 V larger than the MOS-HEMTs used for transfer and output sweeps in Fig. 4, and there exists small variation among devices with different gate length. For a fair comparison between these two cases, V_g-V_{th} is used as the gate reference voltage instead of V_g. Fig. 6 gives the GTLM fitting demonstration with V_g-V_{th}=5.2 V and extracted sheet resistance beneath gate area as a function of V_g-V_{th}. With an increase in gate voltage, the larger energy band bending at semiconductor surface will result in an exponential increase in electron density, causing a sharp decrease in sheet resistance by several orders of magnitude. Similar to the resistance analysis in Fig. 5, post-etch DCIO treatment and wet etch leads to a significant decrease in sheet resistance of MOS-HEMTs channel, which is from 26529 Ω/sq to 16667 Ω/sq with V_g-V_{th}=5.2 V. A certain electron density is determined by the same surface potential and material nature property, so the decrease in sheet resistance should be attributed to an increase in electron mobility.

The field-effect mobility (μ_{FE}) of MOS-HEMTs channel was studied with long-gate devices, where the influence of series resistance on transconductance was negligible. Fig. 7 gives the transfer sweep in linear region and extracted μ_{FE} as a function of gate voltage. DCIO treatment and wet etch leads to an increase in peak field-effect mobility of normally-off MOS-HEMTs

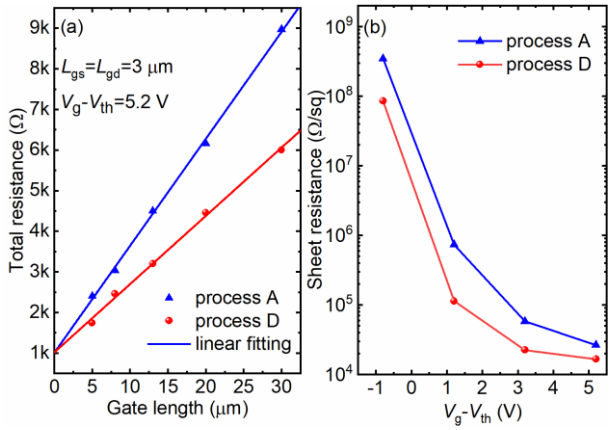

Fig. 6 Conductivity analysis of fully recessed Al_2O_3/AlGaN/GaN MOS-HEMTs channel using GTLM structures: (a) total resistance as a function of gate length and the GTLM fitting curves; (b) dependence of sheet resistance beneath gate area on gate voltage.

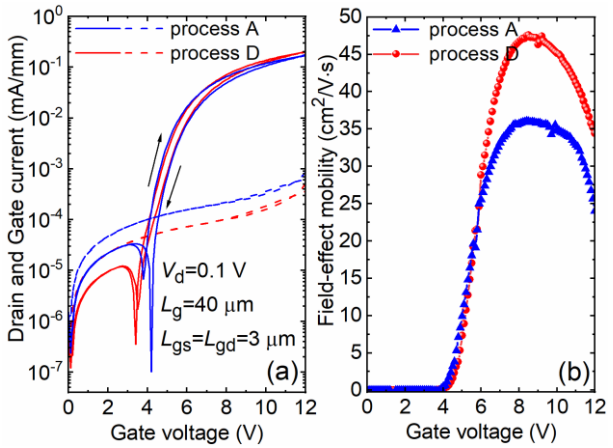

Fig. 7 (a) Transfer characteristics of Al_2O_3/AlGaN/GaN MOS-HEMTs biased at linear region and (b) field-effect mobility as a function of gate voltage for the cases with different post-etch surface treatment process.

from 36 cm²/V·s to 48 cm²/V·s. The increase in mobility by 33% makes contribution to the remarkable decrease in channel resistance and increase in output current. The leakage current with drain biased in the linear region is quite different from the results in Fig. 4 (a). Due to the very small influence of drain bias, gate leakage current is highly dependent on gate voltage and shows sign switch at zero point. In contrast, off-state drain leakage current keeps negative before switch point, which is attributed to the isolation leakage flow from drain contact pad to gate contact pad.

OFF-state blocking voltage as well as gate breakdown is also among the importance figure of merits for power electronics, which is then characterized as shown in Fig. 8. Neither device exhibits gate failure until the forward bias is above 16 V, indicating the excellent electrical insulating property of ALD-grown Al_2O_3. The device with process D shows a reduction of leakage current before gate oxide breakdown, which can be related to the suppression of isolation leakage. For the three-terminal breakdown sweep as shown in Fig. 8 (b), the leakage current shows different behavior with drain varying. With drain biased at moderate voltage, isolation leakage between contact pads dominates the off-state gate and drain current, and the drain current is slightly larger than gate current

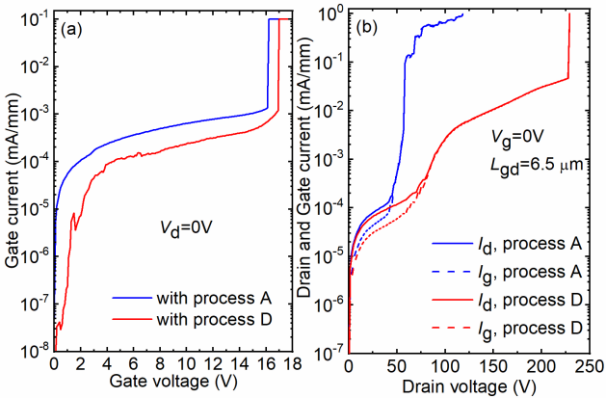

Fig. 8 (a) Forward gate oxide breakdown and (b) off-state breakdown characteristics of normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs.

which is similar to the transfer sweep in Fig. 4. Gate soft breakdown is observed at drain voltage of about 45 V for the normally-off MOS-HEMTs with process A, and the leakage current reaches compliance level at V_d=120V. Gate breakdown and leakage current are related to the electric field and native oxide at the drain edge of gate. [27] The surface residues after ICP etch and rough morphology will result in very high peak electric field at the drain edge of gate, which then causes gate degradation and breakdown. The optimized post-etch surface treatment process helps to smooth the etched GaN surface and results in an improvement in MOS-HEMTs interface, which is beneficial to a decrease in the peak electric field at the drain edge of gate. Therefore, post-etch surface treatment with process D suppresses the leakage current induced by soft breakdown and increases the off-state breakdown voltage up to 230 V for the devices with L_{gd}=6.5 μm. The blocking voltage will be further improved by designing field plate.

For possible power application, the dynamic performance of normally-off MOS-HEMTs fabricated in this work was also characterized using pulsed current-voltage measurement. The dynamic on-resistance was derived from the linear fitting of pulsed I_d~V_d curve with on-state drain voltage ranging from 0 V to 1 V and gate voltage at 0 V. Fig. 9 gives the normalized on-resistance as a function quiescent drain voltage (V_{dQ}) with quiescent gate voltage (V_{gQ}) set at 0 V. With an increase in quiescent drain voltage from 0 V to 80 V, there is a double increase in dynamic on-resistance. The current collapse of MOS-HEMTs in this work is similar to the previous reports where PECVD-grown SiN was used for surface passivation. [28], [29] The optimization of post-etch surface treatment process has little effect on current collapse, because both devices have the same epilayer stack and surface passivation. With an increase in source-drain distance (L_{sd}) from 10 μm to 30 μm, the current collapse is not effectively suppressed. In recess-gate MOS-HEMTs where the channel resistance beneath gate area is much larger than that within access region, most of the drain-source voltage is across the channel beneath gate. Therefore, the increase in length of access region has little effect on the electric field at gate edge, and the current collapse almost remain the same.

The threshold voltage instability of normally-off MOS-HEMTs was characterized by using sequential transfer sweeps with an increase in trap filling voltage (V_{fill}). Different

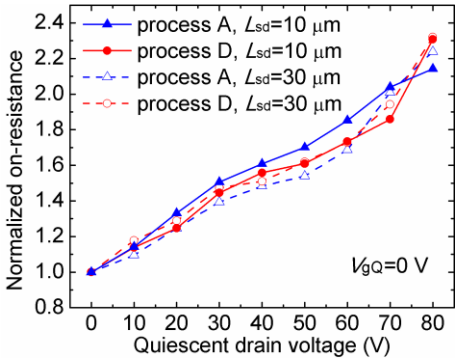

Fig. 9 Impact of post-etch surface treatment and source-drain distance on the dynamic on-resistance of normally-off GaN-based MOS-HEMTs.

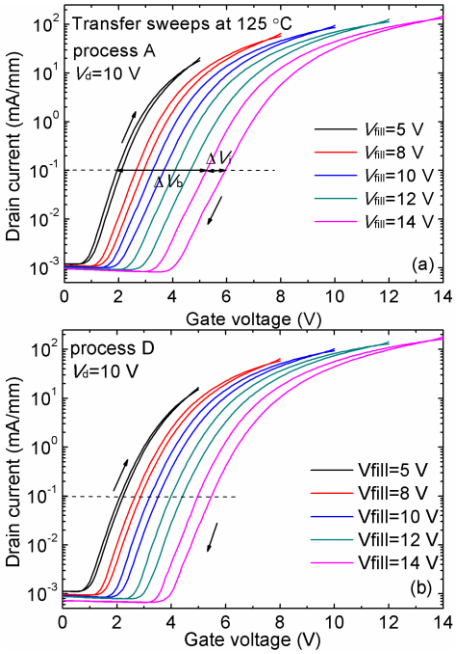

Fig. 10 Influence of trap filling voltage on the hysteresis transfer curves of normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs with (a) post-etch surface treatment process A and (b) process D.

from the method developed in [30], each hysteresis sweep in this paper starts from V_{fill} and then sweeps back, which simplifies the derivation of voltage shift caused by different types of traps. Fig. 10 gives the sequential transfer sweep results of normally-off MOS-HEMTs measured at 125 ℃. The transient voltage hysteresis during each sweep (ΔV_i) is caused by interface trapping effect, while the voltage shift between sequential sweeps (ΔV_b) is attributed to border trapping effect, which exhibits retentivity and cumulation. [30], [31] Negative sweep down to -10 V shows insignificant voltage shift, so the negative bias instability is not further investigated in this work.

Temperature dependent measurement from 25 ℃ to 125 ℃ shows that the trapping effect induced voltage shift remains unchanged for the normally-off MOS-HEMTs. Fig. 11 illustrates the influence of post-etch surface treatment process on positive bias instability of normally-off MOS-HEMTs at 125 ℃. Post-etch surface treatment process with chemical clean or wet etch has little influence on the border trapping effect, which is related to the bulk oxide charges close to interface. The border trapping effect can be further suppressed by optimization of gate insulator, such as annealing under

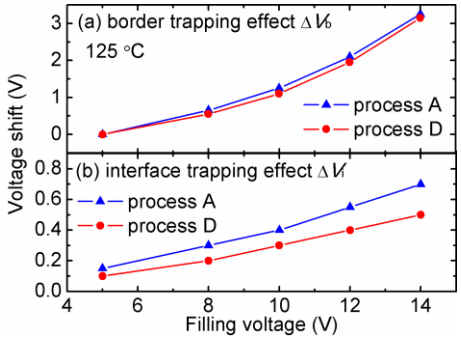

Fig. 11 Voltage shift induced by (a) border trapping effect and (b) interface trapping effect for MOS-HEMTs with different post-etch surface treatment process.

higher temperature or forming gas, alteration of oxygen precursor, and plasma enhancement. The interface trapping effect, however, is improved by using DCIO treatment and wet etch, voltage shift decreasing from 0.7 V to 0.5 V with filling voltage of 14 V.

IV. Conclusion

Post etch surface treatment is of vital importance for the interface issues of GaN-based recess-gate MOS-HEMTs and MOS-HEMTs. Firstly, different post-etch surface treatment process was investigated using AFM analysis. The optimized process effectively removes the surface residues and smooths GaN surface after dry etch, which is chemical clean in $NH_3 \cdot H_2O$, diffusion-controlled interface oxidation, and wet etch in sequence.

Then, normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs were fabricated using fully recessed gate and post-etch surface treatment. The optimized surface treatment process with DCIO and wet etch results in an increase in field-effect mobility of MOS-HEMTs channel by 33%, which makes contribution to a decrease in channel resistance by over 30%, an increase in output current from 233 mA/mm to 300 mA/mm, and an increase in peak transconductance from 35 mS/mm to 41 mS/mm. The post etch surface treatment has little influence on the dynamic characterization and border trapping effect, while improves the interface trapping effect even at high temperature of 125 ℃.

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