Bandwidth-Enhanced Oversampling Successive Approximation Readout Technique for Low-Noise Power-Efficient MEMS Capacitive Accelerometer

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***Abstract*—Bandwidth-Enhanced Oversampling Successive Approximation (BE-OSA) readout technique is proposed in this paper to reduce the noise floor of readout circuit for MEMS capacitive accelerometer while achieving high power efficiency in terms of the figure of merit (FoM). Open-loop structure has been widely used in MEMS capacitive accelerometer for the internet of things (IoT) applications due to its low power consumption. However, in the open-loop accelerometer, the capacitance variation of sensing element is limited to femto-farad level in order to overcome nonlinearity. As a result, the thermal noise from parasitic capacitance becomes significant. The ability of the readout circuit dealing with thermal noise is determined by the front-end switched-capacitor capacitance-to-voltage convertor (SC CVC) rather than the back-end ADC. To reduces the noise floor, traditional oversampling method increases the sampling frequency of SC CVC by increasing transconductance of amplifier, but this leads to low power efficiency. In this work, the BE-OSA technique provides a high power efficiency method as it increases the sampling frequency of SC CVC without increasing the transconductance of amplifier. The SC CVC based on BE-OSA technique is demonstrated in a readout circuit fabricated by a commercial 0.18μm BCD process and tested with a femto-farad MEMS accelerometer. The measurement results show that compared to the readout circuit without using BE-OSA technique, the readout circuit using BE-OSA reduces the noise floor from 2.5aF/√Hz to 0.9aF/√Hz. Compared with the other similar works, the proposed readout circuit achieves the best power efficiency in terms of both the absolute power efficiency (FoM_2=243fJ) among the switched-capacitor readout circuits and the relative power efficiency (FoM_3=0.14).**

***Index Terms*—Capacitive sensor, readout circuit, sensor interface, MEMS accelerometer, parasitic capacitance, low noise, low power, power efficient, switched-capacitor.**

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I. Introduction

MEMS (Micro-electromechanical Systems) capacitive accelerometers play a fundamental part in a wide range of monitoring systems for health care applications [1] and internet of things (IoT) applications [2]. In these applications, sensors are powered by battery, therefore low power consumption and high power efficiency are required to extend battery life [3][4]. To achieve low power consumption, the readout circuits of MEMS accelerometers are designed with open-loop structure (e.g., charge control readout [5][6] and voltage control readout [5][7]-[9]) rather than close-loop one (e.g., force feedback readout [10]-[12]). Compared with the charge control readout structure, the voltage control readout structure offers lower cost. This is because the voltage control readout structure requires only two micromechanical sensing elements to implement fully differential structure while the charge control readout structure requires four [6][7]. However, the main issue of the voltage control readout structure is that its nonlinearity increases with the increase of capacitance variation of sensing element. To suppress the nonlinearity to an acceptable level, the capacitance variation has to be limited to several femto-farad level for an acceptable die cost [3]. But, the fact that the femto-farad level capacitance variation of sensing element is much lower than the parasitic capacitance of sensing electrodes which is at pico-farad-level results in two significant problems: 1) gain accuracy deterioration [13][14] and 2) signal-to-noise ratio (SNR) deterioration [15]-[17]. These are the main challenges for the design of power efficient open-loop MEMS capacitive accelerometers.

The gain accuracy deterioration is caused by signal charge loss due to parasitic-induced gain error, which can be alleviated by three methods. The first method is simply enhancing the gain of pre-amplifier [18] to reduce the signal charge loss. The second method is use of negative impedance (negative-R [19] or negative-C [20]) to compensate the signal charge loss. The third method is to calibrate/correct the gain error with the assistance of the digital circuits [21][22] or the switched-capacitor circuits, such as the oversampling successive approximation (OSA) readout technique [9], correlated double sampling technique [23][24] and correlated level shifting technique [25]-[27], etc. This method is able to provide scaling-

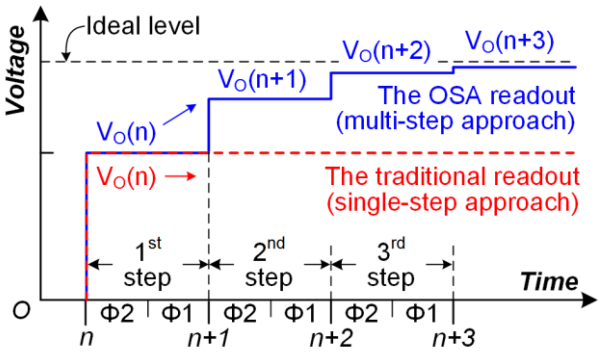


Fig. 1. Concept of OSA readout technique.

friendly solution in modern nanometer CMOS process and it is therefore very popular [28]. The switched-capacitor assisted techniques provide higher power efficiency in capacitive sensor readout circuits than the digital assisted techniques do, as the switched-capacitor assisted techniques are analog-assisted techniques, which do not need power hungry ADC/DAC to interface the assisting circuits with pre-amplifier [29]. Among the switched-capacitor assisted techniques, the OSA readout technique stands out for its insensitivity to parasitic-induced gain error [9]. The basic operation of OSA readout technique will be presented later. The kernel concept of the OSA readout technique is to approach the final output level of SC CVC by multiple steps, rather than traditional single step, as shown in Fig.1. In this way, the gain requirement of pre-amplifier is relaxed and the gain error is therefore minimized.

The SNR deterioration is caused by parasitic-induced noise charge. The existing solutions to this problem are the oversampling method [30], the wideband feedback control [31] [32], the feed forward cancellation [33][34], the holistic noise-power optimization [17] and the parasitic capacitance isolation stage [8] for switched-capacitor readout circuits and negative capacitance cancellation [35] for continuous-time readout circuits. However, these methods are not sufficiently power efficient. In this paper, a "bandwidth-enhanced oversampling successive approximation (BE-OSA)" readout technique is proposed for the switched-capacitor readout circuit to reduce the parasitic-induced noise while achieving high power efficiency. The proposed BE-OSA readout technique in this paper is an advanced version of the reported OSA readout technique [9]. The OSA readout technique focuses on reducing gain accuracy deterioration due to parasitic capacitance, while the BE-OSA readout technique focuses on reducing the SNR deterioration due to parasitic capacitance.

The rest of this paper is organized as follows. In section II, the noise performance of a typical open-loop readout circuit for MEMS accelerometer is discussed. In section III, BE-OSA readout circuit is proposed. In section IV, the physical verification and measurement results are presented. The conclusions are then drawn in section V.

II. Noise Performance of Readout Circuit

For the open-loop readout circuit with significant input parasitic capacitance, the trade-off between noise and power is determined by front-end switched-capacitor capacitance-to

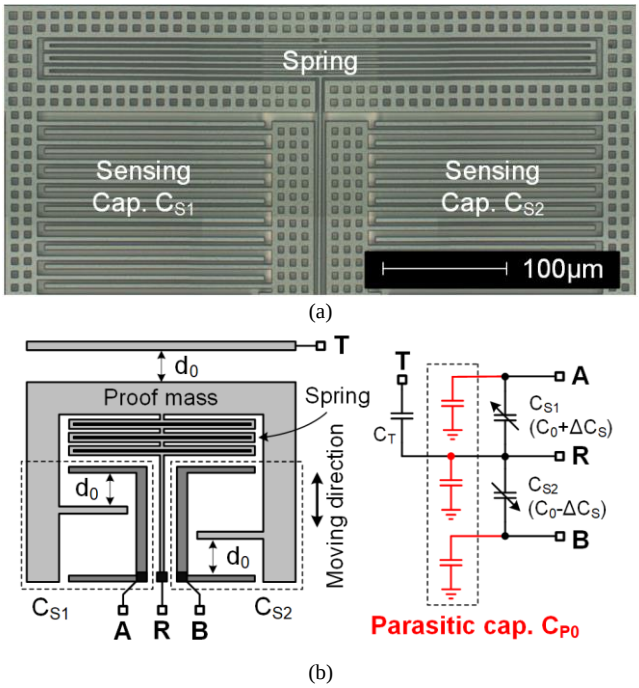


Fig. 2. Sensing element of a typical MEMS capacitive accelerometer. (a) Photograph. (b) Diagram.

voltage convertor (SC CVC) rather than back-end ADC [15][17]. In this section, the sensor structure and SC CVC noise performance are analyzed in detail.

A. Sensor structure

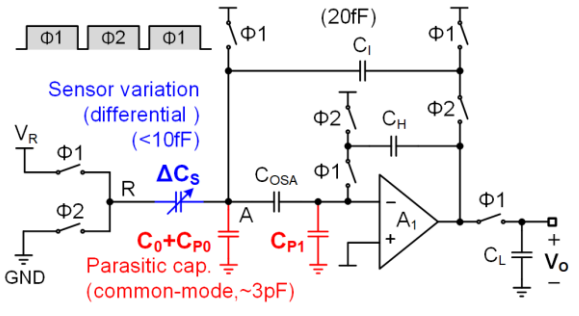
Fig. 2 shows the sensing element in a typical open-loop MEMS capacitive accelerometer. The parasitic capacitance C_{P0} (typically 3pF) from the sensing electrodes A, B and R to the ground is introduced by MEMS device (1pF), electro-static discharge protector (1.5pF) and bonding pad (0.5pF). The sensing capacitances C_{S1} and C_{S2} are the parallel-plate capacitors formed by the stator plates (unmovable plates connected to the electrodes A and B) and the rotor plates (movable plates on the proof mass connected to the electrode R via spring), which are expressed below [36],

$$C_{S1} = C_0\left(\frac{1}{1+\Delta d/d_0}\right), C_{S2} = C_0\left(\frac{1}{1-\Delta d/d_0}\right) \quad (1)$$

where C_0 is the rest capacitance of sensing capacitance, d_0 is the rest distance between a pair of rotor plate and stator plate, Δd is the rotor plate displacement which is in proportion to applied acceleration signal. Equation (1) is a nonlinear function which is undesirable for acceleration measurement. Hence, the linear function (2) is used to approximate the equation (1),

$$\begin{aligned} C_{S1} &\approx C_0(1-\Delta d/d_0) = C_0 - \Delta C_S \\ C_{S2} &\approx C_0(1+\Delta d/d_0) = C_0 + \Delta C_S \end{aligned} \quad (2)$$

According to Taylor's theorem, only by limiting the displacement ratio $\Delta d/d_0$ to a small value (e.g., 3.2%), can the high-order nonlinear approximation error of the equation (2) be limited to an acceptable level (e.g., <0.1%). Thus, given the sensor's typical rest capacitor C_0 being 160fF, the maximum capacitance variation ΔC_S will not exceed 5.0fF to achieve 0.1%



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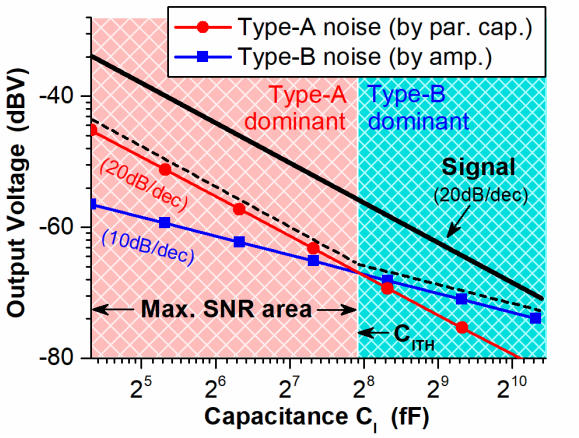

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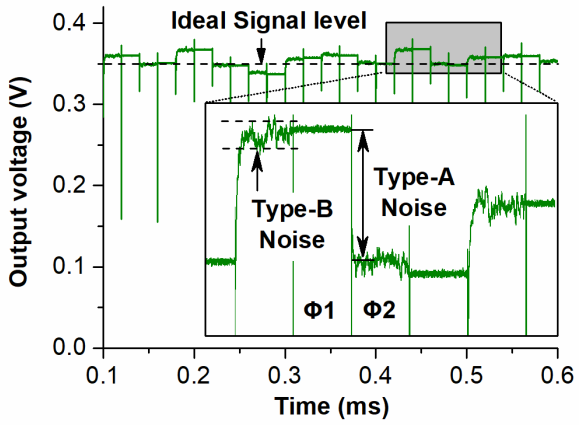


(b)

Fig. 3. Noise analysis of SC CVC. (a) Simplified single-end equivalent circuit model. (b) Relationship between dominant noise and capacitance C_I. (b) Typical transient output waveform of SC CVC when SNR is maximized.

nonlinearity.

B. SC CVC noise performance

The simplified single-end equivalent circuit of the SC CVC based on OSA readout technique (OSA CVC in brief) used to readout the sensing element is shown in Fig. 3(a), where C_{P0} is the parasitic capacitance between sensing electrodes and ground, C_{P1} is the parasitic capacitance introduced by the input transistors of the pre-amplifier A_1. The rest capacitance C_0 of sensing element is also modelled as parasitic capacitance, as it does not contribute to any signal charge. The basic operation of OSA CVC is described as follows. In each step, the pre-amplifier A_1 holds the output level $V_O(n)$ via the feedback network composed of capacitor C_H and C_{OSA}, so that the gain error term of $V_O(n)$ is sampled and will be cancelled in the next

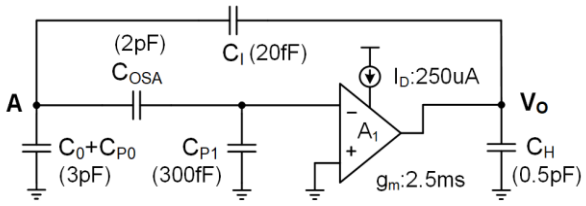


Fig. 4. Equivalent circuit model with typical component parameters of SC CVC during phase Φ2.

step by the capacitor C_{OSA}. As a result, the "new" gain error in the next step is produced by the increment value of the output in the step $\Delta V_O(n+1)$, rather than by the absolute value of the output in this step. Thus, the "new" gain error is smaller than the "old" gain error. Step by step, the gain error is diminished and reduces towards zero exponentially. This means that the gain error will be reduced to infinitesimal at cost of settling time. In this way, the gain requirement of the pre-amplifier $A1$ used in the OSA CVC is relaxed and the gain error is therefore minimized.

1) SNR maximization. According to [30], there are two types of output noise power: the type-A noise $\overline{V_{NA}^2}$ from parasitic capacitance during the phase Φ1 and the type-B noise $\overline{V_{NB}^2}$ produced by the pre-amplifier A_1 during the phase Φ2. They are expressed as follows,

$$\overline{V_{NA}^2} = \frac{kT(C_0+C_{P0})}{C_I^2} + \frac{kTC_{P1}}{C_I^2}\frac{1}{\beta_2^2}$$
$$\overline{V_{NB}^2} = \frac{1}{\beta_1\beta_2}\frac{kT}{C_H}\alpha;\ V_O = \frac{\Delta C_S}{C_I}V_R \quad (3)$$
$$\beta_1 = \frac{C_I}{C_0+C_{P0}};\ \beta_2 = \frac{C_{OSA}}{C_{OSA}+C_{P1}}$$

where α is a constant coefficient with a typical value of 1.5 [30], V_R is reference voltage, C_H is load capacitor during phase Φ2. Equation (3) indicates an important fact that with the decrease of the capacitance C_I, the output signal voltage V_O of SC CVC increases at a rate of 20dB/dec and the output type-A noise voltage $\overline{V_{NA}}$ increases at a rate of 20dB/dec while the output type-B noise voltage $\overline{V_{NB}}$ increases at a rate of 10dB/dec. As a result, the SNR will be maximized when the capacitance C_I is minimized and the type-A noise dominates, as shown in Fig. 3(b). The threshold of the capacitance C_I to maximize SNR is,

$$C_{ITH} = \frac{C_H}{\alpha}\left[\beta_2 + \frac{C_{P1}}{\beta_2(C_0+C_{P0})}\right] \quad (4)$$

When $C_I \ll C_{ITH}$, the noise from amplifier (type-B) is negligible, as shown in Fig. 3(c). In this situation, the power consumption of the pre-amplifier A_1 is no longer determined by its noise performance requirement but by its bandwidth requirement.

2) Noise floor and bandwidth deterioration. As mentioned in the equation (4), the capacitance C_I should be minimized to maximize SNR. Besides, minimizing the capacitance C_I can maximize the sensitivity of SC CVC according to the equation (3), which can further relax the accuracy requirement of the back-end ADC. However, reducing the capacitance C_I leads to

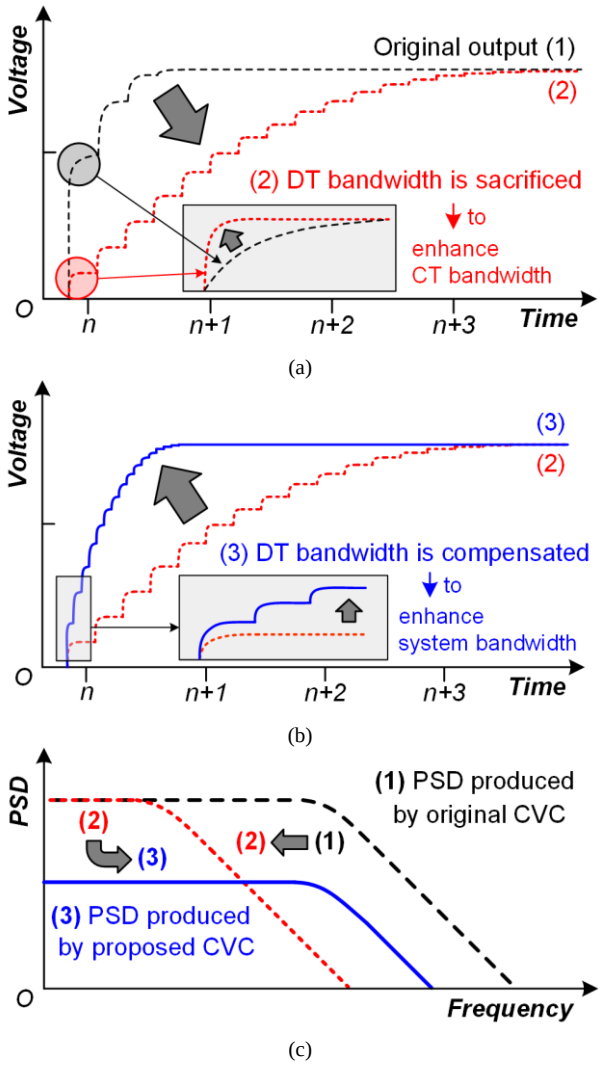


Fig. 5. Concept of BE-OAS technique to reduce noise. (a) DT bandwidth is sacrificed to improve CT bandwidth. (b) Sampling frequency is increased and DT bandwidth is enhanced to compensate system bandwidth. (c) Noise PSD.

reduction of the feedback coefficient β_1 according to the equation (3). And the reduction of β_1 lastly result in reduction of the SC CVC's loop bandwidth BW_{CT} that can be expressed below,

$$BW_{CT} = \beta_1\beta_2\frac{g_m}{C_H} \tag{5}$$

where g_m is the transconductance of the pre-amplifier A_1. Equation (5) is derived from the circuit model in Fig. 4.

Further, reduction of the bandwidth BW_{CT} will lead to reduction of the maximum sampling frequency f_{smax} for a given settling error, as shown by the following expression [17],

$$e^{-\frac{BW_{CT}}{2f_{smax}}} \le Settlig\ error \tag{6}$$

The reduction of the maximum sampling frequency f_{smax} eventually leads to increase of the noise floor that is due to noise aliasing effect and is measured here by power spectrum density (PSD) [30], as shown below,

$$PSD = \frac{2}{\pi}\frac{\overline{V_{NA}^2}}{f_{smax}} \tag{7}$$

Thus, although a small value of C_I will bring high SNR and high sensitivity, the noise floor will be high as well due to reduced sampling frequency. If high sampling frequency is used to reduce the noise floor, large power will be consumed. For example, to support a sampling frequency f_s of 1MHz with 0.1% settling error, the bandwidth BW_{CT} should be at least 13.8MHz according to the equation (6). Given C_I's value being 20fF, as shown in Fig. 4, the value of β_1 is as small as 0.007. As a result, g_m should be as large as 2.5ms according to the expression (5), which requires a typical current supply I_D of 250μA. In practice, this level of current consumes too much power and is therefore too large to be acceptable in IoT applications [3][4].

III. Bandwidth-Enhanced Oversampling Successive Approximation (BE-OSA) Readout Technique

The BE-OSA technique is presented in this section. It increases the sampling frequency of SC CVC without increasing the gain-bandwidth product of pre-amplifier, thus reducing the noise floor without sacrificing power efficiency. For the clarity of explanation, the following three bandwidth terms are used.

1) Continuous-Time (CT) bandwidth, BW_{CT}. The CT bandwidth is the closed loop bandwidth of an amplifier, whose value is dependent on g_m/C constant and feedback coefficient [37]. In this work, the CT bandwidth determines the maximum value of CVC's sampling frequency f_S.

2) Discrete-Time (DT) bandwidth, BW_{DT}. The DT bandwidth is the system bandwidth with normalized sampling frequency f_S, whose value is dependent on the pole of Z trans-function of the system. In this work, the DT bandwidth determines the number of steps/periods that CVC needs to settle down.

3) System bandwidth, BW_{SYS}. The system bandwidth refers to the "-3dB bandwidth" of the system, whose value is dependent on the product of BW_{DT} and f_S [37]. In this work, the system bandwidth determines the total time that SC CVC needs to settle down.

A. Principle

The basic concept of the BE-OSA readout technique is shown in Fig. 5, which includes two stages to achieve power efficient noise floor reduction.

At the stage one, DT bandwidth is sacrificed for CT bandwidth, as shown in Fig. 5(a). Compared with the output of the original OSA CVC (Fig. 2(b)), the output of the BE-OSA CVC takes more steps (sacrificing DT bandwidth) to reach the same final output level, hence the gain requirement of each step is reduced. As pre-amplifier's gain-bandwidth product is constant, the CT bandwidth in each step is therefore enhanced without increasing the pre-amplifier's power consumption.

At the stage two, sampling frequency is increased and DT bandwidth is compensated, as shown in Fig. 5(b). Since the CT bandwidth is improved, the maximum sampling frequency can

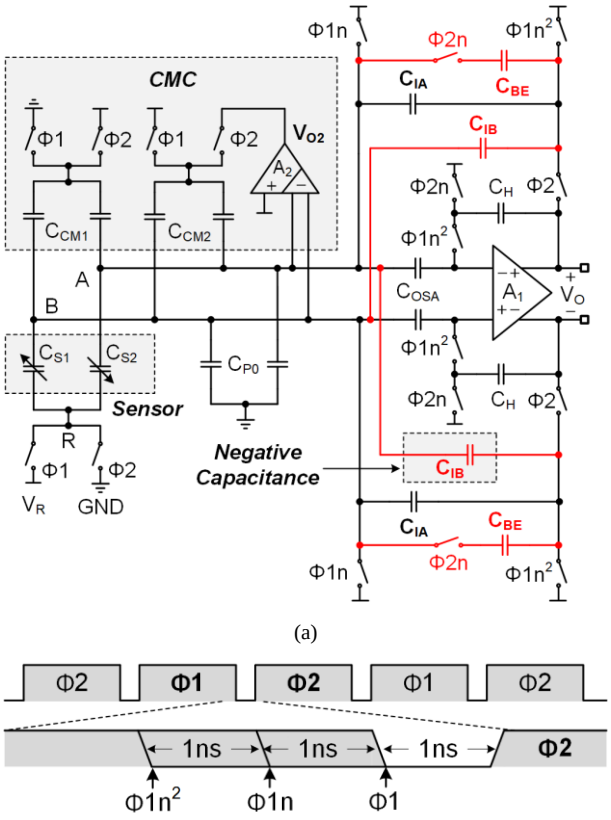


Fig. 6. BE-OSA CVC with negative capacitance C_{IB} and CT bandwidth enhancement capacitor C_{BE}. (a) Schematic. (b) Clock diagram.

be increased. As a result, the noise floor is reduced. A DT bandwidth compensation circuit is also employed at this stage to compensate the DT bandwidth sacrificed at the stage one, in order to avoid the loss of system bandwidth.

The noise PSDs of each step are shown in Fig. 5(c). Compared with the PSD produced by the original CVC, the PSD produced by the proposed BE-OSA CVC is reduced without losing system bandwidth.

The key circuits to implement BE-OSA CVC are: 1) sensitivity boost circuit, 2) CT bandwidth enhancement circuit and 3) DT bandwidth compensation circuit. The other circuits, such as common-mode charge controller (CMC), etc., can be found in [9] and they are not discussed here.

B. *Circuit-I: sensitivity boost*

As mentioned in section II, the capacitance C_I should be minimized to maximize SNR and sensitivity. However, due to physical size limitation in manufacturing process, small capacitance sometimes cannot be directly acquired. So the negative capacitance C_{IB} is employed here to produce an equivalent small value capacitor C_I, as shown in Fig. 6(a). For example, if the expected value of C_I is 20fF while the minimum capacitance possible is 30fF, then C_I of 20fF can be produced by C_{IA} of 50fF and C_{IB} of -30fF. The output voltage is,

$$V_O = \frac{2V_R}{C_{IA} + C_{IB}} \Delta C_S = \frac{2V_R}{C_I} \Delta C_S \tag{8}$$

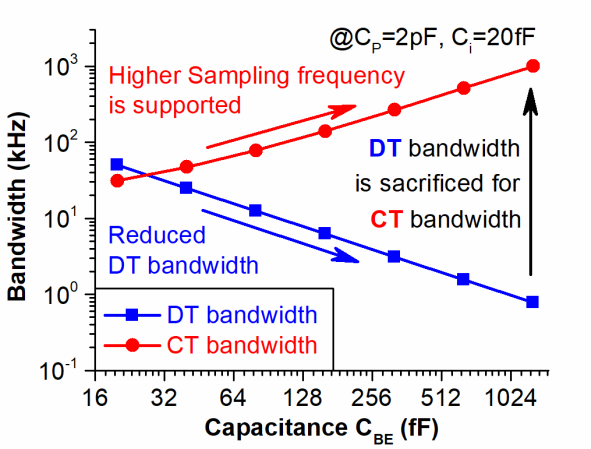


Fig. 7. Bandwidth change with the change of C_{BE}

C. *Circuit-II: CT bandwidth enhancement*

The CT bandwidth is enhanced by the capacitor C_{BE} in Fig.6(a), which plays two important roles. The first role is the CT auxiliary feedback path enhancing the feedback coefficient β_1, hence increasing the CT bandwidth. With C_{BE}, the CT bandwidth becomes,

$$BW'_{CT} = \beta'_1 \beta_2 \frac{g_m}{C_H + C_L}$$
$$\beta'_1 = \frac{C_I + \boldsymbol{C_{BE}}}{C_I + C_{P0} + \boldsymbol{C_{BE}}}; \beta_2 = \frac{C_{OSA}}{C_{OSA} + C_{P1}} \tag{9}$$

where β'_1 is the feedback coefficient enhanced by C_{BE}. The second role of C_{BE} is an integrator which sacrifices the DT bandwidth. The BE-OSA CVC's transfer function and the DT bandwidth are,

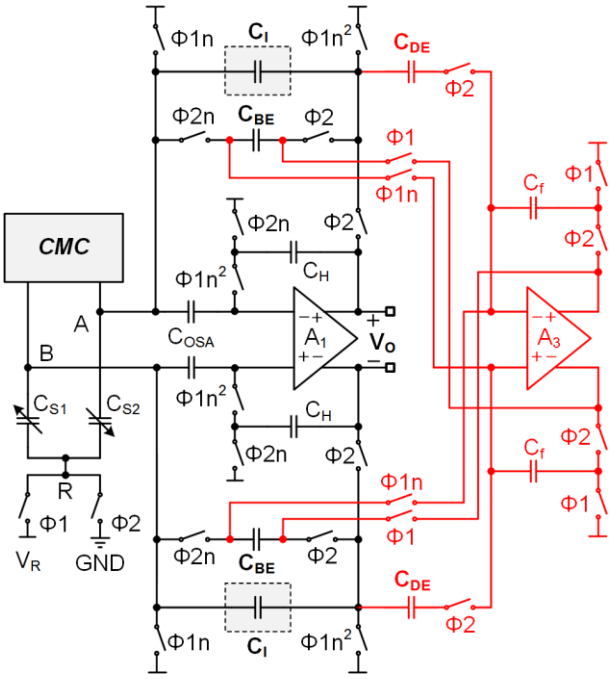
$$H_1(z) = (z - p_0)^{-1};$$
$$BW_{DT} = \frac{2}{\pi} tan^{-1}\left(\frac{1 - p_0}{1 + p_0}\right);\ p_0 = \frac{C_{BE}}{C_{BE} + C_I}; \tag{10}$$

Equations (9) and (10) show that when C_{BE} is smaller than C_{P0}, with increase of the value of the capacitor C_{BE}, the CT bandwidth increases at a rate of +20dB/dec while the DT bandwidth decreases at a rate of -20dB/dec, as shown in Fig. 7. Therefore, the CT bandwidth can be improved at the cost of the DT bandwidth rather than sacrificing power consumption.

D. *Circuit-III: DT bandwidth compensation*

In order to avoid the loss of system bandwidth due to sacrificing DT bandwidth, the compensation circuit composed of the capacitor C_{DE} and the amplifier A_3 is added, as shown in Fig. 8(a). Notably, the additional power consumption introduced by the amplifier A_3 is negligible compared to that of pre-amplifier A_1. This is because the feedback capacitor C_f can be set to a large value to minimize the g_m requirement of A_3.

The rationale of the DT bandwidth compensation circuit is to speed up the charging process of the CT bandwidth enhancement capacitor C_{BE} via the capacitor C_{DE}.The larger the value of C_{DE} is, the faster C_{BE} is charged, and then the more DT bandwidth can be compensated. However, if C_{DE} is too large,



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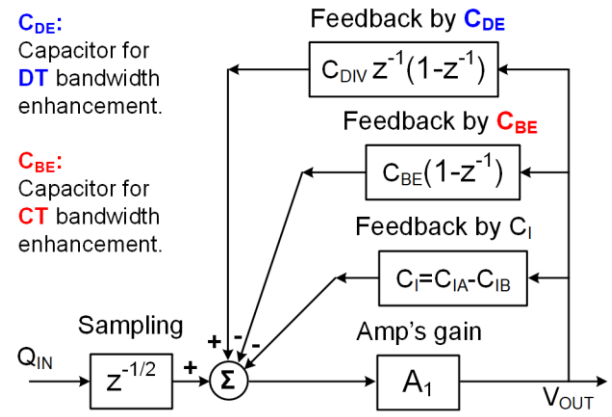


(b)

Fig. 8. Complete circuit implementation of BE-OSA CVC. (a) Schematic. (b) Signal diagram.

the system will become unstable. According to the signal flow diagram shown in Fig. 8(b), the system transfer function is,

$$H_2(z) = \frac{z^2}{z^2 - az + b}$$
$$a = \frac{C_{BE} + C_{DE}}{C_{BE} + C_I}, b = \frac{C_{DE}}{C_{BE} + C_I} \quad (11)$$

To guarantee system's stability, the condition below has to be satisfied,

$$a^2 \geq 4b, \left|\frac{a \mp \sqrt{a^2 - 4b^2}}{2}\right| \leq 1 \quad (12)$$

Then the maximum value of the capacitor C_{DE} can be acquired by solving (17),

$$C_{DE} = C_{BE} - 2C_I\left(\sqrt{1 + C_{BE}/C_I} - 1\right) \quad (13)$$

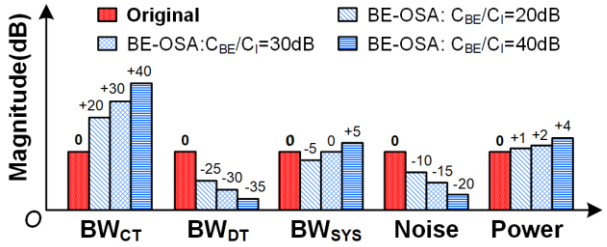


Fig. 9. Comparison of bandwidth, noise performance and power consumption between original CVC and BE-OSA CVC.

By applying the equation (13) to the equation (11), the new pole is

$$p_0' = \frac{1}{2}\frac{C_{BE} + C_{DE}}{C_{BE} + C_I} \quad (14)$$

It can be seen from the equations (10), (13) and (14) that the value of the new pole p_0' is smaller than that of the original pole p_0. Thus, the new pole provides higher DT bandwidth.

The system bandwidth BW_{SYS} is determined by the maximum sampling frequency f_{smax} and the DT bandwidth BW_{DT},

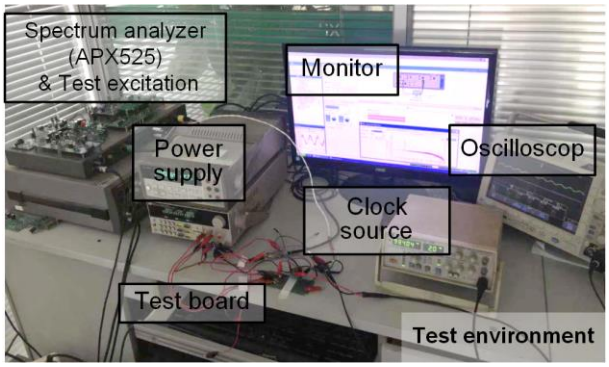
$$BW_{SYS} = 2\pi f_{smax} BW_{DT} \quad (15)$$

An intuitive illustration of the BE-OSA technique's effect is shown in Fig.9. According to the expression (14), with increase of C_{BE}, the CT bandwidth is increased. This leads to increase of sampling frequency and reduction of noise floor. Furthermore, according to the equations (10), (14) and (15), the amount of the sacrificed DT bandwidth is less than that of the increased CT bandwidth. Thus, the overall system bandwidth loss is negligible. The slight power increment is due to the use of the amplifier A_3 and the switched-capacitor network with increased sampling frequency.

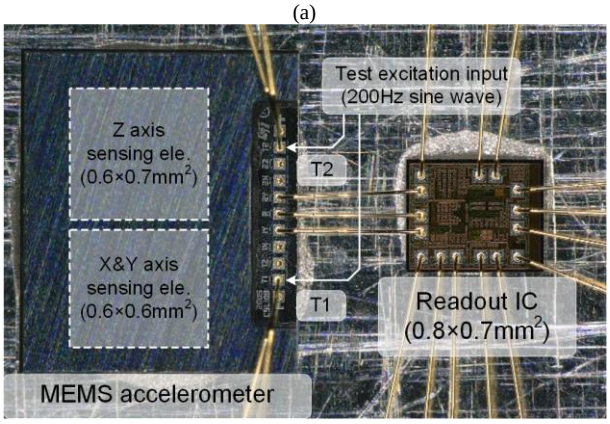
IV. Physical Verification

The BE-OSA CVC described above is demonstrated in a readout circuit fabricated by a commercial 0.18μm BCD process. The readout IC is tested with a femto-farad 3-axis MEMS capacitive accelerometer (only one axis is measured), as shown in Fig. 10(a) and Fig. 10(b). The readout IC integrates BE-OSA CVC, CMC, calibration circuits, references, clock generator and buffers, as shown in the layout in Fig. 10(c). The on-chip clock generator includes an oscillator to generate clock source and a non-overlapping clock generator to provide non-overlapping clock phases. When the readout circuit is in the test mode, the output frequency of the clock generator is synchronized by an outside clock source. The pre-amplifier A_1 used in SC CVC is a traditional fold-cascade amplifier with 70dB gain, 10MHz GBW@2pF capacitive load, 16nV/√Hz input equivalent noise, 200fF input parasitic capacitance and 30μA current consumption. The amplifier A_2 has a 10μA current consumption and a 100fF input parasitic capacitance. The amplifier A_3 has a 3μA current consumption.

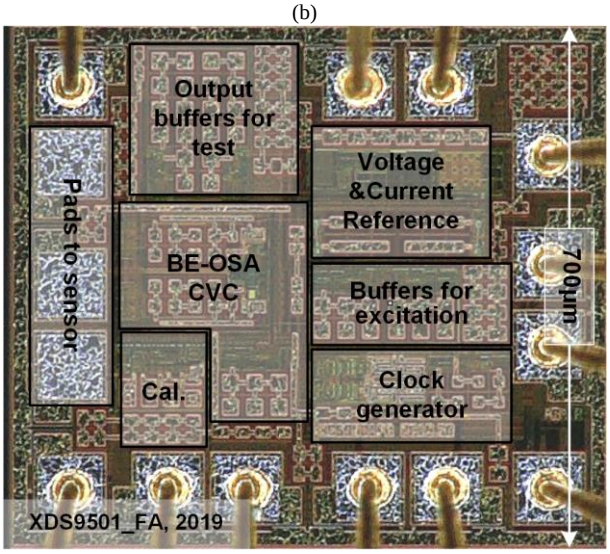
A 200Hz test excitation $V_{TEST} = V_{OS} + A_0 \sin(\omega_0 t)$ generated by the spectrum analyzer (APX525) is applied to the



(a)



(b)



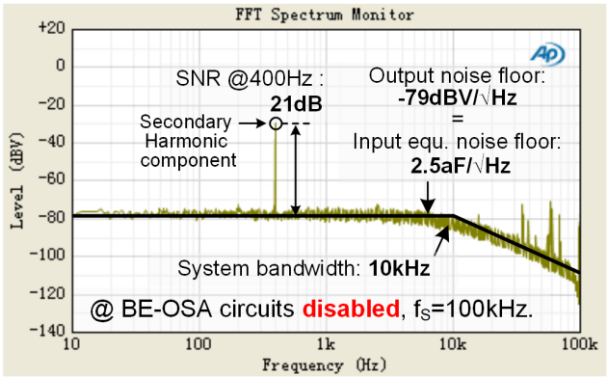
(c)

Fig. 10. Readout chip based on BE-OSA technique tested with a femto-farad MEMS accelerometer. (a) Test environment. (b) Photograph of the chip bonded with the MEMS accelerometer. (c) Photograph of the chip.

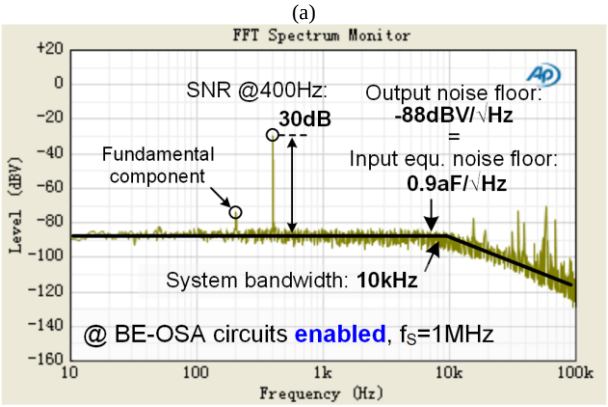
test electrode T (shown in Fig.2) of sensing element. An electrostatic force F_{TEST} is then produced by the test electrode T to drive the proof mass of the sensing element. The electrostatic force can simulate input acceleration signal, which is expressed as,

$$F_{TEST} = \frac{1}{2}\frac{C_T}{d_0}[(1-D)(V_{OS}+A_0\sin(\omega_0 t))^2 + D(V_R - V_{OS} - A_0\sin(\omega_0 t))^2] \quad (16)$$

where d_0 have been defined in the equation (1), C_T is the capacitance between the test electrode T and the proof mass, D is the duty circle of phase Φ1. Given the conditions $D = 50\%$



(a)



(b)

Fig.11. Measurement result of output PSD with 128k points FFT. (a) BE-OSA circuits are disabled. (b) BE-OSA circuits are enabled.

and $V_{OS} = 0.5V_R$, the equation (16) is simplified as,

$$F_{TEST} = \frac{1}{4}\frac{C_T}{d_0}[\frac{1}{2}V_R^2 + A_0^2(1-\cos(2\omega_0 t)] \quad (17)$$

Equation (17) shows that there is no fundamental component and only secondary harmonic component (400Hz) exists in the sensor's response. This is also illustrated in the output PSD in Fig. 11. Therefore, only the secondary harmonic component is used to calculate SNR or noise floor.

A comparison experiment between with and without BE-OSA technique is conducted. Firstly, when the BE-OSA circuit blocks (i.e., circuit-II and circuit-III) are disabled, the single-end output noise floor is -79dBV/√Hz (equal to an input equivalent noise floor of 2.5aF/√Hz) and the SNR at 400Hz is 21dB, as shown in Fig. 11(a). Then, when the BE-OSA circuit blocks are enabled, the sampling frequency can be improved from 100kHz to 1MHz, the output noise floor is reduced to -88dBV/√Hz (equal to an input equivalent noise floor of 0.9aF/√Hz) and the SNR is improved to 30dB, as shown in Fig. 11(b). The current consumption from power supply is measured by a 200Ω series shunt resistor and a commercial low noise amplifier LT1997-1. The measurement results are shown in Fig. 12(a). When the BE-OSA circuit blocks are disabled, the total current consumption of the readout IC is 256μA. When the BE-OSA circuit blocks are enabled, the total current consumption increases from 259μA to 262μA with the sampling frequency increasing from 0.1MHz to 1MHz. So the increment of the total current consumption by using BE-OSA circuits at 1MHz sampling frequency is 6μA (262μA-256μA). The current consumptions from each building block at 1MHz sampling

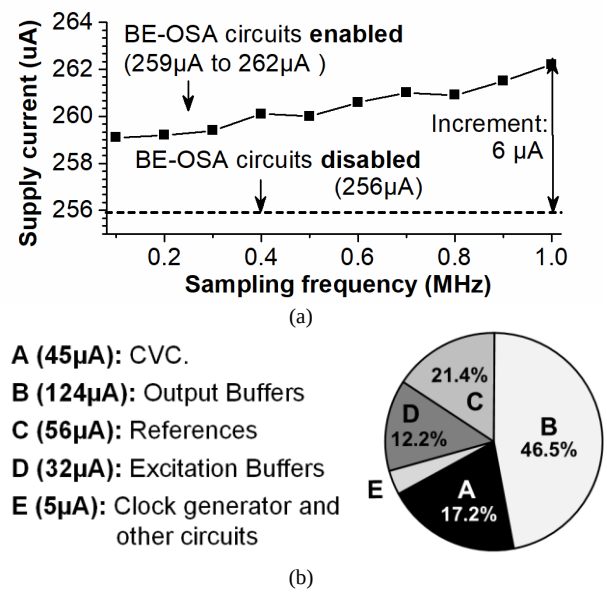


Fig.12. Measurement results of current consumption. (a) Current of whole chip. (b) Current consumption of each building block.

frequency are shown in Fig. 12(b), where CVC consumes 17.2% (45μA) of the total current. The increment of total current consumption (6μA) is mainly due to CVC. Thus, by employing the BE-OSA circuits, the current consumption of CVC increases by 1.2dB from 39μA to 45μA, but the noise floor is reduced by 9dB (88dB-79dB). The spectrum peak in high frequency range is due to deterministic interference rather than random noise.

The comparison between BE-OSA and other similar parasitic-induced noise reduction techniques for CVC is given in Table I. Generally, there are two main types of figure of merit (FoM) used to evaluate the power efficiency of MEMS accelerometer [11],

$$FoM_{1A}[W \cdot F/Hz] = \frac{Power \times Noise\ floor}{\sqrt{Bw}} \tag{18}$$

or [34],

$$FoM_{1B}[W \cdot F/Hz] = \frac{Power}{Dynamic\ range \times Bw} \tag{19}$$

The FoM_{1A} emphasizes on the current efficiency, i.e., to reduce the noise floor with as little increment of supply current as possible. The FoM_{1B} emphasizes on the voltage efficiency, i.e., to increase the signal range with as little increment of supply voltage as possible [38]. Since the purpose of this work is to improve the current efficiency/utilization, the FoM_{1A} is preferred. However, the comparison only by FoM_{1A} may not be true reflection of power efficiency, as FoM_{1A} is defined for close-loop or large size accelerometers for industrial applications whose noise performance is not dominated by the parasitic capacitance. In open-loop or small size accelerometer for IoT applications, the output noise is significantly affected by the input parasitic capacitance which should be taken into account for the measurement of FoM [15]. Therefore, a modified FoM is introduced for fairer comparison, which is defined as,

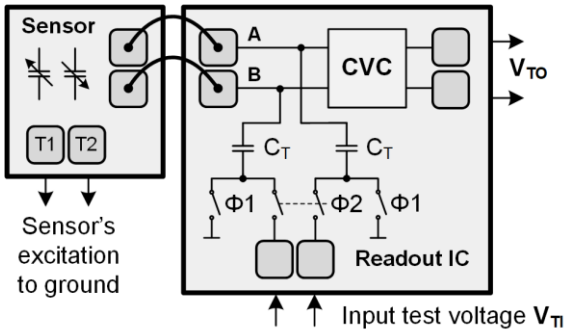


Fig.13. Measurement configuration of IC sensitivity.

$$FoM_2[J] = \frac{Power \times Noise\ floor}{C_P \times \sqrt{Bw}} \tag{20}$$

where C_P is parasitic capacitance. Using FoM_2, this work shows the best power efficiency among the switched-capacitor CVCs ([9] and [17]), as shown in Table I. The work [17] achieves the lowest absolute current consumption (0.13μA) but with poor power efficiency (2,416fJ). This is because the direct successive approximation capacitive-to-digital converter (SAR CDC) structure in [17] uses the capacitor digital-to-analog convertor (CDAC) as the feedback network which introduces additional Type-A noise charge [8]. The work [9] employs the traditional oversampling method and achieves the poorest power efficiency (62,856fJ). The continuous-time CVCs ([35][39][40]) shows averagely better $FoM2$ than that of switched-capacitor CVCs ([7], [9] and this work). This is because the basic continues-time operation is free from the noise aliasing effect introduced by sampling operation [30]. However, continuous-time operation loses the ability to settle out offset and flicker noise from per-amplifier and therefore surfers from serious flicker noise at low frequency range.

Furthermore, as noise reduction techniques lead to increase of power consumption, the relative $FoM2$ is adopted here to evaluate more accurately power efficiency. It is defined as,

$$FoM_3 = \frac{20\log(\Delta P)}{20\log(\Delta FoM_2)} \tag{21}$$

where ΔFoM_2 is the percentage of FoM_2 improvement, and ΔP is the percentage of power increment corresponding to the ΔFoM_2. For example, in order to improve FoM_2 by 10dB ($\Delta FoM_2 = 316\%$) using traditional oversampling method, the power consumption has to increase by 20dB ($\Delta P = 1000\%$). Thus, FoM_3 of traditional oversampling method is 2.0, and so is the FoM_3 of basic continuous-time operation [30]. Compared to [17] and [35] which achieve a FoM_3 of 1.0 and 0.83, respectively, this work achieves a FoM_3 of 0.14. Thus, the BE-OSA technique shows the best power efficiency in terms of FoM_3 for open-loop MEMS capacitive accelerometer. For the purpose of data integrity, the other parameters measured in the experiments are listed in the table II. The measurement configuration is shown in Fig. 13. The two test capacitors C_T are used to inject test charge to CVC to measure the IC sensitivity. The IC sensitivity is then calculated by $V_R V_{TO}/V_{TI} C_T$, where V_{TI} is the input test voltage and V_{TO} is the output

TABLE I COMPARISON OF PARASITIC-INDUCED NOISE REDUCTION TECHNIQUES*

	★	[17]	[9]	[35]	[39]	[40]
Readout circuit type	Switched-capacitor			Continuous-time		
Noise reduction technique	BE-OSA	Holistic optimization	Traditional oversampling	Negative cap. cancellation	Basic continuous-time operation	
Para. cap. C_P (pF)	3	6	3	380	0.45	2.5
Input noise floor (aF/√Hz)	0.9	613.2	54	0.08	0.38	0.85
Bandwidth (Hz)	10,000	30	10,000	46,000	4,000	500,000
Supply Current (μA)	45	0.13	194	10,830	27	88
Supply Voltage (V)	1.8	1.0	1.8	5.0	1.2	2.5
Input range (fF)	10	9,500	-	6.9	48	1,800
IC Process (nm)	180	180	180	-	130	65
FoM_2(fJ)	**243**	**2,416**	**62,856**	**53**	**435**	**104**
FoM_3	**0.14**	**1.0**	**2.0**	**0.83**	**2.0**	**2.0**

*All the results of this work are tested under room temperature (27°C).

voltage excited by V_{TI}. By measuring the output voltage change of the readout circuit when ±1g acceleration is applied to the accelerometer, the system sensitivity of the accelerometer is obtained. The sensor sensitivity is calculated by dividing the system sensitivity by the IC sensitivity. The acceleration noise is calculated by dividing the input noise floor of CVC (shown in table I) by the sensor sensitivity.

TABLE II PARAMETERS SUMMARY

Parameters	Value	Parameters	Value
IC sensitivity	90mV/fF	Sensor sensitivity	1fF/g
Acc. noise	0.9mg/√Hz	Full scale range	±8g
Nonlinearity	0.5%@[0,8g]	Sampling freq.	1MHz

V. CONCLUSION

The BE-OSA technique is proposed in this paper to reduce the noise floor of readout circuit for MEMS capacitive accelerometer while achieving high power efficiency. The noise floor of readout circuit is dominated by the thermal noise charge from parasitic capacitance in the input terminals of the front-end CVC. Traditional oversampling method can reduce the noise floor at the cost of the increased power consumption which is often too high to be accepted for IoT applications. The BE-OSA readout technique sacrifices the CVC's DT bandwidth rather than power consumption to improve sampling frequency and then compensates the DT bandwidth with negligible increase of power consumption. As a result, the noise floor of SC CVC is significantly reduced while system bandwidth loss and power consumption increment are minimized, i.e., high power efficiency is achieved. The SC CVC based on BE-OSA readout technique is demonstrated in a readout circuit fabricated with a commercial 0.18μm BCD process and tested with a femto-farad MEMS capacitive accelerometer. The measurement results show that compared to the readout circuit without BE-OSA circuits, the readout circuit with BE-OSA circuits reduces the noise floor from 2.5aF/√Hz to 0.9aF/√Hz. Compared with the other similar works, the proposed readout circuit achieves the best power efficiency in terms of both the absolute power efficiency (FoM_2=243fJ) among the switched-capacitor readout circuits and the relative power efficiency (FoM_3=0.14).

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