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Data-Driven Fault Localization of a DC Microgrid with Refined Data Input

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Abstract—This paper proposes an online fault localization method for low voltage DC microgrids. This method is based on Artificial Neural Network (ANN) and only requires real-time measurements of a local power converter to locate a fault. During a DC fault, the current component fed by the AC grid can contribute to time-variant non-linearity, which is undesirable to the development of the data-driven method. A novel real-time scheme is thus proposed to exclude such components from DC fault current. The principle of the scheme is introduced and illustrated with time-domain analysis. The effectiveness is verified by case studies of locating a DC fault in a radial DC network fed by a 3-phase voltage source converter.

Keywords — Low-voltage DC Microgrid, Fault localization, Data-driven, Data-refining, ANN

I. INTRODUCTION

VULNERABILITY of short-circuit faults and lack of mature protection scheme are the major constraints in the practical implementation of voltage source converter (VSC) based low-voltage direct current (LVDC) distribution system [1]. However, LVDC distribution system (or DC Microgrid) is becoming an attractive option due to increased penetration and development of renewable energy sources (RES), energy storage systems (EES), and electric vehicles (EV) [2]. Further, it provides flexible operational control to RES along with enhanced efficiency and optimal power flow [2].

Regardless of all the advantages of establishing LVDC system, detecting, isolating and locating DC fault appropriately has become a bottleneck in the development of LVDC distribution system. Majority of the established fault locating techniques so far locates the fault after isolating the faulty section (i.e. by using off-line methods), which normally requires extra signal injecting relay and/or device to locate the fault. A typical approach is to inject a special signal into the faulty section using a power probe unit (PPU) after fault isolation [3]–[5]. The injected signal can be then analyzed for locating fault using various methods, such as method based on voltage comparison [6], a non-iterative method based on least square [3], and impedance estimation [4]. Extra signal injecting device (i.e. PPU) is required adding an extra cost and complexity as well as increased fault locating time. The use of PPU along with the human intervention (even for portable PPUs [3]) makes these techniques costly and inconvenient.

Conversely, non-unit based fault-locating techniques based on an analytical model involve derivation criterion with the high probability of inaccuracy due to the addition of noise [7]. Further, some recently established fault location techniques incorporated multi-resolution analysis (MRA) based on Wavelet Transform (WT) [8], [9], and data-driven methods with Artificial Neural Networks (ANN) [10] in LVDC networks. With a trained neural network from a collection of off-line data, ANN has the ability to perform fast calculations, which makes it suitable for developing real-time fault location technique using real-time data. Comparing with the deterministic analytical method, data-driven approaches do not have to seek analytical solutions for complex systems, which is mathematically complicated, hence making such methods practically challenging to implement. ANN based fault-locating technique for LVDC system is introduced to locate a DC fault in an off-line manner [11]. Taking advantage of data-driven approach, such power electronics-based network is treated as a black box in network training. However, this method requires large number of cases and dataset for training purposes which increases its implementation time as the network gets bigger. Further, the reported techniques have also overlooked the non-linearity introduced by the AC source, which can be quite significant for large impedance fault. On the other hand, a DC fault also produces an impact on the variation of AC side fault current contribution. This inserts an additional complexity in DC fault current. Without the exclusion of such impact, the robustness of fault-locating techniques could be undermined.

In this paper, an online technique for locating fault is proposed based on ANN. The technique is based on local measurement (i.e. using only voltage and current signal), which can be embedded within a power converter. By excluding the non-linear AC contribution in fault current detection, the robustness against fault timing can be improved.

The paper is outlined as follows. Section II illustrates the modelling of LVDC system and analyses the fault behaviour of LVDC system detailing the current contribution from the AC source. In Section III, a novel online AC fault current exclusion method is proposed. ANN-based fault locating estimation technique is demonstrated and validated by performing a case study analysis in Section IV. Finally, the conclusion is drawn in Section V.

II. MODELLING OF LVDC SYSTEM

A. System Layout

Two-level three-phase voltage source converter (VSC) is commonly used for AC-DC interfacing in utility DC systems due to its operational flexibility with RES [12]–[14]. Switching and average models for VSC have been developed so far to utilize in LVDC system modelling [15]–[18]. By looking into the modulation transient, the switching model can detail the high-frequency circuit switching for a converter during a fault transient. Whereas the modulation process is assumed instant in an average model hence the ignorance of transients during a modulation cycle [19]–[21]. Therefore, a detailed switching model is being used in this research.

At a steady state, a vector control method is used to regulate the current and power exchange between the DC Microgrid and the mains. As illustrated in Fig.1., the function extends to DC voltage regulation as well. During a severe DC fault, the DC voltage may drop well below the essential level [23] out of modulation; hence the current/voltage will not be functioning. This will disable the vector control of the interfacing VSC [22], which is demonstrated in Fig. 1.

LVDC system with a detailed VSC switching model is developed based on in Fig. 1 to analyze the post-fault behaviour under short-circuit fault conditions. VSC is connected to AC voltage source through AC side inductive reactance, L_{ac} and resistance, R_{ac} . Whereas, C_f , L_{cable} and R_{cable} represent terminal capacitance, DC side cable inductance and resistance, respectively for an unearthened system. Whereas, R_f demonstrates the level of fault resistance during short-circuit faults. V_{DC} corresponds to DC voltage, i_c is the capacitor current and i_{cable} expresses the current passing through DC side cable. A capacitor between earth and the cables is negligible due to low voltages of the system.

B. DC Post-Fault Analysis

DC pole-to-pole fault is the most vulnerable fault for VSCs. The fault transient can be divided into three stages [2]: In Stage (I), VSCs terminal capacitors discharges and high current flows through the short-circuit loop. Stage (II) is initiated after the complete discharge of the terminal capacitor. In this stage, as the fault current reaches its peak

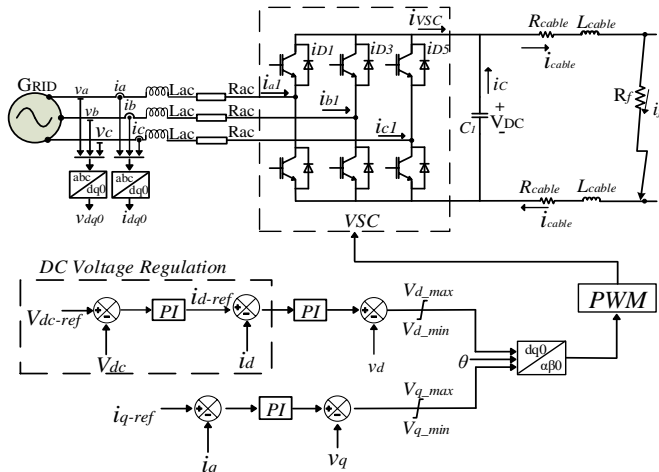


Fig 1. LVDC system with General Control Scheme for 2-level VSC [22] value, it gradually decays through the free-wheeling diodes. In Stage (III), AC side source starts to contribute towards the fault current through AC side reactance and the diodes. The transient model for each stage during the short-circuits fault is demonstrated in Fig. 2.

The transient fault current through the cable during stage (III), i.e. after the conduction of free-wheeling diodes is solved as [23]:

$$i_{fT}(t) = K_1 \sin(\omega_{ac}t + \partial) + K_2 e^{-\gamma t} + [K_3 (\omega_i/\omega_d) e^{-\alpha t} \sin(\omega_d t + \delta)] + [(K_4/\omega_d) e^{-\alpha t} \sin(\omega_d t)] \quad (1)$$

$$v_{fT} = R_T i_{fT}(t) + L_T \frac{di_{fT}(t)}{dt} \quad (2)$$

where

$$\begin{aligned} K_1 &= I_m \sqrt{(1 - \omega_{ac}^2 L_T C)^2 + (R_T C \omega_{ac})^2} \\ \partial &= \varphi - \theta \\ \theta &= \tan^{-1}[(R_T C \omega_{ac}) / (1 - \omega_{ac}^2 L_T C)] \\ \gamma &= R / (L_{ac} + L_T) \\ K_2 &= I_{m-p} [\gamma^2 L C - R C \gamma + 1] \\ K_3 &= -(K_1 \sin \partial + K_2) \\ K_4 &= K_2 \gamma - \omega_{ac} K_1 \cos \partial \end{aligned}$$

where R_T , L_T , and C represents the total resistance, inductance, and capacitance of DC side, respectively. ω_{ac} represents the ac source angular frequency, φ is the angle of phase-a at time t .

From (1), we can clearly find that the fault current is relevant to the timing of a fault.

$K_1 \sin(\omega_{ac}t + \partial)$ represents the AC side feed in current during fault stage (I & II) transient

$K_2 e^{-\gamma t}$ represents the decaying of the capacitor discharging current during Stage I transient

$K_3 (\omega_i/\omega_d) e^{-\alpha t} \sin(\omega_d t + \delta)$ represents the AC feed in current and circulating the current flow through converter in Stage (II & III) transient

$(K_4/\omega_d) e^{-\alpha t} \sin(\omega_d t)$ represents the final steady-state fault current after the transient

III. AC SOURCE CURRENT FILTRATION

Due to the clear non-linear and time-variant characteristic of fault current in (2), it is difficult to develop an accurate fault locating technique based on that. However, when the

TABLE I
LVDC SYSTEM SIMULATION PARAMETERS

Parameter	Nominal Value
Rated Input Power	2 MW
AC side Transformer L-L Voltage	690 V
AC Nominal Frequency	50 Hz
AC side Inductive Reactance	0.2 p.u.
AC side Resistance	0.01 p.u.
DC Side Voltage	1200 V

Terminal Capacitance (C_T)	10 mF
Cable length (l_c)	1 km
Cable Resistance/m	0.01 mΩ/m
Cable Inductance/m	0.1 μH/m
Diode Resistance (R_D)	0.01

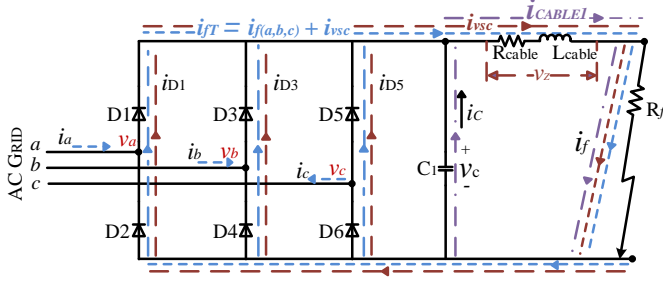


Fig. 2. Equivalent Circuit for fault analysis at each stage. (a) Stage-I, Capacitor discharging stage. (b) Stage-II, Free-wheeling diodes conduction stage. (c) Stage-III, AC-Source fault contribution stage.

components relevant to AC side are excluded, the remainder becomes irrelevant to time and still relevant to the fault location.

The flow of fault current through free-wheeling diodes in each arm of VSC is determined by voltage and resistance (R_D) across each diode. Hence, diode current is a function of AC side phase voltage, v_j , impedance voltage, v_Z , and diode resistance, which can be expressed as a function as:

$$i_D = f(v_j, v_Z, R_D) \quad (3)$$

During a DC fault, the AC feed-in current through the diodes can be obtained with a switching model in Fig. 2 and is illustrated in Fig. 3. It can be observed that the AC feed-in component is dependent on time. Hence, the dependency of AC fault current on time has a direct influence on AC side fault contribution towards the DC side. This fault current contribution from AC side varies signal characteristics at each instance and induces extra intricacy in locating fault accurately.

By varying the timing of the same DC fault, the faulty behaviour can be obtained as Fig. 4 shows. It can be seen that the profile in the first 10 ms (a typical data window for the data-driven method) are different when the fault timing is changed from $t = 0.3$ to 0.301 . This variation is caused by the time-variant nature of the AC voltage, which can directly cause variation of the result of fault-locating. This variation can be more significant when the fault is less severe and the time-consistent component becomes less significant. On the contrary, once the AC current is excluded, both profiles are almost identical in the first 10 ms, which is illustrated in Fig. 4 as well.

A. Exclusion of Source Current Contribution

Taking advantage of the fast sampling capability of a power converter, the prospected currents and voltages can be continuously sampled and monitored in every control cycle e.g. every $1/5000$ second. By embedding voltage measurement across the middle point of each arm within a power converter, the diode current can be determined instantaneously after the converter has been blocked during

the fault. Based on this, an AC current exclusion scheme is developed in this section.

Given the symmetry of 3 phases, phase a is used to illustrate the developed scheme. Considering the schematic of the diode arm in Fig. 5, the route of phase- a current is determined by the bias of both diodes. If phase a current, i_a is greater than zero, the voltages v_a and v_Z will be compared to

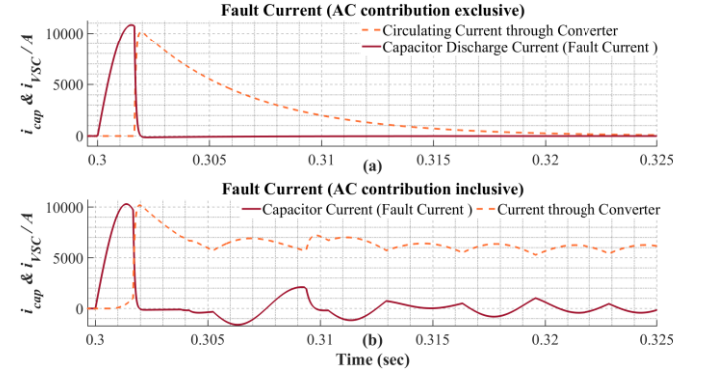


Fig.3. Fault currents with and without AC side contribution

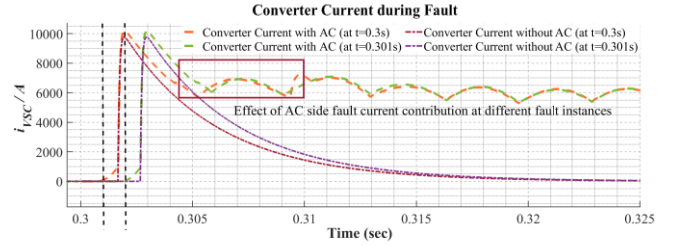


Fig.4. AC fault current contribution

check the biasing of the diode. If the voltage v_a is greater than $+v_Z$, diode D_1 conducts and i_a will be equal to the current through the diode. By implementing the forecited scheme in every control cycle, the AC contribution to DC current from phase a can be obtained in real-time and then deducted from the diode current detection, which is illustrated in Fig. 6. Fault current shown in Fig. 6 shows a converter current, where the AC fault current and circulating current generated by DC side are flowing together during fault at DC Side. In Fig. 6, i_{a-F} represents filtered current and i_{D1-M} illustrates the measured current flowing through the diode, D_1 .

$$i_{a-F} = i_{D1} = f(v_a, v_Z, R_{D1}) \quad (4)$$

By applying a similar scheme in all phase, the mechanism of source current exclusion can be summarized as follows:

Algorithm: Proposed Online Algorithm to filter AC side fault contribution

Step 1: Acquire phase current, i_j , phase voltage, v_j (where j represents phases a, b or c) at AC side, and line impedance voltage, v_Z at DC side.

Step 2: If the magnitude of i_j is greater than zero, go to the next step, otherwise start again.

Step 3: If v_a is greater than v_z , this determines that the acquired sample of current passes through diode $D1$ (upper arm diode). The acquired sample is the filtered fault current contributed by phase a through $D1$. Compare the filtered current with the measured current through diode $D1$ for any error.

Step 4: If v_a is less than v_z , this determines that the acquired sample of current passes through diode $D2$ (lower arm diode). The acquired sample is the filtered fault current contributed by phase a through $D2$. Otherwise, terminate the comparative analysis and start again. Compare the filtered current with measured current through diode $D2$ for any error.

Step 5: Filter the fault currents contributed by each phase and sum them all to acquire a total fault contribution from AC source.

Step 6: Calculate Error

Step 7: End procedure

i_{e2} shows the part of the filtered transient current which has been separated by using measured diode current and filtered current as

$$i_{e2} = i_{D1-M} - i_{a-F} \quad (5)$$

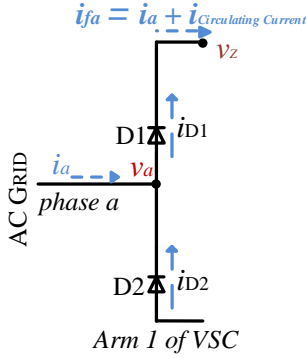


Fig. 5. Fault current and AC side current flow during Stage (III) through arm 1.

The extracted signal can be seen in Fig. 7. The figure represents the filtered circulating current through $D1$ that flows in the converter after the capacitor-discharge, discussed earlier.

This clearly demonstrates that the fault current contribution from the AC side has been filtered out effectively and can be used in further evaluation. Similarly, AC side contribution from phase b and phase c can be filtered out using the same methodology. By filtering AC fault current from each arm of VSC, total circulating current through VSC (i.e. without AC fault current) can be calculated as:

$$i_{E-VSC}(t) = i_{D1} + i_{D2} + i_{D3} \quad (6)$$

Total circulating current through converter after filtering the AC feed-in current is shown in Fig.8.

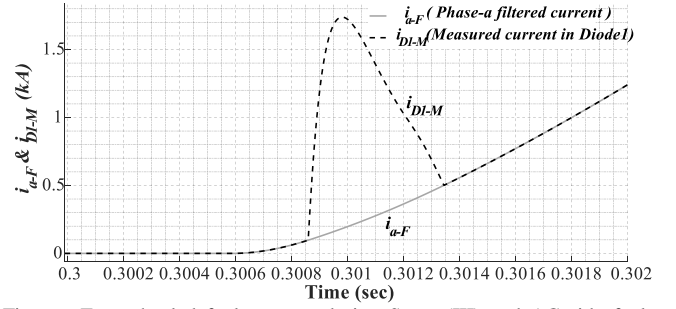


Fig. 6. Free-wheeling fault current during Stage (III) and AC side fault current through arm 1.

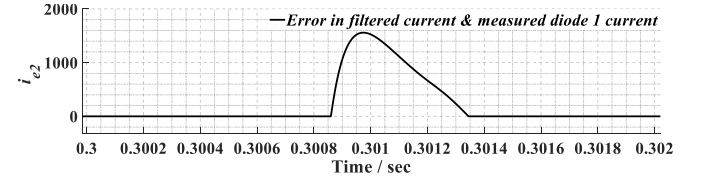


Fig. 7. Currents after filtering out AC side contribution

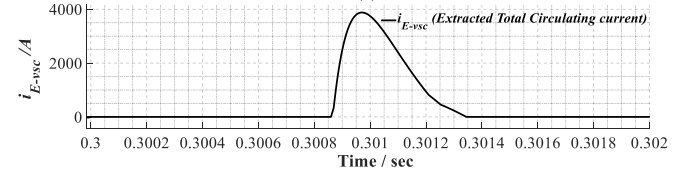


Fig. 8. VSC filtered free-wheeling circulating current

IV. ANN BASED FAULT LOCATION TECHNIQUE

To avoid the mathematical complexity of solving a circuit of a high order, a data-driven method, ANN, is introduced in this section.

A. Artificial Neural Network-Fault Locating (ANN-FL) Algorithm

ANN has the ability to establish a non-linear mapping between input data set and output variables by appropriately selecting the number of layers and neurons. With pre-collected data of a certain system, a cascaded multi-layered network can be built, where the output of one layer is fed into another. Each layer is being associated with its specific weight matrix ' ω ', a bias vector ' β ', an input vector ' η ' and an output vector ' o ' [24], which summarized the characteristic of the target system.

Using feedforward three-layered (1-Input and 2-Hidden layer) ANN (ANN-FL) [25], the number of neurons for the input layer is set equal to the input variables. This layer process input signals to ANN and sends an output signal from each layer to calculate weights and biases.

Proposed ANN-FL uses hyperbolic tangent transfer function (as demonstrated by (7)) in its hidden layers to analyze system conditions and make decisions appropriately [24]. The number of neurons can be selected accordingly in these layers, where the processing power of ANN is proportional to the number of neurons.

$$H = \text{Tansig}(x) = [2/(1 + e^{-2x})] - 1 \quad (7)$$

Fifteen neurons are selected for hidden layer-1 and 4 neurons for hidden layer-2 for the ANN-FL. Less number of

neurons are selected to keep the computational time as low as possible while maintaining the appropriate fault locating accuracy of the network. Finally, hidden layers process the data and send it to the output layer after transforming results in appropriate value i.e. the location of the fault in this case.

Data of circulating fault current through VSC is gathered to create a database for different fault locations from $d=10\%$ to $d=100\%$ (with steps of 10%) of the cable length. This database matrix is used to train ANN-FL. Training of ANN-FL has performed with Error Back Propagation (EBP) technique by the Levenberg-Marquardt (LM) [26] algorithm considering the 1000 number of iterations in the training epoch. Pseudo-code for proposed ANN-FL method for locating fault is described as:

Algorithm: Proposed Artificial Neural Network-based Fault Location Method

```

1: Input: feature  $I_f$  from actual data
2: Linearization of data
3: Initialization
4: for  $1 \rightarrow K$  do
5:   Load ANN
6:   Train ANN-FL Model
7:   Calculate Mean Square Error (MSE)
8:   if  $MSE > \text{Threshold}$ , then
9:     Adjust weights
10:  else
11:    Save weights
12:  end for
13: Test ANN-FL Model for fault Location
14: Calculate Error
15: end procedure

```

B. Case Studies

A radial network of DC microgrid supplied by a VSC is established in MATLAB-Simulink based on parameters given in Table-I.

1) *Neural-Network Training Process:* For illustration, the fault resistance is set to 100% of the system's nominal resistance i.e. fault resistance, R_f to be $7.2 \text{ m}\Omega$. Data samples of circulating fault current through VSC is gathered to create a database for different fault locations from $d=10\%$ to $d=100\%$ (with steps of 10%) of the cable length.

With a 2-dimensional output of both fault resistance and fault location, ANN is trained for the data collected for different fault locations, locating fault with 10% increment of a cable length where the total length of the cable is taken as 1000m with a data window of 10 ms at a resolution of 1 ms after the fault occurs.

Data samples collected for each fault location are being given as input $\eta = (\eta_1, \eta_2, \eta_3, \eta_4, \dots, \eta_{10})$ to the network, as shown in Fig. 9, for training purposes. The training process of the network is based on the forward propagation of fault current input samples and backpropagation of errors. Continuous adjustment of weights and biases is made by comparing the desired output with calculated values using error backpropagation. This process of training ANN tries to achieve the accuracy requirement between the real output

and estimated output and thus develops a correlation between the fault current and fault location.

The training of this 2-layered ANN with (10×1000) input matrix, 15 neurons in first layer and 4 neurons in second layer is achieved in 11 mins and 35 secs.

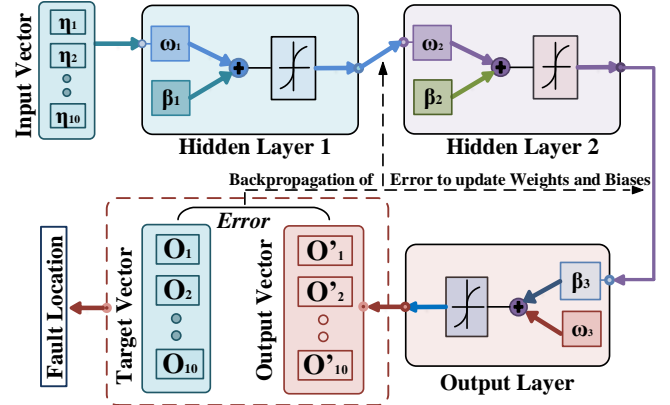


Fig. 9. Fault Locating ANN Structure

2) *Neural-Network Testing Phase:* After the ANN has been trained, it is ready to use for locating fault online. Keeping the fault resistance constant, the trained network is tested with various fault locations over a DC feeder of 1000m supplied by a 3-phase VSC and fault timing of $t = 50 \text{ ms}$ and $t = 51 \text{ ms}$, respectively. The protection of VSC is considered to be based on overcurrent protection and it is blocked one step further, as the circuit breaker is not closed immediately. The results are shown in Fig. 10.

Test results (in Fig. 10) for estimating fault location without blocking the AC side current illustrates a higher degree of inaccuracy in fault localization with AC side fault contribution. Moreover, the impact of time-variability becomes obvious when the fault location (including AC side fault current contribution) is estimated after the fault initialization at $t = 51\text{ms}$. Estimation error increases to a higher value with an average increase of 4% by varying the time of fault as the fault current contribution of each phase varies accordingly.

The robustness of developed methodology for locating fault is tested by first filtering the AC fault current contribution with fault initiated at $t=51\text{ms}$. Results in Fig. 10 clearly demonstrate that estimation error for the filtered fault current overlaps the results tested for without AC current contribution when fault initiated at $t=50\text{ms}$. Fig. 10 illustrates that the fault estimation accuracy is between $\pm 2\%$ between 230m to 750m of fault which confirms the efficiency of the technique.

Discussion: The fault locating result at the front and end side is relatively less accurate, as the fault estimation error varies from $\pm 4\%$ to 8% . The accuracy at these points can be improved by enhancing the resolution of the data window. Since this is not the focus of this paper, the result is not further discussed considering page limit. Since the illustrated fault timing variation is only 1 ms whereas the grid frequency is

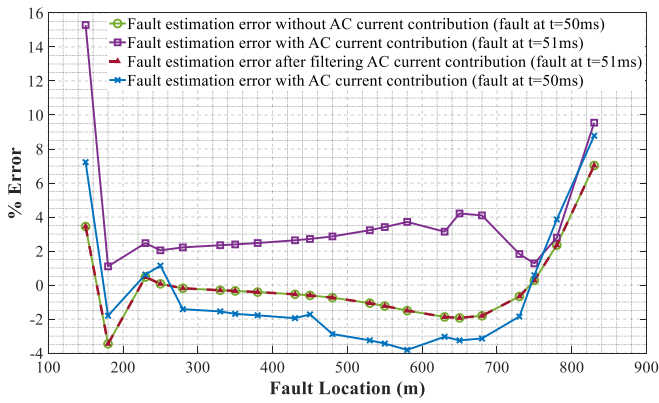


Fig. 10. Fault location estimation error at random locations

50 Hz, it can be anticipated that the robustness and accuracy can be further deteriorated when the time variation is between 1ms and 19 ms when the input data is not refined. Although it is possible to improve accuracy without exclusion of AC contribution by introducing an extra dimension of phase angle in the ANN training, it will significantly add up to the complexity.

V. CONCLUSION

In this paper, the ANN-based online fault locating method for LVDC system is proposed. By analytically refining input data, the proposed method demonstrates a clear advantage over those “black box” approaches when applying a data-driven method to locate a fault. The proposed technique is proved to be able to locate a DC fault using real-time local measurements and hence can be embedded in a power converter. By incorporating the proposed scheme of AC current exclusion, the accuracy can be improved. In addition, this method can significantly improve the robustness against the variation of fault timing.

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