A Multifunctional Integrated Circuit Router for Body Area Network Wearable Systems

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Abstract—A multifunctional router IC to be included in the nodes of a wearable body sensor network is described and evaluated. The router targets different application scenarios, especially those including tens of sensors, embedded into textile materials and with high data-rate communication demands. The router IC supports two different functionality sets, one for sensor nodes and another for the base node, both based on the same circuit module. The nodes are connected to each other by means of woven thick conductive yarns forming a mesh topology with the base node at the center. From the standpoint of the network, each sensor node is a four port router capable of handling packets from destination nodes to the base node, with sufficient redundant paths. The adopted hybrid circuit and packet switching scheme significantly improve network performance in terms of end-to-end delay, throughput and power consumption. The IC also implements a highly precise, sub-microsecond one-way time synchronization protocol which is used for time stamping the acquired data. The communication module was implemented in a 4-metal, 0.35 μm CMOS technology. The maximum data rate of the system is 35 Mbps while supporting up to 250 sensors, which exceeds current BAN applications scenarios.

Index Terms—Integrated circuit, body area network, wearable sensor network, hardware implementation, digital circuits, routing.

I. INTRODUCTION

WEARABLE electronic systems with embedded computing and sensing devices provide a platform for continuous monitoring of physiological signals in sports and health care, as well as for supporting people exposed to high

risk work environments [1]. By fully embedding electronic devices in the textile fabric, the quality of the Wireless Body Area Network (WBAN) will improve while also expanding the acceptance of smart textiles [40], [41].

Conductive yarns or copper wires have been used to provide the electrical connections [12] within a wired network of sensors embedded in textile. The electrical characteristics of conductive yarns are not exactly those of normal wires. They exhibit much higher impedance in comparison to copper wires and significant variation in their electrical properties between relaxed and stretched modes. In addition, the connections are subject to wear and tear due to use and washing. Therefore, data transmitters and receivers must be tolerant to both catastrophic and parametric faults.

Wearable Body Sensor Networks (WBSNs) are distributed systems in which each sensor node acquires data from the body. In most applications, the network is organized in a bus, star or mesh topology. For small numbers of sensors, a bus or star topology is a suitable choice. However, the single node connections seen in these configurations, together with the vulnerability of conductive yarns to wear and tear, make these topologies more prone to failure. When the number of sensors increases, a mesh network provides better performance. Also, in these network typologies, each node is usually connected to several other nodes, leading thus to more than one connection being available in the case of failure, whilst leading to longer system lifetime. Besides, the data rates in mesh and star cases are higher than in bus topologies.

The authors of [11] and [5] introduced an Field Programmable Gate Array (FPGA)-based implementation of the packet-switching router for a mesh WBAN, which was designed to capture electromyography signals and movement information from the lower limbs. In the present work, an enhanced version of that router implemented as an Application-Specific Integrated Circuit (ASIC) designed in Complementary Metal Oxide Semiconductor (CMOS) technology, is presented that supports circuit, packet and hybrid switching for mesh-topology WBSNs. The proposed circuit improves the performance of the system by decreasing end-to-end delay, and energy consumption. An independent time stamping circuit based on a highly precise time synchronization protocol [7] is also included in this ASIC. The main contribution of this paper is twofold:

1) Customized hardware implementation of a hybrid circuit and packet switching mechanism for WBSNs.
2) A low-power router design for use in sensor and base nodes.

The Integrated Circuit (IC) implements a transmitter, a receiver, the network layers up to the routing layer, a Serial Peripheral Interface (SPI) port, support for hybrid switching, time synchronization and data rates up to $35\,\mathrm{Mbps}$.

The remaining of the paper is organized as follow: Section II presents an overview on related work on ICs for WBSN applications. The motivation for designing the new IC is addressed in Section III. Section IV presents the wearable system architecture. The functionality of all IC modules is presented in Section V. Section VII presents and discusses the experimental results, followed by the discussion of the main conclusions in Section VIII.

II. RELATED WORK

Different solutions for wearable sensor networks have been proposed in the last years. In [36] a self-configured body sensor network controller and a high-efficiency, wirelessly-powered sensor for a wearable, continuous health monitoring bandage system is presented. The sensor chip consumes $12\,\mu\mathrm{W}$ to implement an Electrocardiography (ECG) analog front-end and an Analog to Digital Converter (ADC). It harvests power from the surrounding health monitoring band using an Adaptive Threshold Rectifier (ATR) with 54.9% efficiency. The ATR is implemented in a standard CMOS process. The adhesive bandage comprises the sensor chip, a Planar-Fashionable Circuit Board (P-FCB) inductor and a pair of dry P-FCB electrodes. This kind of dry electrodes enables long term monitoring without skin irritation. The integrated network controller automatically locates the sensor position, self-configures the sensor type, wirelessly supplies the configured sensors, and exchanges data only with the selected sensors while dissipating $5.2\,\mathrm{mW}$ from a single $1.8\,\mathrm{V}$ power supply. The sensor and network controller chips occupy $4.8\,\mathrm{mm}^2$ and $15\,\mathrm{mm}^2$, respectively, in standard $0.18\,\mu\mathrm{m}$ CMOS.

In [17], a circuit for efficient data acquisition from sensor networks with a large number of nodes is proposed. The design allows for simple device connections in a daisy-chain SPI network configuration. Such a networking method, eliminates addressing problems and allows synchronized sampling design by using just 4 wires. The associated experimental setup demonstrates its ability to acquire data from up to 200 sensors, but with only $50\,\mathrm{Hz}$ sampling rate using conventional low-cost hardware. In consequence, a very low data rate and a significant amount of power consumption, due to all nodes being involved in the data delivery, are the main drawbacks of the proposed solution.

The authors of [31] present an analog receiver front-end based on intra-body communication topology, which is able to transmit at data rates of $2.5\,\mathrm{Mbps}$ and $5\,\mathrm{Mbps}$, and a transmission distance of $170\,\mathrm{cm}$. To verify the receiver, a discrete circuit was designed, fabricated and tested. The circuit was also applied to an FPGA-based audio player to produce a data stream. The data was transmitted from one hand, through the body, to the other hand. Sensor nodes were attached by means of a transmitter/receiver electrode to the skin surface. As the transmitter and receiver work with independent clocks, an asynchronous serial frame with start bits and end bits is used. The total power consumption is $69.44\,\mathrm{mW}$ at $2.5\,\mathrm{Mbps}$.

A low-power and self-reconfigurable WBAN controller circuit with Branched Bus (BB) topology and Continuous Data Transmission (CDT) protocol for wearable health care applications is proposed in [21]. The BB topology and CDT protocol are a combination of conventional bus and star topology and a variation of the TDMA protocol, respectively. They are able to compensate for the electrical faults in bio-signal monitoring systems caused by the misoperation of the electrodes. The overall chip area is $1.5\,\mathrm{mm}\times0.95\,\mathrm{mm}$, including all pads, and was fabricated in a $0.18\,\mu\mathrm{m}$ CMOS technology.

The authors of [13] address transceivers and a wireless power delivery system for a Body Area Network (BAN) system that uses an e-textile-based physical layer capable of linking a diverse set of sensor nodes. A central base node controls power delivery and communication resource allocation for every node using an on-chip Node Network Interface (NNI). The network architecture is fault-tolerant, reconfigurable and easy to use through a dual wireless-wireline topology. The nodes are powered at a maximum end-to-end efficiency of 1.2% and can transmit at a peak data rate of $1\,\mathrm{Mbps}$. While transferring power to a single node, the base node consumes $2.9\,\mathrm{mW}$ power and the node recovers $34\,\mu\mathrm{W}$, of which $14\,\mu\mathrm{W}$ are used to power the network interface circuits, while the remaining power is used to power the signal acquisition circuitry. Fabricated in $0.18\,\mu\mathrm{m}$ CMOS technology, the base node and the NNI occupy $2.95\,\mathrm{mm}^2$ and $1.46\,\mathrm{mm}^2$ area, respectively.

A digital active electrode (DAE) system for multi-parameter biopotential signal acquisition in portable and wearable devices is presented in [33]. A custom designed IC performs local analog signal processing and digitization with the help of on-chip instrumentation amplifiers, a 12-bit ADC, and a digital interface. Up to 16 digital active electrodes (15-channels) can be connected to a commercially available microcontroller via a standard Inter-Integrated Circuit ($\mathrm{I}^2\mathrm{C}$) bus. The DAE uses a DC-coupled amplifier to preserve the input DC signal, while still achieving state-of-the-art performance: $60\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ input-referred noise and $350\,\mathrm{mV}$ electrode-offset tolerance. The adopted common-mode feed forward scheme improves the Common Mode Rejection Ratio (CMRR) of a DAE pair from $40\,\mathrm{dB}$ to $102\,\mathrm{dB}$.

A power and data transfer network on conductive fabric material, which is based on the $\mathrm{I}^2\mathrm{C}$ protocol is proposed in [26]. In this system, $\mathrm{I}^2\mathrm{C}$ data are transferred to tiny sensor nodes distributed on a double-sided conductive textile along with DC power supply using a scheme based on frequency division multiplexing. Two carriers are modulated with the clock and the data signals of $\mathrm{I}^2\mathrm{C}$. The authors have proposed a special filter to enable passive modulation. Two carriers at $20\,\mathrm{MHz}$ and $50\,\mathrm{MHz}$ have been used for transmitting the Serial Data Line (SDA) and Serial Clock Line (SCL) signals at a data rate of $100\,\mathrm{kHz}$.

Each of the systems introduced in this section have their own advantages and disadvantages and they have been used in practical applications. However, there are still many things that need to be improved for new applications. The systems presented in [13], [31], [33], [36] include only a few sensors. In contrast, those proposed in [17], [21], [26] are capable of supporting more sensors but in practice they may not exceed several tens of sensors due to the increased load on the communication line which reduces the communication speed and increases the power consumption as well. The circuit presented in this article can support up to hundreds of sensors without slowing down the communication speed. As with any multi-hub network, the power consumption of the entire system is not as good as single-hop such as star topology. However, improvements were introduced to reduce the power by optimizing the routing and using different switches. For the prototype circuit, a CMOS $0.35\,\mu m$ technology was used. Using advanced CMOS technologies can be very effective in reducing power.

III. MOTIVATION

One of the characteristics of BANs in general is the limited number of nodes they have. However, due to the growing use of this type of systems in many medical and non-medical fields, the number of nodes per system is also increasing. Currently, the use of wireless sensors or conventional star or serial bus topologies meets the needs of many BAN applications with just a few nodes. Wireless technologies such as WiFi are capable of transmitting tens of megabytes of data. But increasing the number of nodes, due to channel sharing and interference, their performance will be reduced and power consumption will be significantly high for battery driven systems. In contrast, wired networks are more immune to interference, nodes have a direct connection to each other, and typically use much less power to transmit a certain amount of data. Therefore, when the number of sensors is high, a suitable method is to use a wired network between the sensors, which will eventually collect data and transmit through a single wireless node to a computer. The circuit proposed in this paper was developed in the context of the ProLimb project [27], whose sensing and network solutions require tens of sensors embedded in textiles. The BANs being proposed is based on a mesh topology and supports applications that require a large number of sensor nodes. Due to the fixed location of the sensors on the body and the use of a textile substrate, the embedded sensors are connected to each other by means of embroidered conductive yarns. These characteristics, together with appropriate protocols and communication circuits, facilitate optimizing the achievable data rate and throughput, with characteristics of low-power and better reliability.

IV. WEARABLE SYSTEM ARCHITECTURE

The system includes a wearable infrastructure and an on-body Central Processing Module (CPM), which is in connection with a computer via a wireless link as shown in Figure 1. The wearable infrastructure includes a set of
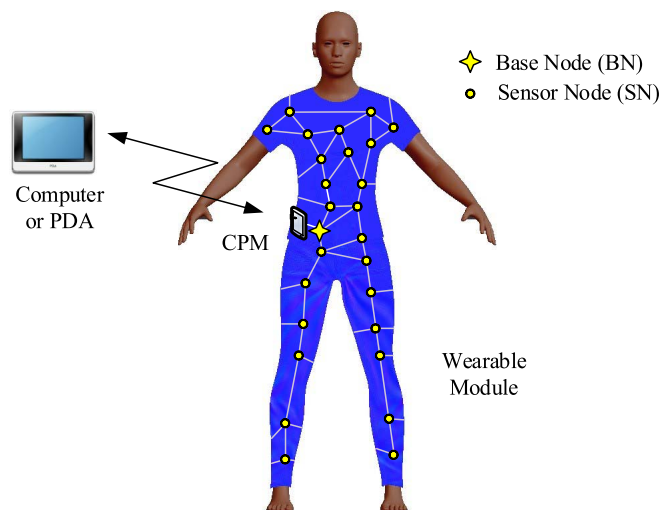

Fig. 1. General architecture of the system including; 1) wearable infrastructure, 2) CPM, 3) computer or PDA.
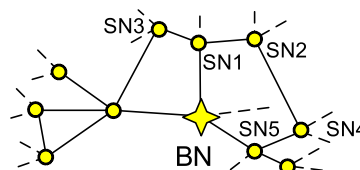

Fig. 2. A mesh network of sensors embedded in textile.

Sensor Nodes (SNs) equipped with Electromyography (EMG) electrodes for capturing electrical signals from skin surface, and also accelerometers and gyroscopes for measuring kinetic and kinematic parameters. The Base Node (BN) node is responsible for collecting all data captured by SNs and relaying it to the CPM. Each SN acts as a router device to handover packets from the source SN to the BN. The CPM, as an on-body low-power wireless device, gathers data from the wearable network via a communication link to the BN module and transfers the collected data to a computer or a Personal Digital Assistant (PDA). The network structure and layers are described next.

A. Network of Sensors Embedded in Textile Substrate

The intra-network in wearable systems is made of a set of SNs and the BN node, all connected to each other by conductive yarns in a mesh topology, as shown in Figure 2. Each SN provides connections to its neighbor nodes. In case of link failures, each SN maintains the capability of establishing communication via the BN alternative paths.

B. Physical Layer

The communication media among SNs is implemented with conductive yarns. The type of yarns adopted here present an impedance of about a few Ω/cm, a value which is much higher than that presented by copper wires, but provides enough conductivity to implement reliable and isolated communication between nodes. Baseband communication signals coded with
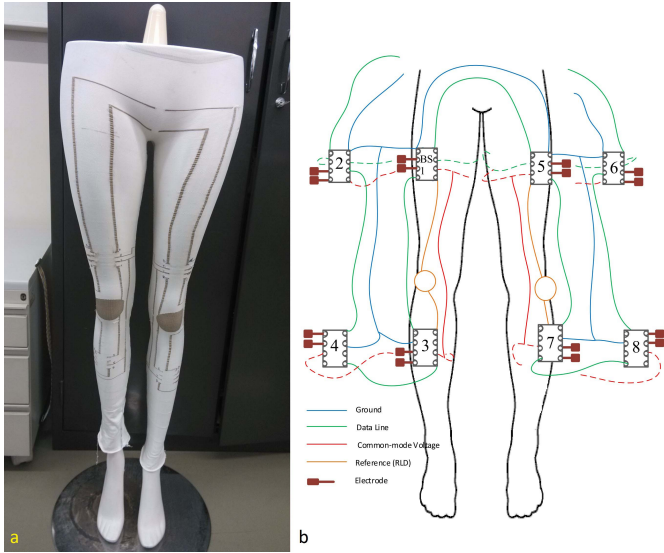
Fig. 3. a) E-legging for capturing human locomotion, b) Interconnection diagram of wearable platform [adapted from [14]].
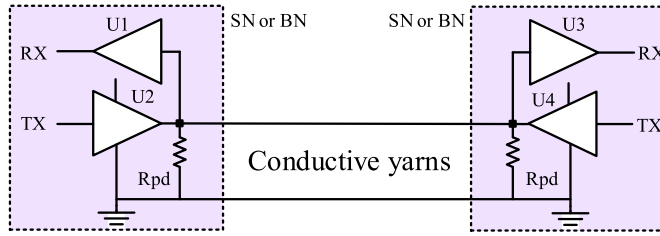

Fig. 4. Connection between the nodes in physical layer including SN-to-SN and SN-to-BN.

Non Return to Zero Inverted (NRZI) coding, to flexibly select either AC or DC coupling, are used.

Figure 3.a shows a flexible wearable textile BAN for gait analysis developed in the ProLimb project [27]. Figure 3.b illustrates the sensor interconnections which use a mesh topology. The prototype uses conductive yarns with resistance R = 1.5Ω/cm and inductance L = 8 nH/cm. The woven conductive yarns can be clearly seen on the garment. In order to decrease the impedance, each line is composed by 10 yarns in parallel.

To avoid the use of separated lines for transmitting and receiving, and also to reduce the complexity of the yarn network that must be embedded in the fabric, the communication between SNs uses bidirectional communication, as shown in Figure 4. A parallel to serial shift register drives the TX. In this figure, U2 and U4 are tri-state buffers and Rpd is a pull-down resistor. A mechanism is included in the circuit for detecting and avoiding collisions that may occur.

C. MAC Layer

Sharing the communication medium implies, however, a Media Access Control (MAC) protocol at the data link layer to manage the access [18], [37]. Selecting a MAC protocol depends on system requirements. In BAN applications, reliability, line sharing, and energy efficiency are important features to take into account. To achieve the aforementioned features
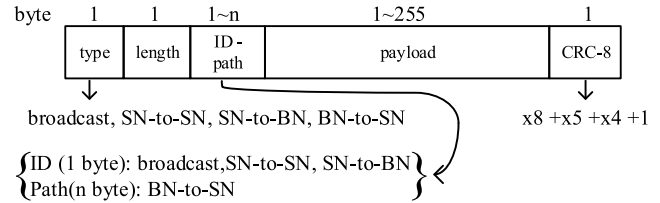

Fig. 5. Format of packets.

in the present system, communication at the MAC layer is controlled by a RTS/CTS handshaking mechanism. In order to efficiently manage the requests, the sender and receiver nodes should be aware of the status of each other. Otherwise, a significant number of data packets may be lost, requiring retransmission. The use of RTS/CTS handshaking helps to ensure reliable communication with low packet loss if used with an appropriate resource management mechanism.

D. Routing Layer

To establish end-to-end communication in a multi-hop topology, a routing protocol is needed. In this work, the Source Routing for Minimum Cost Forwarding (SRMCF) protocol has been used, which is a reactive, energy-efficient routing protocol for both wired and wireless wearable sensor networks [10]. This protocol is based on Source Routing (SR) concepts [15], [39] for *ad hoc* networks and Minimum-Cost Forwarding (MCF) [34] methods for heterogeneous Wireless Sensor Networks (WSNs). SNs maintain no information about the network topology, but packets (sent from SNs to BN or vice-versa) always transit over paths with minimum cost. In this approach, only the packets from the BN to SN include routing information [19], [39]. The proposed protocol is intended for application scenarios where the availability of limited resources requires the energy consumption to be kept at low levels. Under SRMCF, the BN starts to setup the network by broadcasting its cost value and all SNs obtain the minimum cost value to reach the BN. In this phase, each SN is assigned a minimum cost value, together with the port connected to the adjacent SN on the minimum cost path to the BN; this adjacent node is called the *near-node*.

Besides the routing protocol, which is used to determine all routing paths, the switching methods have to be defined. The proposed IC architecture is able to support packet, circuit or hybrid switching methods. The flexibility of selecting switching methods increases the range of applications.

1) Routing by Packet Switching: Packet switching or store-and-forward method is used in most of *ad-hoc* networks. However, buffering packets in intermediate nodes aggravates the end-to-end delay and also increases power consumption due to the extra packet processing needed for routing [30]. Figure 5 depicts the packets format. The field *type* determines the packet type and *length* is the payload size in bits. The payload can be any kind of data, such as sensor information and time stamps. The value of *ID-path* depends on the packet sender. In case of packet transmission from BN to any SN, it contains path information, otherwise the ID of the packet sender.

Each packet carries a CRC-8 checksum in trailer for detecting transmission errors. The utilized polynomial is the same as that used in the standard 1-Wire protocol.

2) Routing by Circuit Switching: One of the methods that can overcome the drawbacks of packet switching is circuit switching at the MAC layer, because it is a bufferless method. In bufferless networks, such as optical networks or some Network-on-Chip (NoC) architectures, a packet arrives at the destination node over intermediate nodes without any buffering [2], [16], [25], [38]. This approach usually reduces the total network power consumption and delay under low network workloads, but routing performance for randomly generated packets is significantly worse when compared to packet switching for high network workloads. In fact, a bufferless algorithm without communication scheduling at the nodes may be significantly ineffective. The system performance by scheduling of the nodes is better than packet switching, and close to ideal network performance. A scheduling mechanism is included in the proposed IC.

3) Routing Hybrid Packet and Circuit Switching: The IC being proposed supports SN-to-BN, BN-to-SN and node-to-node (just neighbors) communication, and also broadcasting messages originated by any node. When the network is set to work with packet switching, all the aforementioned types of communication perform normally, but in case of circuit switching different rules must apply. The issue is that, although circuit switching can be used in the SN-to-BN case, other types of communication support only packet switching. Hence, the network has to work in a hybrid mode to support both switching modes without or, at least, with minimum, system performance degradation. In this way, the system can benefit from advantages of circuit switching. This IC is also able to handle packets from any SN to the BN with a combination of circuit and packet switching.

E. Recovery of Link or Node Failures

In wired networks with star or bus topologies, there is no failure recovery mechanism. Failure consequences are worse for bus topologies, because, in this case, all nodes will be affected after a link failure. In contrast with star or bus topologies, the mesh topology is more robust to faults, as each node may have several redundant links to use in case of any link or node failure. A fault-tolerant wearable system based on a mesh topology is presented in [35]. In this system, the fault-finding phase is only executed when the system is reset.

In the proposed IC, recovering from a link or node failure involves updating the cost value field. The method used by SRMCF is explained in [9]. Unlike [35], the fault-finding process runs continuously during normal system operation. For the purpose of failure recovery, each node monitors the activity of its near-node (e.g. in Figure 2, SN2 and SN3 monitor SN1). If no activity is observed for a specified amount of time, the near-node initiates the recovery procedure by broadcasting cost request messages periodically until finding another available path. For example, if the link between SN1 and SN2 fails then SN2 will consider SN4 its near-node.
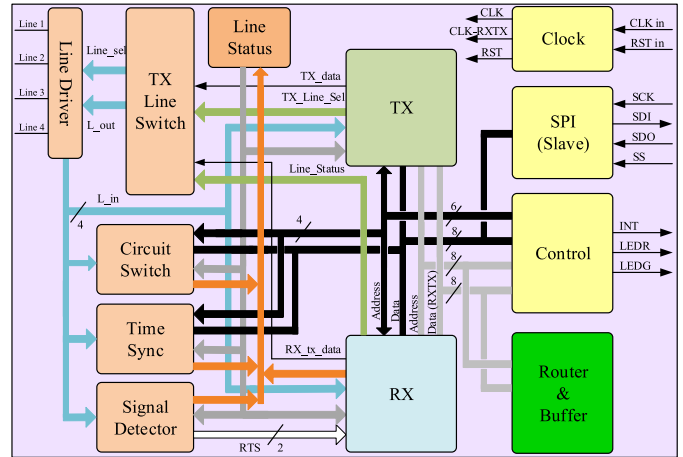

Fig. 6. Block diagram of the router IC including all submodules and main interconnections.

F. Scalability

A set of sensors is able to form any arbitrary network. The hop count, which is the number of links between a node and the destination node, depends on the node arrangement. For each number of nodes, the value of hop count is upper and lower bounded. The upper bound (H_{max}) occurs when all nodes are arranged in a line with the source node at one end and the destination node at the other end, which is equal to the number of nodes. For the lower bound (H_{min}), consider a network composed of N sensors and a sink node BN in the middle as shown in Figure 3. Assume that all sensors and also the *BN* have K ports. In [4], it is calculated that the value of H_{min} is given by

$$H_{min} = \left\lfloor 1 + \log_{K-1} \frac{(N-1)(K-2) + K}{K} \right\rfloor \qquad (1)$$

With the given values, for example with 250 4-port sensors, many combinations can be considered leading to hop count values in a range from 5 to 250. The circuit is capable of sending data between sensors and the BN with any hop-count, size, and node arrangement.

V. Integrated Circuit for Node Communication

The block diagram of the complete integrated routing circuit is shown in Figure 6. It includes the implementation of a hybrid packet/circuit routing protocol in hardware and a highly precise time synchronization circuit. Each IC has four ports and one Clock and Data Recovery (CDR) circuit per port. (The choice for the number of ports per node is justified in [4]). A very small fully-digital circuit CDR was designed, which is described in Section V-A. The IC requires four such circuits because it is meant to be able to run several asynchronous communication tasks simultaneously.

The IC communicates with a microcontroller via a SPI interface. The routing operations could be implemented on the microcontroller, but to reduce packet serving time and power consumption, the IC provides itself the routing from SNs to BN. Such an implementation significantly reduces power consumption and end-to-end delay.

To reduce the circuit power consumption, during idle time, the internal *Clock* module puts all the other modules except *Time sync* in sleep mode (disabled clock). The reception of any preamble signals or any SPI communication wakes up the system. At the end of any task, the system immediately returns to sleep mode. Further power savings can be obtained if time synchronization is not activated. The following subsections explain the functionality of each submodule.

A. Clock Synchronization and Data Recovery

Many CDR methods have been designed and discussed in the literature [22]–[24]. In [8], an open-loop, low-complexity, very small size, fast-lock synchronization circuit for clock and data recovery in wearable systems is proposed, which is also utilized in the current IC.

From the standpoint of the network, each SN is a four-port router with bidirectional links to other SNs. The SNs are equipped with a local crystal oscillator. When sensors communicate, the receiver node must be able to synchronize its clock to the incoming data. Due to the lack of global synchronization, a local synchronization method is necessary. The following aspects have been taken into account in the design of the clock synchronization circuit:

- *Size:* Each SN has four independent CDR circuits and it is important to have small circuits.
- *Energy consumption:* Sensor nodes are typically energy-limited systems.
- *Bandwidth:* In comparison to copper wires, conductive yarns exhibit higher electrical impedance, leading to significant signal attenuation with increasing frequency. This drawback leads to adopting communication mechanisms or modulations that operate with reduced bandwidth.
- *Internal node synchronization:* Even if precise clock recovery is achieved, synchronization between the system core and the recovered clock signal should be taken into account.

Figure 7 shows the block diagram of the clock synchronization circuit. In this figure, $r(t)$ denotes the incoming signal, $C_2(t)$ the local oscillator, $C_r(t)$ the recovered clock and $m_r(t)$ the detected (received) message. The CDR circuit keeps the phase difference $\Delta\varphi(t)$ between an incoming signal and the recovered clock in the range

$$\frac{-\pi}{2} < \Delta\varphi(t) < \frac{\pi}{2}. \tag{2}$$

The synchronization circuit consists of eight logic gates in total, making it small enough for four instances being included in the communication ASIC. Each CDR circuit occupies only $0.0022\,\mu\mathrm{m}^2$ when implemented in a $0.35\,\mu\mathrm{m}$ CMOS process.

B. Time Synchronization

A synchronization method, such as a network protocol or dedicated hardware, is necessary to establish time synchronization with an acceptable accuracy [20], [28], [29], [32]. A fully digital circuit for one-way master-to-slave, highly precise time synchronization, in a low-power wearable system equipped
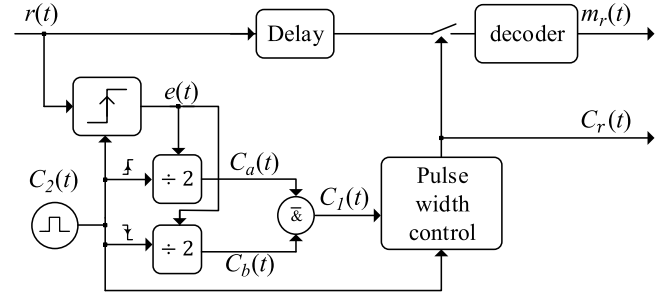

Fig. 7. Block diagram of the clock synchronization circuit (adapted from [8]).

with a set of sensor nodes, has been proposed in [6], [7]. This digital circuit is also employed in this work.

C. Router and Buffer Module

To ensure good routing performance of the nodes in both directions (SNs to BN and vice versa), the SRMCF protocol is used as discussed before. For that purpose, a router module (provided with direct access to the buffer inside the IC) is added to the circuit. The buffer memory is shared via a SPI port with the microcontroller, which is able to access the packets stored in it. This module starts serving the packets as they are placed in the buffer, either received by the *RX* module or generated by the node itself. The router is connected to the *data bus* and reads or writes data from the buffer like the other modules. This way of handling packet routing avoids involving the microcontroller in the routing process for the most frequent cases, decreasing significantly both power consumption and end-to-end delay (Sections VII-A and VII-B).

D. Transmitter Module

The *TX module* is responsible for encoding the payload, encoding, generating of MAC messages, sending packets and transmission control. It is always responsible for starting packet transmission to the BN or to neighbor nodes. The type of switching depends on the destination and the *TX* module handles all of them. Depending on the switching mode, this module is able to generate *RTSnd* (node-to-base transmission) and *RTSnn* (node-to-node transmission) messages for circuit and packet modes, respectively. The *Encoder* submodule is responsible for generating the Request to Send (RTS) signals. Concerning the *RTSnn* mode, it generates the preamble signals followed by the *RTSnn* code; for *RTSnd* it also adds a *hop-count* field, whose initial value is one plus the CRC3 checksum, as shown in Figure 9.

E. Receiver Module

To control the communication and determine the end of the packet, a counter is loaded with the packet length at the beginning of a packet processing. It starts counting down while data is received. When the value of the counter reaches zero, the *RX* finalizes the reception. After a successful packet reception, *RX* changes the *Status* field of the buffer segment that contains the packet to inform the router that a valid packet was received.

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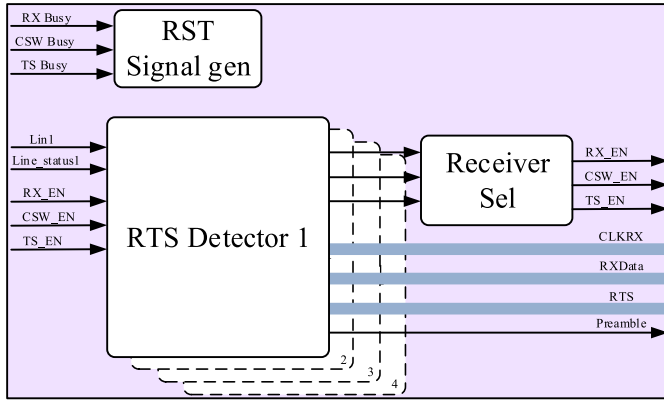

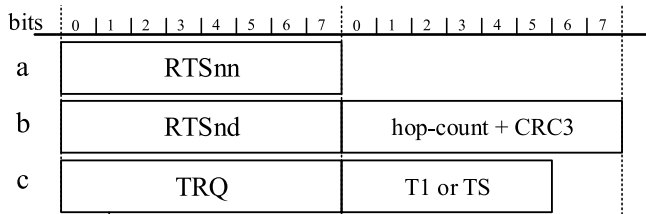Fig. 8. Signal detector module for tracking line activity.

Fig. 9. The three different types of RTS messages required by the SRMCF routing protocol: a) node-to-node, b) node-to-BN, c) time synchronization request.

F. Signal Detector

Figure 8 shows the *Signal Detector*, which comprises the *RTS Detectors*, *Receiver Sel* and *RST Signal gen* submodules. The MAC frames can be one of three different kinds: packet switch, circuit switch and time synchronization. In this context, an RTS message carries more information than just being a request. The module *Signal Detector* performs a pre-detection and then selects the next module for handling the message, which can be *RX* (for packet switching), *CSW* (for circuit switching) or *Time Sync* for timing messages.

Any data exchange starts with an RTS message. The three possible types of RTS messages are shown in Figure 9:

1) *RTSnn*: This message is used to establish communication over node-to-node packet switching, and can be used for all types of communication: broadcasting, node-to-node, base-to-node or even node-to-base.
2) *RTSnd*: If a sender node wants to send a packet to the BN then it may request the intermediate nodes to establish a circuit path by sending a *RTSnd* message.
3) *TRQ*: Any node can send a timing request to its *near-node* node. The receiver node replies to the *TRQ* message with its time information. The details and analysis of the synchronization protocol and corresponding circuit implementation are discussed in [7].

To handle concurrent requests, each port is equipped with its own *RTS Detector*. For example, while receiving a packet by one port, a time synchronization request (*TRQ*) may be received by another port.

Figure 10 shows an example of SN-to-SN packet delivery from SNa as sender node to SNb as receiver; the example
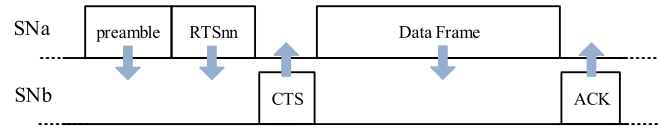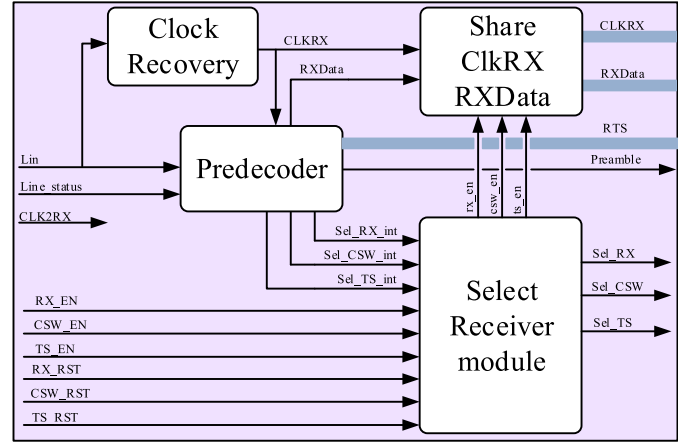

Fig. 10. SN-to-SN packet delivery.

Fig. 11. RTS detector module.

includes *RTSnn* which performs in fact RTS/CTS handshaking. The data frame can have any kind of data with size from 1 to 255 bytes.

At the end of a communication (packet reception, circuit switching or time message exchange), the *RST Signal gen* submodule generates internal reset signals to release the involved *RTS Detector*. For example, if the *RX* is receiving a packet from port 1, then at the end of reception, the signal *RX Busy* changes to low (deactivated), and *RST Signal gen* generates a pulse on *RX-RST* to release *RTS Detector 1*.

The *Receiver Sel* module generates enabling signals to select the responsible receiver. This module contains a ring counter that prevents the overlapping requests. For example, if two *RTSnn* requests are received simultaneously from ports 2 and 3, then the *RX* module is able to receive from either port 2 or 3. In this case, *Receiver Sel* selects either port 2 or 3, and releases the other one.

The *RTS Detector* module is shown in Figure 11. In idle mode, the status line indicates whether the line is free to receive signals or occupied (either by the transmitter or time synchronization modules). The first reception step of a RTS message happens when the submodule *Predecoder* detects the preamble signals. This signal is used to wake up the receiver and is connected to the *Clock* module. It is worth noting that the *Clock* module stops sending clock signals to the modules while in the sleep mode and needs to be waken up by preamble signals from the receiver modules or request signals from other parts of system. In any case, to generate the preamble signal, the *Predecoder* does not need a clock signal. To enable the preamble signal, the *Predecoder* has to detect at least two consecutive transitions in the incoming signal. After waking up the system, the *Clock Recovery* module generates a recovered *CLKRX* that is synchronized with the received signal.
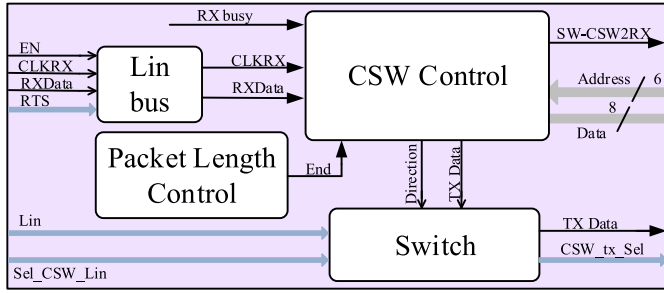
Fig. 12. Organization of the circuit switching module.

Fig. 13. Organization of the *Clock* module.

After detecting the preamble signals, the *Predecoder* determines the RTS message (*RTSnn*, *RTSnd*, or *TRQ*).

G. Circuit Switching Module

The participation of each node in circuit-based transmission is managed by the *Circuit SW* module. This module is responsible for establishing a path between an input and an output port inside the router, for monitoring the data transfer during communication, and for releasing the path at the end. Figure 12 shows the block diagram of this module. The *CSW Control* module controls all switching steps, generates *RTSnd* messages, evaluates the received *hop-count*, detects *CTS* messages, enables and changes the direction of the *Switch* module and switches to hybrid mode. The *Switch* module establishes a path between the selected ports.

In circuit switching mode, none of the intermediate nodes buffer the packet. Compared to packet switching, that is the main advantage of circuit switching because it reduces power consumption and end-to-end delay. Although circuit switching reduces the buffering and eliminates packet serving delay, long circuit paths may degrade network performance. To control path length, each node imposes two limitations on the number of hops:

- *Maximum hop-count*: determines the maximum hop cont in a path with which an intermediate node can get the packet and then make another circuit in the direction of BN.
- *Hop-count threshold*: is similar to *Maximum hop-count* with the difference that an intermediate node can decide to release the circuit path or get the packet based on the status of its *near-node*.

H. Clocking

The system clock signal synchronizes the data flow inside and between modules. On the other hand, each module may require other clock signals with a different frequency. For example, the communication data rate (determined by both *CLK2TX* and *CLK2RX*) can be equal or lower than the system clock frequency. The *Clock* module shown in Figure 13 is responsible for generating, controlling and distributing all clock signals.

The *Reset* submodule generates an internal synchronous reset signal. To reset the entire system, the *RST-pin* must be held high for at least one clock period.
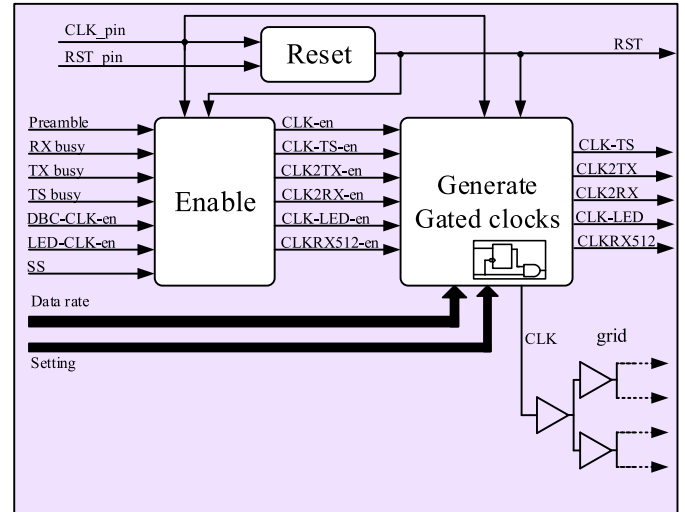
TABLE I
CHARACTERISTICS OF THE COMMUNICATIONS IC

Parameter	Value
Technology	CMOS $0.35\,\mu\text{m}$
Power supply voltage	$3.3\,\text{V}$
I/O	$3.3\,\text{V}$
Clock frequency	up to $70\,\text{MHz}$
Data rate	up to $35\,\text{MHz}$
Die size	$5.86\,\text{mm}^2$
Core size (with RAM)	$2.53\,\text{mm}^2$
Internal memory	$2\,\text{kB}$

As mentioned before, to reduce power consumption, the system can be put into sleep mode whenever there are no tasks to be executed. In the sleep mode, all the clocks except *CLK-TS* are disabled by the *Clock* module. In this mode, two conditions may occur which require the system to change its status to active: reception of preamble bits from a neighbour SN or SPI port activity initiated by the microcontroller, by pulling pin *SS* low.

VI. ASIC IMPLEMENTATION FLOW

Before fabricating the IC, its operation was verified within a low-power Igloo FPGA from Actel. The circuit was developed with Libero IDE from Actel, a complete design environment for FPGAs. A program developed in C# was used to replace the Actel macros with standard cells. The Verilog files for the ASIC version were automatically generated from the ones used for the FPGA version.

After validation, the Design Compiler tool from Synopsys was used to perform logic synthesis and technology mapping to the Austria Micro Systems (4-metal CMOS $0.35\,\mu\text{m}$) cell library. Physical synthesis was carried out with Cadence Encounter. At the end of the process, a file containing fabrication information in the GDSII format was generated. Table I summarizes data rate, supply voltage, clock frequency, and other parameters of the IC.
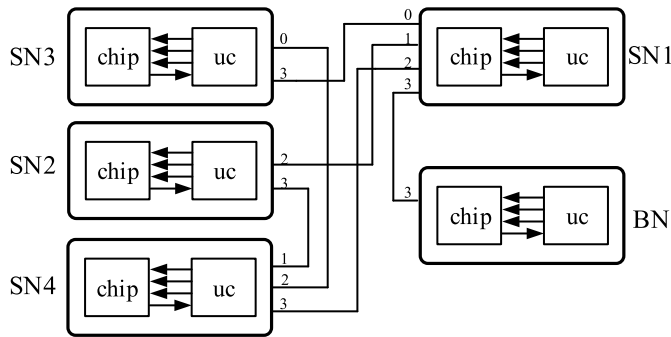
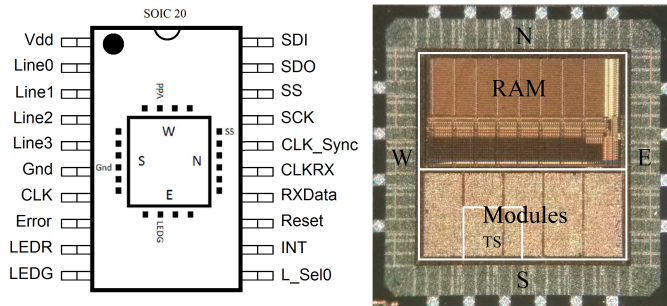Fig. 14. Example of a testbench with four SNs and BN.

Fig. 16. Sensor node prototype used for evaluating the ASIC implementation (IC at the bottom) of the multifunctional router.

Fig. 15. SOIC20 package and photograph of the prototype IC.

Fig. 17. Behavior observed during the delivery of a packet generated by SN3 to BN by packet switching.

For validation of the descriptions in all the design steps, some testbenches were designed. Since the ASIC is to be used in a sensor network, the testbench sets up a simple network with a BN and a few SNs. All the ASIC operations are set and controlled by an external microcontroller via the SPI port. Hence, the nodes of the testbench include a microcontroller, described in Verilog and connected to the ASIC with an SPI port. Each microcontroller communicates with the ASIC as in a real application. Figure 14 shows the diagram of a testbench, including four SNs and a BN. Depending on the desired tests, the testbench can include more nodes in any connection pattern.

The photograph of the fabricated ASIC prototype is shown in Figure 15. It has 20 pins including communication ports, SPI interface, power supply and test pins, and is packaged in a SOIC20 for testing. To evaluate the CDR, the recovered clock and the data line of port 0 are available on pins 14 and 15. To monitor and evaluate the lines activity, line *Line-sel0* of port 0 is connected to pin 11.

VII. EXPERIMENTAL RESULTS

This section presents the experimental results obtained with the sensor node prototypes that include the communication ASIC, as shown in Figure 16. The node was evaluated both with normal copper wire and conductive yarns interconnections. The signals on the lines between the nodes were observed and measured with a digital oscilloscope. The results of signal quality and performance of both clock and time synchronization are presented separately in [6]–[8].

A. Routing Operations

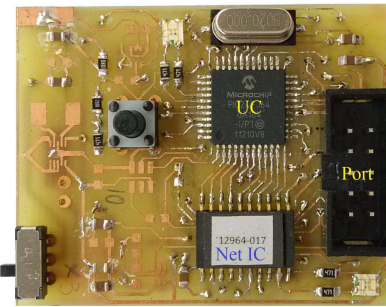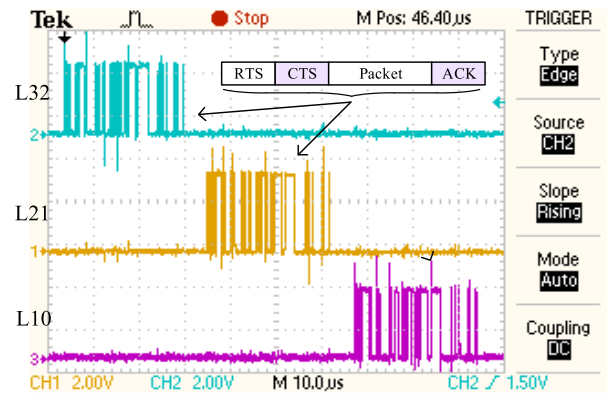The different types of switching and routing operations were explained in the previous sections. This section evaluates the SN-to-BN routing behavior and performance in all configurations (packet, circuit or hybrid mode) for the network of sensor nodes depicted in Figure 2.

1) Routing by Packet Switching: Figure 17 shows the evolution of signals during the transmission of a small data packet (4 bytes) generated by SN3 and sent to the BN via a path through intermediate nodes SN1 and SN2. The routing operation is independent from packet length and a small packet was selected to show the signals clearly. To configure the sensor nodes to act in normal packet switching mode, the value of *Maximum hop-count* and *hop-count threshold* must be set to 1. All nodes are working at $16.383\,\text{MHz}$ and the data rate is set to $4.096\,\text{Mbps}$. In each node, at the end of packet reception, the router starts to serve the packet and route it to the next node. The measured value for serving time is $5.3\,\mu\text{s}$. The measured end-to-end delay for packet transmission is $90.16\,\mu\text{s}$.

2) Routing by Circuit Switching: The signals generated while transmitting the same packet, but using circuit switching are shown in Figure 18. SN3 starts establishing a circuit path by sending an *RTSnd* message at $t = 0.24\,\mu\text{s}$; transmission is completed at $t = 36.3\,\mu\text{s}$. So, in this case, the end-to-end delay is $36.06\,\mu\text{s}$, which is 40% of the time required with packet switching.

Figure 19 shows the message exchange required to establish the circuit path between SN3 and BN. As mentioned earlier, the *Line-sel* of port 0 is available on one of the pins and was used to measure the activity of port 0 of all intervening nodes, as shown in Figure 20.
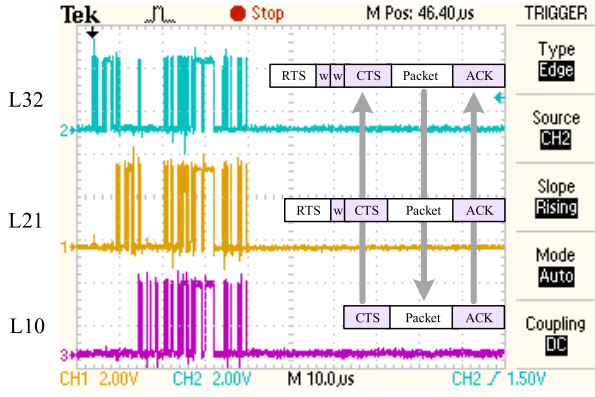
Fig. 18. An example of pure circuit switching transmitting the same packet as in the previous figure.
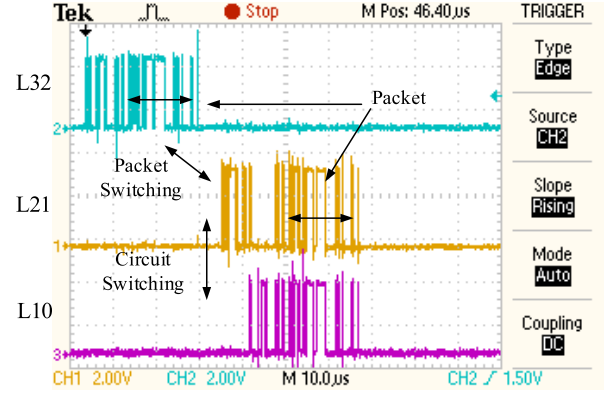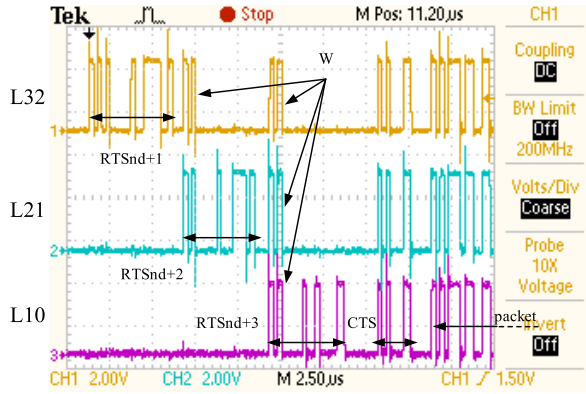

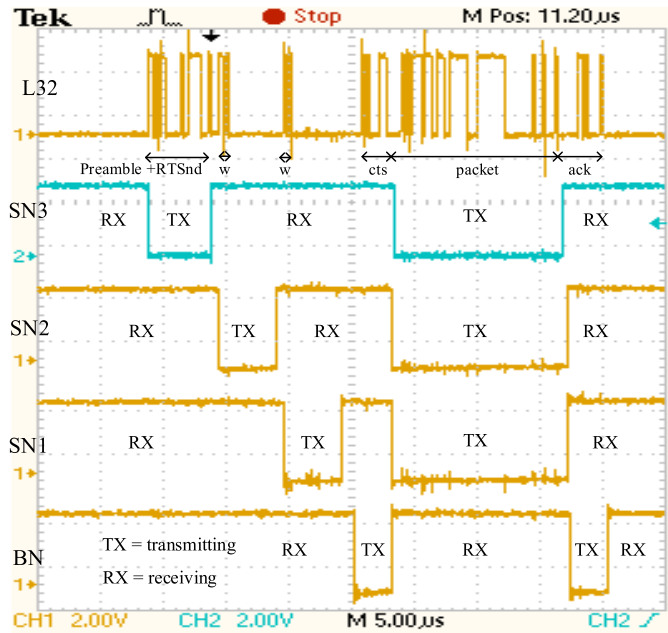Fig. 19. Details of message exchange to establish the circuit path between SN3 and BN.

Fig. 20. Status of the communication ports of each SN during circuit switching.

Node SN3 starts communication by sending *RTSnd + 1* to SN2 at $t = 0.24\,\mu s$ (cf. Figure 19). Node SN2 receives the *RTS* message, and simultaneously sends both a *Wait* message

Fig. 21. An example of hybrid circuit and packet switching.

back to SN3 and a *RTSnd + 2* message forward to SN1 at $t = 5.8\,\mu s$. SN1 starts communication with the BN at $t = 10.84\,\mu s$. In this instant, a circuit path has been established between BN and SN3. Therefore, SN3, SN1 and SN2 directly receive the *CTS* message from BN at $t = 17.12\,\mu s$. Then, SN2 and SN1 change the direction of the switch to allow SN3 to transfer the data packet starting at $t = 20.24\,\mu s$. The packet has $4\,\text{bytes}$ and takes $12.56\,\mu s$ to transmit, finishing at $t = 32.8\,\mu s$. At the end of the packet, SN2 and SN1 change the direction of their switches to transmit the *ACK* message from the BN. All nodes release the lines and finish communication at $t = 36.28\,\mu s$.

3) Routing by Hybrid Circuit and Packet Switching: As explained before, a data packet can be sent to the BN by using both switching modes, thereby implementing a hybrid mode of transmission. To show the signals and network operation in this case, packet switching is used between SN3 and SN2; then, SN2 sends the buffered packet to the BN via circuit switching through SN1. Figure 21 shows the signals observed during hybrid switching. SN3 starts to send the packet at $t = 0.24\,\mu s$, finishing at $t = 2.87\,\mu s$. After processing the packet at $t = 5.6\,\mu s$, SN2 sends it to the BN by establishing a circuit path via SN1, finishing at $t = 63.6\,\mu s$. The measured end-to-end delay in this case is $\Delta t = 63.6\,\mu s - 0.24\,\mu s = 63.34\,\mu s$, which, as expected, is shorter than the time required by pure packet switching, but longer than the time required by pure circuit switching.

B. Power Consumption

In sleep mode, all internal clocks (except *CLK-TS* in case of enabling the time synchronization) are disabled in order to save power. To separately evaluate the power consumptions of receiver, transmitter and other modules in sleep mode, the ability to disable the *CLK2RX*, *CLK2TX* and *CLK* signals was added to the *Clock* module. In the active mode, all clock signals are permanently driving the respective modules. The results can be seen in Figure 22 for both $16.383\,\text{MHz}$ and $20\,\text{MHz}$ system clock frequencies. The signs "-" and "+" represent sleep and active modes, respectively. When all clock signals except the one for the *Time sync* module are disabled, the current is at the minimum values of $0.5\,\text{mA}$ at
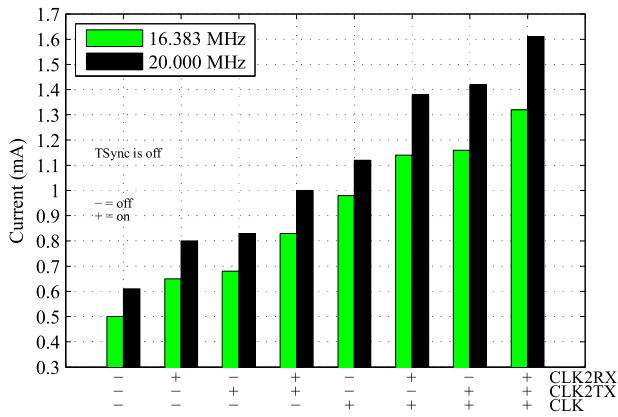
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Fig. 22. Measured ASIC supply current as a function of the activity of *CLK2RX*, *CLK2TX* and *CLK*.

Fig. 24. The measured power consumption as a function of data rate for different operation modes (VCC = 3.3 V).

Fig. 23. Measured power consumption as a function of data rate (VCC = 3.3 V).

$16.383\,\mathrm{MHz}$ and $0.61\,\mathrm{mA}$ at $20\,\mathrm{MHz}$. When all clock signals are active, the system requires almost 2.64 times more current, and therefore consumes as much more power (the supply voltage is constant).

The measured current at the maximum frequency of $70\,\mathrm{MHz}$ varies from $2.1\,\mathrm{mA}$ for the all blocks in sleep mode to $5.7\,\mathrm{mA}$ for the all blocks in active mode.

Figure 23 shows the measurement results of the power usage in terms of the selected data rate for $20\,\mathrm{MHz}$ system clock. In sleep mode or when only *CLK* is active, the power consumption remains constant, as expected. By increasing the data rate, the power consumption increases when either *CLK2RX* or *CLK2TX* are active. *CLK2TX* drives more elements than the *CLK2RX*; therefore, it has a larger impact on the supply current.

The IC power consumption when operating as a transmitter, receiver or participating in circuit switching is shown in Figure 24. The power increases almost linearly with the data rate. In circuit switching mode, the ASIC draws less current than in packet switching mode (either as transmitter or receiver). In packet switching mode, each node receives and then sends the packet. Hence, power consumption for each packet requires the addition of both receiving plus transmitting power consumption, whereas, in circuit switching, because of the absence of buffering, the power consumption is only due
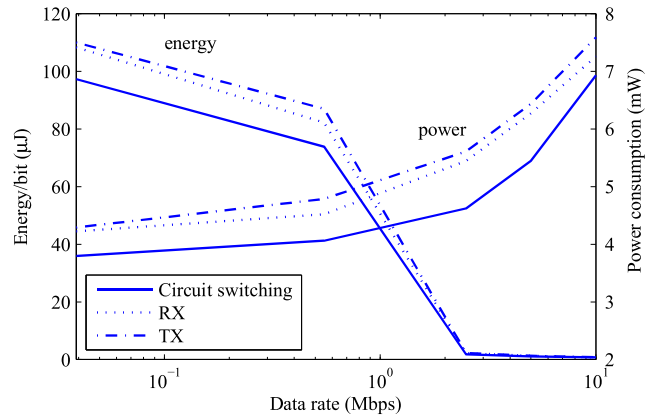
to the internal connection between the ports, which is smaller than the power required for packet switching. So, operating the IC in circuit switching mode decreases both power consumption and end-to-end delay. This figure also shows energy consumption per bit. As can be seen, as the circuit data rate increases, the power consumption increases, but the energy per bit decreases sharply. This is due to the static part of the total power consumption and, as the data rate increases, the power consumption not increasing proportionally.

The power supply is a single coin type rechargeable lithium battery (LIR2450) with $120\mathrm{mAh}$ capacity and nominal voltage $3.6\,\mathrm{V}$, which drops to $2.75\,\mathrm{V}$ during operation. So a buck-boost DC-to-DC converter is needed to generate $3.3\,\mathrm{V}$ at the output. For this purpose, the TPS63031, a high-efficiency single-inductor buck-boost converter has been used. According to Figures 22 to 24, the lifetime of the battery depends on the system clock, data-rate, and node activity. Nodes closer to the BN hand over more packets than more distant nodes, leading to decreased lifetime of the respective batteries. However, the results obtained in the ProLimb project show that all nodes can run for a full day on a single battery. An alternative way to supply nodes consist of using a common power and data line shared by all nodes that are connected to a single higher capacity power battery, placed somewhere near the BN. A preliminary implementation of this approach was published by the authors in [3].

C. Concurrent Multitasking

The router ASIC is able to handle several concurrent tasks. For a demonstration of this ability, consider the network shown in Figure 25. All SN2 ports are used to communicate with BN and other SNs.

Figure 26 shows the signals captured while performing three tasks on SN2. First of all, a circuit path between SN4 and BN is established. $24\,\mu\mathrm{s}$ after starting that communication, SN3 sends a packet. SN2 receives the packet from SN3 without any effect on the communication between SN4 and BN. The third task is a time synchronization message exchange between SN5 and SN2. At this time, all ports of SN2 are occupied, but the node can handle all tasks without any problem or interruption.
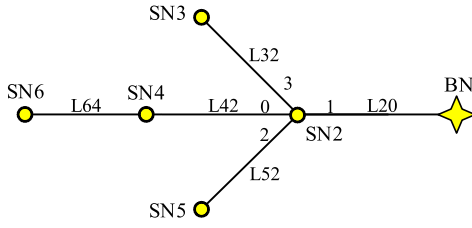
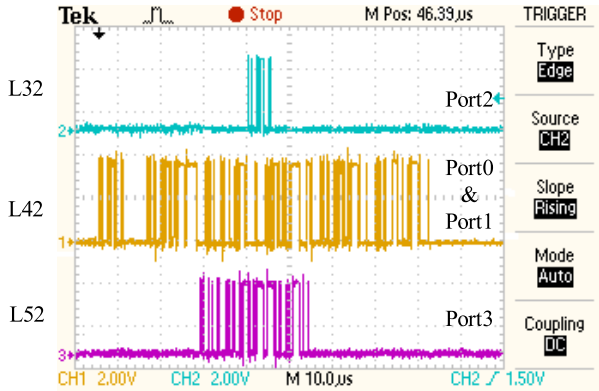Fig. 25.   Network used for evaluation of communication multitasking.

Fig. 26.   Signals on the data lines of SN2 while concurrently performing three communication tasks.
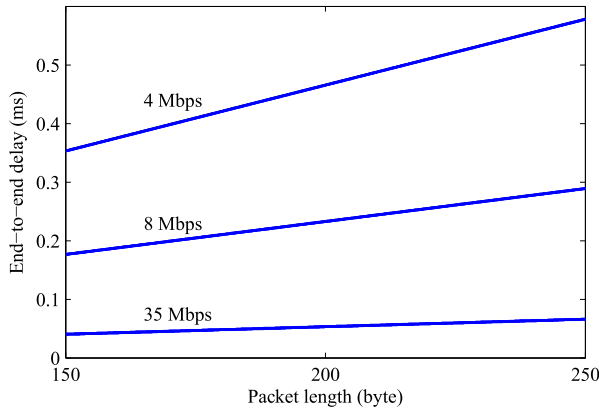

Fig. 27.   End-to-end delay as a function of packet length for two data rates.

D. Circuit Switching

The performance of the network in Figure 25 was also evaluated while using circuit switching. The total end-to-end delay from SN6 to BN for three nominal data rates ($4\,\mathrm{Mbps}$, $8\,\mathrm{Mbps}$, and $35\,\mathrm{Mbps}$) is shown in Figure 27. The delay increases linearly with packet length. Unlike the end-to-end results for packet switching, in circuit switching the end-to-end delay is independent from the traffic. Circuit switching exhibits a delay of $0.58\,\mathrm{ms}$ at $4\,\mathrm{Mbps}$ for a $250\,\mathrm{B}$ packet length. In comparison with packet switching, the delay is 7 times shorter than the delay at data rate $640\,\mathrm{kbps}$ and 3 times shorter than the delay at $20.8\,\mathrm{kbps}$.

Figure 28 shows the throughput of the network as a function of packet length, for different amounts of the total network traffic at a nominal data rate of $4\,\mathrm{Mbps}$. The system reaches 88.8% of the maximum throughput for $100\,\mathrm{B}$ packet length and $3.4\,\mathrm{MB}$ traffic, which is more than 5 times higher than with
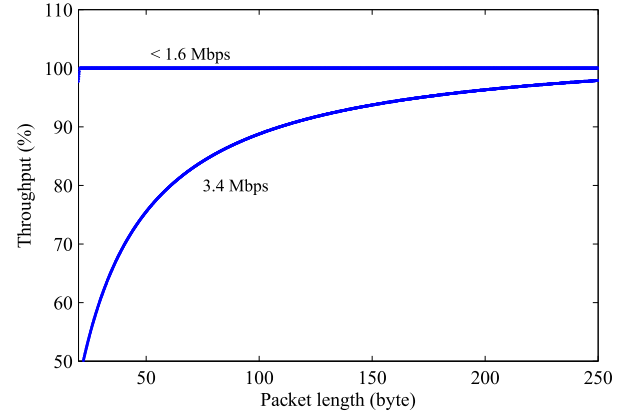

Fig. 28.   Network throughput as a function of packet length at 4 Mbps.

packet switching ($640\,\mathrm{kbps}$). Increasing the packet length to $250\,\mathrm{B}$, the throughput reaches almost 98% with a total traffic of $3.4\,\mathrm{MB}$. Independently of the packet length, for data rates below 1.6 MB, throughput can reach 100%. Increasing the data rate to $35\,\mathrm{Mbps}$, throughput reaches almost 97% with 30 MB total traffic and a packet length of $250\,\mathrm{B}$.

VIII. Conclusions

An ASIC meant to be used as a multifunctional router for body area networks of sensors is described in this paper. Its structure and functionality, which includes the on-chip implementation of a routing algorithm supporting both circuit, packet, and hybrid switching, and a one-way, high precise, time synchronization are presented. It is also able to run several asynchronous communication tasks simultaneously. An open-loop, very small size, and low power CDR has been designed to support the involved clocking operations.

The proposed IC was fabricated in a $0.35\,\mu\mathrm{m}$ CMOS technology and was thoroughly tested and evaluated. The experimental results presented here show that the circuit works up to $35\,\mathrm{Mbps}$. The obtained results also confirm that in a wearable BAN consisting of nodes connected in a mesh topology, the power consumption of the intermediate nodes involved in constructing a circuit path and in packet handover for circuit switching is lower than that obtained in packet switching mode.

It should be noted that the circuit's power consumption and speed depend strongly on the technology used. A $0.35\,\mu\mathrm{m}$ CMOS technology was used to fabricate the present prototype. However, since it is a fully digital circuit, the same design can be easily scaled to newer technologies to work at even higher speed and/or lower power consumption.

The architecture of the proposed IC provides for reliable communications with high data rates, while supporting networks comprised of tens of sensor nodes embedded in textile.

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