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LUCAS BARROSO SPEJO

STRESS CHARACTERIZATION OF STRAINED SILICON NANOSTRUCTURES BY RAMAN SPECTROSCOPY

CARACTERIZAÇÃO DO ESTRESSE MECÂNICO DE NANOESTRUTURAS DE SILÍCIO TENSIONADO POR ESPECTROSCOPIA RAMAN

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Lucas Barroso Spejo

Stress characterization of strained silicon nanostructures by Raman spectroscopy

Caracterização do estresse mecânico de nanoestruturas de silício tensionado por espectroscopia Raman

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Coorientador: Dr. Marcos Vinicius Puydinger dos Santos

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“Thoroughly conscious ignorance is the prelude to every real advance in science”

James Clerk Maxwell

ABSTRACT

Strained silicon engineering has proven to be a successful technology to keep Moore's law and presents a great potential for its use in even smaller and highly stressed technological nodes in microelectronics in the future. Such a task demands the use of stress characterization techniques for semiconductor research and development.

One potential characterization tool which makes possible quantitative stress measurement of silicon is the Raman spectroscopy. This characterization method is a well-established non-destructive technique that permits stress characterization with a spatial resolution of below 1 µm and does not require complex sample preparation procedure. However, studies on Raman shift behavior of highly stressed structures (stress greater than 2 GPa) with the critical dimension smaller than 100 nm are scarce in the literature, being a bottleneck for the systematic use of Raman measurements in future technological devices.

Here, it was investigated the Raman shift-stress behavior from the (001) silicon surface of highly strained ultra-thin (15 nm-thick) suspended nanowires with stresses in the range of 0 – 6.3 GPa along the [110] direction. The use of ultrathin nanowires as a platform of study, along the [110] crystallographic direction, allowed the systematic investigation of one essential block that might be present in future nMOS transistors channels. Furthermore, this suspended platform reached ultra-high stress values (up to 6.3 GPa) without external actuators, allowing for the first time the systematic study of the Raman stress behavior of highly stressed nanowires.

The stresses were evaluated by finite element method (FEM) simulations to achieve great accuracy in the stress characterization. Then, experimental Raman measurements were performed, followed by a thermal correction protocol to extract the corrected Raman peak free of thermal effects.

The extracted stress shift coefficient (SSC), for lower stresses (below 4.5 GPa), was in good agreement with some of the SSC values in literature. For higher stresses (greater than 4.5 GPa), it was demonstrated, for the first time, that the linear shift Raman - stress relation does not hold, thus requiring an empirical model correction proposed in this work.

The results demonstrate the feasibility of the Raman technique for the stress characterization of ultra-thin silicon nanowires, which should be useful to characterize

strained silicon nanodevices for technological nodes below 100 nm under a wide range of stresses, contributing to such an important topic in the semiconductor industry.

RESUMO

A engenharia de silício tensionado provou ser uma tecnologia de sucesso para manter a lei de Moore e apresenta um grande potencial para o seu uso em nós tecnológicos altamente estressados e ainda menores na microeletrônica do futuro. Essa tarefa demanda o uso de técnicas de caracterização do estresse mecânico para o desenvolvimento e pesquisa em semicondutores.

Uma potencial ferramenta de caracterização que permite a medição do estresse no silício de forma quantitativa é a espectroscopia Raman. Esse método de caracterização consiste em uma técnica não destrutiva e bem estabelecida que permite a caracterização do estresse com uma resolução espacial abaixo de 1 µm e não requer procedimentos complexos de preparação da amostra. Contudo, estudos sobre o comportamento do deslocamento Raman em estruturas altamente tensionadas (tensão maior que 2 GPa) com dimensão crítica menor que 100 nm são escassos na literatura, sendo um gargalo para o uso de medidas Raman de forma sistemática em dispositivos tecnológicos futuros.

Aqui, foi investigado o comportamento do estresse em função do deslocamento Raman da superfície de silício (001) de nanofios suspensos ultra finos (15 nm de espessura) e altamente tensionados com estresses na faixa de 0 – 6.3 Gpa ao longo da direção cristalográfica [110]. O uso de nanofios ultrafinos como plataforma de estudo , ao longo da direção cristalográfica [110], permitiu a investigação sistemática de um bloco essencial que pode estar presente nos canais de transistores nMOS futuros. Além disso, essa plataforma suspensa atingiu valores de tensão ultra altos (até 6.3GPa) sem atuadores externos, permitindo pela primeira vez o estudo sistemático do comportamento da espectrocopia Raman em nanofios altamente tensionados.

Os estresses foram medidos por simulações de elementos finitos (FEM) como forma de atingir uma grande precisão na caracterização da tensão. Então, medidas Raman experimentais foram realizadas seguidas de um protocolo de correção térmica para extrair o pico Raman corrigido livre de efeitos térmicos.

O coeficiente de deslocamento do estresse (SSC) extraído, para baixa tensão (abaixo de 4.5 GPa), estava em boa concordância com alguns valores de SSC da literatura. Para maiores valores de tensão (maior que 4.5 GPa), demonstrou-se, pela primeira vez, que a

relação linear deslocamento Raman - estresse não ocorre, requerendo uma correção empírica do modelo que está sendo proposta neste trabalho.

Esses resultados demonstram a viabilidade da técnica Raman para caracterização do estresse de nanofios de silício ultrafinos, no qual deve ser útil para caracterizar nanodispositivos de silício tensionado para nós tecnológicos abaixo dos 100 nm sujeitos a uma faixa ampla de tensão, contribuindo para um tópico importante na indústria de semicondutores.

LIST OF FIGURES

Figure 1: A) Relative density of the main components in a micro processed system along last decades, showing an increase of about 6 orders of magnitude over the last five decades, B) Dennard scaling laws of the main parameters in microelectronics, like current, voltage, doping concentration. The κ is a constant that dictates the scaling of the devices and circuits parameters……22

Figure 2: Technological roadmap of processors since the 90 nm node until the 14 nm node……..23

Figure 3: A) Transmission electron microscopy (TEM) image of a nMOS transistor cross-section with deposited high stress film (silicon nitride) creating a tensile stress in the channel (arrows), and B) TEM image of a pMOS transistor cross-section. The SiGe source and drain regions generate compressive stress in the channel (arrows)……………………………………………..24

Figure 4: Examples of accelerometers. A) Capacitive accelerometer, and B) Piezoresistive accelerometer………26

Figure 5: A) Suspended Si nanowire in a nanowire-based resonator, and B) the strain map when the device oscillates, showing the tensioned and compressed regions……………………..27

Figure 6: A) Suspended Si beam strained by a silicon nitride actuator, and B) Sequential TEM images of a strained Si nanowire until its fracture. It was used a piezo motor to stretch the nanowire………...31

Figure 7: Diagram representing the X-rays diffraction of a plane wave in a crystal…………….32

Figure 8: A)HRTEM Si nanowire image. On top is shown the placement of the atoms and on the bottom the smooth nanowire surface, and B) (a) Dark field TEM image of a GAA nanosheet transistor on SOI after source/drain epitaxy, (b) ϵ_{xz}, (c) ϵ_{zz}, and (d) ϵ_{xx}. PED (Precession electron diffraction) images with calculated model………………………………………...33

Figure 9: Feynman diagram and energy levels of a Stokes scattering process……………………..34

Figure 10: A) Raman spectrum of unstrained silicon (center), tensile uniaxial stressed silicon (left), and compressive uniaxial stressed silicon (right). The Raman shift between the unstrained silicon peak and the shifted strained silicon peak is the quantity $\Delta\omega$. B) Raman shift mapping as function of the device channel position from a Si-based device with a silicon nitride top layer………..35

Figure 11: Nanobridge dimensions and stress mechanism. A) Top view of a nanobridge with its dimensions before the suspension. The parameters **A**, **B**, **a** and **b** refer to the NW length, the bridge length, the NW width and the pad width, respectively, and B) Top view of a nanobridge after suspension……………………………………………………………………………………….41

Figure 12: Strain dependence on the dimensions of the nanobridges. A) Longitudinal strain of the NW as function of the pad width, **b**, for **B** = 2.4 µm and **A** = 0.6 µm, and different NW width, **a**. As already mentined, **A**, **B**, **a** and **b** refer to the NW length, the bridge length, the NW width and the pad width, respectively, and **L** refers to the under-etched length. The under-etched length, **L**, is 600 nm for the circle symbol keys, whereas 750 nm for the star symbol key. The initial strain of the wafer is plotted for reference (dashed line), B) Strain as a function of the nW width a for a constant pad width b = 1.5 µm and L = 750 nm. The wire length is A = 0.6 µm, whereas the bridge length was varied from B = 2.4 to 4.4 µm. The initial strain of the wafer is plotted for reference (dashed line), and C) strain enhancement versus the ratio b/a for NWs with different b and a values. The curved lines were obtained from equation. (1), whereas the points represent experimental measurements ………………………..44

Figure 13: Nanofabrication steps: A) sSOI Wafer, B) After nanobridge pattern transfer by ebeam lithography, C) After dry etching and resist removal. The dimensions from the nanobridge are also shown (a = NW width, b = Pad width, A = NW length, B = Nanobridge length), and D) Suspended nanobridge after selective wet etching…………………………………….45

Figure 14: Fabricated Suspended Nanobridges. A) Nanobridge with the inner region in a circular shape , B) Nanobridge with the inner region in a trapezoidal shape ……………………….46

Figure 15: Fabricated nanobridges. A) Trapezoidal nanobridge and B) Circular nanobridge The shaded areas correspond to the region where the electron beam impinges the electron-sensitive resist for further revealing process during the lithographic steps. The scale bar corresponds to 1 µm……47

Figure 16: Complete layout with 180 nanobridges. This layout is composed of 5 blocks with the NW width dimension, **a,** equal to 75, 100, 150, 150, 175, and 200 nm. Each one of these blocks has 6 lines with **b** dimensions equal to 500, 750, 1000, 1200, 1500, and 1700 nm. Each one of these lines has 6 identical nanobridges. Every nanobridge has the following dimensions: A = 700nm, and B = 3000 nm. The total number of devices for each layout is 180………47

Figure 17: A) Nanobridge after resist developing process. The darker region is PMMA, and the lighter one is the exposed silicon. B) Nanobridge after dry etching and resist removal. The inner regions are the exposed silicon dioxide, and the outter region is the Si thin film………49
Figure 18: Nanobridges after the wet etching process. The under etching zone corresponds to the suspended region, where the HF buffer has etched the silicon dioxide. A) Nanobridge with the layout from Figure 15A, B) Nanobridge with the layout shown in Figure 15B..........50
Figure 19: A) Top-view SEM image of the fabricated nanobridge with dimensions a = 138 nm, b = 1431 nm, A = 690 nm, B = 3520 nm, and average underetching of 273 nm, and B) Corresponding simulated COMSOL geometry……………………………………………………………………51
Figure 20: Nanobridge image with zoom of 70 kX. The large magnification minimizes errors when measuring the device dimensions …………………………………………………………………….....53
Figure 21: Nanobridge with irregular under etching . The guidelines are used to perform the measurements of the corrosion profile in the edges. B) Corresponding simulated Comsol geometry………54
Figure 22: A) Top-view of a fabricated nanobridge with the cut-line indicated (before platinum deposition). The ion beam milled the region below the cut-line after platinum deposition. B) Lateral view (indicated in A) from the milled nanobridge. C) Lateral view from the region highlighted in B. It is possible to check the deposited platinum, the 145 nm-thick buried silicon dioxide (BOX), and the silicon bulk. The 15 nm-thick strained Si film was indicated in the figure but still not visible because of the equipment resolution limit (~10 nm). One can see the profile of the etched area by the penetration of platinum into the box etched area. D) Top-view image of the nanobridge with the outer border dimension (arrows) and the corresponding Comsol CAD simulation (top-view). One can also observe the simulated lateral profile of the region demonstrated in Figure 22C……………………………………55
Figure 23: Stress components simulated by FEM of the suspended nanowire presented in Figure 19. A) Color map of the σ_{xx} stress component in the nanostructure, B) Cut-Line graph for the triaxial stress components in the structure along the center, and color map of the C) σ_{yy} and D) σ_{zz} stress components at the nanostructure……………………………………………………….58
Figure 24: A) Raman spectrum from the strained nanowire of Figure 19 with an incident laser power of 34 µW, B) Raman spectra evolution from nanowires of different stress. The spectra were measured at 23 uW incident laser power from nanowires with 2.3 GPa up to 6.3 GPa,

and C) thermal correction procedure from the nanowire of Figure 19 (red circles) measured in 5 distinct incident powers (4, 10, 23, 34 and 69 µW). The sSNW peaks are plotted with a linear fit. The intercept at zero laser power represents the "heat-free" shift. *Inset*: top-view SEM image of a stressed silicon nanowire and its thermal correction procedure (black squares)………...60

Figure 25: A) Experimental Raman shift as a function of the simulated stress for 28 different nanowires, B) comparison between the extracted SSC modulus from our work with the SSC values reported in literature. The shaded area region covers the previous works reported on bulk silicon or with bulk silicon parameters, and C) Stress as function of the Raman shift from 49 different nanowires. Up to around 4.5 GPa the linear model is in agreement with the quadratic model……62

LIST OF TABLES

Table 1: Reported silicon phonon deformation potentials (PDPs) in literature and the stress-shift coefficient (SSC) for uniaxially stressed silicon at the [110] crystallographic direction on a (001) surface. The thickness of the characterized structure (also the smaller dimension) and the stress type with its range are shown as well……………………………………………………………37

Table 2: Reported silicon phonon deformation potentials (PDPs) in literature and the stress-shift coefficient (SSC) for uniaxially stressed silicon at the [110] crystallographic direction on a (001) surface. The thickness of the characterized structure (also the smaller dimension) and the stress type with its range are shown as well. The results from this thesis are demonstrated in the last row ……………………………………………………………………………………...……65

LIST OF SYMBOLS

FEM	Finite Element Method
SSC	Stress Shift Coefficient
MEMs	Micro-Electro-Mechanical Systems
NEMs	Nano-Electro-Mechanical Systems
MOS	Metal Oxide Semiconductor
FinFET	Fin Field Effect Transistor
GAA	Gate All Around
FET	Field Effect Transistor
DTCO	Design-Technology-Co-Optimization
SiGe	Silicon Germanium
pMOS	p-type Metal Oxide Semiconductor
nMOS	n-type Metal Oxide Semiconductor
TEM	Transmission Electron Microscopy
Si	Silicon
TSV	Through Silicon Via
W	Tungsten
Cu	Copper
CMOS	Complementary Metal Oxide Semiconductor
SEM	Scanning Electron Microscopy
1D	One Dimensional
3D	Three Dimensional
AFM	Atomic Force Microscopy
XRD	X-Ray Diffraction
HRTEM	High Resolution Transmission Electron Microscopy
SOI	Strained Silicon On Insulator
PED	Precession Electron Diffraction
FIB	Focused Ion Beam
PDPs	Phonon Deformation Potentials
Compre	Compressive
EBL	Electron Beam Lithography

sSOI	strained Silicon On Insulator
PMMA	Polymethyl methacrylate
Ar	Argon
SF_6	Sulfur hexafluoride
RF	Radiofrequency
O_2	Oxygen gas
SiO_2	Silicon dioxide
NH_4F	Ammonium fluoride
HF	Fluoridric Acid
sSNW	strained Silicon Nanowire
NW	Nanowire
CAD	Computer Assisted Design
Pt	Platinum
BOX	Silicon dioxide from sSOI wafer

TABLE OF CONTENTS

AGRADECIMENTOS 06
ABSTRACT 08
RESUMO 10
LIST OF FIGURES 12
LIST OF TABLES 16
LIST OF SYMBOLS 17
CHAPTER I – INTRODUCTION AND MOTIVATION – STRAINED SILICON AT THE MICRO AND NANO SCALE 21
1.1. STRAIN APPLICATION IN MICROELECTRONICS 22
1.1.A. MICROELECTRONICS PANORAMA 22
1.1.B. STRAINED SILICON ENGINEERING 24
1.1.C. STRAIN INDUCED BY TSV (THORUGH SILICON VIA) INTERCONNECT TECHNOLOGY – UNDESIRABLE STRESS 25
1.2. STRAIN APPLICATION IN MEMS (MICRO-ELECTRO-MECHANICAL SYSTEMS) AND NEMS (NANO-ELECTRO-MECHANICAL SYSTEMS) 25
1.2.A. ACCELEROMETERS 26
1.2.B. PRESSURE SENSORS 27
1.2.C. RESONATORS 27
1.3. STRAIN/STRESS CHARACTERIZATION OF NANODEVICES 28
1.4. AIM OF THE THESIS 28
1.5. ORGANIZATIONS OF THE THESIS 29
CHAPTER II – BACKGROUND - SILICON STRESS/STRAIN CHARACTERIZATION METHODS 30
2.1. VISUAL INSPECTION 31
2.2. X-RAY DIFFRACTION (XRD) 32

2.3. TRANSMISSION ELECTRON MICROSCOPY (TEM) 33
2.4. RAMAN SPECTROSCOPY 34
CHAPTER III - METHODOLOGY 40
3.1. SUSPENDED NANOBRIDGE: ANALYTICAL MODELLING 41
3.2. NANOFABRICATION PROCESS 44
3.2.A. OVERVIEW 44
3.2.B. LAYOUT DESIGN 46
3.2.C. EBEAM LITHOGRAPHY 48
3.2.D. DRY ETCHING 48
3.2.E. WET ETCHING 49
3.3. FEM MODELLING 50
3.4. DIMENSIONS CHARACTERIZATION 53
3.5. RAMAN CHARACTERIZATION PROTOCOL 55
CHAPTER IV - RESULTS AND DISCUSSION 57
4.1. RESULTS AND DISCUSSIONS 58
4.1.A. FEM SIMULATION 58
4.1.B. RAMAN CHARACTERIZATION 59
4.1.C. RAMAN SHIFT – STRESS BEHAVIOR 61
CHAPTER V - CONCLUSIONS AND PERPECTIVES 64
CURRICULUM VITAE 67
REFERENCES 69

Chapter I - Introduction & Motivation

Strained Silicon at the Micro & Nano scale

This chapter aims to review the state of the art in the field of strained silicon and the most recent literature, as well as to place the objective of this thesis, which is the development of the stress Raman characterization from strained silicon nanostructures to low and high stresses. Firstly, the importance of strained silicon is demonstrated by the state-of-the-art from strained silicon at the micro & nanoscale and its main applications in microelectronics, and micro & nanoelectromechanical devices (MEMs & NEMs). Then, the challenges of the stress characterization and its importance for the research and development of new nanodevices are demonstrated, reaching to the Raman technique as a potential candidate for strain characterization. Finally, the aim and the organization of this thesis is addressed.

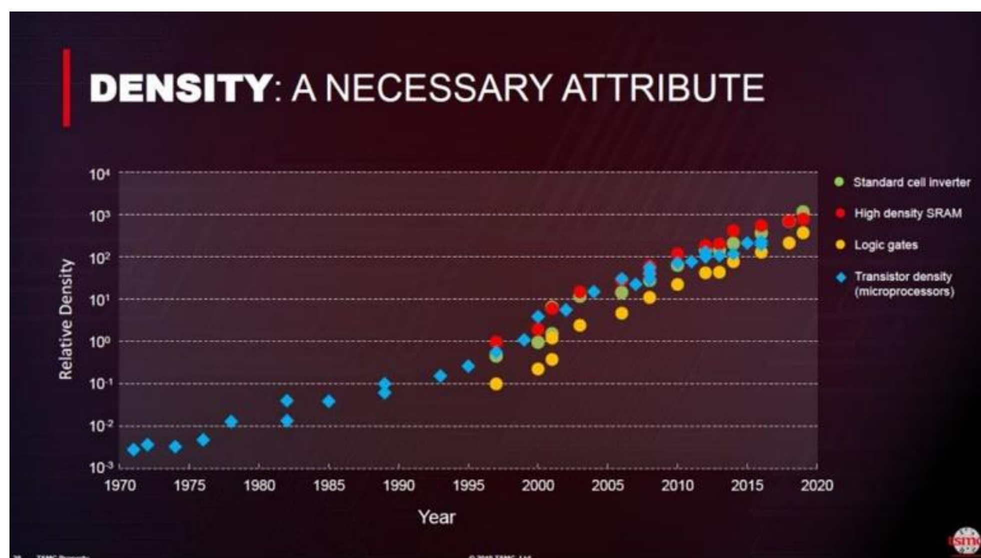
The results of this thesis are going to be published in academic journals. Also, some of the results presented in this thesis (mainly related to the COMSOL simulations) were developed in collaboration with the PhD student José Luis Arrieta Concha, from the School of Electrical and Computer Engineering – FEEC/UNICAMP, who was the main responsible for the finite elements simulations (FEM) and modelling. Those results will be part of his thesis as well.

1.1. Strain Application in Microelectronics

1.1.A. Microelectronics Panorama

The history of microelectronics is strongly related to economic and performance efficiency. In 1965, Gordon Moore, director of research from Fairchild Semiconductor, published his seminal paper: "Cramming more components onto integrated circuits " [1]. In this paper, he stated that the number of transistors in an integrated circuit doubles every 2 years, keeping the same cost of production. Such a statement was based on the shrinking of the components' size with technology advancement. The transistor scaling provided the enhancement of the speed operation, performance and power consumption along the years, as proposed by Dennard scaling [2]. Figure 1A shows the relative density increase of the main components in a micro processed system along the last five decades.

A



B

SCALING RESULTS FOR CIRCUIT PERFORMANCE

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Figure 1: A) Relative density of the main components in a micro processed system along last decades, showing an increase of about six orders of magnitude over the last five decades **[3],** B) Dennard scaling laws **[2]** of the main parameters in microelectronics, like current, voltage, doping concentration. The κ is a constant that dictates the scaling of the devices and circuits parameters.

The transistor scaling had followed Dennard rules (Figure 1B) until the 130 nm node in the early 2000s [4]. After this point, new technological advancements have been implemented to overcome the increased difficulty in reducing the dimensions by process limitations and costs. Some examples are shown in Figure 2, like the implementation of strained silicon engineering by Intel, in 2003, to enhance the carriers electrical mobility [5]. The use of high dielectric constant (high-k), in 2007, for increased Metal-Oxide-Semiconductor (MOS) capacitance permitted the use of thicker gate oxides in order to reduce the leakage current of the MOS structure. Finally, in 2011, the implementation of the Fin Field-Effect-Transistor (FinFET) architecture has improved the electrostatic control of the channel [6]

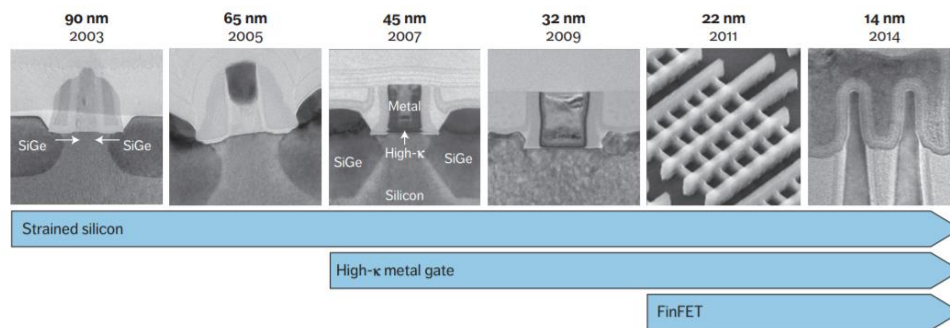


Figure 2: Technological roadmap of processors since the 90 nm node until the 14 nm node **[4]**.

From now on, the nanosheet gate all around (GAA) structure presents a great potential to be the chosen architecture for continued performance enhancement of the microelectronic industry [7], [8]. In addition, in the near future, nanosheet GAA-based architectures present excellent potential candidates for continued scaling such as the Forksheet transistor [9] and the Complementary FET Transistor [10]. In all of these technologies, since 2003, the strained silicon engineering has been implemented and will be used in future nodes. Several techniques in different fields of research have been studied for continued performance enhancement, such as Design-Technology-Co-Optimization techniques (DTCO), novel interconnects technologies, 3D system integration, use of 1D and 2D materials and new physics-based devices [11].

1.1.B. Strained Silicon Engineering

The Strained Silicon Engineering technique is a significant milestone in the microelectronic industry [4]. Since its implementation in commercial transistors in 2003, it has been used in all technological nodes as aforementioned and will probably be used in the future nodes [7], [12], [13]. Even for a far future, with a possible change from silicon to a higher mobility channel, such as germanium, the use of strained engineering might be implemented [14]–[17].

The success of the strained silicon engineering is based on the growth of SiGe alloy and deposition of silicon nitride films. The SiGe alloy can be used as the source and drain of a p-type MOS (pMOS) transistor (Figure 3B). The lattice mismatch between Si and SiGe creates compressive stress in the channel region, enhancing the holes electrical mobility [18]. For the n-type MOS transistors (nMOS) a tensile stress in the channel region is necessary in order to enhance the electron mobility [18]. The deposition of silicon nitride films under different experimental conditions (temperature, pressure) can induce tensile stress on the channel region due to the intrinsic stress of the silicon nitride (Figure 3A) [19].

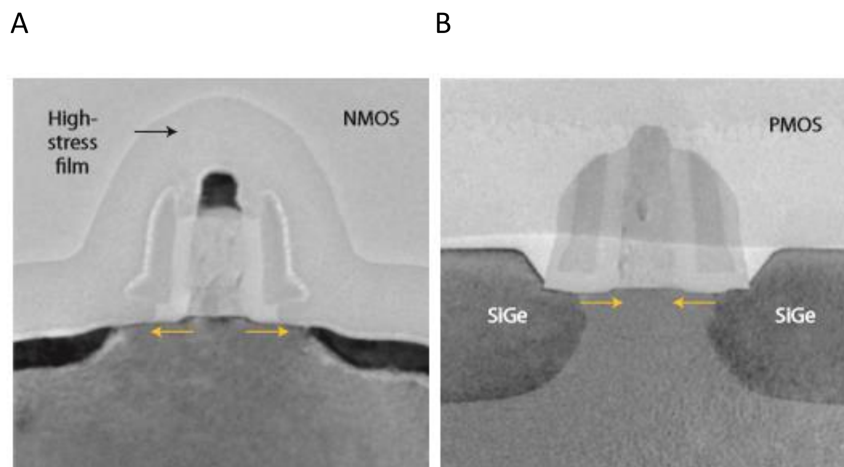


Figure 3: A) Transmission electron microscopy (TEM) image of a nMOS transistor cross-section with deposited high-stress film (silicon nitride) creating a tensile stress in the channel (arrows), and B) TEM image of a pMOS transistor cross-section. The SiGe source and drain regions generate compressive stress in the channel (arrows) **[4]**.

Both methods have limitations related to the maximum applied stress. In the case of the SiGe alloy, the process bottleneck is the creation of dislocations and defects in the Si channel as the stress is increased [20], thus degrading the carriers mobility. As the channel is

downscaled to follow future technological nodes, further research must be done to develop methods for achieving high-stress values in smaller technological nodes for further optimization of the carriers' electrical mobility [7], [12], [21]–[24].

This topic showed how the strain represents a desirable effect for the microelectronic industry. The next topic will demonstrate the opposite case, which is an example of undesirable strain in silicon generated by the electrical interconnects.

1.1.C. Strain Induced by TSV (Through Silicon Via) Interconnect Technology – Undesirable stress

Due to the high complexity of the integrated circuits, the metallic interconnection levels are vias located above the fabricated transistors. The use of these vias permits a high density of interconnects onto the integrated circuit. These vias are vertical electrical connections with high aspect ratio filled with a metal. Depending on the material (examples: Cu and W), intrinsic stress from the metal can induce undesirable stresses at the transistor level [25], changing the electrical characteristics from the transistor in a random way. Another issue is regarded to reliability problems with the isolation of the interconnects [25]. These cases are examples of undesirable stresses induced by the deposition of metals.

1.2. Strain application in MEMS (Micro-electro-mechanical systems) and NEMS (Nano-electro-mechanical systems)

MEMS are devices at the microscale that have mechanical and electrical functionalities with the aim of acting as a sensor or an actuator. In general, these devices have a mobile mechanical part, and most of the MEMS are fabricated on a silicon substrate. It allows full CMOS (Complementary Metal Oxide Semiconductor) compatibility and benefits from the excellent mechanical and electrical properties of silicon [26].

These devices have been successfully employed in industrial application over the last decades as accelerometers, gyroscopes, and micro-mirrors. Several other applications are possible, with its use in chemical, biological, electrical, mechanical, and optical systems [27]. Nowadays, with the advance of the nanofabrication techniques, a new field of research has been introduced: NEMS. This new class of devices comprises machines at the nanoscale that

offer some improved characteristics when compared to MEMS, such as higher working frequencies and improved sensibility due to the smaller mass and dimensions [28], [29].

In the next topics, several examples of MEMS and NEMS will be presented.

1.2.A. Accelerometers

Accelerometers are devices used to measure the acceleration magnitude. The physical mechanism behind the accelerometers is, in general, a proof mass that acts as a string, stretching and compressing, when subjected to an accelerated movement [30]. Then, a transducer is used to transform the mechanical energy into an electric signal. Figure 4A shows an example of a capacitive accelerometer, with a proof mass that is accelerated along the X direction, changing the capacitances by the dielectric thickness variation. Figure 4B is a type of piezoresistive NEM accelerometer. When the proof mass moves in one or more directions, the Si nanowire stretches and change the electrical resistance of the nanowire as a function of time. This type of system takes advantage of the high nanostructures' sensibility, like the giant piezoresistance from silicon nanowires [31], being one of the possible improvements provided by the dimensions scaling.

A B

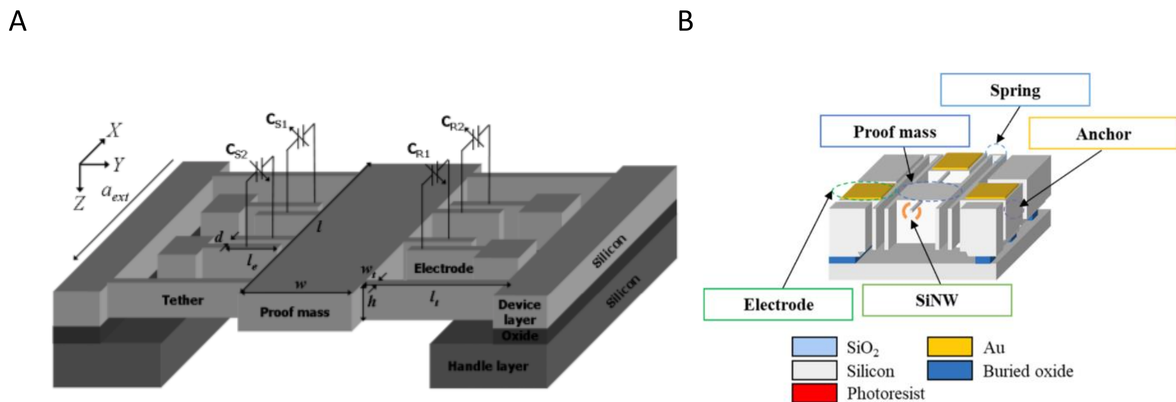


Figure 4: Examples of accelerometers. A) Capacitive accelerometer **[32]**, and B) Piezoresistive accelerometer **[33]**.

1.2.B. Pressure sensors

Some of the microfabricated pressure sensors on silicon employ the piezoresistivity effect. The electrical resistance of silicon is modulated by a strain created upon applied pressure. Therefore, by measuring the electrical resistance and correlating it with the applied pressure, one can calibrate the device. The usual platform employed for these sensors is the microfabricated suspended membranes for improved sensibility [34].

1.2.C. Resonators

Electromechanical resonators are devices that vibrate mechanically under an external stimulus. Figure 5A shows an example of a suspended silicon nanowire resonator and its strained points when vibrating (Figure 5B). The use of nanostructures instead of microstructures allows higher frequencies of operation and higher sensitiveness. Some candidate applications are in mass spectroscopy experiments to detect molecules by the frequency shift from vibrating silicon nanoresonators [35], or even in ultra-sensitive mass sensing [29].

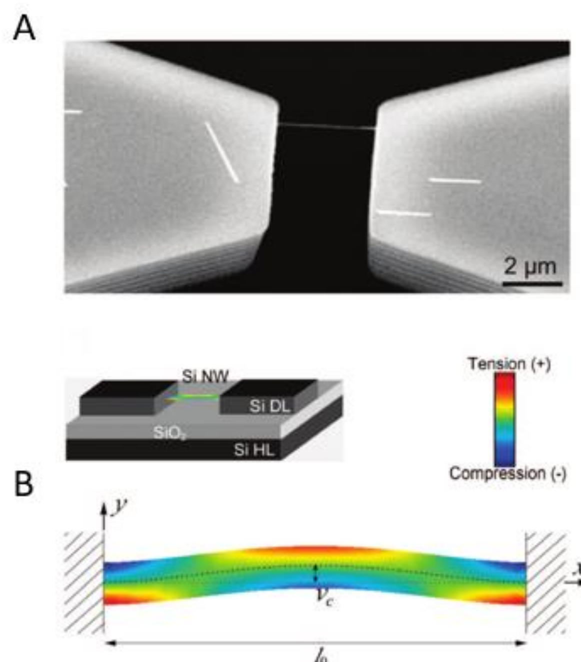


Figure 5: A) Suspended Si nanowire in a nanowire-based resonator, and B) the strain map when the device oscillates, showing the tensioned and compressed regions **[36]**.

1.3. Strain/Stress characterization of nanodevices

With the technological advancement of the strained silicon technologies, two characteristics are observed: the first one is the gradual reduction of the dimensions from microscale down to the nanoscale (below 100 nm). This permitted the creation of devices with improved properties in the fields of microelectronics and NEMS. The second one consists of the continuous search for higher stress levels applied to silicon nanodevices for further electrical mobility enhancement in microelectronics.

In order to permit the downscaling of devices and continuous stress improvement of devices, stress characterization plays a key role in the optimization of the fabrication parameters and choice of the adequate materials and devices geometries. Therefore, prior systematic investigation of the chosen technique in nanoscale prototypes is necessary, with a systematic study in a vast range of applied stresses. Regarding the stress characterization of individual nanostructures, many issues must be addressed such as the spatial resolution of the technique employed, preparation of the sample and the use of invasive methods that changes the stress distribution or even damage the sample. In this sense, the micro-Raman spectroscopy is a well-established non-destructive technique that permits stress characterization with a spatial resolution of below 1 μm and does not require complex sample preparation procedures [37], being an excellent candidate to measure the stress from silicon nanodevices.

1.4. Aim of the Thesis

As previously discussed, strained semiconductors have vast use in several different fields and industrial applications. The ability to accurately measuring the stress/strain applied to a semiconductor is essential for the development of new technologies and products. However, some critical questions arise when dealing with the techniques employed to measure stress on semiconductor devices at the nanoscale. Some essential parameters are the spatial resolution, accuracy, feasibility of the employed technique or if the technique is destructive for the material. As aforementioned, the Raman spectroscopy is a feasible option because of its simplicity, good spatial resolution, and it is a non-invasive technique.

In this thesis, the objective is to investigate the Raman spectroscopy characterization of the stress/strain from highly strained ultra-thin silicon nanostructures. The main challenges that make possible the proper characterization of stressed silicon nanostructures using Raman spectroscopy will be elucidated. For such investigation, the nanofabrication of top-down strained suspended structures was performed as platform prototypes to reproducibly stress nanowires in a wide range (0 up to 6.3 GPa) without the use of external actuators, allowing for the stress/strain control. Then, Finite Element Method (FEM) simulations were performed to quantify the stress, and finally, Raman measurements were carried out. High levels of stresses were found on nanostructures with rectangular cross-section of 15 nm thick and width around 100 – 200 nm. This allowed the systematic investigation of the Raman stress behavior in an unprecedented vast range of applied stresses and permitted the discovery of unexpected Raman behavior of silicon nanostructures subject to high levels of stresses.

1.5. Organization of the Thesis

This thesis is organized in 5 chapters. The first chapter is a motivational introduction for the use of strained semiconductor in different applications and technologies followed by the importance of the stress characterization. Chapter 2 presents an overview of the state-of-the-art of strain characterization methods, with a particular focus for the Raman spectroscopy technique, showing its open issues and challenges. Chapter 3 describes the methodology of this thesis, beginning with the type of nanostructure chosen in order to achieve reproductible low and high stresses in a controllable way at the nanoscale. Then, the nanofabrication procedure is detailed, followed by the stress modelling by FEM simulations. The dimensions measurements by Scanning electron microscopy (SEM) of the fabricated structures and the Raman characterization protocol are demonstrated. Chapter 4 is focused on the results and discussion, beginning with the stress FEM simulation results followed by the Raman results. Then, Raman-stress behavior is discussed in details. Finally, Chapter 5 presents the main conclusions and perspectives of the thesis for future works.

Chapter II - Background

Silicon Stress/Strain Characterization Methods

Here, the most traditional methods to characterize the stress/strain in silicon are discussed. Their main characteristics, physical mechanisms, instrumentation, and applications will be presented. A special focus will be given on the Raman spectroscopy technique, which is the chosen technique of this thesis to accurately measure stress on nanodevices.

2.1. Visual Inspection

When dealing with one-dimensional (1D) structures, such as nanowires or nanotubes, one can perform strain characterization by directly measuring the initial and final dimensions of the structure with a 'ruler'. Generally, the ruler will be used in a captured image of a Scanning Electron Microscope (SEM), Transmission Electron Microscope (TEM), or in optical microscopes in cases of larger structures. Figure 6A shows an example of strain measurement of a Si beam with the use of microfabricated cursors. By the misalignment of the cursors, it is possible to measure the final strain. Figure 6B are sequential images of a nanowire stretched until its fracture. Here, it was used a piezo motor to stretch the nanowire.

A B

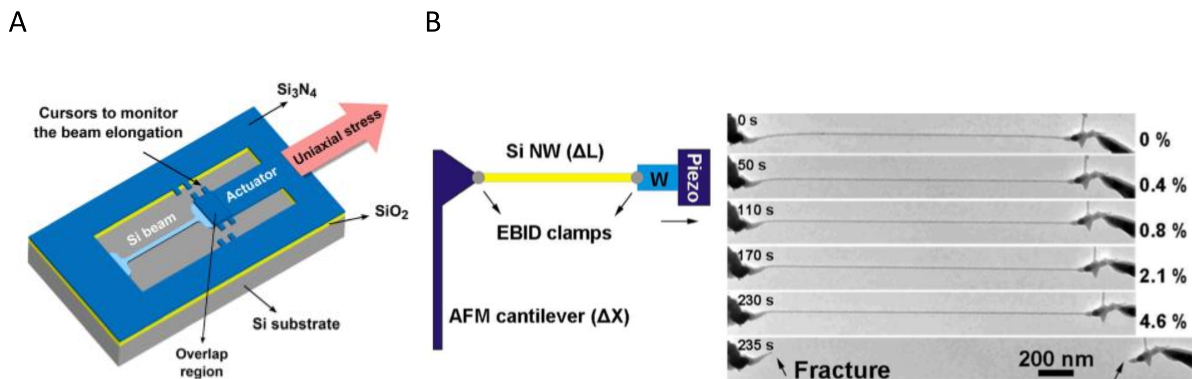


Figure 6: A) Suspended Si beam strained by a silicon nitride actuator **[38]**, and B) Sequential TEM images of a strained Si nanowire until its fracture. It was used a piezo motor to stretch the nanowire **[39]**.

These characterizations demand, in most of cases, careful manipulation of the nanostructures to maintain the system aligned and the use of external systems to stretch the nanowire. It can be used a MEMs system or an Atomic force microscopy (AFM) tip connected to the nanostructure. Also, sometimes it is necessary to care about the clamp between the external actuator and the nanostructure.

The visual characterization is limited to 1D nanostructures and allows the uniaxial strain characterization. Besides, these measurements are limited to structures with uniform uniaxial strain along with it and do not permit local strain measurements from structures with stress gradient.

2.2. X-Ray Diffraction (XRD)

XRD is a classical technique used in different materials for studies of the material's crystallography, strain, grain analysis, crystal phase, and bonds [40]. The analysis is based on the X-Ray diffraction in the crystalline structure.

Figure 7 shows schematically the wavefront of a plane wave impinging on the crystal and the scattered rays with different phases.

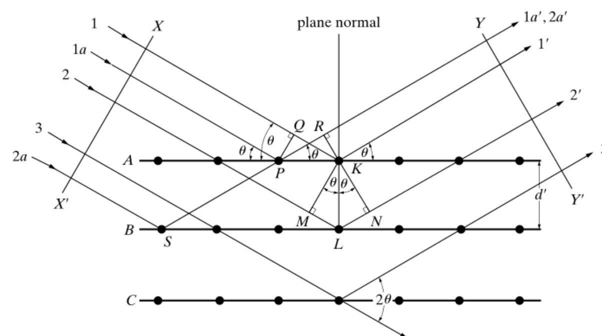


Figure 7: Diagram representing the X-rays diffraction of a plane wave in a crystal **[40]**.

The scattered waves will interfere and create a diffraction pattern, according to Bragg's law:

$$n\lambda = 2d'sin\theta$$

Where d' is the distance between the planes (A to B, B to C) and n is the order of diffraction (n = 1, 2, 3, …). This law indicates the necessary condition to the scattered rays 1' and 2' be in phase. It is possible to see that there are several angles in which a constructive interference of the scattered rays will occur. The analysis of the crystal structure by X-Ray diffraction technique is called structural analysis.

From Bragg's law, if the incident wavelength is known, and the incident angle is measured, the displacement between the planes is characterized. From this fact, it is possible to analyze the diffraction patterns from complex crystal structures and to measure if the material is subjected to a strain. Silicon films have been characterized by XRD in order to quantify its strain and the type o strain (uniaxial, biaxial, shear) [41]. The XRD spatial resolution is several micrometres to millimetres. Some improvements in this technique

permitted the creation of the micro-XRD technique. In this new technique, because of the presence from complex optical systems, the typical spatial resolution is around 0.5 µm [42].

2.3. Transmission Electron Microscopy (TEM)

TEM can be performed to characterize semiconductor materials in the sub-nm spatial resolution. Such a powerful spatial resolution is achieved by the small de Broglie wavelength of electrons that are transmitted through an ultra-thin specimen of the material, in general, just a few tenths of nanometers. With a TEM, it is possible to obtain high-resolution images to analyze the crystalline structure of the material. Figure 8A-top shows an image from a Si nanowire. It is possible to see the periodic atoms' arrangement and the smooth atomic surface (Figure 8A-bottom).

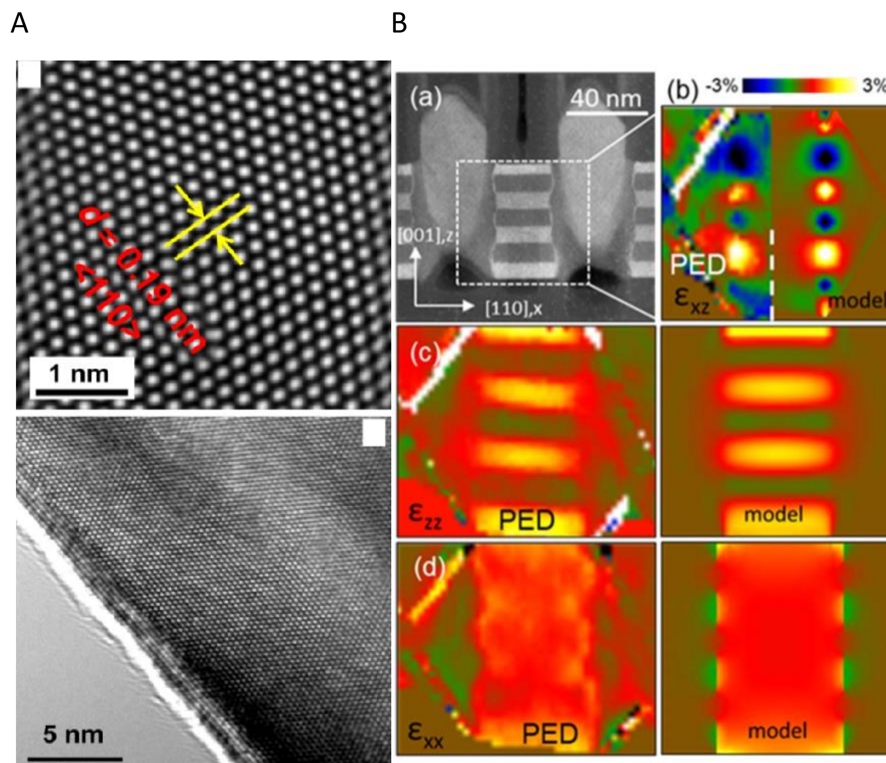


Figure 8: A) HRTEM Si nanowire image **[43]**. On top is shown the placement of the atoms and on the bottom the smooth nanowire surface, and B) (a) Dark field TEM image of a GAA nanosheet transistor on SOI after source/drain epitaxy, (b) ϵ_{xz}, (c) ϵ_{zz}, and (d) ϵ_{xx}. PED (Precession electron diffraction) images with calculated model **[12]**.

TEM characterization requires specific sample preparation. Since the sample must be ultra-thin, it is required the use of special grids that are ultrathin supports to put the target material on the grid. In other types of structures, such as transistors fabricated on silicon wafers, it necessary the preparation of a lamella. The fabrication process of a lamella is very complex, requiring manipulation and material etching in FIB (Focused ion beams) systems [44]. The result is an ultrathin structure that can be analyzed in the TEM system.

The TEM system can also be used for strain measurements with sub-nm resolution. Several techniques have been developed during the last decades [45]. Some examples are Moire interference, convergent beam electron diffraction, geometrical phase analysis, dark field electron holography, and in-line dark field holography [45]. Figure 8B shows a strain map from a GAA Nanosheet transistor compared to a FEM simulation. In this work, it was prepared a lamella from the fabricated transistor. One issue related to the strain characterization of lamellas is that it suffers from strain relaxation in some directions that must be considered when analyzing the data.

2.4. Raman Spectroscopy

The Raman characterization is based on the Raman effect. An incident photon (frequency ω_i, wavevector k_i) from a monochromatic laser source interacts with the crystal. The photon may lose or gain energy interacting inelastically with an electron from the crystal. Part of its energy is transferred to a phonon (frequency ω_j, wavevector q_j), which is a quantized particle related to the modes of vibration from the crystal, in an inelastic energy transfer event. The scattered photon is then emitted in a new state (frequency ω_s, wavevector k_s). Figure 9 shows a schematic of this process. The emitted photon is captured to form a spectrum showing the intensity of emitted photons in function of the shifted wavenumber.

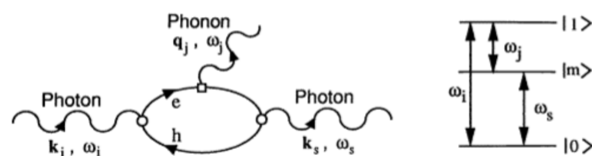


Figure 9: Feynman diagram and energy levels of a Stokes scattering process **[37]**.

In the case of strained samples, mechanical stress may affect the vibration resonance modes in the crystal, thus shifting the frequency of the emitted photon. For semiconductors with diamond crystalline structure (such as silicon and germanium), this effect can be easily verified in the Raman spectrum. Figure 10A shows a spectrum from an unstrained silicon sample in the center, and the shifted peaks from strained silicon samples. Studies on strained silicon have several practical applications in microelectronics. One example is the stress measurement in silicon generated by silicon nitride stressors (Figure 10B). Others examples [37] are the strain measurement on silicon generated by the TSV interconnect technology, isolation, metal deposition, and SiGe stressors.

A B

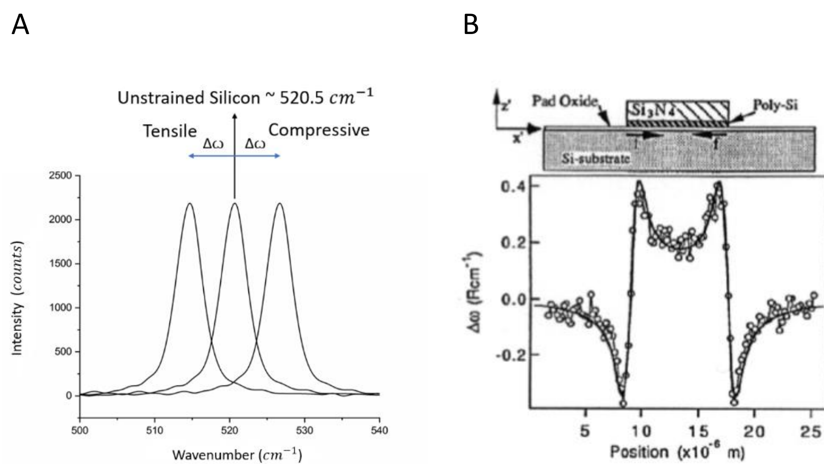


Figure 10: A) The Raman spectra of unstrained silicon (center), uniaxial tensile stressed silicon (left), and uniaxial compressive stressed silicon (right). The Raman shift between the unstrained silicon peak and the shifted strained silicon peak is the quantity Δω. B) Raman shift mapping as function of the device channel position from a Si-based device with a silicon nitride top layer **[37].**

The stress characterization of silicon samples can be quantified by means of Raman spectroscopy with the analytical model demonstrated in Eq. 1 [25]. This model is valid for (001) silicon wafers with negligent shear stress components, and triaxial stress components along the X, Y, and Z axes oriented with the crystallographic directions [110], [-110] and [001], respectively.

$$\Delta\omega = \omega_i - \omega_0 = \frac{1}{2\omega_0}\{[pS_{12} + q(S_{11} + S_{12})](\sigma_{xx} + \sigma_{yy}) + (pS_{11} + 2qS_{12})\sigma_{zz}\}$$

(1)

Where $\Delta\omega$ is the Raman shift (in cm^{-1}) between the unstrained silicon peak ω_0 = 520.5 cm^{-1} and the shifted strained silicon peak ω_i (cm^{-1}). In addition, p and q are the phonon deformation potentials (PDPs) from silicon and the S_{11} and S_{12} are the elastic constants from silicon bulk (Pa^{-1}).Besides, σ_{xx} is the stress (Pa) component along the X-axis ([110]), σ_{yy} (Pa) is the stress component along the Y-axis ([-110]), and σ_{zz} (Pa) is the stress component along the Z-axis ([001]).

Equation 1 relates the shifted Raman peak with the sample stress components. In the case of a sample with uniaxial stress along the [110] direction, we can simplify Eq. 1 by neglecting the σ_{yy} and σ_{zz} stress components, yielding to the Eq. 2:

$$\Delta\omega = SSC \times \sigma_{xx} = \left\{\frac{1}{2\omega_0}[pS_{12} + q(S_{11} + S_{12})]\right\} \times \sigma_{xx}$$

(2)

Here, the Stress shift coefficient (SSC) ($\frac{cm^{-1}}{Pa}$) of uniaxially stressed Si samples along the [110] direction on a (001) plane is defined. Such parameter plays an important role in Raman characterization of uniaxially stressed silicon since the stress component, σ_{xx}, is directly obtained from the Raman shift divided by the SSC. Equation 2 also shows the dependence of the SSC with the PDPs (p and q) and silicon mechanical parameters (S_{11} and S_{12}). Consequently, uncertainties in the PDPs and in the Si mechanical parameters generate systematic errors on the stress characterization of Si samples using Raman spectroscopy.

Therefore, in order to use the micro-Raman characterization for quantitative stress analysis of silicon nanostructures, it is required to investigate the SSC from uniaxially stressed samples. This coefficient will be extracted in this thesis from ultrathin silicon nanostructures subjected to low and high levels of stress. Such coefficient depends on the silicon PDPs and its elastic constants (S_{11} and S_{12}). The elastic constants can be evaluated by the Young modulus and Poisson coefficient [46]. Table 1 shows a compilation of the main works from the literature that reports experimental silicon PDPs extracted under different

stress conditions, and sample thicknesses. The SSC calculated for uniaxially stressed silicon at the [110] crystallographic direction on a (001) surface is also demonstrated. The [110] crystallographic direction on a (001) plane has extensive use in microelectronic devices, with a great impact in technological applications [24].

Table 1: Reported silicon phonon deformation potentials (PDPs) in literature and the stress-shift coefficient (SSC) calculated for uniaxially stressed silicon at the [110] crystallographic direction on a (001) surface. The thickness of the characterized structure (also the smaller dimension) and the stress type with its range are shown as well.

Reference	**PDPs**	**Thickness & Structure**	**Stress (GPa)**	**SSC[a]**
Reference [47] (1970)[b]	p/ω_0^2 = -1.25 q/ω_0^2 = -1.87	1 mm - Wafer	Compr. ~ 0 – 1.15	-2
Reference [48] (1978)[b]	p/ω_0^2 = -1.43 q/ω_0^2 = -1.89	1.3 mm - Wafer	Compr. ~ 0 – 1.8	-1.93
Reference [49] (1990)[b]	p/ω_0^2 = -1.85 q/ω_0^2 = -2.31	~1 mm - Wafer	Tensile ~ 0 – 1.2	-2.3
Reference [50] (2007)[b]	-	- - Film	Biaxial	-2.13
Reference [51] (2009)	p/ω_0^2 = -1.56 q/ω_0^2 = -1.98	- - Wafer	Tensile ~ 0 – 0.2	-1.99
Reference [52] (2012)[b]	p/ω_0^2 = -1.85 q/ω_0^2 = -2.25	70 nm - Film	Tensile Biaxial ~ 1.3	-2.22
Reference [53] (2013)[c]	-	200 nm - Nanostructure	Tensile ~ 0 – 4.5	-2.03
Reference [38] (2018)[d]	-	100 nm - Nanostructure	Tensile ~ 0 – 2.5	-2.4

[a]SSC from references 47, 48, 49, 51, and 52 were calculated using the corresponding PDPs and bulk silicon elastic constants (S_{11}= 7.68 x 10^{-12} Pa^{-1}, and S_{12} = -2.14 x 10^{-12} Pa^{-1}) using Eq. 2. The SSC from reference 38, and our work were determined experimentally.

[b]The PDPs and SSC values from these references are also reported in Ref. 25.

[c]The SSC was calculated from the strain-shift coefficient and the bulk silicon Young modulus (169 GPa) along the <110> direction.

[d]P-type doped nanostructure (10^{16}atoms/cm^3).

As shown in Table 1, the broad variation in the SSCs values can be attributed to the large dispersion presented at the PDPs values reported. Such variation is related to factors

like surface orientation, scattering effects, light polarization, temperature, surface effects, still being under debate by the scientific community [25], [53]. Another open question in the academy [54] is the Young modulus reduction in thin silicon samples or nanowire structures. Several simulations works simulations have reported that a reduction in the Young modulus should be expected only for structures with dimensions smaller than around 10 nm [55]–[58]. In addition, experimental works demonstrate constant Young modulus of bulk silicon [39], [59]–[62] for structures with dimensions between 10 – 100 nm, being in good agreement with the theoretical works. On the other hand, some experimental works report a considerable diminishing of the Young modulus for silicon thin films or silicon nanowires with dimensions smaller than 100 nm [43], [63]–[66]. Such different conclusions are highly dependent on the nanowire geometry, fabrication-induced defects, as well as the methods used for the parameters extraction and the auxiliary analytical models employed. All these variables require a deeper investigation and dedicated experiments would be needed to shed light on this observation in order to conclude on the dimensionality effects of the Young modulus [54], [67], [68].

The study of the SSC permits the correct stress quantification from silicon samples under uniaxial stress using Raman spectroscopy. Nevertheless, as aforementioned, this topic is complex because of the experimental challenges in determining the PDPs. In the case of nanostructures, the challenge increases significantly because of the size-effect phenomena that may affect both the mechanical parameters and the PDPs [38], [53], [69]. Additionally, the intrinsic difficulty when fabricating, characterizing, stressing and modelling structures at the nanoscale imposes a greater difficulty compared to the macro-scale. The scarce number of works performed on structures at the nanoscale, with the smallest dimension around 100 nm [38] and 70 nm [52], as shown in Table 1, corroborates this affirmation. Furthermore, there is a very limited quantity of works that performs such stress characterization on nanostructures compared to thin films or wafers. Another challenge relies both on the stress level and the choice of the platform used for applying such high-stress. So far, most of the works are limited to stress values smaller than 2 GPa (Table 1). For the case of silicon subjected to higher stresses (greater than 4.5 GPa), it has never been investigated the Raman shift-stress behavior systematically. Recently, in the work of Gassenq et al. (2016) [42], highly strained germanium microbridges showed an unexpected quadratic deviation of the Raman shift-strain behavior for strains higher than 1.2%, demonstrated by Micro-XRD

measurements and ab initio simulations. This behavior required calibration of the Raman shift-strain model. Since silicon is a material with a diamond crystallographic structure, similar to germanium, the study of highly stressed silicon structures becomes necessary for the investigation of possible unexpected model corrections, allowing accurate stress characterization by Raman spectroscopy.

In this thesis, the SSC will be quantified for ultra-thin (15nm) silicon nanostructures, of 100 – 200 nm width, along the [110] direction. A vast range of stress (0 – 6.3Gpa) was achieved using a suspended nanobridge platform. This work extended the range of applied stress from 4.5 GPa (Table 1) up to 6.3 Gpa in silicon nanostructures with 15 nm thickness. The SSC obtained is in good agreement with some works from the literature. For ultra-high stresses (greater than 4.5 GPa), an unexpected deviation from the linear model (Eq. 2) has been observed, similar to the case of germanium. Then, it was presented for the first time in silicon a new corrected model for higher stresses.

In this chapter, an overview of the main methods to characterize the strain/ stress from semiconductor samples were discussed. At the end of the chapter, the Raman spectroscopy technique had a special focus, demonstrating the state-of-the-art from stress measurements in stressed silicon and its open issues and challenges. In the next chapter, the methodology of this thesis is illustrated, presenting the theoretical and simulation details of the characterized silicon nanostructure, the nanofabrication procedure, the dimensions characterization by Scanning electron microscopy (SEM) and the Raman measurements protocol.

Chapter III - Methodology

In this chapter, the methods used to achieve highly stressed silicon nanostructures is presented. It is demonstrated the underlying physical mechanisms from the stressed silicon nanostructures, called suspended nanobridges. The stress/strain evaluation can be performed by two methods. The first method is a simplified analytical model that has several limitations, being mainly used for educational purposes. The second method is the finite element method (FEM) simulation that has greater accuracy in evaluating the stress from the nanostructure. Then, the nanofabrication procedure is detailed, followed by the FEM simulation and the dimensions characterization of the nanostructures using the scanning electron microscopy technique. The final part explains the Raman protocol developed in this thesis.

3.1. Suspended Nanobridge: Analytical Modelling

Figure 11A shows the top view of a nanobridge comprising a central nanowire (NW) in between two pads. This nanobridge is fixed at the two lateral borders and has initial tensile uniform stress. The stress is uniformly maintained because this structure is fixed to a sacrificial substrate underneath the bridge. By removing the sacrificial SiO_2 layer under the top-silicon surface, the suspended nano bridge (Figure 11B) has the nanowire region with an amplified uniaxial tensile stress. On the other hand, the pads relax due to the larger cross-section area. Such a phenomenon occurs because the resultant forces in each segment of the nanobridge must sum up to zero under equilibrium conditions. Since the nanobridge has a uniform thickness and the nanowire region has a smaller cross-section, during the suspension process it will be subjected to a larger longitudinal force compared to the pads. Consequently, the nanowire will stretch in order to achieve equilibrium conditions.

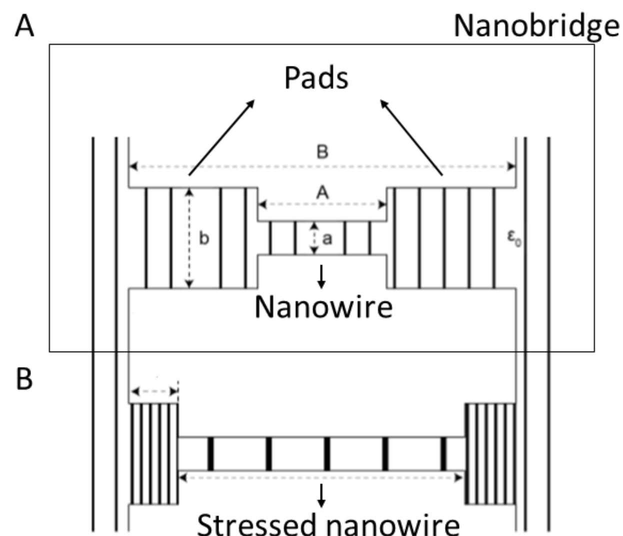


Figure 11: Nanobridge dimensions and stress mechanism. A) Top view of a nanobridge with its dimensions before the suspension. The parameters **A**, **B**, **a** and **b** refer to the NW length, the bridge length, the NW width and the pad width, respectively, and B) Top view of a nanobridge after suspension. **(Modified from Ref [70])**

A simplified one-dimensional analytical model can be deduced by considering: 1) The amount that the central nanowire is stretched is precisely what the pads relax, 2) The material behaves linearly with the applied stress (Hooke's law). The deduction of this model

is demonstrated and discussed in References [22], [70]. Here, it is demonstrated some details.

From consideration 1 and from the fixed constraints in the lateral borders of the nanobridge leads to Eq. 3:

$$\epsilon_0 B = \int_{-\frac{B}{2}}^{+\frac{B}{2}} \epsilon_{xx}(x)dx$$

(3)

where ϵ_0 and $\epsilon_{xx}(x)$ are the initial tensile strain from the wafer and the longitudinal strain along the nanobridge, respectively. Then, by splitting the $\epsilon_{xx}(x)$ component into two news terms lead to Eq. 4:

$$\epsilon_{xx}(x) = \begin{cases} \epsilon_{pad}, & -\frac{B}{2} < x < -\frac{A}{2} \\ \epsilon_{nw}, & -\frac{A}{2} < x < +\frac{A}{2} \\ \epsilon_{pad}, & +\frac{A}{2} < x < +\frac{B}{2} \end{cases};$$

(4)

where ϵ_{pad} and ϵ_{nw} are the longitudinal strain along the pads and the longitudinal strain along the nanowire, respectively. After the suspension, the resultant force acting in each segment of the nanobridge must sum up to zero (equilibrium condition). From this condition and from the fact that the nanobridge has a uniform thickness, the stresses at the nanobridge follows the relation $\frac{\sigma_{pad}}{\sigma_{nw}} = \frac{a}{b}$, where σ_{pad} and σ_{nw} are the pad longitudinal stress and nanowire longitudinal stress, respectively. Due to condition 2 (Hooke's law), the strain components have the same behaviour, as demonstrated in Eq. 5:

$$\frac{\epsilon_{pad}}{\epsilon_{nw}} = \frac{a}{b};$$

(5)

Thus, merging Equations 3 and 4 leads to Eq. 6:

$$\epsilon_0 B = (B - A)\,\epsilon_{pad} + A\,\epsilon_{nw};$$

(6)

From Equations 5 and 6, it is obtained Eq. 7:

$$\frac{\epsilon_{nw}}{\epsilon_0} = \frac{\left(\frac{A}{B-A} + 1\right)}{\left(\frac{A}{B-A} + \frac{a}{b}\right)};$$

(7)

Equation 7 was validated in Reference [22], as demonstrated in Figure 12. It shows that the qualitative behavior of the strain as a function of the nanobridges dimensions follows the analytical model. Then, the increase of the pad width, **b**, or the reduction of the nanowire width, **a**, yields to an increase the nanowire's longitudinal strain. This nanobridge platform has stressed the nanowire without the use of external actuators and has allowed controlling the stress/strain of the nanowire region by changing the dimensions of the nanobridge (**a**, **b**, **A**, **B**). By modifying the dimensions **a** and **b**, the relation between the cross-sectional area of the nanowire and pads is modified, thus resulting in different static equilibrium situations with different stresses at the nanowire region.

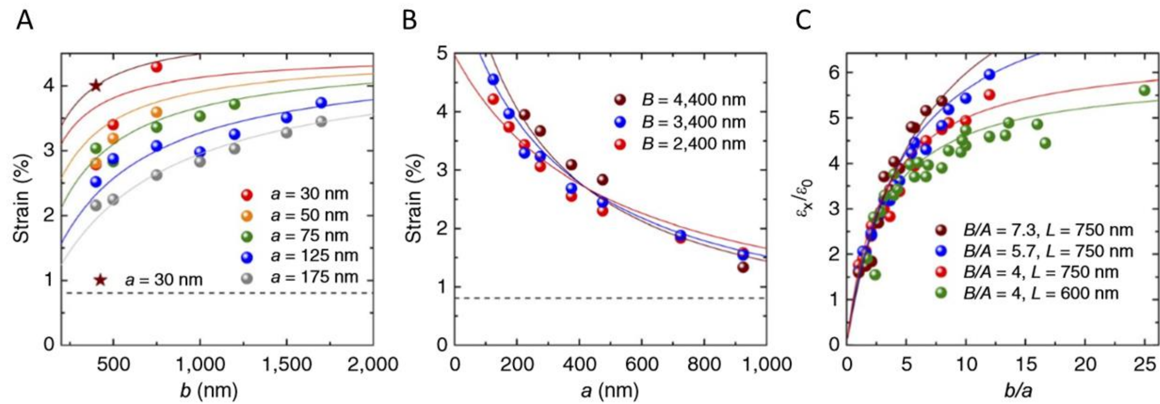


Figure 12: Strain dependence on the dimensions of the nanobridges. A) Longitudinal strain of the NW as function of the pad width, **b**, for **B** = 2.4 µm and **A** = 0.6 µm, and different NW width, **a**. As already mentined, **A**, **B**, **a** and **b** refer to the NW length, the bridge length, the NW width and the pad width, respectively, and **L** refers to the under-etched length. The under-etched length, **L**, is 600 nm for the circle symbol keys, whereas 750 nm for the star symbol key. The initial strain of the wafer is plotted for reference (dashed line), B) Strain as a function of the nW width a for a constant pad width b = 1.5 µm and L = 750 nm. The wire length is A = 0.6 µm, whereas the bridge length was varied from B = 2.4 to 4.4 µm. The initial strain of the wafer is plotted for reference (dashed line), and C) strain enhancement versus the ratio b/a for NWs with different b and a values. The curved lines were obtained from equation. (1), whereas the points represent experimental measurements **(Figure and legend (modified) taken from Ref [22]).**

This analytical model has several limitations that reduce its accuracy. Some neglected parameters that limit the model accuracy are the material anisotropy, crystallographic orientation, the shape of the under etching zone and the fillets. A detailed discussion from these limitations is demonstrated in Reference [70]. In order to solve all these limitations, it is proposed a FEM modelling that will be discussed in Section 3.3 of this thesis.

3.2. Nanofabrication Process

3.2.A. Overview

The fabrication procedure requires a strained silicon-on-insulator (sSOI) wafer (001) (Figure 13A), composed of a top pre-stressed silicon thin film (0.8% biaxial tensile strain of around 1.44 GPa biaxial tensile stress) of 15 nm-thick on the top of an intermediate sacrificial layer (silicon dioxide) of 145 nm-thick on a bulk silicon substrate. It was used

electron-beam-lithography (EBL) to define a central nanowire located in between two pads, which was oriented along the <110> crystallographic direction (Figure 13B). Then, a dry etching process of the unprotected top silicon layer and resist removal (Figure 13C) is performed. In the next step, as the silicon dioxide is exposed, selective wet etching is performed to remove the sacrificial layer under the nano bridge (Figure 13D). As a result, the final suspended nanobridge structure (Figure 14) has the nanowire region holding amplified uniaxial stress and the pads relaxed due to the smaller cross-section area of the nanowire compared to the pads region.

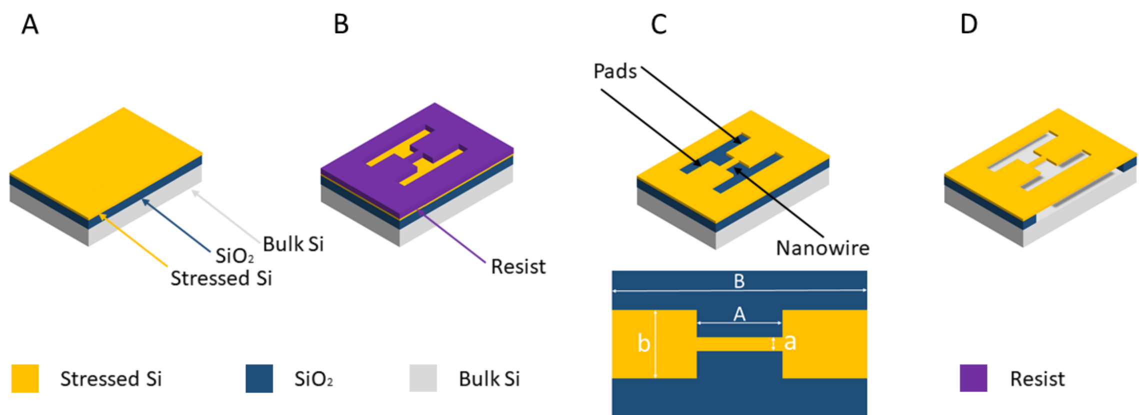


Figure 13: Nanofabrication steps: A) sSOI Wafer, B) After nanobridge pattern transfer by ebeam lithography, C) After dry etching and resist removal. The dimensions from the nanobridge are also shown (a = NW width, b = Pad width, A = NW length, B = Nanobridge length), and D) Suspended nanobridge after selective wet etching.

Figure 14 shows two examples of fabricated nanobridges with different geometries. In both cases, it is possible to check the irregular delamination zone caused by the wet etching process (step D).

A) B)

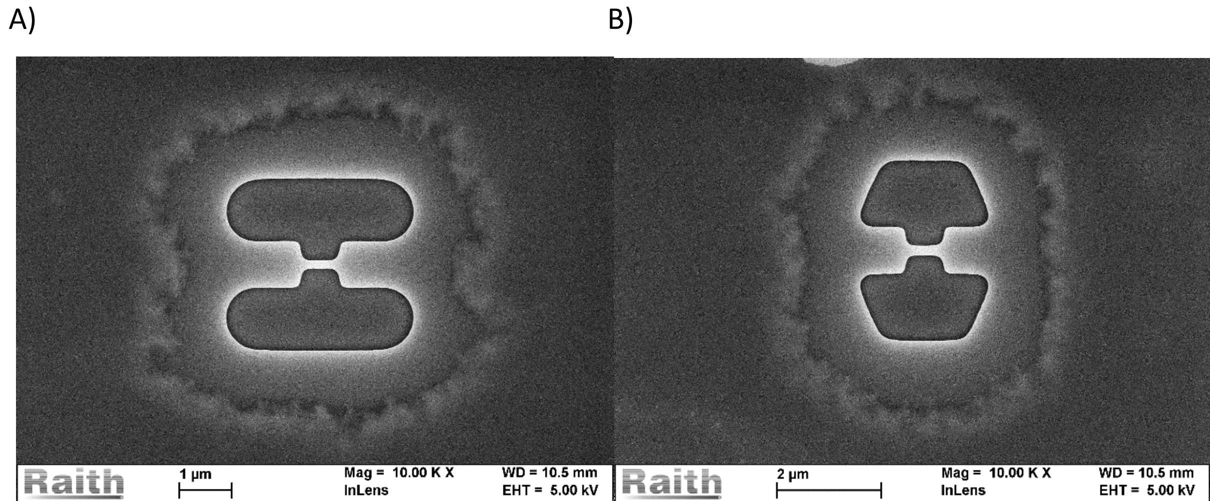


Figure 14: Fabricated Suspended Nanobridges. A) Nanobridge with the inner region in a circular shape , B) Nanobridge with the inner region in a trapezoidal shape.

This platform stressed the nanowire without the use of external actuators, thus allowing to control the stress/strain at the nanowire region. This was achieved by changing the dimensions of the nano-bridge (**a**, **b**, **A**, **B**) by means of EBL, and employing a wet etching recipe in order to modulate the final stress by increasing or decreasing the suspended area. In this work, the dimensions A around 700 nm, and B around 2800 - 3600 nm were fixed. Then, it was varied the dimensions *a* and *b* between 100 - 200 nm, and 500 - 1700 nm, respectively, as well as the under etched volume. The ratio of the cross-sectional areas between the nanowire and the pads was modified by changing the dimensions *a* and *b*, thus resulting in different static equilibrium situations with different stresses at the nanowire region. In addition, the stress of the nanowire region was enhanced as the under etched volume was increased.

The next topics provide more details on each nanofabrication step.

3.2.B. Layout Design

The layouts were designed using the free software KLayout. Two different types of nanobridges were created, as demonstrated in Figure 15A (the inner region with the trapezoidal shape) and Figure 15B (the inner region with the circular shape). These two types of nanobridges were fabricated in order to check if we could achieve greater stresses by reducing possible stress accumulation points with a circular shape. However, no significant

changes were observed. Figure 16 is a layout of nanobridges with several distinct dimensions.

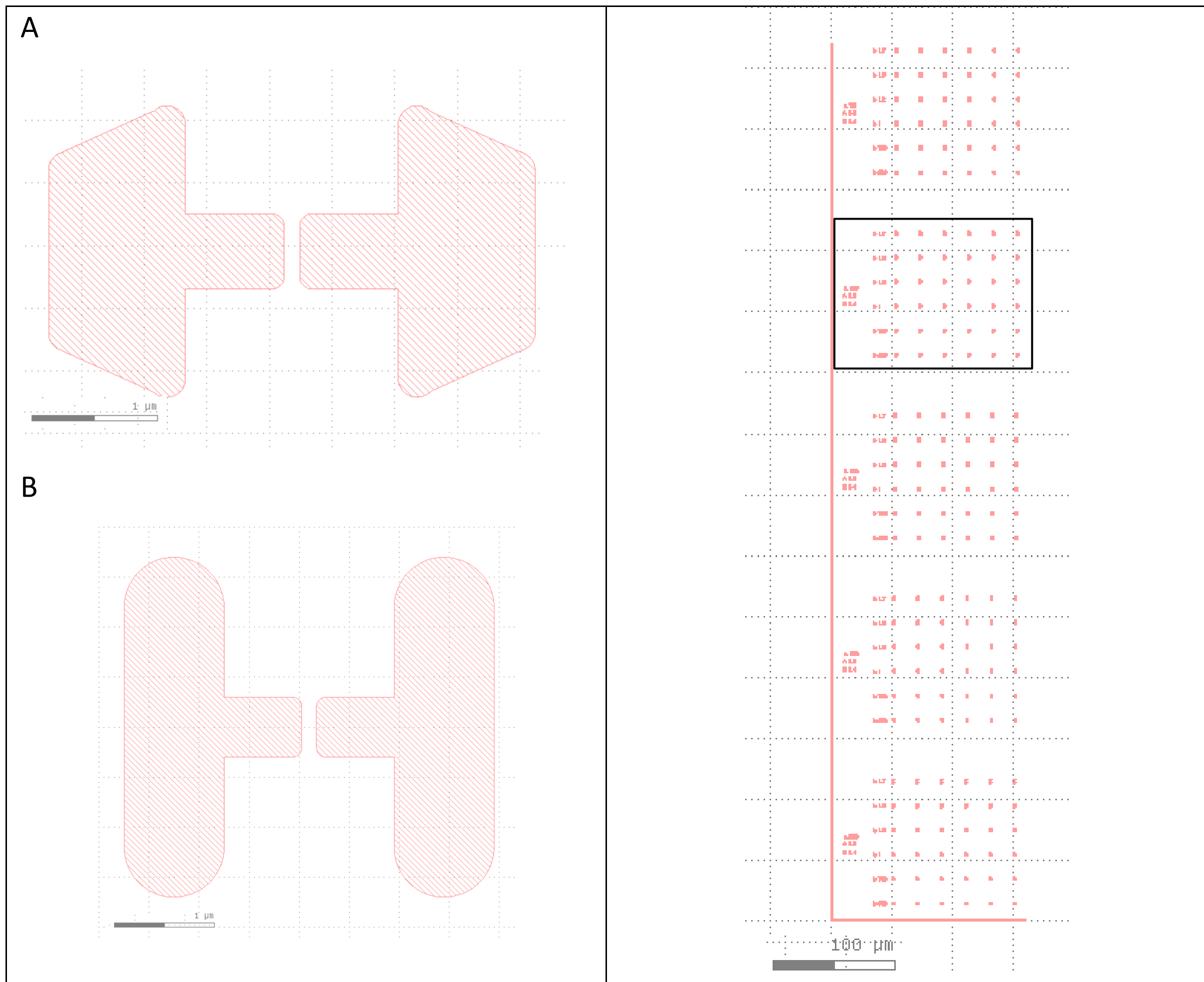


Figure 15: Fabricated nanobridges. A) Trapezoidal nanobridge and B) Circular nanobridge The shaded areas correspond to the region where the electron beam impinges the electron-sensitive resist for further revealing process during the lithographic steps. The scale bar corresponds to 1 µm.	Figure 16: Complete layout with 180 nanobridges. This layout is composed of 5 blocks with the NW width dimension, **a,** equal to 75, 100, 150, 150, 175, and 200 nm. Each one of these blocks has 6 lines with **b** dimensions equal to 500, 750, 1000, 1200, 1500, and 1700 nm. Each one of these lines has 6 identical nanobridges. Every nanobridge has the following dimensions: A = 700nm, and B = 3000 nm. The total number of devices for each layout is 180.

The measurements were performed in a selected number of nanobridges (49) because of the limited time. Nanobridges were selected in order to guarantee a vast range of stress.

3.2.C. E-beam Lithography

The electron-sensitive resist recipe was calibrated to achieve a minimal dimension of around 75 nm. We have used the Poly(methyl methacrylate), PMMA, ARP 679.04 resist manufactured by Allresist. The recipe was:

PMMA resist spinned during 40 s at 6000 rpm. Lithography using the Raith Eline Plus system, acceleration voltage of 30 KV, electron aperture of 7 µm and dose of 300 µC/cm^2 .

These parameters were calibrated according to the resist datasheet and by tests performed with a vast rage of doses. The resist revelation process was performed with the ARP 600-52 developer, for 2 minutes. The result is shown in Figure 17A. It is important to mention that the nanobridge was fabricated along the [110] crystallographic orientation. Such alignment is possible because of the wafer's chamfer indicating the [110] direction.

3.2.D. Dry Etching

After step 3.2.C, a hard-bake process of 125 ^{o}C for 5 minutes was performed to densify the resist in order to prepare it for the dry etching process. The plasma etching was carried out into an Oxford Plasmalab100 reactor with the following recipe:

35 sccm Ar + 12 sccm SF_6 + 100W RF + 50mTorr – duration 15s

This step aims to etch the Si thin film (15 nm) anisotropically from the unprotected regions, patterning the nanobridge on the wafer.

After the dry etching process, the electron resist was removed. We have used an organic cleaning process (10 minutes immersion in CMOS-grade acetone followed by a 10 minutes immersion in isopropanol – both steps performed at hotplate) for resist removal. Then, we performed a stripping process in oxygen plasma asher (O_2 plasma cleaning: 100 W Power, 50 sccm O_2, 100 mTorr) to remove the remaining resist. The result is shown in Figure 17B.

A) B)

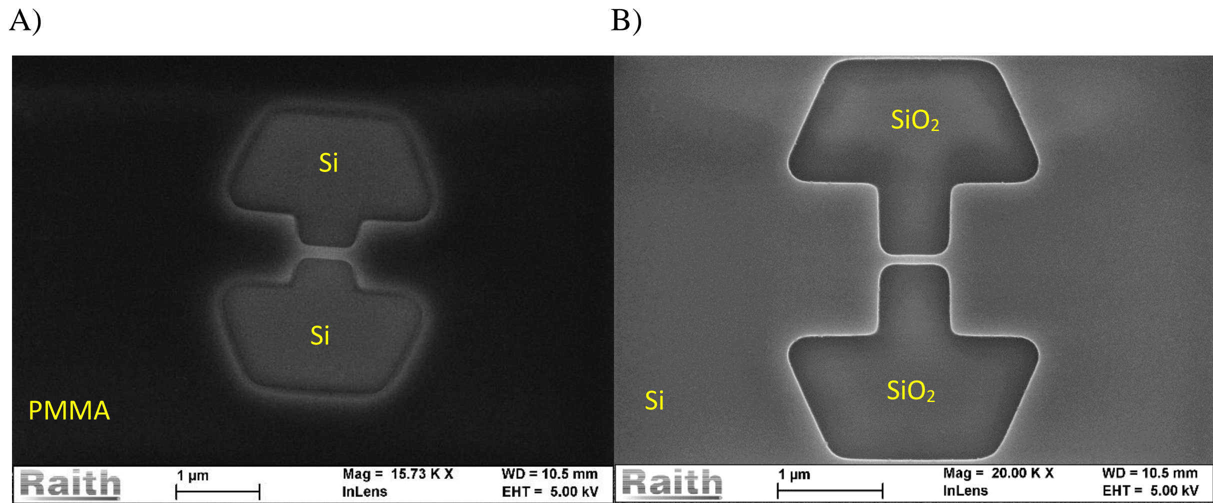


Figure 17: A) Nanobridge after resist developing process. The darker region is PMMA, and the lighter one is the exposed silicon. B) Nanobridge after dry etching and resist removal. The inner regions are the exposed silicon dioxide, and the outter region is the Si thin film.

3.2.E. Wet Etching

The wet etching process for nanobridge suspension was made in a buffer solution of hydrofluoric acid (NH_4F:HF = 6:1). This solution selectively and isotropically etches the silicon dioxide for the nanobridge suspension.

The etching procedure was carried out in several steps to verify the stopping point by means of scanning electron microscopy (SEM) images (under etching dimension control). This is a critical step because, during the suspension, the nanowires become highly stressed. These high-stress values can eventually create a mechanical fracture in the nanowire, then breaking the nanobridge. Thus, it was inserted the sample carefully into the acid buffer and take it out from the solution followed by a water immersion to stop the etching process. The drying process was performed on a hotplate to avoid the use of ultra-pure nitrogen jet that can break the nanowires. The results are shown in Figure 18A and Figure 18B.

The nanobridges from Figure 18A and Figure 18B are fully suspended to permit the relaxation of the pads and increase of the stress from the nanowire region. Figure 19A shows an example of a partially suspended nanobridge. This partial suspension aims to achieve a low stressed nanowires (2 up to 4 GPa) because the pads are not fully relaxed.

A) B)

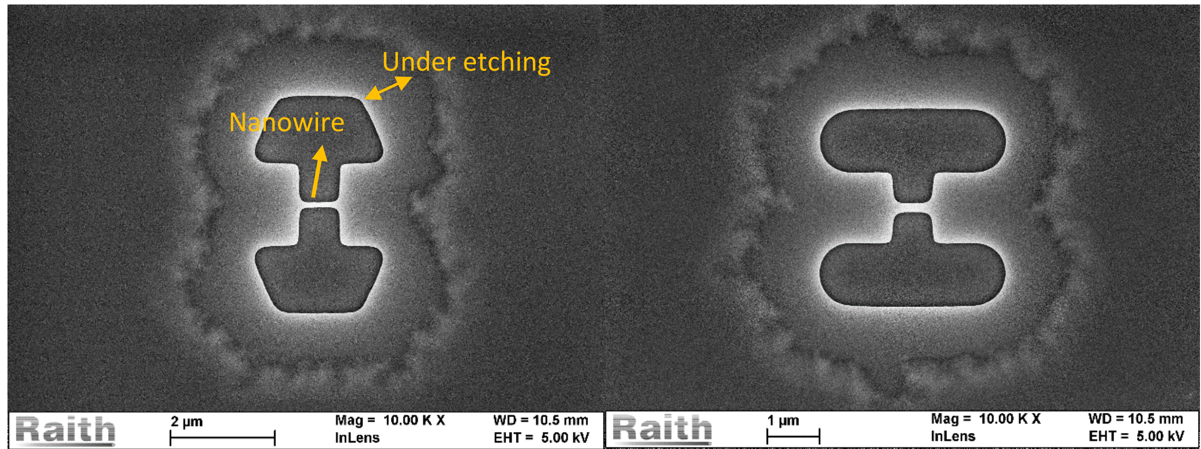


Figure 18: Nanobridges after the wet etching process. The under etching zone corresponds to the suspended region, where the HF buffer has etched the silicon dioxide. A) Nanobridge with the layout from Figure 15A, B) Nanobridge with the layout shown in Figure 15B.

3.3. FEM Modelling

Note: For further details from the FEM Modelling, check the thesis from the PhD student José Luis Arrieta Concha, FEEC – UNICAMP, who was the main responsible for the FEM modelling shown in this work.

In general, analytical models may have simplifications that can reduce their accuracy. Therefore it was used the finite element method (FEM) simulations [46] to achieve high accuracy in determining the stress on the nanowire by considering all the geometrical dimensions (as shown in Figure 13C), as well as other parameters such as the corner radius and the corrosion profile. The 3-dimensional FEM computational analysis was performed using COMSOL Multiphysics®. A scanning electron microscopy (SEM) was employed to measure the dimensions of the fabricated nanostructure and then to accurately achieve geometric representation and realistic physics modelling. With these measurements, it was possible to build the exact geometry for the nanobridge structure and the under etched corrosion profile for each of the fabricated samples with relatively good precision. Figure 19A shows the fabricated structure and Figure 19B illustrates the geometry modelled in COMSOL for a side-to-side comparison. In the case of the nanobridge shown in Figure 19A, one can observe that the pads are partially suspended on the top of the silicon dioxide. This partial corrosion aims to achieve nanowires with lower stresses (2 up to 4 GPa).

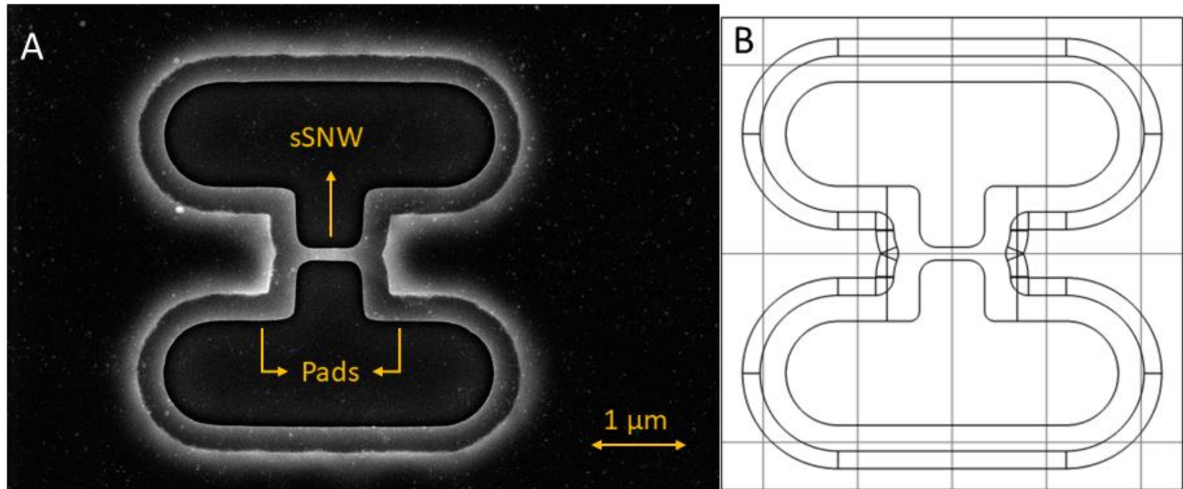


Figure 19: A) Top-view SEM image of the fabricated nanobridge with dimensions a = 138 nm, b = 1431 nm, A = 690 nm, B = 3520 nm, and average under etching of 273 nm, and B) Corresponding simulated COMSOL geometry.

The FEM model was set under the assumption of linear elasticity [22], [71]. The boundary conditions were set to initial strain of 0.8% in the biaxially pre-strained x-y layer according to the wafer specifications [72], fixed constraint opposite to the sample surface, and roller condition on the surfaces framing the structure. The materials stiffness was set to asymmetric by using the stiffness tensor C_{ij} in Voigt notation. In addition, we have used the tensor formalism, which permitted the use of the generalized Hooke's law [73], [74]. The generalized Hooke's law for a linear elastic material is demonstrated in Eq. 8.

$$\sigma_{ij} = \sum_{k=1}^{3} \sum_{l=1}^{3} C_{ijkl} \, \varepsilon_{kl} \tag{8}$$

where C_{ijkl} is the second-order stiffness tensor, ε_{kl} is the strain and σ_{ij} is the stress. The subscripts *ij* corresponds to the Cartesian axes. Equation 8 can be simplified to a short-hand matrix notation [75]. Then, by symmetry relations like $\varepsilon_{12} = \varepsilon_{21}$, $\varepsilon_{13} = \varepsilon_{31}$, and $\varepsilon_{23} = \varepsilon_{32}$ between shear stresses to substitute the subscripts using the following rules: 11→1, 22→2, 33→3, 32→4, 31→5, and 21→6. Then, Eq. 8 is simplified to Eq. 9:

$$\begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \sigma_4\\ \sigma_5\\ \sigma_6\end{bmatrix}=\begin{bmatrix}C_{11} & C_{12} & C_{13} & C_{14} & C_{15} & C_{16}\\ C_{21} & C_{22} & C_{23} & C_{24} & C_{25} & C_{26}\\ C_{31} & C_{32} & C_{33} & C_{34} & C_{35} & C_{36}\\ C_{41} & C_{42} & C_{43} & C_{44} & C_{45} & C_{46}\\ C_{51} & C_{52} & C_{53} & C_{54} & C_{55} & C_{56}\\ C_{61} & C_{62} & C_{63} & C_{64} & C_{65} & C_{66}\end{bmatrix}\begin{bmatrix}\varepsilon_1\\ \varepsilon_2\\ \varepsilon_3\\ \varepsilon_4\\ \varepsilon_5\\ \varepsilon_6\end{bmatrix}$$

(9)

The shorthand notation allows the use of matrix algebra. However, Equation 9 can be further simplified because of the cubic crystallography and orthotropic linear elasticity of silicon [74], reaching to Eq. 10 which is the stiffness matrix C in the [100]-crystal axes.

$$\begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \sigma_4\\ \sigma_5\\ \sigma_6\end{bmatrix}=\begin{bmatrix}C_{11} & C_{12} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & C_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & C_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & C_{44}\end{bmatrix}\begin{bmatrix}\varepsilon_1\\ \varepsilon_2\\ \varepsilon_3\\ \varepsilon_4\\ \varepsilon_5\\ \varepsilon_6\end{bmatrix}$$

(10)

The values of C_{11}, C_{12} and C_{44} for undoped silicon are reported in References [76] and [77]. We have used these references to get the values of C_{11} =165.64 GPa, C_{12} = 63.94 GPa and C_{44} = 79.51 GPa, yielding to the Eq. 11.

$$\begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \sigma_4\\ \sigma_5\\ \sigma_6\end{bmatrix}=\begin{bmatrix}165.64 & 63.94 & 63.94 & 0 & 0 & 0\\ 63.94 & 165.64 & 63.94 & 0 & 0 & 0\\ 63.94 & 63.94 & 165.64 & 0 & 0 & 0\\ 0 & 0 & 0 & 79.51 & 0 & 0\\ 0 & 0 & 0 & 0 & 79.51 & 0\\ 0 & 0 & 0 & 0 & 0 & 79.51\end{bmatrix}\begin{bmatrix}\varepsilon_1\\ \varepsilon_2\\ \varepsilon_3\\ \varepsilon_4\\ \varepsilon_5\\ \varepsilon_6\end{bmatrix}$$

(11)

The compliance matrix from Eq. 11 is related to silicon in the [100] frame of reference. To change this equation for the standard (100) silicon wafer with the cartesian directions aligned in the [110], [-110] and [001] crystallographic directions, it was performed a standard 45° rotation of the compliance matrix [78], resulting in Eq. 12.

$$\begin{bmatrix}\sigma_1\\ \sigma_2\\ \sigma_3\\ \sigma_4\\ \sigma_5\\ \sigma_6\end{bmatrix}=\begin{bmatrix}194.30 & 35.28 & 63.94 & 0 & 0 & 0\\ 35.28 & 194.30 & 63.94 & 0 & 0 & 0\\ 63.94 & 63.94 & 165.64 & 0 & 0 & 0\\ 0 & 0 & 0 & 79.51 & 0 & 0\\ 0 & 0 & 0 & 0 & 79.51 & 0\\ 0 & 0 & 0 & 0 & 0 & 50.85\end{bmatrix}\begin{bmatrix}\varepsilon_1\\ \varepsilon_2\\ \varepsilon_3\\ \varepsilon_4\\ \varepsilon_5\\ \varepsilon_6\end{bmatrix} \tag{12}$$

Equation 12 is the relation of the anisotropic elasticity matrix of silicon on a (100) silicon wafer with the cartesian axes aligned in the [110], [-110] and [001] directions. This equation was inserted into the COMSOL's material properties to represent the material's mechanical properties accurately.

3.4. Dimensions Characterization

The nanobridge dimensions were measured using SEM images with distinct magnifications to reduce the measurement error. As an example, Figure 20 shows a top-view SEM image with a 70 kX magnification employed to quantify the nanowire width, length, and pad width.

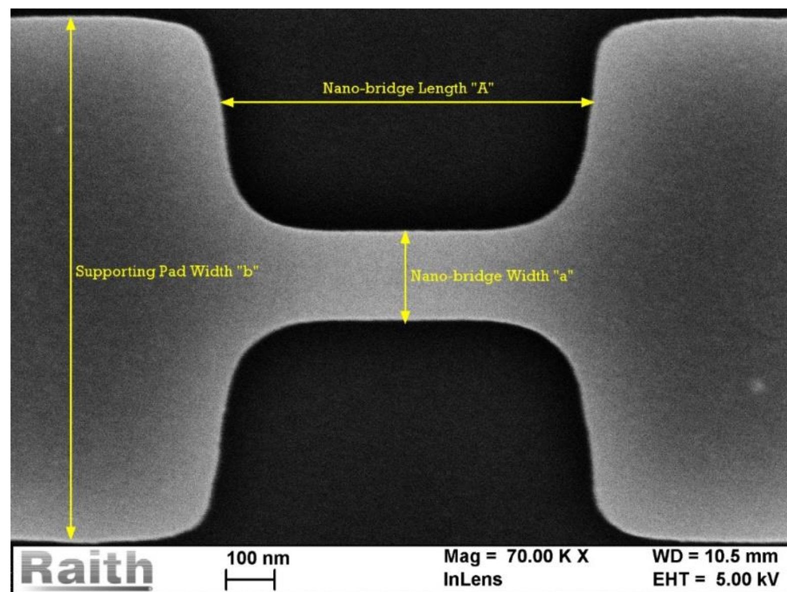


Figure 20: Nanobridge image with zoom of 70 kX. The large magnification minimizes errors when measuring the device dimensions.

Now, in order to improve the simulation accuracy, the irregular etched profile of the silicon dioxide layer was measured at several points around the fabricated structure and then included into the simulation model for all simulated nanobridges. Figure 21A shows the SEM image of one fabricated nanostructure and the guidelines used to perform the measurements of the corrosion profile in the edges. Figure 21B shows the equivalent modelling with the COMSOL CAD, which is very accurate when compared to the image of the fabricated structure.

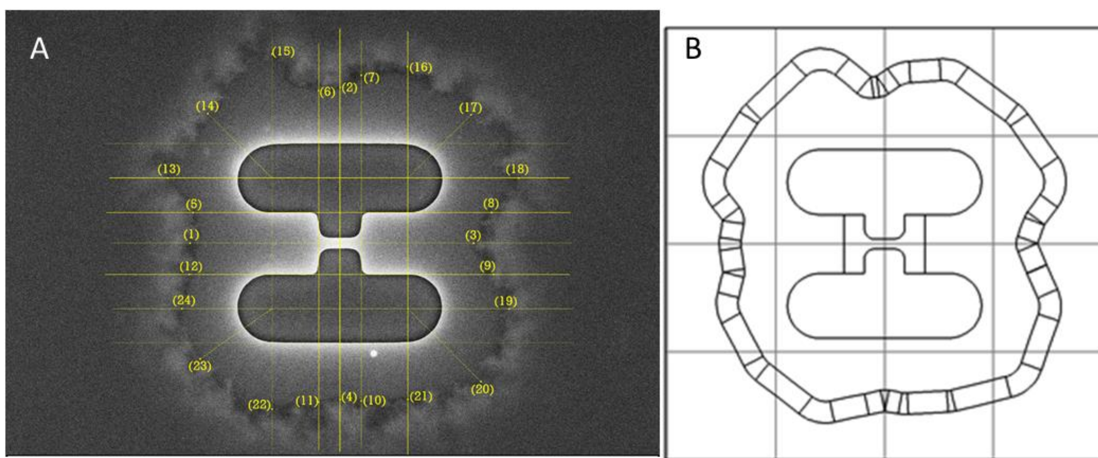


Figure 21: A) Nanobridge with irregular under etching. The guidelines are used to perform the measurements of the corrosion profile in the edges. B) Corresponding simulated Comsol geometry.

Another important feature of the fabricated structure is that it presents partial corrosion underneath the outer borders of the visible under etched profile. This partial corrosion was characterized by a SEM image from a nanobridge that was milled by a Nova NanoLab 200 focused ion beam (FIB) system, from CCSNano – UNICAMP. Firstly, the FIB system was employed to deposit an electron-beam-induced deposition of a platinum film on the bridge to prepare the sample for the milling process. Then, a gallium ion beam was employed to mill the region below the cut line demonstrated in Figure 22A. The next step was to incline the sample to get a lateral view of the sample, as demonstrated in Figure 22B. The region of interest was amplified and showed in Figure 22C. One can see the partial corrosion profile of the buried silicon dioxide (BOX) and the penetration of the deposited platinum into the etched area. This partial corrosion area is demonstrated in detail at Figure 22D, being the transient lighter color region which can be directly measured by the top-view

image. Also, Figure 22D demonstrates the simulated geometry and the lateral view of the simulated geometry representing the partial corrosion of Figure 22C.

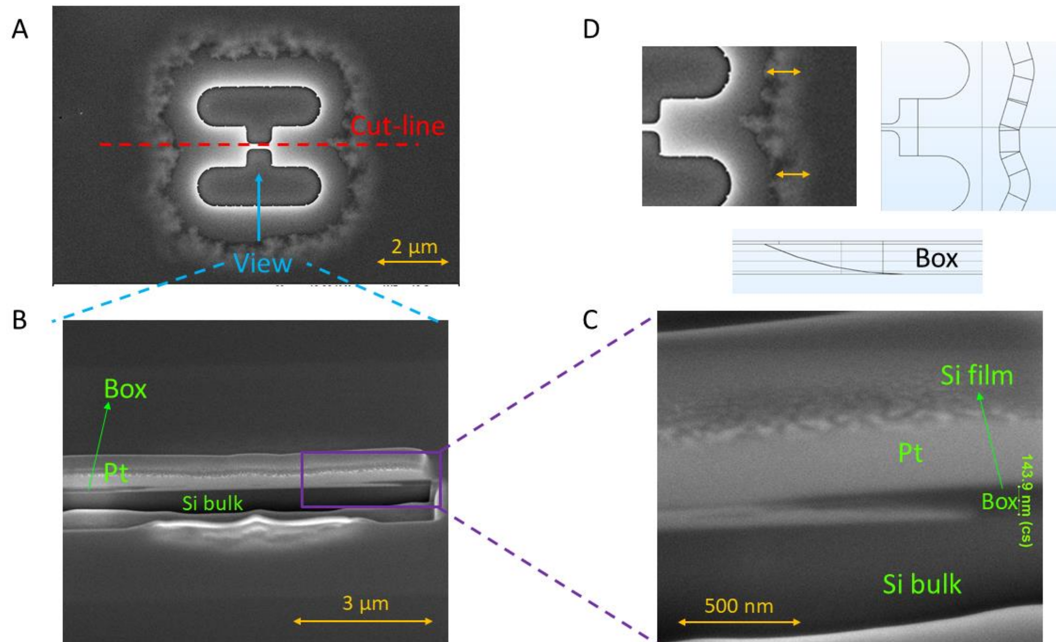


Figure 22: A) Top-view of a fabricated nanobridge with the cut-line indicated (before platinum deposition). The ion beam milled the region below the cut-line after platinum deposition. B) Lateral view (indicated in A) from the milled nanobridge. C) Lateral view from the region highlighted in B. It is possible to check the deposited platinum, the 145 nm-thick buried silicon dioxide (BOX), and the silicon bulk. The 15 nm-thick strained Si film was indicated in the figure but still not visible because of the equipment resolution limit (~10 nm). One can see the profile of the etched area by the penetration of platinum into the box etched area. D) Top-view image of the nanobridge with the outer border dimension (arrows) and the corresponding Comsol CAD simulation (top-view). One can also observe the simulated lateral profile of the region demonstrated in Figure 22C.

3.5. Raman Characterization Protocol

Raman measurements were carried out using a Renishaw spectrometer in backscattering configuration with a 514 nm wavelength excitation source. We have used a grating of 2400 lines/mm, which provides a spectral resolution of around 0.4 cm^{-1} and a 100 X objective lens with a numerical aperture NA = 0.9. The incident power at the sample was measured by a silicon photodiode (Thorlabs PM200/S120C). The laser spot size was around 1 µm. The calibration of the Raman equipment was performed using a silicon reference sample with the peak adjusted at 520.5 cm^{-1}.

The protocol was based on the following steps:

1) The spectrometer is turned on and stabilized for 1 hour to guarantee the laser stability.
2) The equipment calibration is performed into an unstrained silicon sample with the peak adjusted at 520.5 cm^{-1}.
3) The laser power is adjusted and measured by the power meter with the 100X objective lens plugged.
4) The laser beam is targeted at the nanowire, and the spectrum is acquired. The number of accumulations is adjusted in order to get a spectrum with high signal to noise ratio. This adjustment is maintained for all measurements.
5) At the end of the measurements, the laser power is measured again to check the stability of the laser. Also, a new spectrum from the reference silicon sample is measured to check the laser stability. The results were always the same from the calibrated values in steps 2 and 3, demonstrating excellent laser stability. This step is just a system check-up.
6) Return to step 3 to get new measurements in new laser power. The measurements were executed up to 5 different laser powers (4, 10, 23, 34 and 69 μW) to perform the thermal correction procedure that will be described in details at Section 4.1.B of this thesis.

Chapter IV – Results and Discussion

In the next chapter, the results of the FEM simulations and Raman characterization are demonstrated and discussed. Then, both characterizations are used to analyze the Raman stress behavior for low and high stresses.

4.1. Results and Discussion

4.1.A. FEM Simulation

Figure 23 shows the simulated stress components of the fabricated nanowire from Figure 19A. Figure 23A presents the color map from the stress along the X-direction (σ_{xx}). This stress is spatially uniform along the nanowire region with a gradual reduction along the transition zone between the nanowire and pads. From Figure 23B, one can observe the stress components from an imaginary line passing along the center of the pads and the nanowire. This figure shows that in the nanowire region, the stress is uniform and uniaxially stressed since the other components (σ_{yy} – [-110] ~ 0 GPa and σ_{zz} – [001] ~ 0 GPa) are negligible compared to the σ_{xx} = 2.74 GPa stress component. In the transition region, one can see the abrupt reduction of the σ_{xx} component to values smaller than 1 GPa, the σ_{yy} component presenting a value around 0.4 GPa and the σ_{zz} ~ 0 GPa. Figure 23C and Figure 23D show color maps of the σ_{yy} and σ_{zz} stress components, respectively. It was possible to reconfirm that these stress components are much smaller than the σ_{xx} component along the nanowire region, demonstrating the uniaxial behavior of the stress. Not shown here, the shear stress components are also negligible compared to the σ_{xx} stress component.

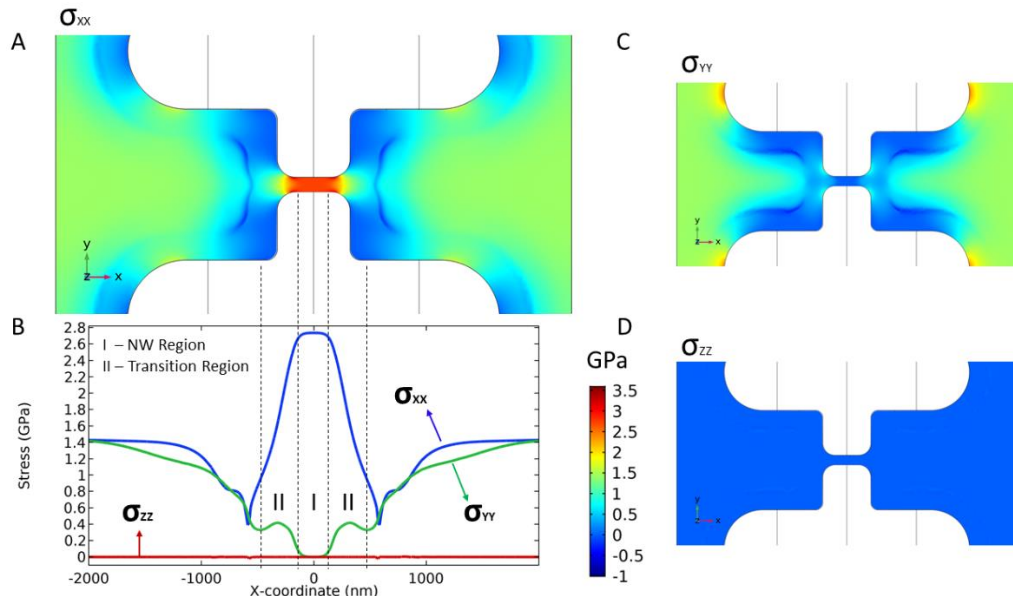


Figure 23: Stress components simulated by FEM of the suspended nanowire presented in Figure 19. A) Color map of the σ_{xx} stress component in the nanostructure, B) Cut-Line graph for the triaxial stress components in the structure along the center, and color map of the C) σ_{yy} and D) σ_{zz} stress components at the nanostructure.

Moreover, it is possible to check for the mechanism of stress redistribution after the suspension. The suspended region of the pads suffered a stress relaxation (reduction of σ_{xx} stress component) to values smaller than the initial 1.44 GPa, enabling the increase of the tensile stress at the nanowire region to 2.74 GPa. The region with oxide underneath the silicon thin film located far from the nanobridge holds its initial biaxial stress at around 1.44 GPa.

4.1.B. Raman Characterization

Figure 24A shows the Raman spectrum of the nanowire from Figure 19A. The spectrum has a high-intensity left-shifted peak in 515.1 cm^{-1} and a band located to the right. Such spectrum is expected as the nanowire region has its whole area with high uniform uniaxial stress (σ_{xx} = 2.74 GPa), as demonstrated in Figure 23. Therefore, the left-shifted peak corresponds to the signal of the strained nanowire region. The band located to the right originates from the transition region between the nanowire and the pads. It turns out that the laser spot diameter is around 1 µm, and the nanowire length around 700 nm, thus there is an overlap between the laser spot and the pads. From Figure 23, this transition zone has smaller stress components (σ_{xx} - abrupt reduction to values lower than 1 GPa, σ_{yy} ~ 0.4 GPa, and σ_{zz} ~ 0 GPa) than the central nanowire with a complex stress profile in the presence of stress gradients. Consequently, the expected Raman signal for this area represents several different peaks, forming a band located to the right of the nanowire peak (smaller stress values compared to the nanowire region). In addition, a Raman peak from the silicon substrate (520.5 cm^{-1}) is expected due to the high penetration of the 514 nm wavelength laser beam into the substrate. The detailed analysis of the spectra from the transition zone is complex and is out of the scope of this thesis. Thus, only the region regarded to the uniaxially stressed nanowire (sSNW peak) was considered for the SSC extraction. Figure 24B shows the evolution of the spectra from different nanowires subjected to different stress levels (2.3 GPa up to 6.3 GPa). All the spectra were measured at 23 µW. As expected, the nanowires subjected to higher stress present downwards shift of the sSNW peaks, ranging from 516.1 cm^{-1} for the 2.3 GPa nanowire to 505.8 cm^{-1} for the 6.3 GPa nanowire.

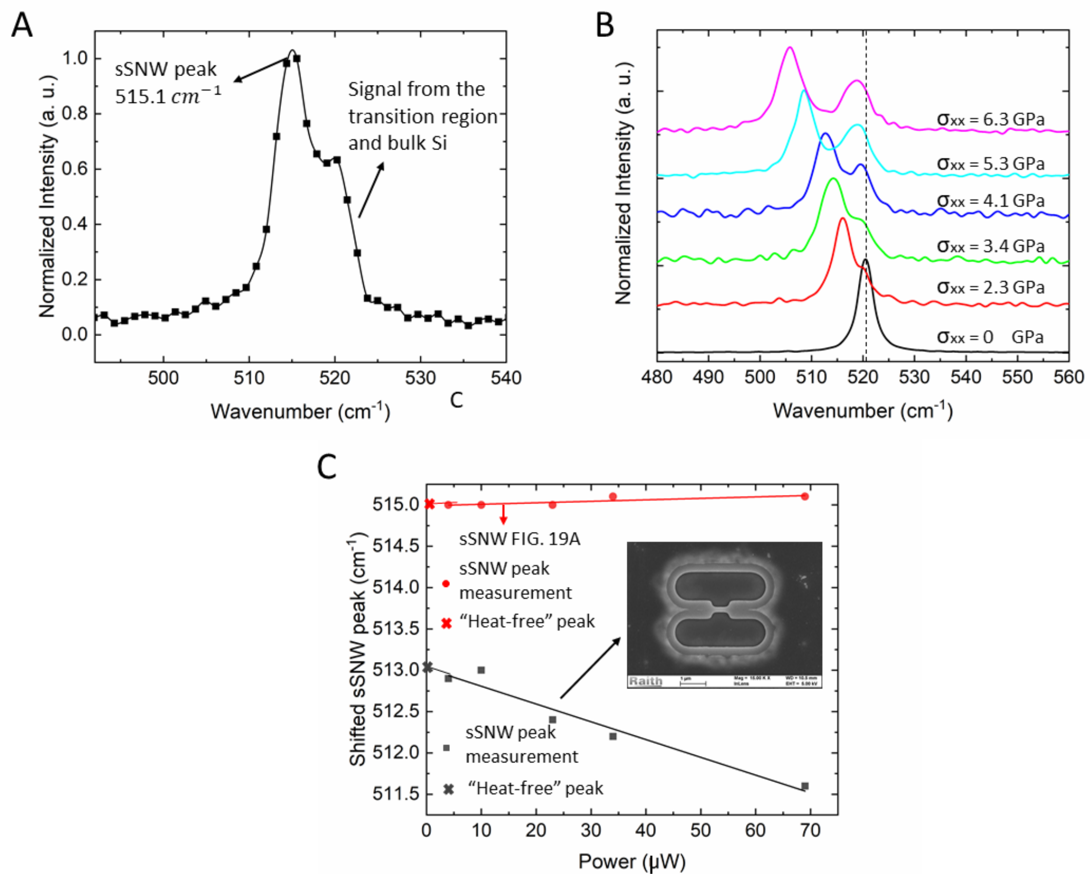


Figure 24: A) Raman spectrum from the strained nanowire of Figure 19 with an incident laser power of 34 µW, B) Raman spectra evolution from nanowires of different stress. The spectra were measured at 23 µW incident laser power from nanowires with 2.3 GPa up to 6.3 GPa, and C) thermal correction procedure from the nanowire of Figure 19 (red circles) measured in 5 distinct incident powers (4, 10, 23, 34 and 69 µW). The sSNW peaks are plotted with a linear fit. The intercept at zero laser power represents the "heat-free" shift. *Inset*: top-view SEM image of a stressed silicon nanowire and its thermal correction procedure (black squares).

Furthermore, the stress-induced peak extraction at each nanowire was achieved by the Raman shift measurement at different incident laser powers (4, 10, 23, 34 and 69 µW). It turns out that incorrect Raman shifts can be observed from the nanowire because of the high local temperatures achieved by the light impinging during the measurements [79]. Therefore, it was performed a thermal correction protocol using a linear extrapolation of the sSNWS peaks, characterized by different laser powers, to a virtual Raman shift at zero power (Figure 24C). Such process aims to extract the Raman peak free of thermal effects, only influenced by the stress [79]. The heat-free shifted peak is the correct value to obtain the

Raman shift ($\Delta\omega$). Figure 24C shows the thermal correction procedure for the nanowire from Figure 19 (red circles). This figure shows that this nanowire does not suffer from thermal effects, presenting the heat-free peak at 515 cm^{-1}, being independent of the laser power as demonstrated by the horizontal line fit. The inset shows the thermal correction procedure from a fully suspended nanowire (black squares). Because of the increased suspended area, the thermal effect has a greater influence (higher slope) due to the lower heating dissipation of the fully suspended nanowire. One can see the thermal effect by the difference between the heat-free peak from this nanowire, located at 513 cm^{-1}, and the Raman peak at 69 μW, located at 511.6 cm^{-1}.

4.1.C. Raman Shift – Stress Behavior

The Raman shift was measured as a function of the nanowire stress (σ_{xx}), as shown in Figure 25A. It was obtained by measuring 28 nanowires of different dimensions in order to extract 28 different stress values. Each nanowire was characterized by Raman spectroscopy with the thermal correction protocol, yielding to the correspondent heat-free Raman shift. In addition, FEM simulations were individually performed to calculate the stress of each nanowire. Here, the maximum stress achieved is around 4.5 GPa, as in Reference [53]. Figure 25A shows the expected theoretical linear behavior from Eq. 2 for this level of stress, being in agreement with Reference [53]. Then, it was measured the SSC from the angular coefficient of the linear fit, yielding a value of 1.9 ± 0.1, which is in good agreement with the literature [47], [48], [51] and very close to Reference [53]. The error is associated with the uncertainty in the slope determination. The error bars from the Raman shift is related to the equipment spectral resolution, and the error bars from the simulated stress were estimated according to the dimension measurements errors and its influence in the simulated stress.

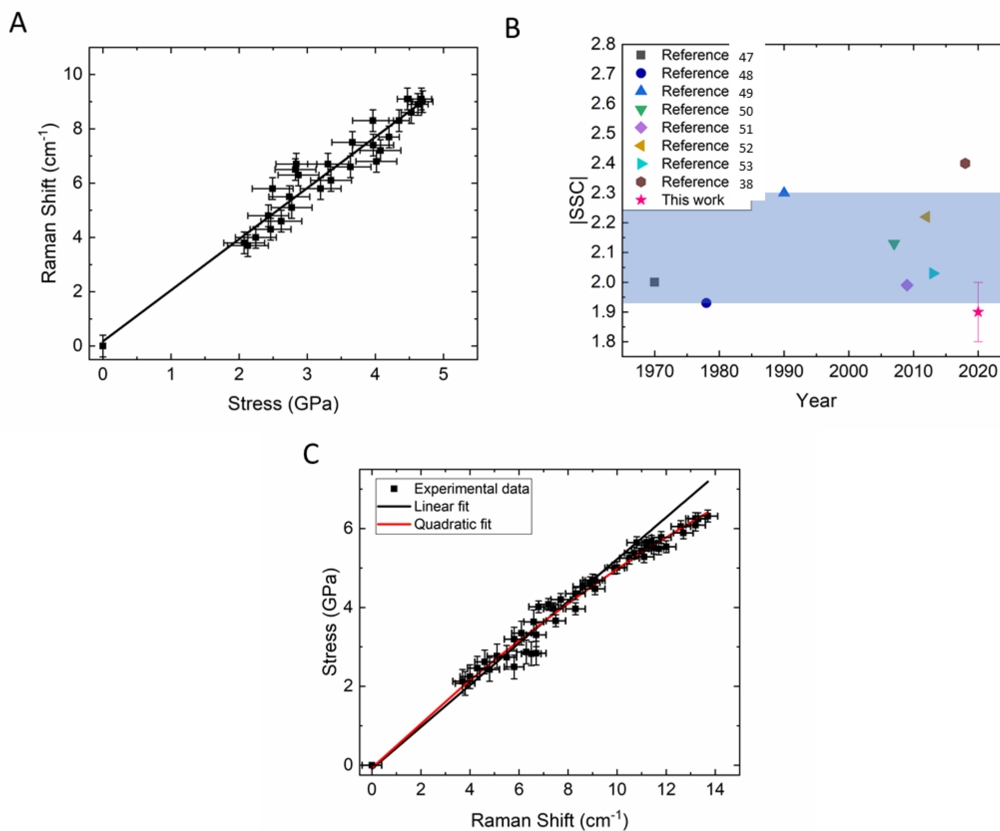


Figure 25: A) Experimental Raman shift as a function of the simulated stress for 28 different nanowires, B) comparison between the extracted SSC modulus from our work with the SSC values reported in the literature. The shaded area covers the previous works reported on bulk silicon or with bulk silicon parameters, and C) Stress as a function of the Raman shift from 49 different nanowires. Up to around 4.5 GPa, the linear model agrees with the quadratic model.

Figure 25B shows the comparison between the SSC from our work with the values so far reported in the literature (Table 1). One can observe a broad dispersion of the SSCs. The shaded area is regarded to the previous works performed on bulk silicon or considering bulk silicon mechanical parameters. The dispersion observed in Figure 25B may be explained by the fact that the phonon deformation potentials (PDPs) from the silicon surface are different from the PDPs inside the crystal because of surface stress relaxation, as previously reported by Anastassakis et al. (1990) [49]. In their work [49], higher PDPs values were reported using a laser frequency in the region of transparency, permitting the study of PDPs without surface effects. These PDP values were confirmed independently by Miyatake et al. (2011) [80] using two different methods: micro-indentation and ball-on-ring. On the other hand, our ultra-thin

15 nm thick suspended nanostructure has a larger surface area to volume ratio compared to previous works. This might explain the smaller SSC value compared to the work of Anastassakis et al. (1990) [49]. Further investigation is needed on the silicon PDPs [25], [81].

So far, the Raman works on stressed silicon have been modeled by the linear model, as shown in Eq. (2) and Figure 25A, with the SSCs in a range around 1.9×10^{-9} $cm^{-1}Pa^{-1}$ up to 2.4×10^{-9} $cm^{-1}Pa^{-1}$ (Table 1). Here, for the first time in literature, it was extended the stress range of silicon from 4.5 GPa [53] to 6.3 GPa. The results, shown in Figure 25C, present the stress as a function of the Raman shift. The axes inversion were performed to have a direct comparison with the work from Gassenq et al. (2016) [42]. The linear model is no longer valid for values higher than around 4.5 GPa. On the contrary, the data points nicely fit the quadratic fit, as shown in Eq. 13:

$$\sigma_{XX} = 0.59(\pm 0.05) \times \Delta\omega - 0.008(\pm 0.003) \times \Delta\omega^2;$$

(13)

For lower stress values (< 4.5GPa), the SSC extracted from the quadratic fit is in good agreement with the SSC employing the linear fit, as shown numerically by Eq. 14.

$$\sigma_{XX} = \frac{1}{SSC} \times \Delta\omega = 0.53(\pm 0.03) \times \Delta\omega;$$

(14)

However, for higher stresses (> 4.5GPa), there is a deviation from the linear model. One can notice that for nanowires with Raman shifts around 13 cm^{-1} the correspondent stress would be around 6.8 GPa using the linear model. This differs from 6.3 GPa by using the quadratic correction. This correction has not been predicted before in silicon for stress values up to 4.5 GPa, albeit has been already demonstrated in Germanium in the work of Gassenq et al. (2016) [42]. Germanium has a diamond-like crystallographic structure, similar to silicon, and presents the same proposed linear model from Eq. 2, with different phonon potentials and mechanical constants. However, this unexpected behaviour, firstly demonstrated in 2016 and reconfirmed by Gassenq et al. (2017) [82], is now being empirically demonstrated for silicon. Further works should better investigate this anomalous behavior for silicon.

Chapter V – Conclusion and Perspectives

This work presented the stress characterization of ultra-thin 15 nm-thick silicon nanowires submitted to ultra-high levels of stress (up to 6.3 GPa) by Raman spectroscopy. Distinct stress values were obtained by the nanofabrication of strained suspended nanobridges of different dimensions without the need of external actuators. To accurately characterize the stress, it was used the finite elements method (FEM) simulations using COMSOL simulation tool. Therefore, all the geometrical and physical characteristics of the silicon nanobridges after lithographic/etching processes were taken into account. The Raman shifts of the strained silicon were determined by a Raman spectrometer with a 514 nm excitation laser source. In addition, a thermal correction procedure was conducted to extract the Raman shift free of thermal effects. The results demonstrate that the theoretical linear Raman-stress behavior still holds for stresses in the range of 0 - 4.5 GPa and the extracted SSC is in good agreement with the lowest SSCs values reported in the literature (Table 2). The results may have been affected by the influence of surface effects in the PDPs due to stress relaxation at the surface since our structure is a suspended ultra-thin nanostructure that has a high surface area to volume ratio. On the other hand, for higher stresses (> 4.5 GPa), it was proposed for the first time in silicon an empirical correction from the linear model similar to the correction proposed for germanium. The results from this thesis have demonstrated the feasibility of the Raman technique for the stress characterization of ultra-thin silicon nanowires, which should be useful to characterize strained silicon nanodevices for technological nodes below 100 nm under a wide range of stresses and without the need of complex sample preparation or to be invasive to the analyzed sample.

Table 2: Reported silicon phonon deformation potentials (PDPs) in literature and the stress-shift coefficient (SSC) for uniaxially stressed silicon at the [110] crystallographic direction on a (001) surface. The thickness of the characterized structure (also the smaller dimension) and the stress type with its range are shown as well. The results from this thesis are demonstrated in the last row.

Reference	**PDPs**	**Thickness & Structure**	**Stress (GPa)**	**SSC[a]**
Reference [47] (1970)[b]	$p/\omega_0^2 = -1.25$ $q/\omega_0^2 = -1.87$	1 mm - Wafer	Compr. ~ 0 – 1.15	-2
Reference [48] (1978)[b]	$p/\omega_0^2 = -1.43$ $q/\omega_0^2 = -1.89$	1.3 mm - Wafer	Compr. ~ 0 – 1.8	-1.93
Reference [49] (1990)[b]	$p/\omega_0^2 = -1.85$ $q/\omega_0^2 = -2.31$	~1 mm - Wafer	Tensile ~ 0 – 1.2	-2.3
Reference [50] (2007)[b]	-	- - Film	Biaxial	-2.13
Reference [51] (2009)	$p/\omega_0^2 = -1.56$ $q/\omega_0^2 = -1.98$	- - Wafer	Tensile ~ 0 – 0.2	-1.99
Reference [52] (2012)[b]	$p/\omega_0^2 = -1.85$ $q/\omega_0^2 = -2.25$	70 nm - Film	Tensile Biaxial ~ 1.3	-2.22
Reference [53] (2013)[c]	-	200 nm - Nanostructure	Tensile ~ 0 – 4.5	-2.03
Reference [38] (2018)[d]	-	100 nm - Nanostructure	Tensile ~ 0 – 2.5	-2.4
This work (2020)	-	15 nm - Nanostructure	Tensile ~ 0 – 6.3	-1.9 ± 0.1

It is worth mentioning that the methodology employed in this work to investigate the Raman – stress behavior for silicon nanostructures had the use of a platform that reproducibly strained the silicon nanowire in a vast range, achieving ultra-high stresses, without the use of external actuators, and requiring just the use of CMOS compatible nanofabrication techniques. This fact is interesting because of the proximity of this study platform to the top-down structures and techniques employed by the microelectronics industry.

As future works, it is proposed the investigation of the quadratic behavior by using the micro-XRD technique as a confirmation of this work with a different experimental technique. In addition, the use of this strained platform to perform transport measurements in order to characterize the carriers' electrical mobility and the piezoresistance from these strained nanowires is a promising challenge. The extraction of the carriers' electrical mobility

can be achieved by the adaptation of this strained platform to a transistor architecture. The piezoresistance can be characterized by 2 point probe measurements thorough the addition of two electrical contacts. Besides, this platform can be adapted to fabricate gate-all-around (GAA) transistors with ultra-strained channels for further enhancement of electrical mobility.

S A O P A U L O / S P • B R A Z I L

P H O N E : + 5 5 1 1 9 9 7 9 2 4 3 6 9 • L U C A S . S P E J O @ G M A I L . C O M

L U C A S B . S P E J O

1. PERSONAL DATA

•Name: Lucas Barroso Spejo

•Nationality: Brazilian

•Date of Birth: July 29, 1994

2. EDUCATION

Mar 2018 - onwards	**State University of Campinas (Score: 4.0/4.0)**
	Brazil
	Master Degree in Electrical Engineering (Microelectronics)
Dec 2017	**University of Campinas (Position: 6th of 81 students)**
	Brazil
	Bachelors in Electrical Engineering
Dec 2012	**Federal Institute of São Paulo**
	Brazil
	Technical Degree Course in Electronics

3. FUNDED RESEARCH PROJECTS

• Graduate Project: Giant Piezoresistance and Electrical Carriers Mobility of Ultra-Strained Silicon Nanowires – Fapesp/Brazil (~12.6k USD) – Master of Science scholarship

• Undergraduate Project: Characterization of Strained Semiconductors Structures by Raman Spectroscopy – Fapesp/Brazil (~3.8k USD) – Scientific initiation scholarship

4. EXTRA ACTIVITIES

Aug. 19	Invited Lecturer
	Presentation Title: “Stress Characterization in Nanostructures using Raman Spectroscopy”
	Event: Workshop on Raman Spectroscopy: Concepts and Applications
	Organized by Renishaw

Apr. 18 – onwards — IEEE Electron Device Society (EDS) - Unicamp Student Branch Chapter. Position: President.

Aug. 18 – Dec. 18 — Teaching Assistant
Course: EE301 Physical Foundations Laboratory for Electrical Engineers

5. PRIZES, AWARDS

• 2019 – IEEE EDS Chapter of the Year Award (R9 – Latin America)

6. PUBLICATIONS (RELATED TO THIS THESIS)

• **L.Spejo** et al., "Stress Characterization of Highly Strained Ultra-Thin Silicon Nanowires by Raman Spectroscopy", FORTHCOMING.

• **L. Spejo** et al., "Triaxial Strain Analysis of Strained Silicon Nanowires by Raman Spectroscopy and Finite Element Method Simulation", The 6th Nano Today Conference, 2019.

• **L.Spejo** et al., "Strained Silicon Nanowire without External Mechanical Actuators", Proceedings of the Seminatec 2018, ISBN:978-85-98123-12-7

• **L. Spejo** et al., "Structural Breakdown of Suspended Strained Silicon NanoWires by Exposure during Scanning Electron Microscopy Analysis.", The 61nd International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication, 2017.

7. BOOK EDITOR

• J. Swart, J. Diniz, **L. Spejo**, P. Petrini, L. Zucchi, L. Costa, and A. Silva "Workshop Proceedings of the XIV Workshop on Semiconductors and Micro & Nano Technology", 2019, ISBN: 978-65-5093-000-4

8. MAGAZINE PUBLICATION

• **L. Spejo** et al., "ED UNICAMP Student Chapter Organizes SEMINATEC 2019", IEEE EDS Newsletter VOL. 26, NO. 3, pp. 23-24, ISSN: 1074 1879

9. EVENT ORGANIZATION

• J. Swart, J. Diniz, **L. Spejo**, P. Petrini, L. Zucchi, L. Costa, and A. Silva "XIV Workshop on Semiconductors and Micro & Nano Technology – Seminatec 2019" held in Campinas, SP, Brazil

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