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LUCAS STUCCHI-ZUCCHI

SILICON WET ETCHING IN NH_4OH SOLUTION AS CHANNEL THINNING MECHANISM FOR JUNCTIONLESS-FET DEVICES

CORROSÃO DE SILÍCIO EM SOLUÇÃO DE NH_4OH COMO FORMA DE AFINAMENTO DO CANAL PARA DISPOSITIVOS JUNCTIONLESS-FET

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Silicon wet etching in NH_4OH solution as channel thinning mechanism for Junctionless-FET devices

Corrosão de silício em solução de NH_4OH como forma de afinamento do canal para dispositivos Junctionless-FET

Dissertation presented to the Graduate Program in Electrical Engineering of the School of Electrical and Computer Engineering of the State University of Campinas as a requirement for the title of Master of Science in the area of Electronics, Microelectronics and Optoelectronics

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Abstract

The industry of nanoeletronics is a symbol of technological innovations and one of the cores of modern-day information systems. After decades of innovations in miniaturizing and improving the traditional inversion-type MOSFET device, its once thought to be unbound potential seems to be arriving at its limits. Among the new devices proposed to sustain the historical increase in computing power and efficiency, the Junctionless-Field-Effect-Transistor (JL-FET) stands out as an alternative that can lower the cost and complexity of fabrication, while at the same time improving key figures such as on and off current, switching delay and subthreshold slope. To achieve JL-FET devices that are compatible with state of the art switching applications, the device channel must be thin enough to enable full charge carrier depletion for null gate voltage, usually a few dozen nanometers.

In this work, the silicon anisotropic etching in NH_4OH solution was developed as means to thin structures to the required thicknesses for JL-FET fabrication. Initially, the devices were simulated numerically on SILVACO Atlas and Athena environments, so as to generate a numerical model that could help on planning and implementing the proposed processes. Every test was carried out in 340 nm silicon (100) over 400 nm Silicon Dioxide Silicon-On-Insulator (SOI) wafers. Building on previous works that measured minimum etch rate at 2.5 nm/s for the specific structures, JL-FET devices were fabricated by two distinct processes. In the original process the silicon etching in NH_4OH solution took place after the active region is already defined and etched and after ion implantation ($^{31}P^{+}$ ion, dose of 6.10^{15} atoms.cm^{-2} , and energy of 50 keV) was carried out to achieve the channel doping. An updated process was proposes, in which the NH_4OH solution silicon etching takes place before any other process, among the advantages of this process flow, the structures can be characterized optically midway through the fabrication and the etching rate becomes even for both pMOS and nMOS devices.

Devices with channel thickness of 63 nm were fabricated using the original process, thinned from 165-nm-thick SOI layers. The dopant concentration on the channel region was estimated at approximately 10^{17} atoms/cm^{3}, obtained by the Pseudo-MOS characterization technique. The device presented Schottky electrical contacts with potential barriers of approximately 1 V and also presented a negative threshold voltage, due to the dopant concentration and thickness of the channel. These results were confirmed by feeding the obtained data back in the numeric simulation models.

Samples with etching times between 50 s to 80 s were fabricated using the updated process, alongside unetched samples. Without the doping effect, this process presents an improved control over the etching rates, enables the fabrication of pMOS devices and an overall larger dopant concentration on the devices. The voltage necessary to deplete every charge carrier in the channel, V_0, were estimated (between -27 V and -10 V) using the Pseudo-MOS measurements for all the samples fabricated using the updated process. Using this data, a fitting was performed to obtain a V_0 versus etching time plot. As V_0 is closely related to the ability of the transistor to achieve cut-off, this figure will be used to guide future fabrication efforts. I_D x V_{GS} measurements also showed increased I_{on}/I_{off} ratios as the etching time increases, from 1 in the unetched sample, to approximately 1.13 in the sample etched for 80 seconds. The transconductance also presented similar evolution, ranging from virtually null on the unetched samples, to approximately 3.5 µS on the sample etched for 80 seconds.

In conclusion, we developed the anisotropic etching of silicon in an ammonium hydroxide (NH_4OH) solution as a way to allow the fabrication of JL-FET devices, with channel thickness up to 63 nm, because these devices require dimensions thinner than 100 nm. This kind of etching is accessible and cheap, presents almost negligible etching rate to the oxide hardmask used to define the etched regions and does not cause the introduction of contaminating ions and materials on silicon substrate.

Resumo

A indústria da nanoeletrônica é símbolo da inovação tecnológica e está no cerne dos sistemas de informações modernos. Após décadas de inovações em miniaturização e melhoramentos na configuração tradicional dos dispositivos MOSFET (*Metal-Oxide-Semiconductor Field-Effect-Transistor*), novos dispositivos precisam ser estudados. Em meio a esses novos dispositivos, o Transistor de Efeito de Campo Sem Junções (*Junctionless-Field-Effect-Transistors*, ou JL-FET) se destaca devido ao seu menor custo e complexidade de fabricação, ao mesmo tempo que apresenta melhorias em características centrais ao funcionamento do dispositivo, como a corrente quando ligado e quando desligado, menor atraso de chaveamento e menor *subthreshold slope*. Para obter dispositivos JL-FET compatíveis com aplicações digitais, o canal do dispositivo deve ser fino o suficiente para que todos os portadores de carga estejam depletados para uma tensão de porta nula, isto ocorre quando a espessura é menor do que 100 nm.

Neste trabalho, foi estudada a corrosão anisotrópica de silício em solução de NH_4OH como forma de afinar estruturas a níveis nanométricos, com foco na fabricação de JL-FETs. Inicialmente, os dispositivos fabricados com o processo foram simulados numericamente nos ambientes SILVACO Athena e Atlas, para gerar um modelo que auxiliasse no planejamento dos processos propostos. Todos os testes foram feitos em lâminas de silício-sobre-isolante (*silicon-on-insulator*, ou SOI), inicialmente com 340 nm de silício monocristalino (100) sobre 400 nm de óxido de silício. Primeiro, a corrosão foi caracterizada através de testes já com os padrões necessários para a fabricação dos dispositivos, visto que a taxa de corrosão da solução de NH_4OH varia conforme as estruturas expostas. Dispositivos JL-FET foram fabricados utilizando duas maneiras distintas: em uma delas a corrosão de silício em solução de NH_4OH ocorre após a definição da região ativa e implantação de dopantes ($^{31}P^{+}$ ion, dose de 6.10^{15} atoms.cm^{-2}, e energia de 50 keV), na outra a corrosão de silício em solução de NH_4OH ocorre antes de todos os outros processos.

Foram obtidos dispositivos com canais com espessuras de 63 nm para o primeiro processo, afinados a partir de estruturas que inicialmente apresentavam 165 nm de espessura. A dopagem do canal nesses dispositivos foi estimada na ordem de 10^{17}atomos/cm^{3}, determinada a partir do método de caracterização Pseudo-MOS, O comportamento observado foi adequado às características medidas: o dispositivo apresentou contatos Schottky com barreiras de potencial da ordem de 1 V, condizente com a dopagem obtida, e uma tensão de limiar

negativa, que também condiz com a dopagem e espessura medidas. Esses resultados foram confirmados pela realimentação dos dados obtidos nos modelos de simulação numérica.

Foram fabricadas amostras com tempos de corrosão variando entre 50 s e 80 s, utilizando a nova sequência de processos. Sem o efeito da dopagem, este processo apresenta um maior controle sobre as taxas de corrosão, permite que sejam fabricados dispositivos pMOS e de maneira geral aumenta a máxima dopagem possível nos dispositivos. Os valores de tensão de corpo que seriam necessários para depletar todos os portadores de carga do canal, V_0, foram estimados (entre -27 V e -10 V) a partir das medições Pseudo-MOS para todas as amostras fabricadas com o novo processo. Usando estes dados, um fitting foi obtido que representa V_0 e sua variação com o tempo de corrosão. Como o V_0 indica o quão próximo um dispositivo está de atingir a região de corte, esta curva será usada para guiar os próximos processos de fabricação. Medições I_D x V_{GS} mostraram uma melhoria na razão I_{on}/I_{off} conforme o tempo de corrosão aumenta, de 1 nas amostras sem corrosão até aproximadamente 1.13 na amostra corroída por 80 segundos. A transcondutância também apresentou evolução similar, de valores nulos nas amostras sem corrosão a 3.5 µS na amostra corroída por 80 segundos.

Concluindo, a corrosão anisotrópica de silicio em solução de hidróxido de amônio (NH_4OH) foi desenvolvida para a fabricação de dispositivos JL-FET com espessura de 63 nm na região de canal, esse processo é necessário pois os dispositivos necessitam dimensões menores do que 100 nm. Este tipo de corrosão é acessível e barato, apresenta uma taxa de corrosão desprezível para o óxido de mascaramento e não causa contaminação com íons ou outros materiais no substrato de silício.

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CHAPTER 1

INTRODUCTION

1.1 HISTORY OF MICRO AND NANOELECTRONICS

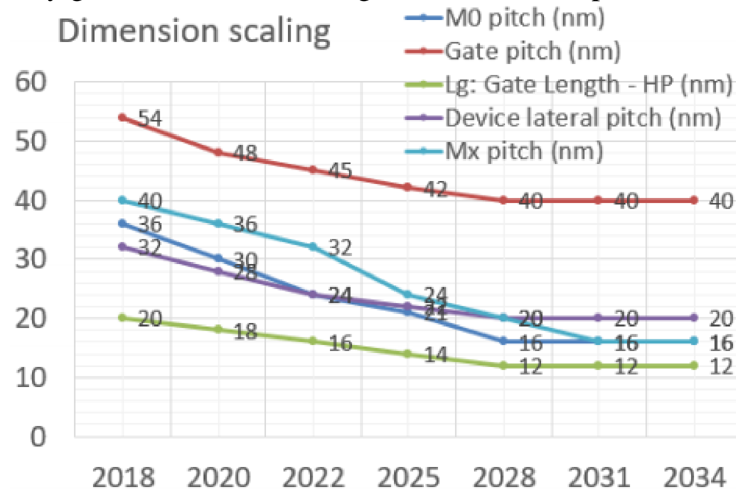
To estabilish the novelty of a Junctionless-Field-Effect-Transistor (JL-FET) device, we must first understand how the inversion-type transistor became the forefront of the nano-eletronics industry. The first ever transistor patent, filed by Lilienfeld, described a depletion-type field-effect-transistor, where a thin layer of semiconductor was stacked on top of an insulator and a metal to modulate the current flow (LILIENFELD, 1930). A functional device was never showed by Lilienfeld, but soon John Bardeen and Walter Brattain obtained the first-ever functional transistor in 1947, which was called the Point-Contact Transistor (BARDEEN, 1956). The Bipolar Junction Transistor (BJT) was demonstrated by the same research group an year later (SHOCKLEY, 1984). It was only by the 1950s that the first Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) devices were achieved (PUERS et al., 2017), and these devices would soon take over the industry. The enhancement-type MOSFET had a lower Ioff that was perfect for digital applications, as when the Gate Voltage (VG) is lower than the Threshold Voltage (VTH), the device behaves as two opposing p-n diodes, blocking the current flow (SEDRA; SMITH, 2015). Also, the enhancement-type transistor was producible in a fast, cheap and reliable manner using the planar process. There is yet another configuration of MOSFETs, the depletion-type transistor. Its main issue arises when fabricated with a planar process in a bulk wafer, this results in a device with a very negative VTH, which makes it unsuitable to digital technologies (SEDRA; SMITH, 2015).

With all these characteristics, and allied to the flexibility of silicon-based materials, the planar process of enhancement-type MOSFETs drove the industry for decades. The scaling of the planar MOSFETs and evolution in processing techniques and materials culminated in an Information Technology Revolution. The speed with which the technology evolved

was put into words by Gordon Moore, at the time the director of R&D in Fairchild Semiconductors and that would later become co-founder of Intel. Moore stated, in an iconic piece in 1965, that the area density of microfabricated devices would roughly double every 18 months, without any increase in production costs (MOORE, 2006). The time frame was then updated to doubling every two years in the following decades, and similar trends can still be observed today. Amidst such prolific era of technological advancements in the MOSFET devices, little to no drive to develop new devices was present.

This era of rapidly advancing technology is coming to a steeping halt. As devices were scaled for decades, their dimensions are now so small that a few dozens of doping atoms are responsible for the dopant concentration in the entire device. This makes even small random dopant fluctuations (RDF) a big concern (SUZUKI et al., 2014) and faster and faster annealing techniques are needed so that de dopant diffusion during annealing steps will not compromise the steep gradient of dopant concentration required in state-of-the-art transistors. Short Channel Effects such as Drain Induced Barrier Lowering (DIBL) and Hot-Carriers injection, and Quantum Effects such as tunneling and confinement are also responsible for degradation on smaller transistors characteristics as the devices draw dangerously close to the tunneling distance (IWAI, 2016). This tendency is notable in 0, where some key ground rules of device scaling are plotted for the predicted values in the near future. M0 symbolizes the distance between two interconnectors on the first metal level, the gate pitch is the distance between the channels of two devices, Lg is the effective gate length, the lateral pitch is the distance between two devices, and Mx pitch is the distance between two interconnectors of the topmost metal level. Taking the gate pitch as an example, which is a ground rule that if historically one of the main goals of scaling, it faced a steep decline in scaling speed in recent years, and is projected to stop scaling altogether as soon as 2028.

Figure 1 Scaling of key ground rules, according to IRDS 2018 report.



This sets the stage for the research and development of novel devices and structures that are capable of mitigating such effects, and continue driving the technological advancements in micro and nanofabrication. So far, the industry has been exploring new device geometries and dispositions that can increase the area density or current of each device. For instance, the finFET device is a multi-gate device that can increase the current of the device by using the sidewalls as current paths (FERAIN; COLINGE; COLINGE, 2011). Newer technologies such as the lateral Gate-All-Around (LGAA) and vertical Gate-All-Around (VGAA) are also in implementation for future technological nodes. This trend is seen in Figure 2.

Figure 2 Transistor roadmap from IRDS 2018 report.[1]

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D

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[1] Note from the source: "*GxxMxxTx notation refers to Gxx: gate pitch, Mxx: tightest metal pitch in nm, Tx: number of tiers. This notation illustrates the technology capability. On top of pitch scaling there are other elements such as cell height, fin depopulation, DTCO constructs, 3D integration, etc. that define the target area scaling (gates/mm2).*" (IRDS report, 2018)

This context made the need for newer devices and materials reemerge. Devices with higher current drives or with steeper subthreshold swings are steadily becoming more ubiquitous (CRISTOLOVEANU; WAN; ZASLAVSKY, 2016). The interest in different switching mechanisms as in tunnel-FETs were reignited (QUINN; KAWAMOTO; MCCOMBE, 1978; IONESCU; RIEL, 2011; NARIMANI et al., 2017), and research in materials became a promising topic for future technological nodes, especially in graphene-based devices and III-V materials such as GaAs.

Jean-Pierre Colinge first proposed the Junctionless-FET device (COLINGE et al., 2010) as a possible device in the next technological nodes, as impurities diffusion, surface scattering of the charge carriers and short-channel effects become increasingly hard to manage (COLINGE et al., 2010). When compared to the traditional enhancement-mode field-effect transistors, the JL-FET devices present clear advantages, such as not requiring expensive junction engineering techniques, as costly Ultra Rapid Thermal Annealing, now required to maintain the sharp dopant concentration gradients needed in inversion-mode transistors and an important focus in scaling research (KIKUCHI et al., 2019; WANG et al., 2016). It also presents a higher current, due to the higher charge carrier mobility when operating in flat-band conditions and by distributing the current through the entire channel, as opposed to only superficial conduction in the inversion-type FETs (COLINGE et al., 2010). One of the advantages of the JL-FET device is full compatibility with current and planned cMOS technologies, as these devices can be implemented with the same materials and structures in every quasi-planar or 3D SOI configurations used in state-of-the-art cMOS applications (COLINGE et al., 2010).

1.2 MOTIVATION: JL-FET FABRICATION CHALLENGES

Despite all the advantages, the JL-FET device also brings a big technological challenge, as these are inherently nanometer-scaled devices that require state-of-the-art patterning processes. This is because the phenomena responsible for modulating the current that flows through the device is the depletion region induced and controlled by the Metal-Oxide-Semiconductor contact of the gate stack and the biasing voltage applied to it. This depletion region width is in the order of a few nanometers for highly doped silicon, which imposes a critical dimension of the same magnitude.

JL-FETs were fabricated using electron-beam lithography patterning (CHUNG et al., 2018; COLINGE et al., 2010; DORIA et al., 2011; MILLAR et al., 2018; THIRUNAVUKKARASU et al., 2017) and focused ion beam milling (LIMA et al., 2012; PUYDINGER DOS SANTOS et al., 2013); as well as being studied by simulation (GUPTA; KRANTI, 2017; RIOS et al., 2011; SAHAY; KUMAR, 2017). Besides silicon-based devices, high mobility materials such as germanium (GUPTA; KRANTI, 2017) and III-V materials (MILLAR et al., 2018) were also reported on the literature.

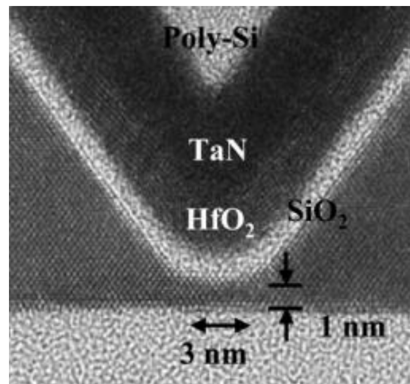
High precision processes such as electron-beal lithography and focused ion beam milling are ideal for prototyping and conceptual demonstrations, but are lacking on productivity and present high costs. This work proposes an accessible way to fabricate these structures with industrial throughputs, improving the competitivity of the JL-FET and other nanometer-scaled devices, and opening up the research possibilities to fabrication facilities that do not have access to advanced junction and patterning processes.

Replacing the traditional inversion-type MOSFET is argued to be the next step on nanoelectronics, since most scaling strategies are now encountering critical challenges that could impair further miniaturization on the coming years (IRDS 2018 UPDATE, 2018a). Multiple new devices have been proposed, and continue to be tested and studied all across the world, and once such device is the Junctionless-FET. In his report on the intricacies of nanowire transistors without junctions (COLINGE et al., 2010) proposes that the JL-FET might be the new flagship device for the next technological nodes. Before this switch can happen, new techniques to fabricate these devices in a reliable and economically viable way must be researched, as must be the intricate effects of devices with small dimensions on the functioning and stability of single and integrated systems. Therefore, the ability to fabricate nanometer-scale structures is paramount not only in achieving functional JL-FET devices, but also for a number of other devices, such as finFETs, monolithic GAA devices and tunnelFETs. The ability to evaluate the wafer-wide behavior of integrated logic devices is one of the main challenges to reduce fabrication and implementation costs of new technologies and devices (IRDS 2018 UPDATE, 2018b).

The ability to fabricate short and thin structures using the anisotropic etching of silicon was shown by laterally etching structures in the <100> direction using an Ion-Bombardment-Retarded-Etching (IBRE) process (MASAHARA et al., 2004), and by vertically etching silicon to the meeting point of the (111) planes (MIGITA et al., 2014). Structures as short

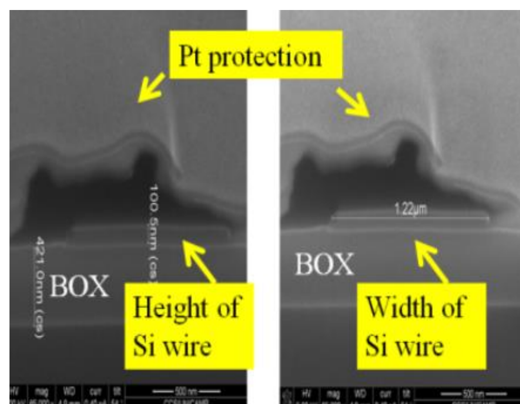
as 3-nm can be seen in Figure 3, with the possibility to fabricate atomically sharp structures. The etching reagent used was Tetramethylammonium Hydroxide (TMAH). (BAN et al., 2015) also showed how the intrinsic characteristics of the anisotropic silicon etching can be used in novel and interesting ways, such as capturing nanostructured particles that can alter the device functioning.

Figure 3 Cross-Section SEM images of the 3-nm-long transistor using TMAH etching fabricated by (MIGITA et al., 2014, adapted).



SOARES et al. (2018) also showed that the anisotropic etching can be used as a lateral thinning technique in the <111> direction. When used to thin the wire laterally, the silicon anisotropic etching generates trapezoid-shaped channels with the (111) crystallographic planes exposed, as seen in Figure 4. The etching reagent used was NH_4OH.

Figure 4 Cross-Section SEM images of the devices thinned laterally with trapezoid-shaped channels fabricated by (SOARES et al., 2018)



These research projects indicate that a vertical thinning of the silicon layer could be a viable alternative to fabricate devices with gates thin enough to achieve JL-FET functioning, with gates long enough to minimize short channel effects by stopping the etching process before the sharp v-groove profile can form.

1.3 OBJECTIVES

As a way to allow the fabrication of JL-FET devices, and therefore of other devices which require dimensions thinner than 100 nm, we propose the usage of the anisotropic etching of silicon in an ammonium hydroxide (NH_4OH) solution. This kind of etching is accessible and cheap, presents almost negligible etching rate to the oxide hardmask used to define the etched regions and does not cause the introduction of contaminating ions and materials on silicon substrate.

This project intends on develop and demonstrate the fabrication of structures thinned using silicon etching in NH_4OH solution. A comprehensive study of the process will be described, with numerical models in SILVACO Athenas and Atlas, evaluation of the device parameters according to etching time and processing techniques.

Another set of novelties established by this project is the fabrication of sub-100-nm devices using dopant diffusion. Dopant diffusion sees little use in semiconductor fabrication due to poor controllability of dopant concentration and junction depth, which is incompatible with the shallow junction and steep dopant concentration gradients needed for traditional enhancement-type MOSFET. When fabricating JL-FETs, on the other hand, these characteristics are not as problematic, and diffusion becomes a powerful technique as it does not introduce as many defects in the silicon crystal as the high-energy ions introduced by ion implantation.

The JL-FET device fabrication and characterization was chosen as an evaluating technique for the proposed process. Chapter two starts by presenting the charge distribution in MOS structures as basis to analyze the intricacies and particularities of JL-FET device functioning when compared to the traditional devices.

1.4 DISSERTATION OUTLINE

In chapter one, the history of the nano and micro electronics industry was layed out to better contextualize the junctionless-FET device and its place in technological innovation. The challenges for the fabrication of these devices and some the techniques that other research works used to achieve working devices were also presented. In the end, the main

objective was presented, to achieve a competitive new process for the fabrication of nanometer-scaled JL-FET devices.

In chapter two, the general field-effect-transistor theory and fabrication techniques are presented.

The MOSFET usage in circuit design and its representations show how these devices work as a component. The MOS capacitor theory is then presented to elaborate on how these devices work physically, enabling further distinction between the two categories of devices presented: the enhancement-type MOSFET device, that dominates the landscape of state-of-the-art nanoelectronics, and the JL-FET, which is the device proposed to take on the next technological nodes.

The techniques used in MOSFET fabrication are described in a broader sense, with patterning techniques, physical and chemical processes and procedures for contaminants control.

The techniques used for traditional fabrication of JL-devices are also presented, as are alternative techniques that were established to achieve functioning devices and techniques previously used by the nanoelectronics group at CCS/UNICAMP. At the end of chapter two, the processes investigated in this work are presented in their context.

In chapter three, the process flow is outlined step-by-step. The necessary cleaning and patterning are listed, as described in chapter two. The numerical simulation and etching rate studies are described, as the results were used in planning the methods. The first process is explained in detail, while the second process is defined by its differences and improvements upon the first.

In chapter four, the results from both of the fabrications are presented. The devices were characterized both structurally, using Scanning Electron Microscopy (SEM) imaging and optical microscopy, and electrically, using Pseudo-MOS and Junctionless biasing techniques.

In chapter five, the conclusions are presented, along the publications and accolades received during this research work.

In the appendices, succinct explanations of the processes and equipments utilized are presented.

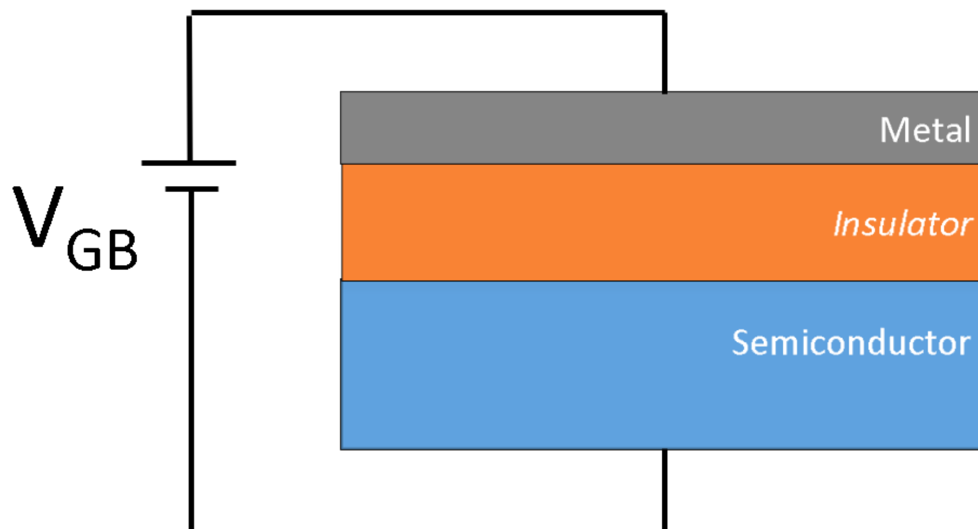
CHAPTER 2

FET THEORY AND PROCESSING TECHNIQUES OF JUNCTIONLESS-FET

2.1 MOSFET FUNCTIONING PRINCIPLE: THE MOS CAPACITOR

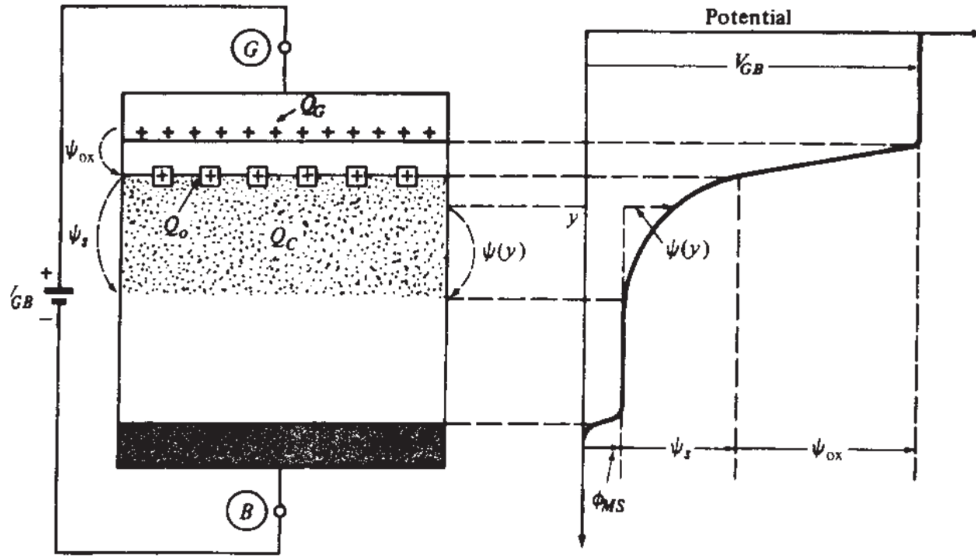
The main structure responsible for the current control in the traditional MOSFETs fabricated with the planar process to 3D MOSFETs and in JL-FET devices is the MOS capacitor. The MOS capacitor is defined by the stack of a metal film, an insulator film and a semiconductor film, as seen in Figure 5 with the external biasing voltage, V_{GB}.

Figure 5 The MOS Capacitor



This configuration means that, as any other capacitor, variations on the biasing voltage incurs in variations on the superficial charges. There is a layer of charge in the metal, called Q_G, a layer of charge trapped in the insulator-semiconductor interface, called Q_0, and a layer of charge in the semiconductor, Q_C. Understanding Q_C is the objective of studying the MOS capacitor, as it is responsible to modulate the current flow in MOSFET devices.

Figure 6 Charge and potential distribution in a MOS capacitor biased with V_{GB} - (TSIVIDIS; MCANDREW, 2011)



2.1.1 Charge sheet model

The surface charge method involves calculating the surface potential and the charge density for each biasing voltage. It is a powerful tool to understand the charges involved and their behavior according to the capacitor functioning conditions.

Using the charge sheet approximation, where it is assumed that the charge is confined to a very thin layer on the semiconductor surface, it is possible to write Poisson's equation (equation 1), as equation 2, and derive an expression for the surface charge Q_C', presented in equation 3.Ψ_s is the surface potential of the charge sheet model, $\Psi(y)$ is the potential in the point y, $\rho(y)$ is the charge density in the point y, ε_s is the absolute permittivity of the semi-conductor, q is the elementary charge, Φ_t is the thermal voltage, p_0 is the surface density of holes, n_0 is the surface density of electrons, N_D is the concentration of donor atoms, Q_C' is the surface density of capacitor charges and n_i is the intrinsic concentration of charge carriers in the semiconductor.

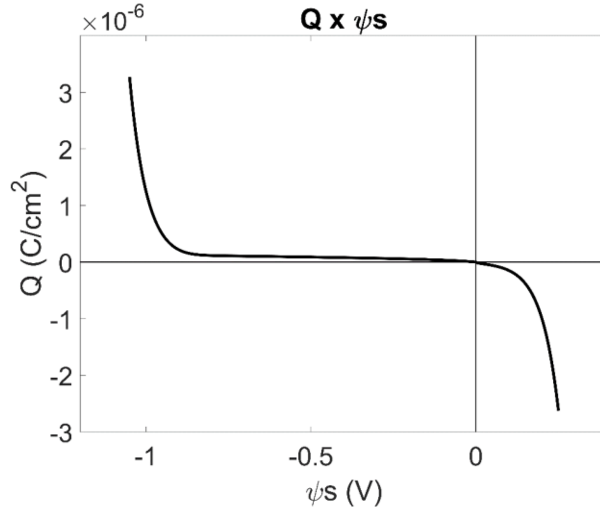
$$\frac{d^2\psi(y)}{dy^2} = -\frac{\rho(y)}{\varepsilon_s} \qquad \text{Eq. 1}$$

$$\frac{d^2\psi_s}{dy^2} = \frac{-q}{\varepsilon_s}\left(p_0 e^{-\psi(y)/\Phi_t} - n_0 e^{\psi(y)/\Phi_t} + N_D\right) \qquad \text{Eq. 2}$$

$$Q'_C = \pm\sqrt{2q\varepsilon_s}\sqrt{\Phi_t \frac{n_i^2}{N_D}\left(e^{-\psi_s/\Phi_t} - 1\right) + N_D\Phi_t(e^{\Phi_s/\Phi_t} - 1) + N_D\psi_s} \quad \text{Eq. 3}$$

By solving equation 3 numerically, it is possible to plot the $Q'_C\ x\ \psi_s$ behavior of the MOS capacitor, as seen in Figure 7. The parameters used are for an-type substrate, with initial doping concentration of 5.10^{16} phosphorus atoms/cm^3, a 10-nm-thick hafnium dioxide (HfO_2) oxide layer, and a TiN metal layer.

Figure 7 $Q'_C\ x\ \psi_s$ plot of the example MOS capacitor



The relation of the surface potential to the external voltage is written in equation 4, where Ψ_{ox} is the voltage drop across the oxide and Φ_{MS} is the metal-semiconductor potential.

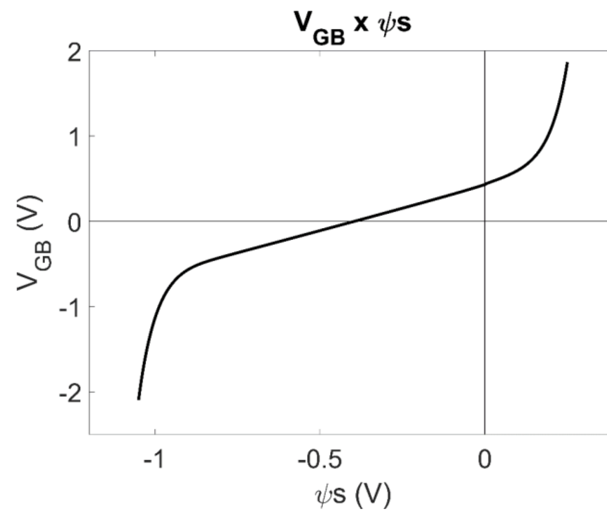
$$V_{GB} = \Psi_{ox} + \Psi_s + \Phi_{MS} \quad \text{Eq. 4}$$

The voltage drop in the oxide is given in equation 5, where Q'_o is the area density of charges in the oxide-semiconductor interface and C'_{ox} is the capacitance per area of the MOS capacitor.

$$\Psi_{ox} = -\frac{Q'_o}{C'_{ox}} \quad \text{Eq. 5}$$

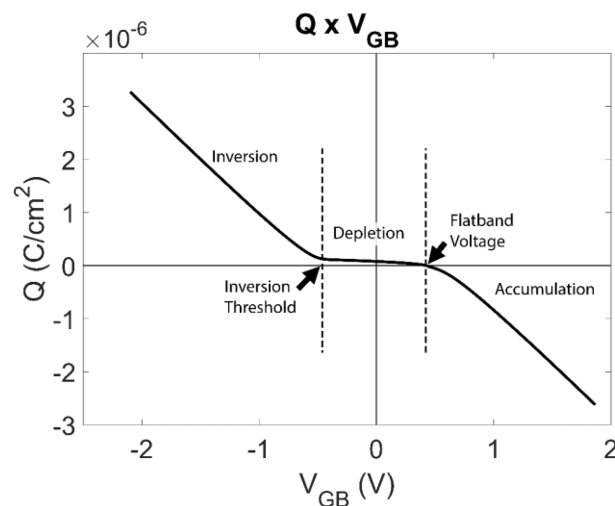
By solving equations 4 and 5, it is possible to plot a $V_{GB}\ x\ \psi_s$ curve for the MOS capacitor, in 0. In this figure it is possible to notice the ψ_s saturation, when V_{GB} exceeds the range of approximately 0.55V around the opposite of the flatband voltage, increasing V_{GB} further has little effect on ψ_s. The saturation effect is the main limit on increasing inversion and accumulation regions by increasing or decreasing the external biasing.

Figure 8 $V_{GB}\ x\ \psi_s$ plot of the example MOS capacitor



By combining the results plotted in both Figure 7 and 0, it is possible to achieve the final behavior of the surface charges according to external bias, $Q_C'\ x\ V_{GB}$, plotted in0. In the $Q_C'\ x\ V_{GB}$ plot, there are three regions indicated: Accumulation, Depletion and Inversion. These conditions are of utmost importance for the functioning of MOSFET devices. By shifting the charge density and polarity on the semiconductor surface through the gate bias, the current can be modulated.

Figure 9 $Q_C'\ x\ V_{GB}$ plot of the example MOS capacitor



In accumulation, the majority charge carriers, those with the same charge type of the semiconductor doping, start to accumulate on the semiconductor-oxide surface, increasing the superficial density of charges.

In depletion, the only charges present are those of the ionized doping atoms. Because those atoms are in a substitutional position in the silicon crystallographic structure, these are

not charge carriers due to having no mobility, and no current can flow through this configuration.

In inversion, in addition to the doping atoms, opposite charge type carriers of the semiconductor charges are generated in the surface, giving this region its name. There are two main thresholds, the weak inversion threshold voltage, where the minority charges start to appear, and the strong inversion threshold voltage where the inversion charges become dominant.

In the flatband voltage, no charges resulting from the capacitor operation are present, only those extrinsically introduced charges from the semiconductor doping. In this configuration, the outside biasing is equal, but opposite, to the metal-semiconductor and the oxide voltage drops, thus making every perpendicular electric field to be cancelled. The net zero electrical field also implicates lesser surface scattering of the charge carriers, and then the semiconductor behaves as a resistor with a resistivity dependent on dopant concentration. In these conditions, (COLINGE et al., 2010) argues that it can be said that the semiconductor presents “bulk mobility”.

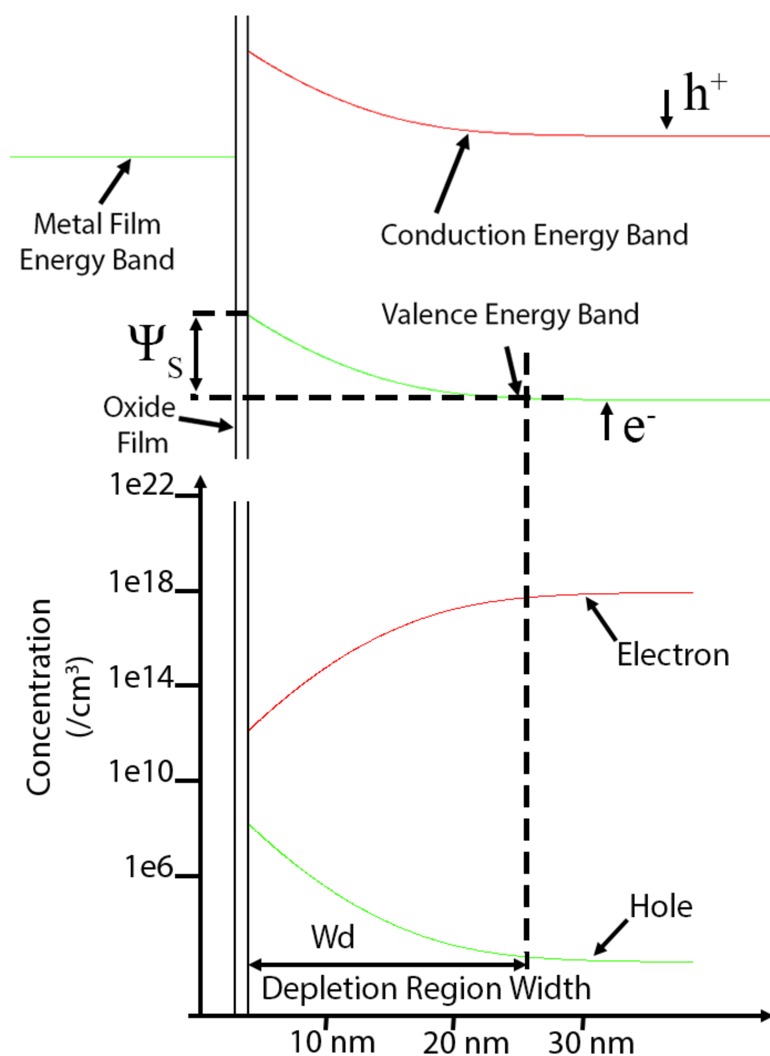
2.1.2 Band diagram

The charge sheet model is most useful when used to define the charge carriers polarity and superficial density in a MOS capacitor. When there is a need to evaluate these charge carriers according to depth in the semiconductor, another tool is used, the Band Diagram. The band diagram is an approximation that consists of plotting the energy levels of the materials used in the y-axis, and the depth in the x-axis. The energy level for holes increased downwards, while the energy level for electrons increases upwards. Known parameters such as the electron affinity, work function and Fermi level are used to situate the bands of different materials in regard to one another. Junctions are then drawn by following current flow or charge carrier accumulations in the materials involved. It is used as a way to visualize the energy levels and the effects of the MOS capacitor on electric field, charge carrier concentration and potential barriers. Due to being an approximation, exact energy levels are usually omitted and are characterized by their relation to one another, although calculated energy and depth values can be added to illustrate junctions and biasing.

In a band diagram, the effects of the MOS capacitor construction and the external biasing are readily visible, and other parameters such as electric potential and voltage barriers can be easily estimated. 0(a) shows the band diagram of a common MOS capacitor compromised of a TiN metal layer, with a work function of around 4.7 eV, a 2 nm thick silicon oxide layer and a semiconductor substrate of n-type silicon with a dopant concentration of approximately 10^{18} atoms.cm^{-3}. In 0(b) it is possible to see the decrease in electron concentration and increase in hole concentration according to the depth, since the hole concentration is not higher than the electron concentration, the surface is in depletion. This image is aligned to the band diagram to show the correlation between charge density, most easily calculated in the charge sheet model, and the energy bands of the band diagram.

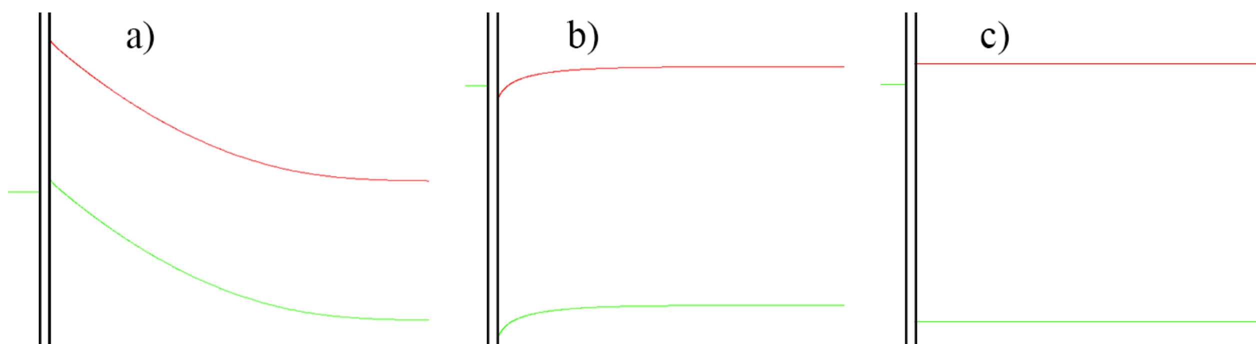
Figure 10 Complete band diagram and charge concentration plot for the example MOS capacitor.

The electron energy level axis and the holes energy level axis are represented by arrows labeled e^- and h^+, respectively. The surface potential, ψ_S, and the depletion region width, W_d, are represented.



By introducing the external voltage V_{GB} the bands can be shifted up and down in relation to one another. In Figure 11 the MOS capacitor represented above is biased to achieve the superficial state of inversion, accumulation and in the flatband voltage.

Figure 11 Band diagram of the example MOS capacitor for different biasing conditions. a) In inversion. b) In accumulation. c) In the Flat-band condition.



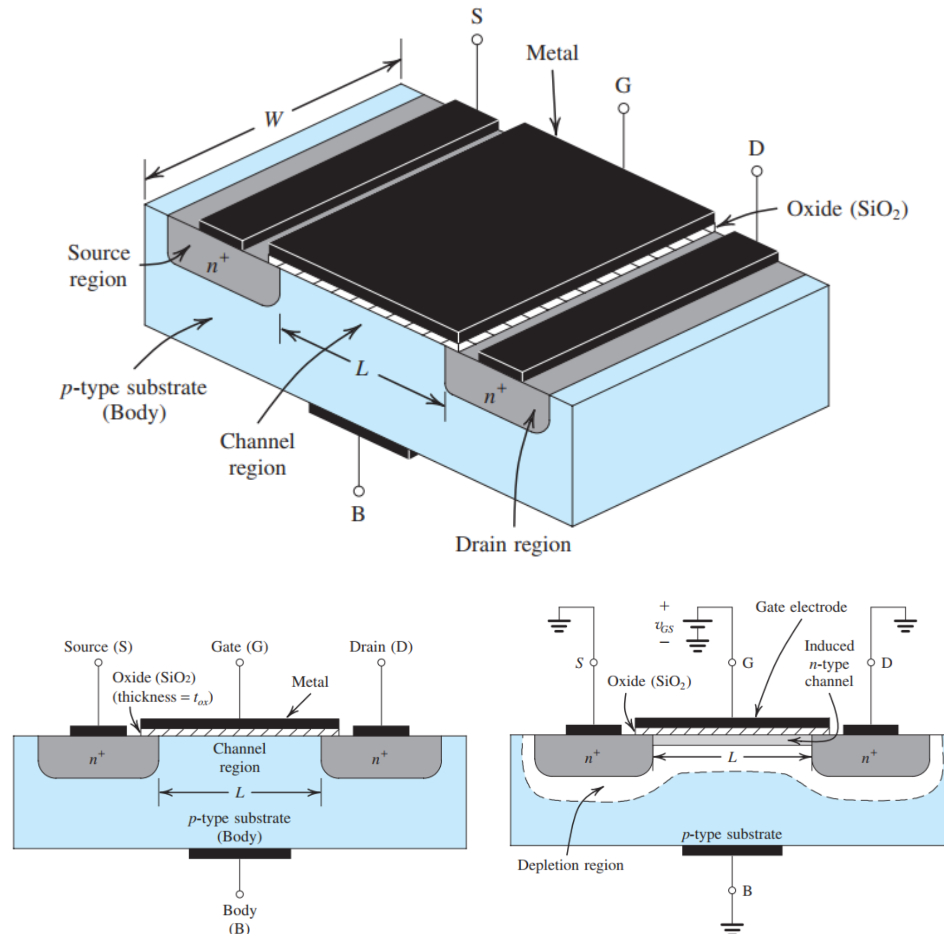
2.2 TRADITIONAL ENHANCEMENT-TYPE MOSFET DEVICE

Enhancement-type MOSFETs are the standard device in the micro and nanoelectronics industry. Their market penetration is well-explained: they are easy to manufacture, present a good I_{on} / I_{off} ratio and very good parameter control. They have been miniaturized and improved upon since their inception in the 1950s.

The functioning principle of the enhancement-type MOSFETs is simple: initially, two opposing p-n junctions act as a very efficient barrier for the electric current, driving down I_{off} figures. In the material that is closer to the gate oxide, the effects of gate bias is able to drive the semiconductor into inversion as soon as the gate voltage surpasses the threshold voltage. In this configuration, there is a continuous conduction path from source to drain made up entirely of electron-rich silicon. Since the semiconductor must be driven into inversion for the current to flow, NMOS devices are fabricated on p-type wafers by implanting the drain and source regions, and PMOS devices are fabricated on n-type wafers by the same technique. Usually a polycrystalline silicon gate is deposited and defined before the source-drain implantation, in what is called a “self-aligned” process. When this polycrystalline gate is removed and another metal gate is fabricated, it is a process named “dummy gate”. The depletion-type MOSFET has the same principles, but a channel is implanted in the substrate, allowing current flow event at 0 V gate bias.

The typical n-type MOSFET fabricated using a planar process is represented in Figure 12.

Figure 12 Schematic of a standard planar MOSFET device (SEDRA; SMITH, 2015)



2.3 THE JUNCTIONLESS-FET DEVICE

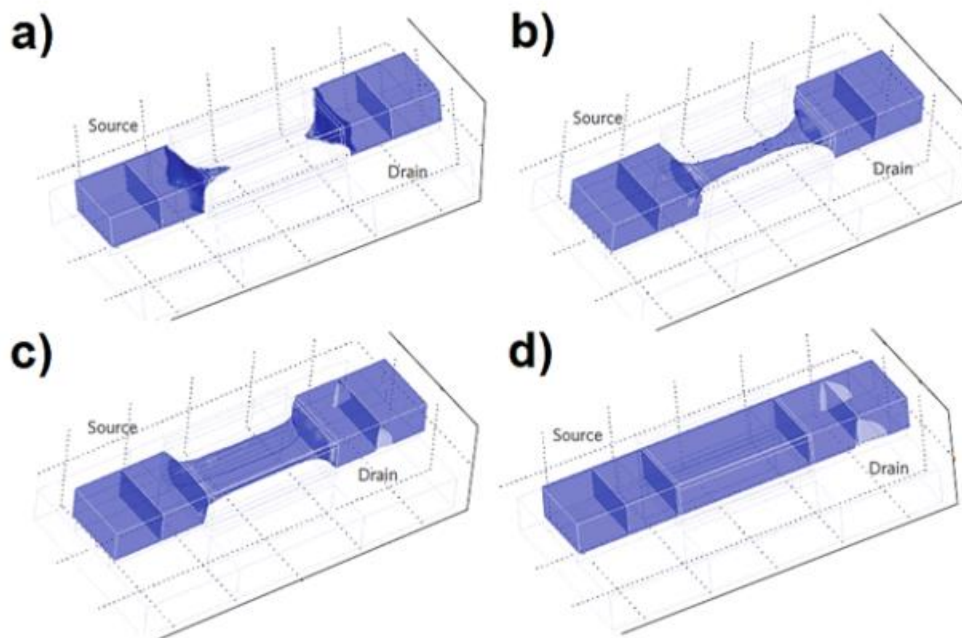
The main difference between the JL-FET and the traditional inversion-type MOSFETs is the flat dopant concentration across the device, and therefore an absence of p-n junctions. Normally, this structure would act as a gated-resistor, since the electrostatic control that stems from the MOS gate-stack does not have a very good control on the charge carriers present on the devices channel.

To operate this device as a transistor, the gate dimensions, or at least one of them, must be equal or thinner than the depletion region width when the gate voltage is 0V. In these conditions, the gate-stack will be able to deplete every charge carrier, thus creating the cut-off region of the transistor operation. When a bias voltage is applied to the gate-stack,

the surface potential diminishes, and the depletion region gets narrower, thus permitting the current flow. As more charge carriers are available to participate in the current flow, the magnitude raises. The charge carrier concentration is represented in Figure 13.

Figure 13 Representation of the charge carrier density in a JL-FET device.(COLINGE et al., 2010)

a) when $V_{GS}< V_{TH}$, the channel is completely depleted. b) when V_{GS} is near V_{TH}, the sub-threshold region, the channel begins to form. c) when $V_{GS}>> V_{TH}$ the channel is completely formed. d) when $V_{GS}=V_{FB}$ the device is in flatband condition, the net perpendicular electric field is null and the device is a doped-silicon resistor.



The current response for the gate voltage in JL-FET devices in comparison with enhancement and depletion type MOSFETs is plotted in 0, while the charge carrier layers and physical comparison of JL-FET and inversion-mode transistors is presented in Figure 15. While comparing the physical structure of both devices side by side, one of the main differences between inversion-mode and JL-FET devices is evident: in inversion devices, the current flow is mainly comprised of minority charge carriers, introduced by the inversion-layer, while in JL-FET devices the majority carriers are the main components of current.

Figure 14 Log(I_D) x V_{GS} plots of MOSFET and JL-FET devices(COLINGE et al., 2010) a) Enhancement-type MOSFET b) Depletion-type MOSFET c) JL-FET

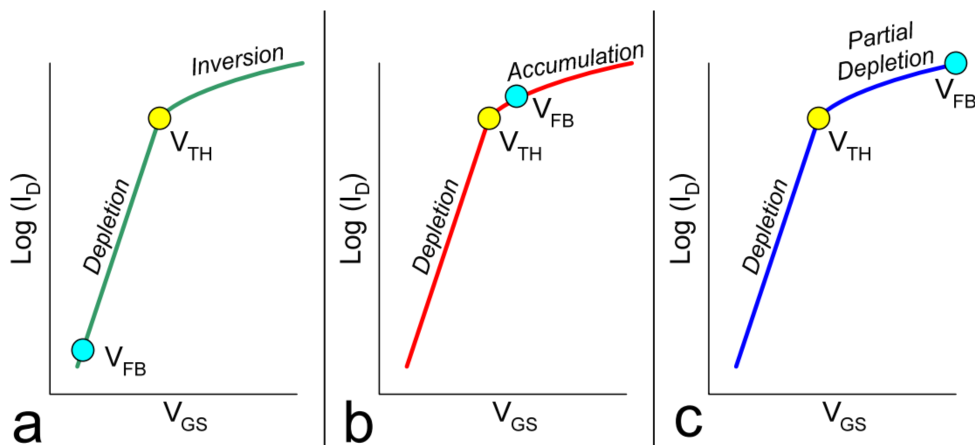
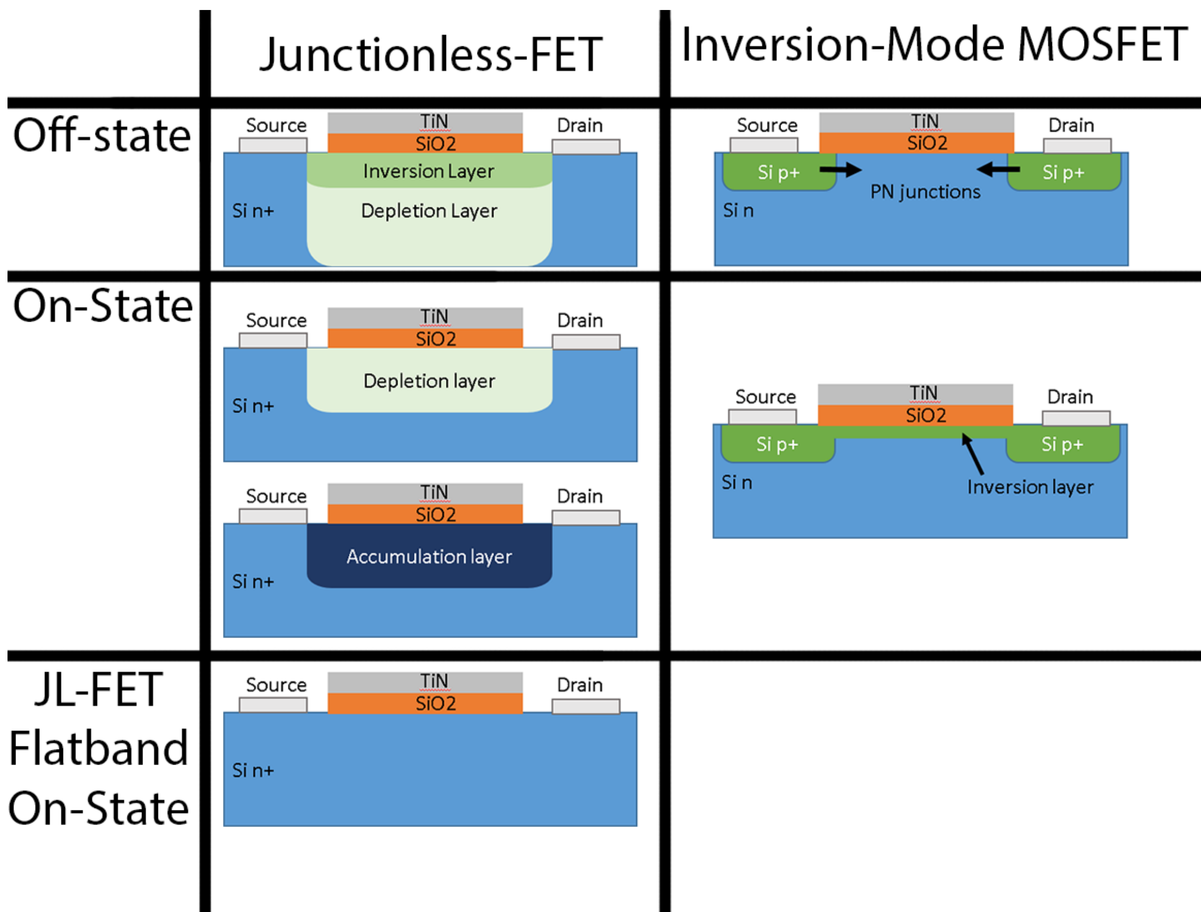


Figure 15 Comparison of charge carrier and dopant concentrations in JL-FET and inversion-mode MOSFETs



2.4 PHOTOLITHOGRAPHIC PATTERNING TECHNIQUES

The patterning process used throughout the fabrication was the optical photolithography, which consists of using light to transfer the patterns from a prefabricated mask onto the samples, through photosensitive reactions in a polymer called photoresist. This process is well established and is used in high-end industrial fabrication plants due to its high throughput, as a flood exposition process capable of patterning thousands of dies with each exposure, and good precision and minimum line length built over decades of technological advancements. Such as the projection lithography, where an array of lenses can improve the patterned structures, and immersion lithography.

2.5 CONTAMINANTS CONTROL

In nanoelectronics, even the smallest contaminants can have destructive effects. Therefore, all device processing must be performed in clean room environment, and precise cleaning techniques must be used. This section is dedicated to explaining the optimal conditions and how to achieve them.

2.5.1 Deionized water

In semiconductor processing, metallic ions such as K^+ and Na^+ must be eliminated, since they present high mobility inside silicon oxide and monocrystalline silicon, and could damage the solid structure of the materials. Therefore, water used in semiconductor processing must be purified and deionized by filtering and ionic exchange with especially engineered membranes. To be adequate for semiconductor processing, deionized water must present a resistivity of 18 MΩ.cm.

2.5.2 Stantard cleaning

The standard cleaning, or RCA cleaning, is used as a first cleaning technique in new wafers and every front-end-of-line cleaning process thereafter. In back-end-of-line processes this cleaning gives place to the organic cleaning, since the alkaline and acidic solutions used are metal etchants. It is responsible to remove organic and metallic contaminants and is performed in a 4-step system, with rinsing in deionized water after each step, as seen in table 2.

Table 1 Steps of the Standard RCA cleaning. (PUYDINGER DOS SANTOS, 2013)

Reagents	Ratio	T (°C)	Time	Comments
H_2SO_4/H_2O_2	4:1	80	10 min	This step removes organic compounds from the surface of the silicon wafer. As a result of this reaction, silicone dioxide is formed in the surface.
HF/H_2O	1:10	Room temperature	10 s	The hydrofluoric acid removes the silicon dioxide formed in the first step.
H_2O	-	Room temperature	-	Rinsing in deionized water with resistivity of 18 MΩ.cm
$NH_4OH/H_2O_2/H_2O$ (RCA standard cleaning #1)	1:1:5	80	10 min	This step removes organic compounds and metals from the 1B and IIIB groups of the periodic table. This step also causes an increase in the superficial roughness of the substrate.
H_2O	-	Room temperature	-	Rinsing in deionized water with resistivity of 18 MΩ.cm
$HCl/H_2O_2/H_2O$ (RCA standard cleaning #2)	1:1:5	80	10 min	This step removes alkaline ions and Fe, Al, and Mg hydroxides. Also polishes chemically the sur-

				face of the wafer, which had become rough after the $NH_4OH/H_2O_2/H_2O$ step.
H_2O	-	Room temperature	-	Rinsing in deionized water with resistivity of 18 MΩ.cm
HF/H_2O	1:10	Room temperature	10 s	The hydrofluoric acid removes the silicon dioxide formed by the last two steps.
H_2O	-	Room temperature	-	Rinsing in deionized water with resistivity of 18 MΩ.cm

2.5.3 Organic cleaning

Organic cleaning is used in back-end-of-line processing, where metallic films are already present in the structures and alkaline and acid solutions cannot be used. It is also widely used to remove photorresists and other polymeric films where the full RCA cleaning is not needed.

The organic cleaning, consists of a quick rinse in cold acetone, followed by a 10 minutes bath in acetone heated to its boiling point in a hotplate, and a 10 minutes bath in isopropyl alcohol also at its boiling point in a hotplate. Rinse in deionized water and isopropyl alcohol with drying in a 110°C hotplate.

2.6 ANISOTROPIC SILICON ETCHING IN NH_4OH SOLUTION

The anisotropic silicon etching is a process in which the silicon is etched in an alkaline solution. This kind of etching reacts about ten times faster with the (100) family of crystallographic planes in silicon than it does with the (111) family of planes, giving the etched structures a distinct V shapes most commonly known as V-Groove(SHIKIDA et al., 2002). In (100) wafers, the sidewalls present a constant angle of 54.74° to the surface of the wafer. These structures can therefore be manipulated to fit a number of etched thicknesses, transferred patterns and effective etched patterns. Other works showed device fabrication by

using the atomically sharp edge of the V-groove to fabricate 3 nm-long devices with TMAH (MIGITA et al., 2012, 2014), and using NH4OH to thin structures sideways using the more controlled (111) etching rate (SILVA et al., 2014).

The anisotropic silicon etching etching can be achieved in a number of alkaline solutions, such as KOH, hydrazine, Tetramethylammonium Hidroxide (TMAH) and NH_4OH. KOH solutons are commonly used in Micro Eletromechanichal Systems (MEMS), and although it is a cheap and well-understood process for silicon anisotropic etching, it causes K^+ ions incorporation in silicon and silicon dioxide, making it unsuitable for nanoeletronics fabrication. TMAH is another alternative, commonly found in most fabrication plants in photoresist developers as it presents a controlled, slow etching rate, and does not introduce metal ions such as K^+. In this work, the NH_4OH solution was chosen to perform the silicon anisotropic etching. This solution can be about 10 times cheaper than TMAH solutions, has a higher etching rate and has then same ion-free properties, making it a perfect choice for accessible nanoeletronics fabrication.

The anisotropic etching rate of alkaline solutions can be seen represented in in greater detail in Figure 16. In Figure 16 (a), the exposed crystallographic planes of the silicon are shown. The angle of the sidewall can be calculated by taking the angle between (100) planes and (111) planes. It is approximately 54.74° as shown in Figure 16 (b).

In Figure 16 (b), the sidewall angle can be used to correlate the etched thickness and the gate length variation, and an effective gate length L' can be calculated using equation 8, as seen in Figure 16 (c).

$$L' = L - \frac{2h}{tan(a)} \qquad \text{Eq. 6}$$

$$L' = L - \frac{2h}{tan(54.74°)} \qquad \text{Eq. 7}$$

$$L' \cong L - 1.41h \qquad \text{Eq. 8}$$

Figure 16 Sidecut view of a structure etched in NH_4OH solution.

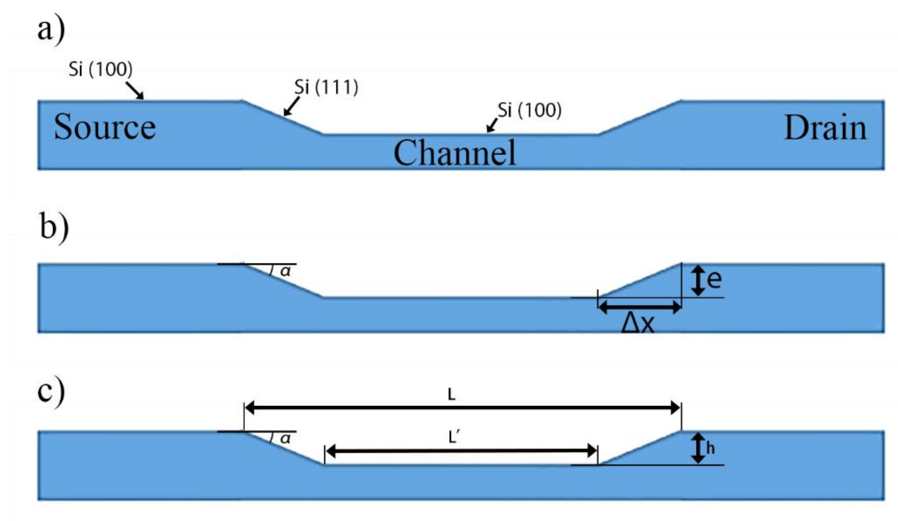
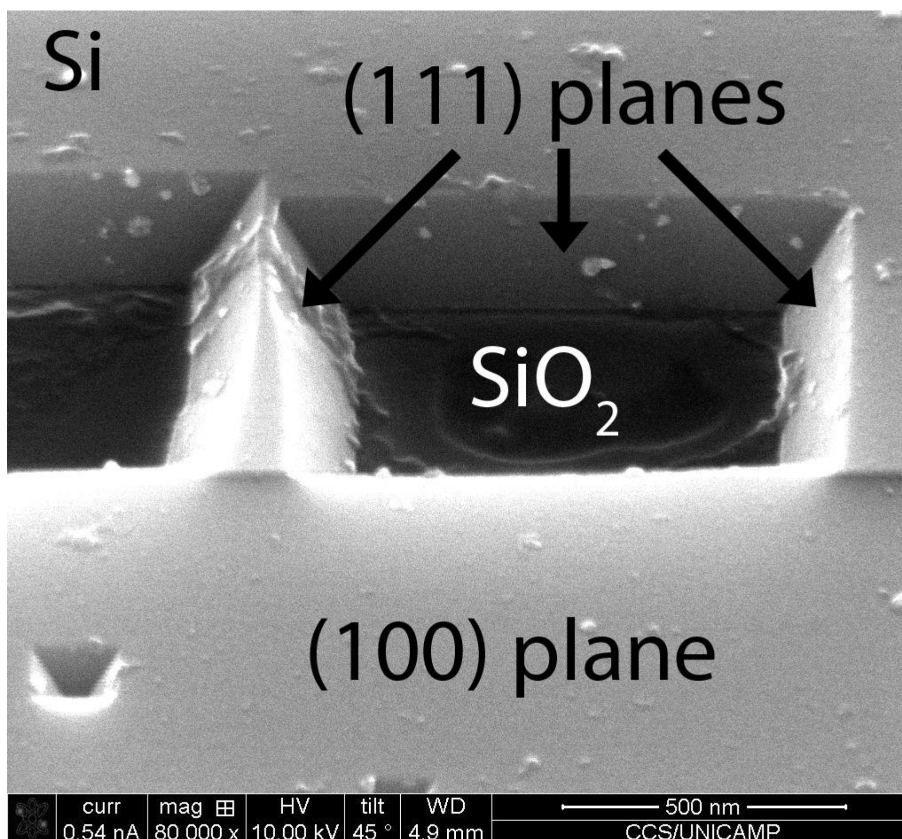


Figure 17 SEM image of a structure etched in NH_4OH solution.



The etching times chosen were calibrated according to previous tests, as described in Chapter 4. As a general rule, it is better to design a longer etching time since this process takes a few seconds to achieve thermal equilibrium, making the etching rate chaotic during the first seconds. Large quantities of Ammonia gas are also a byproduct, causing the formation of gas bubbles on the etched surface and impairing the etchant circulation. In longer

processes, the unpredictable effects of both these phenomena are statistically smoothed, creating a better etch rate function.

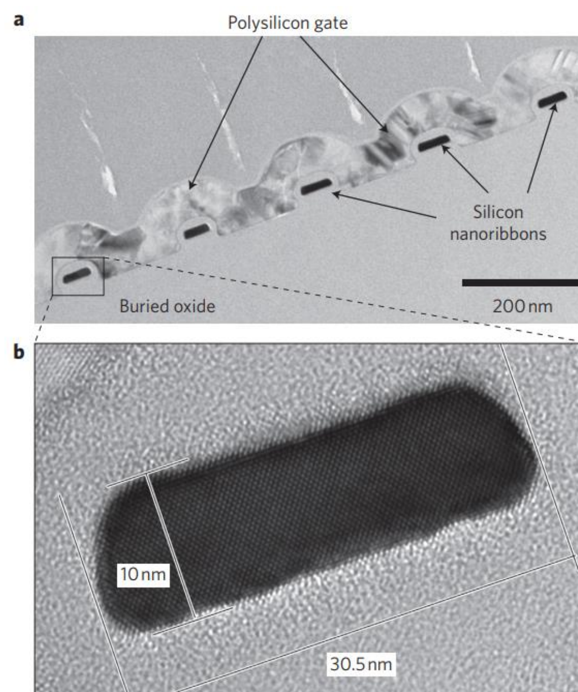
2.7 PREVIOUS RESEARCH

2.7.1 The original JL-FET

First proposed in 2010, the JL-FET devices in (COLINGE et al., 2010) were fabricated using 10-nm-thick and a few tens of nanometers wide silicon channels, called “silicon nanoribbons”, defined using electron beam lithography. The channel doping was performed by ionic implantation of arsenic to yield an uniform doping concentration of $2x10^{19}$to $5x10^{19}$ atoms/cm^3. The gate oxide was a 10-nm-thick grown silicon oxide and the gate was fabricated using polycrystalline silicon. The Transmission Electron Microscopy (TEM) images of the fabricated devices are shown in Figure 18.

Figure 18 TEM images of the devices fabricated by (COLINGE et al., 2010).

“a) Five parallel devices with a common polysilicon gate electrode. b) Magnification of a single nanoribbon device. Individual atomic rows can be seen in the silicon”(COLINGE et al., 2010).



The electric characteristics of the devices shown were parallel to those of the state-of-the-art MOSFETs. In the I_D x V_{GS} plots, shown in 0, the on/off current ratio was larger than 1x10^6, and the substhreshold swing was of 64 mV/dec, close to the theoretical minimum of 60mV/dec. The curve for a trigate FET is also shown for comparison. In the I_D x V_{DS} plots, shown in Figure 20, the typical transistor behavior is seen, with clear cut-off, triode and saturation regions.

Figure 19 I_D x V_{GS} measurements of the devices fabricated by (COLINGE et al., 2010)

> "Drain current versus gate voltage for drain voltages of +50 mV and +1 V. The off current is below the detection limit of the measurement system (1x10^{-15} A), and the on/off current ratio for between V_G=0 and V_G=+1 V is larger than 1x10^6. The width of the device is 30 nm. The curve for a classical trigate FET is shown for comparison." (COLINGE et al., 2010)

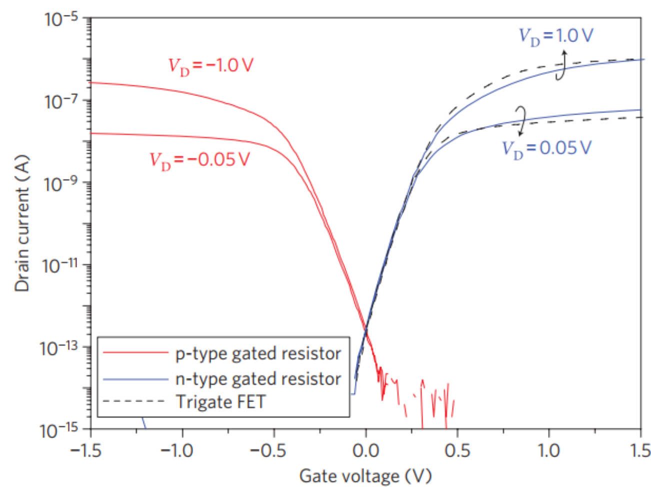
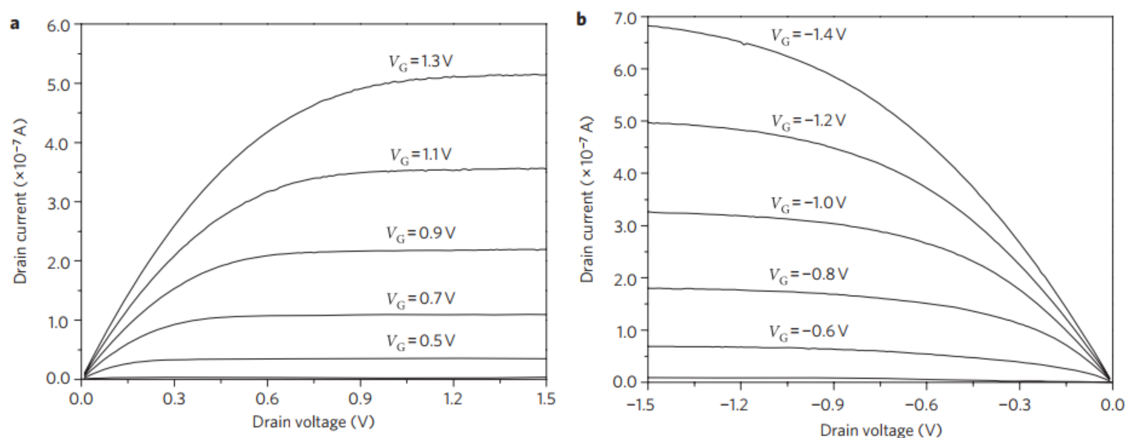


Figure 20 I_D x V_{DS} measurements of the devices fabricated by (COLINGE et al., 2010)

> "a,b, Drain current versus drain voltage for different values of gate voltage for an n-channel gated resistor (a) and a p-channel gated resistor (b). The width of the nanowires, W, is 20 nm and the gate length, L, is 1 mm, such that W/L=0.02." (COLINGE et al., 2010)

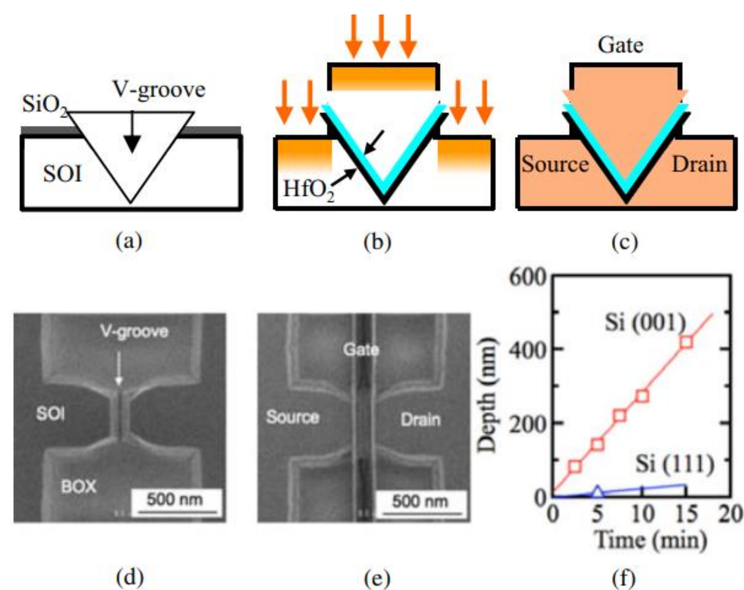


2.7.2 Using silicon anisotropic etching in TMAH

Devices fabricated using silicon etching in TMAH solution were shown by (MIGITA et al., 2012, 2014). In (MIGITA et al., 2014), the surface of a 88-nm-thick silicon over 144-nm-thick silicon dioxide SOI substrate was used. The surface orientation was (100) and the initial dopant concentration was 10^{15} atoms/cm^3 of boron. The surface was covered with a thin film of SiO_2 and slit patterns were drawn using electron lithography, the oxide film in these slit patterns were then etched using HF solution. The silicon wafers were then dipped into a 25 wt% solution of TMAH at room temperature. A 3-nm-thick HfO_2 film was then deposited by atomic layer deposition for the gate dielectric film. A 10-nm-thick TaN film and a 100-nm-thick polycrystalline Si film were then deposited as gate metal by dc sputtering and chemical vapor deposition. The gate was then patterned using electron-beam lithography and reactive ion etching. The wafers were then implanted for both p-type (BF^2 at 15keV and dose of $2*10^{15}$atoms/cm^2) and for n-type (P at 15keV and dose of $2*10^{15}$atoms/cm^2). The electric contacts metallization and final annealing in H_2 gas at 400C for 30 minutes were performed.

Figure 21 Process flow outline of (MIGITA et al., 2014).

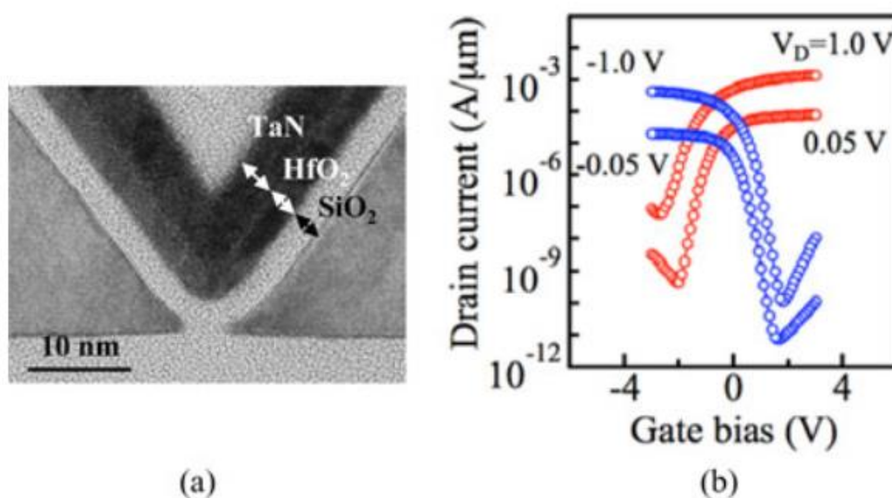
"(a) Partial removalof SiO2 mask and anisotropic wet etching of SOI substrate using TMAH solution. (b) Deposition of gate stack films, gate electrode patterning, and ionimplantation. (c) Long-period annealing for diffusion and activation of dopants(1000 ◦C 10 min). (d) SEM image of the V-groove formed on SOI. (e) SEMimage after the gate patterning. (f) Anisotropic wet etching nature of Si substrate" (MIGITA et al., 2014)



In the first attempt of this study, the devices showed partial oxidation of the device channel during dopant activation, as seen in Figure 22, and degradation on the electrical characteristics. The device is normally-on, due to the 3.2-nm effective oxide thickness (EOT).

Figure 22 TEM images and I_D x V_{GS} measurements of (MIGITA et al., 2014) 3.2 nm EOT devices

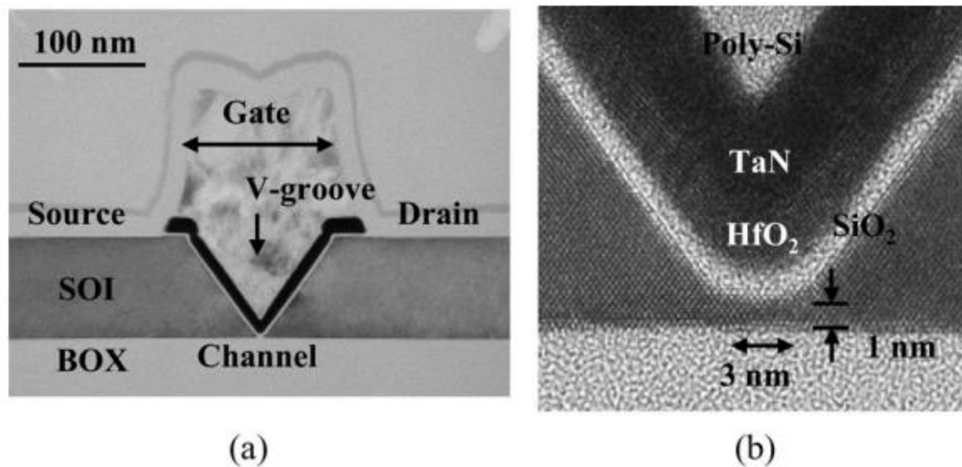
"(a) Cross-sectional TEM image of the V-groove MOSFET with 3.2-nm EOT. (b) Measured ID –VG characteristics (VD = 0.05 and 1.0 V) of n-type and p-type V-groove MOSFETs with 3.2-nm EOT, 1-nm channel thickness, and 1-mm channel width." (MIGITA et al., 2014)



After reducing the EOT to 1.5 nm, and adding a SiN film deposited before the HfO_2 deposition to prevent oxygen diffusion towards the silicon substrate, the devices showed much better electrical characteristics. In 0, the TEM images of the device fabricated with this method is shown, the 1-nm-thick and 3-nm-long device channel is visible with clear distinction of the (100) and (111) planes in silicon. The curving of the sidewalls nearing the channel is argued to be caused by the formation of meta-stable (311) planes in the interface (SHIKIDA et al., 2002).

Figure 23 Cross-Section TEM images of the devices fabricated in(MIGITA et al., 2014)

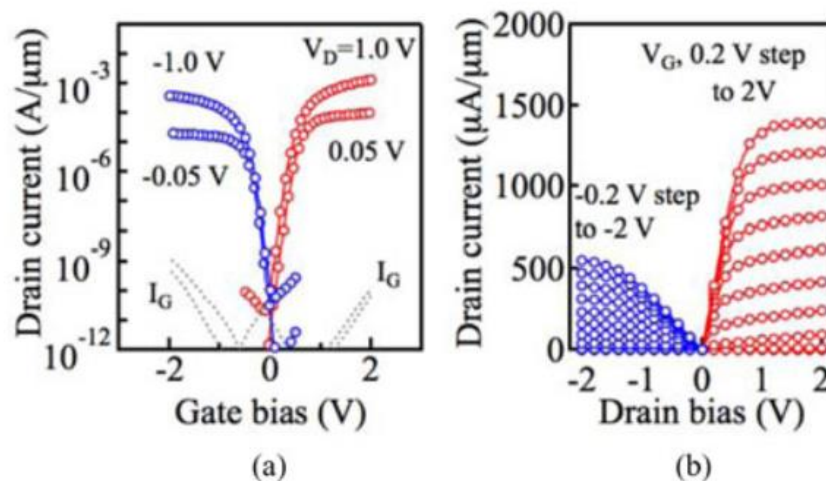
> "(a) Cross-sectional TEM image of the V-groove junctionless FET. The V-groove was formed by anisotropic wet etching of SOI substrate. Source, channel, and drain regions are uniformly doped with high concentration. (b) Magnified image of the channel region. The channel length and the thickness are scaled to 3 and 1 nm, respectively. The gate stack consists of poly-Si/ TaN/ HfO2 /SiO2 layers. The EOT is 1.5 nm and the effective work function is 4.46 eV that were evaluated by C–V measurements MOS capacitors fabricated by the same process flow." (MIGITA et al., 2014)



In 0, the I_D x V_{DS} and I_Dx V_{GS} characteristics are shown. The devices presented good I_{on}/I_{Off} ratio, excellent substhreshold swing and telltale transistor behavior on the I_DxV_{DS} curve.

Figure 24 I_D x V_{GS} and I_D x V_{GS} plots of the devices fabricated in (MIGITA et al., 2014)

> "Electrical characteristics of V-groove MOSFETs corresponding to the sample shown in 0 with 1.5-nm EOT, 1-nm channel thickness, and 1-mm channel width. (a) I_Dx V_{GS} characteristics (V_D = 0.05 and 1.0 V) and (b) I_D xV_{DS} characteristics (VG = 0.0 to 2.0 V by 0.2 V step)." (MIGITA et al., 2014, adapted)



2.8 RESEARCH DEVELOPED AT CCS/UNICAMP

2.8.1 Ga^+ Focused Ion Beam milling and Al diffusion

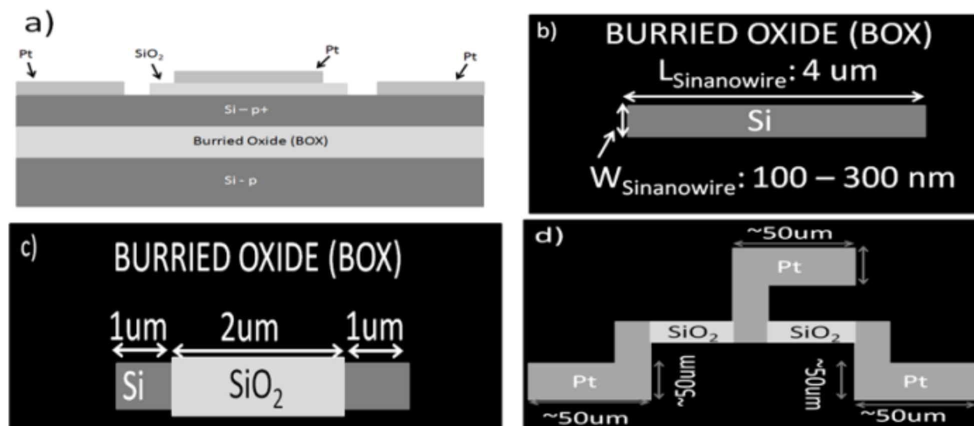
LIMA et al. (2012) demonstrated JL-FET devices fully fabricated using a dual Focused Ion Beam and Scanning Electron Microscopy (FIB/SEM) system. The nanowires were fabricated using FIB milling with Ga^+ ions. In this process, high-energy Ga ions are focused by electrostatic lenses and used to mechanically mill out selected areas. The energy, current and duration of the focused ion beam determine the etched thickness.

The channel doping was performed by diffusing aluminum into the SOI layer. Aluminum was deposited using DC sputtering and an initial diffusing period was performed in conventional furnace at 450ºC for 30 and 60 minutes, the aluminum was removed and a final annealing was performed for 30 minutes at 800ºC and 1000ºC.

The nanowires were then patterned by the FIB milling technique according to the schematics presented in Figure 25. The gate oxide deposition was performed using an electron induced process using a precursor introduced by the Gas Injection System (GIS). The deposition of the gate metal and the electrical contacts were also performed using GIS platinum deposition. Finally, the devices were annealed in forming gas at 450ºC for 5 and 10 minutes.

Figure 25 Schematics of the devices fabricated by (LIMA et al., 2012)

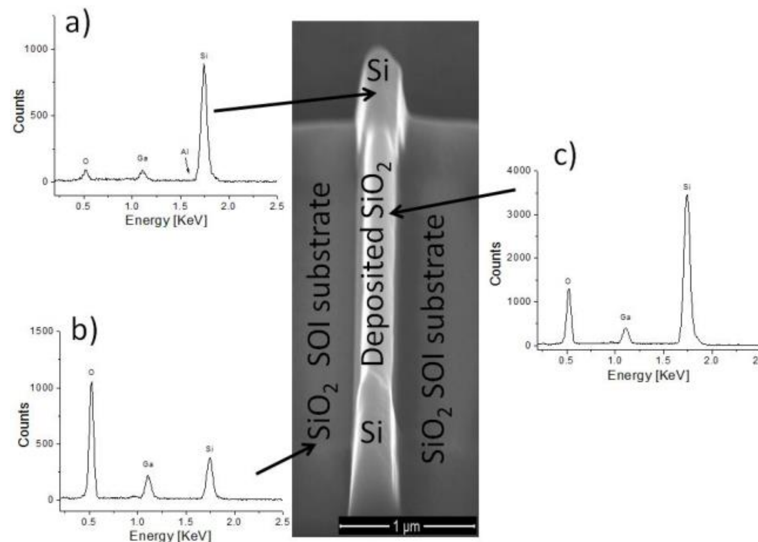
> "JL device on SOI substrate; b) Si p+ nanowire after Al diffusion and FIB milling on SOI substrate; c) gate SiO2 deposited by FIB on Si p+ nanowire; d) Pt gate, source and drain electrodes deposited by FIB." (LIMA et al., 2012)



The structures were characterized by SEM images and X-ray EDS carried out in the FIB/SEM system. These results are shown in 0.

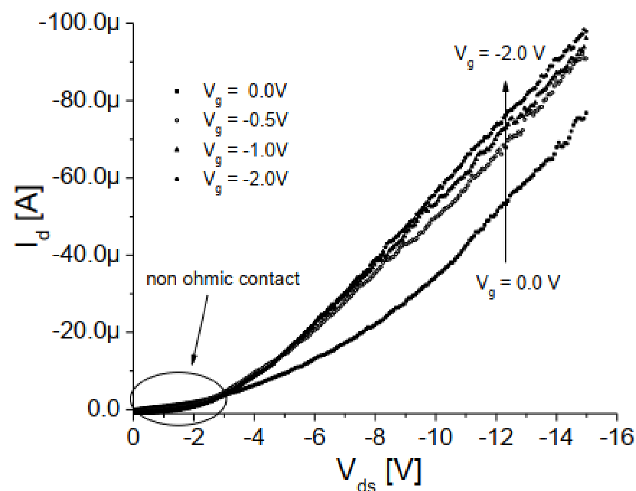
Figure 26 SEM image and EDS measurements of a device fabricated by (LIMA et al., 2012).

"Scanning Electron Microscopy (in the center) of Si nanowire with SiO2 deposited on gate region. EDS measurements of a) Si nanowire region; b) SiO2 of SOI substrate and c) SiO2 deposited by FIB system." (LIMA et al., 2012)



The devices were then electrically characterized in a semiconductor analysis system. The I_D x V_{DS} measurements are plotted in Figure 27. The devices presented a non-ohmic electrical contact, indicating that the aluminum diffusion could not achieve a high enough dopant concentration. The devices also presented a "gated resistor" behavior, this happens when the depletion region is not wide enough to fully deplete the channel of charge carriers.

Figure 27 I_D x V_{DS} measurements of the devices fabricated by (LIMA et al., 2012).



2.8.2 Ga^+ Focused Ion Beam milling with Ga incorporation

PUYDINGER DOS SANTOS et al. (2013) used a similar process to (LIMA et al., 2012), with changes in patterns transferred and that the dopant in the channel region was Ga incorporation after Ga^+ focused ion beam processing and sputtered aluminum was used as gate metal and as a second layer of the electrical contacts metal.

0 shows the process flow used. The SOI layer was thinned to approximately 15 nm by thermal silicon oxidation and HF buffer solution etching. The active region was defined using photolithography. The nanowires were then defined using high energy, 30 keV Ga^+ FIB milling, and a lower energy, 10 keV, Ga^+ FIB process was used to incorporate Ga atoms in the silicon structure. The crystal structure was then reformed and the Ga atoms were activated as doping atoms using RTA processing. Platinum electrodes were then deposited using the GIS system, and the gate metallization and electrical contacts were fabricated using sputtered aluminum and defined using photolithography and lift-off.

Figure 28 Schematics of the process performed by (PUYDINGER DOS SANTOS et al., 2013)

“Schematics of (a) SOI wafer, with 340 nm and 400 nm thick layers of Si and BOX, respectively, after RCA cleaning; (b) SOI wafer (after thermal oxidation and BHF wet etching) with 15 nm thick Si layer on BOX; (c) Si active region mesa on BOX after photolithography and RIE; (d) Si pþ nanowire after GaFIB milling and Gaþ doping; (e) Pt source/drain electrodes deposited by electron beam and GIS dual beam system (see that a pseudo-MOS structure was obtained) and (f) SiO2 gate dielectric also deposited by electron beam, and GIS and Al gate/source/drain electrodes deposited by sputtering and defined by lift-off process” (Puydinger, 2013b)

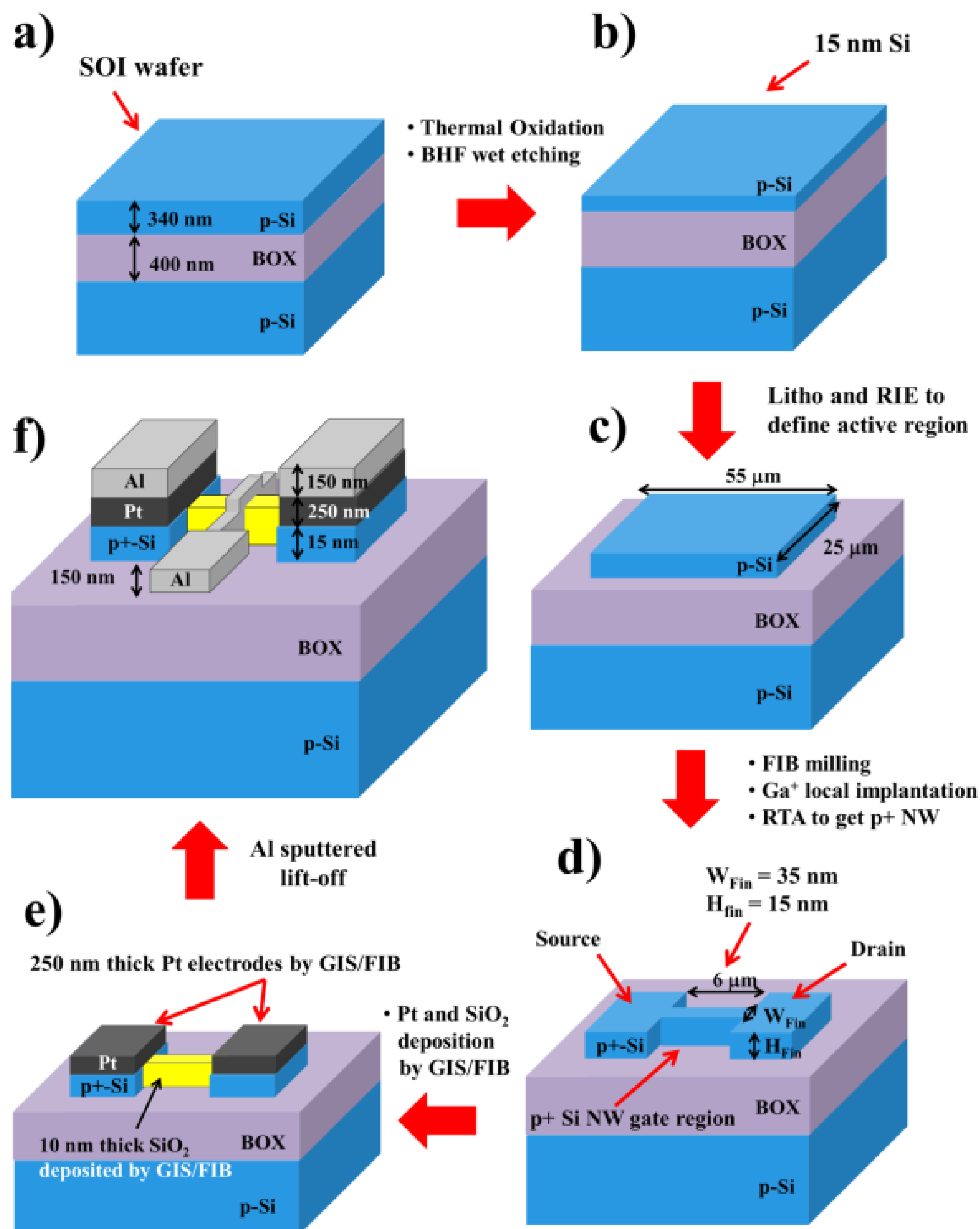
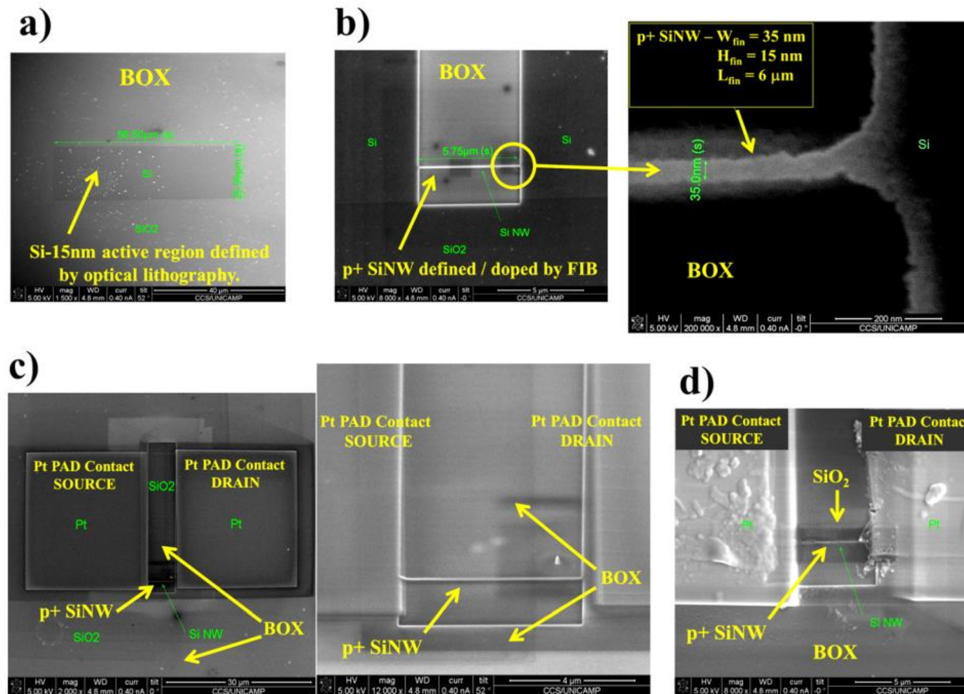


Figure 29 shows the SEM images obtained after each fabrication step. In particular, Figure 29 (b) shows the defined nanowire in detail, measuring approximately 35 nm in width.

Figure 29 SEM images of the structures fabricated by (PUYDINGER DOS SANTOS et al., 2013)

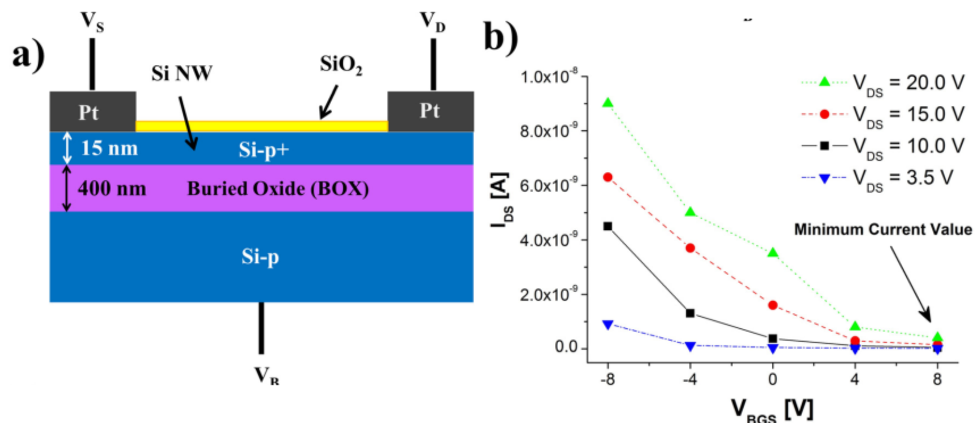
"SEM analyses of (a) Si active region mesa on BOX after photolithography and RIE; (b) SiNW after GaFIB milling and p+ doping; (c) SiNW after Pt source/drain electrodes deposited by electron beam and GIS of dual beam system (pseudo-MOS transistor was obtained); and (d) 10 nm thick SiO2 (also deposited by electron beam and GIS) as gate dielectric for the JNT device" (Puydinger, 2013b)



The structures were characterized using the Pseudo-MOS technique, where an intermediary device is obtained before the gate metal fabrication. This structure is electrically measured by biasing from the backside of the SOI wafer, as shown by the schematic in 0 (a). By using the Pseudo-MOS technique, a number of characteristics of the device channel can be evaluated. The Pseudo-MOS measurements compiled in 0 (b) showed that the minimum observed current is still large, and therefore the depletion region introduced by the gate was not enough to fully deplete the channel region of charge carriers. This indicates that the channel dopant concentration was above $5*10^{15}$ cm^{-3}, confirming the success of the Ga^{+} incorporation doping technique.

Figure 30 Side-view representation and electrical measurements of the Pseudo-MOS device fabricated (PUYDINGER DOS SANTOS et al., 2013)

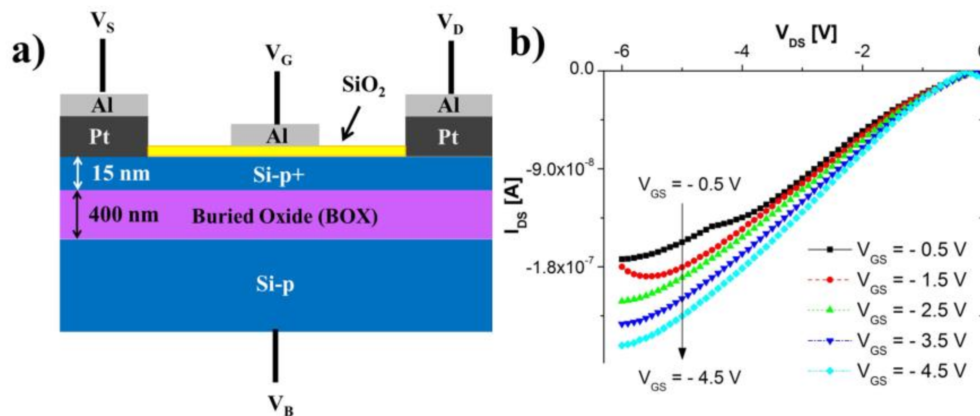
"(a) Schematic of pseudo-MOS device to investigate the electrical behavior of p+-SiNW and (b) I_{DS} vs V_{BGS} curves of pseudoMOS in accumulation regime. The positive voltage for minimum current value (<0.15 nA) indicates that the nanowire structure has doping levels above $5*10^{15}$ cm-3." (PUYDINGER DOS SANTOS et al., 2013)



After the Pseudo-MOS measurements and the confirmation of success in the doping process, the gate-metal was deposited, finishing the device fabrication. The complete Junctionless-FET device, represented in Figure 31 (a), was characterized electrically. The results compiled in Figure 31 (b) show the gated-resistor behavior expected of a device with p-type channel paired with a low work-function gate metal such as aluminum.

Figure 31 Side-view representation and electrical measurements of the Junctionless-FET device fabricated (PUYDINGER DOS SANTOS et al., 2013)

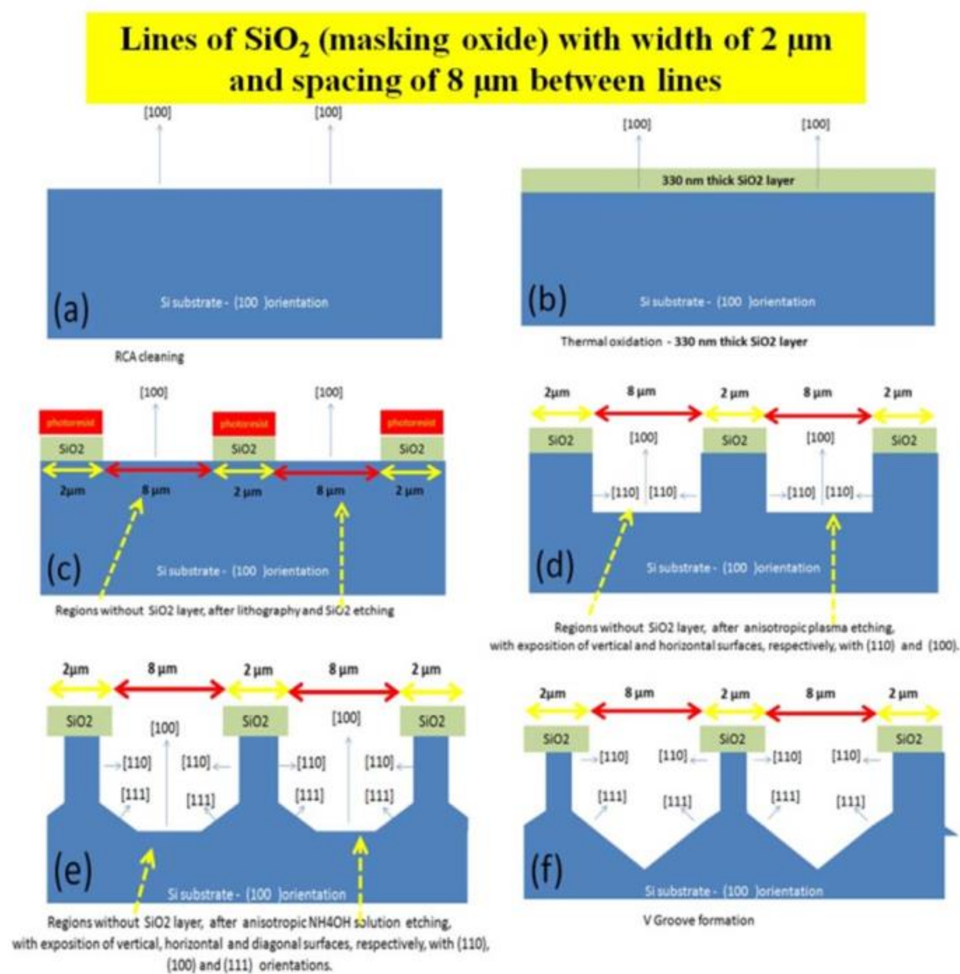
"(a) Schematic of JNT device after completed fabrication and (b) IDS x VDS measurements (for bulk voltage, VB, equal to zero) after 20 min of sintering time"(PUYDINGER DOS SANTOS et al., 2013)



2.8.3 Lateral etching in NH_4OH solution

SOARES et al. (2018) performed a lateral etch using NH_4OH solution to achieve sub-micron wires. In this specific configuration, the silicon channel is etched laterally following the (110) family of planes in silicon, while the bottom portion is initially aligned with the (100) family of planes, at the end of the process the etched area presents an angled sidewall, formed by planes of the (111) family. This occurs since the etching rate of silicon in NH_4OH solution is higher for the (100) family of planes, and there is a saddle-point in the etching rate vs crystal orientation plot exactly in the (111) family of planes.

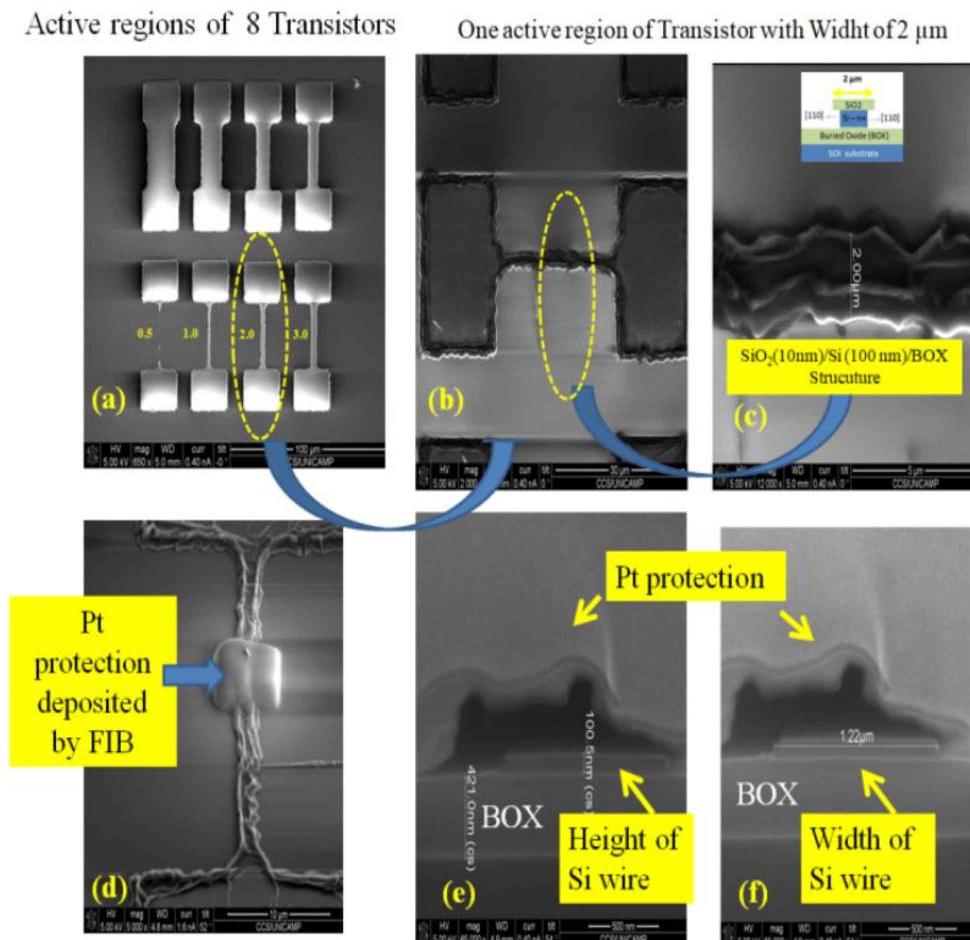
Figure 32 Schematics of the process steps followed by (SOARES et al., 2018)



The structures were characterized using SEM images and measurements, as presented in Figure 33. These images show the Si wires and their respective cross-section view. The fabricated nanowires were measured, and presented thickness of 100 nm and width of

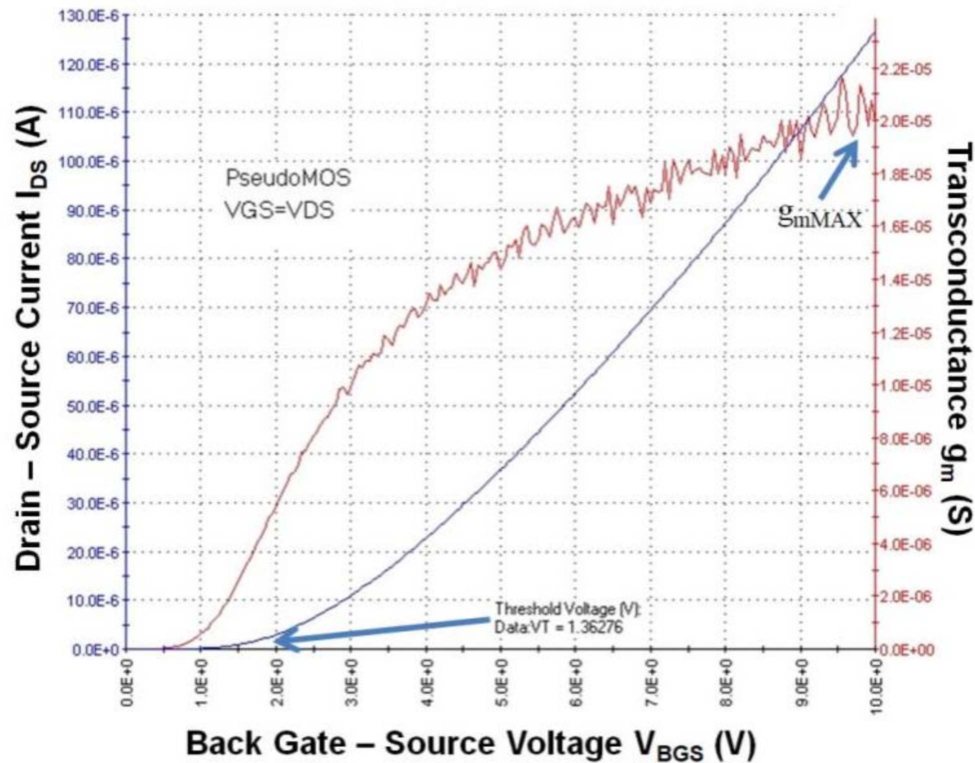
1.22 μm. The nanowire shape is a trapezoid, with the sidewall angle of 54.74 degrees, the characteristic angle formed between the (100) and (111) family of planes in silicon.

Figure 33 SEM images and measurements of the structures fabricated by (SOARES et al., 2018)



The devices were electrically characterized using a Pseudo-MOS measurement. The I_D x V_{BGS} and transconductance (g_m) plot is shown in Figure 34. The devices show the expected behavior of a junctionless-FET device of 100 nm, with a threshold voltage of approximately 1.3 V.

Figure 34 I_D x V_{BGS} and g_m x V_{BGS} plot of the device fabricated by (SOARES et al., 2018)



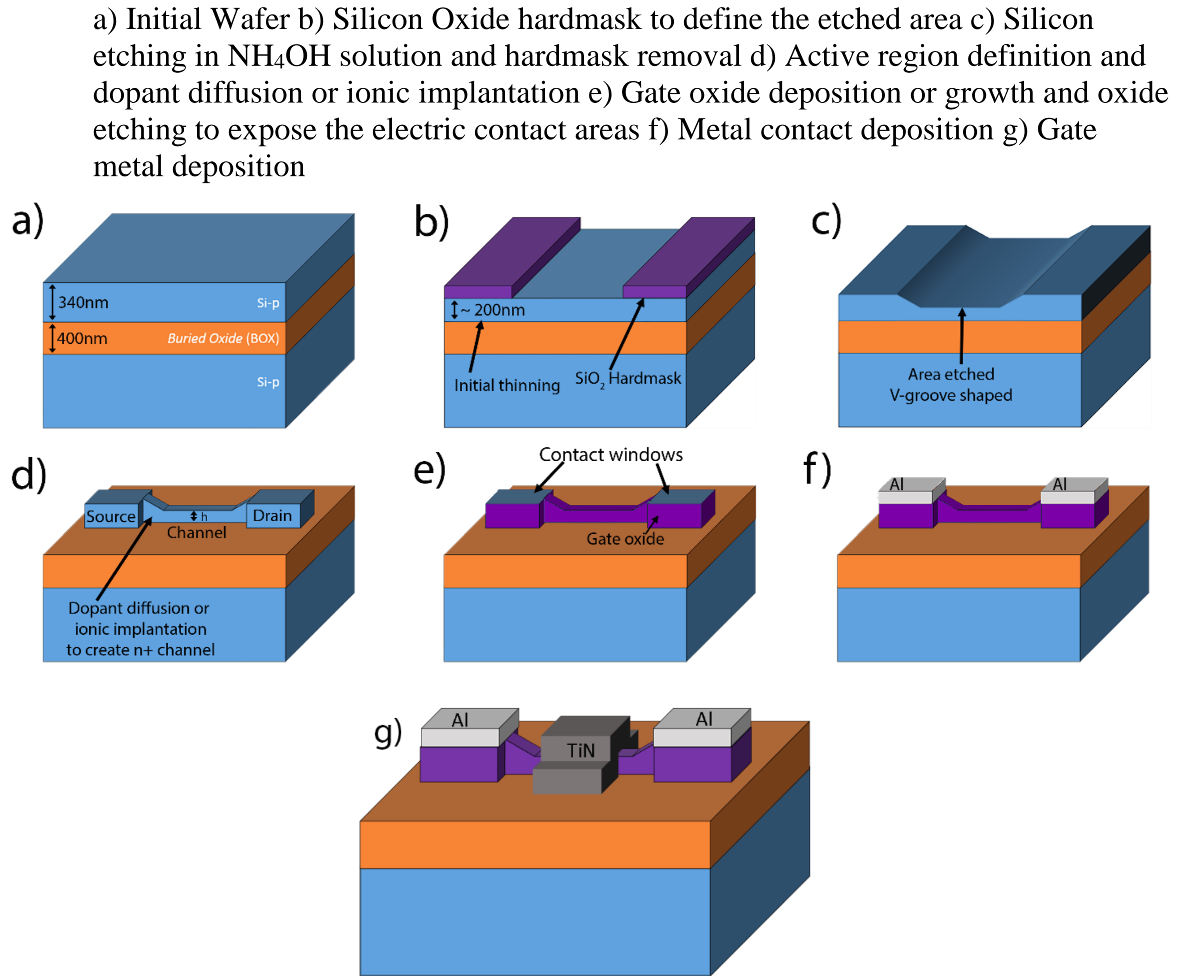
2.9 IN THIS PROJECT

In this project, a technique to fabricate thin devices by anisotropic etching of silicon is proposed. In contrast to (SOARES et al., 2018) efforts to laterally etch a device channel region, the channel is to be thinned down by exposing the top surface of the wafer to NH_4OH solution. The process and resulting structures were presented in section 2.6.

Figure 35 shows a rough outline of the process steps utilized in this project. The fabrication may not follow this specific order, and two different process orders were tested. In both process orders, the same final structures were achieved, although with different dopant concentrations, materials and dimensions.

Figure 35 Simplified process steps of the devices fabricated in this project.

a) Initial Wafer b) Silicon Oxide hardmask to define the etched area c) Silicon etching in NH_4OH solution and hardmask removal d) Active region definition and dopant diffusion or ionic implantation e) Gate oxide deposition or growth and oxide etching to expose the electric contact areas f) Metal contact deposition g) Gate metal deposition



The fabricated structures were characterized mainly by the Pseudo-MOS biasing technique, as used by (PUYDINGER DOS SANTOS et al., 2013) and (SOARES et al., 2018). It was proposed as a wafer-wide characterization procedure in which the backside of a SOI wafer is used as a makeshift gate-stack. By applying the equation 6, it is possible to correlate a number of wafer characteristics. Most notably, knowing the dopant concentration on the channel, NA,D, it is possible to calculate an approximation to the final thickness of the thinned down structure, tSi, shown in equation 7 (CRISTOLOVEANU; MUNTEANU; LIU, 2000). VFB is the flatband voltage of the channel-buried oxide-handling substrate MOS contact, q is the elementary charge, εox is the silicon dioxide absolute permittivity and tox is the buried oxide thickness.

$$V_0 = V_{FB} + \frac{q t_{Si} N_{A,D}}{C_{ox}} \quad \text{Equation 6}$$

$$N_{A,D} = \frac{\varepsilon_{ox}(V_0 - V_{FB})}{q t_{Si} t_{ox}} \quad \text{Equation 7}$$

CHAPTER 3

SIMULATION AND EXPERIMENTAL PROCEDURES

In this chapter, the experimental procedures is presented, starting from the simulations that were used to guide the fabrication steps planning. In the second section, the fabrication steps are also presented, starting from the etching rate characterization performed to obtain an approximated etching rate for the structures to be fabricated. Both the initial process proposed and the updated process obtained after the first set of characterizations are presented with the characterization techniques used to obtain the results presented in chapter 4.

3.1 SIMULATION

Prior to the actual device fabrication, the process flow and electrical characteristics were simulated in a Silvaco Athena and Atlas environments, respectively. The resulting model was then used to evaluate the necessary dimensional and material restrictions and correlate the final structures with effective JL-FET operation.

The fabrication processes were simulated on Silvaco Athena environment using parameters and materials available at CCS/Unicamp. The gate oxide was a 6-nm-thick Silicon Oxynitride and the gate metal work function was set to 4.7 eV, to mimic the electrical parameters of TiN; initially a high dopant concentration was set, 10^{18} atoms/cm^3. The process simulation results are shown in Figure 36 (a), due to scale constraints, the sidewall angle is hard to visualize. Devices of different channel thicknesses, h, were simulated to achieve a fabrication goal.

The simulated devices were then imported into the Silvaco Atlas environment to extract the charge distributions and the electric operation of the devices. The I_D x V_{GS} curves of these devices are shown in Figure 36 (b).

The model obtained was used in every step of the fabrication, first to plan the processes and then to compare simulated and measured results. This saves fabrication cost and time, and enables the testing of alternative parameters and processes.

Figure 36 Simulation results of the JL-FET device

a) Cross-section view of the simulated structure b) I_D x V_{GS} plots of the simulated devices for various channel thickness, h, values.

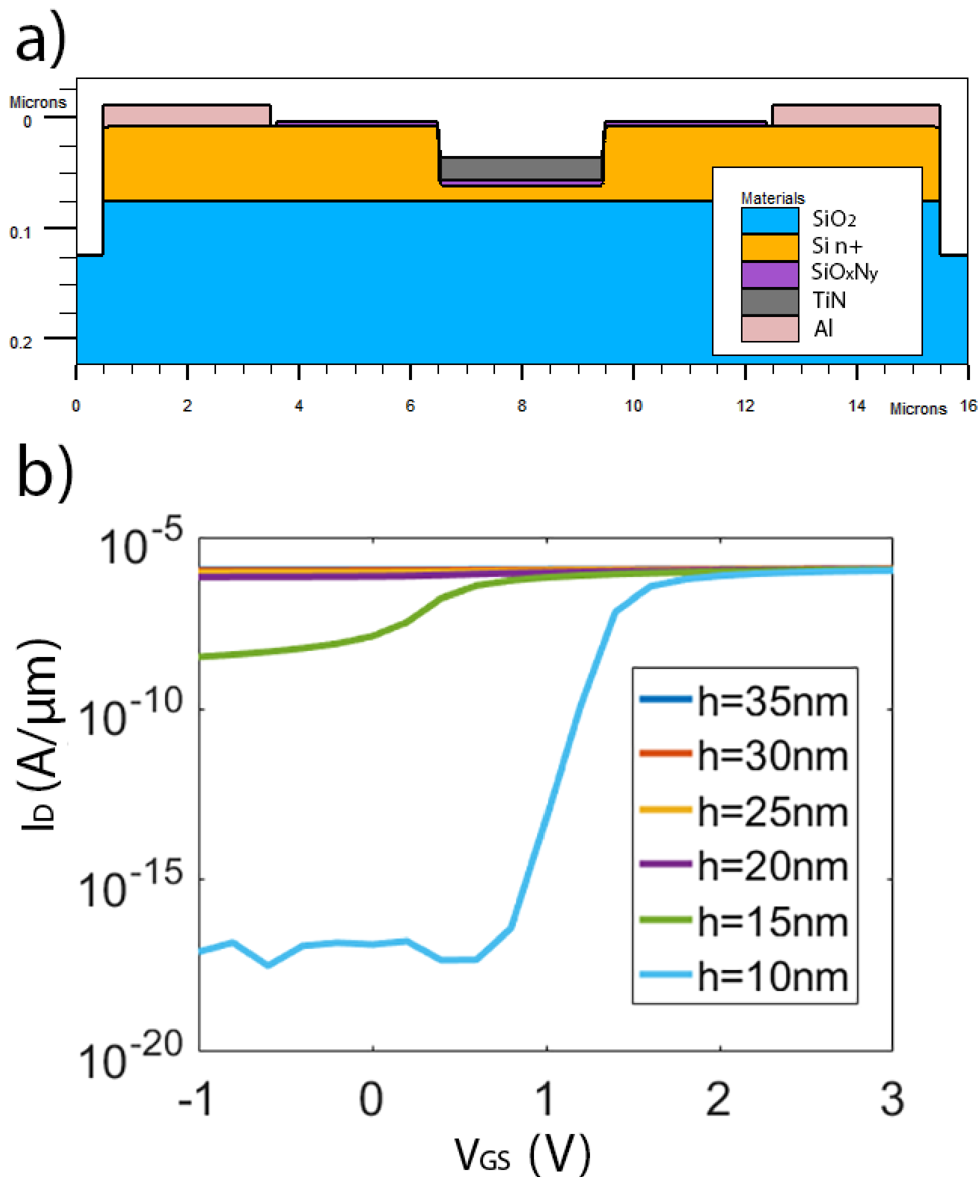


Table 2 shows key characteristic of the simulated transistors that were extracted from the I_D x V_{GS} curves. It is possible to notice that I_{on} is relatively constant, with the variations being accounted by the difference in cross-section area in the channel region. I_{off} on the other hand, presents a slow decline in the 20 to 15 nm thickness range, and a sharp decrease in the 15 to 10 nm thickness range. This happens due to the increased influence of the depletion

region in the charge carriers of the channel region. These effects manifests as a higher V_{TH}, which becomes positive in devices with channels thinner than 15 nm, indicating a normally off device appropriate for digital aplications. The device with 10-nm-thick channel showed excellent transistor behavior with an I_{on}/I_{off} ratio larger than 10^{10}, and presented a subthreshold swing of approximately 60 mV/dec, indicating a suitability for low power VLSI applications. Values that were not indicated could not be determined using the V_{GS} range simulated.

Table 2 Characteristics of the simulated transistor according to the channel thickness

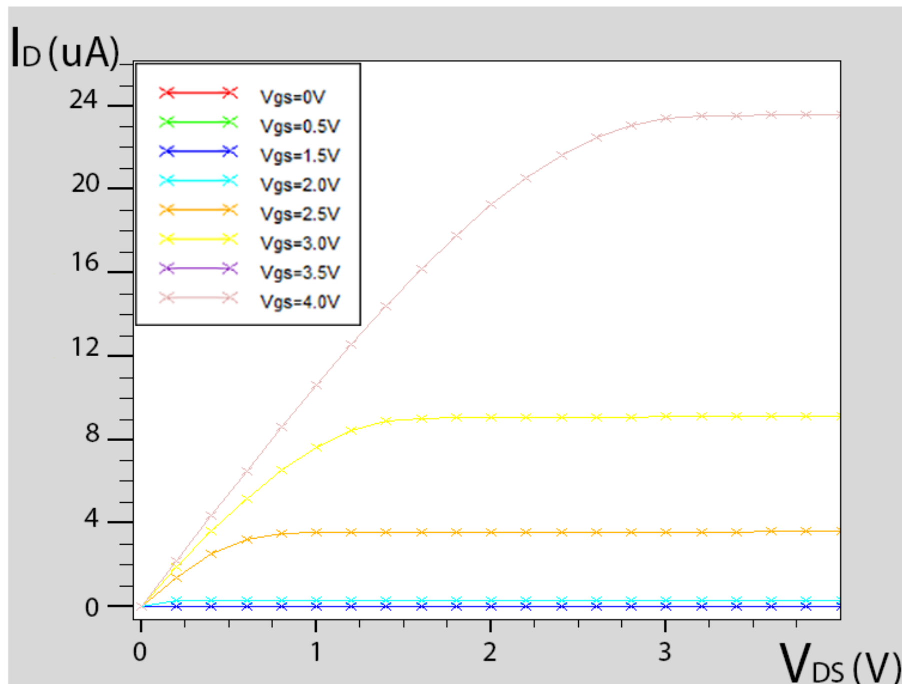
Channel thickness h (nm)	Ion (A)	Ioff(A)	Ion/Ioff	V_{TH} (V)	Subthreshold Slope (mV/dec)
35	1.18×10^{-6}	1.10×10^{-6}	1.07	-	-
30	1.16×10^{-6}	1.05x10-6	1.10	-	-
25	1.13×10^{-6}	9.29×10^{-7}	1.22	-	-
20	1.10×10^{-6}	7.10×10^{-7}	1.55	-2.4	6489.06
15	1.04×10^{-6}	1.31×10^{-8}	79.96	0.2	285.66
10	9.20×10^{-7}	1.38×10^{-17}	6.67×10^{10}	1.3	60.29

The I_D x V_{DS} plot of the 10-nm-thick device is shown in Figure 37. It shows telltale transistor behavior, and clear triode, saturation and cut-off region. This device presents a V_{TH} close to 1 V, corroborated by Figure 36, which allied to the excellent subthreshold swing and I_{on}/I_{off}, makes the JL-FET optimal for low powered digital applications when the critical dimension of 10 nm of channel thickness is achieved. For the 20 nm to 15 nm channel thickness range, the device is appropriate for analog applications, as reported by DORIA et al. (2011).

These simulations results yielded a very clear goal for the final device thickness. By reducing the dopant concentration tenfold, to 10^{17}atoms/cm^3, the depletion width increases approximately three times, as it is inversely proportional to the square root of dopant concentration. This minor modification would make the analog-ready characteristics of the JL-FET apparent in devices that are approximately 60-nm-thick.

Thus, a precise etching rate calibration was needed. A method for obtaining the etching rate was proposed and is presented in section 3.2.

Figure 37 I_D x V_{DS} plot of the simulated device with a channel thickness of 10 nm.



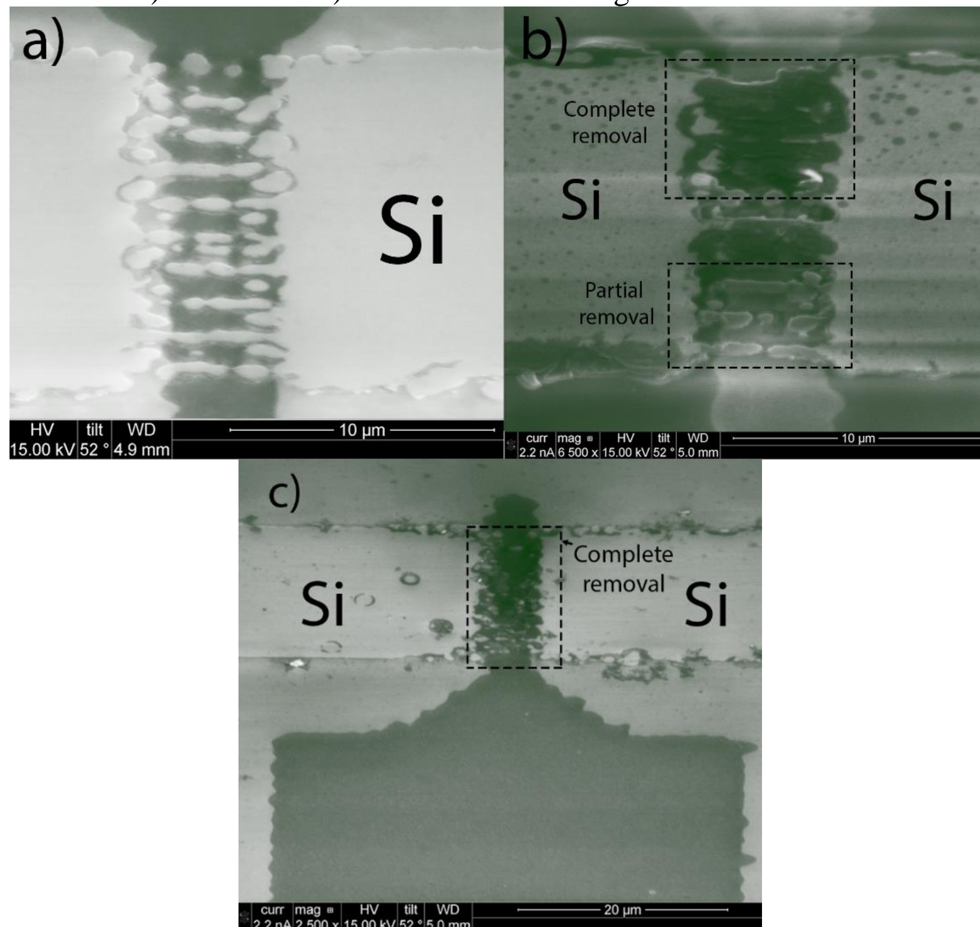
3.2 FABRICATION: ETCHING CALIBRATION

The etching rate of the silicon etching in NH_4OH solution is of utmost importance to the control and reproducibility of the process. Thus, the first few steps of this work was focused on studying the etching rate for the specific structures that will be fabricated. Using the specific structures is required, as the etching rate varies greatly with area exposed to the etching process, the width of the patterned lines, and other characteristics that can affect the reagents and byproducts flowing to and from the exposed areas. One other factor that greatly affects the etching rate and must be taken into account is the dopant concentration. This effect was used profusely to achieve finFETs, and was named Ion-Bombardment Retarded Etching process (MASAHARA et al., 2004).

An initial thinning using wet oxidation and silicon oxide etching in HF solution was performed to reduce the SOI layer to around 200-nm-thick. Ionic implantation of phosphorus and dopant activation in a conventional furnace were performed to achieve a doping concentration of 10^{18} cm^{-3}. A silicon oxide hardmask was deposited using ECR plasma. The gate area was exposed using optical lithography and silicon oxide etching in HF solution. The samples were then etched in NH_4OH solution for 25, 40 and 55 seconds and the resulting structures were analyzed using SEM imaging. Figure 38 shows the structures after etching.

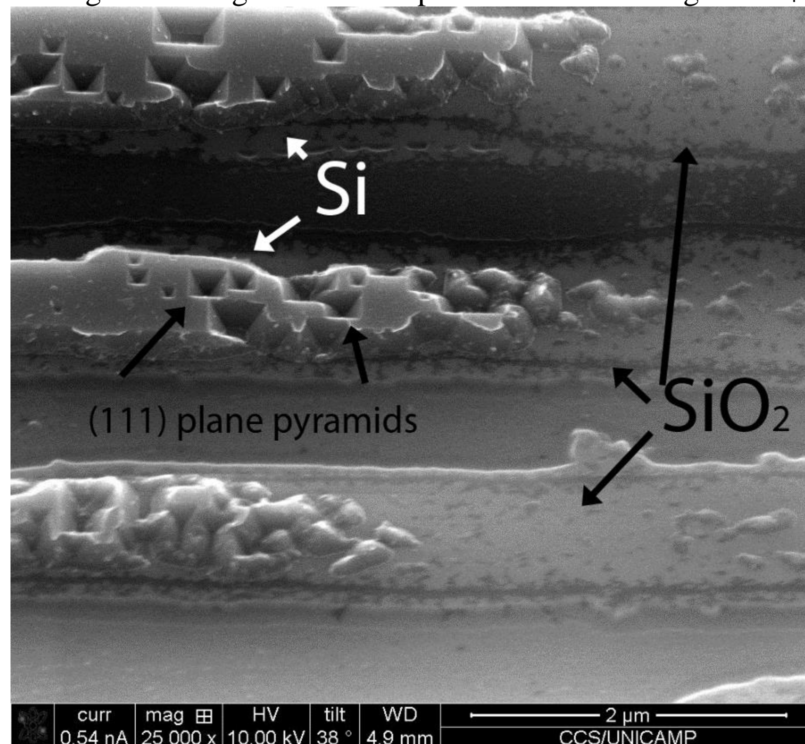
After 25 seconds, there was little etching in the area, at 40 seconds etching time, there was partial etching of the SOI layer, indicating that the etching was at the verge of fully removing it. After 55 seconds, the SOI layer was completely removed and no channel was left present. This indicates that 40 seconds is just enough to etch the 75 nm of the SOI layer for these conditions. An approximation for the etching rate was then calculated, since 75 nm of Si were etched in just about 40 seconds, the etching rate must be at least 1.875 nm/s.

Figure 38 SEM image showing the area etched in NH_4OH solution
a)25 seconds b) 40 seconds c) 55 seconds of etching time.



Additionally, the SEM images of the samples etched for 55 seconds, in 0, showed the characteristic sidewall profile of the anisotropic etching process, in parts pyramids of (111) crystallographic planes are visible. This phenomenon is proposed to be byproduct of the long etching times, as underetching causes unpredictable structures to appear.

Figure 39 SEM images detailing the sidewall profiles of the etching in NH_4OH solution.



With the information obtained in the simulation and etching characterization, all remaining processes were planned.

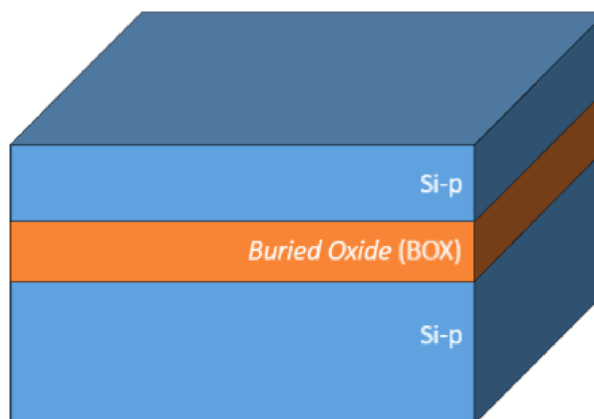
3.3 FABRICATION: FIRST BATCH OF JL-FET DEVICES

The fabrication of the first batch of devices started just after the estimation of the etching rate was obtained.

3.3.1 Initial wafer configuration

The samples were prepared on a 340 nm monocrystalline silicon over a 400 nm silicon dioxide Silicon-On-Insulator (SOI) wafer chips. The top side presents (100) plane orientation and is initially of p-type silicon, with approximately 10^{15} atoms.cm^{-3} of Boron.

Figure 40 Initial wafer configuration



3.3.2 Standard cleaning

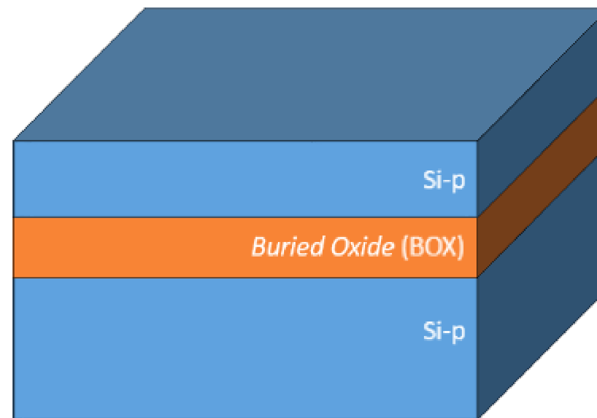
The wafers were cleaned using standard RCA cleaning. This removes every contaminant that may have been introduced during wafer transportation and storage, including organic contaminants from human sources and from the packaging and metallic contaminants from handling tools and other shedding.

3.3.3 Initial thinning

Samples prepared by thinning the superior silicon layer of the SOI sample from 340 nm to approximately 200 nm, by using wet silicon oxidation in a conventional furnace at 1000 for 45 minutes, and oxide etching in HF buffer solution.

The samples were then cleaned using a complete standard RCA cleaning process, to prepare them for the furnace processing.

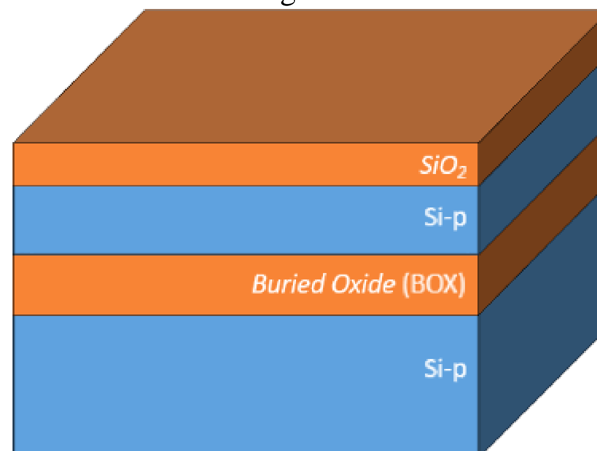
Figure 41 Silicon wafer after initial thinning



3.3.4 Oxide barrier for ionic implantation and ionic implantation

Then, an oxide barrier was grown using dry silicon oxidation at 1000°C in a conventional furnace for 10 minutes. This will be responsible to minimize the damages to the crystallographic structure of the silicon caused by the high energy ion bombardment in the ionic implantation step. Ionic implantation of phosphorus (^{31}P) was performed, with a dose of 6.10^{15} atoms.cm^{-2}, to achieve a N-Type doped silicon channel.

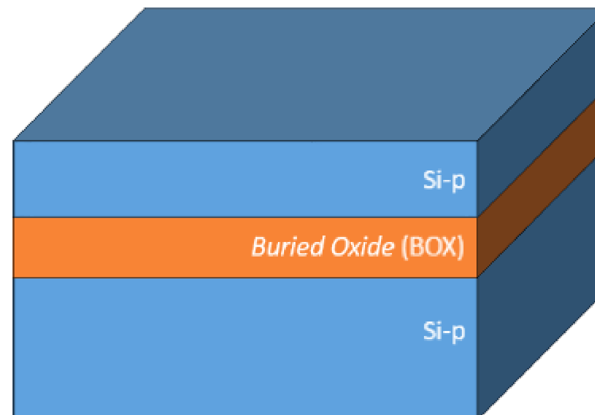
Figure 42 Silicon wafer after oxide barrier growth



3.3.5 Standard Cleaning and oxide etching

The samples were cleaned with a complete standard cleaning process. During the cleaning process, the HF etching step was extended to remove the oxide barrier used in the ionic implantation step.

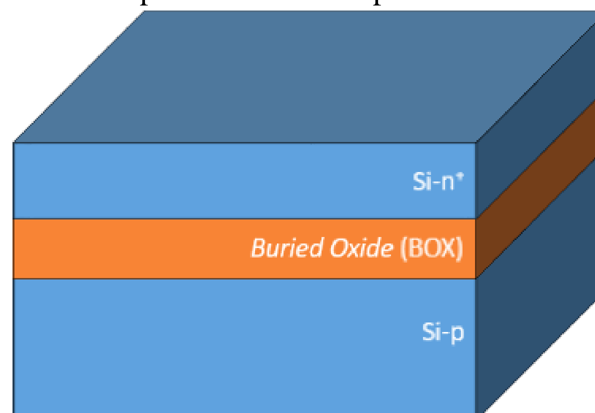
Figure 43 Silicon wafer after ionic implantation and oxide etching



3.3.6 Dopant activation and crystal structure reconstruction

The structure was annealed in a conventional furnace for 30 minutes at 1000°C in an inert environment (N_2) to activate the dopant impurities and to reform the crystallographic structure of the silicon, damaged by the ionic implantation.

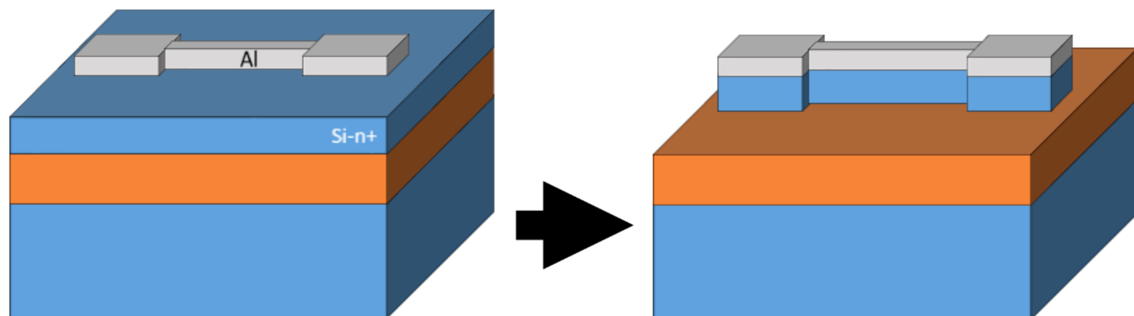
Figure 44 Silicon wafer after dopant activation step



3.3.7 Active Region definition

Sputtered aluminum defined using photolithography and lift-off was used to fabricate an aluminum hardmask for the active region etching. The first process described in section 2.5 was used. The active region was then defined through ICP-RIE SF_6 plasma etching. The devices present 10 parallel fins, each 1-µm-wide.

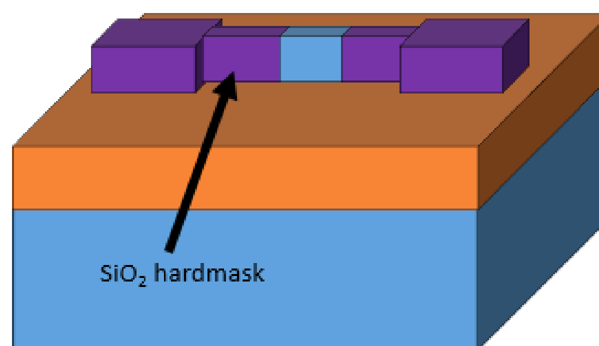
Figure 45 Silicon wafer after hardmask definition and after active region etching in ICP-RIE



3.3.8 Oxide hardmask deposition and definition

The aluminum hardmask was removed using a solution of HNO_3 and H_3PO_4 and a silicon oxide layer was grown using O_2 ECR plasma. The area to be exposed to the silicon etching in NH_4OH solution was defined using lithography and the oxide was etched in HF solution. The first process described in section 2.5 was used. This mask defines the transferred lengths of the devices, which presented transferred lengths of 1 µm and 10 µm.

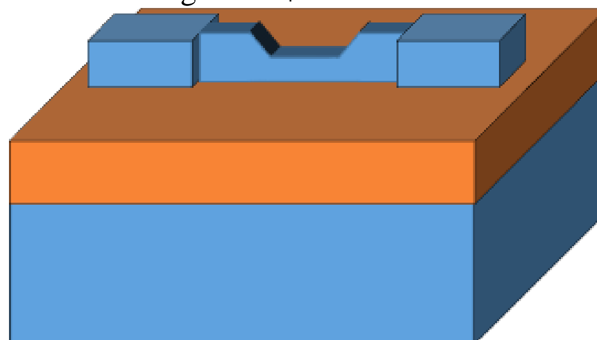
Figure 46 Silicon wafer after oxide hardmask deposition and definition



3.3.9 Silicon etching in NH_4OH solution

The samples were then exposed to the NH_4OH solution at 75°C for 40 seconds.

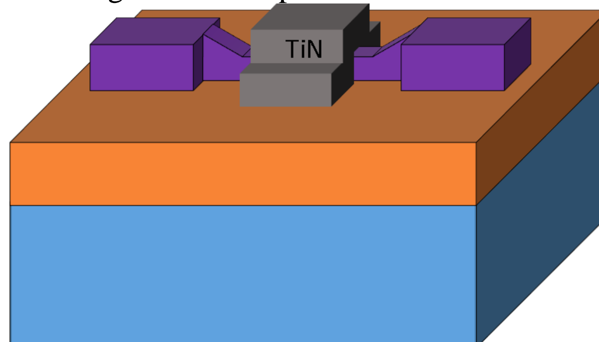
Figure 47 Silicon wafer after etching in NH_4OH solution and hardmask removal



3.3.10 Gate oxide deposition and gate metal deposition and definition

The gate insulator was Silicon Oxynitride grown using O_2/N_2ECR plasma. The gate metal was Titanium Nitride (TiN) deposited using reactive sputtering and defined using photolithography and lift-off. The first process described in section 2.5 was used.

Figure 48 Silicon wafer after gate metal deposition

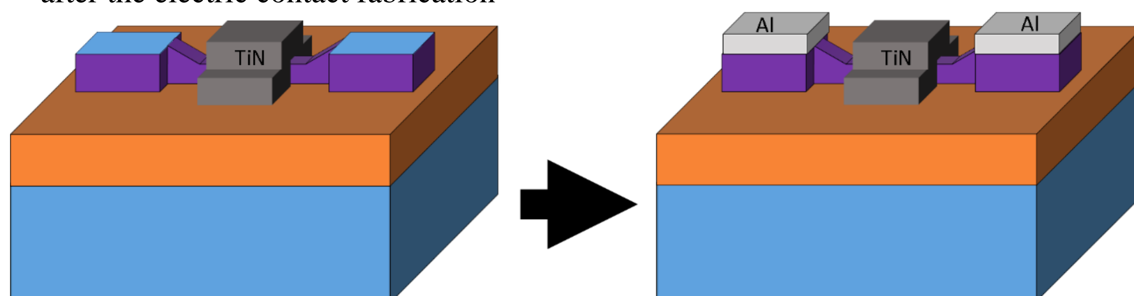


3.3.11 Electric contacts metallization and definition and final annealing

The electric contacts were fabricated using sputtered aluminum, patterned using photolithography and lift-off, and annealed in a conventional furnace in 5 minutes steps at 450°C

in 92% N_2 and 8% H_2 environment. The devices were measured electrically after every annealing step, and the best results were those measured after a total of 20 minutes of annealing. The second process described in section 2.5 was used.

Figure 49 Silicon wafer after HF solution oxide etching to open electric contact area and after the electric contact fabrication



3.4 FABRICATION: SECOND BATCH OF JL-FET DEVICES

The second batch of devices was fabricated using an updated process. Most of the process flow is identical to the first process, with main divergences being in the usage of dopant diffusion to achieve the channel doping. The dopant diffusion process is ideal for JL-FET devices, as it is a much less damaging process to the silicon crystallographic structure when compared to the ionic implantation. Other divergences were: switching the silicon etching in NH_4OH solution to the start of the fabrication and switching the gate metal and the metal contact fabrication orders.

By performing the etching in NH_4OH solution at the end of the process, two advantages arise: the etching rate becomes the same for both pMOS and nMOS devices, as it is performed with the dopant concentration indicated by the wafer manufacturer and by not performing the initial thinning, the etching time is longer, allowing a better process control.

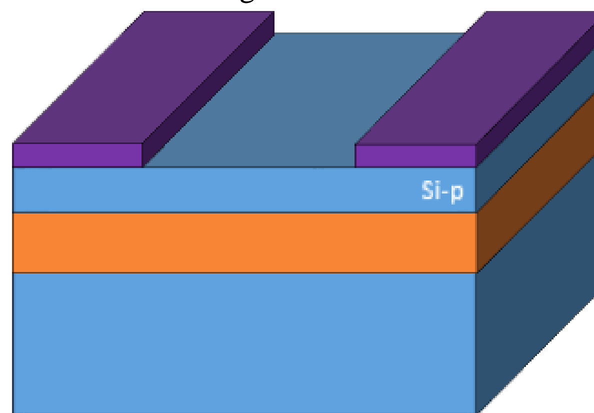
The metal deposition sequence was altered to enable mid-fabrication electrical characterization using pseudo-MOS measurements. As soon as the electric contacts are fabricated, it is possible to perform measurements using the backside MOS stack and to measure the quality of the fabricated device before the final gate fabrication. This could be a big advantage, as provides informations that could affect gate oxide and metallization processes.

At the end of the fabrication, the structures obtained are the same as in the original process. The following sections indicate the divergences in process and parameters when compared to the original process.

3.4.1 Oxide hardmask growth and definition

After the initial cleaning, following the original process until section 3.3.2. The samples went through thermal oxidation to create a silicon dioxide layer that was patterned and used as a hardmask for the NH_4OH solution silicon etching. The patterning was performed using optical lithography, and the oxide etching was performed using a HF buffer solution. The first process described in section 2.5 was used.

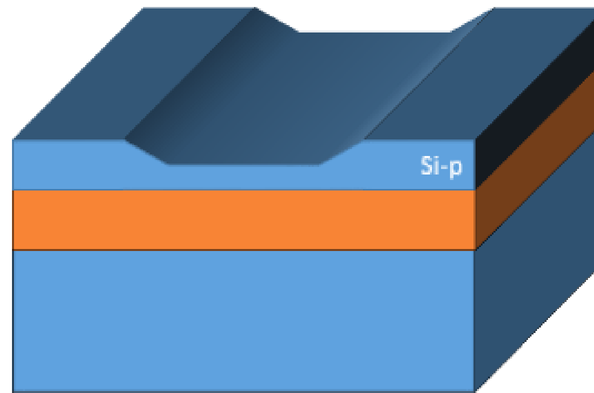
Figure 50 Silicon wafer after hardmask growth and definition for the updated process



3.4.2 Silicon etching in NH_4OH solution

The NH_4OH solution silicon wet etching then took place: one sample was etched for 50 s, one was etched for 60 s and one was etched for 80 s. Two samples were left unetched to better evaluate the effects of the channel thinning on JL-FET operation.

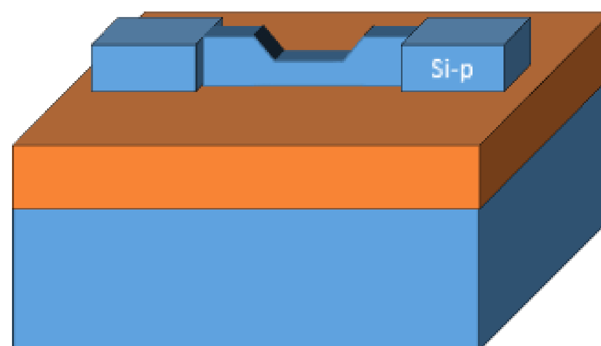
Figure 51 Silicon wafer after etching and hardmask removal for the updated process



3.4.3 Active Regionde finition

An aluminum hardmask for the active region definition was deposited using sputtering and patterned using optical lithography and lift-off. The first process described in section 2.5 was used. The MESA structures were then defined by silicon etching in SF_6 ICP-RIE plasma.

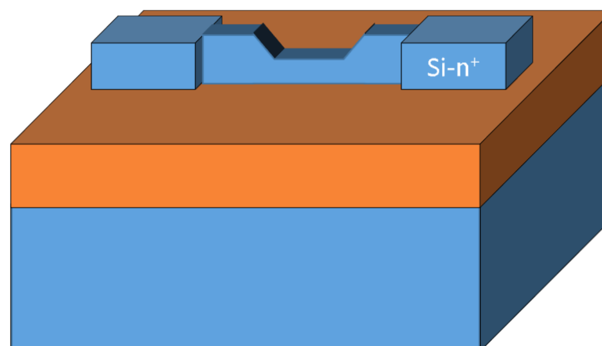
Figure 52 Silicon wafer active region definition for the updated process



3.4.4 Dopant diffusion

The channel doping was achieved using Phosphorus diffusion in a conventional furnace. The substrate superficial doping concentration was measured after the diffusion process using a 4-point probe at around 10^{19} atoms.cm^{-3}, enough to maintain ohmic electrical contacts (VILMS, 1969).

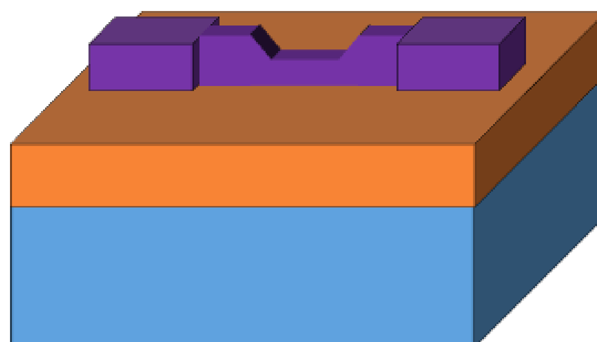
Figure 53 Silicon wafer after dopant diffusion for the updated process



3.4.5 Gate dielectric growth

The gate dielectric was grown using silicon thermal oxidation in dry O_2 environment for one minute and annealed for oxide densification for 10 minutes in inert gas (N_2).

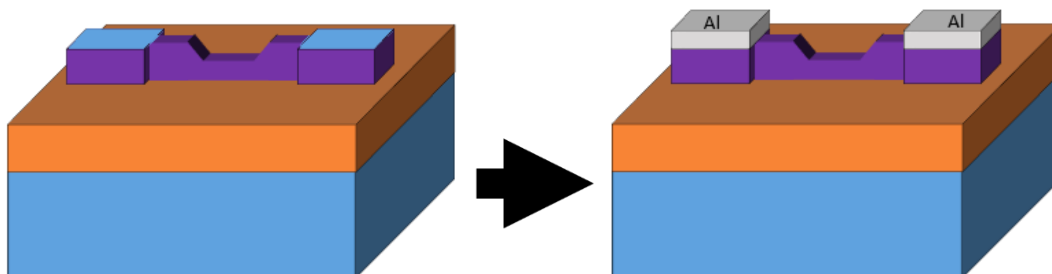
Figure 54 Silicon wafer after gate dielectric growth for the updated process



3.4.6 Metal contacts patterning, fabrication and initial annealing

The metal contacts were fabricated using aluminum deposited by sputtering, and defined by lift-off technique. The second process described in section 2.5 was used. Before the aluminum deposition, a dip in HF solution was used to remove the silicon oxide in the electrical contact area. The electrical contacts were annealed for 10 minutes at 450°C in 92% N_2 and 8% H_2 environment.

Figure 55 Silicon wafer after HF solution oxide etching to open electric contact area and after the electric contact fabrication for the updated process.



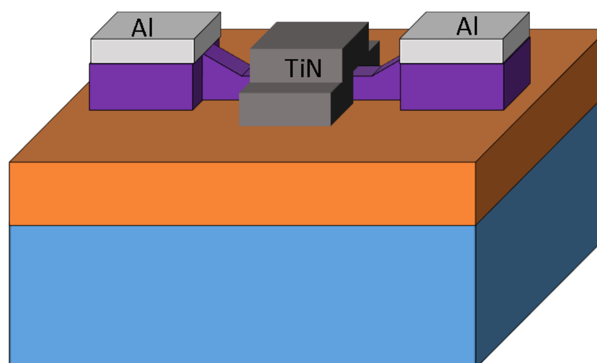
3.4.7 Pseudo-MOS channel characterization

Electrical measurements were carried out to evaluate the contact quality and the properties of the resulting silicon channel, using pseudo-MOS biasing, in which the backside of the SOI wafer is used as a gate stack. This is one of the novelties of the updated process; it is usable as a quick and accessible way to evaluate the resulting structures before the final gate fabrication. This saves fabrication costs and time, as it facilitates the detection and binning of defective devices that would only be possible after the fabrication is complete. These advantages are especially useful when state of the art processes such as selective ALD are used in the gate metal fabrication, or even for oxide fabrication with some modifications to process flow.

3.4.8 Gate metal patterning, fabrication and final annealing

The gate metal was then deposited using reactive sputtering. The material used was once again TiN. The gate metal patterning was performed using photolithography and the lift-off technique. The first process described in section 2.5 was used.

Figure 56 Silicon wafer gate metal fabrication for the updated process



3.5 CHARACTERIZATION

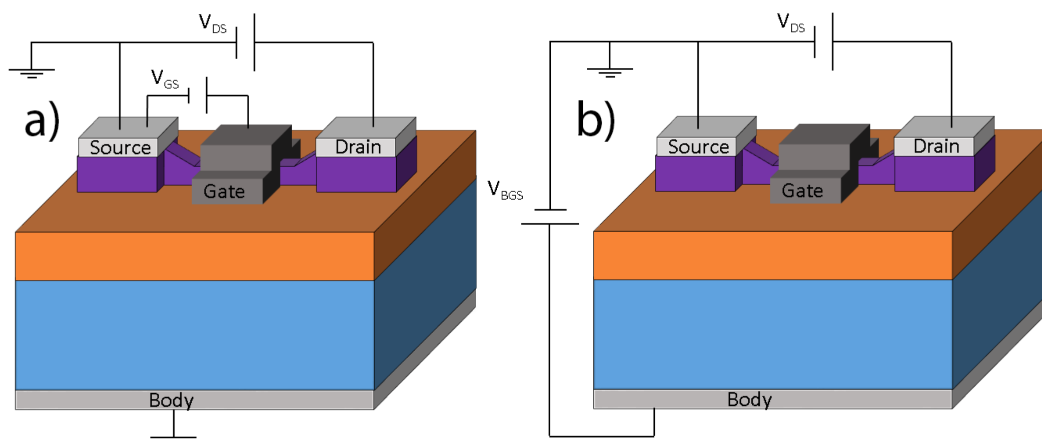
Throughout the fabrication process, optical microscopy was used as a characterization technique to evaluate process such as metal deposition, patterning and lift-off.

To observe the fabricated structures in detail, cross-section SEM images were performed in a FIB-SEM system. The cross-section images consists of, after depositing a protective platinum layer, milling the structure to expose a cross-section of the device.

The devices were then characterized electrically in a Keithley Semiconconductor Analysis system Model 4200. I_D x V_{DS} and I_D x V_{GS} curves were obtained for the junctionless-FET biasing, shown in Figure 57 (a) , and I_D x V_{BGS} curves were also measure in the pseudo-MOS biasing, shown in Figure 57 (b), to evaluate key channel characteristics such as doping concentration. As the gate contact is not connected in the Pseudo-MOS biasing, this measurement can be performed with or without the presence of a gate stack. Pseudo-MOS characterization steps carried out during the fabrication were indicated in section 3.4 whenever used.

Figure 57 JL-FET and Pseudo-MOS biasing schematics

a) JL-FET biasing, body shorted to the source to eliminate body-effects. b) Pseudo-MOS biasing.



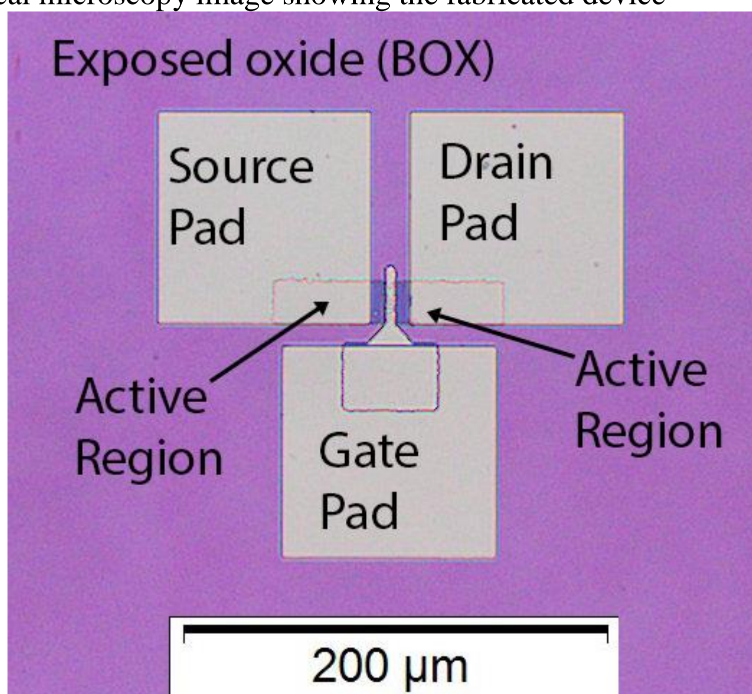
CHAPTER 4

RESULTS AND DISCUSSION

4.1 ORIGINAL PROCESS

The devices fabricated in the first batch were structurally characterized using a number of techniques, starting from optical microscopy imaging. Figure 58 shows an optical microscopy image of the fabricated device.

Figure 58 Optical microscopy image showing the fabricated device



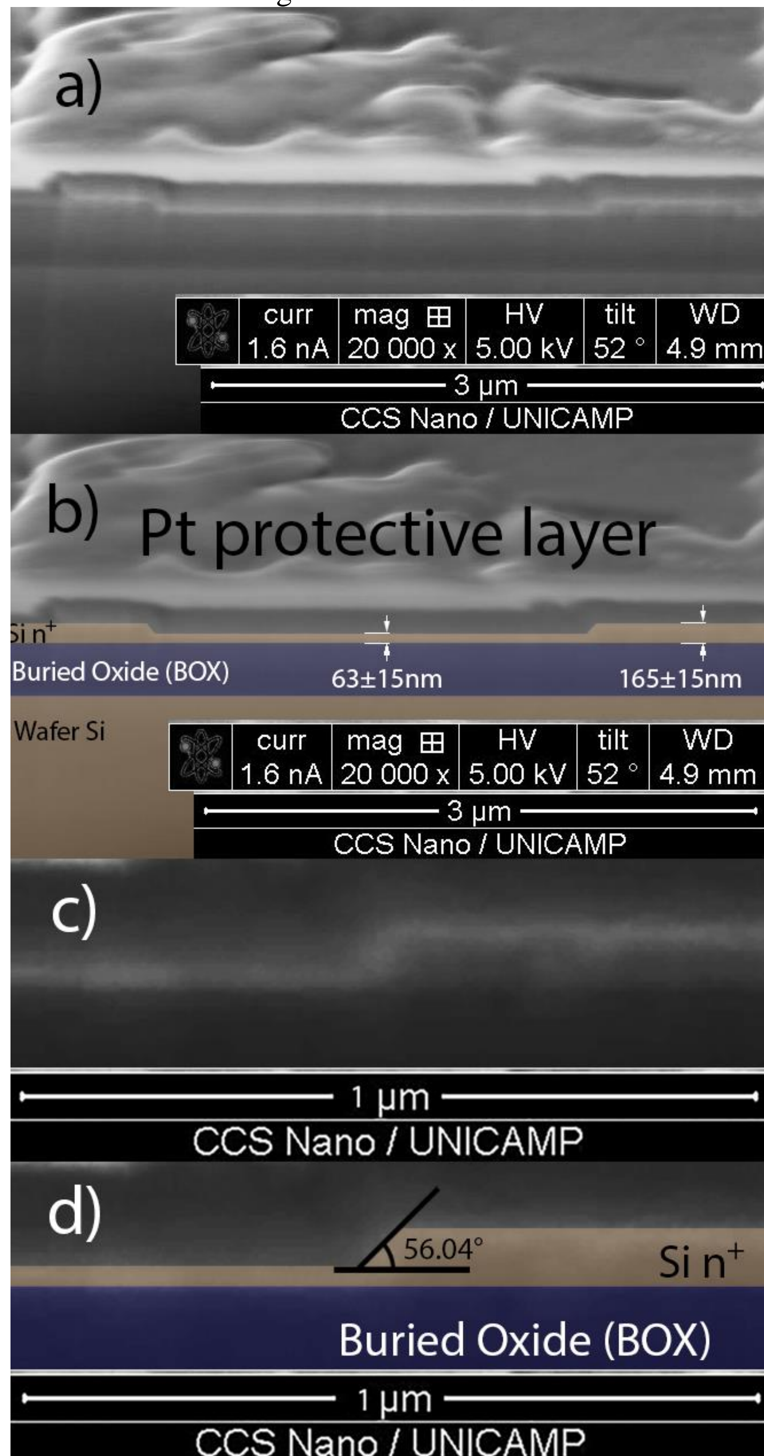
Then, cross-section SEM imaging performed in a FIB/SEM system. Platinum was deposited using a Gas-Injection-System, both by electron beam assisted deposition and by gallium ion beam assisted deposition. A FIB milling process was used to expose and polish the cross-section for SEM observation. These images, shown in Figure 59showed the expected shapes for the anisotropic etching, characteristic of the NH_4OH solution wet etching.

Figure 59 (a) and (b), where a colored overlay was added for better understanding, show the cross-section view of the etched area, where the thickness of the initial SOI layer

and of the thinned-down channel region were measured. The initial top layer of silicon thickness was approximately 165 nm, this is within the expected range after the top layer of silicon were thinned down to 200 nm using wet oxidation, and then several processes that consumed the layer, such as silicon oxidation and oxynitridation in ECR plasma. In the area exposed to the etching process, the silicon layer was thinned to 63 nm, with no noticeable effect on the surface roughness. This result indicates a success in fabricating devices for analog applications, as according to the numerical simulations carried out, the current modulation properties of the JL-FET device starts to take place at approximately 60 nm for the dopant concentration of 10^{17} planned for the device.

To confirm that the thinning was indeed result of the anisotropic etching of silicon, the sidewall profile was analyzed in detail, as shown in Figure 59 (c) and (d), where a colored overlay was added for better understanding. The angle of the sidewalls was measured at approximately 56 degrees, which is remarkably close to the characteristic angle between the (111) and (100) family of crystallographic planes in silicon, 54.74 degrees. The rounding in the meeting of the walls, such as reported by (MIGITA et al., 2014) and explained by the formation of meta-stable (311) planes in silicon (SHIKIDA et al., 2002) were also observed.

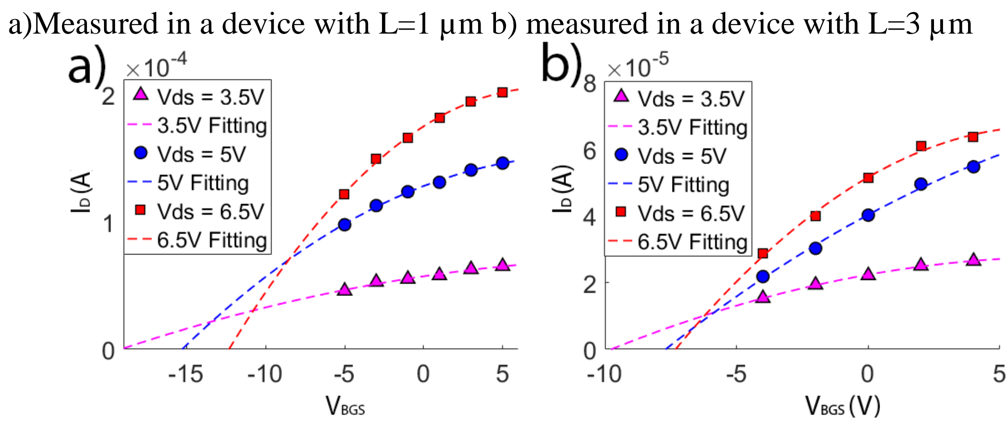
Figure 59 Cross-section SEM images of the device fabricated using the original process a) Sidecut of the channel region b) colored overlay added shows materials and measurements c) Closer view of the sidewall of the etched area d) colored overlay shows materials and measured angle of the sidewall.



$I_D x V_{BGS}$ curves biased in pseudo-MOS, $I_D x V_{DS}$ and $I_D x V_{GS}$ using JL-FET biasing were measured, according to the schematics in 0.

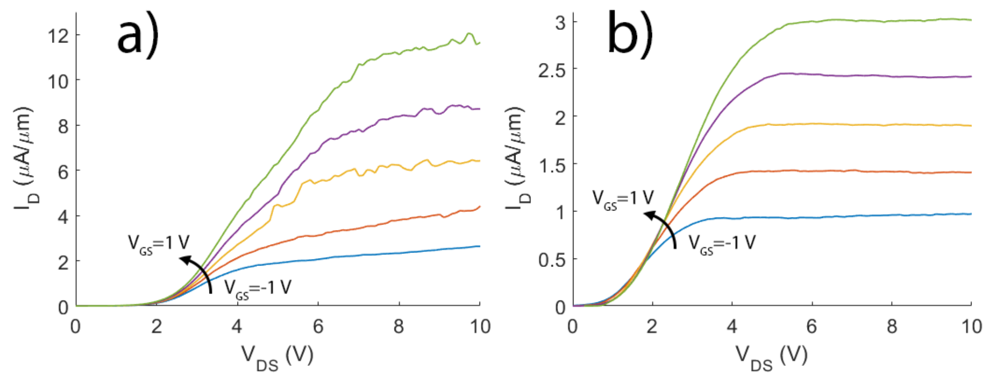
$I_D x V_{BGS}$ pseudo-MOS measurements of the fabricated devices were carried out to confirm the presence of a silicon channel after the anisotropic silicon etching process. These curves are shown in. It is noticeable that the pseudo-gate-stack formed by the backside of the substrate has a good control on the current, indicating the presence of a good quality silicon channel. It is possible to plot a second order fitting of the curves, and extrapolate to a theoretical voltage V_0 that would be enough to deplete every charge carrier in the channel. With this V_0 and the equation 2 showed in the section 2, it is possible to calculate an approximation for the dopant concentration on the channel. By using a V_0 that ranges from -7 V to -20 V the final calculated concentration was around 10^{16} to10^{17} atoms.cm^{-3}, which is within the expected ranges determined in the process planning.

Figure 60 I_D xV_{BGS} plots for the pseudo-MOS device fabricated using the original process a)Measured in a device with L=1 μm b) measured in a device with L=3 μm



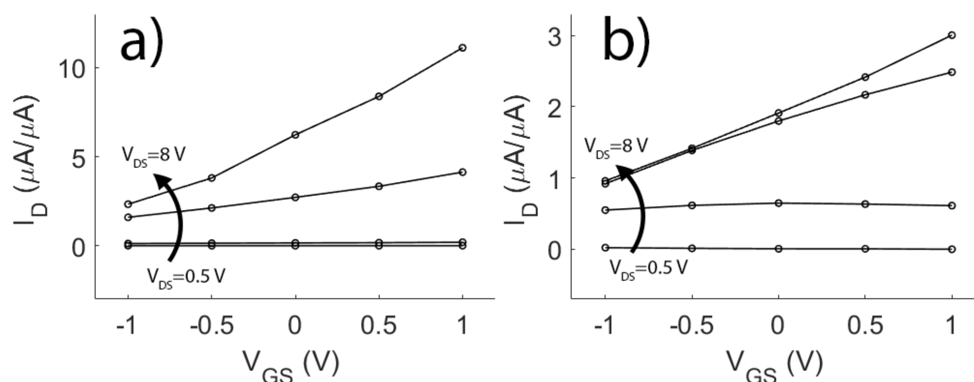
$I_D x V_{DS}$ measurements were also carried out and showed the expected behavior for the devices. The gate voltage had a good control on current magnitude, and the drain current showed clearly distinguished triode and saturation operation. With a device thickness of approximately 65 nm, the gate-stack influence on the charge carriers present in the channel is not wide enough to cause the complete depletion, and thus the cut-off operation mode. Because the dopant concentration on the source and drain regions was relatively low, around 10^{17} atoms.cm^{-3}, the electrical contacts shows a non-ohmic behavior, as expected from the information in the literature (SCHWARTZ, 1969).

Figure 61 I_D xV_{DS} plots for the JL-FET device fabricated using the original process a)Measured in a device with L=1 µm b) measured in a device with L=3 µm



0 shows the I_D x V_{GS} plots of the fabricated devices. Then extracted I_{on} and I_{off} characteristics are shown in Table 3. In both the 1-µm-long and the 3-µm-long devices, the I_{on}/I_{off} ratios present distortions in the values measured using 0.5 V and 2 V of drain voltage, due to the presence of the Schottky electrical contacts. For the measurements performed using 4 V and 8 V of drain voltage, an I_{on}/I_{off} ratio of 1.38 to 1.78 was observed. This value can be compared to the simulated device presented in section 3.1. The fabricated device, that presents a channel thickness of 64 nm, presents similar characteristics to the simulated device with gate thickness of 20 nm, both present a I_{on}/I_{off} ratio of approximately 1.5, according to Table 2 and Table 3. This is an expected result, since the dopant concentration in the fabricated device is approximately 10 times lower than in the simulated device, the characteristics presented would be equivalent of a device 3 times thinner, due to the inverse dependence of the depletion region width to the square root of the dopant concentration.

Figure 62 I_D xV_{GS} plots for the JL-FET device fabricated using the original process a)Measured in a device with L=1 µm b) measured in a device with L=3 µm. Plotted for V_{DS} values of 0.5 V, 2 V, 4 V and 8 V.



By introducing the obtained parameters in the simulation model, a 63-nm-thick device with a dopant concentration of $8*10^{17}$ atoms.cm^{-3} was obtained as the best fit for the results observed. The Schottky barrier observed, of about 1 V, was also simulated. Due to convergence issues, the series resistance introduced by the measuring setup could not be simulated, leading to an increased apparent current. The I_D x V_{DS} plots of these devices are presented in Figure 63. The simulations confirm the behavior of the fabricated structures, showing that the models obtained are congruent to the structures fabricated.

Figure 63 I_D xV_{DS} plots for the JL-FET device simulated
a)Device with L=1 µm b) Device with L=3 µm

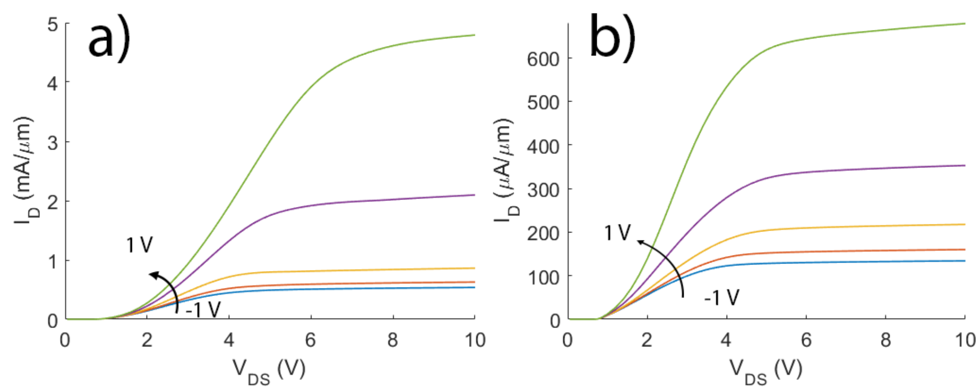


Table 4 shows the I_{on} and I_{off} characteristics obtained for the devices simulated using the parameters extracted. The values of the I_{on}/I_{off} ratio show similar trends to those extracted from the fabricated transistors and presented in Table 3. I_{on} values on the simulated device are slightly higher to those observed in the fabricated transistor, causing some distortion on the I_{on}/I_{off} ratio, this is likely due to the absence of the series resistance, which could not be simulated due to convergence restraints imposed by the simulating software.

Table 3: I_{on} and I_{off} characteristics for the fabricated devices.

Channel length	V_{DS}	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}
L=1 µm	0.5 V	503 pA	914 pA	0.[illegible]
	2 V	0.19 µA	0.15 µA	1.[illegible]
	4 V	4.12 µA	2.71 µA	1.[illegible]
	8 V	11.1 µA	6.22 µA	1.[illegible]
L=3 µm	0.5 V	38.9 pA	6.73 nA	5.78x1[illegible]
	2 V	0.61 µA	0.64 µA	0.[illegible]
	4 V	2.48 µA	1.79 µA	1.[illegible]
	8 V	3.00 µA	1.91 µA	1.[illegible]

Table 4: I_{on} and I_{off} characteristics for the simulated devices.

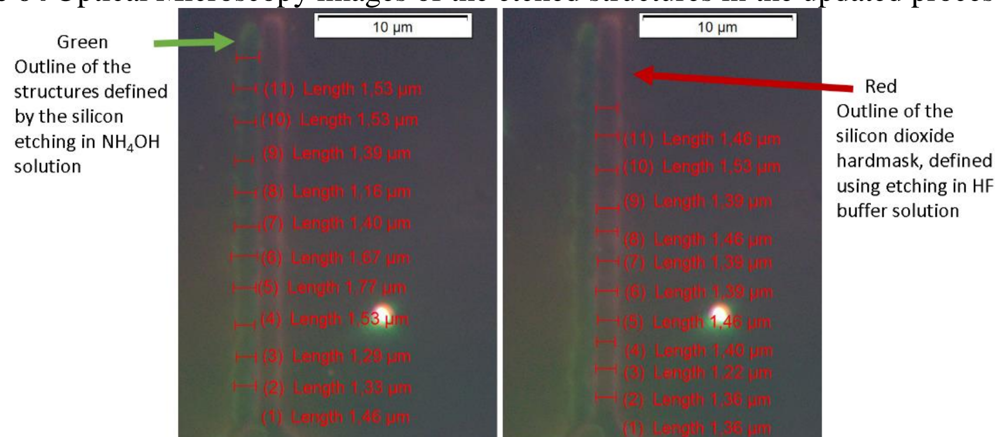
Channel length	V_{DS}	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}
L=1µm	0.5 V	8.95 fA	8.99 fA	1.00
	2 V	0.22 µA	0.17 µA	1.28
	4 V	1.32 µA	0.71 µA	1.85
	8 V	2.01 µA	0.83 µA	2.41
L=3µm	0.5 V	8.95 fA	8.99 fA	0.99
	2 V	92.2 µA	66.7 µA	1.38
	4 V	279. µA	182. µA	1.53
	8 V	346. µA	214. µA	1.62

4.2 UPDATED PROCESS

4.2.1 Optical Microscopy process confirmation

In the updated process, some results are readily available such as the confirmation of the etching process using optical microscopy and dark field filter, shown in Figure 64. It is possible to see both the red-tinted outline, that corresponds to the pattern etched in the SiO_2 hardmask, and the green-tinted outline that is the final etched structure in the silicon.

Figure 64 Optical Microscopy images of the etched structures in the updated process

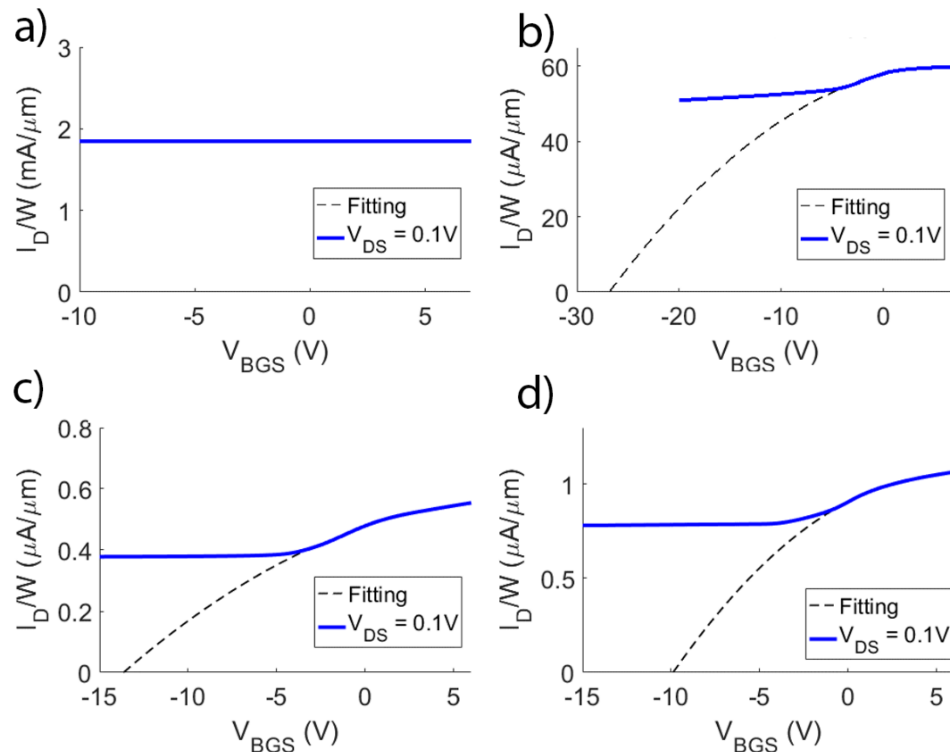


4.2.2 Pseudo-MOS measurements prior to gate fabrication

Electrical measurements in Pseudo-MOS biasing were carried out, and are shown in Figure 65. As expected, the current modulation from the gate voltage is very poor for the unetched sample. In the etched samples, the evolution of the current modulation is noticeable as the etching time increases. In the I_D x V_{BGS} Pseudo-MOS measurements, this is exemplified by the increasing V_0 that would be theoretically needed to deplete every charge carrier in the channel. In the I_D x V_{DS} measurements, this behavior is seen in the bigger gap between current curves for each given gate voltage. It is also noticeable that, as opposed to what would be expected for a device with thinner channel, the sample etched for 80 seconds has a higher current flowing through the device for any given biasing condition. This behavior indicates either that a larger dopant concentration was achieved in thinner layers, or that

there is smaller number of fins in operation, indicating that some may have been damaged during the device processing

Figure 65 I_D x V_{BGS} pseudo-MOS measurements for each sample prior to gate fabrication a) Unetched control sample b) Sample etched for 50 s c) Sample etched for 60 s d) Sample etched for 80 s



Using the V_0 obtained when measuring each sample, a fitting of the V_0 behavior according to etching time was proposed, shown in equation 8, apart from the measured results, a calculated theoretical V_0 for the unetched sample was included, as a -555 V for 0 s etching time. The exponential fitting was chosen as it fits better the expected behavior of the etching process, at the start a lot of reagents are present at the surface, which results in a faster etching rate, as the time progresses, the gas byproducts affects the renewal of reagents and slow the etching rate. This results in a chaotic start with a very fast etching rate, followed by a part with slower etching rate. Analysis of the sum of the squares of the residuals, showed that both linear and quadratic fittings are not optimal. Third and fourth order polynomial fittings present a behavior not compatible with the expected of this functions, with local minimums or points of inflection in between the experimental points. Equation 8 was plotted in Figure 66; the calculated V_0 for the unetched sample was omitted.

It is important to notice that the parameters obtained are valid only for this specific process, and will be used in further fabrication efforts.

$$V_0 = 0.73 - 4.528 * e^{-0.06(t-80)}$$ Equation 8

Figure 66 V_0 x etching time measurements and fitting for the fabricated samples

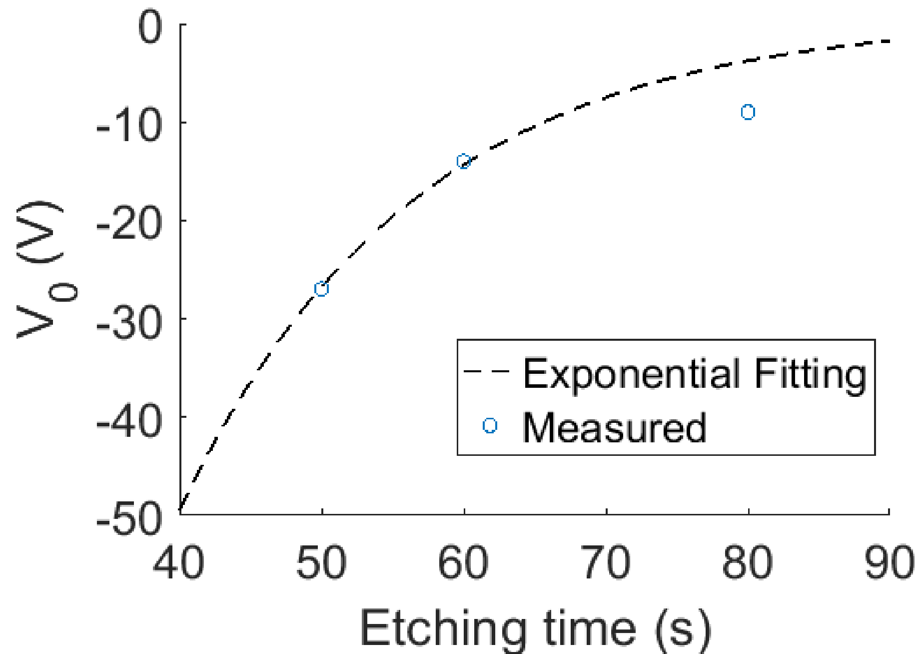


Table 5 Sum of the square of the residuals for each fitting curve

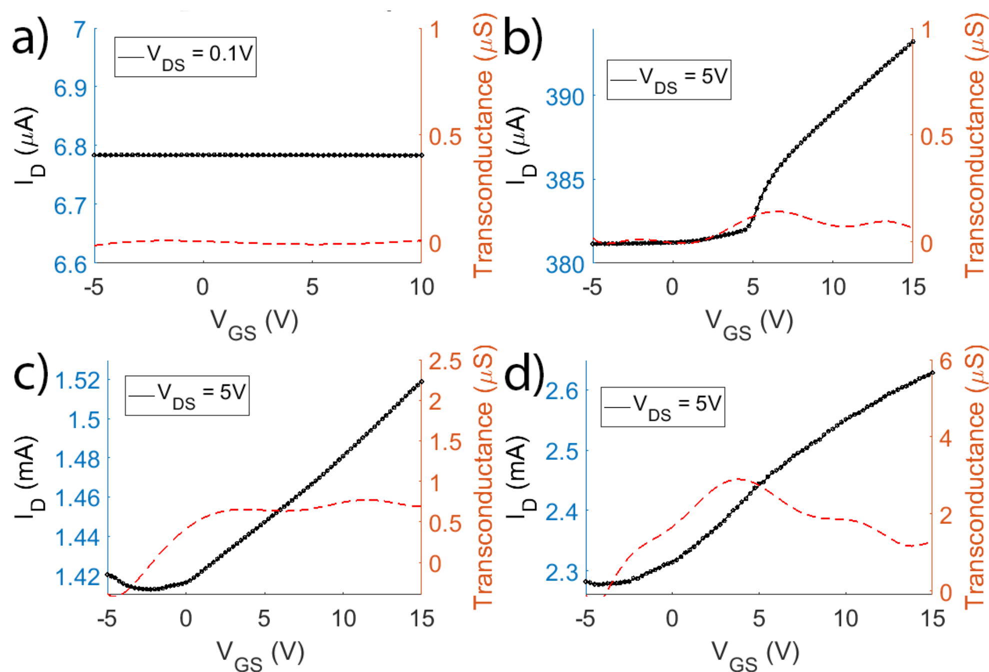
Fitting	Sums of the squares of the residuals	Comment
Linear	$2.5*10^4$	
Quadratic	188.43	
3rd order	$1.22*10^{-24}$	Point of inflection at t≈80 s, incompatible with the etching behaviour
4th order	$4.76*10^{-24}$	Local minimum at t≈75 s, incompatible with the etching behaviour
Exponential	27.26	

4.2.3 JL-FET biasing measurements in the completed devices

After completing the device fabrication, the I_D x V_{GS} measurements were plotted in Figure 67, with the calculated transconductance plotted in the right axis. The distinguishing feature of the unetched sample is the flat I_D x V_{GS} which results in a transconductance close to 0 S. This happens due to the SOI layer being much thicker than the depletion region created by the gate stack, therefore the electrical biasing has little to no effect on the drain current. The behavior of decreasing current magnitude as the etching time increases, observed in the Pseudo-MOS measurements, continues.

As the etching time increases, it is possible to observe curves where the gate biasing has a greater effect on the drain current. This is the expected effect of the longer etching times on the devices, as a thinner SOI layer means that the width of the depletion layer introduced by gate biasing is more expressive. The increase in gate control is mostly seen in the peak transconductance, as it increases from approximately 0.1 µS for the sample etched for 50 s, to approximately 1µS in the sample etched for 60 s, to approximately 3 µS for the sample etched for 80 s.

Figure 67 I_D x V_{GS} JL-FET measurements for each sample after complete fabrication a) Unetched control sample b) Sample etched for 50 s c) Sample etched for 60 s d) Sample etched for 80 s. V_{DS} is indicated in each figure.

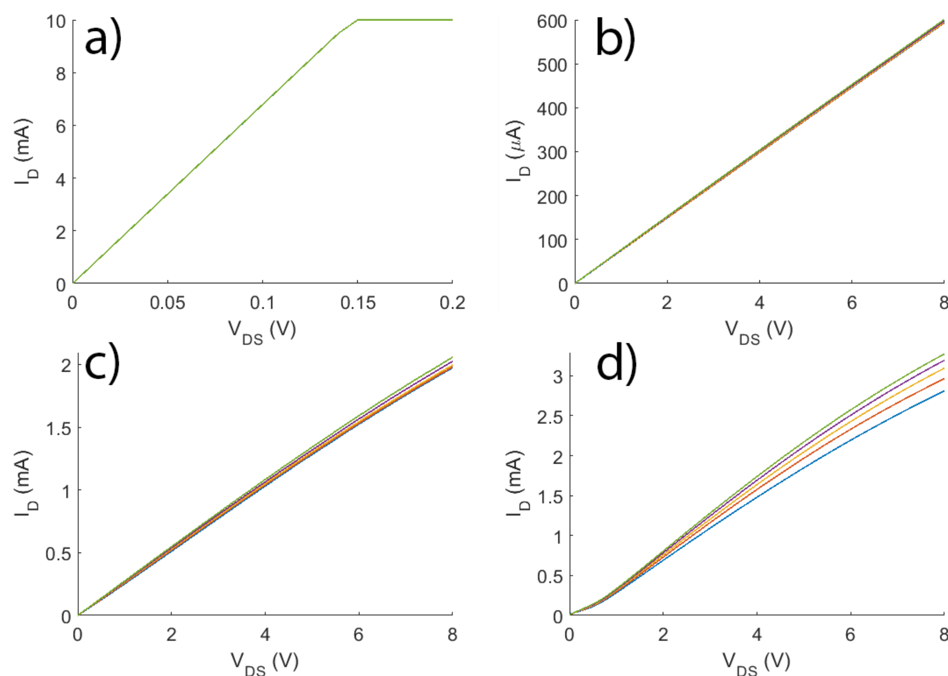


The increased transconductance observed in Figure 67 manifests itself as a larger separation between the I_D x V_{DS} curves for different V_{GS} values, from nearly indistinguishable in the 50 s sample to a clear separation in the sample etched for 80 s. Some distortion can also be observed for low V_{DS} values in the plot of the sample etched for 80 s, this could be due to imperfections in the metal deposition process or fluctuations on the dopant concentration.

The I_D x V_{DS} curves were also extracted and are plotted in 0. The first noticeable parameter is the increase in the channel resistance as soon as 50 s etching time. In the unetched sample the gate current rises to the set maximum measured current, 10 mA, with a V_{DS} variation of less than 0.15 V.

Figure 68 I_D x V_{DS} JL-FET measurements for each sample after complete fabrication

a) Unetched control sample b) Sample etched for 50 s c) Sample etched for 60 s d) Sample etched for 80 s. In each figure, V_{GS} varies from 0 V to 16 V in 4V steps.



CHAPTER 5

SUMMARY AND CONCLUSIONS

5.1 PROJECT SUMMARY

In this work, a technique to fabricate Junctionless-FET devices was studied. The simulations and theoretical study of the devices were used as base to propose this novel technique, based on vertical thinning of silicon wires by etching silicon in a NH_4OH solution.

After performing tests using the NH_4OH solution, an estimate for the etching rate was obtained. This step also familiarized the laboratory staff and authors with the intricacies of the etching technique.

By continuous study of the literature and the introduction of information obtained during simulation and etch rate tests, the parameters of the original process were proposed. Cross-Section SEM images were used to physically characterize, and both pseudo-MOS and JL-FET biasing were used to electrically characterize the devices. The devices fabricated using this process showed the expected behavior of devices with the observed dimensions and dopant concentrations.

Following the success of the first batch of devices, an update process was proposed. The silicon etching in NH_4OH solution was performed as soon as possible, mitigating the difference in etch rate when fabricating p-mos and n-mos devices. Paired with the use of mid-gap materials, this makes the process identical for p-MOS and n-MOS channels. The introduction of dopant diffusion instead of ionic implantation was also used, as dopant diffusion does not introduces as many imperfections in the silicon structures as ionic implantation does.

Also introduced by the updated process were two characterization techniques: first, optical and SEM images can be used in the first steps to confirm the success of the NH_4OH solution etching process, while enabling some measurement of underteching and evaluation of sidewall quality. Second, the gate-less Pseudo-MOS measurements, which are performed before the gate stack fabrication. This electrical characterization technique enables a quick

and reliable way to evaluate the process prior to the gate stack fabrication, which usually require techniques that are costly and of difficult access.

5.2 CONCLUSIONS

The numerical simulation model proved to be a valuable asset in evaluating and verifying the characteristics of the JL-FET device. The mode was used to accurately predict a range of channel thicknesses that would result in JL-FET operation and to verify the electrical properties of the fabricated device. An accurate numerical model is paramount to future fabrication efforts.

A first silicon etching rate calibration yielded an estimative for the NH_4OH solution wet etching, 2.5 nm/sec. This estimative was used to achieve a considerable precision in etching the desired areas.

The silicon wet etching in NH_4OH solution was applied to fabricate JL-FET devices. These devices showed that the channel regions were successfully thinned from 165 nm to 63-nm-thick, as observed in cross-section SEM imaging. SEM imaging also confirmed the sidewall profiles and effects expected of the wet etching. The devices were then electrically, characterized by pseudo-MOS measurements, which was used to evaluate the dopant concentration in the channel region, which was calculated to be on the order of 10^{17} atoms/cm^3. JL-FET biasing measurements were then used to verify the characteristics of the device when in operation. As expected of the figures of channel thickness and dopant concentration measured using SEM and pseudo-MOS measurements, the devices showed a negative V_{TH}, which means the devices are normally-on, and electrical contacts that presented Schottky barriers. This is akin to the results obtained by (PUYDINGER DOS SANTOS et al., 2013) and (LIMA et al., 2012).This characteristics are enough to for the devices to present analog-applications-ready JL-FET operation with mid-gap materials such as Titanium Nitride, and therefore completely compatible with state-of-the-art cMOS technologies.

The obtained parameters were used in the numerical simulation models and confirmed the operation of the device in JL-FET biasing.

The devices fabricated using the updated process were used to model the electrical characteristics according to etching time. Each sample was electrically measured using

Pseudo-MOS biasing prior to gate stack fabrication, showing the expected evolution of parameters. These measurements were used to perform a fitting of the V_0 measured in each sample to the etching time. The JL-FET measurements showed that the devices were indeed thinned and now presented behaviors closer to the expected JL-FET device, although still with negative threshold voltages.

5.3 FUTURE WORKS

In the future, the fabrication efforts will be focused on achieving the critical dimension of 10 nm, enabling a higher dopant concentration to be used, and possibly resulting in devices ready for digital applications. While the electrical characteristics of the device evolve, simple CMOS inverters will be used to characterize the electrical behavior and equivalence of the dual pMOS and nMOS processes.

The etching rate and characteristics will be refined and catalogued as to increase efficiency and precision in device fabrication. At the same time, wafer-wide fabrication processes will be performed, which will be used to evaluate the yield characteristics of the wet etching.

Better dopant diffusion processes that do not introduce as many contaminants and imperfections in the crystal lattice are also being studied for future applications, as are novel structural configurations that show promise in fabrication monolithic and GAA channels. These improvements would increase current modulation, raising V_{TH}, sharpening the I_{on}/I_{off} ratios and increasing current figures.

5.4 SCIENTIFIC CONTRIBUTION: PUBLICATIONS AND AWARDS

The scientific contributions of this work were published as:

- Extended abstract at XII Workshop on Semiconductors and Micro & Nano Technology (Seminatec 2018), presented at the event poster session in São Bernardo do Campo, SP:

STUCCHI-ZUCCHI, L.; SILVA, A. R.; DINIZ, J. A. Silicon channel thinning using NH4OH wet etching. p. 2, 2018.

- Extended abstract at XIII Workshop on Semiconductors and Micro & Nano Technology (Seminatec 2019), presented at the event poster session in Campinas, SP

STUCCHI-ZUCCHI, L.; SILVA, A. R.; DINIZ, J. A. Evolution of pseudo-MOS measurements in JL-FET structures according to silicon etching time in NH4OH solution, 2019

- Full paper at SBMICRO 2018, presented orally at Chip in The Pampa event in Bento Gonçalves, RS:

STUCCHI-ZUCCHI, L. et al. **Junctionless-FET fabrication using NH4 OH solution wet etching for silicon channel thinning**. 2018 33rd Symposium on Microelectronics Technology and Devices (SBMicro). **Anais**... In: 2018 33RD SYMPOSIUM ON MICROELECTRONICS TECHNOLOGY AND DEVICES (SBMICRO). Bento Gonçalves: IEEE, ago. 2018

- Full paper at SBMICRO 2019, presented orally at Chip in The Sampa event in São Paulo, SP:

STUCCHI-ZUCCHI, L;. SILVA, A. R.; DINIZ, J. A. **Junctionless-FET device fabrication using silicon etching in NH4OH solution: device behavior according to etching time**. 2019 34th Symposium on Microelectronics Technology and Devices (SBMicro). **Anais**... In: 2018 34th SYMPOSIUM ON MICROELECTRONICS TECHNOLOGY AND DEVICES (SBMICRO). São Paulo: IEEE, ago. 2019

- Abstract at 2018 AVS International Symposium and Exhibition, presented at the Electronic Materials and Photonics Division (EMPD) poster session in Long Beach, CA, USA:

STUCCHI-ZUCCHI, L.; SILVA, A. R.; DINIZ, J. A. **NH4OH Solution Wet Etching for Silicon Channel Thinning of Junctionless-FET**. AVS 65th International Symposium & Exhibition. **Anais**... abstract: EM-ThP6, pg. 239, In: AVS 65TH INTERNATIONAL SYMPOSIUM & EXHIBITION. Long Beach: AVS, out. 2018b Disponível em: <https://www2.avs.org/symposium2018/default.html>

This work was also awarded the **Electronic Materials and Photonics Division (EMPD) Student Poster Award** at 2018 AVS International Symposium and Exhibition in Long Beach, CA, USA.

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APPENDIX A: SILICON DOPING PROCESS DESCRIPTION

In nanofabrication, material doping is responsible by controlling the charge carrier concentration in the semiconductor substrate of the devices. According to solid solubility, electron distribution and chemical properties, a few dopant species are used: Phosphorus, Boron and Arsenic.

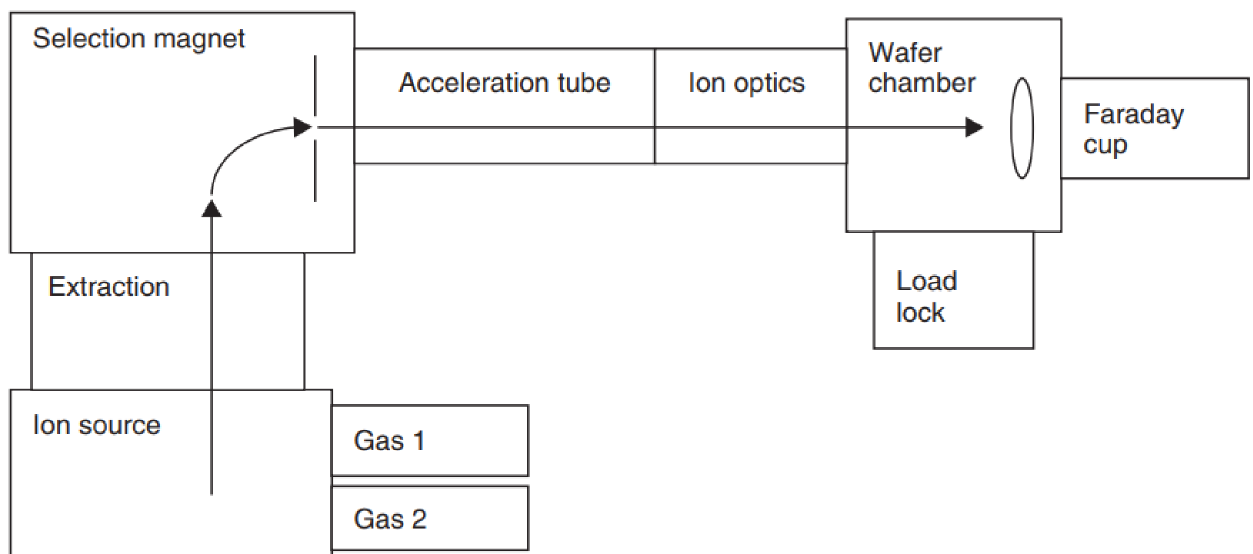
3A and 5A elements are the most common dopant species because Silicon is a 4A element, meaning that when in a monocrystalline arrangement, each silicon atom participates in a covalent bond with 4 neighboring silicon atoms. This configuration does not leave any free electrons that could participate in a current flow, but due to Fermi distributions of free electrons, some have enough thermal energy to make it to the Conduction Band. In this situation, the silicon is known as intrinsic silicon, and presents a small concentration of charge carriers, and therefore a considerable electric resistance. By introducing atoms of the 5A family, such as Phosphorus, or of the 3A family, such as Boron, it is possible to manipulate the concentration and polarity of the charge carriers. This happens, for example, because each atom will take the place of a silicon atom, and participate in the same four covalent bonds. If it is a phosphorus atom, all four bonds will be completed, and a free electron will be added to the crystalline array, making it richer in electrons. If it is a boron atom, three bonds will be completed, and a fourth will be left without and electron. This is called a hole, and although there is no particle associated to it, this lack of an electron in a covalent bond acts as a positively charged particle (SWART, 2008).

There are two main techniques used to introduce doping atoms in semiconductor materials after crystal formation: dopant diffusion and ion implantation. Both achieve the same effect, introducing foreign species in substitutional places in the semiconductor crystal lattice, which changes electrical, optical and/or mechanical characteristics of the semiconductor.

ION IMPLANTATION

In the ionic implantation process, atoms of the desired element are accelerated by an electric field and selected using a mass spectrometer, bestowing this process with reproducibility and control. These accelerated atoms collide with the silicon sample and penetrate in the crystalline structure. A faraday cup is used to count the number of atoms introduced, and the energy of each atom can be controlled by the electric field (FRANSSILA, 2010).

Figure 69 Schematics of a typical implanter (FRANSSILA, 2010).



A thermal process is then used so that these impurities take a substitutional place in the silicon crystallographic lattice, becoming active as sources of holes or electrons.

DOPANT DIFFUSION

The dopant diffusion technique is another way to introduce dopant atoms, and therefore charge carriers, in the semiconductor material. In the dopant diffusion, the samples are put in an environment saturated with the dopant atoms, such as phosphorus or boron. Then the sample temperature is raised to increase the dopant diffusity and allow the atoms to penetrate the sample and take substitutional places in the silicon crystallographic array.

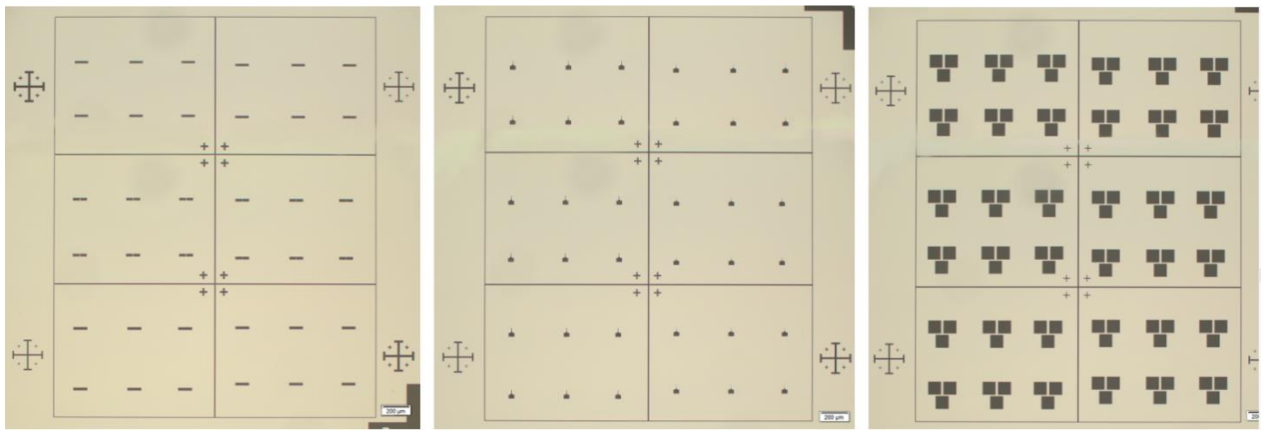
Two dopant diffusion processes are commonly used. The first is to use a furnace with its atmosphere saturated with a gas that carries dopant atoms, such as phosphine (PH_3) and

diborane (B_2H_6). The gasses are adsorbed by the sample surface, and the byproducts are dragged by the gas flow (FRANSSILA, 2010) The other process is called Spin-On-Diffusion (SOD) where a silicate solution saturated with doping atoms is deposited in the sample surface (USAMI et al., 1992). Using a hot plate or oven, the solvent is evaporated, leaving a borosilicate or phosphosilicate glass film. In an annealing furnace, usually in an inert gas environment, the diffusion temperature is achieved and the atoms penetrate the sample. With the drive-in process, the silicate film is removed and another thermal process is used to further drive in the dopants, this prevents the dopant atoms to segregate back in to the silicate.

APPENDIX B: OPTICAL PHOTOLITHOGRAPY PATTERNING PROCESS

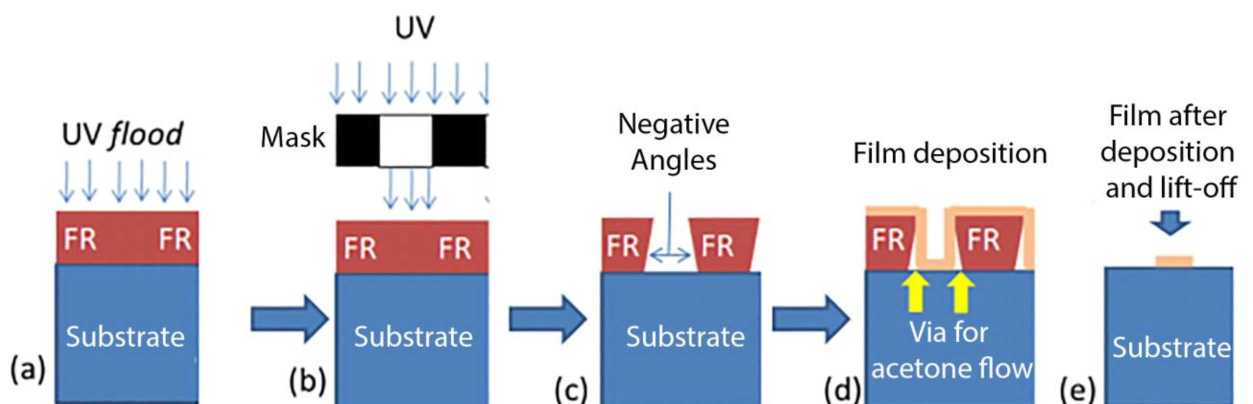
In device fabrication, the patterning processes are of utmost importance and determine key device characteristics, as the minimum patterned structure length, device pitch and others. Every photolithographic patterning process in this report, starting from the etching calibration, was carried out in a Karl Suss MJB3 mask-aligning system. It is a contact lithography type. The masks used are presented in Figure 70.

Figure 70 Photolithography masks used in the fabrication process. (LEONHARDT, 2016)



For all lithographic processes, a lift-off recipe was used as it achieved better precision and more regular sidewalls in previous works. This process generates angled walls that allow reagent flow underneath films deposited on top of the photoresist, enabling the removal of said films by photoresist stripping in acetone bath.

Figure 71 Lift-off process flow (RUFINO, 2019, adapted)



For the processes using the first mask, which corresponds to the active region, and the second mask, which corresponds to the gate region, the following processes were developed by (LEONHARDT, 2016):

Table 6 Process for patterning structures with active region and gate region masks

Process	Parameters	Comments
HMDS deposition and spin-coating	30 s of spinning time at 5000 RPM	The HMDS forms a thin polymer layer that promotes photoresist adherence to the silicon wafer
Solvent evaporation	1 minute at room temperature	
Photoresist (AZ5206) deposition and spin-coating	30 s of spinning time at 5000 RPM	At these parameters, the photoresist forms a 0.6μm-thick layer and presents a maximum resolution of 0.5μm-wide lines, according to the manufacturer
Baking	1 minute at 90℃	The solvents are evaporated, densifying the film
Pre-exposure without mask	0.8 s of UV light with power density of 190 mW/cm^2, Resulting in 0.15 J/cm^2.	Formation of a thin superficial film with different diffraction index. This film scatters the incoming light, forming the angled sidewalls needed for lift-off procedures.
Baking	45 seconds at 110℃	Part of the lift-off sidewall formation
Exposure using mask	20 s UV light with power density of 190 mW/cm^2, resulting in 3.8 J/cm^2.	Patterning of the structures
MIF300 developer	10 s at room temperature	Developing of the patterned structures

For the processes using the third mask, which are the metal pads, the following process was performed:

Table 7 Process for patterning structures with the metallic pads mask

Process	Parameters	Comments
HMDS deposition and spin-coating	30 s of spinning time at 5000 RPM	The HMDS forms a thin polymer layer that promotes photoresist adherence to the silicon wafer
Solvent evaporation	1 minute at room temperature	
Photoresist (AZ5206) deposition and spin-coating	30 s of spinning time at 5000 RPM	At these parameters, the photoresist forms a 0.6µm-thick layer and presents a maximum resolution of 0.5µm-wide lines, according to the manufacturer
Baking	1 minute at 90℃	The solvents are evaporated, densifying the film
Pre-exposure without mask	1 s of UV light with power density of 190 mW/cm^2, resulting in 0.19 J/cm^2.	Formation of a thin superficial film with different diffraction index. This film scatters the incoming light, forming the angled sidewalls needed for lift-off procedures.
Baking	45 seconds at 110℃	Part of the lift-off sidewall formation
Exposure using mask	25 s UV light with power density of 190 mW/cm^2, resulting in 4.75 J/cm^2.	Patterning of the structures

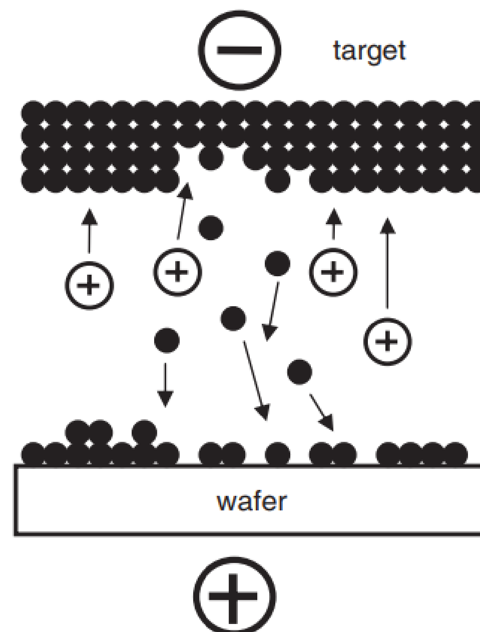
MIF300 developer	12 s at room temperature	Developing of the patterned structures

APPENDIX C: DC SPUTTERING

DC sputtering is a process commonly used to deposit metallic films. In this work, it was used in all metal depositions.

The DC sputtering process consists in electrically accelerating Argon ions generated during a glow discharge plasma towards a metallic target of the material to be deposited. The high-speed ions cause the ejection of the target atoms which redeposits onto the wafers, creating thin metallic films (FRANSSILA, 2010).

Figure 72 Schematic of the DC sputtering process (FRANSSILA, 2010)



Usually, a magnetron-generated magnetic field is used to confine the discharge plasma on the surface of the target, increasing the number of collisions, and therefore of ejected atoms.

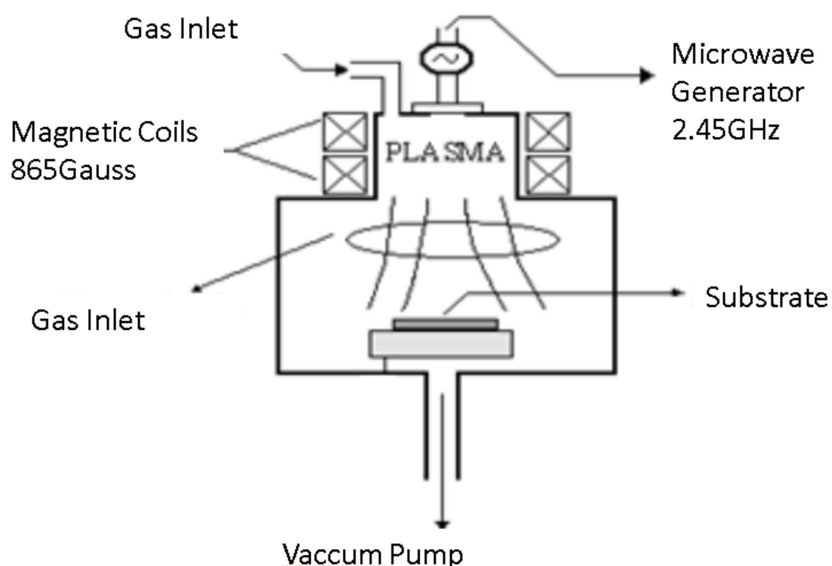
For Al depositions, pure argon is used with an Al target. For TiN depositions a Ti target is used, alongside a technique called reactive sputtering. N_2 gas flow is introduced and ionized alongside argon atoms in the glow discharge plasma, thus making reactive nitrogen available for TiN formation.

APPENDIX D: ECR-CVD

The Electron-Cyclotron-Resonance-Chemical-Vapor-Deposition (ECR-CVD) is a plasma-enhanced CVD (PE-CVD) process that can achieve high-density plasma. This method enables low-temperature deposition and growth of a number of materials, including silicon oxynitride (SiO_xN_y), silicon dioxide (SiO_2) or amorphous silicon (a-Si).

By using ions accelerated by a 2.45 GHz microwave generator and a magnetic field introduced by coils. When both the cyclotron motion of the ionized gasses induced by the magnetic field and the microwave generator achieve resonance, maximum energy is transmitted to the reagents, enabling and enhancing the deposition of numerous materials (SILVA, 2012). Figure 73 shows the schematic of the ECR-CVD chamber employed.

Figure 73 Schematic of the ECR-CVD chamber (SILVA, 2012)



APPENDIX E: SCANNING ELECTRON MICROSCOPY

Scanning Electron Microscopy (SEM) is widely used to physically characterize nanometer-scaled structures due to its high resolution, up to 5 nm depending on equipment (FRANSSILA, 2010), and high accuracy in representing topographic information.

This technique relies on the interaction between the primary electron beam and the specimen, shown in Figure 74, where a number of signals are generated and can be used in different material characterizations, such as the x-rays analyzed in Energy-Dispersive-Spectroscopy. In SEM applications, particularly, the secondary electrons are analyzed. These electrons generally present low energy, so they can only escape from shallow regions of the specimen and are easily captured by the detector (ZHOU et al., 2006). As SEM relays precise topographic information of the materials, it is important on surface roughness and structural characterizations. When paired with cross-section imaging, SEM can also show layering and structural characteristics of different materials, usually with good contrast between semiconductor and conductor materials. Insulator materials usually present charging problems, and require charge-dispersing techniques. 0 shows the typical structure of a Scanning Electron Microscope.

Figure 74 Interactions between electron beam-specimen and the corresponding signals generated (ZHOU et al., 2006)

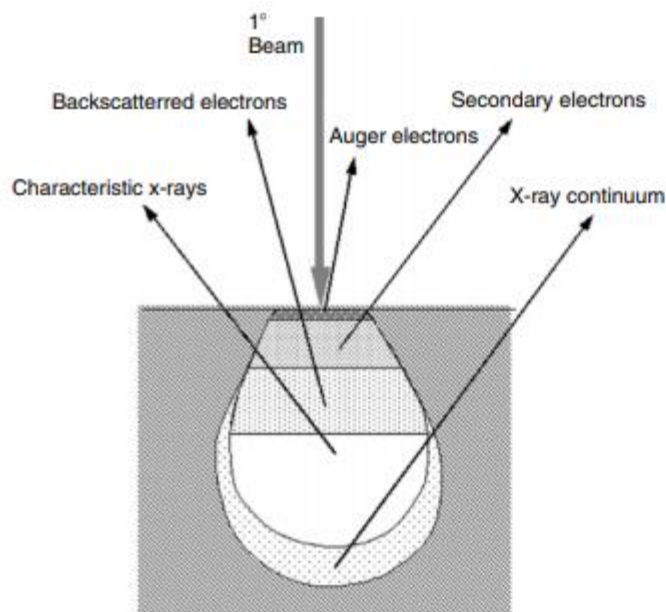


Figure 75 Schematic of a typical Scanning Electron Miscroscope (ZHOU et al., 2006)