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Comparative study between wet and dry etching of silicon for microchannels fabrication

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ABSTRACT

In this work we present a comparative study of two processes for the fabrication of an array of microchannels for microfluidics applications, based on integrated-circuit technology process steps, such as lithography and dry etching. Two different methods were investigated in order to study the resulting microstructures: wet and dry deep etching of silicon substrate. The typical etching depth necessary to the target application is 50 µm.

Keywords: Microfluidics, Microchannel array

1. MICROCHANNEL ARRAY FABRICATION

In this work we present a comparative study of two processes for the fabrication of an array of microchannels for microfluidics applications [1], based on integrated-circuit technology process steps, such as lithography and dry etching [2-4]. Figure 1 shows the process steps sequence for the microchannels fabrication employing dry and wet etching of silicon.

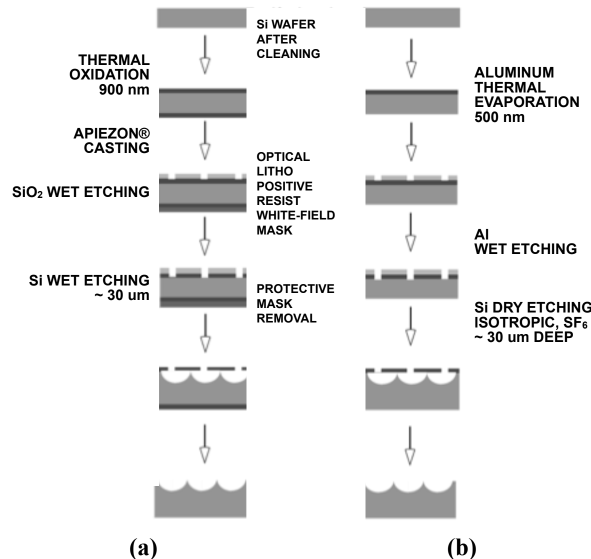

Figure 1. Process steps for the microchannels fabrication employing (a) wet and (b) dry etching of silicon.

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With the particular mask dimensions employed, it is possible to implement channels of approximately 40 µm depth, aspect ratio of (40/60) = 0.667, with trapezoidal and rounded cross sections.

Concerning the process carried out by wet chemical etching, the fabrication of the silicon microchannels consists of the following conventional microelectronics process steps: 1) standard wafer cleaning process, 2) thermal growth of a silicon dioxide film, 3) lithographical patterning of a 90 µm line - 10 µm space structure on top of silicon dioxide, 4) chemical wet etching of the oxide appearing in the 10 µm open spaces, 5) chemical wet etching of the silicon substrate using the oxide layer as a mask. A 3-inch diameter, (100), 1-20 Ω.cm n-type doped, 381 ± 50 µm thick, silicon wafer was used. A conventional Piranha - RCA sequence for wafer cleaning was used.

The thermal oxidation was performed in a conventional furnace, at 1150 °C, during 36 hours, resulting in a 0.9 µm thick silicon oxide film.

The lithography was performed using a contact printer. The photo resist (TOKYO OHKA ONPR800) was spun at 2500 rpm during 20 s, and submitted to a pre-bake at 105 °C for 90 s, resulting in a thickness of 1.2 µm. The wafer was exposed during 30 s, submitted to a post-bake at 120 °C for 35 minutes and developed (HPRD-402 OCG positive resist developer) at a proportion of 2 Developer : 1 DI-water.

The first wet etch, needed to open the oxide windows, see figure 1, was performed using a composition of 6 NH4F + 1 HF, at room temperature, resulting in an etch rate of 0.12 µm/min. Figure 2 shows micrographs of the resulting microchannels structures fabricated from dry and wet deep etching of silicon.

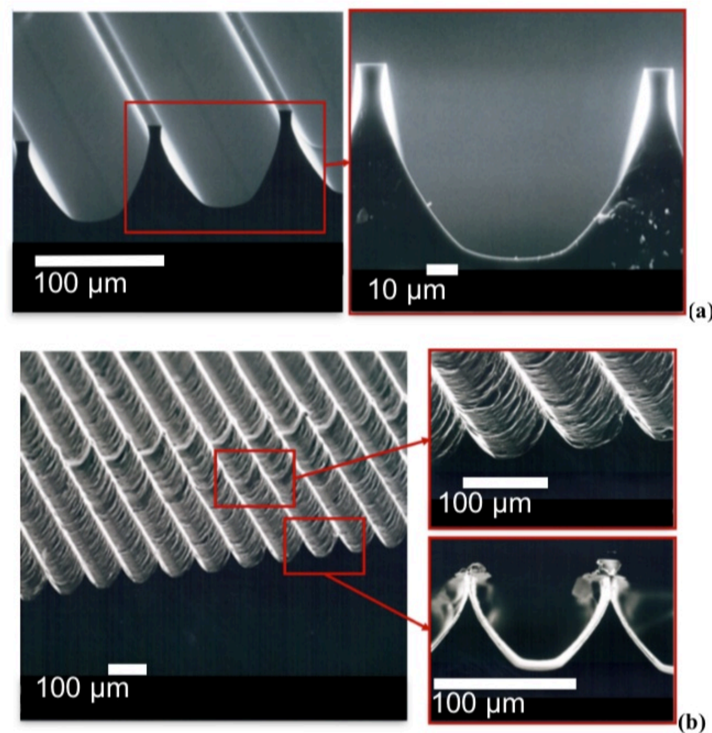

Figure 2. Micrographs of the resulting microchannels structures fabricated from (a) wet and (b) dry deep etching of silicon.

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The wet etching of the silicon substrate was performed using a solution to chemically polishing silicon substrates [ref Quick Reference Manual for Silicon Integrated Circuit Technology] that consists of 1 HF + 6 HNO3 + 1 CH3COOH, at room temperature, resulting in an etch rate of approximately 2.4 µm/min. After about 15 minutes the oxide mask has been entirely etched away. A final dip in a diluted HF solution was done to clean some residual oxide material remaining after the silicon etching.

Concerning the dry etching process, the fabrication of the silicon microchannels consists of the following conventional microelectronics process steps: 1) standard wafer cleaning process, 2) thermal evaporated aluminium film, 3) lithographical patterning of a 90 µm line - 10 µm space structure on top of aluminium, 4) chemical wet etching of the aluminium appearing in the 10 µm open spaces, 5) plasma etching of the silicon substrate using the aluminium layer as a mask.

Here again a 3-inch diameter, (100), 1-20 Ω.cm n-type doped, 381 ± 50 µm thick, silicon wafer was used, and submitted to conventional Piranha - RCA sequence for wafer cleaning was used. The 500 nm-thick aluminium mask was obtained by thermal evaporation. For the particular geometry of the used equipment, the final thickness is related tho aluminium mass by the rate of 34 gm/100nm.

The lithographic exposure and development steps were similar to the previous case, except that the exposure time was reduced from 30 to 18 seconds due to the high reflective of aluminium.

The exposed aluminium was then chemically etched, using photoresist as mask. It was carried-out by using an phosphoric acid solution (67.1%vol), nitric acid (5.8%vol) and de-ionized water (18MΩ.cm), during 5 minutes, after which the sample is read to deep silicon dry etching.

Just before to be inserted in the plasma chamber, the sample was submitted to a 1-second dip in 1HF : 50 H2O-DI solution to remove native oxide. The plasma etching was carried out by SF6 plasma (25 sccm) with thermal aluminum mask. The etching was carried out at relatively low power / high pressure (50W, 150mTorr) discharge level, enabling low cathode self-bias (20V), and therefore low-energy ion bombardment on a reactive ion etching (RIE) configuration.

Its important to notice that de smoothness of the resulting microchannels will dictate the flow regime in terms of turbulence. Therefore it is very important to keep the ion bombardment average energy as low as possible in order to avoid mask material sputtering and re-deposition, causing the so-called micro-masking. The resulting etching rate was 62 nm/min. The obtained structures presented a rough surface, which is favourable to maintain more turbulent flow regime.

Table I summarises comparative results in terms of average roughness, Ra, and channel depth results, obtained by AFM/SEM microscopies and step-height topography measurements (SHM). Average Roughness results were measured in the field regions of the samples. The surface quality obtained from wet etching is 17.7 times better (smoother) with respect to dry etching, whereas the channel depths are 32 and 36 um for wet- and dry etching, respectively.

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Table I. Average roughness, Ra, and deepness of the channel results, obtained by AFM/SEM microscopies and step-height topography measurements (SHM). Roughness measured in the field regions of the samples, on a white-field photomask.

sample	Ra [Å] by AFM	Channel depth [μm] by SHM	Remark / etching time
Si wafer	2,5 ± 10%	-	Si wafer (after RCA cleaning procedure)
After wet etching	6,3 ± 19%	32	21 min
After dry etching	112 ± 10%	36	80 min , SF6 plasma

Another important aspect is to keep a flat part of the periodic structure, in order to have available surface for the subsequent sealing of the microchannels by using wafer bonding. Defining the rate S = (s/T), and the aspect ratio R = (h/d), as shown in figure 3, one can notice that higher sealing area coverage is obtained by decreasing the aspect ratio, and therefore the cross section of the microchannel element

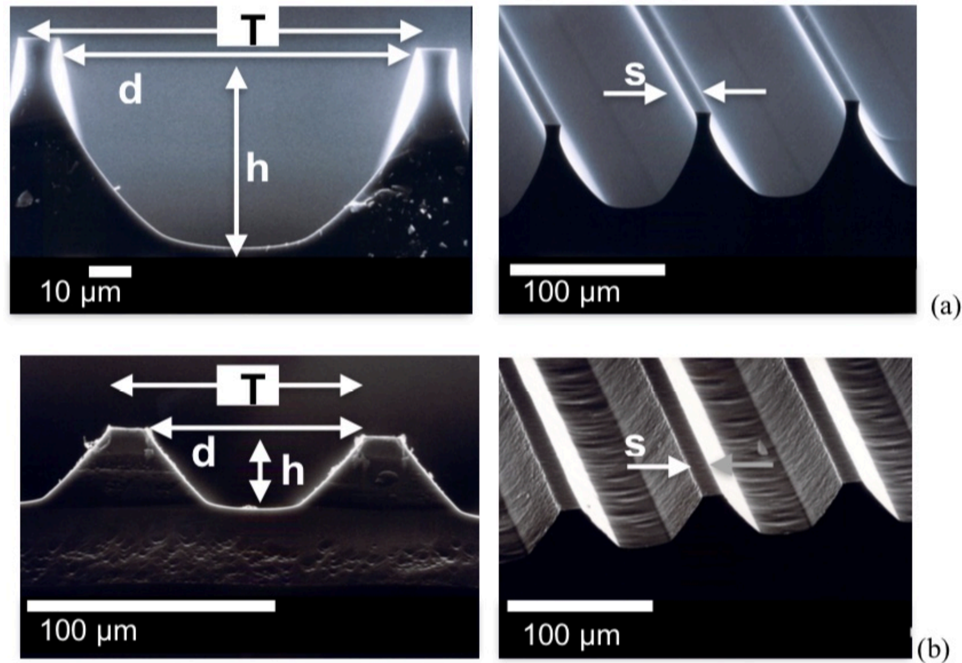

Figure 3. Micrographs of the resulting microchannels structures with a flat part on its top, to help the sealing of the microstructure enabling a higher operation pressure. (a) fabricated by wet etching , lower-S and higher-R and (b) fabricated by dry deep etching of silicon, higher-S and lower-R.

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For figure 3a (wet etching) one has S = 10% = (10µm / 100µm) and R = 55% = (50µm / 90µm); for figure 3b (dry etching) one has S = 17% = (17µm / 100µm) and R = 40% = (34µm / 83µm) = 40%. Figure 3 shows final results with two different surface sealing, as percent of the pitch of the channel array.

2. CONCLUSION AND FUTURE WORKS

This work presented a comparative study of two processes for the fabrication of an array of microchannels for microfluidics applications. Concerning the process carried out by wet chemical etching, the obtained structures presented a very smooth surface, which is favourable to maintain a laminar flow. The etching rate was 2,4 µm/min. Considering the dry etching process, the resulting etching rate was 62 nm/min. The obtained structures presented a rough surface, which is favourable to maintain more turbulent flow regime. As a future works we propose study of other high-aspect ratio plasma deep etching process by changing the plasma chemistry exploring the combination of selective passivation and etching.

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