Si3N4 photonic integration platform at 1 μm for optical interconnects

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Si_3N_4 photonic integration platform at 1 μm for optical interconnects

XIAONAN HU,[1] MARCELLO GIRARDI,[1] ZHICHAO YE,[1] PASCUAL MUÑOZ,[2] ANDERS LARSSON,[1] AND VICTOR TORRES-COMPANY[1,*]

[1] *Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Gothenburg, Sweden*
[2] *Photonics Research Labs, Universitat Politècnica de València, c/ Camino de Vera s/n, 46021 Valencia, Spain*
[*] *torresv@chalmers.se*

Abstract: Vertical-cavity surface-emitting lasers (VCSELs) are the predominant technology for high-speed short-range interconnects in data centers. Most short-range interconnects rely on GaAs-based multi-mode VCSELs and multi-mode fiber links operating at 850 nm. Recently, GaAs-based high-speed single-mode VCSELs at wavelengths > 1 μm have been demonstrated, which increases the interconnect reach using a single-mode fiber while maintaining low energy dissipation. If a suitable platform for passive wavelength- and space-multiplexing were developed in this wavelength range, this single-mode technology could deliver the multi-Tb/s interconnect capacity that will be required in future data centers. In this work, we show the first passive Si_3N_4 platform in the 1-μm band (1030-1075 nm) with an equivalent loss < 0.3 dB/cm, which is compatible with the system requirements of high-capacity interconnects. The waveguide structure is optimized to achieve simultaneously single-mode operation and low bending radius, and we demonstrate a wide range of high-performance building blocks, including arrayed waveguide gratings, Mach-Zehnder interferometers, splitters and low-loss fiber interfaces. This technology could be instrumental in scaling up the capacity and reducing the footprint of VCSEL-based optical interconnects and, thanks to the broad transparency in the near-infrared and compatibility with the Yb fiber amplifier window, enabling new applications in other domains as optical microscopy and nonlinear optics.

1. Introduction

With the development of cloud services, the capacity requirement for optical links in data centers is growing rapidly. Future data centers will require short-reach optical links with multi-Tb/s capacity [1] while keeping low cost (~ 1 $/Gbps), low energy consumption (pJ/bit) per lane, and high reliability [2–4]. Short-range interconnects are the most common ones in data centers, where 90% of the links are shorter than 100 m. One example is the cables between the top of the rack (ToR) switch and the servers in the rack. Here, the energy consumption is a metric of paramount relevance, owing to the large number of connections involved. These links are dominated by active optical cables based on an intensity modulation/direct detection scheme using GaAs-based vertical-cavity surface-emitting lasers (VCSELs) and multimode fibers (MMFs) [2]. This solution is inexpensive, simple to implement and reliable, but presents two major drawbacks: the length of the link is limited at high data rates by the chromatic dispersion and attenuation in the MMF [3] and the form factor of the transceiver module is limited by the integration of all the active and passive components in the module itself when positioned at the front panel of the ToR switch. This suggests that a higher bandwidth density can be achieved by reducing the footprint of the active components and positioning them close to the switch ASIC (application specific integrated

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circuit), as shown in Fig. 1(a), leaving the passive optical connection only at the front panel of the switch [5,6].

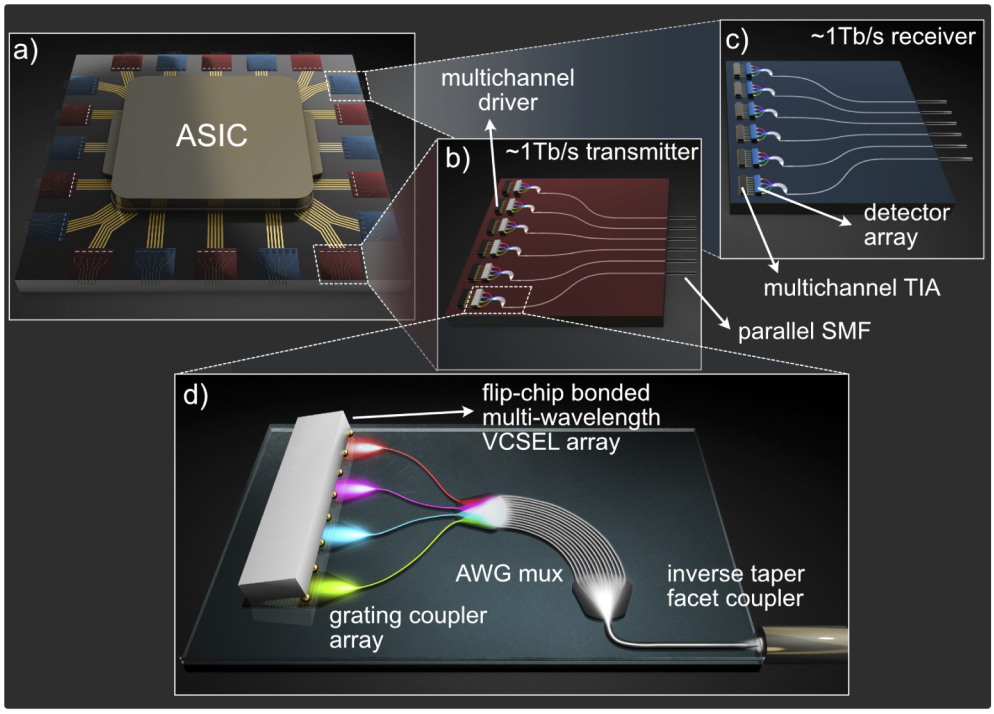

Fig. 1. Vision of a future switch ASIC interfaced with > 1 Tb/s optical transmitters and receivers (a). The Tb/s transmitter is enabled by a monolithic multi-wavelength array of directly modulated single-mode GaAs VCSEL at 1 µm and multi-fiber cables. This vision requires the use of a low-cost, low-loss passive photonic platform for laser integration, multiplexing, and low-loss fiber coupling (b). The multi-wavelength VCSEL array is flip-chip-bonded to the low-loss Si_3N_4 passive platform using an array of grating couplers [7]. The thermal crosstalk in the array can be considered negligible with sufficient distance between the VCSELs [13] and the metal contacts deposited on the SiO_2 cladding will help dissipate the heat of the VCSEL array (d). An on-chip multiplexer based on an arrayed waveguide grating combines the signals from individual channels in a single waveguide and couples them to the multi-fiber cable by means of a broadband inverse taper. The receiver side adopts a similar design, where the VCSEL array is replaced by a high-speed photodetector array and a transimpedance amplifier (TIA) (c). In this work, we focus on the passive platform for the transmitter.

Medium- and long-reach interconnects (300 m to 10 km) are less abundant in data centers, hence their energy consumption becomes a lesser critical issue; instead, it is the link capacity that becomes the relevant metric. Such longer-reach interconnects can exploit more complex modulation schemes, like discrete multitone [8] and/or quadrature amplitude modulation [9]. The transmission length is achieved based on a combination of single-mode fiber (SMF) and InP distributed feedback laser sources at 1310 nm, which are compatible with hybrid Si photonics technology [2]. Drawbacks of this technology are that it is more expensive, more difficult to manufacture and less efficient compared to GaAs VCSELs [10].

Recent developments in GaAs VCSELs and SMF herald an alternative to the established technologies by shifting the operating wavelength to ~ 1060 nm. At this wavelength, the dispersion and losses in SMF are decreased more than twofold with respect to links operating at

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850 nm with standard OM4 MMF cables [11]. Moreover, 1060 nm single-mode GaAs VCSELs have been demonstrated to operate with extremely low energy dissipation (100 fJ/bit) [12], and minimize the impact of chromatic dispersion due to the fewer spectral components in the VCSEL emission spectrum. Notwithstanding, a key remaining challenge is to reach multi-Tb/s interconnect capacity. Since the modulation bandwidth of a single VCSEL is practically limited to ~ 30GHz [1], achieving the target link capacity will likely require a form of space- and wavelength division multiplexing scheme based on e.g. parallel or multicore fibers and VCSEL arrays of multiple wavelengths [13–16].

Realizing this vision in the 1-μm band will require the use of a low-cost, low-loss passive photonic platform for laser integration, multiplexing, and fiber interfacing, as sketched in Fig. 1(b) and (c). In this work, we present a Si_3N_4 passive technology that meets the loss requirements of the passive technology at the transmitter side. Si_3N_4 is a low-loss passive technology that is transparent from the visible to the mid infrared [17] and compatible with CMOS fabrication techniques. Although diverse low-loss passive components in the visible and very near infrared have been demonstrated before [18–25], this is the first time that a Si_3N_4 platform is specifically designed for the 1-μm window (1030-1075 nm). One key aspect of our platform is that is aimed at moderate field confinement, allowing for small bending radii and dense integration. In spite of the drawbacks associated with strong scattering losses when going to shorter wavelengths in moderate-confinement waveguides, we demonstrate equivalent losses < 0.3 dB/cm. In addition, the platform is developed considering the design constraints imposed by the needs of cascading multiple low-loss devices. Beyond optical interconnects, this wavelength window is relevant for applications in microscopy because the 1-μm band provides a better balance between water absorption and scattering, allowing for deeper penetration depths in tissue, see e.g. [26]. Incidentally, our target bandwidth coincides with a portion of the gain window of Yb-amplifiers [27], making our waveguide technology compatible with mode-locked Yb fiber lasers and offering additional prospects for ultrafast optics and nonlinear applications.

2. Loss-budget analysis from a system-level perspective

In this section, we analyze the maximum level of tolerable losses in the transmitter and receiver. We envision reaching > 1 Tb/s by using coarse-wavelength division multiplexing with 4-wavelength VCSEL arrays (wavelengths located at 1033, 1041, 1049 and 1057 nm), where each VCSEL is directly modulated at 25 Gbaud, providing 50 Gb/s data rates using 4-pulse-amplitude modulation (4-PAM) signaling. The channel spacing is designed to accommodate potential thermal drifts with temperature of the VCSEL array [13]. Following the schematics in Fig. 1, a pre-FEC data rate of 1.2 Tb/s could be achieved by multiplexing to 6 parallel single-mode fibers in a single optical cable. Figure 2 shows the bit error ratio (BER) at different received optical powers for On-Off Keying (OOK) and 4-PAM encoding, assuming a thermal-noise-limited receiver. Setting a typical BER threshold at 10^{-3} for hard-decision FEC [18] yields a minimum received optical power to -8 dBm for 4-PAM. Given that single-mode VCSELs at 1060 nm can deliver 6 dBm [10], we end up with 14 dB of loss budget for the whole link.

Single-mode fiber in the 1 μm band features losses in the order of 1 dB/km [11], leaving us with ~ 6 dB for the transmitter loss budget in a 2 km link. We consider splitting equally the losses between transmitter and receiver because similar components will be realized at either side. One important difference is that the components at the receiver side must be polarization insensitive in order to avoid the use of polarization maintaining fiber in the link, but this can be achieved by properly selecting the cross-section geometry of the passive components [29–31].

We consider Si_3N_4 technology owing to its compatibility with CMOS fabrication techniques [32], low-loss and ultrabroad transparency window extending to the visible range [17,33]. In view of recent developments of low-loss Si_3N_4 waveguides in the visible [18] and very near-infrared (VNIR) [19], arrayed-waveguide-gratings (AWGs) [20,21], and efficient fiber to chip coupling

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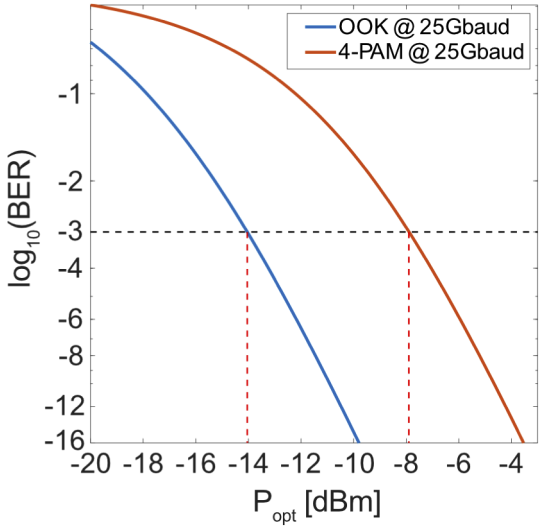

Fig. 2. Theoretical BER versus received optical power under OOK and 4-PAM encoding, calculated for a thermal noise limited system at T=298K and Gray labelling for the 4-PAM encoding [28]. The bandwidth, responsivity of the photodiode, noise figure of receiver amplifier and the load resistance are 50GHz, 0.4A/W, 5dB and 50Ω.

interfaces based on inverse tapers [22,23] as well as surface couplers [24,25], we set < 2 dB loss as a feasible target for each of the components.

3. Platform considerations and fabrication process

A key aspect of this work is that we consider a holistic approach in the component design, i.e. we embrace crucial constraints that must be taken into consideration when designing a full photonic platform. For example, ultra-low losses could be attained by designing thin Si_3N_4 cores that minimize scattering losses due to sidewall roughness [34], but this solution would come at the expense of large bending radii and device footprint that would make the devices incompatible with dense integration. Low-loss AWGs can be achieved with thin Si_3N_4 waveguides, but thick waveguides are preferred for grating couplers [35,36].

We restrict ourselves to a waveguide cross-section geometry that results in moderate field confinement in a Si_3N_4 core. The core dimensions are 900×160 nm (width x height) and the thickness of both the SiO_2 substrate and cladding is 3 μm, see Fig. 3(a). The indices used for Si_3N_4 and SiO_2 are obtained with ellipsometry measurements and their values are respectively around 2.00 and 1.45 at 1045 nm. The thickness is selected to ensure simultaneously single-mode operation and optimal VCSEL coupling efficiency with a single-etched grating coupler (see next section). The resulting waveguide geometry supports both fundamental quasi TE and TM modes. However, the TM mode is less confined than the TE and it is not guided for a bending radius smaller than 230 μm.

On the contrary, the simulated bending losses for the TE mode shown in Fig. 3(b) indicate negligible losses for a bending radius larger than 30 μm, making the platform promising for dense on-chip integration and practically single-mode when using single-polarization single-mode VCSELs [37].

The fabrication flow starts from the thermal oxidation of a 3" Si wafer to make a 3μm-thick SiO_2 undercladding. Then, stoichiometric Si_3N_4 is deposited in a furnace chamber at a temperature

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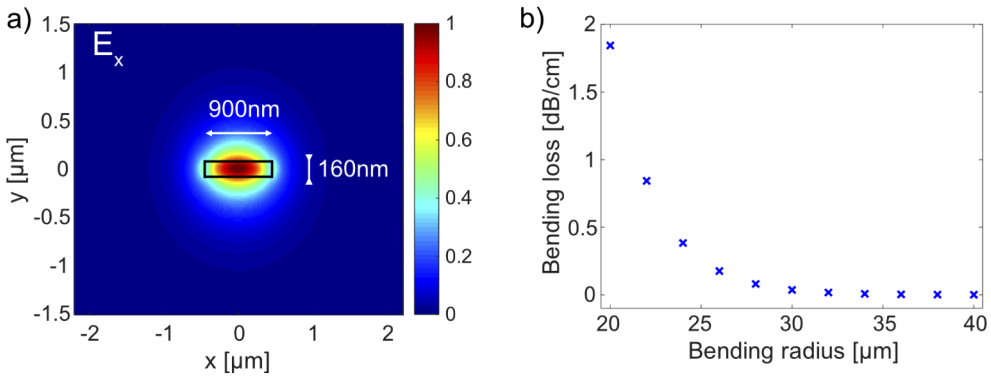

Fig. 3. (a) Simulated mode distribution of x-component of the electric field for the fundamental TE mode at 1045 nm and (b) simulated bending loss for different bending radii.

of 770°C by low-pressure chemical vapor deposition (LPCVD) with a desired thickness of 160 nm on the oxidized wafer. After that, the wafer is patterned by electron-beam lithography (EBL), followed by CHF_3 and O_2-based dry etching to pattern Si_3N_4. The obtained waveguide sidewall root mean squared (RMS) roughness ~ 1 nm and surface RMS roughness < 0.18 nm are measured by top view SEM image and atomic force microscopy, respectively. The wafer is thoroughly cleaned by a standard cleaning procedure and clad by deposition of tetraethyl orthosilicate (TEOS) via LPCVD with a thickness of 500 nm. Lastly, the wafer is clad with SiO_2 by plasma-enhanced chemical vapor deposition (PECVD) again to have a total upper cladding thickness of 3 μm.

We note that we used two processes that are not fully compatible with low-cost, high-volume CMOS manufacturing. The first one is LPCVD which is allowed only in the front end of line of the CMOS fabrication. This high temperature process requires the wafers to be metal free. This issue could be overcome with a careful planning of the manufacturing steps or via wafer bonding [38]. An alternative solution is to use lower temperature deposition of Si_3N_4 via PECVD, which has been demonstrated to give similar loss performance to LPCVD in the very near infrared, far from the N-H absorption peaks [39]. The second process not fully CMOS compatible is EBL. To minimize the impact of this development technique, the minimal feature in our designs is kept above 300 nm, so that processing can be achieved by commercial wafer scale deep-UV lithography. Note that with a careful selection of pattern size and minimum feature size, a similar sidewall roughness could be achieved with deep UV stepper lithography [40].

4. Si_3N_4 component library

In this section, we show our results for the diverse passive components fabricated with the Si_3N_4 technology described above. The width of the waveguide can be varied depending on the particular device, but all components maintain a guiding layer height of 160 nm. For the measurements, a tunable single mode laser between 1015-1075 nm is used as the light source. The polarization of the laser is controlled by a fiber polarization controller, where the right polarization is selected by monitoring the throughput of a polarization sensitive device, e.g. a bent waveguide. The laser wavelength is swept continuously, and the light is coupled in/out of the devices via lensed fibers.

The power is detected by a photodiode and monitored by a sampling oscilloscope. The laser tuning is calibrated with the aid of a fiber interferometer whose arm delay is measured with a mode-locked laser that has its repetition rate stabilized. This allows to link the value of the interferometer delay to a radio-frequency reference, providing an accurate means to calibrate the

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tuning speed of the laser vs time, and in turn the wavelength axis of the transmission response of the passive devices here presented.

We begin with microring resonators. These devices allow to infer the propagation losses by analyzing the intrinsic quality factor [41]. The section follows by results of AWGs and inverse tapers, after which simulations of the grating couplers are presented.

4.1. Microring resonators

The point coupling between the ring waveguide and bus waveguide is adopted for the ease of fabrication process. Both the bus and ring waveguide have the same dimensions as in Fig. 3. The coupling region of the ring resonator can be seen in the scanning electron microscope (SEM) image presented in Fig. 4(a). The sidewall of the waveguide is nearly vertical and the gap between the ring and bus waveguide is successfully resolved, which prove the high quality of our fabrication process. The gap between the ring and the waveguide is 650, 700 and 750 nm for the rings included in the histogram in Fig. 4(b). The radius of the ring is selected as 196 μm, so that bending losses can be considered negligible. The intrinsic quality factor (hereafter Q) of multiple microring resonator devices has been measured and we present the results in the form of a histogram in Fig. 4(b), together with a representative critically coupled resonance dip in the inset. The mean Q is 2.3 million (corresponding to an equivalent waveguide loss < 0.3 dB/cm [41]). The loss is mainly attributed to scattering due to sidewall roughness, and potential aliasing from pattern fracturing due to field stitching in EBL lithography. Such loss level is comparable with what has been demonstrated at shorter and longer wavelength for moderate confinement [17], thus providing a solid foundation for the system architecture presented in Fig. 1.

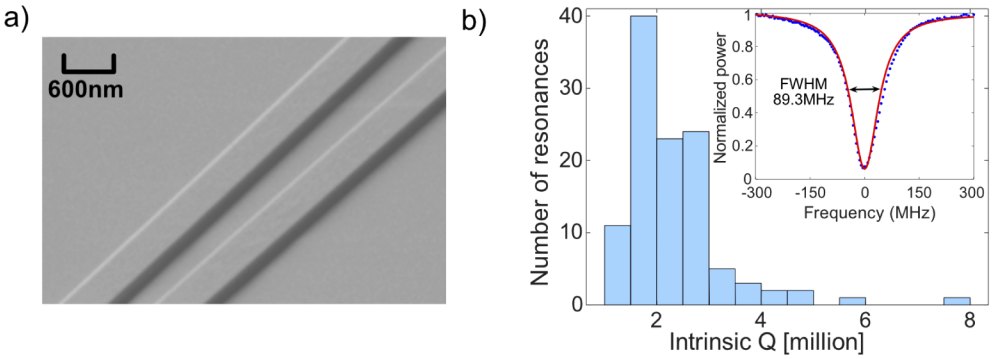

Fig. 4. (a) SEM image of the gap between the microring and the bus waveguide and (b) histogram of the intrinsic quality factor of the measured ring resonators with a representative resonance in the inset.

4.2. Arrayed-waveguide-grating (AWG)

Here, a 4-channel AWG serves as multiplexer/demultiplexer of our platform. The AWG has been designed symmetrically with 4 input x 4 output channels (Fig. 5). The channel spacing is set to 8 nm in the range 1033–1057 nm and the design follows the procedure discussed in [42]. A tapered waveguide is included between the arrayed waveguide and the free propagation region (FPR) to decrease the mode mismatch [43]. The design is guided by simulations, where the best case predicted a bandpass transmission of -1.2 dB and -33 dB crosstalk. The relevant geometrical parameters of the AWG are reported in Fig. 5(c), which consists of 28 waveguides with a length difference 15.7 μm. The free-spectral-range (FSR) is designed to be 40 nm, which is larger than (4×8=) 32 nm, in order to maintain low insertion loss for all channels.

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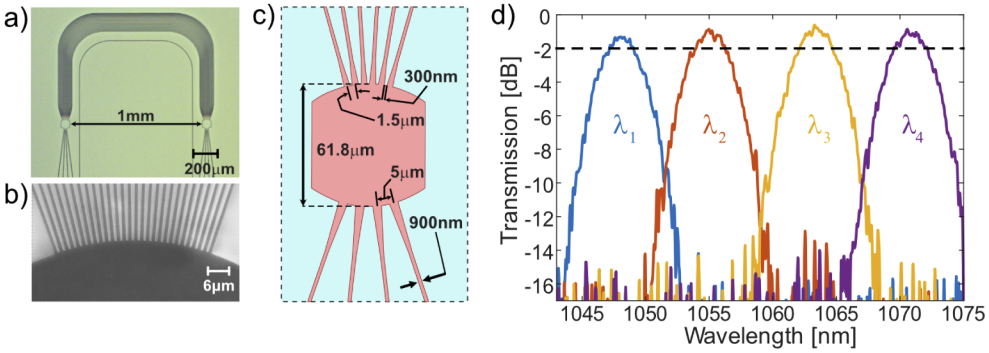

Fig. 5. (a) Optical microscope image of the fabricated AWG. (b) SEM image of the interface between the arrayed-waveguide and the FPR in the fabricated AWG. (c) Schematic diagram of the FPR with detailed dimensions in the design. (d) Measured transmission of the AWG device, normalized to the coupling loss between the waveguide and lensed fiber.

The footprint of the device is roughly 1×1 mm – excluding the input and output waveguides. In Fig. 5(b), it can be seen that the gap between the arrayed waveguide is fully resolved. A reference waveguide is included besides the AWG to evaluate the fabrication quality. The light from a tunable laser is injected to input channel 2 and the responses of all the 4 output channels are recorded. The responses are normalized to the coupling loss between the optical fiber and the chip, resulting in the transmission spectra shown in Fig. 5(d), which therefore represents the response of the single AWG. In Fig. 5(d), it can be noted that loss of each channel is within the 2 dB limit set in Sect. 2 and the average loss per channel is 1.1 ± 0.2 dB. The measured channel spacing and FSR of the device are 7.6 ± 0.7 nm and 41.0 ± 0.1 nm, respectively. The small ripples on the response of each channel are caused by the Fabry-Perot interference from the chip facets. The crosstalk is -13.2 ± 0.7 dB, but we believe this is limited by the sensitivity of our photodetector and the characterization setup. We note that the center wavelength of the channels deviates from the target values, possibly due to a slight variation in array waveguide thickness or in the refractive index of the film. In future designs, a thermal heater [44] may alleviate these constraints.

4.3. *Inverse tapers*

The inverse taper structure as shown in Fig. 6(a) is a common waveguide structure located at the chip facet to facilitate the coupling between the fibers and on-chip components by increasing the mode effective area to match the Gaussian mode in the fiber coupled to the chip. The adiabatic taper provides a smooth transition of the confined mode along the propagation direction. Although various taper geometries have been explored extensively in the past [23,45], here we adopt a simple adiabatic linear taper geometry.

The length of the taper is set to 300 μm to fulfill the adiabatic condition, while the width is tapered down from 900 nm to different values. Simulations of the tapered structure show an optimum tip width of 380 nm for the lowest coupling loss at 1045 nm. In the simulation we considered to couple the taper to a lensed fiber single mode at 1065 nm, with mode field diameter (MFD) 2.0 ± 0.5 μm. The MFD of the waveguide at the tip of the inverse taper is asymmetric and the diameters are $\mathrm{MFD_x} = 0.9$ μm and $\mathrm{MFD_y} = 0.7$ μm. No conversion from the fundamental TE mode to other mode is found, guaranteeing that the polarization is maintained along the transmission.

We first fabricated a series of devices to calibrate the shrinkage from the design value and the actual fabricated device. After calibration, the performance of the taper is obtained by

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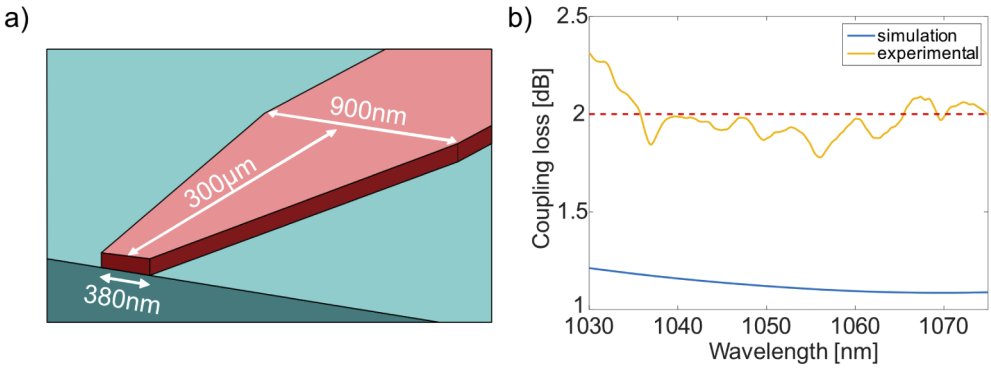

Fig. 6. (a) Sketch of the inverse taper. (b) Measured coupling loss of the inverse taper with 380nm tip (yellow) and simulated loss for the same inverse taper (blue).

characterizing the coupling loss of a reference inverse taper with a fixed tip width. The coupling loss of the inverse taper with a fabricated tip width of 380 nm is reported in Fig. 6(b). Coupling losses < 2 dB are obtained over a 30 nm bandwidth, meeting our requirements. The deviation between the measured coupling loss and the simulated loss showed in Fig. 6(b) may come from a misalignment of the fiber, the slanted sidewall of the taper tip and/or the uncertainty in the value of the spot size of the lensed fiber.

4.4. Surface grating coupler

The analysis of the surface grating coupler is done via simulation only. The designs are customized to fit different channel wavelengths. The design procedure starts from a normal grating of uniform period and 50% duty cycle, where the thickness of the waveguide is kept at 160 nm, to make the device compatible with the other components discussed previously. The incident light from the VCSEL has an angle of 11° to the normal of the grating to enable unidirectional coupling and prevent optical feedback to the VCSEL by specular reflection, and the source is positioned 24.58 µm above the top cladding.

Six pairs of SiO_2/TiO_2 (CMOS compatible) with thickness 115 nm and 182.7 nm, respectively, have been included between the substrate and under-cladding layer to form a distributed Bragg reflector (DBR), see Fig. 7(a), and improve the coupling efficiency [24], providing a better coupling efficiency compared to other geometries based on Si, where the index contrast and a careful tunining of the reflection helps in decreasing the coupling loss [46]. The DBR does not affect the simulated losses of the waveguide. Indeed, the bending losses for a waveguide with this DBR included in the under-cladding are the same as showed in Fig. 3(b). The materials are selected according to our previous work [47], which proved that high reflectivity in this wavelength band could be attained. The thicknesses of the top and bottom SiO_2 cladding have been optimized to minimize the light reflected outside the grating and maximize the light coupled in the waveguide at the central wavelength 1045 nm. The total thickness of the under-cladding, including the DBR is 3.64 µm, while the thickness of the top cladding is 2.92 µm. Once cladding layers and the DBR are fixed, the period and duty cycle of the grating are swept iteratively in the simulation in order to obtain a chirped grating that maximizes the coupling efficiency at the different target wavelengths.

The simulation results for all the 4 channels are shown in Fig. 7(b), resulting in < 1 dB coupling losses. The optimization process is done only by sweeping the period and the duty cycle of the grating, so that all the gratings can be fabricated on the same wafer simultaneously. The coupling loss is sensitive to the upper and lower cladding thickness, and a careful control of thickness is crucial in order to maintain the high performance of the grating couplers.

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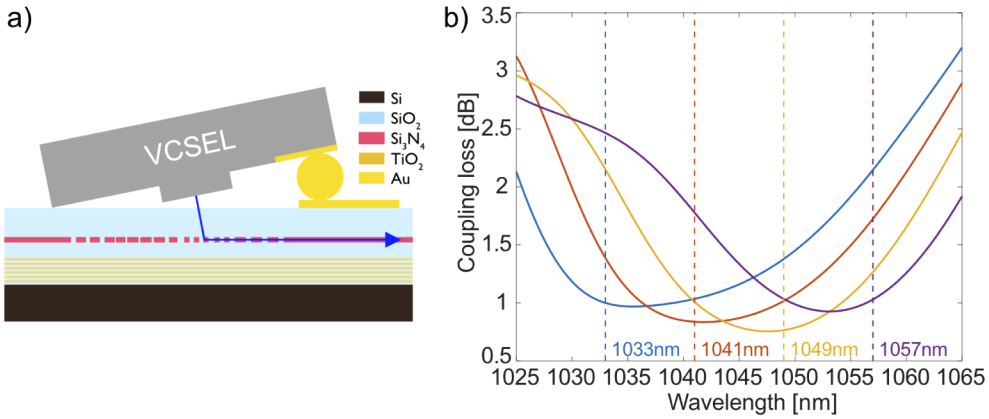

Fig. 7. (a) Cross section of grating coupler design (b) Simulation results for the optimized grating couplers designed for each channel.

5. Additional components beyond optical interconnects

The devices presented in the previous section constitute the basis for the system in Fig. 1. In this section we present a series of devices that complement the platform and whose performance can enable additional applications relying on this low-loss passive waveguide platform in the near infrared.

5.1. Multimode interference couplers (MMIs)

MMIs are widely used in photonic integrated circuits for power-splitting and combining [48]. There are several advantages for MMIs, including the high tolerance to dimension deviations in the fabrication, large bandwidth and low polarization dependence [49–51]. Here both 1×2 and 2×2 MMIs are designed under the same waveguide dimension, which could be incorporated in the platform to split/combine on-chip signals evenly. The combination of two signals generally requires control over the relative phase between the signals. In this case a simple evaporated Pt heater could be included on top of the cladding to tune the phase of one channel [52].

Similar to [53], the taper is included between the multimode waveguide and input/output waveguides in order to provide a better mode matching and thus reduce the insertion loss of the device. The tapers start from a 900 nm width to an optimized end width of 1700 nm where only the fundamental TE mode could propagate.

An optical microscope image of a fabricated 1×2 MMI is shown in Fig. 8(a). In the mask layout, the MMIs are designed in a way that one of the two output waveguides of the previous MMI is cascaded with the input waveguide of the next MMI, so we can measure the transmission for different numbers of MMIs. This allows us to do a first-order polynomial fitting of transmission versus the number of MMIs. The loss per MMI stage and coupling loss between the lensed fiber and waveguide can be inferred from the slope and intercept of the polynomial, respectively. The obtained average total loss for both 1×2 and 2×2 MMIs are shown in Fig. 8(a). The average loss per stage for the 1×2 and 2×2 MMI are, respectively, 0.6 ± 0.1 dB and 0.5 ± 0.2 dB across 1020-1060 nm, comparable to the losses of other similar devices described in the literature [54].

5.2. Mach-Zehnder interferometer (MZI)

The Mach-Zehnder interferometer (MZI) configuration is a commonly used structure for modulators in conventional Si photonics [55–57]. As a proof-of-concept, we fabricate simple passive MZIs, which consist of two 2×2 MMIs as input and output couplers, and two interference

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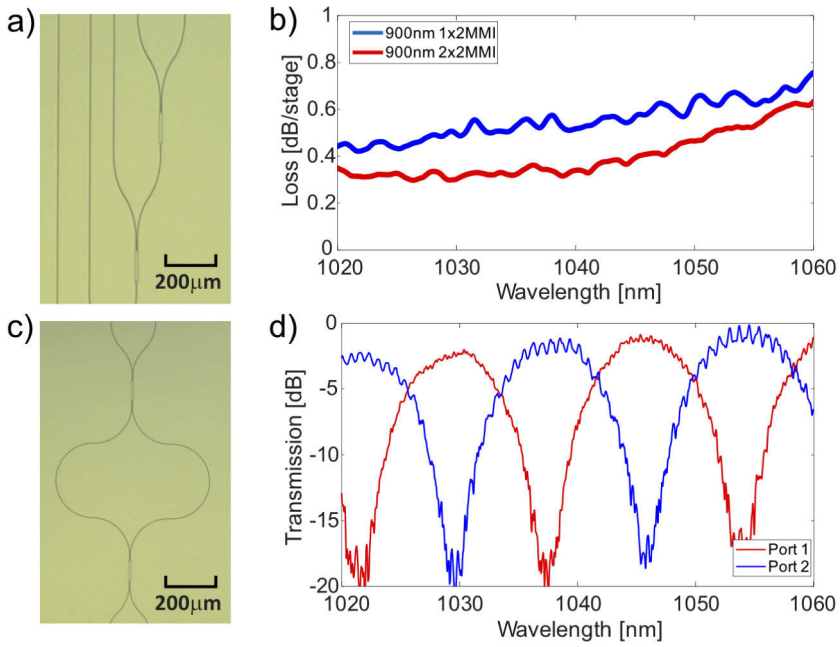

Fig. 8. (a) Optical microscope image of fabricated 1×2 MMIs. (b) Measured total loss per MMI stage. The results for both 1×2 and 2×2 MMIs are included. (c) Optical microscope image of fabricated MZI. (d) Measured transmission of MZI normalized to the coupling loss between the lensed fiber and the chip.

arms with different length. MZIs designed with MMIs are easier to fabricate and have a broader bandwidth compared with Y-junction or directional coupler based MZIs [48,53]. No active control of the phase difference is included in the design for the interference arm. The phase difference comes from the length difference in the arms, which is designed to be 18.4 μm, leading to an FSR of 16 nm. The broadband performance of our MZI will be limited by the bandwidth of 2×2 MMIs [52,53], but it is sufficient to cover the range between 1020-1060 nm.

A microscope image of the fabricated MZI is shown in Fig. 8(c). The radius of the interference arms is 200 μm in order to avoid bending losses in the curved waveguides. The transmission normalized to the coupling loss between the lensed fiber and the chip is shown in Fig. 8(d). The measured FSR is 16 nm and the insertion loss is 1 dB between 1020-1060 nm.

6. Conclusion

We have presented a passive low-loss Si_3N_4 platform in the 1-μm window (1030-1075 nm). It features moderate field confinement, allowing for small bending radii and dense photonic integration. We have introduced a broad library of components, including AWGs, inverse tapers, MMIs and MZIs, and provided a design of an efficient grating coupler with a DBR underneath. The demonstrated performance is compatible with the realization of on-chip wavelength- and space-division multiplexing of multi-wavelength single-mode single-polarization VCSEL arrays, paving the way for the realization of high bandwidth density and energy-efficient Tb/s optical interconnects.

The raw data of the measurement results within this work is accessible in https://doi.org/10.5281/zenodo.3715296.

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