Design and modelling of magnetic on-chip structures at 240 GHz

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***Abstract*— Different magnetic structures including couplers, baluns, and power splitters are designed, simulated and realized in 130nm IHP SiGe Bi:CMOS process. The iterative design procedure employing EM-simulation and computer-aided fitting against an equivalent circuit is described and verified with measurements to be an effective way to design success for passive magnetic on-chip structures. Magnetic components are especially small compared to equivalent circuits using coupled transmission lines enabling tighter integration and lower metal losses. Especially for active devices such as power amplifiers and necessary power splitter or combiner magnetic couplers offer the great advantage of an inherent feeding point for a DC-bias and compactness.**

***Keywords*— Millimetre wave integrated circuits, passive circuits, millimetre wave measurement**

I. Introduction

On-chip structures employing magnetic coupling, primarily transformers and derived components, offer improved system performance and inherent benefits like galvanic isolation and biasing options. However, the necessary structure sizes are linked to the operating frequency, thus making these components expensive in terms of chip space and fulfilling DRC rules. Further, parasitic influences degrade the performance at higher frequencies, which drives designers to employ transmission line structures for their known and proven design methodology.

In the following chapter, the design of a magnetic on-chip balun based on a single transformer design for the use in the 240 GHz band is presented, the design methodology explained and verified by measurements. Likewise, the design methodology is proven to be effective by the design and measurement of a magnetic coupler and a differential power splitter.

All design steps are based on EM-simulating the structures in a 2.5D simulator, such as *Keysight ADS Momentum*. The results are fitted against an equivalent circuit using numerical optimization, which is, in turn, used to evaluate the necessary changes in the physical dimensions to reach the desired performance. Lastly, the necessary matching is added and integrated within the structure itself by modifying the equivalent circuit.

II. Design Procedure

A. Initial design step

The electromagnetic induction describes the basic operating principle of all transformers. This effect is dependent on the magnetic flux, which in turn is dependent on the current through a given surface and the distance between the primary and secondary coil. Hence an optimal transformer consists of infinitely close conductors that run alongside each other infinitely. The impedance a transformer is presenting is a short in the DC case. For an AC stimulus, the impedance results from Lenz law due to the secondary side load impedance together with the mutual self-inductance due to the magnetic field around the conductors.

With increasing frequency, the stray capacitance between neighboring lines is causing two problems: Firstly, it offers a common mode path between both sides degrading the performance, and secondly, it self-resonates with the mutual inductance. Therefore a transformer is only usable up to its self-resonance. This derives a size constraint for on-chip transformers, as both the mutual inductance as well as the parasitic capacitance scale up with the size. Another size restraint is the wavelength: at 240 GHz and in SiO_2 with $\epsilon_r = 4.2$ the wavelength is approximately 610 µm, which gives a rough upper limit to the usability of lumped element fitting approaches[1]. Structures near the wavelength are better modeled as coupled transmission lines.

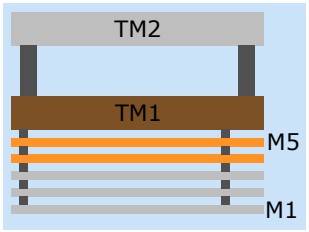

Fig. 1. Metal stackup of the used SiGe process

All further consideration requires knowledge about the used substrate, which for the presented case here is shown in figure 1. The stack-up consists of five thin metal and two thick metal layers. As the closest distance between the two coils is desired, top metal 1 and the combination of metal 4 and 5 are used respectively for the two coils in a stacked manner as presented in [2]. For the first step, a more or less arbitrary coil shape can be used that full-fills the size constraints, a priori knowledge, and the desired function, as depicted in figure 2. This initial layout is EM-simulated at the target frequency band.

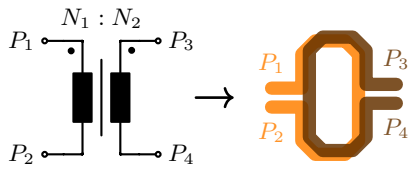

Fig. 2. Transforming a desired component into a layout geometry

B. *Equivalent Circuits*

Based upon the initial EM-simulation, an equivalent circuit is fitted. Over the years numerous models were developed that model on-chip transformers [3][4][5] to various degree of accuracy at high frequencies. Accurate modeling of all parasitic influences, as well as the propagation delay due to the line length, is challenging. The designer has to be cautious not to add to many circuit components as the resulting model becomes an arbitrarily high order polynomial fit rather than a physical representation of a circuit. The chosen generalised model for the presented circuits in this paper is shown in figure 3 and is based upon [4][5]. It models the transformer as four parts, two halves of each side consisting of two coupled inductors modeled as a transformer element and parasitic capacitances. In the generalized form, this equivalent circuit has a large number of free parameters; however, due to layout symmetry, many are linked together. Ports P_5 and P_6 model the center tap connection for DC-bias.

Depending on the coil size the model has to account the increasing transmission line effects. These can be approximated by placing the coil elements marked in red in figure 3 multiple times in series. This also allows to account for asymmetric construction as shown with the balun in figure 4. However, the designer has to be careful not to increase the model complexity unnecessarily.

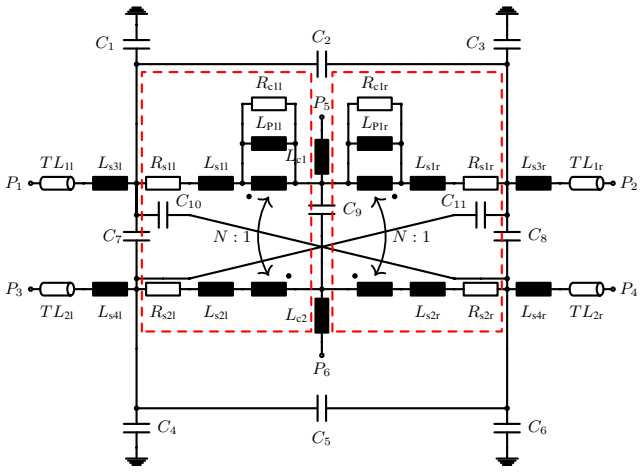

Fig. 3. The generalized equivalent circuit for the transformer

The transmission lines TL_1 and TL_2 as well as the series inductors L_3 and L_4 model the connection to the transformer as in most simulations EM-ports cannot be placed directly at the coil. The transmission lines are modeled as ideal transmission lines to include the phase shift due to the wave propagation. This model is fitted against the EM-simulation by numerical optimization to extract the necessary design elements. The result of the fitting has to be evaluated for physical correctness as there might be more than one fitting solution to the minimisation problem. Bounds to the parameters can be estimated by the layer to layer capacitance specifications for the used process as well as the expected resistances. Numerical approximation will yield higher resistance values as this accounts losses in the substrate.

C. *Iterative design improvement*

The resulting model gives an insight into the black-box nature of EM-simulation and the free layout parameters like the line width and length can be correlated to the model parameter. Tuning and modifying of these parameters is inherently faster compared to EM-simulations. This gives a fundamental understanding of the inherent performance problems due to parasitics as well as the necessary changes to achieve the desired performance. Appropriate changes in the layout, EM-simulation and refitting of the model close the design loop.

Essential to consider in this iterative design are the parasitic elements. They limit the performance and might be prohibitive for the set design goals. Therefore the desired performance goals should be re-evaluated.

One further consideration is the circuit simulation of the model, as well as the EM-simulation. Simulating three-, four- or six-port devices necessitate separate analysis of the even and odd-mode as well as mixed-mode parameters to separate performance problems from lacking coupling from parasitic capacitance.

III. Example Design of 240 GHz Balun

A transformer-based balun is created by shorting P_2 of fig 3 to ground. It is detrimental for decent performance to present an open impedance for the even mode signal on the differential side. This, however, is very problematic at 240 GHz as the parasitic capacitors C_4 and C_6 form a path to ground. Further, due to P_2 being shorted to ground the capacitances C_8 and C_{11} are also connected to ground. Injecting a DC-offset through P_6 will cause another AC-impedance to ground due to the limited inductance L_{c2}. A way to compensate this is to add a capacitor at the center tap such that it resonates in the even mode stimulus with

$$L_{\mathrm{s,even}} = \frac{L_{\mathrm{s2l}} \cdot L_{\mathrm{s2r}}}{L_{\mathrm{s2l}} + L_{\mathrm{s2r}}}. \tag{1}$$

Another method used with the designed balun here is to short P_6 directly to ground and designing the balun to present an AC-short instead of an AC-open, thus losing the ability to add a DC-bias this way and accepting limited performance.

The balun is designed by the aforementioned design steps. The initial layout is shown on the left in figure 4, the final design on the right. Fitting the model against the simulation yields the values presented in table 1. The initial coil design is symmetric, however, due to the values obtained from the model it is clear that the capacitive loading of one half is

Table 1. Initial model values

Parameter	Value	Parameter	Value
R_{s1}	0.4 Ω	R_{s2}	5.92 Ω
L_{s1}	61.2 pH	L_{s2}	43.09 pH
L_{P1}	30 pH	N	1.15
R_{c1}	12 kΩ	K	0.73
L_{s3l}	1.25 pH	L_{s4}	8.42 pH
L_{s3r}	5.7 pH	L_{c2}	0.12 pH
C_1, C_3	0.42 fF	C_4, C_6	8 fF
C_2	0.01 fF	C_5	9 fF
C_7, C_8	0 fF	C_{10}, C_{11}	0.1 fF
C_9	4.3 fF		
E_{TL1l}	17.8° @ 240 GHz		
E_{TL2}	24.7° @ 240 GHz		

higher, therefore the coil is offset in one half as described in [6] to compensate the resulting phase and amplitude imbalance. The center tap of the second coil is grounded, leaving the small strip of ground plane below the balun. The ground plane is open to prevent eddy currents which causes increased losses. A separate version with a patterned ground plane on metal 1 as described in [7] is also manufactured to demonstrate the additional loss. A solid ground plane also poses a problem in fitting the equivalent circuit as it has to be modeled as an additional transformer coupling into a resistance.

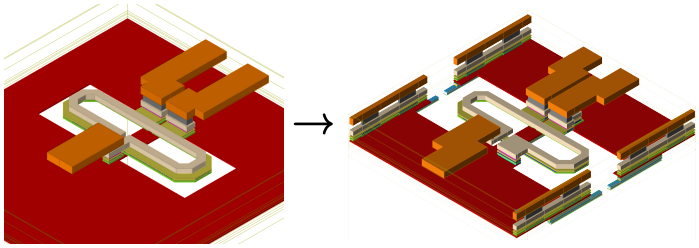

Fig. 4. Layout view of initial balun and end result of design iteration

To compensate the phase and amplitude offset a small 3 fF MOM-capacitor is added at P_4 and placed as close to the end of the coil as possible. The matching circuit was evaluated by matching the equivalent circuit allowing to place a capacitor parallel to C_6, thus allowing to embed the matching within the device itself instead of a separate matching network placed in series.

A. *Verification*

The devices are implemented in IHPs SG13S BEOL run, the chip micrograph is shown in figure 5. Additionally to the balun, a magnetic coupler and folded power splitter are designed and fabricated, their layout is shown in figure 6. The measurements were done in three bands from 1 GHz to 330 GHz with a gap from 170 GHz to 200 GHz. Discontinuities at the band edges are due to the different probing, modules and calibration. To measure the differential structures the baluns are used. The power splitter is placed back-to-back with two baluns, the coupler between two baluns. To measure the balun in the metal only run a 50 Ω all-metal termination consisting only of VIAs and conductors as described in [7] is built. The dimensions were optimized using a 2.5D solver. Its simulated and measured reflection is shown in figure 7. Measurement and simulation match quite well, the offset is due to the pad capacity that is not included in the simulation. The match achieves better than −10 dB matching up to 270 GHz and is therefore suitable to measure the baluns.

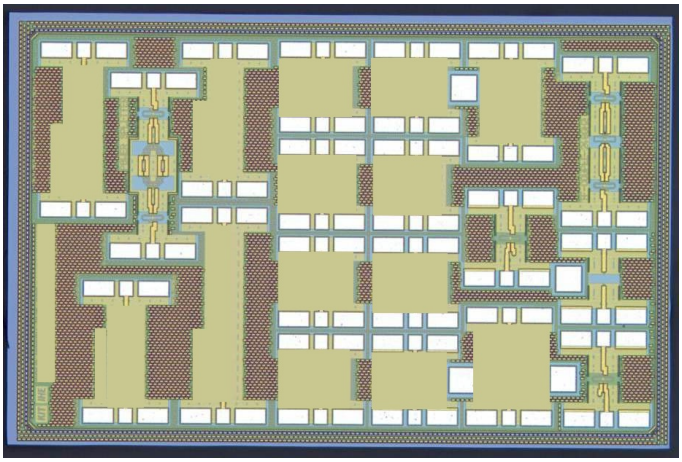

Fig. 5. Chip micrograph of manufactured magnetic components

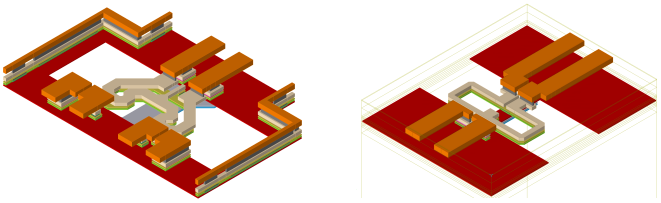

Fig. 6. Power splitter and coupler layout

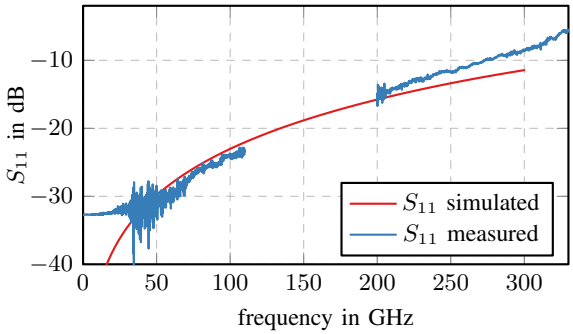

Fig. 7. 50 Ω all metal termination S_{11}

The balun is measured with either side of the differential output matched. This measures amplitude and phase through the balun for either side. Figure 8 shows the simulated and measured amplitude and phase balance as well as the comparison to the fitted model. From 200 GHz to 270 GHz the EM-simulation and the measured amplitude balance match quite well and is close to 0 dB. The phase balance of the

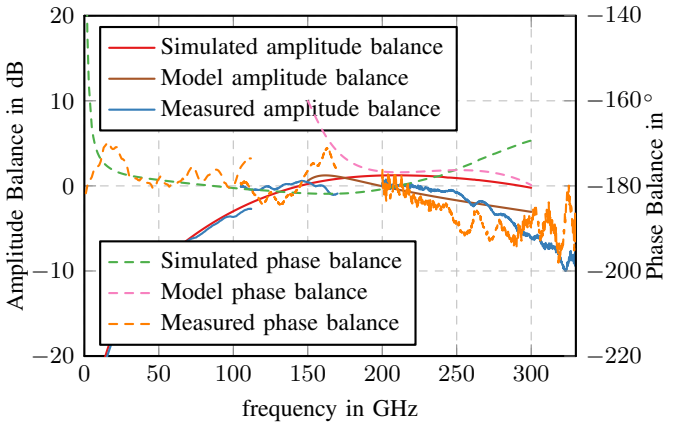

Fig. 8. Measured and simulated balun amplitude and phase balance

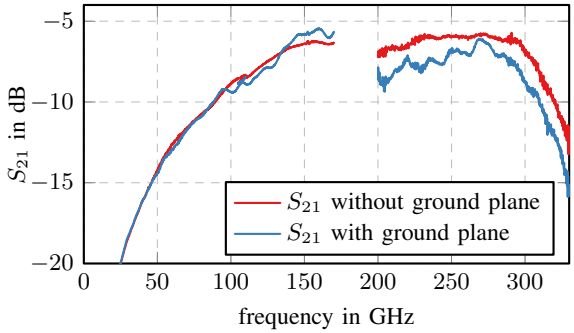

Fig. 9. Measured transmission through balun with and without ground plane

measurement is 20° off, which is rather bad. This, however, can be an artifact of incorrect calibration. The loss through the ablun is about 1.9 dB.

Another aspect considered is the presence of a ground plane. Figure 9 shows the comparison in S_{21} for a balun with patterned ground plane and one without. The ground plane causes about 2 dB more insertion loss at H-band, while showing little to no effect at 0 GHz to 110 GHz. Omitting a ground plane, therefore, enhances the performance of a magnetic balun, however, one has to be careful to avoid substrate coupling, substrate waves or radiation.

The measurement and simulation results for a magnetic coupler is shown in figure 10. In the H-Band a little bit more loss is measured which can be expected. The loss through all stages is −5.8 dB. Subtracting the loss through the baluns the coupler has −2 dB loss.

Figure 11 shows the measurement and simulation of a magnetic 2:1 power splitter. Its insertion loss in a back-to-back configuration matches the simulation quite well. The overall loss is −8.9 dB, the loss in one splitter is therefore 2.55 dB.

IV. Conclusion

In this paper, a design methodology for designing magnetic components in a SiGe BiCMOS process at 240 GHz was introduced. The design iterations were demonstrated on a balun circuit and the resulting layout verified by measurements and good agreement of measurement and simulation was shown.

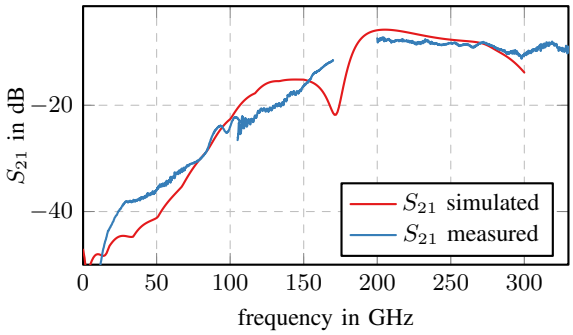

Fig. 10. Coupler with baluns S_{21} simulated and measured

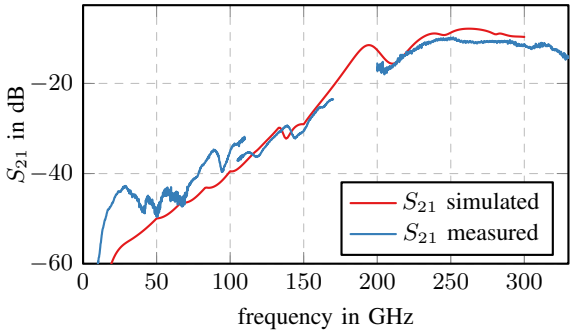

Fig. 11. Power splitter back-to-back with baluns S_{21} simulated and measured

Further components were measured and their accordance with the simulation demonstrated. Overall a good agreement of simulation and measurement for passive components at 240 GHz could be demonstrated.

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