Fast Switching SiC Cascode JFETs for EV Traction Inverters

Ruizhu Wu
School of Engineering
University of Warwick
Coventry, UK
Robert.Wu.1@warwick.ac.uk

Jose Ortiz Gonzalez
School of Engineering
University of Warwick
Coventry, UK
J.A.Ortiz-Gonzalez@warwick.ac.uk

Zarina Davletzhanova
School of Engineering
University of Warwick
Coventry, UK
Zarina.Davletzhan@gmail.com

Philip Mawby
School of Engineering
University of Warwick
Coventry, UK
P.A.Mawby@warwick.ac.uk

Olayiwola Alatise
School of Engineering
University of Warwick
Coventry, UK
O.Alatise@warwick.ac.uk

***Abstract*—This paper investigates the potential performance of high speed SiC cascode JFETs in EV traction inverters with high switching frequencies. Traction inverters implemented with SiC devices have shown improved energy conversion efficiency compared to IGBT based traction inverters however SiC MOSFETs suffer from unstable threshold voltage due to charge trapping at the SiC/SiO_2 (due to high density of traps). Since SiC cascode JFETs combine low voltage silicon MOSFETs (at the input) with high speed/high-power density SiC JFETs (at the output), cascode JFETs combine the electrical gate oxide reliability of silicon devices with the power density of SiC. This paper simulates an EV driving cycle using experimental power loss measurements (at different currents and temperatures) of commercially available 650V SiC cascode JFETs and SiC MOSFETs. The inverter has been simulated at 10, 25 and 50 kHz to investigate the impact of increased switching frequency on device losses. The model is fully electrothermal since conduction and switching losses have been measured at different junction temperatures and used as inputs to the model. The results show the potential of superior performance of the SiC cascode JFET in terms of power loss and junction temperature swings. Furthermore, since higher switching frequencies might be desirable in future high-speed traction motors, the fast switching and low loss performance of SiC Cascode JFETs becomes more attractive.**

Keywords—SiC, Cascode JFETs, EV, Traction Inverter

I. INTRODUCTION

Silicon Carbide (SiC) devices have better energy conversion efficiency than silicon devices in high switching frequency applications such as electric vehicle (EV) powertrains [1]. The first SiC power devices considered for implementation in EV traction inverters was the SiC JFET [2-4]. However, the preference for MOS gated power devices meant silicon IGBTs retained their position as the device of choice in EV inverters. Since, the release of SiC power MOSFETs, there has been significant research on the implementation of SiC based traction inverters for EVs [1, 5-13]. However, there are important reliability and robustness issues like crosstalk [14] and the paralleling devices [15, 16]. A critical reliability issue in the case of SiC MOSFETs is threshold voltage shift from bias-temperature-instability (BTI) [17-19]. Thermal oxidation of SiC results in higher interface and fixed oxide trap density, hence, BTI is more evident in SiC. SiC cascode JFETs combine a low voltage silicon MOSFETs as the gate input with a high speed SiC JFET for voltage blocking as shown in Fig. 1. As the gate of the SiC JFET is connected to the source of the Si MOSFET, the gate voltage of the SiC JFET will be the reverse of the voltage drop on the Si MOSFET, i.e. $V_{GS,SiC\_JFET} = -V_{DS,Si\_MOS}$. In OFF state, the Si MOSFET blocks a voltage which is higher than the absolute value of the SiC JFET's threshold voltage (e.g. -6 V), so the SiC JFET is turned OFF. In the ON state, a positive voltage is applied to the Si MOSFET thus the Si MOSFET is turned ON and its voltage drop becomes almost zero. Because $V_{GS,SiC\_JFET} = -V_{DS,Si\_MOS}$, the gate voltage of the SiC JFET becomes close to zero which is higher than its threshold voltage thus the SiC JFET is turned ON [20]. Using this configuration, the reliability issues caused by the SiC gate oxide are avoided.

The switching performance and reliability of different SiC and Si devices, including SiC MOSFETs, Si IGBTs and SiC cascode JFETs, is evaluated in [21]. However, it is important to study how they will perform in the application and benchmark the impact of adopting a new power semiconductor. This paper investigates the potential performance of newly released 650V SiC cascode JFETs on the power efficiency of an EV traction inverter using Matlab/Simulink with experimentally pre-measured switching losses. For bench-marking, similar rated SiC Trench and Planar MOSFETs are also evaluated.

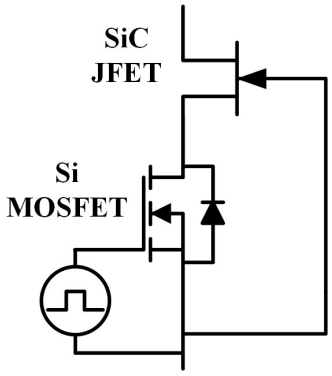

Fig. 1. SiC Cascode JFET device

II. EXPERIMENTAL MEASUREMENTS OF LOSSES

To correctly simulate an EV traction inverter under load conditions, accurate conduction and switching energies are required together with their current and temperature dependencies. While some studies have used datasheet parameters with analytical formulas, in this study, the losses

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are evaluated experimentally at different currents and temperatures for a more realistic set of results.

Three closely rated MOSFET devices of different technologies are selected for comparison on power efficiency in an EV traction inverter, namely SiC Cascode JFET (UJ3C065080K3S), SiC Trench MOSFET (SCT3060AL) and SiC Planar MOSFET (C3M0065090D). The basic parameters are listed in Table I. These devices are designated as the Cascode, Planar and Trench in the rest of the paper for simplified description. It should be noted that the Planar is rated at 900 V while the Cascode and Trench are 650 V. Regarding the current ratings, although they are different at ambient temperature, closer values are found at higher case temperatures which is more aligned to practical condition. It is worth noting that, according to the datasheets, the Cascode has a much higher current density compared to the Trench and Planar. The chip areas are obtained from decapsulated devices and the rated current densities can then be calculated by dividing the stated current rating by the chip area.

TABLE I. DEVICE DATA

	Selected Devices		
	Cascode	***Planar***	***Trench***
Datasheet Reference	UJ3C065080K 3S	C3M0065090 D	SCT3060AL
Voltage Rating	650 V	900 V	650 V
Current rating at T_{case} = 25°C	31 A	36 A	39 A
Current rating at T_{case} = 60°C	27 A	30 A	33 A
Current rating at T_{case} = 100°C	23 A	23 A	27 A
Chip Size	2.92 mm^2	6.05 mm^2	7.79 mm^2
Required device number at T_{case} = 60°C	34	30	28

A. Static Measurement

The datasheet values of conduction losses are verified via static measurements done by passing a DC current of 20 A through the device and measuring the ON-state voltage drop. The experimental circuit for the static measurement is shown in Fig. 2. The ON-state voltages are shown in Fig. 3 (a) where the values match the datasheets. The voltage drop values are approximately 1.8 V, 1.5 V and marginally less than 1.5 V for the SiC Cascode, Planar and Trench devices, respectively. The Trench device has the smallest ON-state voltage as expected because of its higher channel density. The ON-state resistance of the Trench MOS is the most temperature-invariant while the Cascode and Planar rise slightly due to self-heating. Fig. 3 (b) shows the specific ON-state resistances of the three devices. Because of the significantly smaller chip size, the Cascode device has the lowest specific ON-state resistance which is about 3 mΩ·cm^2. It is worth noting that different rated devices from the same manufacture will have almost the same rated current density.

As the datasheet values of ON-state characteristics have been verified in our experimental test, these values and their temperature dependencies will be directly used for power loss calculation.

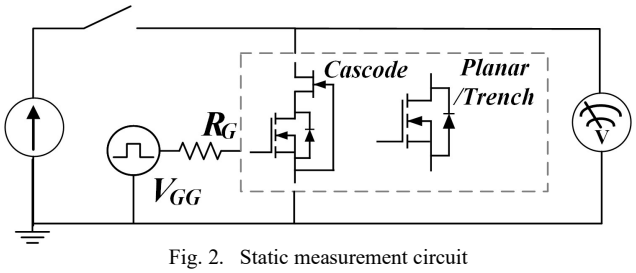
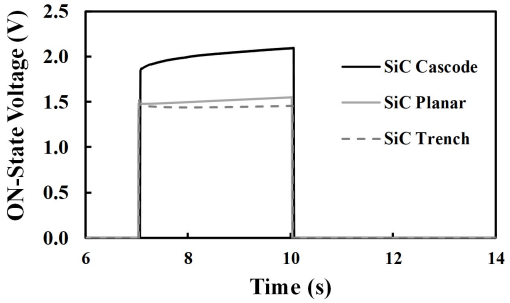
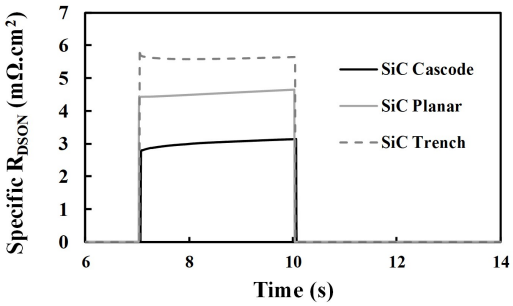


Fig. 2. Static measurement circuit



(a)



(b)

Fig. 3. Experimental result of static measurement: (a) ON-state voltage drops; (b) specific ON-state resistance $R_{DS\text{-}ON}$

B. Dynamic Measurements

Compared to conduction loss, the switching loss of a semiconductor device is more complicated as it is greatly affected by DC link voltage, gate voltage, gate resistance and stray/parasitic inductance. Because different manufacturers have their own measurement set-ups, it is therefore necessary to measure the switching losses of different devices in the same circuit under identical conditions. A double pulse test circuit as shown in Fig. 4 is used for measuring the dynamic characteristics (switching transient) of the selected devices at different currents and temperatures. The DC link voltage is set at 400V and various gate resistances are used but only the results with 33Ω will be shown.

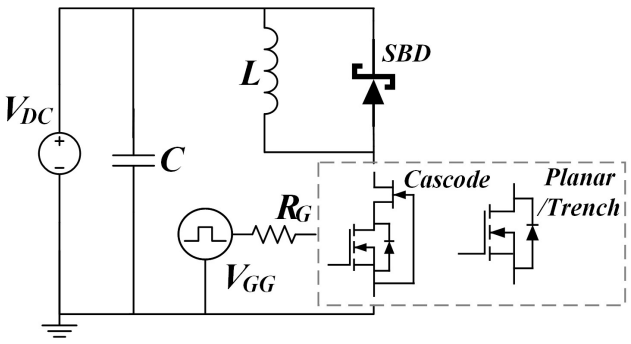


Fig. 4. Dynamic measurement circuit (a double pulse test)

Fig. 5 (a) and (b) show the turn-ON and turn-OFF transients of the three selected devices at 20 A and 75 °C. For high temperature tests, heaters are attached to DUTs (devices under test) and sufficient waiting time (30 mins at least) is applied to ensure the junction temperature get stabilized at required temperatures. Due to different delay times, the turn-ON and OFF of each device starts at different moments. Here, the turn-ON and OFF transients are synchronized so that the slopes can be compared. The solid lines represent device current while the dashed lines represent the voltage across device.

For the turn-ON, the dI/dt of the Cascode and Planar are almost identical while the dV/dt of the Planar is higher. The turn-ON speed of the Trench is the slowest on both dI/dt and dV/dt. In terms of the turn-OFF, the Cascode is the fastest followed by the Planar and the Trench in sequence.

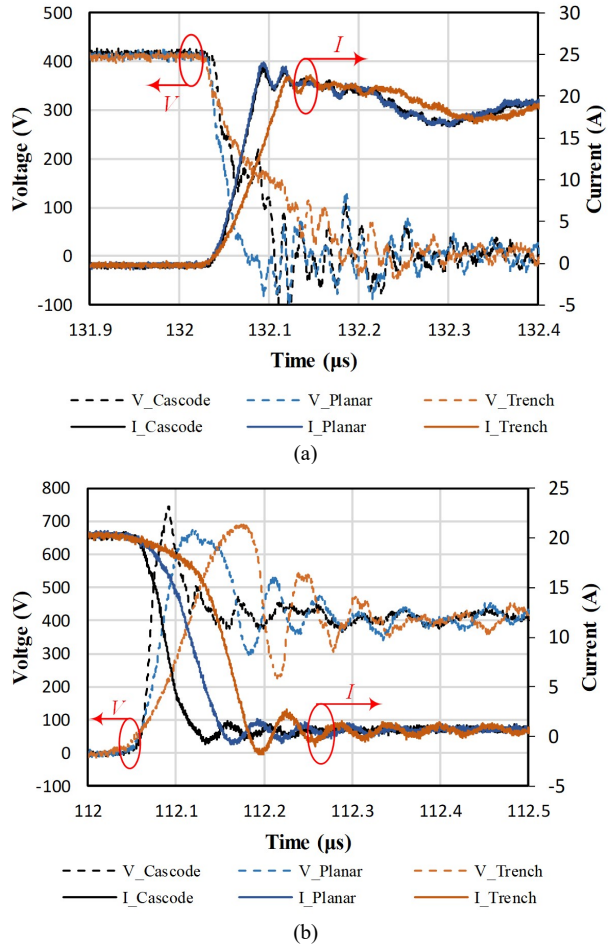


Fig. 5. Votlages and currents of the Cascode, Planar and Trench during switching transients at 20 A, 75 °C: (a) Turn-ON; (b) Turn-OFF.

The fast switching speed makes SiC devices outperform Si devices on the aspect of power efficiency especially at high switching frequencies. As a result, SiC devices will generate less switching losses and could be a good choice for applications that require high switching frequency, e.g. traction inverters for high-speed and low-inductance motors. However, the EMI generation due to high switching speed will require additional EMI mitigation measures. The common-mode current excited by high dV/dt can damage motor insulation [22]. The dV/dt of the selected devices are shown in Fig. 6. The Cascode has significantly higher dV/dt during the turn-OFF and hence, additional measure might need to be taken to motor insulation.

The calculated total switching energies of the three devices (20 A, 33Ω) at different junction temperatures, i.e. 25 °C, 75 °C and 150 °C are shown in Fig. 7. It can be seen that the switching loss of SiC devices are not sensitive to junction temperature. And the Cascode has the lowest total switching loss while the Trench has the highest which corresponds to the information in Fig. 5 and 6.

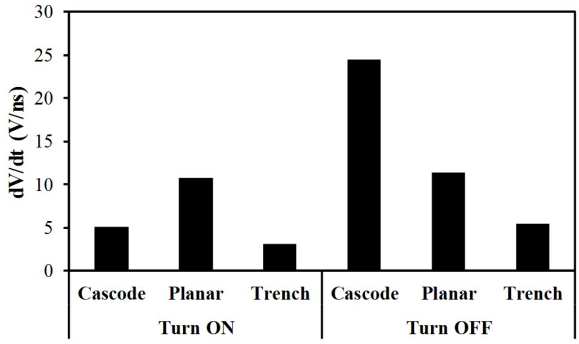


Fig. 6. dV/dt during turn-ON and turn-OFF at 20 A, 75 °C.

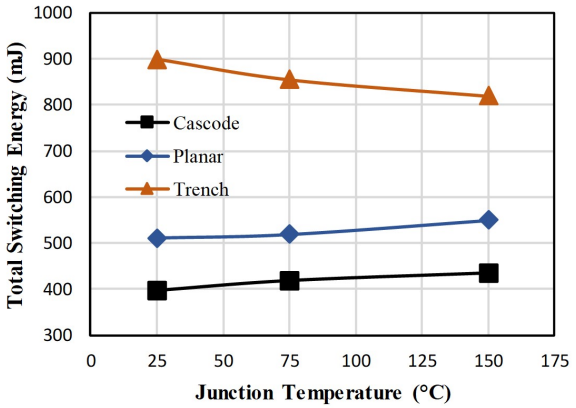


Fig. 7. Total switching losses of the Cascode, Planar and Trench devices

III. EV Powertrain Modelling

The power efficiencies of the selected devices are evaluated in a 3-phase, 2-level voltage source converter as the traction inverter in an EV powertrain. The inverter is directly connected to a permanent magnet synchronous machine (PMSM) which has the maximum power of 300 kW. The DC link voltage is assumed to be stablized at 400 V. The model is implemented in MATLAB/Simulink and the whole system diagram is shown in Fig. 8.

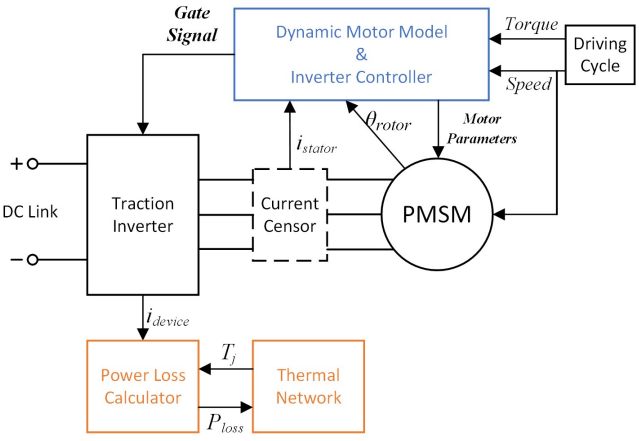


Fig. 8. System diagram

The speed and mechanical torque of the PMSM are the inputs of the model that are from certain driving cycles. The torque and speed are fed into an interacting model including the dynamic motor model and inverter controller which generates gate signal, as its output, for the traction inverter. Then, the traction inverter will provide required voltage and current to the PMSM to generate correlating torque at a given speed from the driving cycle. In this matter, the operating condition of the inverter is simulated. An electrothermal model is built to estimate the power loss in the semiconductor devices in the traction inverter taking into account the junction temperature dynamics.

A. Dynamic Motor Model and Inverter Controller

A more detailed diagram of the dynamic motor model and current controller is shown in Fig. 9. In this study, look-up tables (LUTs) built with experimentally pre-measured motor data are used to determine the operating condition of the PMSM. The flux linkage λ, quadrature and direct inductances (L_q and L_d), and phase resistance R_s are measured with different q and d-axis currents at different speeds. The "Stator Current LUTs" generate the q and d-axis current reference, i_{q_ref} and i_{d_ref}, for a given torque and speed. The "Motor Parameters LUTs", having the motor speed, i_{q_ref} and i_{d_ref} as the inputs, outputs the motor parameters that are dynamically updated in modified Simulink PMSM block. The stator three-phase current, i_{stator} is measured for closed-loop current control. The rotor angular velocity, θ_{rotor} is measured for building synchronous rotating frame to convert the stator three-phase current from stationary coordinates to dq0 coordinates.

A standard PI controller is used to control the stator current. Internal Model Control (IMC) which requires the estimated plant model is used to simplify the control gain selection. As the plant model, i.e. the phase resistance and inductance of the PMSM, are varying with operating condition, it is therefore necessary to update the control gains (related to L_q, L_d and R_s) dynamically. It is worth noting that the phase resistance, R_s varies with operating condition. This is because the AC resistance of the stator coils is rising with the current frequency (rotor speed) due to skin effect.

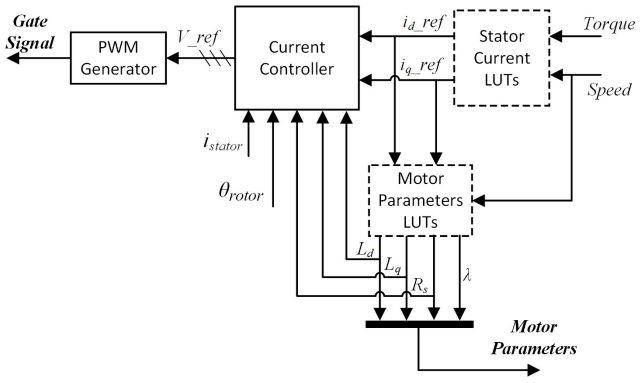


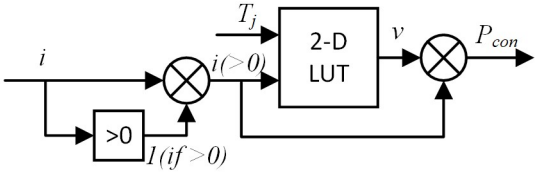
Fig. 9. Dynamic motor model and inverter controller

B. Electro-thermal Model

The power loss of an inverter is dominantly caused by the semiconductor devices inside. In a balanced three-phase system, the power loss in each arm should be identical. Therefore, it is reasonable to calculate the loss of one switch unit to derive the inverter total loss. The semiconductor transistor introduces conduction loss and switching losses (turn-ON and turn-OFF). The free-wheeling diode introduces conduction loss and reverse recovery loss if it is a PiN diode. In this study, the same Schottky barrier diode (SBD) is used for all cases. The SBD has very fast recovery time hence its reverse recovery loss is neglected in this study.

The conduction loss is calculated by multiplying the device current by the ON-state voltage. As the device static characteristics in datasheet have been verified experimentally as shown in Section A, Chapter II, hence the datasheet values are used for obtaining the ON-state voltage. For a given gate voltage, the ON-state voltage is a function of the device current and junction temperature. The recommended gate voltages in the datasheet are used for each device, i.e. 15 V for the Cascode and Planar, 18 V for the Trench. 2-D LUTs with device current and junction temperature as inputs and ON-state voltage as the output are built using datasheet information. Logic operations are required to make the power losses are calculated at the correct time.

Fig. 10 shows the block diagram for calculating device conduction loss. Firstly, the measured device current is multiplied by the output of a logic comparison block to extract the positive component representing the current flowing through the transistor (current flowing from drain to source is defined as positive) or the negative component representing the current flowing through the diode. The logic comparison outputs "1" when the criteria is satisfied and "0" when the criteria is not met. The ">0" comparison is used for transistor while "<0" is used for diode. Then, the extracted component of the device current is fed into the 2-D LUT together with the junction temperature to get the ON-state voltage. The last step is simply to multiply the ON-state voltage by the current to get the power loss.



Using "<0 block" for diode

Fig. 10. Conduction loss calculation

For calculating switching loss, more logic operation is required. As shown in Fig. 11, an "Monostable" block from Simulink library is used against the gate pulse to capture the switching instant and generate a pulse with defined width, T_s which is also the step size of the simulation. When the edge detection is set at rising the block will generate turn-ON pulse, while when the detection is set at falling the block will generate turn-OFF pulse. The next is to multiply the generated pulse by the positive component of the device current to get pulsed current representing the current value at each switching instant. Then, the switching energy can be obtained via the LUT for a given junction temperature and current. The last step is to convert the energy to power by dividing the switching time T_s because the thermal network requires power not energy as the input.

The switching time of WBG devices can be as short as 10 ns in reality. However, it will take too much computing resource to simulate such a small step size and significantly slow down the simulation. In this paper, the switching energy is assumed to be distributed evenly in a pulse width of 2 μs which is considered to be an accurate assumption as the

thermal transfer in the chip has a response time of a few microseconds.

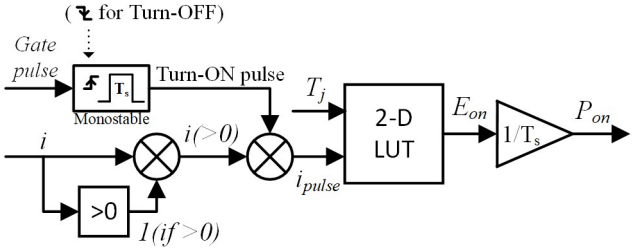


Fig. 11. Switching loss calculation

So far, the calculation methods of conduction and switching losses have been introduced. A conceptual example of the calculated power loss is shown in Fig. 12. As designed, conduction loss is only calculated when there is current conducting while switching losses are calculated only when the device turn-ON or OFF. Finally, the power loss of the transistor and diode will be separately fed into their own thermal networks (either Cauer or Foster) to extract the junction temperatures that are then fed back to the LUTs. The case temperature in this study is fixed at 60 °. By this mean, the electro-thermal model which takes into account the coupling effect of the electrical loss and temperature has been built.

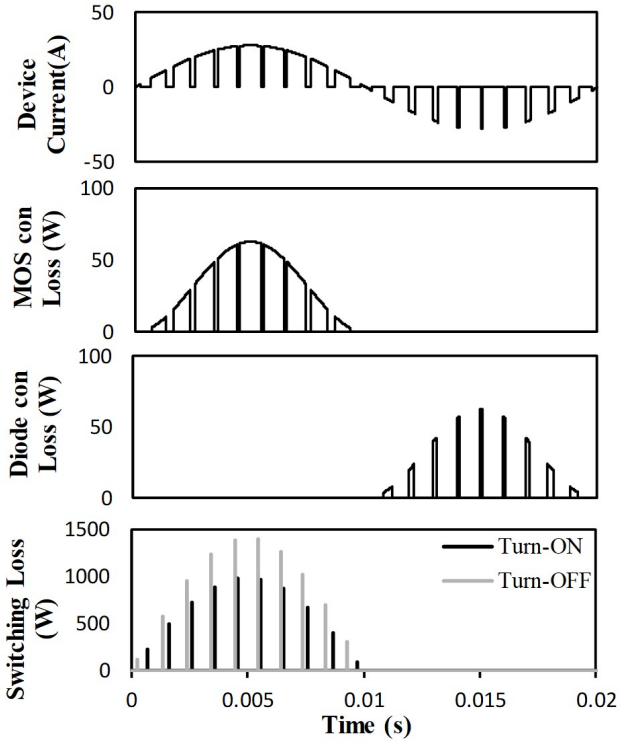


Fig. 12. Conceptual figure of calculated power losses, from top to bottem are: device curret, MOSFET conduction loss, diode conduction loss, Turn-On and OFF losses.

IV. Simulation Results

In this chapter, the simulation results of the inverter power loss and device temperature at different operating conditions will be shown. The first case is a 20 s period from WLTP (Worldwide Harmonised Light Vehicle Test Procedure) driving cycle including acceleration, cruise and deceleration. The second case is a locked-rotor case which is simulated to evaluate the devices under the most stressful condition.

A. WLTP Driving Cycle Case

The vehicle speed, motor torque, stator three-phase current and motor power during the simulated cycle are shown in Fig. 13. In this cycle, the vehicle accelerates from approximately 30 to 50 km/h in the first five seconds and then cruise for about seven seconds. In the last eight seconds, the vehicle decelerates to 10 km/h. The torque tracks the reference very well (the "Torque" line is on top of the "Ref Torque" line) which means the model and controller are working properly as designed.

The four plots are all correlated. In the first part which is an acceleration period, a varying torque up to near 250 N·m is generated in the motor from the input electricity power. The amplitude of the stator current is proportional to the absolute value of the torque. In the second part in which period the vehicle is cruising, small torque, consequently small current and power are required. In the last part representing the deceleration of the vehicle, negative torque is applied to the shaft and an amount of active power is flowing reversely from the motor to the DC link (regenerative braking). The average power losses during this cycle of different technologies with different switching frequencies are shown in the bar chart in Fig. 14 and the correlated junction temperature responses are plotted in Fig. 15.

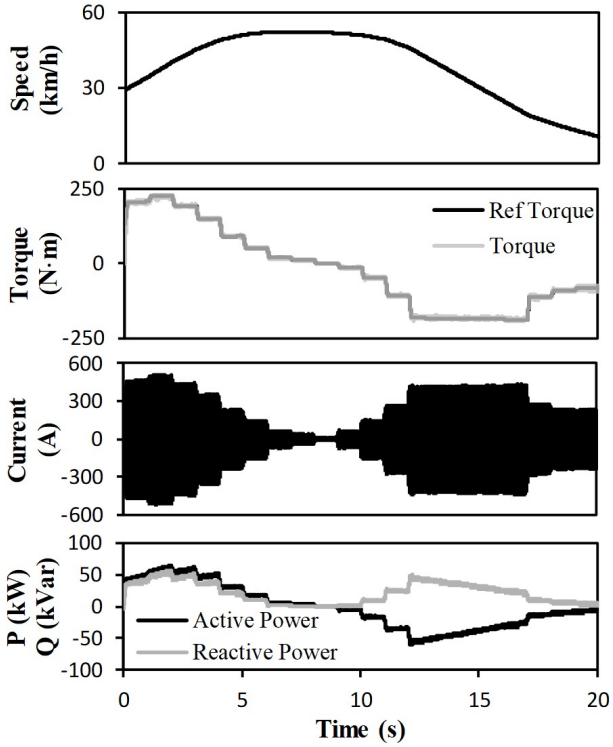


Fig. 13. Operating condition during 960 – 980 s of WLTP driving cycle, from top to bottom are: vehicle speed, PMSM torque, stator three-phase current, active and reactive power input to PMSM.

In general, the Cascode device has the smallest total loss followed by the Planar and Trench. The Cascode has the lowest switching loss but the highest conduction loss. The Trench, in contrast to the Cascode, has the highest switching loss and lowest conduction loss. The losses of the Planar is located in between on both switching and conduction. The

results are correlated to the measurement results in Chapter II. It is worth noting that the diode conduction loss is considerable because in the regenerative braking period the current mainly flows through the diode.

As the performance of SiC devices is not sensitive to junction temperature. The conduction losses of all the three devices marginally increase at higher switching frequencies. However, as a matter of course, the switching loss is greatly affected by the switching frequency. Due to excellent switching speed, the Cascode outperforms the other two at high frequency and the advantage is amplified with the increase of switching frequency.

The junction temperature response simulated by the electrothermal model for the 50 kHz switching frequency case is shown in Fig. 15. The Cascode has the lowest average junction temperature during the whole cycle (62.3 °C) as well as the temperature swing. In the period between approximately 12 to 20 s where the regenerative braking is taking place, the junction temperature of the SBD rises a lot which validates that an increased portion of current is flowing through the diode.

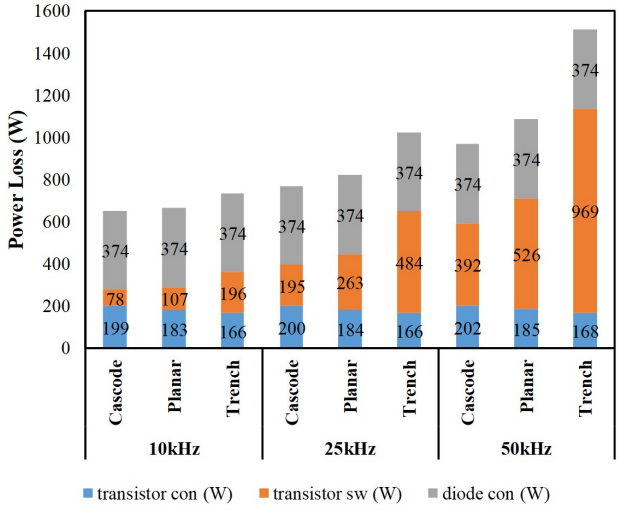


Fig. 14. Average power loss during the driving cycle

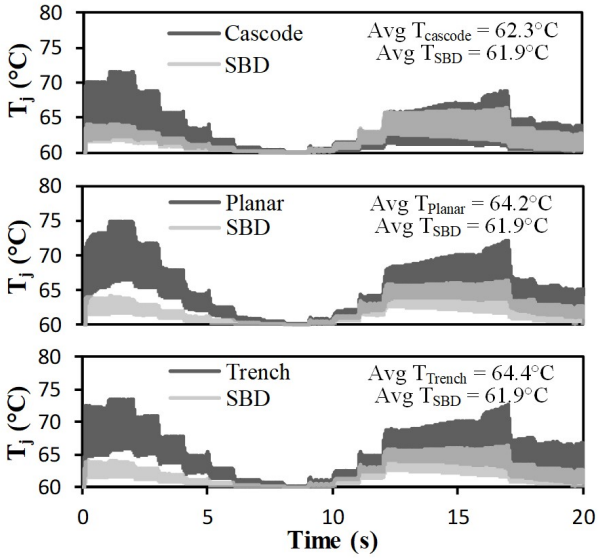


Fig. 15. Simulated junction temperatures at the switching frequency of 50 kHz

B. Locked-rotor Case

In the locked-rotor case, the PMSM is set running at a very low speed (60 RPM) with the maximum torque (350 N·m). This can happen when the vehicle launches while massively loaded. This is the most critical case for the traction inverter because the devices are conducting the largest current and meanwhile having the largest temperature swings due to low fundamental frequency of the current.

The operating condition of a one second simulation of locked-rotor case is shown in Fig. 16. The vehicle speed is less than 1 km/h and the torque is at 350 N·m. The amplitude and frequency of the current are 800 A and 4 Hz. The active and reactive power are about 2.2 kW and 2.5 kVar, respectively. The inverter power loss of different technologies at 10, 25 and 50 kHz are shown in Fig. 17. The overall trend is similar to the previous case. However, as the result of large current, the conduction loss has significantly increased. At 10kHz switching frequency, the Planar surpasses the Cascode marginally (2% less loss than the Cascode) thanks to its lower ON-state resistance. The power loss of the Trench is also competitive at 10kHz due to its excellent conducting characteristics. Nevertheless, at 25 and 50kHz, the Cascode still outperforms the other two as a result of the advantage on switching speed.

The junction temperature responses of the three devices are shown in Fig. 18. The Cascode always has the smallest average value and swing. It means less effort in thermal management is required and smaller swing is beneficial for device lifetime [23].

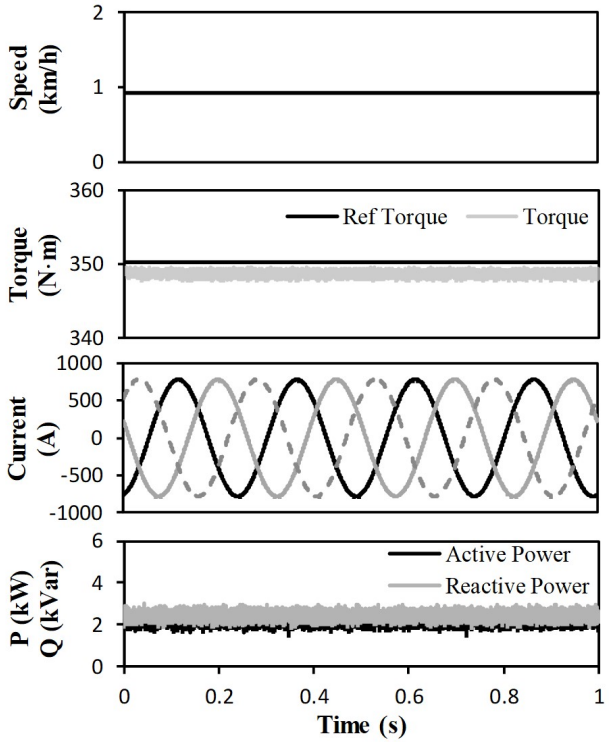


Fig. 16. Operating condition in locked-rotor case, from top to bottom are: vehicle speed, PMSM torque, stator three-phase current, active and reactive power input to PMSM.

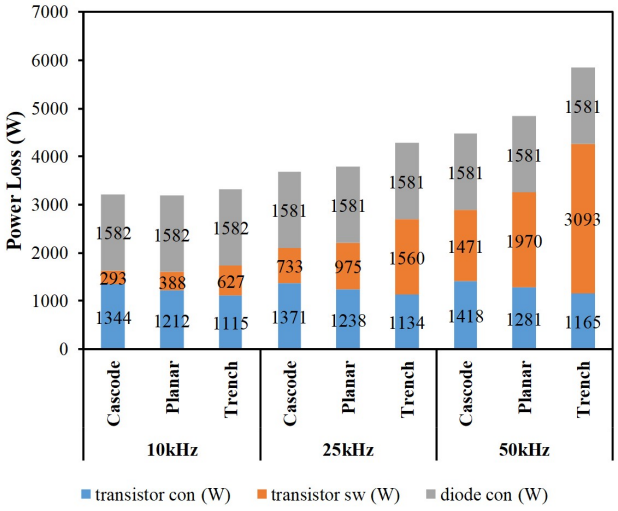


Fig. 17. Power loss in locked rotor case

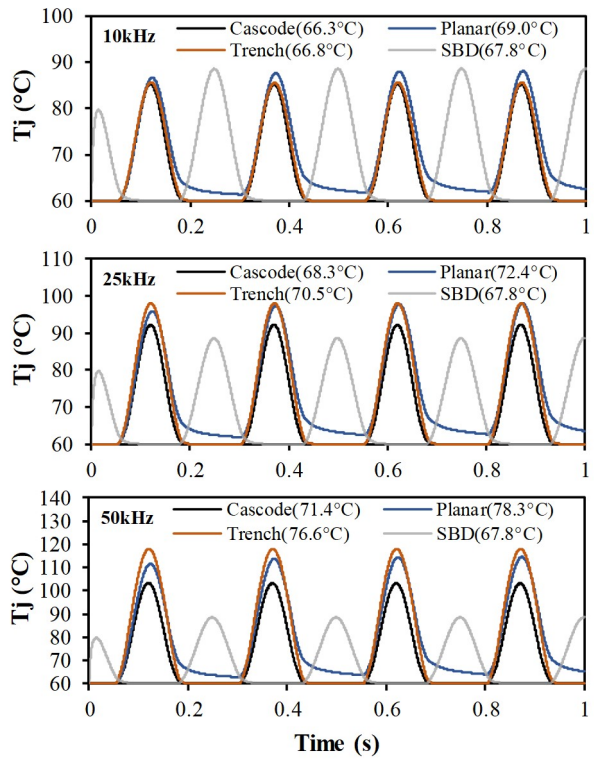


Fig. 18. Simulated junction temperatures in locked-rotor case at different switching frequencies, from top to bottom are: 10 kHz, 25kHz and 50kHz

V. Conclusion

This paper has presented a performance comparison among three latest generation SiC power semiconductor devices via experimental measurement and simulation. The three devices are SiC cascode JFET, SiC planar MOSFET and SiC trench MOSFET. The static and dynamic characteristics are measured experimentally. The ON-state feature is verified by experimental results and the switching performance is tested under identical condition for all the three devices. The Cascode has the highest switching speed and the Trench has the lowest ON-state resistance.

The performance in a traction inverter of EV powertrain is carried out by simulation in MATLAB/Simulink. The results show that, on the aspects of power efficiency and junction temperature, in both general and critical case, the Cascode is the best device among the three despite that the Planar has marginally lower loss at 10 kHz in locked-rotor case. The advantage of the Cascode increases with the switching frequency because of its high switching speed.

In conclusion, this study has presented that, on the aspects of power efficiency and thermal management, SiC cascode JFET has great potential of being used for EV traction inverters. And in addition, SiC cascode JFET avoids the gate oxide reliability issues by using SiC MOSFETs as gate.

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