Reliable 50Gb/s Silicon Photonics Platform for Next-Generation Data Center Optical Interconnects

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Abstract— The next generations of data centers require a scalable optical transceiver technology. In this paper we present a silicon photonics platform supporting single-channel data rates of 50Gb/s and above. Advanced process options include 56Gb/s GeSi electro-absorption modulators, high efficiency thermo-optic phase shifters with P_π <5mW and silicon carrier depletion-based phase-shifters supporting Mach-Zehnder and micro-ring modulators. The performance and reliability of the key library components such as modulators, detectors, fiber couplers and heaters is described.

I. Introduction

The next generations of data centers require a scalable optical transceiver technology to address the projected exponential growth of datacenter networks. Silicon photonics (SiPh) based optical interconnects are progressively emerging as a key technology to support the increase of bandwidth at shorter distances. The SiPh is a cost-effective and high yield manufacturing platform for co-integrating high performance photonics components by leveraging the existing CMOS foundries [1,2,3]. In this paper we present a silicon photonics platform supporting 50Gb/s and above non-return-to-zero on-off keying (NRZ-OOK) data rates. First, we briefly describe the SiPh platform integration standard process based on 193nm lithography and germanium (Ge) selective epitaxy growth (SEG) as well as the extra modules enabling additional functionalities. The third section provides an overview of the key performance metrics for the modulator, detectors, heaters and fiber couplers. The reliability of the active components is reviewed in the last section of this paper.

II. Silicon Photonics Platform Description

A. Process Technology

The imec 50Gb/s SiPh platform technology is based on 200mm SOI substrates with 220nm of silicon on 2000nm of buried oxide (BOX) [4]. The fabrication processes are primarily based on the same tool generation as the 130nm CMOS node augmented with 193nm lithography, Ge SEG and MEMS-like deep silicon etch. The integration flow schematic is provided in Fig. 1. The shallow (70nm), deep (150nm) and fully (220nm) etched waveguides and grating couplers are patterned with 193nm lithography and reactive ion etching (RIE) processes that support features down to 130nm. The silicon junctions are then formed with boron (p-type) and phosphorous (n-type) dopants using ion implantation (I/I) and rapid thermal anneal. The technology supports up to ten implant levels in silicon used for depletion-based Si Mach-Zehnder (MZM) and micro-ring modulators (MRM), Ge photodetectors, GeSi modulators and doped Si heaters. After the Si doping, the Ge detectors are grown using Reduced-Pressure Chemical Vapor Deposition (RPCVD) SEG on silicon followed by Chemical Mechanical Polishing (CMP) and doping by I/I and activation by rapid thermal anneal. The contacts are then formed by the means of a local nickel (Ni) salicidation process (t_{NiSi}~20nm) and 0.25µm x 1.0µm tungsten (W) plugs landing on doped Ge and NiSi. The interconnects are made of two levels of metals, respectively 450nm and 950nm thick, using standard Cu damascene processes. The electrical back-end-of-line (BEOL) process is completed with AlCu bondpads embedded in a SiN passivation layer deposited with Plasma Enhanced Chemical Vapor Deposition (PECVD), which is acting as a moisture barrier. Finally the optical BEOL process consists of locally removing the multiple BEOL dielectric layers and replacing them with ~2.5µm of PECVD SiO_2 to form the top layer of the grating couplers and the inverted tapers edge couplers. The last step is the trench module that includes etching in two steps the optical facet of the edge coupler and an 80µm deep recess in the silicon substrate for fiber access to the etched facet.

One of the key quality factors of an integrated photonics technology resides in the control of the waveguide physical dimensions. The variability of the silicon thickness, the waveguide width and the waveguide coupling space are provided in Fig.2. Particularly important for silicon photonics devices, the overall silicon thickness 1-σ variation is 1.2nm with a within-wafer 1-σ variation of ~0.7nm. Another important parameter is the waveguide propagation loss that is impacted by the roughness of etched surfaces and by the surrounding oxide. Fig.3 gives the optical propagation loss at the wavelength of 1550nm for three waveguide types: (1) 650nm wide, 70nm deep ~0.75dB/cm, (2) 450nm wide 150nm deep ~1.2dB/cm and (3) 450nm wide 220nm deep ~ 1.5dB/cm on par with the state-of-the-art processed with dry 193nm or 248nm lithography.

B. Special components and options

The baseline flow described in Fig.1 (plain bullets) can be complemented or modified with multiple options (hatched bullets) enhancing or complementing the performance of various components. First the Ge SEG can be replaced by GeSi SEG with a Si concentration of ~1% for C-Band electro-absorption modulators. Additionally, a W layer can be inserted between the W plugs and the M1-Cu serving as metal heater which can be positioned directly above an optical device. A third option creates a local cavity in the substrate underneath thermo-optic devices via a local undercut of the silicon substrate below the BOX to reduce the power consumption of the heaters. Finally the edge coupler SiO_2 deposition can be replaced by a 3µm PECVD SiON (silicon oxy-nitride) film that is then further patterned to form a guided edge coupler.

Fig.4 provides an overview of the key devices that are fabricated in this SiPh technology platform. An overview of the performance of the main electro-optical devices is provided in the next section.

III. Device Results

A. Silicon depletion modulators

The layout and cross-section of a reference p-n depletion-based MZM modulator are shown in Fig.5(a,b). The junction is formed with the p and n dopants, the series resistance is reduced with the n- and p-body implants while the low contact resistance is made in the n+ and p+ regions, capped with NiSi. The propagation loss (free carrier absorption) and the carrier-induced refractive index change are antagonist effects proportional to the carrier density [5]. The trade-off between the two effects is provided in Fig.6 for imec's platform. The C-band MZM phase shifter waveguide has a propagation loss of ~12dB/cm and a $V_\pi.L_\pi$~1.45V.cm at 0V bias. The static tuning for a 14nm Free Spectral Range (FSR) imbalanced MZM is provided in Fig.7 and the eye diagrams at 25Gb/s and 56Gb/s are shown in Fig.8 for a 1.5mm long

device that has a 27.5GHz 3dB electro-optical (EO) frequency response. The "50Gb/s" MRM (Fig.9) uses a phase shifter with propagation loss of 77dB/cm and $V_\pi.L_\pi$~0.65V.cm providing a modulation efficiency greater than 50pm/V (Fig.10). This MRM exhibits a 47GHz 3dB EO frequency response enabling open 56Gb/s NRZ-OOK eye diagrams even with a modest peak-to-peak voltage (Vpp) of 1.0V (Fig.11). Imec's platform allows for two phase shifter conditions to be integrated side-by-side.

B. GeSi electro-absorption modulators

Franz-Keldysh GeSi electro-absorption C-band modulators [6] can also be integrated in imec's platform [7]. The p-i-n diode is formed by SEG of GeSi and subsequent p- and n-type doping in GeSi (Fig.12). A 0.8% Si concentration enables operation at 1560nm at room temperature. The 3dB EO frequency response of the device exceeds 50GHz and supports an open eye diagram at 56Gb/s (Fig.13) and even at 100Gb/s NRZ-OOK [8].

C. Ge photo-detectors

The SiPh platform supports both Silicon-Contacted Lateral p-i-n (SLPIN) [9] and Vertical p-i-n (VPIN) (Fig.4(b)) waveguide-based photodetectors (PD) for which a cross-section TEM is given in Fig.14(a). The VPIN PD has an EO 3dB bandwidth exceeding 50GHz at V_{bias}=-1.0V (Fig.14(b)) supporting detection at least up to 50Gb/s (Fig.14(c)) while the SLPIN is used as a monitor photodiode with 10GHz bandwidth . The VPIN PD has a C-band responsivity of ~0.9+/-0.1 A/W and a dark current (I_{dark}) <100nA at -1V bias (Fig.15(a,b)). The SLPIN PD has a responsivity of ~1.1+/-0.1A/W and I_{dark} < 60nA at -1V bias.

D. Heaters

Thermo-optic tuning can be realized either using doped silicon stripes or W wires (Fig.4(c)) and can be used with and without local substrate undercut. The W heaters have a P_π~17.5mW which can be reduced by a factor of 4 when combined with the local substrate undercut (Fig.16).

E. Fiber couplers

The surface fiber coupling is achieved with Si/poly-Si grating couplers [10] with typical single polarization SMF28 fiber-to-waveguide insertion loss of ~2.5dB for both C- and O-band (Fig.17). The inverted taper edge coupler fiber-to-waveguide transmission spectra are provided in Fig.18 when using a lensed SMF28 fiber. The C-band insertion loss is less than 2dB from 1500nm to 1600nm while the O-band insertion loss is less than 3dB from 1280nm to 1380nm when coupled to lensed fiber.

IV. Reliability

A. Ge photo-detectors

2000h high-temperature operation life tests (HTOL) at 175°C and -2V reverse bias (=$2V_{op}$), have been performed on VPIN and SLPIN Ge photo-detectors. The tested VPIN detectors were 13.7µm long and 2µm wide, while the tested SLPIN detectors where 14.2µm long and 400nm wide. Fig.19 shows I_{dark} at -1V as a function of $1/k_BT$, where k_B is Boltzmann's constant, in the temperature range between 25°C and 175°C. The obtained activation energy E_a of I_{dark} at -1V is 0.43eV for both detectors. Fig.20 shows the I_{dark} at -2V and 175°C as a function of time during HTOL. No increase of I_{dark} with time is observed which indicates no degradation. During the HTOL-test, at intermediate times, the I_{dark} at -1V and 25°C is measured and shown in Fig.21. Most of the VPIN detectors show no increase in I_{dark}. One die at the wafer edge shows an increase, but the I_{dark} remains low and within specification. The I_{dark} of the SLPIN detectors shows a small increase from 3.5nA to 11nA (median value). In summary, the I_{dark} at operation voltage remains within specification after HTOL for both types of devices.

B. Silicon depletion modulators

A similar HTOL-test has been performed on silicon depletion modulators, where the stress was done at 175°C with a 5.5V reverse bias. The test structure was a 1.5mm long p-n diode without termination. As the leakage of these devices was too low to be measured in our package-level HTOL-system, the leakage current vs voltage response was obtained before and after HTOL. As can be seen from Fig.22, little or no degradation in I_{leak} is observed, indicating a high reliability.

C. Integrated heaters

Both Si-heaters and W-heaters were tested for their resistance to electromigration (EM). For the Si-heater, a 13µm and 1µm wide line was used. To avoid voiding in the feeder lines, a wide copper M1 line was used and the structure was contacted with 2 rows of 4 contacts at each end of the line. For the W-heater, a 150µm long and 0.6µm line was used. The line was connected to a wide Cu line with an overlap of 1µm. The W-heater was tested with an undercut in the Si under the heater. For each structure, the average heating as a function of current was determined based on resistance R vs temperature T and R vs I-measurements. For the Si-heaters, EM was performed at 3 temperatures between 280 and 330°C and 3 currents between 1.2 and 2.4mA. The failure criterion was set to 10% R-change. For the W-heaters, EM was performed at 3 temperatures between 200 and 260°C and a current of 10mA. Failure criterion was set to open. Typical R-change vs time curves for both structures are shown in Fig.23. For the Si-heaters, a gradual change without line open is observed, where for the W-heaters the lines go to a complete open. Maximum likelihood analyses of the data using Black's model as acceleration factor and the lognormal distribution as distribution of failures times resulted in an E_a=1.53(1.37,1.69) eV, an n-factor=1.81(1.14,2.47) and a σ= 0.43(0.35,0.55) for the Si-heaters and an E_a=1.49(0.66,2.35) eV and a σ=1.73(1.13,1.86) for the W-heaters (the n-factor is not yet determined and assumed to be -1.5 in the extrapolation described below), where the values in brackets represent the 95% confidence interval. For both structures, the E_a is high, which is encouraging from a reliability point-of-view. The high σ for the W-heaters suggests process improvements leading to less variability would be beneficial for reliability. Fig.24 shows the extrapolated lifetime for 1000ppm failures for an operating temperature of 125°C (left axis) and the average line temperature (right axis) as a function of current. To guarantee a 10y lifetime, the Si-heaters can withstand a line temperature of 200°C, where this is limited to 160°C for the W-heaters. Also, the samples had an undercut in the Si under the structure and the impact of this undercut on reliability is not yet fully characterized.

V. Conclusion

We have a presented a silicon photonics platform supporting NRZ-OOK data rates of 50Gb/s and above. We have reviewed the key performance characteristics and the reliability of this complete technology that will support the development of the next generation of electro-optical transceivers.

Acknowledgment

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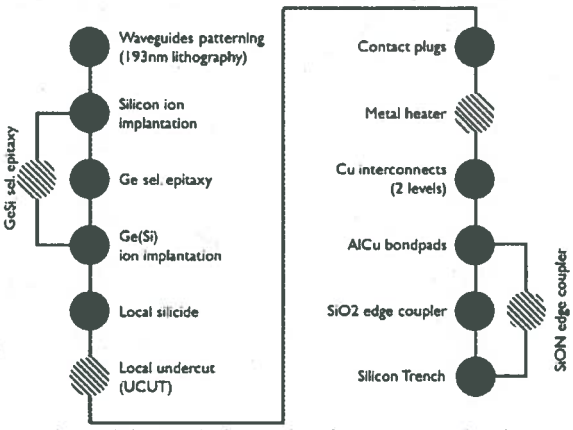

Fig. 1 SiPh process integration flow. The baseline flow modules are represented by plain bullets while the optional process modules are represented by hatched bullets.

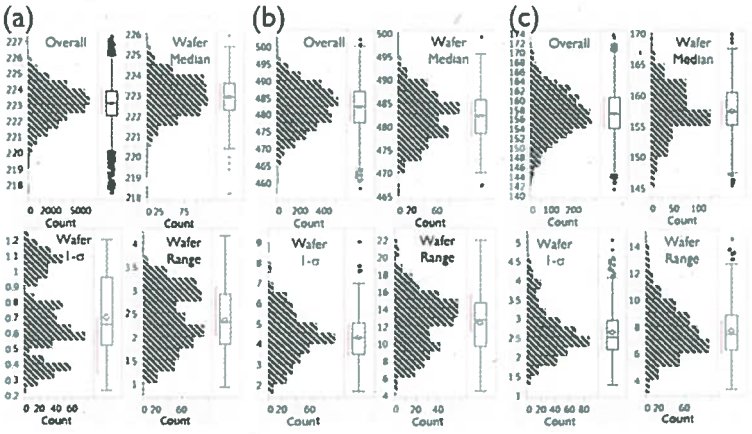

Fig. 2 Waveguide fabrication process control (in nm): (a) 220nm silicon thickness variability, (b) 450nm waveguide width variability and (c) 180nm directional coupler gap variability.

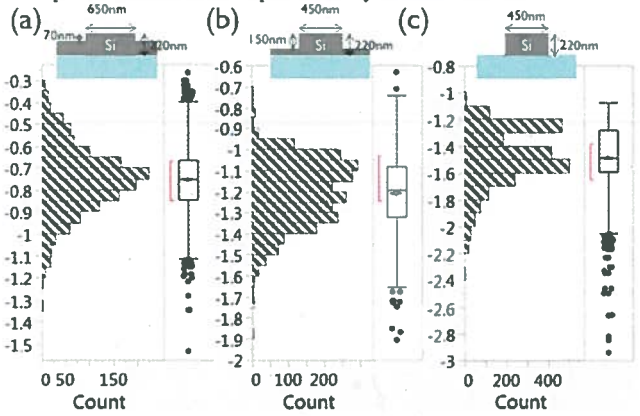

Fig. 3 SiPh waveguides optical propagation loss at 1550nm variability (in dB/cm) for (a) 650nm wide shallow etch (70nm deep), (b) 450nm wide deep etch (150nm deep) and (c) 450nm wide full etch (220nm).

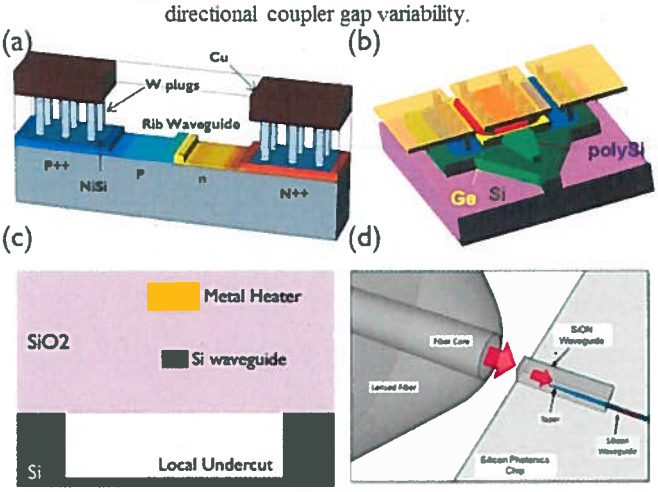

Fig. 4 Schematic of key devices supported by the 50Gb/s silicon photonics technology platform: (a) silicon-based depletion modulators, (b) Ge-based modulators and detectors, (c) thermo-optic metal heater and (d) SiON-based edge fiber coupler.

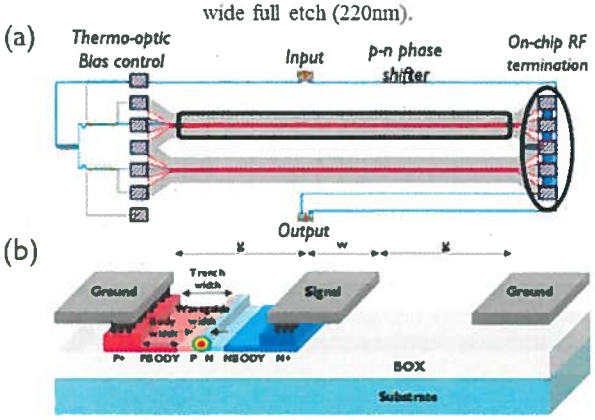

Fig. 5 Depletion-based balanced travelling-wave Mach-Zhender electro-optic modulator with integrated thermo-optic heaters: (a) layout and (b) cross section.

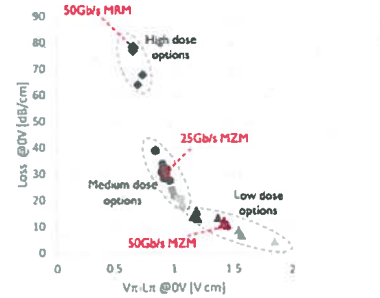

Fig.6 Efficiency (V_π-L_π)-Propagation loss trade-offs for high does, medium dose and low dose for p-n depletion modulators

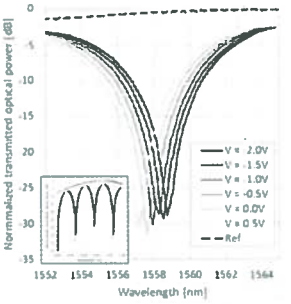

Fig.7 Static tuning of the spectrum of a 1.5mm long imbalanced MZM with applied biases from +0.5V to -2.0V. Inset: wide spectrum.

Fig.8 Eye diagram of a 27GHz MZM operating at 25Gb/s (left) and 56Gb/s (right) for a Vpp=xxV.

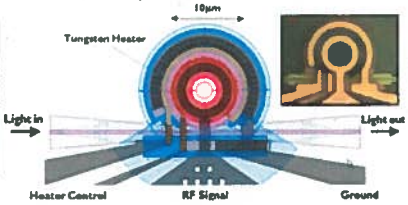

Fig.9 Schematic of a depletion-based 50Gb/s micro-ring modulator (radius=5μm) with an integrated W heater for thermo-optic tuning.

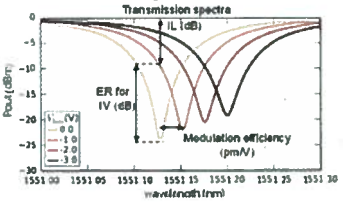

Fig.10 Static resonance tuning of the MRM as a function of applied voltage.

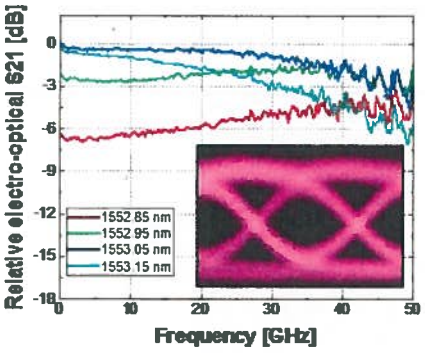

Fig.11 MRM EO S21 response at minimum transmitter penalty wavelength (blue) and away from the that wavelength (others). Inset: 56Gb/s eye diagram at 1Vpp.

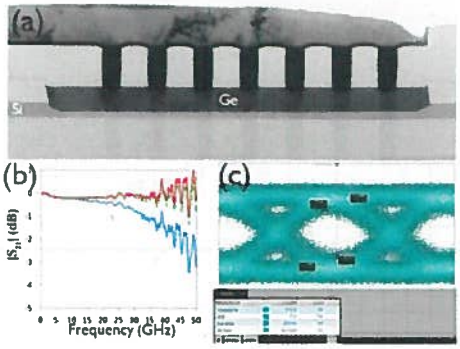

Fig.14 Waveguide-based Ge p-i-n photodetector (a) XTEM, (b) EO S21 response and (c) 50Gb/s eye diagram at Vbias=-1.0V.

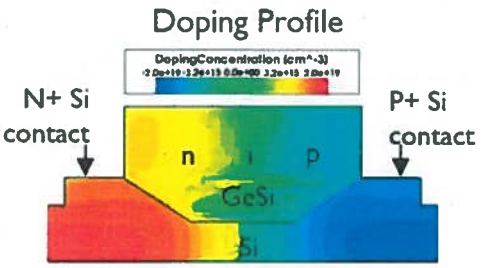

Fig.12 2D dopant profile distribution in reversed bias p-i-n GeSi diode of the GeSi EAM.

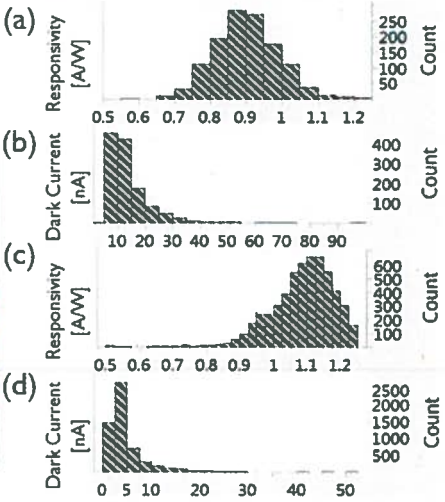

Fig.15 Ge p-i-n responsivity and dark current variability for VPIN (a,b) and SLPIN (c,d) devices.

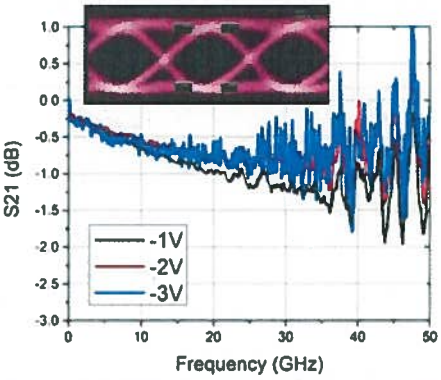

Fig.13. GeSi EAM electro-optical S21 response at minimum transmitter penalty for different voltage bias. Inset: 56Gb/s eye diagram.

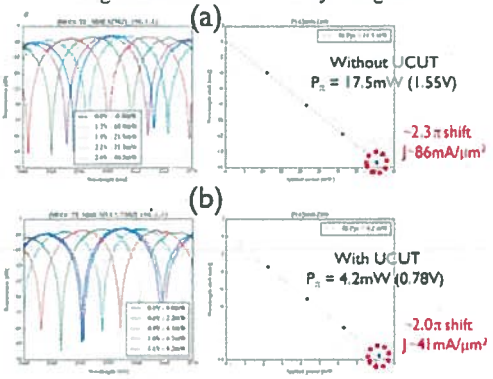

Fig.16 MZ interferometer response for various W heater power for case without (a) and with (b) the substrate undercut (UCUT).

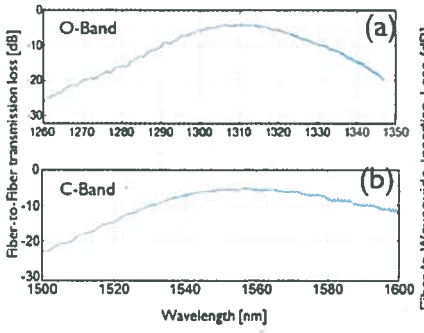

Fig.17 Fiber-grating-waveguide-grating-fiber transmission spectra for O-band (a) and C-band (b) with optimized designs for TE polarization.

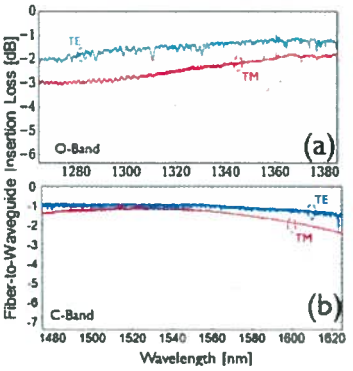

Fig.18 Lensed SMF28 fiber-to-waveguide transmission spectra for TE and TM polarization for the inverted taper edge couplers.

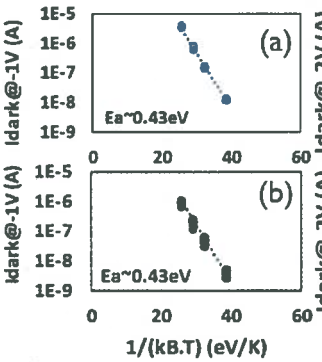

Fig.19 I_{dark} at -1V vs $1/k_BT$ for the (a) VPIN and (b) SLPIN Ge photo-detectors.

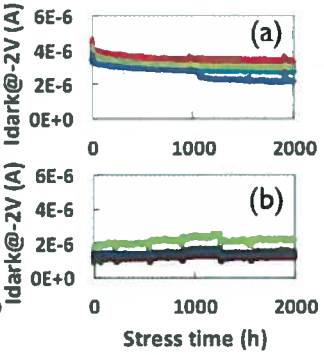

Fig.20 I_{dark} at -2V at 175°C vs time for the (a) VPIN and (b) SLPIN Ge photo-detectors.

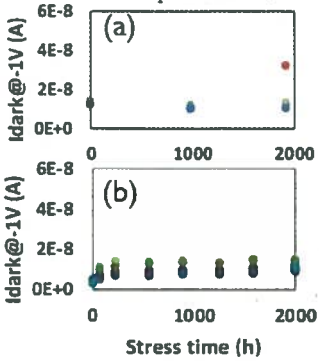

Fig.21 I_{dark} at -1V at 25°C vs time for the (a) VPIN and (b) SLPIN Ge photo-detectors measured at intermediate times during HTOL.

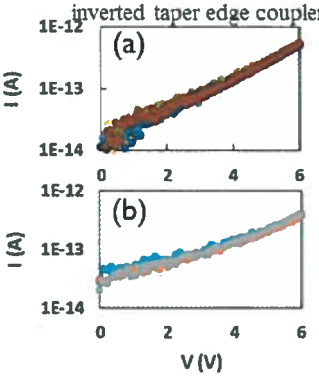

Fig.22 IV in reverse mode of the silicon depletion modulators (a) before and (b) after 2000h HTOL.

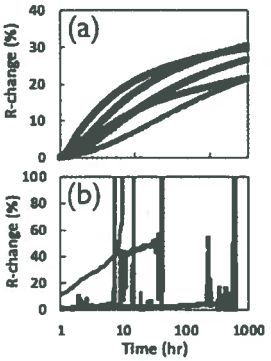

Fig.23 Typical R-change vs time curves during EM for (a) Si-heaters and (b)W-heaters.

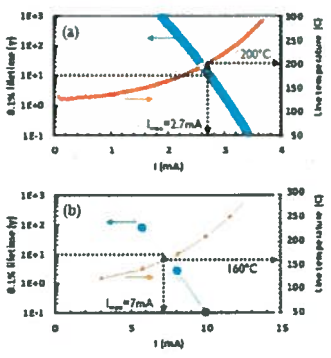

Fig. 24 1000ppm lifetime at Top=125°C (left axis) and average line temperature (right axis) for (a) the Si-heaters and (b) the W-heaters.

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9:05 AM
34.1 Advanced Silicon Photonics Technology Platform Leveraging a Semiconductor Supply Chain (Invited), P. De Dobbelaere, A. Dahl, A. Mekis, B. Chase, B. Weber, B. Welch, D. Foltz, G. Armijo, G. Masini, G. McGee, G. Wong, J. Balardeta, J. Dotson, J. Schramm, K. Hon, K. Khauv, K. Robertson, K. Stechschulte, K. Yokoyama, L. Planchon, L. Tullgren, M. Eker, M. Mack, M. Peterson, N. Rudnick, P. Milton, P. Sun, R. Bruck, R. Zhou, S. Denton, S. Fathpour, S. Gloeckner, S. Jackson, S. Pang, S. Sahni, S. Wang, S. Yu, T. Pinguet, Y. De Koninck, Y. Chi, Y. Liang, Luxtera Inc.

This paper covers a silicon photonics technology platform that leverages a commercial semiconductor supply chain for the manufacturing of high performance optical trans-ceivers for high performance computing and hyper-scale data-center applications.

9:30 AM
34.2 Reliable 50Gb/s Silicon Photonics Platform for Next-Generation Data Center Optical Interconnects (Invited), P. Absil, K. Croes, A. Lesniewska, P. De Heyn, Y. Ban, B. Snyder, J. De Coster, F. Fodor, V. Simons, S. Balakrishnan, G. Lepage, N. Golshani, S. Lardenois, S.A. Srinivasan, H. Chen, W. Vanherle, R. Loo, R. Boufadil, M. Detalle, A. Miller, P. Verheyen, M. Pantouvaki and J. Van Campenhout, imec vzw

The next generations of data centers require a scalable optical transceiver technology. In this paper we present a silicon photonics platform supporting single-channel data rates of 50Gb/s and above. Advanced process options include 50GHz GeSi electro-absorption modulators, high efficiency thermo-optic phase shifters with Ppi

9:55 AM
34.3 Developments in 300mm silicon photonics using traditional CMOS fabrication methods and materials (Invited), C. Baudot, M. Douix, S. Guerber, S. Crémer, N. Vulliet, J. Planchot, R. Blanc, L.