LOW-COST TEST AND CHARACTERIZATION PLATFORM FOR MEMRISTORS

by

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DEDICATION

To My Dad, Richard Jones.

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I have a deep admiration for my advisor, Dr. Nadar Rafla, who advised me and gave me constant encouragement. Dr. Rafla supplied my research with equipment and gave me a sense of belonging to the department. His belief that I could learn anything he put in front of me, and ingraining into me a just “Learn it Attitude”, inspires me today. I would have not completed my course work, and research with personal growth without him being my advisor.

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ABSTRACT

The electrical Testing and Characterization of the devices built under research conditions on silicon wafers, diced wafers, or package parts have hampered research since the beginning of integrated circuits. The challenges of performing electrical characterization on devices are to acquire useful and accurate data, the ease of use of the test platform, the portability of the test equipment, the ability to automate quickly, to allow modifications to the platform, the ability to change the configuration of the Device Under Test (DUT) or the Memristor Based Design (MBD), and to do this within budget. The devices that this research is focused on are memristors with unique test challenges. Some of the tests performed on memristors are Voltage sweeps, pulsing of Voltages, and threshold Voltages. Standard methods of testing memristors usually require hands-on experience, multiple bulky work stations, and hours of training.

This work reports a novel, low-cost , portable test and characterization platform for many types of memristors with a voltage range from -10V to +10V, which is portable, low-cost, built with off-the-shelf components, and with configurability through software and hardware. To demonstrate the performance of the platform, the platform was able to take a virgin memristor from "forming" to operation voltages, and then incrementally change resistances by Voltage Pulsing. The platform within this work allows the researcher flexibility in electrical characterization by being able to accept many memristor types and MBDs, and applying environmental conditions to the MBD, with this flexibility of the platform the productivity of the researcher will increase.

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LIST OF ABBREVIATIONS

BIT	Binary digIT
DAC	Digital to Analog Converter
DC	Direct Current
DUT	Device Under Test
FPGA	Field Programmable Gate
PGU	Pulse Generator Unit
HP	Hewlett Packard
IC	Integrated Circuits
I/O	input/output
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
MBD	Memristor Based Design
O-scope	oscilloscope
PCB	Printed Circuit Board
PCM	Phase Change Materials
SMU	Source Measure Unit
SVM	Support Vector Machine
VCC	Voltage at the Common Collector

CHAPTER 1: INTRODUCTION

Device variability

Electrical testing and characterization of devices that are fabricated on silicon wafers, diced wafers, or package parts have hampered research from the beginning of integrated circuits. This is due to a large variety of devices being developed and modified, that are not well known with different electrical characteristics that require time of the researcher to develop and execute tests, and this time cannot be devoted to the development of the device [1]. The devices considered in this research are memristors, which are two-terminal devices that change resistance as a function of Voltage and retain their resistance when the Voltage is removed [2].

There are a variety of challenges in developing memristors that come from the different mechanisms of changing resistance found in many types of memristors, that may require new or modification of standard electrical characterization methods [3]. Even when memristors have the same mechanism of operation, the life cycle of the memristor from first creation, virgin (high Voltage), to operation (low Voltage) causes multiple electrical test equipment to be used. The changes in the device under test (DUT) and Memristor Based Designs (MBD) require different tooling for the test and characterization process, e.g., direct current in Voltage or current based tooling, and alternating Voltages in time base for pulse-based tools. This creates problems if the test equipment cannot adapt to the DUT or MBD, by requiring the researcher to modifying existing tooling or buy new tooling. Even though there exist some development boards for testing memristors or

MBD, they have limited Voltages, are not flexible for a variety of tests, and cannot accommodate a variety of designs operating under different operating conditions. To increase the productivity of researchers, or even enable a novice to do characterization, the Engineering community needs a flexible electrical test and characterization platform that can be easily automated, possess the ease of re-configuration, accommodate different DUTs and MBDs, be cost-efficient, and be portable when the laboratory environment changes.

Motivation

According to Dave Peterson, a senior test engineer, “Creation of a device is not where the work ends, but where it begins.” Dave Peterson was saying that electrical characterization is a large part of the research for implementation of a device into integrated circuits. Currently, memristor’s electrical characterization is not fully defined to allow implementation into applications. Memristor’s electrical characterizations are largely ignored because of the pressure to create a new memristor in research environments. This is due to the lack of time to learn what electrical characterization is needed, time for test platform setups, and the cost of test equipment.

Problem Statement

The creation of a test and characterization platform that can define the electrical characterization of a memristor is needed. There is a great need for an off-the-shelf, programmable, testing-board that can accommodate different types of DUTs and MBDs, has a large Voltage range, low cost, is easily learned, and can test an assortment of memristor variations with variety of operating characteristics. Such a test platform will cut costs, reduce setup time of tests, and allow generating improved test data, which can

increase research productivity. So, an electrical characterization platform with these attributes will allow researchers to characterize the memristor for applications.

The variety of memristor types make electrical testing challenging. Memristors have different mechanisms to change resistance. Some use conducting filaments that connect two plates separated by an insulator, others use heaters to change the crystalline structure, or use carbon nanotubes [3]. Figure 1.1 shows an example of a cross-section of the mechanism of using the heater to change crystalline structure to manipulate resistance, known as a Phase Change Material (PCM) memristor [4] .

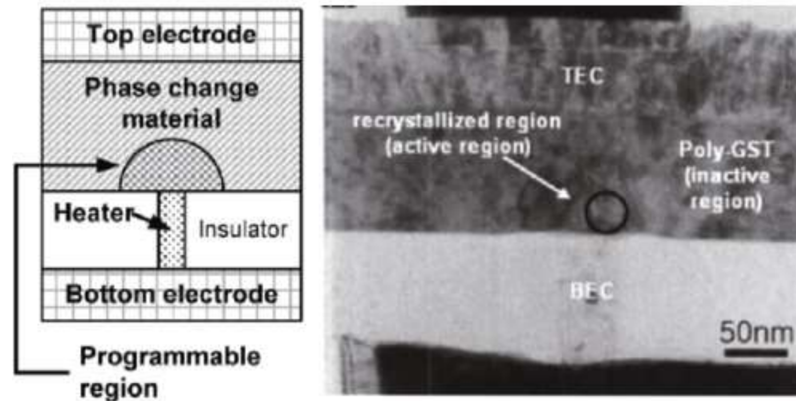

Figure 1.1 Example of PCM Memristor type [4]

The variety of memristors create different Voltages of operation, different current limits that can be applied, add heat components to the setup of the test platform, and these options change how the memristor could be used in MBD (sensor, logic, or weight [5]). All these options will affect the electrical test conditions. Because of this variability of memristor types, they can have operating characteristics that can be classified as unipolar (only positive Voltage operation), near unipolar (mostly positive Voltage operation) and bipolar (positive and negative Voltage operation), as listed in Table 1.1 [6].

Table 1.1 Memristors Operating Voltages Polarity [6].

Polarity	**Voltage Operation**
Unipolar	Only positive Voltage operation
Near unipolar	Mostly positive Voltage operation
Bipolar	Positive and negative Voltage

These operational differences require a new flexible electrical test and characterization platform which is modular in design, and with software operating the test platform that can be updated easily.

Current test platforms can only accept a limited number of different DUTs and MBDs, and this limits the tests that can be performed. The MBD could be configured as a Voltage divider, a circuit element, an array of memristors, a logic setup of memristors, a feedback controller, and a detection method [7, 8, 9, 10]. These MBDs require flexibility of the test and characterization platform to propagate a signal with signal access points for an oscilloscope (O-scope), and feedback circuits for the controller of the test platform. An MBD needs to be easily replaced while protecting its connection to the Voltage source of the test platform. Having flexible DUTs allows the researcher to run the same tests for different configurations of MBDs (single, logic and array), test conditions (heat and radiation), and at different stages of the manufacturing process and packaging of the memristors (partial fabricated, wafer level, die, or package die). In conclusion, current test and characterization tools are inadequate to accept the variety of DUTs and MBDs that are constructed.

Another issue of electrically testing and characterizing memristors in an experimental lab environment, is that the test platforms currently used are for conventional types of devices like transistors, resistors and so on. Having no particular tool that is

specifically designed for memristor testing, researchers spend time deciding which test and characterization platform could perform the test needed, as well as time spent training for the characterization tool. This process re-occurs until the researcher has a battery of tests to perform [11]. This battery of test solutions is spread out over many electrical test platforms and often are only available in different lab locations. The movement among these labs may require a reservation for the test platform if not owned by the researcher, access to the lab if not their own; even just moving a DUT or MBB from one test platform to another requires time. In addition, performing the full battery of tests developed may require a long time. The execution of the battery of tests takes time away from the development of a memristor device or design, so often only minimal electrical tests and characterization can be done on the devices to allow more time for development. So, electrical testing suffers: too little testing, too little verification, and too little integration of the device into a working system. Therefore, a new electrical test and characterization platform is needed to be able to perform many types of characterization, i.e., Voltage pulsing and Voltage sweeps.

Impacts of memristor life cycle on electrical characterization

Memristors can have different operating Voltages in their lifecycle. Memristor devices that are tested in this research are ionic devices in chalcogenide glass. This type of memristor has states of electrical performance in the lifetime of the device that require application of different Voltages across its terminals. When an ionic memristor is first made, it requires high positive Voltage to decrease its resistance in many types of ionic memristors, and within this research, this state is referred to as a “virgin device”. The next stage of the device is to cycle the resistance, i.e. apply positive Voltage across the

memristor terminal to obtain a low resistance, then a negative Voltage for a high resistance. The cycling of resistance is to stabilize the operating Voltages, and this is referred to as "forming" [12]. Once the memristor is "formed", it can be used in "operational mode". In "operational mode", direct current (DC) characterization will have an equivalent threshold Voltage (rapid decrease in resistance with rapid increase in current) paired with a standard negative Voltage to reduce resistance and a constant maximum allowed current, known as "current compliance". Characterization of a memristor in a pulsing environment, in "operation mode", will have a similar movement in resistance when a pulse (positive or negative) is applied from a similar starting resistance. So, the electrical test and characterization platform must have not only a large enough Voltage to decrease resistance for many types of memristors throughout their lifecycle, but also necessary negative Voltage to increase the resistance, and with the ability to pulse the DUT or MBD [13].

Thesis Organization

The thesis organization is structured as follows: Chapter 2 describes the memristor theory, polarity, and types of memristors, with a survey of the operational Voltages of the types of memristors. The type of memristor that will be used in this research, with the fabrication and layout of the memristors used is presented in Chapter 3. Chapter 4 describes singulation of a silicon wafer into its packaging with initial DC Voltage sweeps. Chapter 5 describes the pulse generating station that was used to understand the Voltage pulsing over a memristor to enable the characterization and test platform. The characterization platform requirements, design, list of parts, results, and conclusion are in Chapter 6.

CHAPTER 2: A REVIEW OF OPERATING VOLTAGES AND LITERATURE

Introduction: Memristors

Memristors have different operational Voltages because of the type of memristor used to change the resistance, the fabrication methods of the type of memristor, the geometric shape of the memristor, the impurities introduced into the memristor, the materials used in the memristor and the electrical connections to the memristor. To design a test and characterization platform that is successful for the researcher, the platform must encompass as many types of memristors and the variations of each type of a memristor as possible. To achieve a global test and characterization platform for memristors, this chapter will review memristor theory, the equations that govern the change of resistance, the polarity variations of memristors, and the types of memristors, as well as operating Voltages.

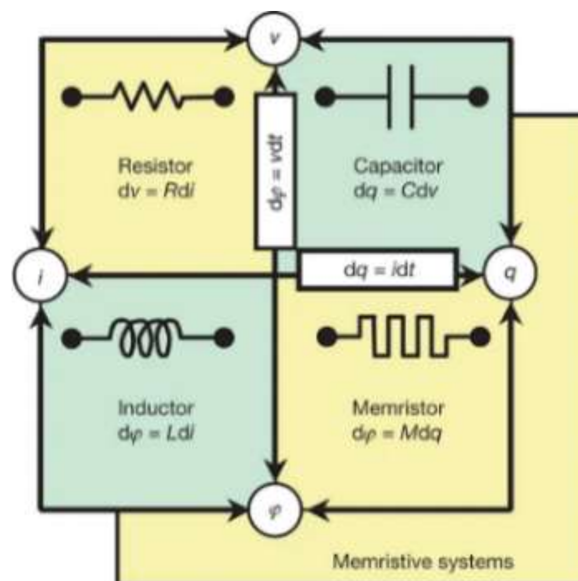

Figure 2.1 How a Memristor fits with a Resistor, Capacitor, and Inductor [14].

Memristor theory had its origin with Leon Chua when he published "Memristor-The Missing Circuit Element" in 1971 [2]. Chua described how a memristor, a two-terminal device, fits into the other three basic electrical elements (resistor, capacitor, and inductor), by bridging flux and electric charge as illustrated in Figure 2.1 [15].

Figure 2.2 shows Chua's curve for charge and the flux in a non-linear relationship based on the memristor which bridges flux and charge. But it is not reasonable to use flux and charge to change the resistance of a memristor, because most applications will not have those sources. So the equations will be put in terms of current and Voltage, as most applications of memristors will use these sources.

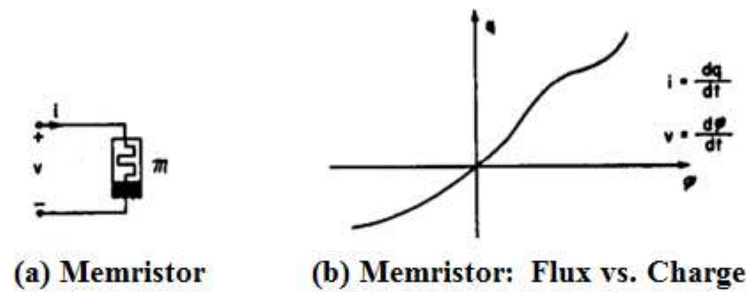

Figure 2.2 Chua's Memristor and its Φ-q Curve [2]

The given equations by Chua [2], (2.1) and (2.2), shows current (i) equal to charge with respect to time and Voltage (v) equal to flux with respect to time, respectively. M is the memristance for equations (2.3) to (2.6). But within this work, memristance is equivalent to the resistance at a certain time of the memristor. Examining "instantaneous power dissipated by memristor" as shown by Chua, equation (2.3), shows that dividing $[I(t)]^2$ into $v(t)i(t)$ yields equation (2.5). Substituting equations (2.1) and (2.2) into equation (2.5) generates equation (2.6). Therefore, the memristance is affected by forcing current or Voltage across the memristor.

$$i = \frac{d\mathrm{q}}{dt} \tag{2.1}$$

$$v = \frac{d\Phi}{dt} \tag{2.2}$$

$$p(t) = v(t)i(t) = M\big(q(t)\big)[i(t)]^2 \ (Instantanous\ Power) \tag{2.3}$$

$$M(q) = \frac{v(t)i(t)}{[I(t)]^2} \tag{2.4}$$

$$M(q) = \frac{v(t)}{i(t)} \tag{2.5}$$

$$M\big(q(t)\big) = \frac{d\Phi_m/dt}{dq/dt} = \frac{v(t)}{i(t)} \tag{2.6}$$

The Voltage-current characteristics described above by Chua's theory and formulas, illustrated in Figure 2.3, demonstrates the standard pinch hysteresis [16]. Chou's theorem, Passivity Criterion, proves that a change in Voltage or current the resistance is change of the memristor is continuous. The equations and the generated I-V curve give the researcher a guide to memristors' behavior according Chua's theory. But as different memristors have been developed, they show different shapes of their I-V curves and their operating polarities.

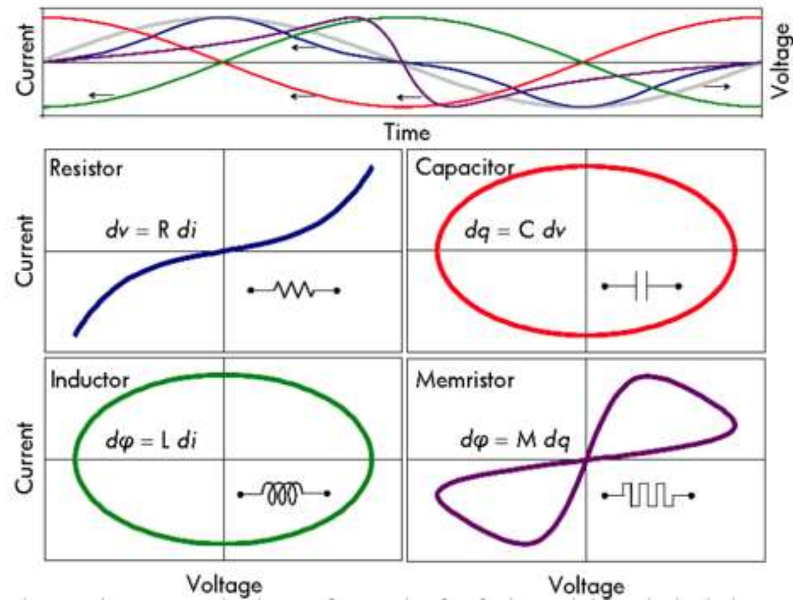

Figure 2.3 I-V Curve of a Resistor, a Capacitor, an Inductor, and a Memristor [16].

The Polarity of Memristors

Chua's theory shows the polarity of the operating Voltage as bipolar, as positive Voltage and a negative Voltage to change resistance. Memristors can also display a unipolar behavior in the operating Voltage, as described by Akikhito Sawa [17]. Another category introduced in this research is a near unipolar category to fill the gap of memristors that need a very small Voltage to decrease resistance. The test and characterization platform must be able to perform within these Voltage polarities, as described by the forcing Voltage and the measuring current (I-V) in the graphs below.

Figure 2.4 shows a bipolar memristor's I-V characteristics. Figure 2.4 Label "1" on the graph, the Voltage increased from 0 to a positive Voltage. When the Voltage reaches V_{TH_1} on the graph, a rapid increase in current happens, this is known as the threshold Voltage (V_{TH}), labeled "2". The rapid increase in the current is the result of the resistance of the memristor rapidly decreasing because of the Voltage potential across the memristor.

At Label "3" on the graph, the Voltage is swept back to 0 with no change in the slope, which indicates that the resistance stays constant. On the graph labelled "4", the Voltage is swept from 0 to a negative Voltage towards V_{TH_2}, a rapid decrease in current takes place as the result of a rapid increase of resistance. The decrease of current is the result of a rapid increase in resistance of the memristor induced by the negative Voltage. For the rest of this work, V_{TH_1} will be the threshold Voltage when the current increases rapidly, and V_{TH_2} will be the threshold Voltage for when the current decreases rapidly.

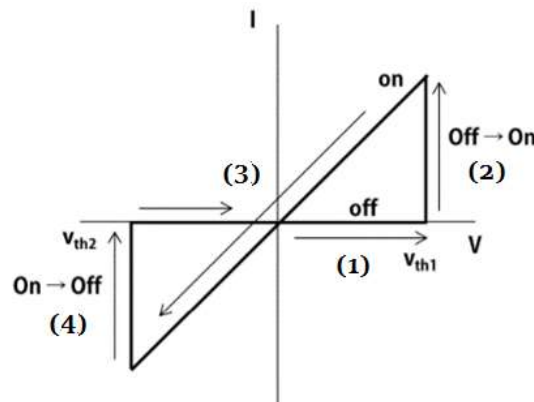

Figure 2.4 Voltage Sweep Measuring Current: Bipolar Memristors [18]

In a unipolar memristor, the device can be brought to high resistance or low resistance in one Voltage polarity, as shown in Figure 2.5.

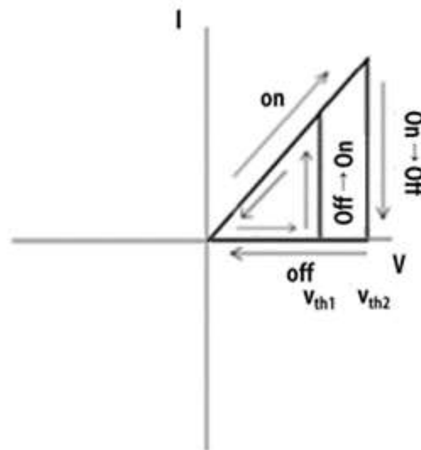

Figure 2.5 Voltage Sweep Measuring Current: Unipolar Memristors

The thresholds Voltages, V_{TH_1} and V_{TH_2}, are within the same polarity of negative or positive Voltage. The Voltage is driven to V_{TH2} and then rapidly dropped to 0 Volts to increase the resistance of the memristor, and then to decrease the resistance of the memristor the Voltage is driven to V_{TH1} [17, 19].

With different construction methods of memristors, a bipolar device, Figure 2.4, can have a much lower V_{TH_1} amplitude than V_{TH_2} amplitude showing a near unipolar Voltage operation characteristic, as shown in Figure 2.6. By having such a low V_{TH_1} the near unipolar memristor will have lower power consumption, but be more susceptible to negative Voltage noise in the circuit.

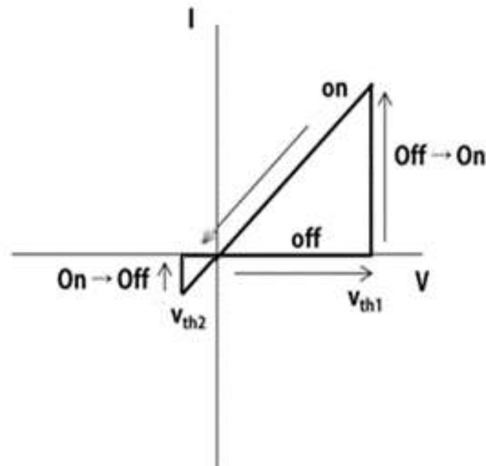

Figure 2.6 Voltage Sweep Measuring Current: Near Unipolar Memristors

Types of Memristors

The first device published as a memristor was a bipolar device shown in the magazine *Nature* in 2008 in the article, "The missing memristor found". The bipolar device was produced in the Hewlett Packard laboratories [15]. The HP memristor, anion type (described later in this text), sparked a race to create new memristors. These new types of memristors and different fabrication methods within the type of memristors have

different operating Voltages and polarities. To define the electrical output of the test and characterization platform, a review of the publications on the types of memristors, as well as their operating Voltages and their polarities will be discussed below. Table 2.1 contains a list of the types of memristors with their corresponding mechanisms, and operating Voltage range.

Table 2.1 Types of Memristors and Operating Voltages

Types	Mechanism	Operating Voltages
Anion	Oxygen vacancies, and negatively charged oxygen ions.	-0.7 to 3.7
Cation	Conductive bridging, reox reaction and migration of metal ions with a positive charge	-1 to 1
Carbon-based	Carbon Nano-tube bundles or carbon switching layer (Carbon-DLC).	-3.7 to 4
Spin and Magnetic	Electron spin as the switching mechanism.	-1.5 to1.5
Thermal	Crystalline state to induce high/low resistive state.	0 to 2.2

Anion Memristors

In 1962 Hikmott observed resistive switching with an anion mechanism [20], that was documented well before Chua's memristor theory was published. Resistive switching is defined as creating a low resistance path in an insulator from an anode to a cathode. Some of the reasons the device created by Hikmott was not acknowledged as a memristor at the time of Chua's publication, were that the device was large, and it had a negative resistance that was not allowed under Chua's theory. As the cation device (memristor) advanced, the first implantation was as memory that was call resistive random access memory (RRAM) in the 2000s [21, 22].

Anion memristors are a sandwich of materials containing a bottom and a top conductive plate with oxide base material in between. The variation in resistance is achieved by generating oxygen vacancies and displacing oxygen ions, as illustrated in Figure 2.7 [15, 17, 23, 24, 25].

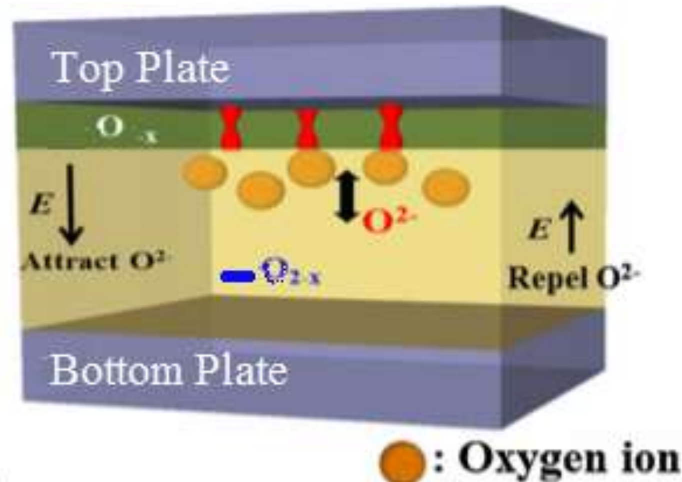

Figure 2.7 Anion Memristor's Operation [17]

To lower the resistance, oxygen vacancies must form a conductive path from the top plate to the bottom plate. To regain a high resistance, the oxygen ions will recombine with the vacancies. To build an anion memristor, there is a requirement of a layer that is rich in oxygen ions and a depleted layer that are metal oxides and doped oxides. The anion oxygen base memristor is split up into anion and cation memristors, and is usually bipolar in operation. Examples of metal oxide depletion layer chemistries are: WO_X, HFO_X, TaO_X, TiO_x and AlO_X [15, 26, 27, 28, 29]. Doped oxide and silicon-rich oxide [30] is an oxide material that has been sputtered with impurities of metal or silicon. This allows the same mechanism of low and high resistance shown in Figure 2.7 [31]. Some of the metal-

doped oxide memristor chemistries are $Ta:SiO_2$, $Cu:SiO_2$, $Pt:SiO_2$, $Zn:SiO_2$, and $Ni:SiO_2$ [32, 33, 34].

An example of an anion memristor with metal oxide films is a memristor that was fabricated by HP laboratories. The HP memristor is a type of bipolar anion memristor. The HP memristor was fabricated as a Titanium-Dioxide Titanium vertical sandwich. The bread, or outer layers of the sandwich, are the top electrode (TE) and bottom electrode (BE) made of Platinum, shown in Figure 2.8 [15].

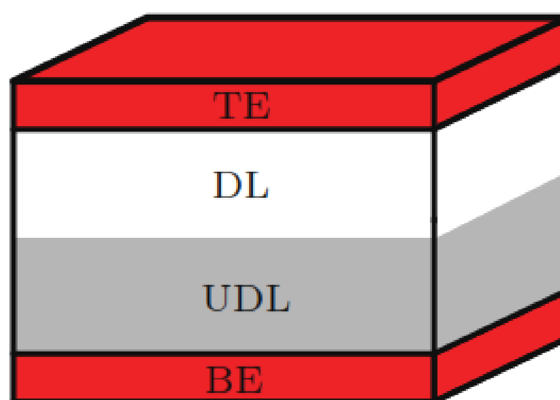

Figure 2.8 Vertical Sandwich of the HP Memristor [15]

The DL, in Figure 2.8, is the doped layer with plentiful oxygen vacancies, and the UDL has fewer vacancies with a one to one ratio of Titanium and Oxygen. When "write" Voltage or low resistance Voltage is applied, the oxygen vacancies will migrate to the UDL. This will decrease the resistance by a magnitude or several magnitudes, creating an "ON" state. A reverse Voltage potential, "erase" Voltage, will reverse the direction of oxygen vacancy drift, migrating them toward the DL, creating a high resistance "OFF" state of the device. The diagram below, Figure 2.9, demonstrates the "ON-OFF" states of the Titanium dioxide memristors [15].

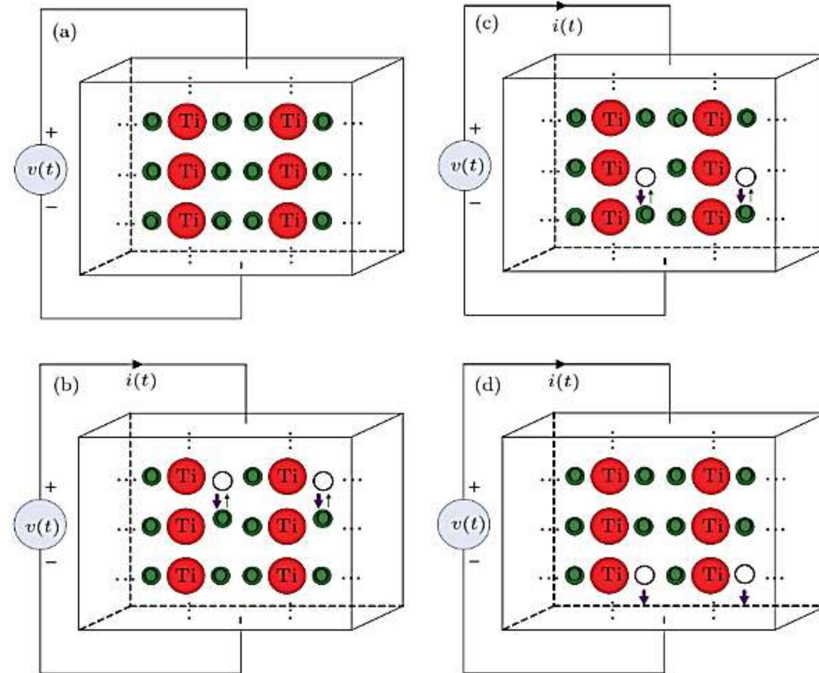

Figure 2.9 Diagram of the Electrical Operation of Titanium Dioxide Memristors [15]

The waveforms generated below show the electrical characteristics of the HP memristor. Figure 2.10 shows a Voltage sweep in time and current that demonstrates memristor behavior, in a pinched hysteresis. The highest operating Voltages of this type of memristor is under positive one Volt to negative one Volt.

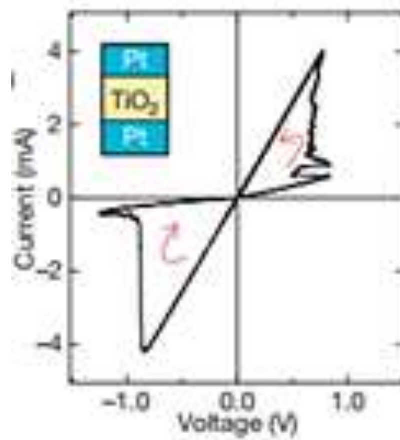

Figure 2.10 I-V Characteristics of Titanium Dioxide Memristors [15]

Some anion memristors have operation Voltages from zero to approximately 3.7 Volts. The unipolar device shown in Figure 2.11 was fabricated out of a sandwich of TiN/Zr0.5Hf0.5O2/In-Ga-Zn-O (or TiN/ZHO/IGZO) on a flexible substrate of mica [35].

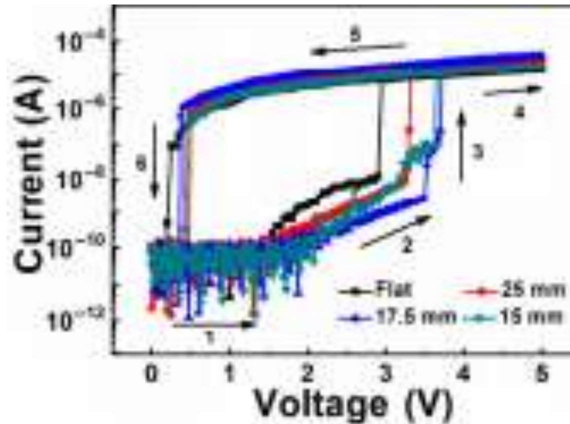

Figure 2.11 TiN/ZHO/IGZO Flexible Anion Memristor: Flexed with IV (0 V→5 V→0 V (with the Numbered Arrows 1→2→3→4→5→6) [35]

Cation Memristor

A cation memristor is based on a metal filament, grown and reversible, to bridge two metal plates separated by an insulator [36]. Cation memristors were developed at Arizona State University by Professor Michael Kozicki and his research group in the 1990s [37, 38]. Micron and Infineon announced cation memristor development in the early 2000s [39], and in 2011 Adesto Technologies was developing a cation memristor in memory. Adesto marketed the cation memristor as a conductive-bridging RAM (CBRAM) that was sampled memory in 2013 [40].

A cation memristor takes advantage of solid-state Ionics, and their performance is based on an electrochemical oxi-reduction process. Using thin layers, a metallic bottom plate (Electrochemically Inert) is created with an insulating middle layer and then a metallic top plate that is ion donating [37]. The ion donating film has highly mobile ions

and high electrochemical potential. After Voltage potential is placed on the two thin-film electrodes, ions start to move across the insulating barrier to the bottom plate, where the ions undergo a reduction on the bottom electrode to become a metal. The metal builds in the direction of the electrical field towards the top plate, creating a filament (Examples: Ag or Cu) to connect the bottom plate to the top plate, and changing the resistance by orders of magnitude, as seen in Figure 2.12 [41].

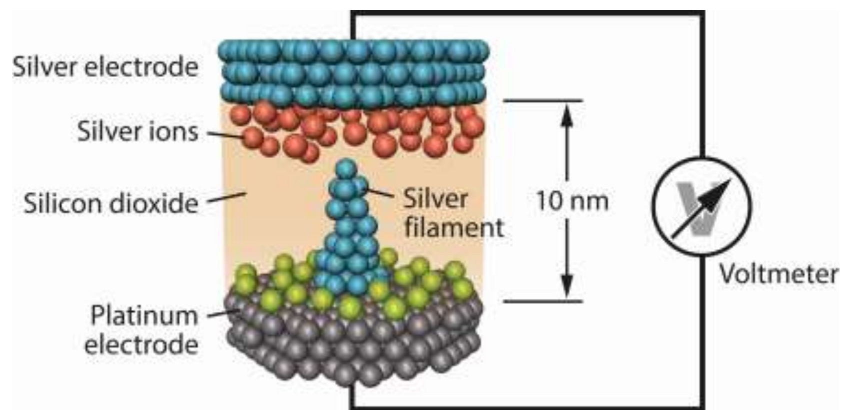

Figure 2.12 Filament Forming in a Cation Memristor [41]

A reverse Voltage potential is applied across the device to bring the device to a high resistance. Then the silver filament deconstructs into silver ions and recombines to the silver electrode [41].

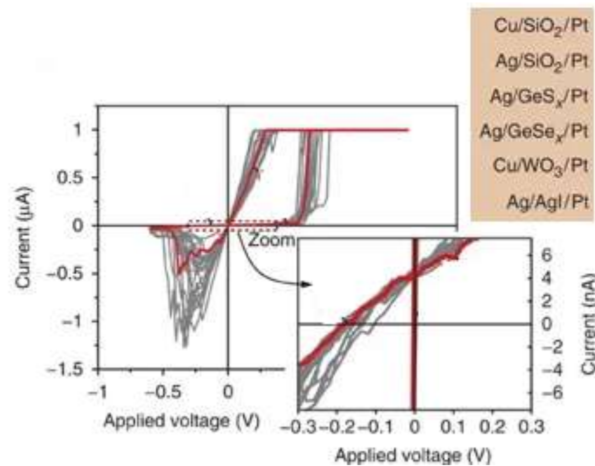

Figure 2.13 Different Cation Memristor Voltage Sweeps [41]

The positive operational Voltages of a typical cation memristor are no more than one Volt with a negative of Voltage no more than negative 0.7 Volts, as seen in Figure 2.13.

Carbon-based Memristor

In 2009, the carbon oxide switching memristor was first published by He et al [42]. The carbon switching layer is an insulator so that a filament can be formed between the conductive plates. A carbon bundle based memristor was published in 2011 by A. Radio et al [43]. The carbon nanotubes used in the device are composed of silicon carbide (SiC), that were arranged in Vertically Aligned Carbon NanoTube arrays (VA CNT), as shown in Figure 2.14 [44]. The nanotubes use stress to affect current when a Voltage is applied to create memristor characteristics.

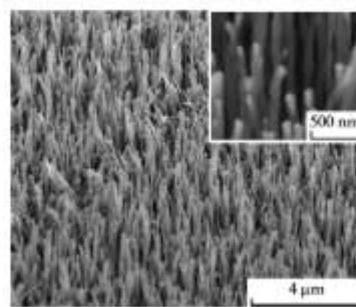

Figure 2.14 Scanning Tunneling Microscope of Vertically Aligned Carbon Nanotube Array [45]

In carbon bundle based memristors, the conducting tip of the Scanning Tunneling Microscope (STM) induces an electric field and is brought near to the VA CNT to create bundles, shown in Figure 2.15 (a) and (b). The Voltage is swept on the tip of the STM and then this induces a stress on the bundle. This stress of the bundles causes a current flow of the tip from the STM. The current and Voltage on the tip are measured and graphed.

This graph has the shape of a pinch hysteresis curve, which is shown in Figure 2.16. If the probe tip Voltage potential is reduced to zero at any time of the hysteresis curve, the bundle will retain the induced stress [46, 45]. The operating Voltage range of the carbon nanotube memristor is negative 1.25 Volts to .75 Volts.

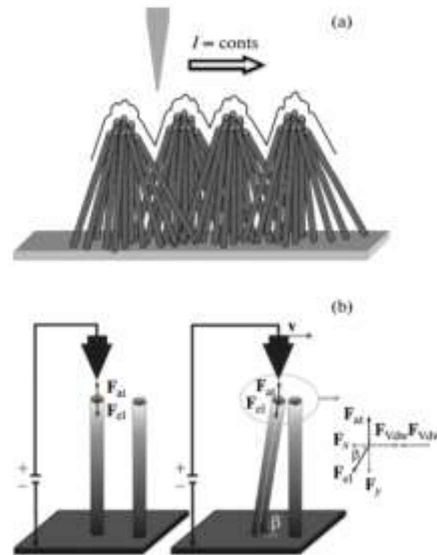

Figure 2.15 Bundling of Carbon Tubes [45]

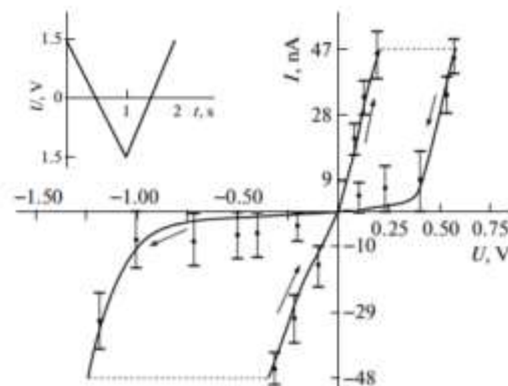

Figure 2.16 Electrical Characterization of Tip [45]

Carbon-based memristors that have a switching layer of Diamond-Like Carbon (DLC) use conductive filaments to change resistance. The fabrication of the DLC memristor has two metal electrodes with a DLC layer between the electrodes. There are

several different variations of these types of carbon sandwiches, and some of these variations are shown in Figure 2.17, from the publication ”Resistance Switching Induced by Hydrogen and Oxygen in Diamond-Like Carbon Memristor” [47]. The figure shows a hydrogen-induced (Single-active-Layer) conductive filament and an oxygen-induced conductive filament (Double-active-Layer) with the order of the layers adjusted to understand the electrical characteristics of each variation. Figure 2.18 shows the electrical results of the pinched hysteresis curve in log scale, showing the impact of fabrication changes in the shape of the I-V curve and the operating Voltages. The operating Voltage range in this publication is from -1.5 to 0.7 Volts [47]. In another publication, “Memristive devices based on graphene oxide”, a variation of fabrication methods resulted in operating Voltages of - 3.7 Volts to 4.0 Volts [48]. Within memristor types, it shows the importance of fabrication methods to the electrical operation of the memristor and the electrical characterization of the memristor.

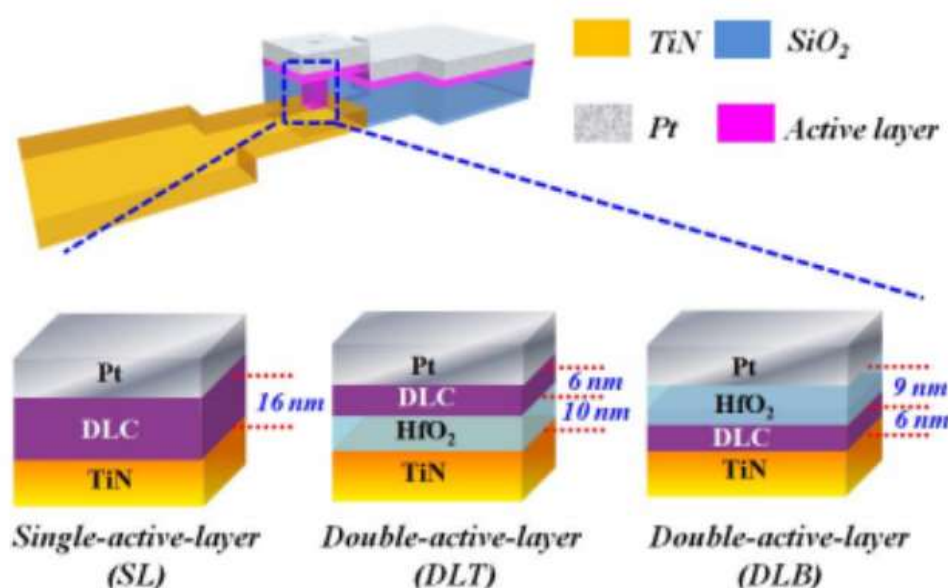

Figure 2.17 Some Types of Carbon Memristors [47]

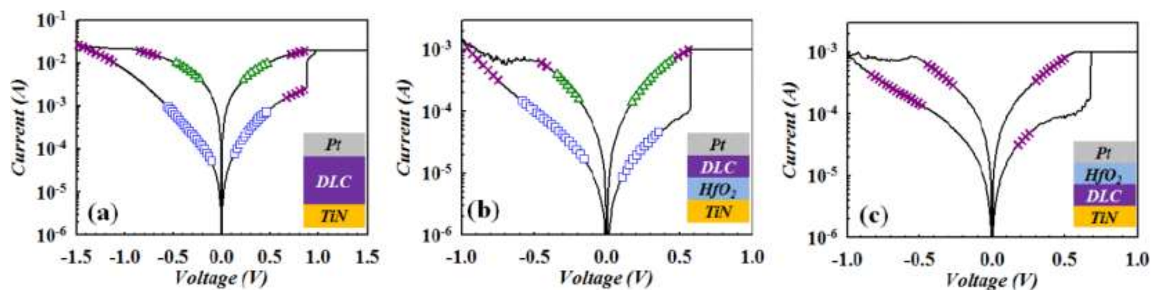

Figure 2.18 IV Characteristics of Different Carbon Stacks [47]

<u>Spin-Based and Magnetic Memristive Systems</u>

In 1995, the Magnetic Tunnel junction (MTj) layer was discovered independently by Moodera and Miyazaki which enables magnetic memristive systems [49]. The fabrication of a magnetic memristive system is based on two ferromagnetic plates. One plate is magnetized in a certain polarity, usually in the manufacturing process, and the other plate changes its polarity because of the electrons tunneling through the MTj. The same polarity of the plates allows the current to flow with low resistance. Then, having the opposite polarity of the plates slows electron flow and increases the resistance. A cross-section of a typical bit cell in a magnetic memristor is seen in Figure 2.19 [50, 51, 52].

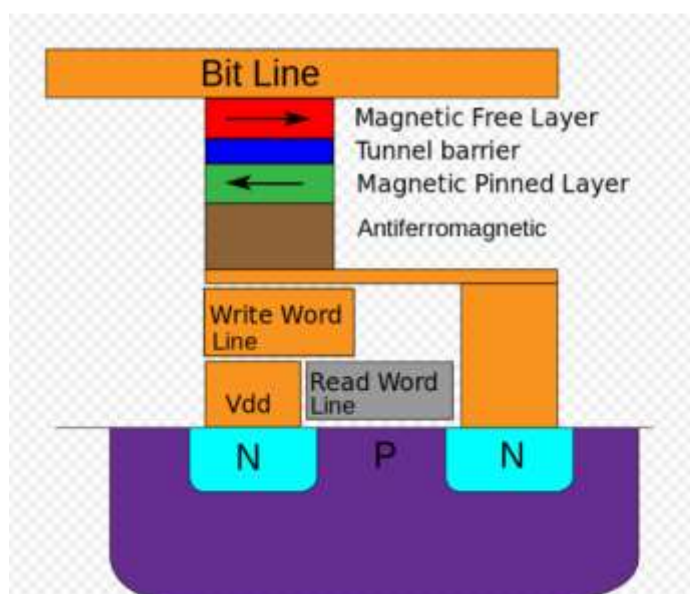

Figure 2.19 Magnetic Cell [50]

An example of the switching Voltages, high to low resistance and low to high resistance, are displayed in Figure 2.20. This figure shows the switching Voltage differences in the size of the device (s28nm×70nm and 80nm×180nm) and the pulse width [53]. These systems have a typical operating Voltage range of a negative 1.5 Volt to 1 Volt.

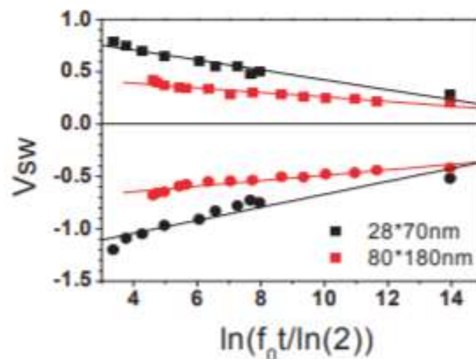

Figure 2.20 Switching Voltage vs Pulse Width of a MJt Memristor [53]

The ability of the spin of an electron to transfer to another is known as Spin Transform Torque (STT). STT was predicted by John Slonzewski from IBM research in 1996 and observed in 2000 by J.A. Katine, et al, [49] (2019). The observation led to the development of the spin-based memristor.

Spintronic memristors use electron spin as the switching mechanism. Controlling the spin of the electron allows changes in the polarity of the magnetization state of the device that will change resistance. Figure 2.21 (a) shows the electrical connections for a spintronic memristor with current density (j is measured). In Part (b) of the same figure, Voltage pulses are applied to the spintronic memristor which decreases the ratio of the current density of the source over the current density of the contact ($^{j}/_{j_c}$). Since the current

density is reduced by a positive Voltage, this implies that the resistance of the system is reduced. A negative pulse will increase resistance in the same way. The publication shows that the magnetization state of the device can be used to control the resistance of the device. Spintronic memristors have an operating Voltage range of negative 1 to 1.5 [54].

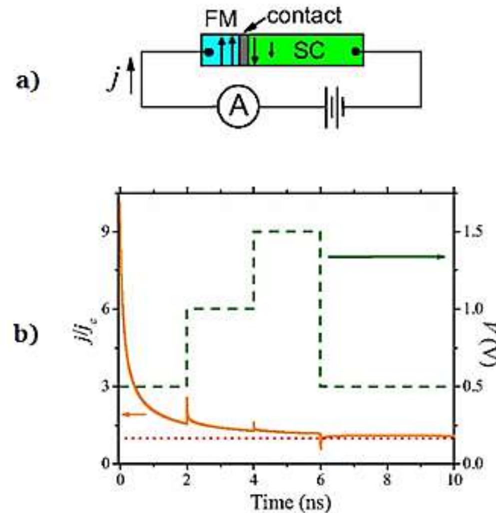

Figure 2.21 Spin Based Memristors: (a) Electrical Hookup of Spintronic Memristor (b) Voltage Pulse in Time vs Current Density [54]

<u>Thermal (Phase Change) Memristor</u>

A. V. Pohm first published, in 1970, using chalcogenide glasses for nonvolatile memory, because of the ability of the material to retain the state of resistance (Phase-change Random Access Memory-PRAM) [55]. With the change of resistance of the Phase Change Material (PCM), the optical properties change, and this forms the foundations of the Digital Versatile Disc (DVD) and the Compact Disc ReWritable (CD-RW) that is used today [56]. The phase change memristor can be used as a Voltage induced heated memristor, discussed in this work, an optical memristor, or heat memristor.

Some of the different materials which can be used for the formation of Phase change memory (PCM) devices are Antimony (Sb), Tellurium (Te) and Germanium (Ge).

The phase-change memristor (Phase-change Memory), PCM, uses the crystalline state to induce the low resistive state, amorphous state, to a high resistive state, as seen in Figure 2.22 [57].

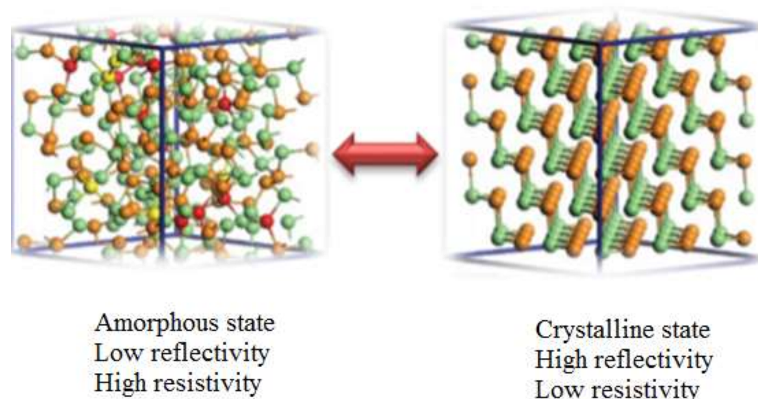

Figure 2.22 High/Low Resistivity Compared to the Lattice Structure of the PCM Device [57]

Figure 2.23 shows the pulsing of a PCM device that will cause the temperature to change across the device (Joules Heating). The heating will change the phase of the material, inducing a resistance change. A “Set” pulse will heat the amorphous PCM material to a state that will crystalize the material to reduce the resistance to a certain delta. Then a “Reset” pulse, higher than the “Set” pulse, would be applied to the device above the melting point to change the material to amorphous, creating a high resistance [58].

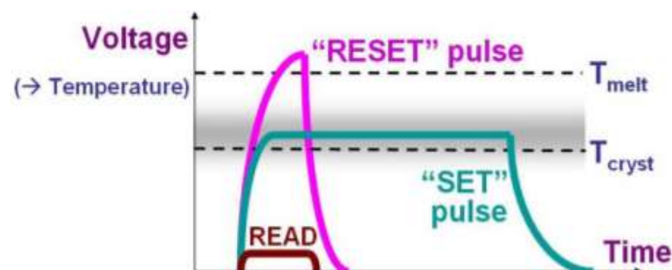

Figure 2.23 Reset and Set Pulses for PCM Resistance [57]

Figure 2.24 shows a typical integration of PCM material into memory. Each memory cell has a heater to allow “Reset” and “Set” in the crossbar array.

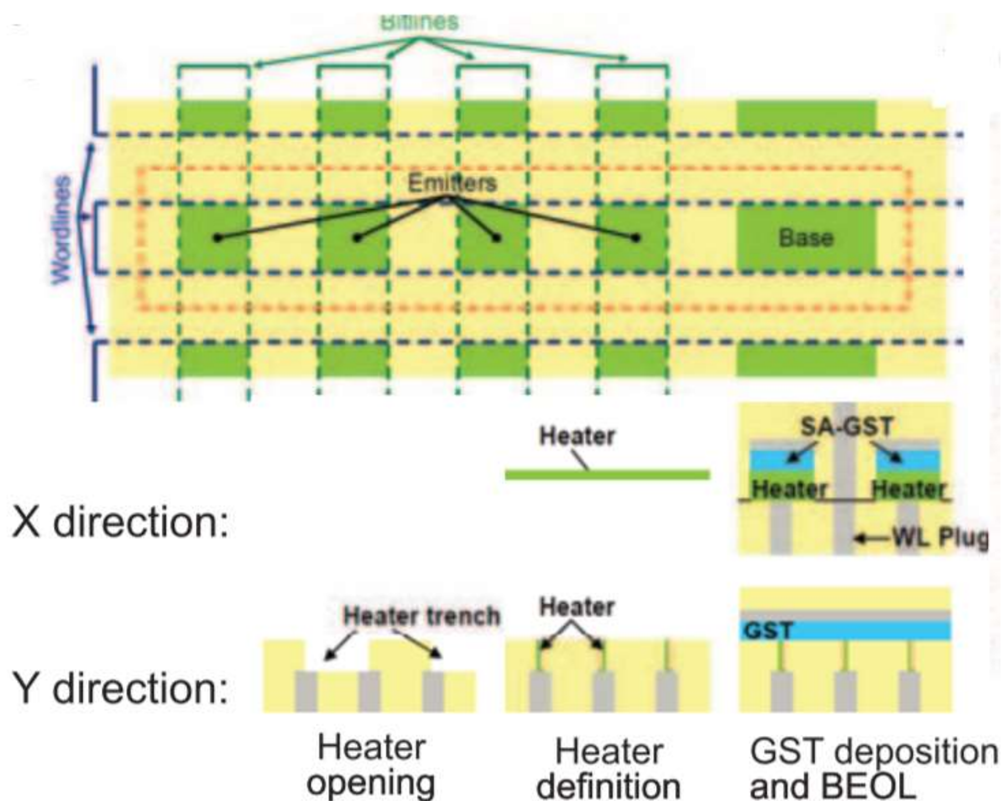

Figure 2.24 Typical PCM Integration into an Array [57]

Figure 2.25 shows the electrical operations of a Ge2Sb2Te5 PCM device. The paper describes how doping, introducing an element into the lattice structure, affects the electrical operation of the device. Figure 2.5 (a) shows that doping with Ti will affect the operational Voltages by shifting the set Voltage from 3.1 Volts, non-doped, to 1.1 Volts doped. In (b) the pulse width can also affect the operational Voltages of the devices, but this will be dominated by the fixed capacitances of the device. (C) shows the standard operation Voltages for the new doped device, Ge2Sb2Te5 (5.67% of Ti) at 0 to 2.2 Volts.

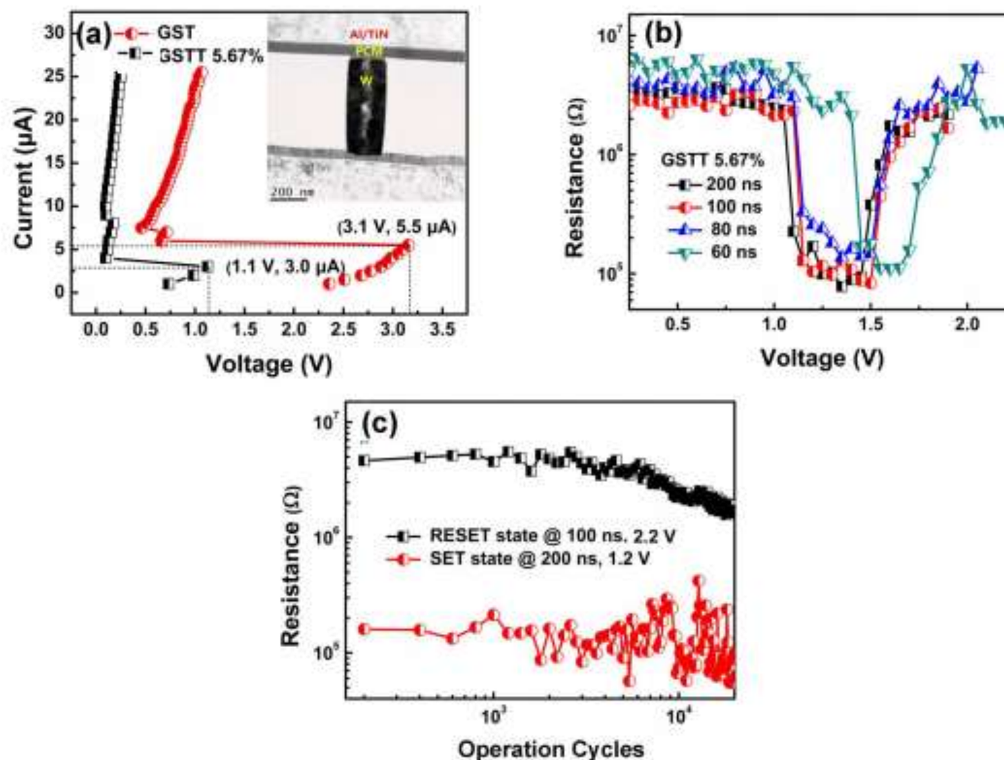

Figure 2.25 Ge2Sb2Te5 (GST) PCM Device: a) Non-Doped vs Doped with Ti: Current Forced b) Pulse Width vs Voltages c) Doped at 5.67% of Ti: Set and Reset Voltages [44]

Conclusion

As memristors have developed over many decades, several types of memristors with different operating Voltages and polarities have been created. If the past is an indication of the future many more types of memristors will be created with variations that will impact Voltage operation. In many of the publications reviewed, the electrical characterization tool and the corresponding setups used to electrically characterize the memristor were not mentioned. Where the tool was mentioned, the tool classes were semiconductor parameter analyzers used for I-V sweeps and waveform generators for pulsing Voltage. These tools cost several thousand dollars to tens of thousands of dollars. Research for a global test and characterization platform for memristors is needed that is

portable, uses off the shelf components, and is low cost. This platform would cover many types and variations of memristors, which would have a range of Voltage output of -3.7 Volts to 5 Volts (+3 Volts if Forming is needed [12]).

CHAPTER 3: THE MEMRISTOR USED TO TEST THE TEST CHARACTERZATION PLATFORM

Introduction

Before the work of the design of the test and characterization platform, a memristor was fabricated on a silicon wafer to enable the design and electrical characterization of the platform. The memristor that was fabricated was a cation memristor with a chalcogenide glass matrix of $Ge_{20}Se_{80}$ in a columnar vertical configuration that has larger columns of glass than originally fabricated and removal of the photo-diffusion of silver step to set the silver into the silicon lattice. These modifications were done to have a high initial Voltage than most types of memristors with a life cycle Voltage range of approximately -0.4 Volts to ten Volts [59]. The understanding of the processing of the memristor will allow the electrical characterization to be differentiable from the device and the platform, as the materials and the shape of the device will influence the electrical performance [60, 61]. The layout of the device shows how to connect electrical connections to the device. The fabrication and layout of the device were done as follows:

The Memristor Fabricated for the Development of the Test and Characterization Platform

The cationic columnar memristor was fabricated using silver as a cation source to form a conductive bridge (filament) within the columnar structure of the chalcogenide glass to adjust resistance. The device processing, was guided by Dr. Maria Mitkova, done by Muhammad Rizwan Latif, and the layout of the layers (the glass, the silver, and the

electrodes) was done by Steve Wald. Processing was done at Boise State University and then shipped to Advotech for singulation and packaging. The layers of the device were glass columns sandwiched between electrodes of silver and tungsten, as shown in Figure 3.1.

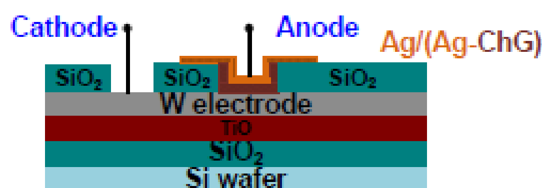

Figure 3.1 Cross Section of the Cell [59]

The silicon wafer was a 4" (100 orientation) diameter boron-doped (p-type) 380 micrometers thick. The 3 in 1 reticle, mask, was shifted that contained all the layers' geometries to build the cationic columnar memristor. The layers on the 3 in 1 mask, seen in Figure 3.2, are used to define the cathode (W Mask), the hole through the oxide to the cathode (Via Mask), anode of silver (Ag Mask) and another hole through the oxide for the cathode electrical access (W Pad Mask).

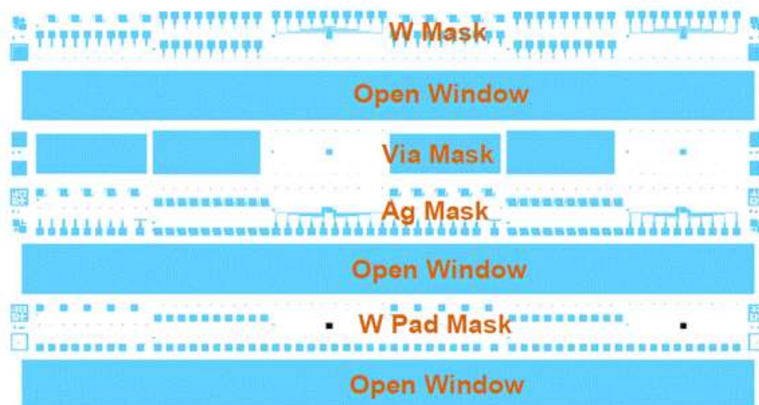

Figure 3.2 Mask (All in one Layer) [59]

The 3 in 1 mask avoided the need for individual masks for each layer and reduced cost, but did waste a portion of the silicon wafer surface. The usable die size is 7500

micrometers by 600 micrometers Figure 3.3, with an unusable area of 13 times of the usable area [59].

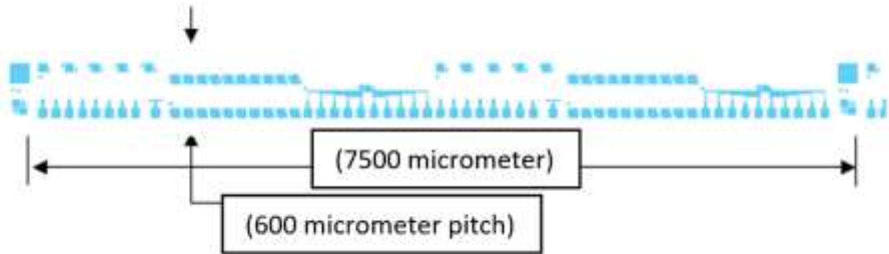

Figure 3.3 Die Size [59]

This novel approach of using the 3 in 1 mask was developed by Steve Wald and Rizwan Latif [59]. The process flow for fabrication of the cationic columnar memristor, that will guide the next sections, is shown in Figure 3.4.

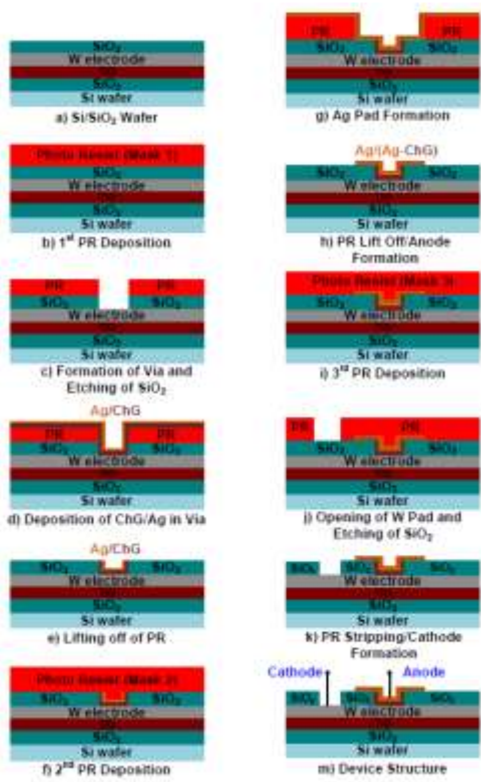

Figure 3.4 Cross-Sectional Flow, Fabrication of Memristor [59]

Bottom Electrode (Cathode) Layer

To isolate the devices from the p-type substrate, so a leakage path would not exist, a thermal Oxide layer (SiO_2) was grown at a thickness of 200-300nm. Titanium oxide (TiO) was deposited to promote adhesion for the tungsten bottom electrode. The bottom electrode was created by sputtering tungsten (W) and was not defined. Since the bottom electrode was not defined it made the cathode continuous, known as a "common bottom electrode" for all devices on the wafer, shown in Figure 3.4 part (a).

Via Layer

On top of the tungsten, an oxide was deposited to isolate each device from one another. This was done by spinning photoresist onto the wafer and using the pattern glass (3 in 1 mask) to transfer the geometric shapes into the resist by ultraviolet light. This process is known as photolithography. After a geometric shape was defined in the resist, the hole patterned was transferred from the resist to the oxide layer, by etching only the oxide. This created a hole through the oxide to the tungsten, shown in the flow of process presented in Figure 3.4 part (b) and (c). The hole in the oxide was formed for locations for the memristor devices to reside. Thus, each device had electrical contact to the bottom electrode and was isolated from the other surrounding devices. The hole, called a via, was etched with a Buffered Oxide Etch (BOE) a mixture of HF and NH_4F. A scanning electron image of the via is shown in Figure 3.5.

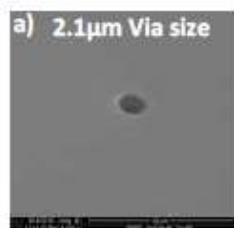

Figure 3.5 Via Angle Overview [59]

The photoresist used in the etching of the via, usually removed, was kept to enable a lift-off process for the active layer, described later.

Active Layer

Chalcogenide matrix, $Ge_{20}Se_{80}$, was thermally evaporated over the photoresist which is the active layer (ChG). Using a specialized technique to deposit the chalcogenide glass, a columniated structure can be formed, shown in Figure 3.6, with one exception, the columns have a larger width so the device requires forming within its life cycle. This columniation has unique electrical characteristics of a near unipolar device. After the active layer, a thin layer of silver (Ag) was evaporated on top of the chalcogenide glass as the source of silver ions, shown in Figure 3.4 part (d). A lift-off process was used to dissolve the resist and lift off (remove) the active layer and silver over the resist that was not needed. This process left the active layer and silver only in the via over the tungsten, shown in Figure 3.4 part (e) [59, 60, 61].

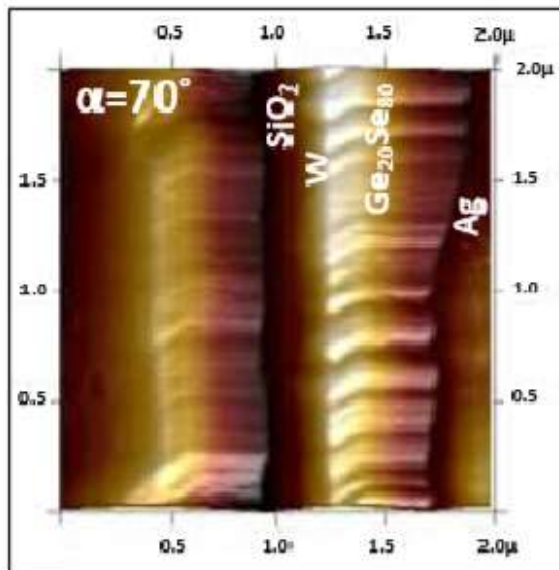

Figure 3.6 AFM Images of the Columnar Structure [60]

Top Electrode (Anode) Layer

Using standard photolithography, the resist was defined to have a pad shape opening with a lead that extends over the via. After that silver (Ag) was evaporated over the resist and into the openings of the resist. Then the same lift-off process was done to remove unwanted silver and to isolate the pads and leads from one another, as shown in Figure 3.4 part (f) to (h). The pads of silver allowed a wire to adhere to the memristor or tungsten pin to touch the memristor, to have electrical access to the top of the device (Anode), as shown in Figure 3.7.

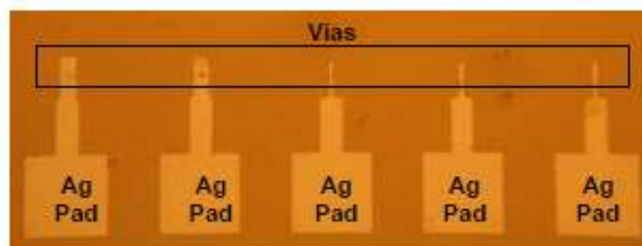

Figure 3.7 Anodes with Pads [59]

Exposing Cathode layer

To make electrical contact with the cathode, tungsten (W) common bottom electrode, a creation of holes through the oxide is necessary. Another photolithography and etch is done through the oxide to allow electrical contact to the two-terminal device, as shown in Figure 3.8. Shown in Figure 3.9 is a vertically shifted 3 in 1 mask from the layout with pictures of the actual die after the final processing.

Figure 3.8 Exposing Bottom Cathode [59]

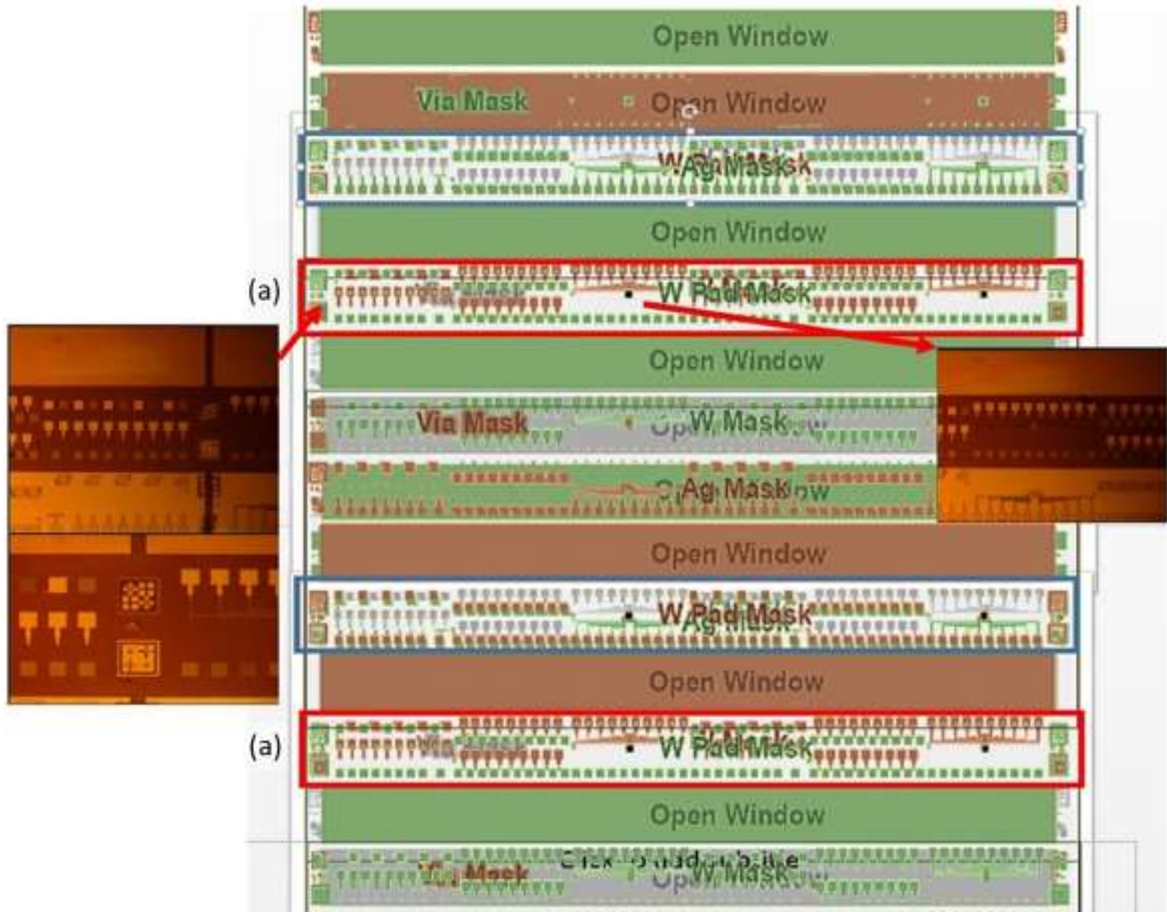

Figure 3.9 Photos of Devices and Pads Produced by the 3-1 Mask that was Physically Shifted Vertically (a) Active Die Area Boxed in Red

The understanding of the device processing and layout will guide the wafer electrical characterization, the packaging processing and the post packaging electrical characterization. Modification to the active layer of thicker columns will require forming to be done. Adding forming to the cation columnar memristor will allow the test and characterization platform to show that it is able to handle a variety of memristors.

CHAPTER 4: ELECTRIAL CHARACTERIZATION AT WAFER LEVEL AND PACKAGING

The Electrical Characterization Details

After the near-unipolar cationic columnar memristor devices were fabricated on a silicon wafer, the wafer was electrically characterized for functionality and to guide the design of the test and characterization platform. The electrical characterization of the silicon wafers was carried out on the Micromanipulator 6200 Probe Station with a Cascade Microtech DCM 210 Series Precision Positioner XYZ Micromanipulator [62] with tungsten tips, shown in Figure 4.1.

Figure 4.1 6200 Micromanipulator Probe Station and DCM210 [62]

The parametric analyzer used was the Hewlett Packard (HP) 4155B [63] connected by coaxial cables to the probes shown in Figure 4.2. The control software of the parametric analyzer was Easy Expert Software [64], provided by Agilent. All measurements were carried out at room temperature to verify the operating Voltages and the lifetime Voltages of the cationic columnar memristor. The wafer was placed on the chuck, the

micromanipulators used to make contact with the pads of the device (Forcing Voltage on the cathode), and the parametric analyzer used to sweep Voltage.

Figure 4.2 Hewlett Packard 4155B [63]

Electrical Characterization of the Direct Current Station: Virgin Sweep and Forming the Cationic Columnar Memristor.

The lifecycle of a memristor may impact electrical characterization, as the Voltages required to change resistance may change as the memristor cycles resistance. Part of the lifecycle may be forming when a memristor needs to cycle from high to low resistance many times to have a stable positive threshold Voltage for a given current compliance. Most cation filament devices [65, 66] must go through a forming cycle, and with the original columnar cationic structure developed [59] forming was not necessary. But the columnar cationic memristor developed for this research has larger columns in diameter that will need forming.

With the larger columns in the device, the silver ions (Ag^{+}) travel through the glass column down to the inert cathode and undergo reduction by which a filament of silver starts

growing towards the anode in an electrochemical oxidation mechanism [67]. With the column being larger the filament will have many potential areas in the lattice of the glass to grow horizontal nodules of silver, requiring more silver ions to form silver than the smaller in diameter columns. The energy required to produce the nodules of silver will translate into a high positive threshold Voltage (V_{TH_1}), but the larger columns do not affect the negative threshold Voltage (V_{TH_2}), since the energy is the same to break the filament in any diameter size of columns in the cationic columnar memristor. Having only one conductive path to break, oxidation, makes the columnar cation memristor to have a low V_{TH_2}, giving its near-unipolar polarity. After the silver filament is broken in the thicker column, the silver remains where the nodules were formed but multiple cycles are required to fill all the potential areas where the nodules could grow. During each filament growth the V_{TH_1} will decrease until the positive threshold Voltage stabilizes to an operating Voltage. The first sweep on a device will be called a virgin sweep within this work and the following sweeps to operating Voltages are the forming sweeps.

The first sweep on a virgin device requires the largest threshold Voltage for the modified cationic columnar memristor that will range from 3 to 10 Volts. Figure 4.3 shows the first four sweeps of a near unipolar device with a compliance of 80 Nano-Amps to prevent the breakdown of the device's active layer.

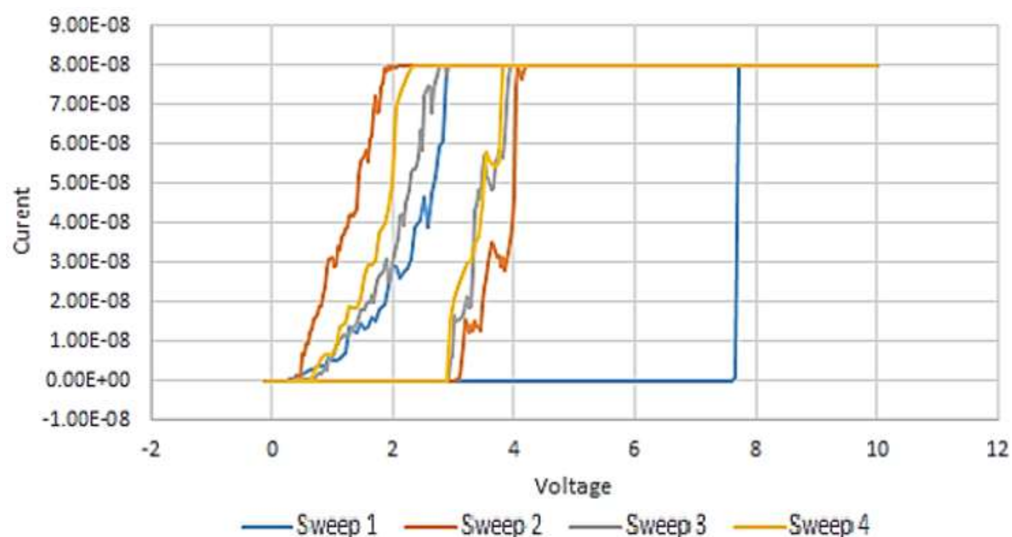

Figure 4.3 Forming: First 4 Sweeps at 80nA Compliance

The virgin device, “sweep 1”, shows a much higher threshold Voltage at 7.8 Volts than the next three sweeps which have a threshold Voltage at about 3.8 Volts.

Changing to 50 Nano Amp compliance and moving to another memristor on the silicon wafer showed differences in the IV curves, displayed in the Figure 4.4 compared to Figure 4.3. The first sweep, shown in Figure 4.4, has a much higher threshold Voltage than the first sweep, shown in Figure 4.3. The average slope of the shifted resistance of the last three sweeps is 20/1 (Nano-amps/Volt) shown in Figure 4.3 and 45/1 (Nano-amps/Volt) shown in Figure 4.4 that has a difference of 25/1 (Nano-amps/Volt). At the early forming of a memristor, including the virgin sweep, the threshold Voltage varies drastically. Because of this variation of potential sites to form nodules, it would be hard to conclude that the compliance current has influenced the variability.

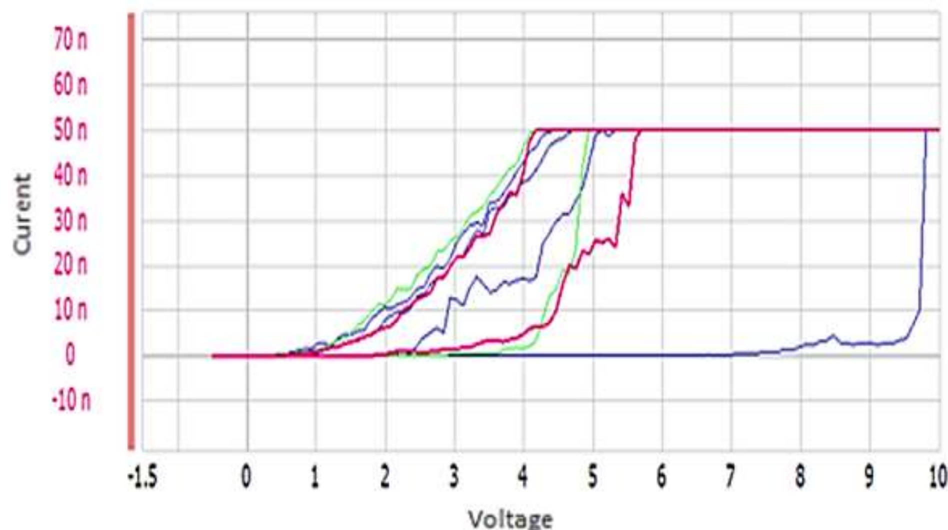

Figure 4.4 Forming: First 4 sweeps at 50nA Compliance

The number of forming sweeps needed to reach operating Voltages vary because of the processing of the memristor and how it was fabricated. The Voltage sweep was set at negative 100 milli-Volts to five Volts at 50nA. After one hundred Voltage sweeps, the threshold Voltage stabilized at 1.9 Volts with a compliance of 50nA. The last four sweeps are shown in Figure 4.5. The lifetime Voltages of the cationic columnar memristor were approximately -0.5 Volts to 10 Volts.

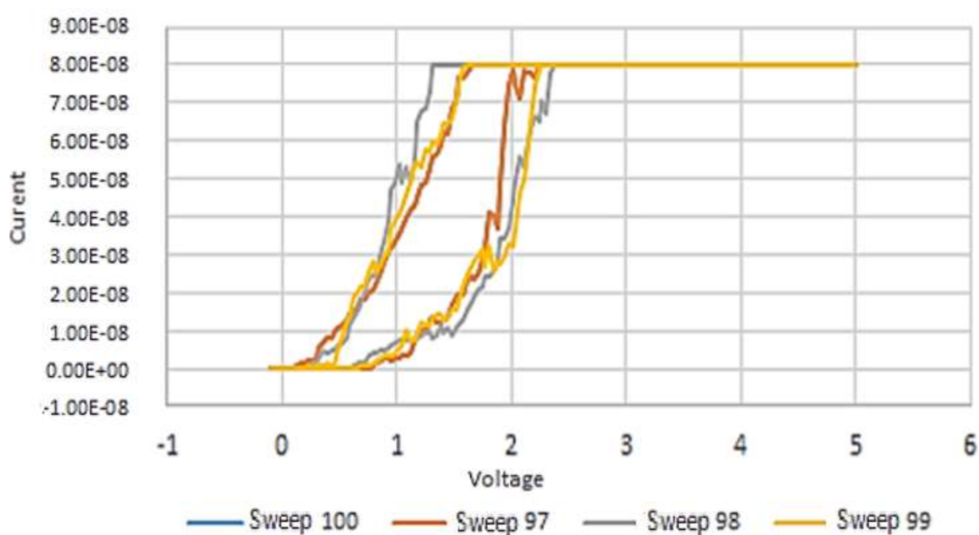

Figure 4.5 Forming: Last 4 Sweeps of 100

The Packaging of Memristors

Memristors on silicon wafers cannot be integrated into Printed Circuit Board boards (PCB) for applications. So, the wafer needs to be cut to small pieces (singulation), which is known as a die so that they can be placed into packages. The singulation of a wafer into a die is where the wafer is physically sawed into individual IC's (Integrated Circuits) or a group of devices for packaging, as shown in Figure 4.6.

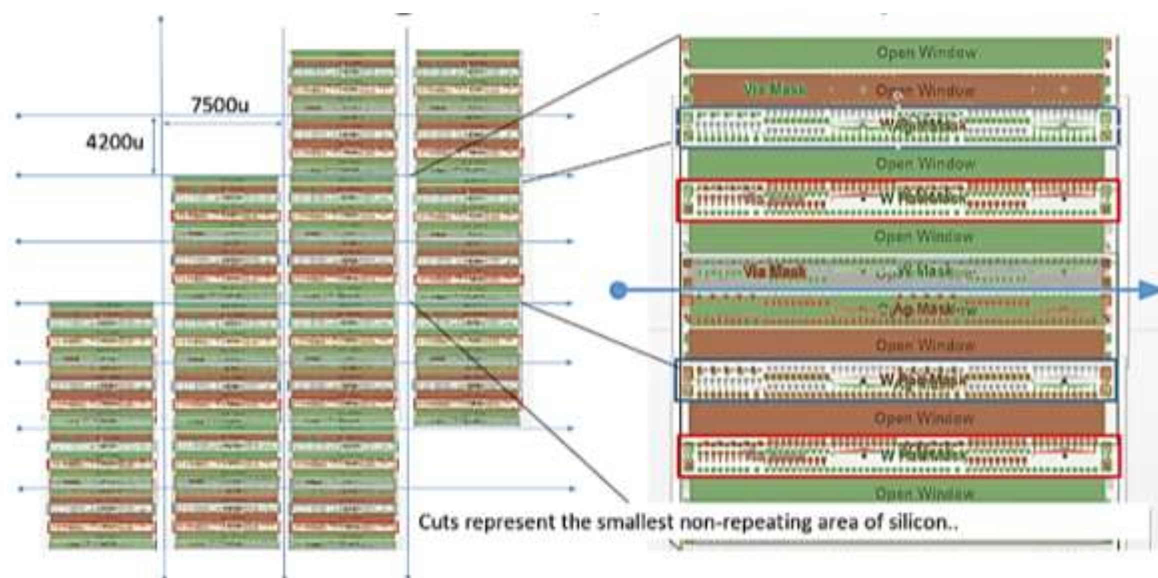

Figure 4.6 Singulation of the Memristor Wafer (Blue Arrows=Saw lines)

The packages are placed into PCB boards for experimental applications. Electrical characterization after packaging is important for the functionality of the memristors, and to find any Voltage shifts that are due to the processing of packaging.

The singulation and the packaging of the wafer was done by Advotech Incorporated. The die were placed into 28-pin ceramic packaging (CERDIP28F6-SB-N310) which was purchased from Topline Inc. The package has 0.360-ohm max leads (pins), with a pitch between pins of 0.100 inch, and a square cavity (for die insertion) of

0.420 inches [68]. This package type was chosen, because it would fit into a standard breadboard.

Figure 4.7 Testing of the Package Part on the Micro-Manipulator Probe Station

The testing of the packaged device was done on the Micro-Manipulator Probe Station to confirm functionality and that no threshold Voltage shifts are present after packaging. Double-sided tape was placed on the metal chuck of the probe station to prevent movement of the package and pin to pin shorts, as shown in Figure 4.7.

The Voltage sweeps of the device in the package need to be compared to wafer-level Voltage sweeps. Shown in Figure 4.8, V_{TH_1} is approximately 9.8 Volts compared to the wafer-level V_{TH_1} of approximately 9.7 Volts, as shown in Figure 4.4. V_{TH_2} was not captured by the parametric analyzer, because the negative Voltage required for the high resistance state is too small to be recorded in most instances. The virgin sweeps at wafer level and package level differ by 0.1 Volts and are equivalent. Also, the shape of both sweeps are very similar and do not show any parasitic capacitances added by the package or the process of packaging.

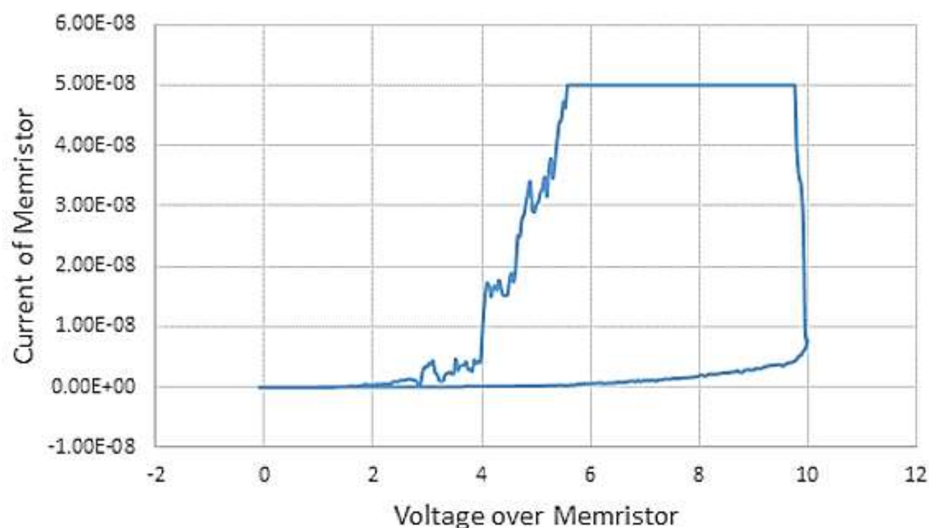

Figure 4.8 Forming: Voltage Sweep of a Virgin Device after Packaging

After forming of the memristor in the package, shown in Figure 4.5, V_{TH_1} was approximately 1.4 Volts. The memristor at package level at forming had a V_{TH_1} that was comparable to the water level forming of V_{TH_1}, approximately 1.5 Volts.

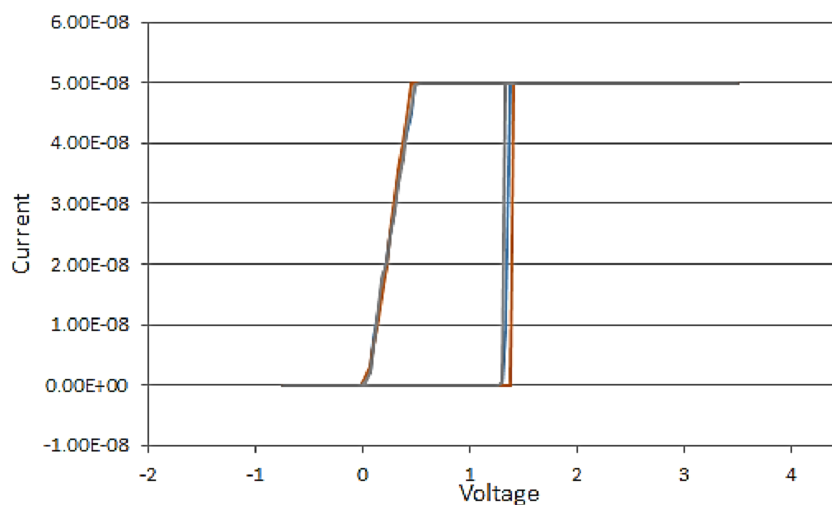

Figure 4.9 Forming: Voltage Sweep 98 to 100 after Packaging

In conclusion, singulation and packaging did not affect the electrical characteristics of the IV curves of the memristors. The lifetime voltages of the cationic columnar memristor remained approximately -0.5 Volts to 10 Volts. Also, by packaging the

memristors, the memristors could be used on breadboards, PCBs and other configurations that would be closer to real life types of experimental applications. So, the test and characterization platform must be able to accept wafer and package level memristors.

CHAPTER 5: THE PULSE GENERATOR STATION

Introduction

The Voltage pulsing of a memristor is important, because in a clocked environment, as in memory and neuromorphic circuits, pulses are used to change the resistance of the memristor [5]. The current memristor memory has two states of resistance, high and low, that correspond to a Multiple Binary digIT (BIT) of memory, “1” or “0”. But in the next generation of memristor-based memory, multiple bits will be stored on a single memristor. The multiple BITs stored on a single memristor will leverage the memristor’s continuous resistance that can stand for many bits of information into one memristor [69]. Neuromorphic applications will use the variable resistance of the memristor as weights within its architecture [70]. This will require the test and characterization platform to perform Voltage pulsing. So, a pulse generating station was assembled to characterize the cationic columnar memristor to determine the design of the test and characterization platform that will be built. The next sections will discuss a memristor design to be used in the station, assembly of the pulse generating station, and the conclusions made from electrical characterization of the cationic columnar memristor using the pulse generating station.

The Voltage Divider (Shunt Resistor)

In most large test stations that are commercial grade, the equipment has a current compliance that will limit the current as the memristor enters a low resistance state, protecting the memristor. The test and measurement platform will not have a current

compliance, so another way to limit current is to have a fixed resistor (shunt resistor) in series with a memristor, to create a Voltage divider, a Memristor Based Design (MBD). Figure 5.1 shows a standard Voltage divider with a shunt resistor and a load, and the load is the memristor. The Voltage divider also allows the ability to measure the Voltage change of the memristor, so the memristor's Voltage can be compared to the Voltage of the divider.

The configuration of the shunt resistor is important to protect the memristor and to produce accurate measurements. The shunt resistor in normal use (without a memristor) is used to measure the Voltage drop across the shunt resistor of the circuit design. Then it's possible to determine the current of the Voltage divider. The shunt resistor is calibrated to an exact resistance to retrieve accurate Voltage or current measurements. Also, the shunt resistor is placed next to the ground in order to prevent common-mode Voltage, which may damage the shunt resistor and reduce the accuracy of the results, as shown in Figure 5.1 part (a) [71]. But when using a shunt resistor with a memristor, the memristor must be protected from any common-mode Voltage errors, so the memristor will be placed next to the ground, as shown in Figure 5.1 part (b).

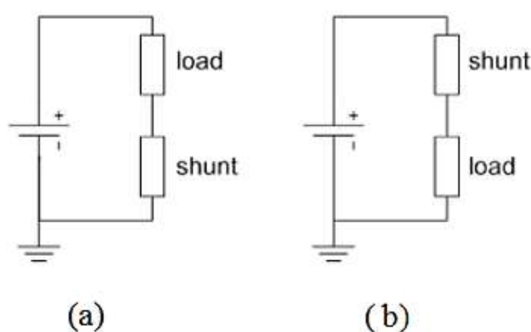

Figure 5.1 Setup of Shunt Resistor (a) Load First Memristor (b) Load Last Memristor [71]

Choosing the proper shunt resistor resistance is important to increase and decrease the resistance of the memristor in the Voltage divider. In Equation (5.1), the memristor's Voltage potential is dominated by the resistance of the memristor in a high resistive state or by the shunt resistor's resistance when the memristor is in a low resistive state.

$$V_{memristor} = \frac{R_{Memristor} * V_{Over\ the\ Divider}}{R_{Total\ Resistane\ of\ Divider}} \quad (5.1)$$

Shown in Figure 5.2, the divider Voltage is held at six Volts, while the memristor resistance is varied. Each curve of the figure represents a fixed shunt resistor that ranges from 25 kOhms to 1 MOhms. If either the fixed shunt resistance increases or the memristor's resistance drops, the Voltage over the memristor decreases. So, when the memristor is in a high resistive state, the memristor will have most of the Voltage dropped over the memristor and applied to the Voltage divider.

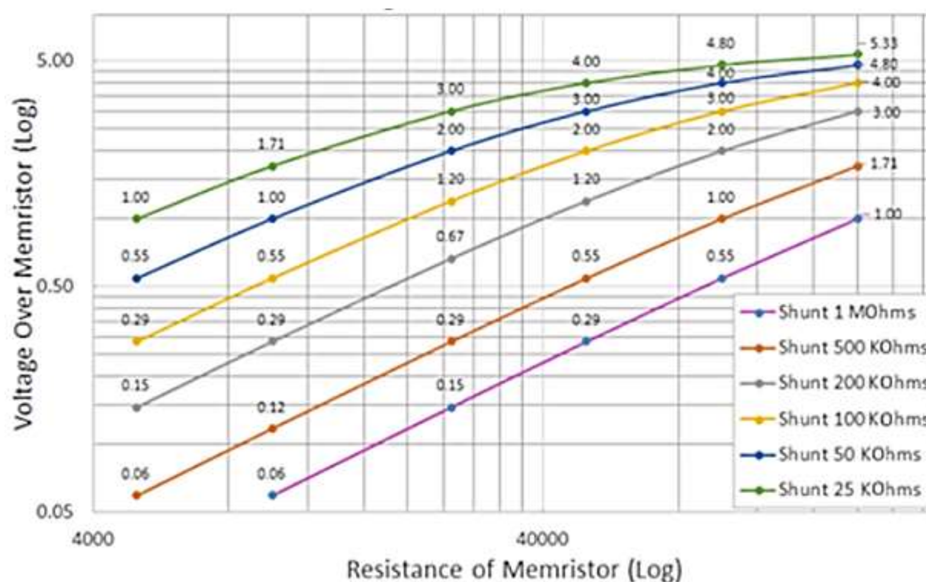

Figure 5.2 Different Shunt Resistors vs. Memristor's Resistance Varied in Voltage Divider (Voltage Applied over the Divider at 6V):

With more of the Voltage over the memristor, the potential is higher to migrate the silver ions to create a conductive filament to lower the resistance of the memristor. But when the memristor is in a low resistive state, more negative Voltage is over the shunt resistor than the memristor. Since the negative Voltage is lower over the memristor, the potential energy to break the filament is lower and may require higher negative Voltage to bring the memristor to a higher resistive state.

Fixing the memristor to 25 kOhms, a low resistive state shown in Figure 5.3, a shunt resistor of 60 kOhms will have one-third of the Voltage over the memristor that is applied to the divider. This implies the shunt resistor in the Voltage divider should be at 60 kOhms or lower, so that a large negative Voltage pulse will not be required to increase the memristor's resistance.

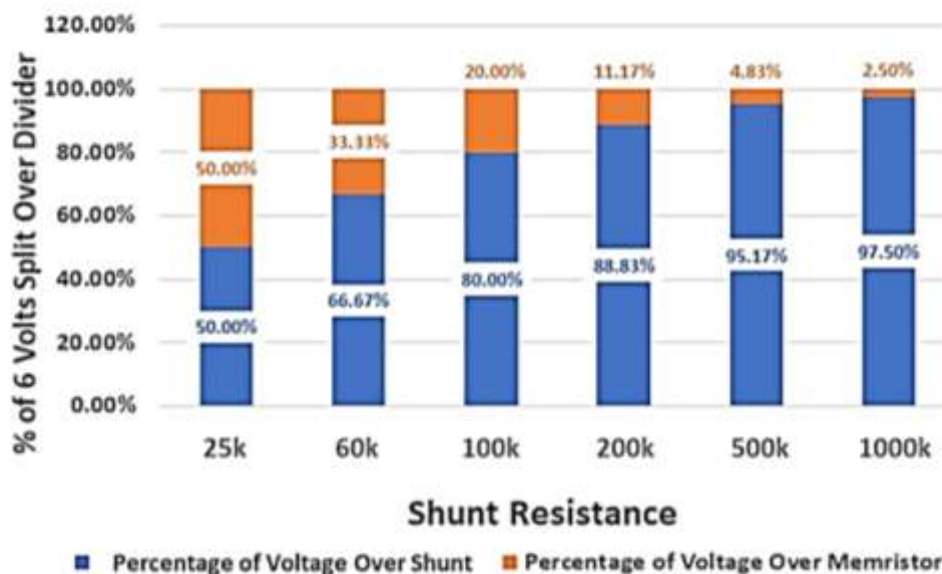

Figure 5.3 Percent Voltage Drop Over the Memristor at 25 kOhms vs. Shunt Resistance.

In the cationic columnar memristor (near-unipolar), the negative Voltage to go to higher resistance is much less, because the memristor only produces one conductive

filament. Even though the negative Voltage potential needed for cationic columnar memristors to increase their resistance is low, a large negative pulse is still required from the test and characterization platform for other types of memristors. But the near-unipolar cationic columnar memristor has a definite advantage in power consumption over the bi-polar memristor types that require a higher negative Voltage to reduce resistance.

Within the Voltage divider, the shunt resistor resistance was chosen to be at 54 kOhms. This choice will allow enough of a Voltage drop over the memristor in a low resistance state to bring the memristor back to a high resistance while restricting the current flow. The Voltage will be measured over the whole divider and over the memristor to be able to calculate the memristor's resistance and the current of the divider, as shown in Figure 5.4.

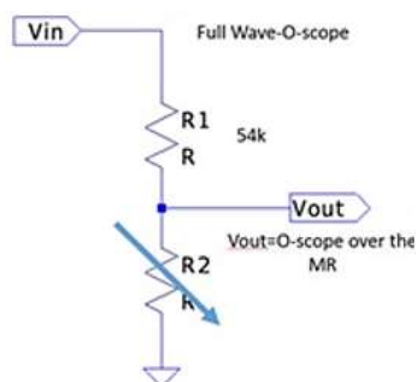

Figure 5.4 Voltage Divider with Memristor

Pulsing Synchronization of Two PGU's

The tool used to apply the Voltage pulse over the MBD, a Voltage divider, was the Agilent 81130A, a Pulse Generating Unit (PGU). The 81130A can only generate 2.5 Volts, with a Voltage offset of 1.5 Volts. A fixed resistor of 100 kOhms is used, instead of the memristor divider to set the testing parameters of the PGU. Also, in this phase, the support equipment of the PGU was established to enable greater ability to test with multiple pulses

and timed pulses. One of the limitations of the Agilent 81130A is that it is only capable of producing one polarity, a positive or a negative Voltage. Because of the polarity issue, two PGUs were used over the Voltage divider, one being used for a negative Voltage and the other being used for a positive Voltage.

One of the challenges was synchronization of the two individual PGUs over the fixed resistor. The first tests showed that each PGU unit was out of phase and would drift, shown in Figure 5.5.

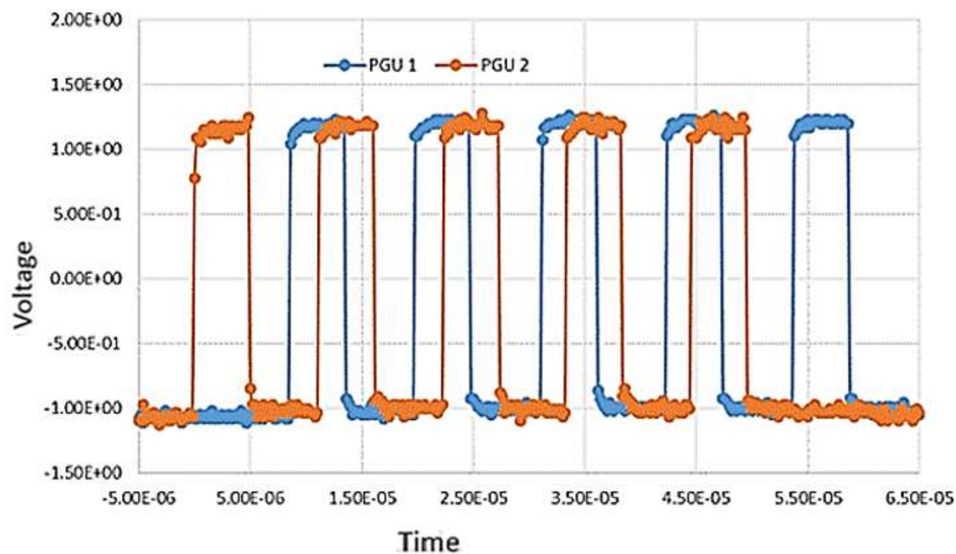

Figure 5.5 PGU's Without Synchronization Clock Both PGUs Triggered for Five Pulse Burst

Supplying a synchronization clock to both PGU's was used to correct the issue. An external waveform generator, the Agilent 33521 (Maximum 30 Megahertz), was connected to the "input clock" port with a coaxial cable which was split between PGU 1 and PGU 2. The input clock, the Agilent 33521, was set to 20 Megahertz, with a 50% duty cycle, with a one-Volt amplitude. PGU1 was used for the positive Voltage pulse and PGU2 for the negative Voltage pulse.

The next step was setting the trigger for each PGU to fire a Voltage pulse at the same time. The Agilent 33220, which was set for a single pulse, was used for the rising edge trigger at one kiloHertz with one-Volt amplitude. After the Agilent 33220 was connected to the PGUs, the trigger pulse was fired manually from the Agilent 33220. The result showed both the PGUs firing Voltage pulses that were synchronized by the input clock and firing at the same time, shown in Figure 5.6.

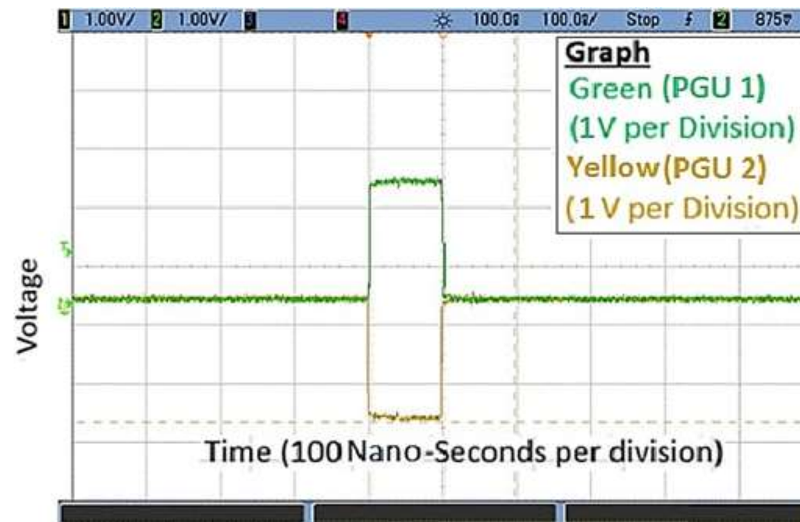

Figure 5.6 2 PGU's Using Synchronized Clock (External Clock)

Then to get a positive pulse to fire first, the PGU2's negative pulse was delayed by 100 nanoseconds, shown in Figure 5.7.

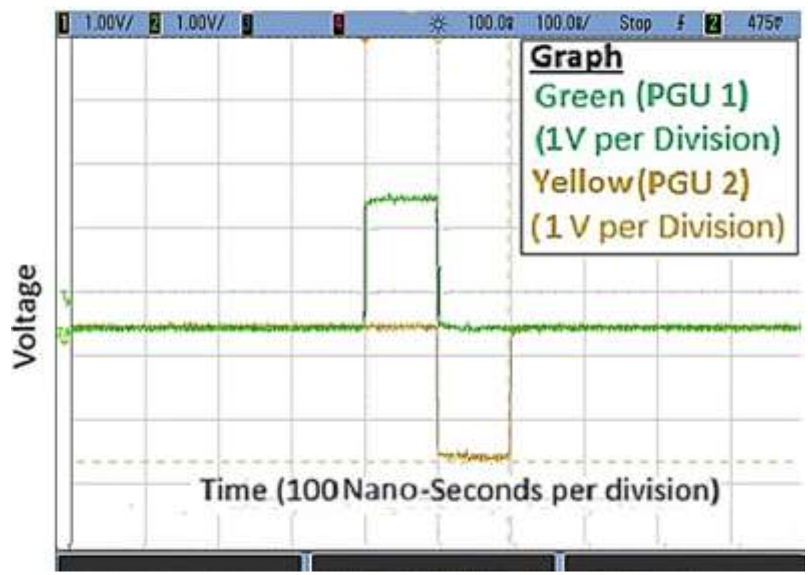

Figure 5.7 Offset Negative and Positive Pulses Synchronized

To make sure a "burst of 2 pulses" would be synchronized with a single pulse, PGU2 was set up to burst 2 pulses, the results in Figure 5.8 shows that the burst was synchronized to the single pulse.

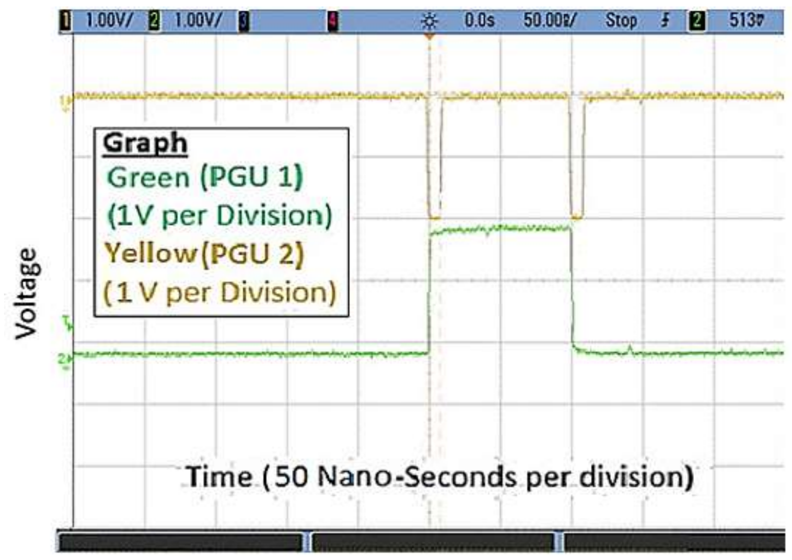

Figure 5.8 Multiple Pulsing vs. Single Pulsing

The full PGU station that was developed, Figure 5.9, shows the PGU's, the input clock, and the trigger. Then in the "Laboratory Virtual Instrument Engineering

Workbench" (LabVIEW), a programming environment created by National Instruments, a program was developed to control the PGU station and provide automation [72].

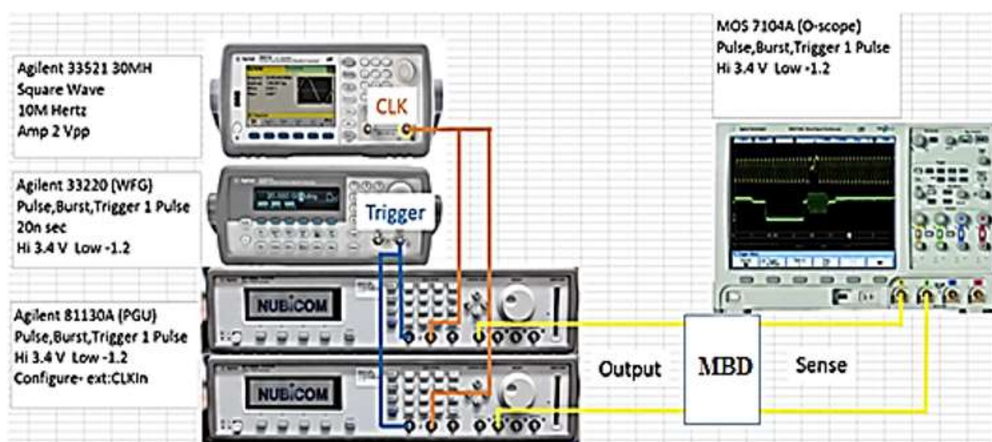

Figure 5.9 PGU Station Set up with MBD or Fixed Resistor

PGU Testing with a MBD

After the setup was established with a fixed resistor, the MBD (Voltage divider) with a cationic columnar memristor was introduced into the PGU station. The PGU tools cannot generate Voltages higher than four Volts, so the PGU tool cannot cycle a virgin memristor that requires approximately 10 Volts. So, before the memristor was used in the MBD, it was cycled until it was formed on the Micromanipulator Probe Station, then transferred into the MBD and then placed into the PGU station.

The PGU1 was set for a positive pulse, and the PGU2 was set to give a negative pulse, with a delay applied to the negative pulse of 17.5 microseconds. A positive Voltage pulse of 1.79 Volts for 30 microseconds was generated by the PGU1, and was applied over the MBD shown in Figure 5.10. The memristor in the divider dropped to 531 milli-Volts, from 725 mill-Volts, within 5 microseconds of the positive Voltage pulse. The rest of the positive pulse, 25 microseconds, drove the Voltage of the memristor to 134 milli-Volts. The Voltage drop over the memristor is constant with a resistance drop of the memristor,

by Equation (5.1). The PGU2 then generated a negative Voltage pulse over the MBD of a negative 1.70 Volts. A negative Voltage spike occurred over the memristor when the negative pulse was applied over the MBD. The spike reached its maximum at negative 394 mV, then fell. This shows the memristor's resistance increasing.

Examining Figure 5.10 at (a), shows Voltage dropping while the memristor is at a high resistive state. This is an indication that resistance shifts while the filament is not fully formed. A sudden drop in the Voltage shows that the filament has formed between the anode and cathode of the device at location (b) in the figure. Then another slow shift to a lower Voltage occurs at (c), which means a thickening of the filament.

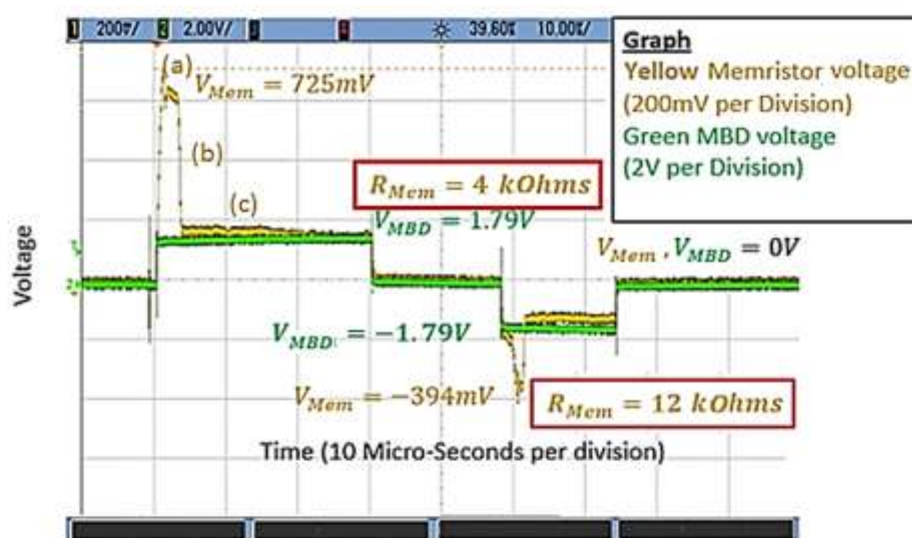

Figure 5.10 PGU Station Pulsing: MBD (Divider-Memristor) PGU1 (Positive Voltage) PGU2 (Negative Voltage) (a) Adjustment to Resistance in Near-off State-Forming Filament (b) Rapid Change in Resistance-Filament Formed (c) Adjustment to Resistance in Near-On State-Thickening of Filament.

In conclusion, the Voltage pulsing to shift the resistance will not be done as the filament makes its initial contact to the anode as the transition (slope) (b) is much too fast to have multiple individual resistance states with Voltage pulsing. But when the memristor is in a near-off (high resistive state) (a) or near-on (low resistive state) (b) the slope of

transition is much slower and the memristor will be able to have multiple resistance states using Voltage pulsing.

The next set of pulses from the PGUs over the memristor did not show a decrease in Voltage over the memristor from a high resistive state. So, PGU1 and PGU2 were set to a positive 2.5 Volts. This combined the Voltages of the PGUs to 5 Volts amplitude, with the PGU1 Voltage floor set to 1.2 Volts. The combination of Voltage floor and combining the pulse of the PGUs allowed 6.2 Volts to pulse over the MBD. Graphs (a), and (b) of Figure 5.11 showed the Voltage remaining similar over the memristor after 100 Voltage pulses.

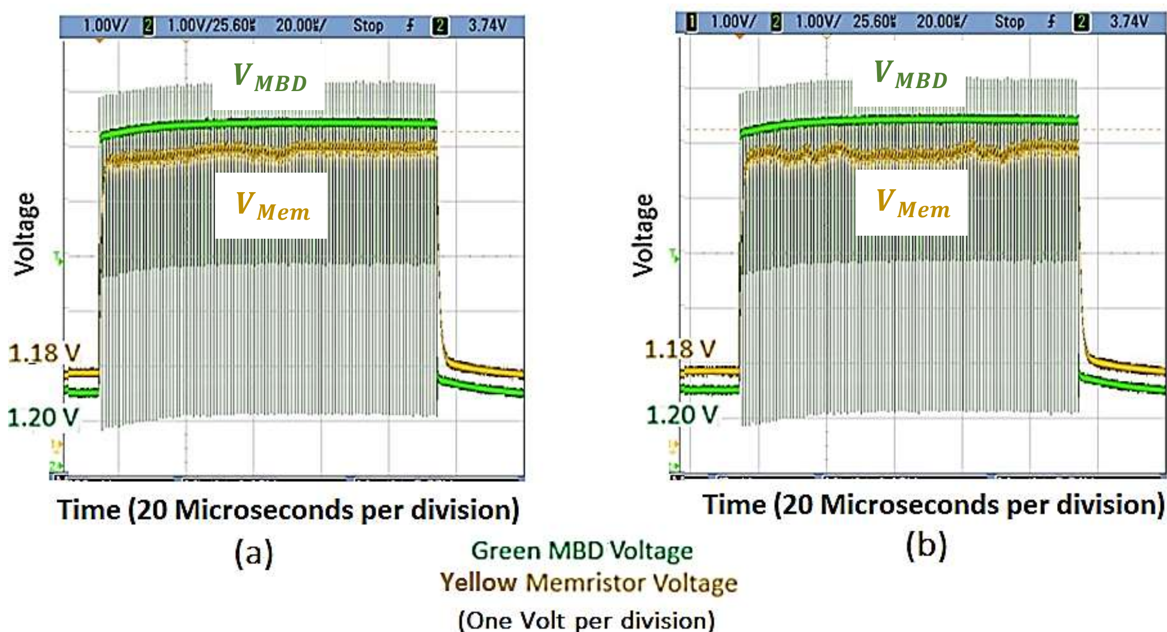

Figure 5.11 Recovery from High Resistance: 100 Voltage Pulses in 0.50 Microsecond Width with 50% Duty Cycle. Voltage over MBD is Approximately 6.2 Volts. (a) Voltage over Memristor is Approximately 5 Volts (b) Voltage over Memristor is Approximately 5 Volts.

Then the PGUs Voltage pulses were increased to 150 pulses. This showed a large Voltage decrease, also shown in the Voltage floor of the memristor which decreased from 1.08 Volts to 0.10 Volts, and this equates to a large resistance decrease, shown in the Figure

5.11 graph (d) and (c). This new configuration was outside the capabilities of the LabVIEW program and had to be done manually. Even though this technique of combining the PGU's Voltage output worked most of the time, sometimes the cationic columnar memristor had to be transferred back to the Micromanipulator Probe Station to reduce the memristor's resistance to resume Voltage pulsing, as the PGU station could produce the proper Voltage. No effort was made to modify the LabVIEW program, because the LabVIEW visual interface was complicated to modify once written, and the PGU electrical characterization of the cationic columnar memristor was nearly complete.

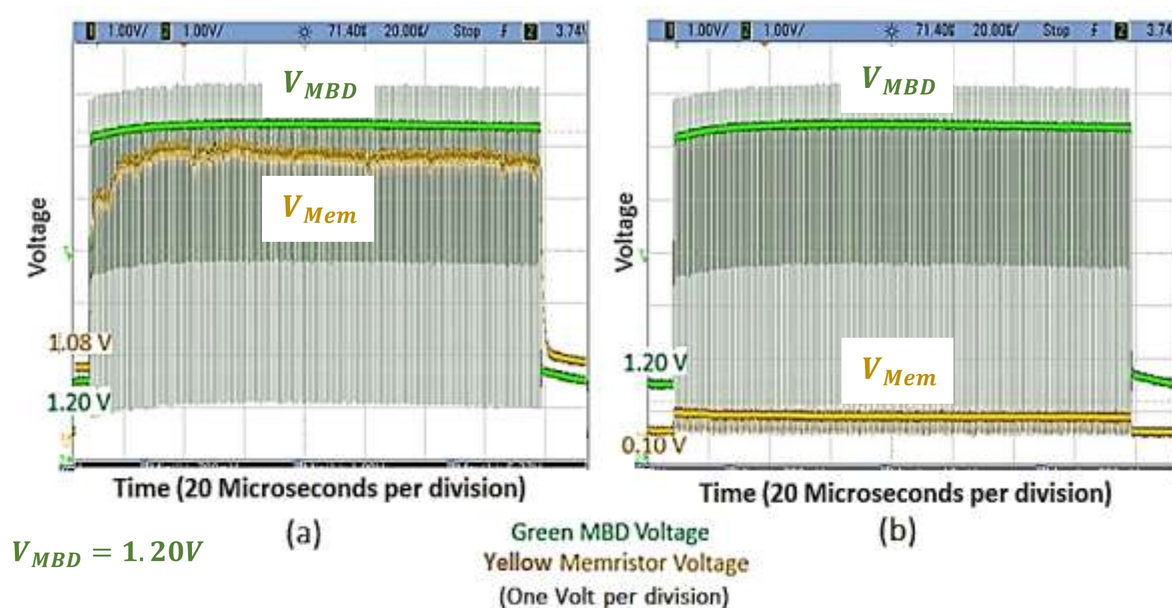

Figure 5.12 Recovery from High Resistance: 150 Voltage Pulses in 0.50 Micro-Second Width with 50% Duty Cycle. Voltage over MBD is Approximately 6 Volts. (a) Voltage over Memristor is Approximately 5 Volts. (b) Voltage over Memristor is Approximately 0.6 Volt.

After recovering the cationic columnar memristor from a high resistive state, a series of Voltage pulses was characterized. The characterization was done to see if the memristor would steadily decrease resistance within each set of pulses as predicted [73].

This characterization would show if the PGU station was capable of operating the cationic columnar memristor as expected. The PGUs were set for a burst of 10 pulses of 1.9 Volts with a 4 microseconds pulse width at an 80% duty cycle over the MBD, with a Voltage floor of 2.75 Volts. Figure 5.13 shows a rapid Voltage decrease over the memristor that was unexpected, as the memristor is supposed to have a step decrease in resistance for each pulse.

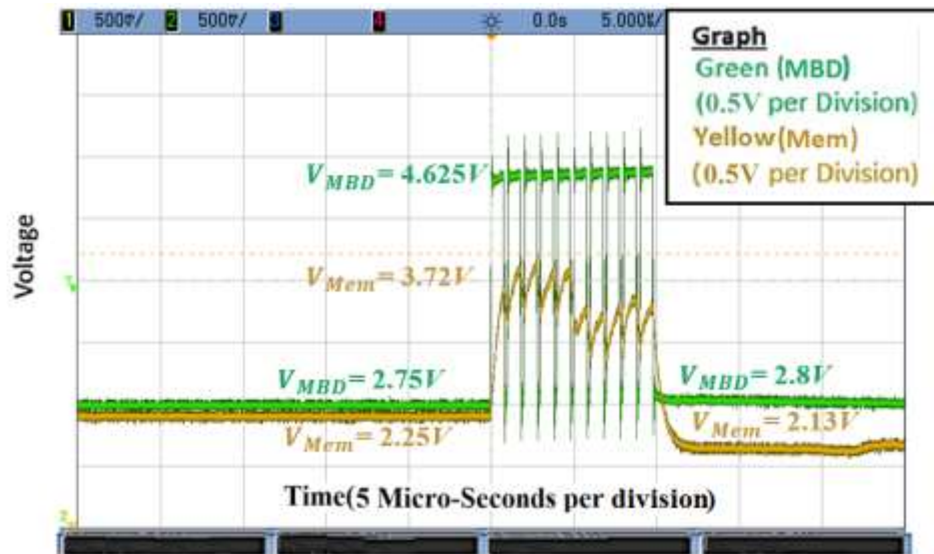

Figure 5.13 Pulsing the MBD (1) (Divider): 2.75 Volts floor, and 10 pulses of 1.9 Volts with a Width of 4 Micro-Seconds at 80% Duty Dycle.

Using the same conditions, Figure 5.14 shows a decrease in Voltage over the memristor at a steady rate of the MBD, as expected.

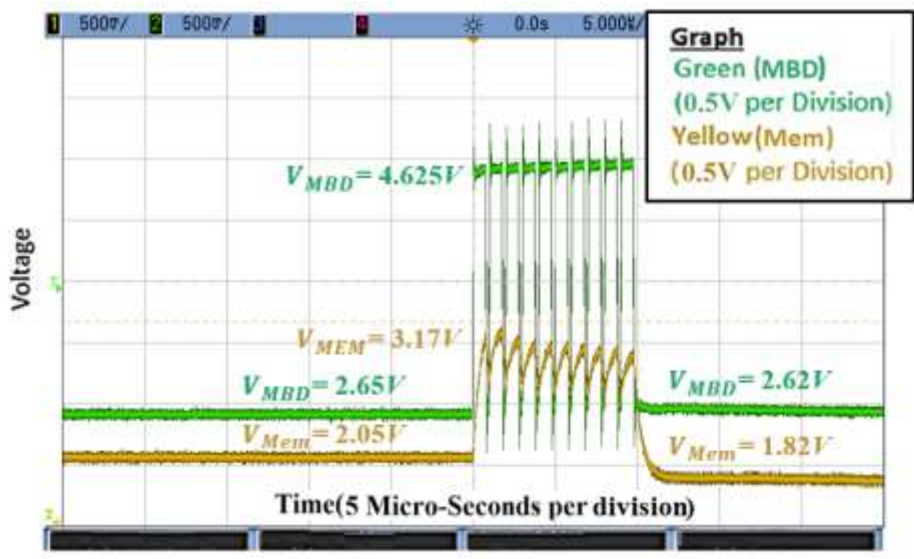

Figure 5.14 Pulsing the MBD (2) (Divider): 2.75 Volts floor, and 10 Pulses of 1.9 Volts with a Width of 4 Micro-Seconds at 80% Duty Cycle.

The Voltage over the MBD was reduced to 4.4 Volts, shown in Figure 5.15, then the Voltage over the memristor decreases steadily with each pulse for six pulses, then the Voltage increases over the memristor for the next four pulses. This showed that the PGU system was unstable, because of the PGU's floating grounds.

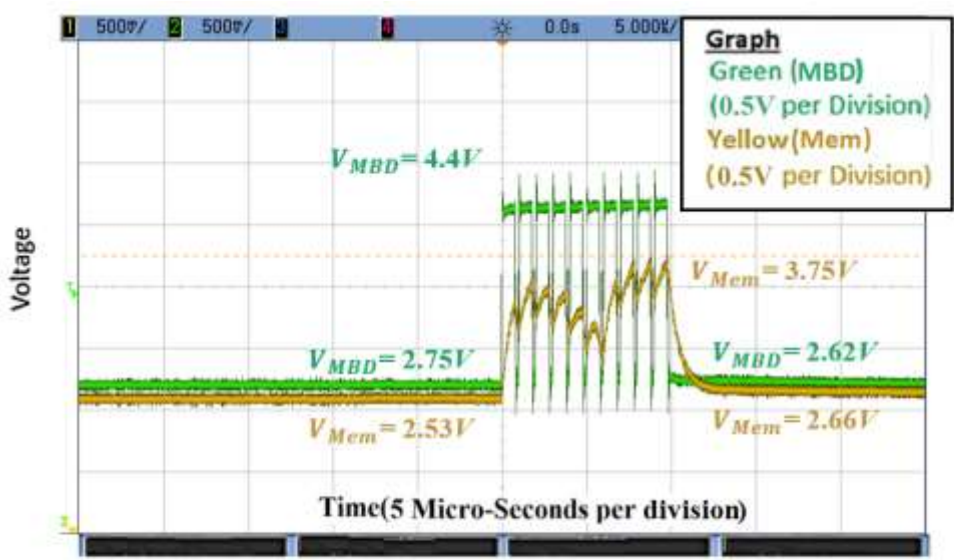

Figure 5.15 Pulsing the MBD (3) (Divider): 2.75 Volts Floor, and 10 Pulses of 1.7 Volts with a Width of 4 Micro-Seconds at 80% Duty Cycle.

PGU Setup Conclusion

The PGU workstation proved to be hard to operate because of the limited Voltages which required adjustments to the PGU station. Also, the cationic columnar memristor sometimes had to be transferred to the Micromanipulator Probe Station to lower the resistance of the memristor after the memristor entered a high resistive state, because the PGU's could not generate enough positive Voltage. The automation of the station was unable to handle all the setups of the PGUs necessary to electrically characterize the memristor and the LabVIEW program could not be easily adapted to handle the changes, also the LabVIEW was not free. The PGU station could not take a virgin device from high to low resistance and the cationic columnar memristor had to be formed at the Micromanipulator Probe Station. The instability of the floating ground made the steps of resistance of the memristor unpredictable. But the PGU station Voltage pulsing electrical characterization did show the need for a stable floating ground, a pulse generator that could produce a negative Voltage and a positive Voltage up to ten Volts, a portable station, to have a easily updatable automation for the station, and a station that is low cost.

CHAPTER 6: THE TEST AND CHARACTERIZATION PLATFORM

Introduction

After understanding the pulsing of the cationic columnar memristor and the lessons learned from the PGU station, a test and characterization test platform was constructed to solve the issues of accepting multiple MBDs with all Voltage ranges associated with them, in order to reduce the use of multiple commercial tools and stations, to solve the mobility and ease of use of tools and stations, and to reduce the high costs associated with commercial tools and stations. The next sections will describe the test characterization platform's design, the part list with the costs of the platform, the build of the platform, the programming of the platform, the results of the platform characterizing a cationic columnar memristor and the portability of the platform.

The Test and Characterization Platform Design

A simple abstract design of the test and characterization platform, shown in Figure 6.1, has a controller block, a Voltage supply unit block to the MBD block, a MBD block, the Voltage supply sources for the logic and the analog ICs, and a graphical output block. The controller will control the Voltage supplied to the MBD by a common communication interface. The controller will be programmed by a standard programing language that is free to the Researcher. The MBD must have proper access points to the Voltage applied over it, to measure the Voltage over the MBD and the memristor's Voltage. Since the analog supply Voltage will be critical, because this Voltage will be used to create the Voltage pulse applied to the MBD, this supply must have a low Voltage noise. The logic

supply will supply both the logic circuitry of the controller and the unit that supplies the Voltage to the MBD to enable of the test and characterization platform to be low cost. All units should be easily separated from each other for modularity, but still be able to protect the integrity of the operation of the test and characterization platform.

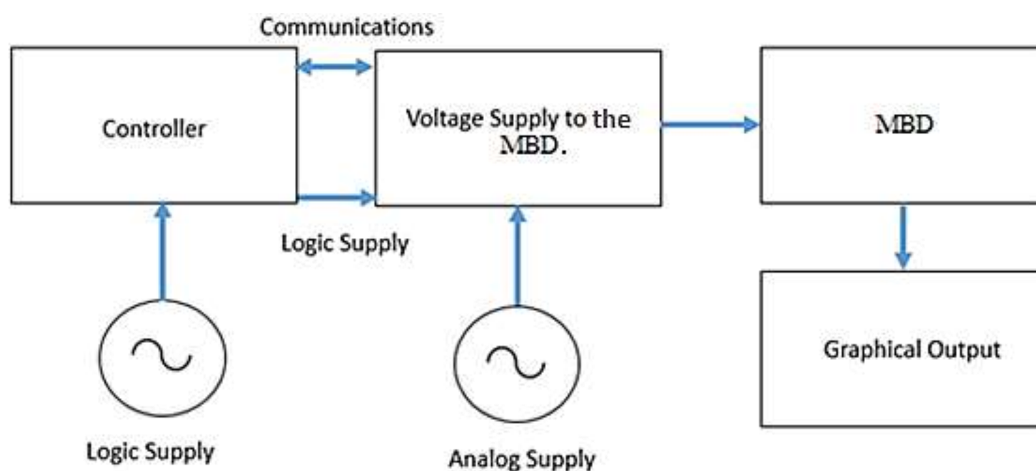

Figure 6.1 The Abstract Design of the Test and Characterization Platform

Commercially available parts were chosen for each portion of the Figure 6.1 to enable a low-cost solution for the build of the test and characterization platform. The next section of this work will discuss the parts chosen for the build of the platform and why each part was chosen. But the researcher should change any component or reprogram the firmware of the test and characterization platform for whatever the experiment dictates. For this build of the test and characterization platform, keeping the costs low but meeting the requirements was a priority.

The core of the test and characterization platform is the unit that will supply the Voltage to the MBD, since its choice will dictate the Voltage range output, the communications to other chips, the Voltage sources, and the type of controller needed. The Voltage supply to MBD is an extremely important choice, so the platform can electrically

characterize as many memristor types as possible and the lifetime Voltage range of the cationic columnar memristor built to test the platform. This results in a required Voltage output range of -3.25 Volts to 10 Volts supplied to the MBD. The part that was selected was the Maxim 5661 (MAX5661), a single 16-Bit digital to analog converter (DAC) with both current and Voltage analog outputs. The MAX5661 has a bipolar range Voltage of ±10.24V (±25% Over Voltage) with a 320u Voltage step. The ability of the MAX5661 to produce negative and positive Voltages from a single output, allows a unipolar, a near unipolar, and a bipolar memristor types to be characterized. The MAX5661 communicates with a serial peripheral interface (SPI) that is common to most controllers. The MAX5661 part requires three DC Voltage supplies for the logic (positive) and analog (positive and negative) to have a clean analog output to the MBD. The digital Voltage for the MAX5661 can range from 4.75 to 5.25 Volts. The analog Voltages supplied to the MAX5661 can range from 13.48 to 15.75 Volts for the negative and positive power supply of the MAX5661 [74].

The rise and fall times of the Voltage output of the MAX5661 are extremely dependent upon the load of the MBD. The MAX5661 can achieve a rise time (0 Volts to 5 Volts) of 120 nanoseconds and a fall time of 80 nanoseconds. The floating ground of the Max 5661 allows multiple test and characterization platforms to supply Voltage to a single MBD, and to not create shorts on the terminals of the MBD. This is important when investigating Voltage pulse collisions over the MBD, otherwise known as spike timing plasticity (STP). The choice of the MAX5661 dictates that the controller needs an SPI interface. Both the controller and the MAX5661 must have the same digital Voltage source for cost reduction.

The controller that was chosen was a Cypress Programmable embedded System-on-Chip one (PSoC 1). This controller was chosen for its simplicity of the physical hookup, the ease of programming the firmware of the PSoC 1, the SPI communication capability, and the requirement of a digital supply that is compatible with a MAX5661. The free software to write the firmware for the PSoC 1 is the "PSoC Designer 5.4". The Designer 5.4 software can use several programming languages, but the programming language used since C, as C is a common programming language. The PSoC 1 has an on-chip SPI module, and the Designer 5.4 has built-in software to control the module for the SPI. To program the PSoC 1, a mini-programmer (CY8CKIT-002 Cypress Programmer) module must be purchased, but the mini-programmer module comes with free software, "Cypress Programmer 2.0", to program the PSoC 1 with software developed in the PSoC Designer. The digital Voltage supply required for the PSoC 1 ranges from 1.71 to 5.5 Volts [75]. The PSoC 1 is a proven chip and reliable, is simple to set up and program, and is compatible with the MAX5661 digital supply requirements.

The analog Voltage supply for the MAX5661 that was chosen was a Mean Well Dual Output Switching Power Supply [76]. The Mean Well Voltage supply is a DC Voltage supply can generate 15/-15 Volts and up to 0.8 amps of current. The analog power supply was chosen for its reliability and low noise Voltage supply for the MAX5661. The digital supply is the SparkFun Breadboard Power Supply 5V/3.3V set at 5 Volts for the MAX5661 and PSoC1 [77].

The graphical output tool could be a general lab Oscilloscope, but the Discovery 2 offered by Digilant for the graphical output tool has advantages for the test and characterization platform, which are that it has an analog oscilloscope, a digital

oscilloscope, it is programmable, has input/output (I/O) ports, and it is low-cost. Programming in the Discovery 2 with its I/O ports can be linked to the PSoC I/O ports to allow the automation of data characterization, shown in Figure 6.2 [78].

Figure 6.2 Digilant Discovery 2: Digital and Analog Oscilloscope [78]

The electrical connection layout for the test and characterization platform is shown in Figure 6.3, and does not include daughter boards and connection components used to interface the I/O ports of the PSoC 1 and the MAX5661. The output compensation feedback capacitor, not shown in figure as not used, was removed from the circuit to decrease the rise and fall times of the MAX5661. No surge protection was implemented on the MAX5661, because this was optional and would increase the rise and fall times of the Voltage output of the MAX5661 [78].

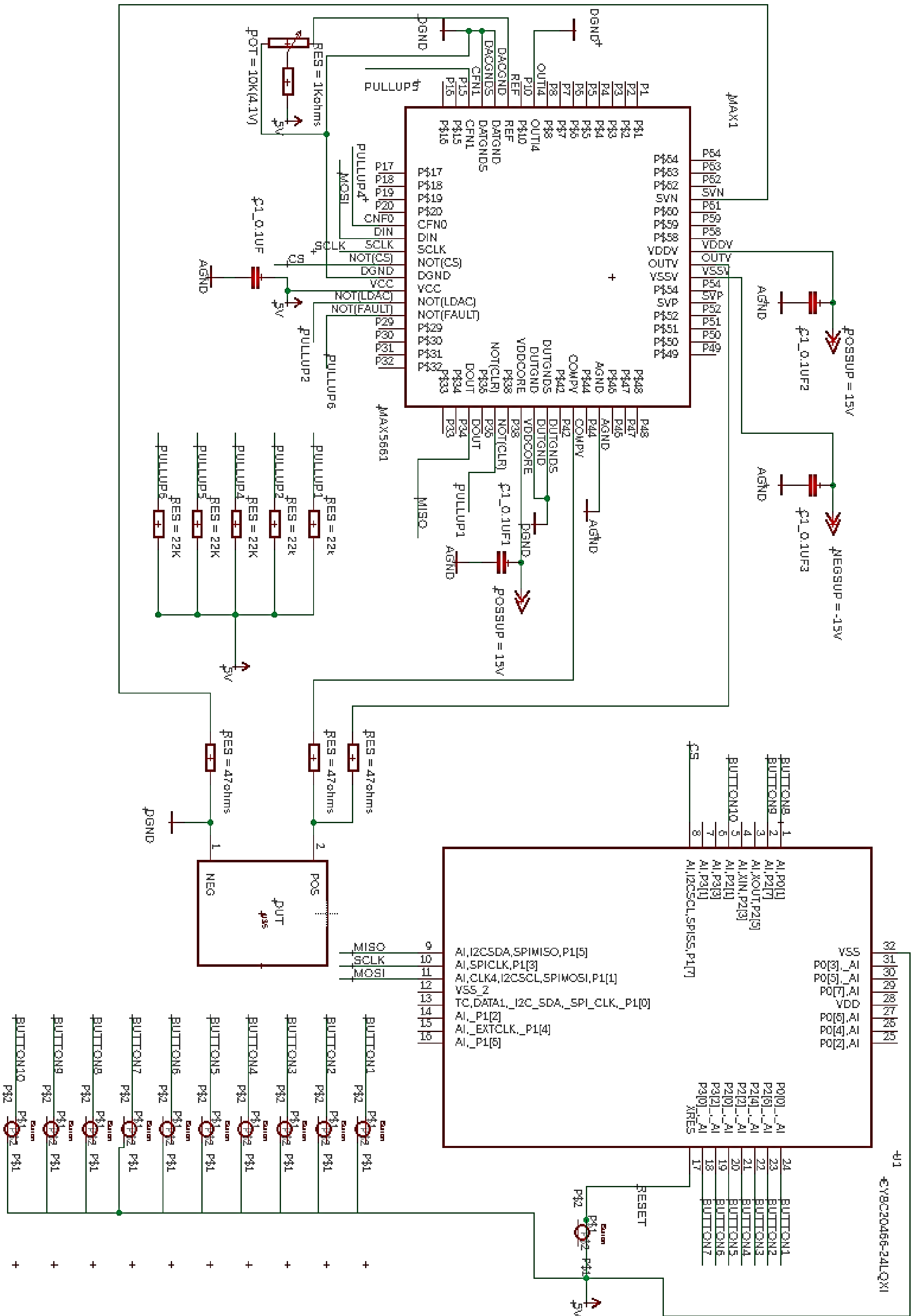

Figure 6.3 The Test and Characterization Platform Electrical Design

Several pins on the MAX5561 are pull-up resistors, shown in Figure 6.3. The pull-up pins are connected to the Voltage at the common collector (VCC) with a 22K resistor. The 22K resistor was designed to be removable, to allow the PSoC 1 to connect through either Input or Output (I/O) pins of the controller to the MAX5561. The removal of the pull-up resistors allows flexibility of the MAX 5661 operation. The pins that are pulled up are 37, 27, 9, 21, 14, and 28 which correspond to the not(CLR), not(LDAC), OUT4/0, CNF0, CNF1, and the not(fault), pins found on the pinout of the Maxim 566, shown in Figure 6.4. The Maxim 5661 pin reference, shown in Figure 6.4, has a number of pins labeled as no connect (N.C.) and they will be ignored. The hardware clear (CLR) on the MAX 5661 is not needed, since the SPI interface allows a software clear, so it was pulled up to disable the functions.

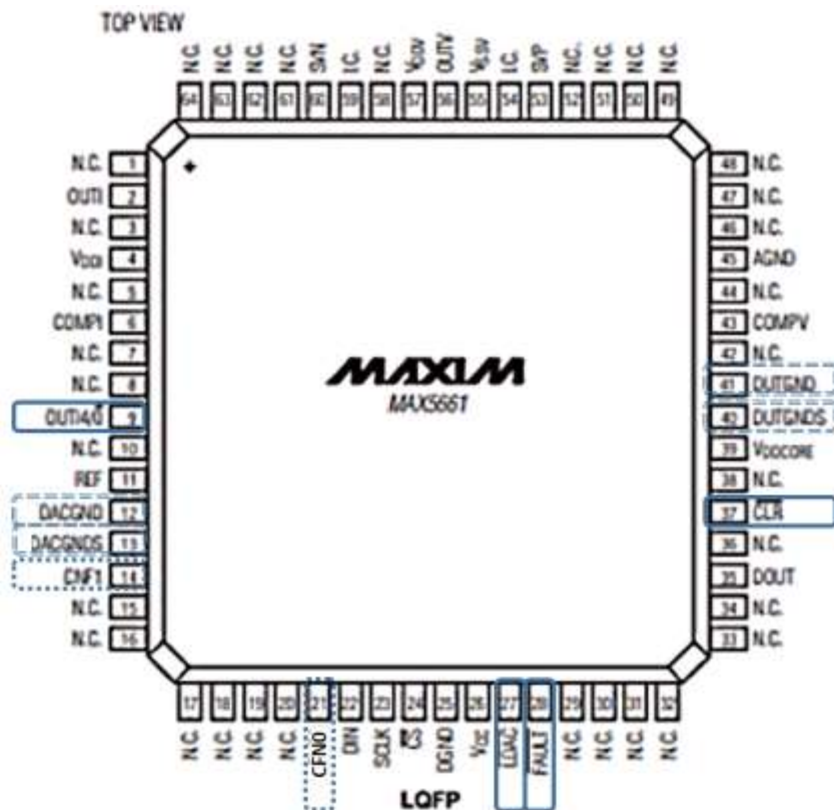

Figure 6.4 Pin Reference for the MAX5661 [78]

Pins CNF0 and CNF1 control the output of the MAX5661 by either having a ground (0) or a VCC (1). Table 6.1 shows how the CNF0 and CNF1, pins 21 and 14, can be stimulated to get the output desired.

Table 6.1 Enabling Outputs of the MAX5661 (1-Pin Set to VCC, 0-Pin Set to Ground) [78]

CFN0	CFN1	Output of the MAX5661
0	0	Both outputs disabled.
0	1	OUTI active, set to 0 to 20mA range.
1	0	OUTV active, set to bipolar mode.
1	1	Outputs controlled by serial interface.

Since a serial interface from the PSoC 1 needs to control the MAX5661 by SPI, both CNF0 and CNF1 are pulled up (11). For the SPI control, the LDAC pin that controls direct updates to the Voltage out is disabled. The OUT4/0 is for current out modifications and is not needed for the test and characterization platform and is disabled by a pull-up.

To set the reference Voltage of the MAX5661 to 4.1 Volts, as described in the datasheet, a potentiometer (adjustable 10K resistance) in series with a fixed resistor (adjustable Voltage divider) was incorporated into the design. The Voltage divider allowed the reference Voltage to be adjusted from the 5 Volts digital supply to 4.1 Volts connected the reference pin of the MAX5661. The ability to adjust the reference Voltage, in turn, adjusts the maximum Voltage output of the MAX5661.

Parts List of the Test and Measure Platform

The prices for the parts from the previous section with the support materials are listed in Table 6.2. The total cost of the parts of the test and characterization platform was $107.11, and an additional cost of the programmer for the PSoC1 was $130.00 but was not a part of the physical build of the platform, because programmers are fully packaged products.

Table 6.2 Part List for the Test and characterization Platform [74, 75, 76, 77, 78, 79, 80]

Supplier	Part	Number	Cost	Total
Maxium	MAX5661GCB+	1	$15.03	$15.03
Schmart Board	SCHMARTBOARD|EZ .5MM PITCH, 64 PIN QFP/QFN TO DIP ADAPTER	1	$7.00	$7.00
Digi-Key	CY8C20466AS-24LQXI-ND "Psoc 1"	1	$7.95	$7.95
Digi-Key	SMT ADAPTERS 3 PACK 32QFN/TQFP	1	$5.95	$5.95
	Resistors			
Digi-Key	22k Resistor CF14JT22K0CT-ND	10	$0.10	$1.00
Digi-Key	1.2 k Resisistor OX122KE-ND	1	$1.74	$1.74
Digi-Key	47ohm Resistor CF14JT22K0CT-ND	1	$0.10	$0.10
	Caps			
Digi-Key	0.1uF cap CCF14JT22K0CT-ND	6	$0.10	$0.60
Sparkfun	Solder Leaded - 100-gram Spool	1	$5.95	$5.95
Amazon	Solderable Copper Pad Extra Large Perf Board (5 pack)	1	$10.00	$10.00
Amazon	Paxcoo 17 Pcs Double Sided PCB Board Prototype Kit for DIY	1	$8.99	$8.99
Sparkfun	SparkFun Breadboard Power Supply USB - 5V/3.3V	1	$11.50	$11.50
Sparkfun	Wall Adapter Power Supply - 12VDC, 600mA (Barrel Jack)	1	$5.95	$5.95
Sparkfun	Mean Well Dual Output Switching Power Supply (15VDC, -15VDC	1	$16.95	$16.95
Sparkfun	Jumper Wires - Connected 6" (M/M, 20 pack)	1	$1.95	$1.95
Sparkfun	Break Away Female Headers - Swiss Machine Pin	1	$3.95	$3.95
The Reuseum	Bottons	10	$0.10	$1.00
The Reuseum	Pot 10k	1	$1.50	$1.50
Total				$107.11

Add Ons				
Digielent	Analog Discovery 2: 100MS/s USB Oscilloscope, Logic Analyzer and Variable Power	1	$279.00	$279.00
Lab Made	MBD	??	??	????

The Build of the Test and Characterization Platform

The Test and characterization platform build started with the MAX5661 that was soldered to the 64-pin daughter board. A star configuration was used for the MAX5661 (MAX5661GCB+) ground pins numbered 12, 13, 40 and 41, as shown in Figure 6.4. The star configuration was done to eliminate noisy ground loops by keeping the ground wires short and to connect the grounds to the same portion of the ground plane of the daughterboard (SchmartBoard) [81]. The Voltage supplies, digital and analog, have a capacitor of 0.1 pico-Farads soldered to the ground, which provide a low pass filter for the noise from the power supplies. The use of the daughterboard and its ground plane by the MAX5661 was intended to reduce noise that would affect the output of the Voltage over

the MBD and to allow a replacement if the MAX5661 is damaged. If the output Voltage of the MAX5661 is affected by noisy grounds and ground loops, this could give unexpected results of the electrical characterization of the MBD.

Figure 6.5 Daughter Board of the Max 5661

To check the operation of the daughterboard of the MAX5661 and the design of the test and characterization platform, the design was bread-boarded with the daughterboard of the MAX5661, as shown in Figure 6.6. The power supplies on the breadboard version were two Agilent E3631A, instead of the Sparkfun power supply and the Mean Well dual power supply. The MBD in this test of the design was a single fixed 22 kOhms resistor. The firmware was programmed in C and then converted to a bitstream file to program the PSoC 1(CY8C20466AS). The firmware used the SPI communication protocol package with the PSoC1 as the master and the MAX5661 as the slave. The communication pins of the PSoC 1 where connected to the MAX5661 communications pins as described in the data sheets. The program (firmware) once installed or reset on the PSoC 1, would run the firmware at the beginning of the code, which would have the MAX5661 to generate a single negative pulse and then a sine wave on the Voltage output. The PSoC 1 was soldered to the daughterboard and a button was connected to the reset pin of the PSoC1, so that the PSoC 1 could be brought back to initial conditions.

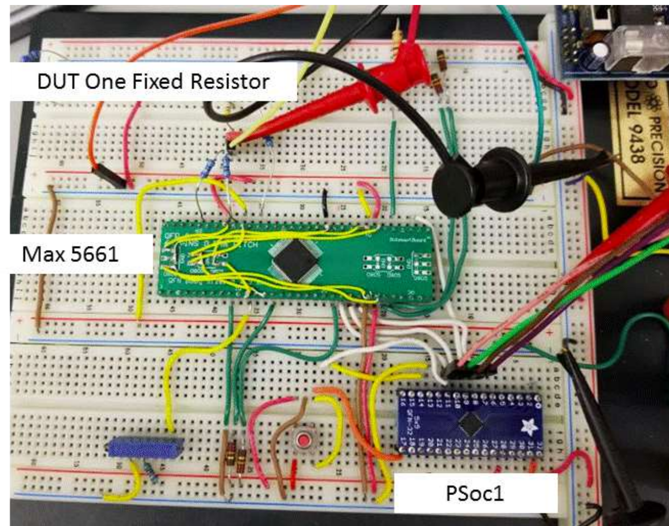

Figure 6.6 Breadboard of the Design

The PSoC 1 as the master with the MAX5661 as the slave were able to produce a sine wave with a maximum value of 10 Volts and a minimum value of -10 Volts with a negative Voltage pulse, shown in Figure 6.7.

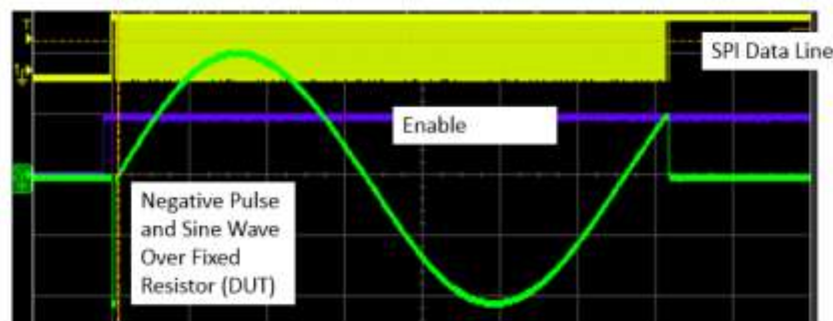

Figure 6.7 MAX 5661 Sin Wave +/-10 Volts over a Fixed 22 kOhms Resistor

After the design was confirmed, the construction of the test and characterization platform began. Individual perforated 9 (Copper and PCB perf board) boards were used to follow the block design of the test and characterization platform to enable modularity in the design. The modulation will allow different modules to be swapped out when needed or if damaged. The controller board module was built with a PSoC 1 that has buttons for

a manual interface, with a SPI interface, a Sparkfun (Breadboard) digital power set at five Volts, and solder-in pins for a programming interface, as shown in Figure 6.8.

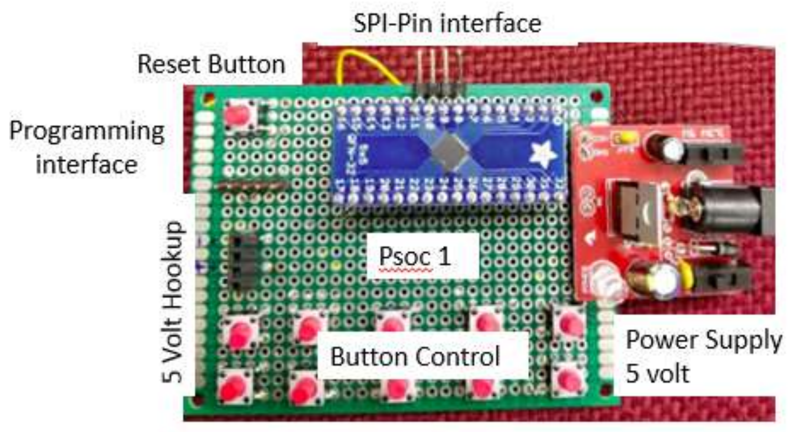

Figure 6.8 PSoC 1 and Power Supply

The module that will deliver the Voltage to the MBD will consist of the MAX5661, the pull up resistors and the POT to deliver the reference Voltage, as shown in Figure 6.9.

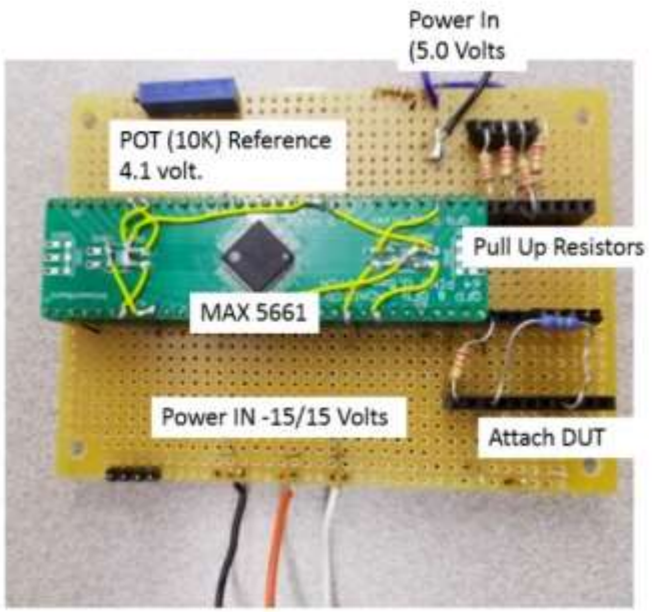

Figure 6.9 MAX 5661 Voltage Supplied to the MBD

The MBD can have many configurations, but a Voltage divider that contains a cationic columnar memristor with a shunt resistor of 22 kOhms was used to characterize the test and characterization platform, as shown in Figure 6.10. The build of the MBD module used a high frequency socket that was soldered to the perforated board to allow the memristor that was packaged to be inserted into it. This socket will allow memristors that were packaged to be exchanged for new memristors. The MBD module has electrical connections for the Voltage pulse to be applied to the MBD and for the oscilloscope to monitor the Voltage of the MBD and memristor.

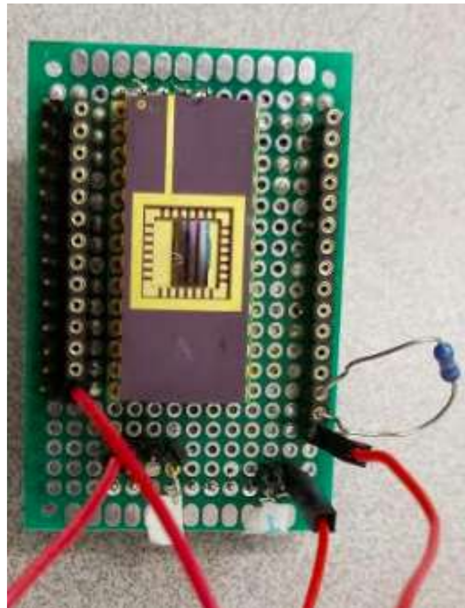

Figure 6.10 MBD (Voltage Divider)

Each module was connected together to make the test and characterization platform as shown in Figure 6.11. The power supplies and the SPI cable can be removed from the MAX5661 board to allow easy replacement of the modules. The test and characterization platform has dimensions that would fit within 23 centimeters by 20 centimeters and weighs approximately 297 grams, so in conclusion the platform is portable.

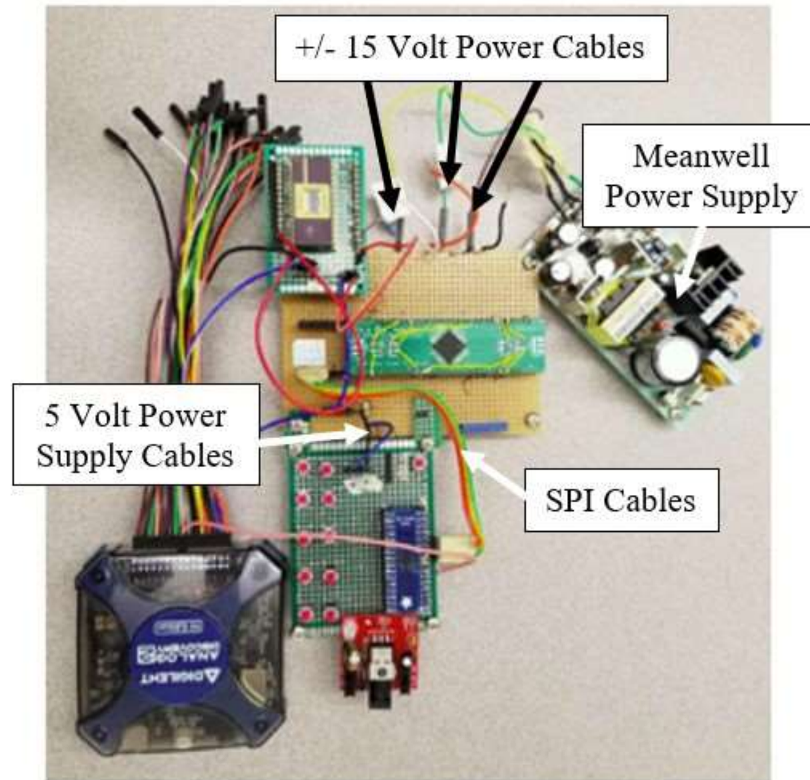

Figure 6.11 The Test and Characterization Platform

The Programming of the Platform

After the assembly of the test and characterization platform was complete, the firmware was developed. The flexibility and the ease of programming of the PSoC 1 is needed to allow new experiments to be developed on the test and characterization platform in a timely manner. Allowing the PSoC 1 firmware to be updated allows modifications of the software interface to be developed to change experiments while characterizing a memristor or when changing to new types of memristors. The physical setup to enable programming of the PSoC 1 is described below.

The first step in programming the PSoC1 is to shut down all power supplies to the test and characterization platform. This is to protect the Mini-Programmer 2 from the Voltages from the test and characterization platform. Then disconnect the SPI cable from

the PSoC1 to the MAX5661 as seen in Figure 6.12, to allow the programming by the mini-programmer 2 to the PSoC1.

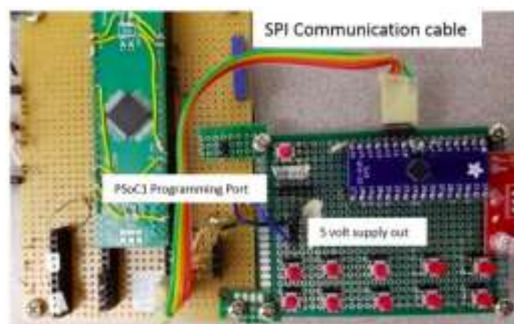

Figure 6.12 Test and Characterization Platform for Programming Description

The SPI communication cable was connected to the mini programmer with another cable, and the program port of the PSoC 1 control board, as shown in Figure 6.13. The mini-programmer 2 was connected to a laptop computer by a USB cable. Then the bitstream file was programmed from the computer to the PSoC 1.

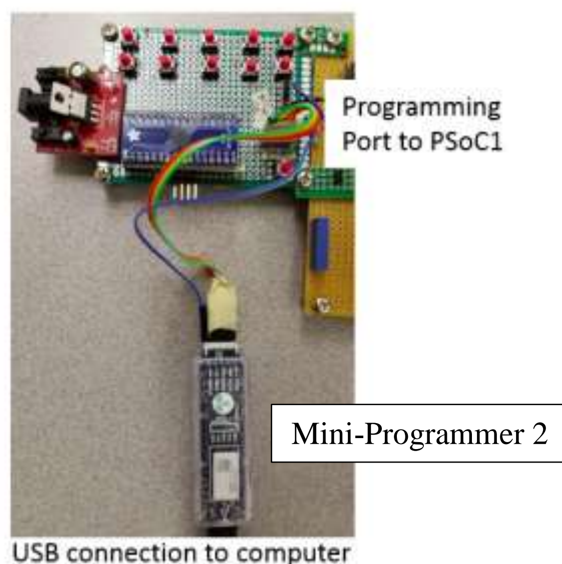

Figure 6.13 Programming Setup on the Test and Characterization Platform

To electrically characterize the memristor within the MBD by the platform, the PSoC 1 was programmed to perform a step Voltage, a positive pulse, a negative pulse and

a combination of a positive and a negative pulse by pressing the buttons described in Figure 6.14 of the PSoC 1 control board. The amplitude, the pulse width and a number of steps in the pulse ramp can be controlled through the buttons. The toggle button allows buttons 2, 3, 7 and 8 to have different functionality. The firmware can be updated to change the functionality of the buttons. This allows the platform to be easily updated as the needs of the researcher change.

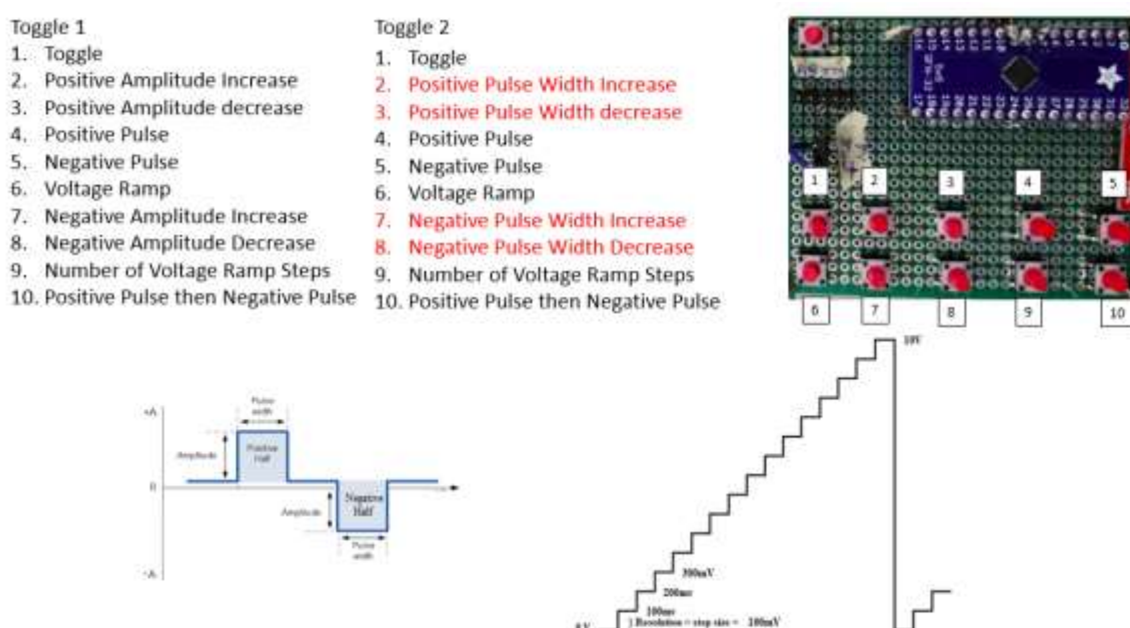

Figure 6.14 The Researcher Interface of the Test and Characterization Platform (Firmware Defined)

The Experiments Performed with the Test and Characterization Platform

After the interface was created in the firmware, experiments were performed to characterize the test and characterization platform. The experiments that were performed and described below with the MBD (Voltage divider with memristor) were done to see if the test and characterization platform can operate a memristor throughout its lifecycle (Virgin, Forming, and Operational). A virgin near unipolar cationic columnar memristor was placed into the Voltage divider of the MBD. Also, the shunt resistor in the MBD

(Voltage divider) was reduced to 22 kOhms to allow a greater Voltage across the memristor in a low resistive state.

Reducing the Virgin Memristor to a Low Resistive State

The Voltage produced over the MBD by the MAX5661 and controlled by the PSoC 1, was a Voltage step of 100 milli-Volts that was held for 300 micro-seconds and then increased by 100 milli-Volts and held for another 300 micro-seconds. This step was repeated until the Voltage reached 9.8 Volts (Step Voltage Ramp) and the duration of the Voltage ramp was 0.029 seconds. The memristor's Voltage did show some movement, displayed in Figure 6.15, as the step Voltage ramp was applied, but the memristor did not go into a low resistive state.

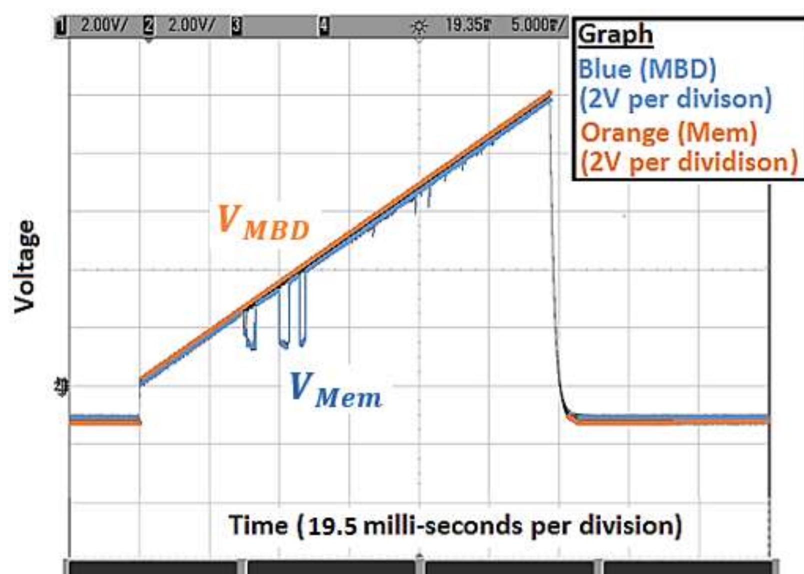

Figure 6.15 Virgin Step Voltage on Near Unipolar Memristor (Duration of Ramp Voltage Ramp 0.029 Seconds)

Another step Voltage was performed as before, but the step was held 26 milli-seconds at each step, which increased the step Voltage duration to 2.6 seconds. The step Voltage ramp reduced the Voltage over the memristor to a low resistive state, shown in

Figure 6.16. The experiment of the test and characterization platform was successful in reducing a unipolar cationic columnar virgin memristor to a low resistive state.

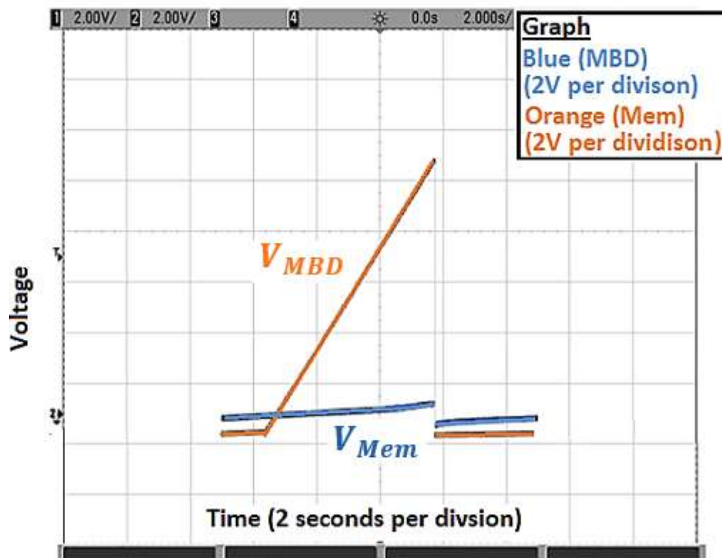

Figure 6.16 Memristor's Second Step Voltage on Near-Unipolar Sweep Memristor (Duration of Voltage Ramp=2.6 Seconds)

<u>Forming of the Memristor</u>

After the cationic virgin memristor was reduced to a low resistive state, the forming of the memristor was done. To perform the forming of the cationic columnar memristor, the step ramp was modified to a hold time of 12 milli-seconds with total ramp time of 1.1 seconds. The memristor has a capacitive component formed by the anode and cathode layers, and when a Voltage potential is applied across the memristor, an electron charge will build on the plates. Also, a potential Voltage across the memristor for an excessive time could damage the active layer. A negative pulse of -3.4 Volts was added to drain the capacitive component of the memristor before applying another Voltage. Adding a negative pulse induces a slower change of resistance, lessoning the chance of the memristor entering a very low resistive state that might damage the MBD.

Using the Voltage ramp with the negative Voltage pulse described above, the firmware was modified to run 7 times with an 80 milli-seconds negative Voltage pulse width, then pause for 1.7 seconds, and then run 7 more times with a 190 milli-seconds negative Voltage pulse width, shown in Figure 6.17. The first two Voltage ramps displayed in the Figure are the last two Voltage ramps of the seven 80 milli-seconds negative pulse width in the Figure 6.17 (a), but the Voltage over the memristor did not increase. But the second set of seven pulses with the 190 milli-seconds negative pulse width increased the Voltage over the memristor, so the resistance of the memristor increased, as shown in Figure 6.17 (b).

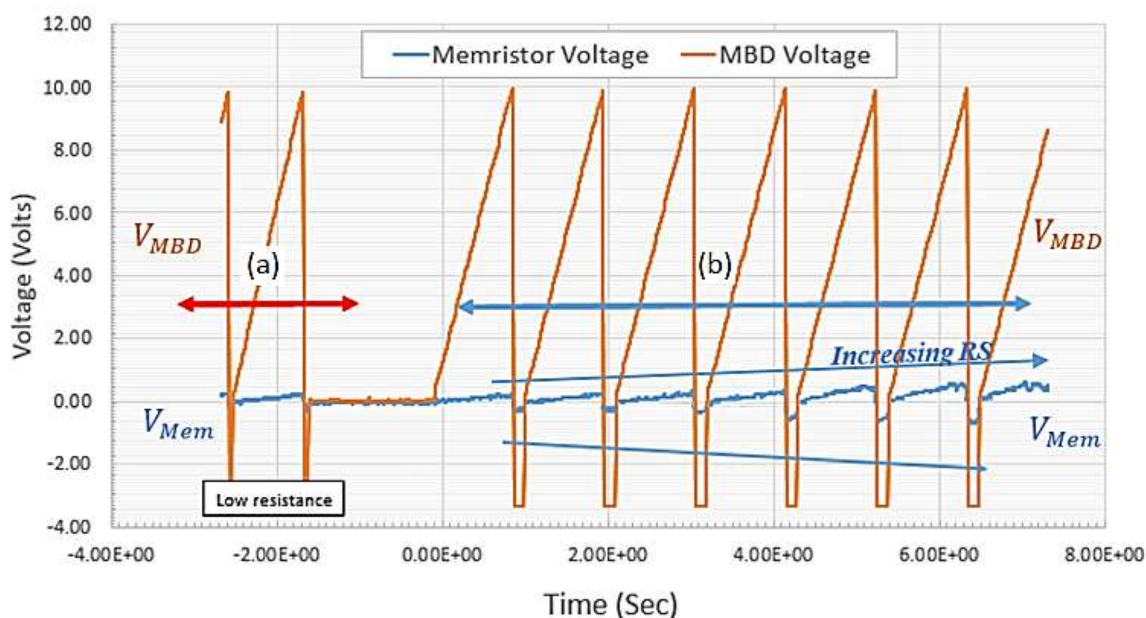

Figure 6.17 Memristor Forming (Cycling Resistance in a Low Stress Method): Positive Voltage Ramp: Voltage Step of a 100 Milli-Volts with a 12 Milli-Second Hold Time (a) Negative Voltage Pulse of -3.4 Volts Held for 80 Milli-Seconds (b) Negative Voltage Pulse of -3.4 Volts Held for 190 Milli-Seconds

After executing five more sets of seven pulses with a negative pulse width set at 190 milli-seconds the memristor entered a high resistive state. By reducing the negative pulse width to 50 milli-seconds and running 5 more times, the memristor entered a low resistive state

once again. This process of increasing resistance of the memristor and then reducing the resistance of the memristor, was done approximately 100 times to form the cationic columnar memristor. The act of cycling the resistance of the memristor with the test and characterization platform, showed that the platform is capable of forming a memristor.

Operation of the Memristor

After forming the cationic columnar memristor was completed on the test and characterization platform, an operational experiment was performed as described below, starting with the memristor in a low resistive state. To operate the memristor, memristor Voltage pulsing is necessary. Voltage pulsing of the memristor was done by the test and characterization platform from a low resistive state to a high resistive state. So, two pulses were produced by the platform over the MBD, one positive and one negative. The first pulse has a positive Voltage amplitude of 8.1 Volts and a negative pulse amplitude of -5.9 Volts, shown in the graph of Figure 6.18 (a). The resistance of the memristor after the Voltage pulses was 7 kOhms. The calculation of the memristor's resistance, with the Voltages measured over the MBD and the memristor, was done with equation (6.1), which was derived from equation (5.1).

$$\mathrm{R}_{\mathrm{Memristor}} = \frac{\mathrm{V}_{\mathrm{Memristor}}}{\frac{\mathrm{V}_{MBD} - \mathrm{V}_{\mathrm{Memristor}}}{\mathrm{R}_{\mathrm{Fixed\ Resistor}}}} \tag{6.1}$$

Shown in graph (b) of Figure 6.18, the positive Voltage pulse with an amplitude of 3.7 Volts and paired with a Voltage pulse of -3.7 Volts, increased the resistance of the memristor from 7 kOhms to 10 kOhms, shown from graph (a) to (b). After another pair of Voltage pulses were generated with a reduction of 3.4 Volts to a positive Voltage pulse of 3.9 Volts and an increase of amplitude of -0.2 Volts to -7.4 Volts, the resistance of the

memristor from graph (b) to (c) jumped from 7 kOhms to 132 kOhms. For the next two sets of pulses, the positive pulse amplitude was set to 0.4 Volts and the negative pulse amplitude was set to -7.9 Volts, the resistance of the memristor stabilizing at 330 kOhms, shown in graph (d) and (e). The experiment above shows that an operational memristor can be pulsed from a low resistive state to different states of higher resistances with the test and characterization platform developed in this work.

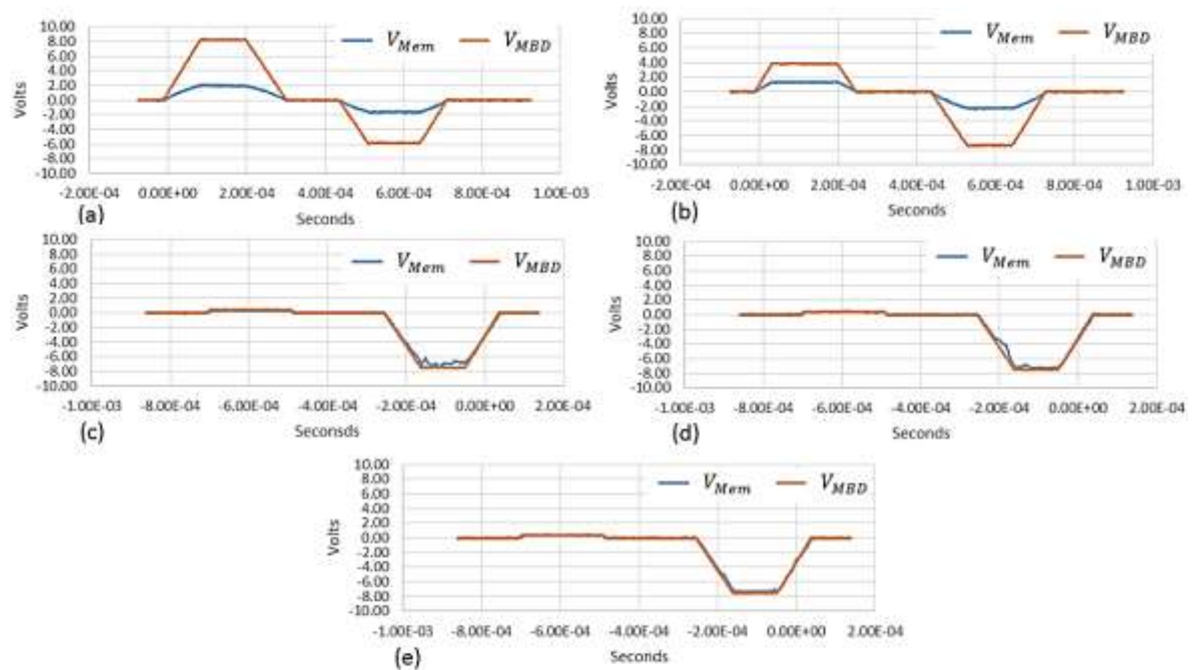

Figure 6.18 Test and Characterization Platform Voltage Pulsing (Increase Memristor to a High Resistance):
(a) $V_{MBD\ Pos}$=8.1V R_{Mem}= 7 kOhms $V_{MBD} = -5.9V$
(b) $V_{MBD\ Pos}$=3.9V R_{Mem}= 10 kOhms $V_{MBD} = -7.4V$
(c) $V_{MBD\ Pos}$=0.5V R_{Mem}=132 kOhms $V_{MBD} = -7.6V$
(d) $V_{MBD\ Pos}$=0.4V R_{Mem}=230 kOhms $V_{MBD} = -7.9V$
(e) $V_{MBD\ Pos}$=0.4V R_{Mem}=330 kOhms $V_{MBD} = -7.9V$

The next experiment was to see if the test and characterization platform could decrease the memristor's resistance incrementally by using Voltage pulses. The sequence of a positive Voltage pulse and then a negative Voltage pulse over the MBD is shown in

Figure 6.19. Graph (a) and (b) of Figure 6.19 shows the movement of the Voltage over the memristor by applying first a positive Voltage of 8.9 Volts and then a negative Voltage of 1.0 Volt over the MBD. The next set of pulses with the same conditions over the MBD on Figure 6.19 graph (c), shows a decay of Voltage over the memristor, from 8.9 Volts to 6 Volts, with the memristor's resistance of 43 kOhms. Maintaining the same pulse conditions, the next set of pulses, shown in Figure 6.19 graph (d) to (e), shows a further decay of Voltage over the memristor down to 2.5 Volts with a resistance of 7 kOhms. This experiment shows that an operational memristor can be brought down to a low resistance state incrementally, using the developed test and characterization platform.

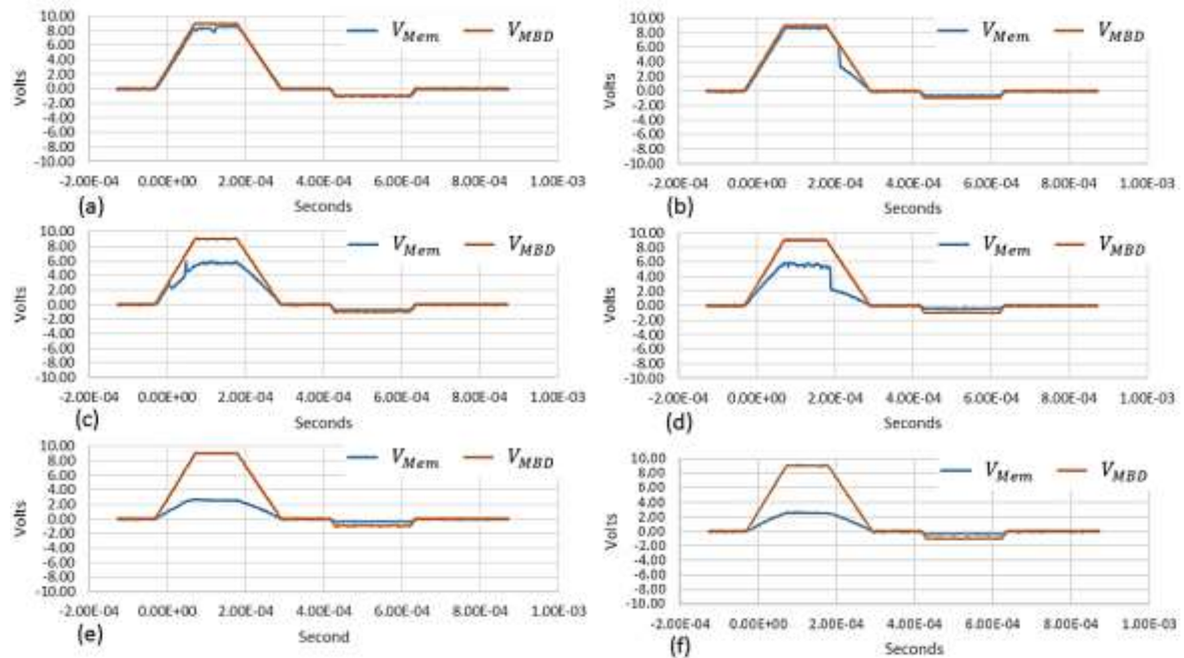

Figure 6.19 Test and Characterization Platform Voltage Pulsing (Decrease Memristor to a Low Resistance):
(a) $V_{MBD\ Pos}$=8.9V R_{Mem}=534 kOhms $V_{MBD} = -1.0V$
(b) $V_{MBD\ Pos}$=8.9V R_{Mem}=413 kOhms $V_{MBD} = -1.0V$
(c) $V_{MBD\ Pos}$=9.0V R_{Mem}= 43 kOhms $V_{MBD} = -1.0V$
(d) $V_{MBD\ Pos}$=9.0V R_{Mem}= 39 kOhms $V_{MBD} = -1.0V$
(e) $V_{MBD\ Pos}$=9.0V R_{Mem}= 8 kOhms $V_{MBD} = -1.0V$
(f) $V_{MBD\ Pos}$=9.0V R_{Mem}= 7 kOhms $V_{MBD} = -1.0V$

The summary of the experiments performed on the test and characterization platform are is as follows. The test and characterization platform could ramp a Voltage on a virgin memristor and toggle the resistance to a low Ohmic value. The developed platform could perform “forming” of the memristor by taking the memristor to a high resistive state to a low resistive state and back repeatedly. Also, the experiments of the test and characterization platform could pulse Voltage over the MBD (shunt and memristor) that would encompass most operational Voltages of many types of memristors and their variations. In conclusion, the developed test and characterization platform with the ability to pulse from -10 Volts to 10 Volts, can operate many types of memristors over their life cycle.

Multiple MBDs Constructed for the Test and Characterization Platform

The test and characterization platform has dimensions that would fit within 23 centimeters by 20 centimeters and weighs approximately 297 grams, therefore the platform is portable. The portable test platform can accept many types of MBDs. This allows the ability to experiment with designs, electrical characterization under applied external conditions, or to test silicon wafers throughout the processing of the memristor based designs or of different memristors types. Examples of different MBDs built for use in the platform are described below.

Shown in Figure 6.20, the test and characterization platform is connected to the Micromanipulator Probe Station to enable electrical characterization at the wafer level, or a bare die. This is helpful when the researcher does not need to package the memristors built, but wants to electrically characterize the MBD.

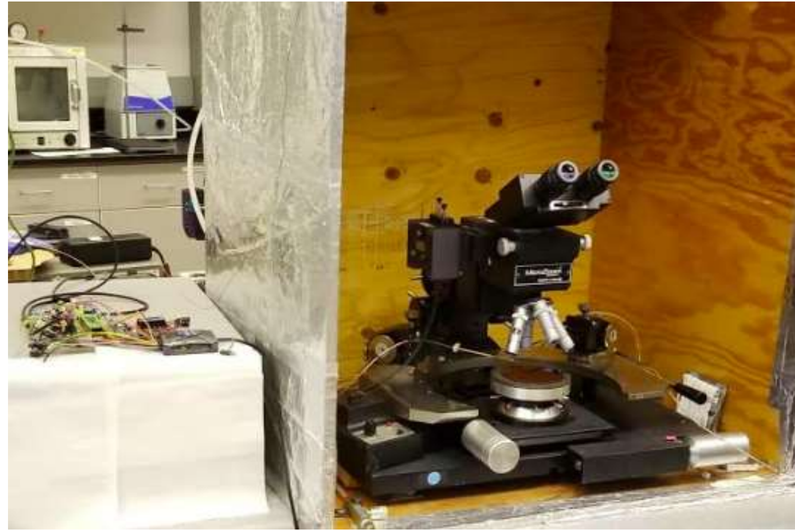

Figure 6.20 The Test and Characterization Platform can be Attached to a Micro-Manipulators for Wafer and Die Level Characterization

The Voltage divider MBD shown in Figure 6.21 has been used to test the memristor for memristor life cycle Voltages within this research. This MBD type allows ease of transition from package part to package part, oscilloscope scope access points, and the ability to characterize the Voltage over the MBD. These types of tests are used to see how the memristor will be used in a more complex design.

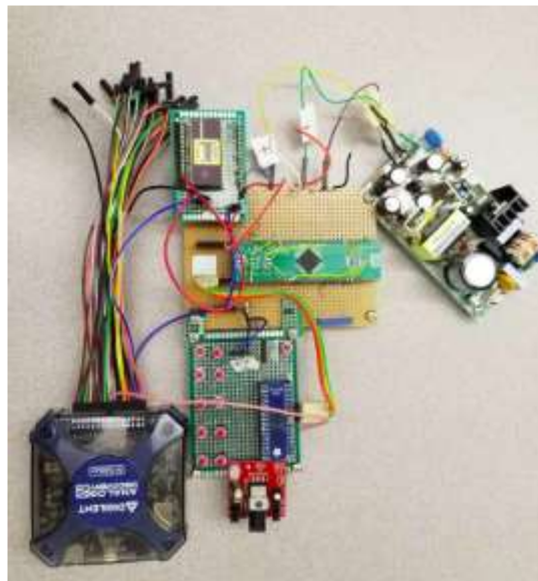

Figure 6.21 Test and Characterization Platform with Voltage Divider MBD with a Memristor Package

The MBD below in Figure 6.22 allows a heat chuck with a gas purge to be attached to the test and characterization platform. This MBD can be used for PCM memristors to perform heat ramps or eradiate the memristor, as the platform uses a low Voltage bias to check for Voltage drop or increase. This particular MBD only accepts a silicon wafer or a bare die as a design or device. The multiple MBDs constructed show that the test and characterization platform is portable and flexible.

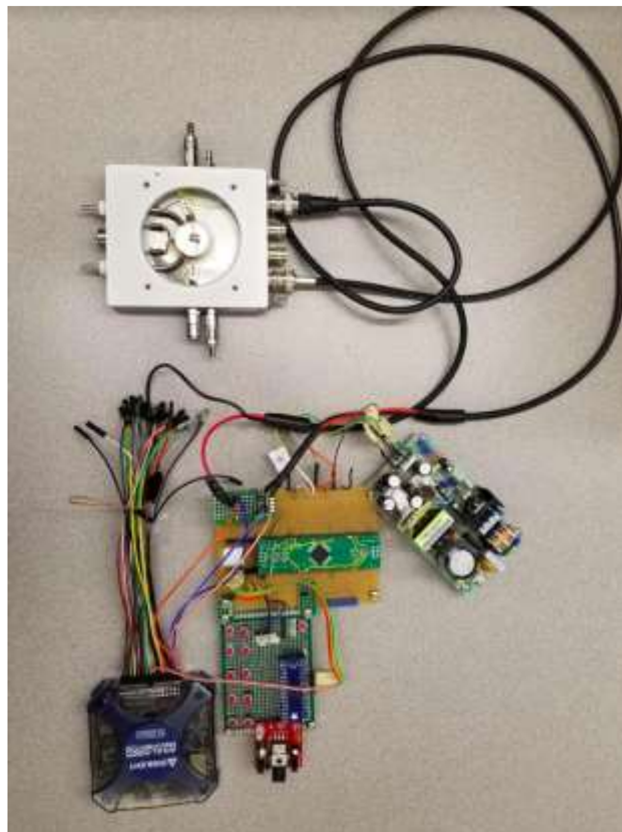

Figure 6.22 Test and Characterization Platform with MBD for Bare Die with a Heated Chuck

The test and characterization test platform can accept many types of MBDs, memristor types at different stages of processing, and memristor types under different environmental conditions, without worry of the platform being destroyed because it is low

cost. The desktop test and characterization platform developed is flexible and portable, increasing the ability of the researcher to collect more data from most memristors.

The Build of the Test and Characterization Platform Conclusion

In conclusion, the build of the test and characterization platform is modular in design. The modularity of the platform enables the exchange of the controller, the Voltage generator, and the MBDs if the modules are damaged or the requirements of the researcher change. The platform provides Voltages for the lifetime of most memristor types, and can operate unipolar, near-unipolar and bipolar memristors, making it unnecessary to switch from electrical characterization tools or stations to another tool or station. The design is portable, allowing a change in experimental conditions as the research experiments require. Also, the controller can be easily reprogrammed for automation, a new user interface control, or a new electrical characterization experiment by the researcher. The test and characterization platform was low cost and easy to build. The test and characterization platform developed will accelerate the researcher's ability to take electrical characterization under different experiments, different environmental conditions and different MBDs.

CHAPTER 7: SUMMARY AND CONCLUSION

The characterization of memristors is a difficult task due to their large variety of types. The problem is compounded by the incompatibility of the electrical characterization tools with different types of memristors, which in turn increases the cost associated with the overall integration process. This thesis presented a novel, low-cost, portable test and characterization platform for memristors with a Voltage range from -10V to +10V. To demonstrate its performance, columnar cationic memristors were characterized within this setup to study their resistance behavior. The platform has the potential to be a low-cost alternative to the traditional bulky characterization equipment and could be used to characterize many different memristor types.

Since there are many types of memristors which have different mechanisms to change their resistance and many variations within each type, a review of the literature revealed Voltage polarity differences and different operating Voltages, under Voltage pulsing and DC Voltages. The Voltage polarities of memristors are bipolar, unipolar, and near-unipolar, with a Voltage operating range that are within -3.7 Volts to 5 Volts. What was learned was that forming (+3 positive Volts to Operating Voltages) would be required in some types and variations of memristors.

The original cationic columnar memristor that was fabricated did not require forming, so the cationic columnar memristor fabricated for this work was modified to require forming. So, two modifications in the fabrication of the memristor was done. One modification was to increase the column width of the cationic memristor to allow nodules

of silver to form on the filament, and the second was to remove the photo-diffusion step of silver into the lattice structure during the fabrication of the memristor. These two modifications of the fabrication of the cationic columnar memristor required forming of the memristor.

After the investigations of the types of memristors for electrical performance, the modified cationic columnar memristor was fabricated on silicon wafers, but to demonstrate that the platform could accept packaged parts as part of an MBD, the wafer of memristors had to undergo singulation and packaging. At the wafer level and after packaging, the memristor had to show electrical functionality. The wafer and packaged part was placed on the 6200 Micromanipulator Probe Station paired with a parametric analyzer, the Hewlett Packard 4155B, to do the DC electrical characterization. The DC electrical characterization of the cationic columnar memristor demonstrated a near-unipolar electrical behavior that needed forming, with a virgin Voltage sweep of 10 Volts. After forming the memristor, the operational Voltage range of the cationic columnar memristor was -0.5 Volts to 1.5 Volts. What was learned by examining the positive side of the lifetime Voltage range, the modified cationic columnar memristor of 10 Volts was beyond the 8 Volt range of other memristor types, allowing the modified memristor to represent most memristor types. Also, the DC characterization probe station and the parametric analyzer were too bulky and not portable with a cost in the tens of thousands.

Then Voltage pulsing of the cationic columnar memristor was done by using the PGU station to reduce or increase the resistance. The PGU station consisted of two pulse generating units (Agilent 81130A), a synchronization clock (the Agilent 33521) for the PGUs, and a trigger (Agilent 33220) for the PGUs. Even though all the units of the PGU

station fit on one bench, it was not easily moved and the cost of the station was in the thousands. The station was automated by a LabVIEW program, but the LabVIEW program was ultimately abandoned because the visual language of LabVIEW after it was written, was not easily modified as the data was collected. The memristor was placed in a Voltage divider (MBD) with a shunt resistor that was below 60 kOhms, so that the memristor's resistance could be lowered by the PGU station. But even with the shunt resistor below 60 kOhms, sometimes the PGU station could not lower the resistance of a memristor while in a high resistive state, and then the memristor had to be placed back on the probe station to lower its resistance. Then after lowering the resistance, the memristor was transferred back to the PGU station for further Voltage pulsing characterization. The PGU station was able to use a Voltage pulse or a Voltage pulse burst across the MBD to increase the resistance or lower the resistance of the cationic columnar memristor. But due to an unstable floating ground of the PGUs, that produced unexpected results when the station burst pulses, burst pulsing was not predictable. The lessons learned that was applied to the test and characterization platform was an easily updated programmable controller with a common language, a pulse generating unit of the platform that has a stable floating ground, the platform must have a wide enough Voltage range to operate cationic columnar memristors, and to have portability of the platform for desktop use that enables exposed experiments to the environment (e.g. radiation).

The construction of the test and characterization platform was done next. The cost of the test and characterization platform was $107.11, with an additional cost of the programmer for the PSoC 1 of $130.00, bringing the total cost of the platform to $237.11. The critical parts for the platform are the MAX5661 pulse unit, the PSoC 1 for the

controller, a Meanwell Dual analog power supply, and a Sparkfun breadboard digital power supply. The choice of the parts was dictated by the cost and the lessons learned from the previous sections. The MAX5661 16 bit DAC was chosen to be the pulse unit because the MAX5661 has a Voltage range of ±10.24V (±25% Over Voltage) with a 320 micro Volt step that would be applied to the MBD. The cationic columnar memristor's lifecycle Voltage range of -0.5 Volts to 10 Volts and the survey of memristor type's lifecycle Voltage range of -3 volts to 8 Volts, was within the Voltage produced by the MAX5661. The step of 320 micro Volts of the MAX5661 allowed an incremental change in resistance. The PSoC 1 was chosen for the controller because of the communication protocol of SPI that is shared with the MAX5661 and the ease of programming in "C". The modularity of the platform enables the exchange of the controller, the Voltage generator, and the MBDs if the modules are damaged or the requirements of the researcher change. The low-cost and portable test and characterization platform have the dimensions that would fit within 23 centimeters by 20 centimeters and weighed approximately 297 grams. The lesson learned was that the dimensions of the test and characterization platform could be reduced if a stacked modular approach was done, not the modular side by side approach within this work.

Then the test and characterization platform demonstrated its ability to reduce the resistance of a virgin cationic columnar memristor to a low resistive state, to form the memristor by cycling the resistance, and to incrementally change the resistance of the cationic columnar memristor by Voltage pulsing. This showed the test and characterization platform was able to operate a cationic columnar memristor throughout the memristor's life cycle. Also, because of the voltage range of the cationic columnar memristance, -.5 to

10 volts, and with the platform's ability to pulse down to -10 volts, the test and characterization platform will be able to operate most memristor types throughout their lifecycle and operating voltage range.

The future work of the test and characterization platform would be to add a detection module to the platform that would detect the resistance of the memristor and store the value. Once the memristor's resistance is stored, the resistance value will be sent to the controller of the test and characterization platform. With the memristor's resistance, the controller could determine if another Voltage pulse is needed by the experiment. Another electrical characterization test performed on a memristor is spike timing plasticity, this is done by constructing multiple test and characterization platforms to apply Voltage pulses over one MBD with different time deltas between pulses, to see how the resistance of the memristor is affected. Another future configuration of a new MBD should be a cross-point array of memristors. Using the cross-point array MBD and multiple test and characterization platforms, then construct a switching module so the platform could Voltage pulse a certain coordinate (x and y) of the cross-point array to demonstrate simulated deep learning algorithms with memristors.

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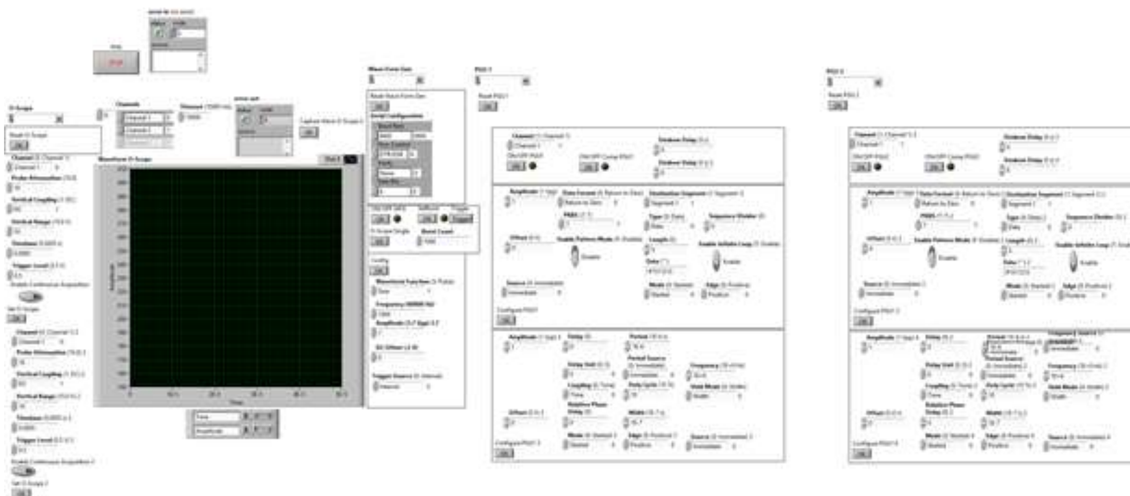
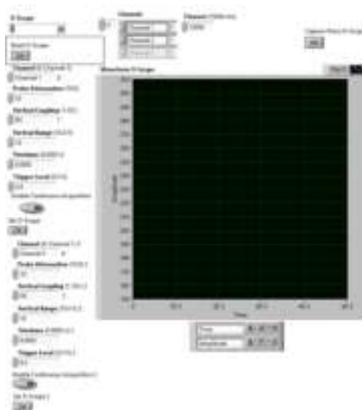
APPENDIX A

LabVIEW Program for the PGU Based System

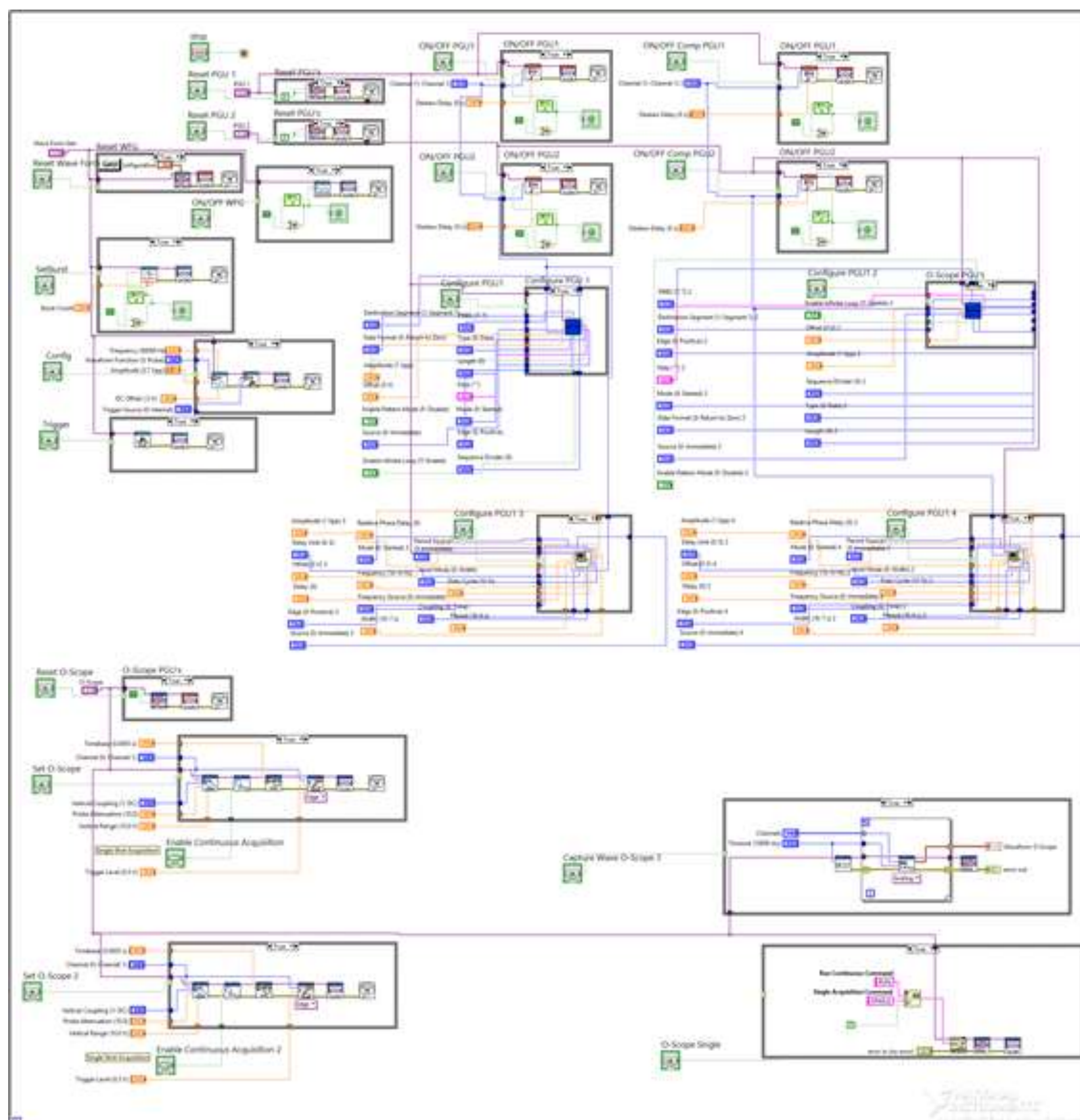
The visual programming language, LabVIEW, was used to drive the PGU based system in Figure 5.9. LabVIEW program was able to collecting data, perform instrument control with automation.



Appendix Figure A.1 LabVIEW Main Panel (Graphical User Interface)



Appendix Figure A.2 LabVIEW Graphical interface for Oscilloscope



Appendix Figure A.3 Data Flow Program for PGU Base System

APPENDIX B

PSoC firmware C code

PSoC firmware C code enables SPI communications that control the MAX5661 to increase and decrease voltage output over MBD. This code also defines the user interface (buttons).

```
//----------------------------------------------------------------------
// C main line
//----------------------------------------------------------------------

#include <m8c.h>        // part specific constants and macros
#include <string.h>
#include <stdlib.h>
#include <math.h>       // for random number generator
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules

//#include "PSoCGPIOINT.h"
#include "delay.h"            // Delays
//#include "SleepTimer.h"

// Maxim 5661 command register definitions (Table 1.)
#define MAXCMD_NOP                          0x00
#define MAXCMD_WRITE_CTLREG           0x01
#define MAXCMD_READ_CTLREG            0x02
#define MAXCMD_LOAD_INPREG            0x03
#define MAXCMD_LOAD_DACandINP 0x04
#define MAXCMD_LOAD_DACfromINP        0x05
#define MAXCMD_WRITE_CLRREG           0x06  // Only works with HW CLRb
pin
#define MAXCMD_READ_INPREG            0x07
#define MAXCMD_READ_DAC               0x08
#define MAXCMD_READ_CLRREG            0x09
#define MAXCMD_WRITE_FSOUT            0x0A
#define MAXCMD_XFER_SROUT             0x0F

// Maxim 5661 command data bit masks (Table 4.)
// Left Byte (MSB) reading from left to right
#define MAXCTL_OUTVON                 0x80
#define MAXCTL_OUTION                 0x40
// Reserved: always set to zero 0x20
#define MAXCTL_Bb_U                         0x10  // 0-Bipolar 1-Unipolar
#define MAXCTL_OUTI4EN                0x08
#define MAXCTL_14to20                 0x04
#define MAXCTL_CLRENb                 0x02
#define MAXCTL_CLRMODE                0x01
// Right Byte (LSB)
#define MAXCTL_RCLR                         0x80  // Never Use! Remains
in CLR until POR or ...
#define MAXCTL_FAULTEN                0x40
#define MAXCTL_CLRFLGEN               0x20
#define MAXCTL_FAULTV                 0x10  // RO
#define MAXCTL_FAULTI                 0x08  // RO
#define MAXCTL_CLEARST                0x04  // RO
```

```
// D1, D0 not used

#define MAXFSO_FSEN                         0x8000
#define MAXFSO_DATA                         0x03FF

#define MaximumVal                    64768 //  10.2345V
#define MinimumVal                      768 // -10.2345V
#define CenterVal               32768 //   0V

#define CMD_RAMP  1
#define CMD_SAWTH 2
#define CMD_SINE  3
#define CMD_CHIRP 4
#define CMD_MAXMIN      5

#define SSSTART_CONFIG        (SPIM_SPIM_MODE_0 | SPIM_SPIM_MSB_FIRST)

// TO DO: Setup CLRb Pin output to shut off OUTV between runs
//             Other method is to use CNF pins to turn off output

CHAR Message[]     = "Maxim MAX5661 Controller Firmware";
CHAR *pbStrPtr     = Message;
CHAR SetClrReg0V[]       = {MAXCMD_WRITE_CLRREG, 0x80, 0x00};      // 0V
= 32768
CHAR InitMAX[]           = {MAXCMD_WRITE_CTLREG, MAXCTL_OUTVON |
MAXCTL_CLRMODE, MAXCTL_FAULTEN | MAXCTL_CLRFLGEN};
CHAR InitNoClrMAX[]      = {MAXCMD_WRITE_CTLREG, MAXCTL_OUTVON |
MAXCTL_CLRENb,  MAXCTL_FAULTEN | MAXCTL_CLRFLGEN};
CHAR ClearMAX[]          = {MAXCMD_WRITE_CTLREG,
MAXCTL_CLRMODE, 0x00};       // Force the DAC to 0V? -No, to 0 DAC value
CHAR ResetMAX[]          = {MAXCMD_WRITE_CTLREG, 0x00, 0x00};
CHAR bDummy;

void printf(__flash char * expr) {
      ;
}

// Enable / Disable the SPI Slave Select
void ss_enable(CHAR enab) {
      if (enab)
            SPIM_SS__DataShadow &= ~SPIM_SS__MASK;
      else
            SPIM_SS__DataShadow |=  SPIM_SS__MASK;
      SPIM_SS__Data_ADDR = SPIM_SS__DataShadow;
}

// Send a DAC Command String (3 bytes)
void sendDacCmd(CHAR *cmdStr) {
      /* Ensure the transmit buffer is free */
      while( ! (SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY) );
      ss_enable(1);
      SPIM_SendTxData( cmdStr[0] ); /* load the command byte */

      while( ! (SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY) );
      SPIM_SendTxData( cmdStr[1] );

      while( ! (SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY) );
```

```
      SPIM_SendTxData( cmdStr[2] );
      ss_enable(0);
}

void sendDacValueSlow(unsigned int val) {
    ss_enable(1);
      /* Ensure the transmit buffer is free */
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( MAXCMD_LOAD_INPREG );
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( (BYTE)(val >> 8 ));
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( (BYTE)(val & 0xFF ));
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      ss_enable(0);
      delay_us(1);
    ss_enable(1);
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( MAXCMD_LOAD_DACfromINP );
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( (BYTE)( 0 ));
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( (BYTE)( 0 ));
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      ss_enable(0);
}

void sendDacValue(unsigned int val) {
    ss_enable(1);
      /* Ensure the transmit buffer is free */
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( MAXCMD_LOAD_DACandINP );
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( (BYTE)(val >> 8 ));
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      SPIM_SendTxData( (BYTE)(val & 0xFF ));
      while( !(SPIM_bReadStatus() & SPIM_SPIM_TX_BUFFER_EMPTY ) );
      ss_enable(0);
}
void PulseIt(unsigned int PulsMe,unsigned int PW){
                              //sendDacCmd(ResetMAX);
                              //SPIM_Start(SSSTART_CONFIG);
                              //sendDacCmd(SetClrReg0V);
                              sendDacValue(CenterVal);
                              //sendDacCmd(InitNoClrMAX);

                              //delay_us(50);
                              sendDacValue(PulsMe);//MaximumVal
                              delay_us(PW);
                              //sendDacValue(CenterVal);
                              sendDacValue(CenterVal);//ADDED!!!!
                            //sendDacCmd(ResetMAX);
}
void PulseIt2(unsigned int One,unsigned int Two,unsigned int PWP,unsign
ed   int PWN){
      PulseIt(One,PWP);
      delay_us(50);
```

```
        PulseIt(Two,PWN);
}



void RampPulse(unsigned int PulsMe,unsigned int PW,unsigned int HowMany
Steps){
                int i=1;int j=1; int PA=32768+320;int saveplac=0;
                /*sendDacCmd(ResetMAX);
                    SPIM_Start(SSSTART_CONFIG);

                sendDacCmd(SetClrReg0V);
                      sendDacValue(CenterVal);
                      sendDacCmd(InitNoClrMAX);*/
            saveplac=PA;
                for (j=1; j<= 10;j++){

                for (i=1; i<= HowManySteps;i++){
                            //delay_us(50);
                            sendDacValue(PA);//MaximumVal
                            delay_ms(PW);
                          PA=PA+320;
                      }
                      PA=saveplac;
                      sendDacValue(CenterVal);
                      delay_us(50);
                }
                      PA=320;
                            //sendDacValue(CenterVal);
                    sendDacValue(CenterVal);//ADDED!!!!
                      //sendDacCmd(ResetMAX);
}
void dataGen(CHAR cmd) {
        int i, j;
        //static int Tcount = 0;
        static float Tperiod = 30e-6; //2.54e-3;  // sec
        static float pi = 3.1415926;
        static float freq_f = 1000.0/1.2;   // Hz
        static float amp_f = 32000.0;
        static float twoPiFT;

        if (cmd == CMD_RAMP) {
              for (i=512; i<1024; i++) {
                    sendDacValue(i<<6);
                    delay_ms(1);
              }
              for (i=1023; i>= 0; i--) {
                    sendDacValue(i<<6);
                    delay_ms(1);
              }
              for (i=0; i<=512; i++) {
                    sendDacValue(i<<6);
                    delay_ms(1);
              }
        } else if (cmd == CMD_SAWTH) {
              for (j=0; j<2; j++)
                    for (i=1; i<1024; i++) {
```

```
                        sendDacValue(i<<6);
                        delay_ms(1);
                  }
            sendDacValue(CenterVal);
            delay_us(400);
      } else if (cmd == CMD_SINE) {
            twoPiFT = 2.0*pi*freq_f*Tperiod;
            for (i=0; i<512; i++) {
                  sendDacValue((unsigned int)(amp_f*(sinf(twoPiFT*i)+1.
0)));
                  delay_us(216);     // 10us with result 1.784ms
            }
      } else if (cmd == CMD_CHIRP) {
            for (i=400; i>=0; i--) {
                  sendDacValue(MaximumVal);
                  delay_us(i);
                  sendDacValue(MinimumVal);
                  delay_us(i);
            }
            sendDacValue(CenterVal);
            delay_us(10);
      } else if (cmd = CMD_MAXMIN) {
            for (i=0; i<10; i++) {
                  sendDacValue(MaximumVal);
                  sendDacValue(MinimumVal);
            }
            sendDacValue(CenterVal);
```