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Design and Realization of a Bidirectional Full Bridge Converter with Improved Modulation Strategies

Filippo Pellitteri [1,*], Rosario Miceli [1], Giuseppe Schettino [1], Fabio Viola [1] and Luigi Schirone [2]

[1] Department of Engineering, University of Palermo, 90128 Palermo, Italy; rosario.miceli@unipa.it (R.M.); giuseppe.schettino@unipa.it (G.S.); fabio.viola@unipa.it (F.V.)

[2] School of Aerospace Engineering, Sapienza University of Rome, 00138 Rome, Italy; luigi.schirone@uniroma1.it

* Correspondence: filippo.pellitteri@unipa.it

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Abstract: In this paper a Full-Bridge Converter (FBC) for bidirectional power transfer is presented. The proposed FBC is an isolated DC-DC bidirectional converter, connected to a double voltage source—a voltage bus on one side and a Stack of Super-Capacitors (SOSC) on the other side. The control law aims at the regulation either of the bus current (when the load requires power) or of the SOSC current (when the stack requires a recharge). Analysis and design of the proposed FBC are discussed. A Phase Shift Modulation (PSM) scheme is proposed, along with an improved modulation variant for the efficiency optimization, through a proper reduction of the transformer power losses. The realized prototype, compliant with automotive applications, is presented and experimental results are highlighted. The target power level is 2 kW.

Keywords: full-bridge converter; phase shift modulation; supercapacitors; isolated DC-DC bidirectional converter

1. Introduction

Energy Storage Systems allow the durable collection of electrical energy arising from different sources. With respect to the electrical grid, alternative ways of obtaining power are renewable sources and energy harvesting [1–3]. As far as storage systems are concerned, their hybridization is gathering momentum in several fields, such as automotive or aerospace, due to the opportunity to integrate different features in the same storage system. Among the possible electrical storage elements, batteries and supercapacitors offer significant benefits in terms of energy density and power density respectively, so that their combination can lead to improvements in terms of total cost and efficiency [4–9]. Investigation of possible power system architectures and power converter topologies in order to properly manage the electrical energy inside a hybrid storage system is therefore an attractive research topic [10–12].

According to specific application and power level, different types of power system architectures are possible. A common DC voltage bus is generally used to supply the existing loads and this bus could be either directly connected to a battery or connected to it through a DC-DC converter. The supercapacitor instead shall be properly managed in order to supply the load or to recharge the battery itself—a bidirectional DC-DC converter can be used for this purpose. The mentioned DC-DC bidirectional converter shall be able to control the charge/discharge of the supercapacitor from/to the bus.

State of art and future trends concerning DC-DC converters for automotive applications are widely provided in Reference [13], whereas different investigations on DC-DC bidirectional converters for both supercapacitors and battery charging applications are provided in References [14–17], with particular focus on reliability, ease of control, sizing and robustness. Due to the potentially high voltage range of

a stack of supercapacitors, proper DC-DC converter architectures could be used—in References [18–21] high-voltage-ratio topologies are described, feasible for several applications such as automotive, DC microgrids and renewable energy sources. At the same time, such high voltage levels could suggest the use of galvanic isolation in order to guarantee safety—in References [22–27] different applications of isolated DC-DC converters for energy storage management are reported.

In this paper, an insulated DC-DC bidirectional converter is proposed for the management of a hybrid storage system based on battery and supercapacitor. The proposed topology is a full-bridge converter (FBC), which has been realized and experimentally tested with two DC sources emulating a Stack Of Supercapacitors (SOSC) whose maximum voltage is 70 V and a 28 V bus. The rated power level is 2 kW. In order to avoid expensive clamping networks and maintain a high efficiency target, the conventional Phase Shift Modulation (PSM) has been modified through a novel variant aiming at reducing undesirable voltage spikes.

The proposed power converter could find its application whenever a battery-supercapacitor hybrid storage system is present—the battery provides average power, whereas the supercapacitance is able to provide the peak power pulses. Typical application examples of power system architectures are those inside an Electric Vehicle (EV), based on an automotive DC voltage bus or inside a space launcher, based on an avionic DC voltage bus.

This paper is organized as follows—Section 2 provides a description of the proposed power system architecture and analyzes the proposed bidirectional DC-DC converter; Section 3 focuses on the Full Bridge converter design, accordingly, comparing different modulation strategies; Section 4 reports experimental results concerning a Full Bridge converter prototype, able to transfer a 2 kW power; in Section 5 conclusions are given.

2. Analysis of the Full Bridge Converter (FBC)

The aim of the proposed DC-DC converter is to manage the energy flow between two energy sources, being in the specific case a Stack Of Supercapacitors (SOSC) and a DC voltage bus, as highlighted in Figure 1, showing the power system architecture. A typical current profile, required from the bus section, is highlighted as well: the positive current values correspond to a SOSC discharge, whereas the negative ones correspond to a SOSC recharge. The maximum required current value is 70 A, which is equivalent to a maximum rated power of 2 kW for a nominal DC bus voltage equal to 28 V.

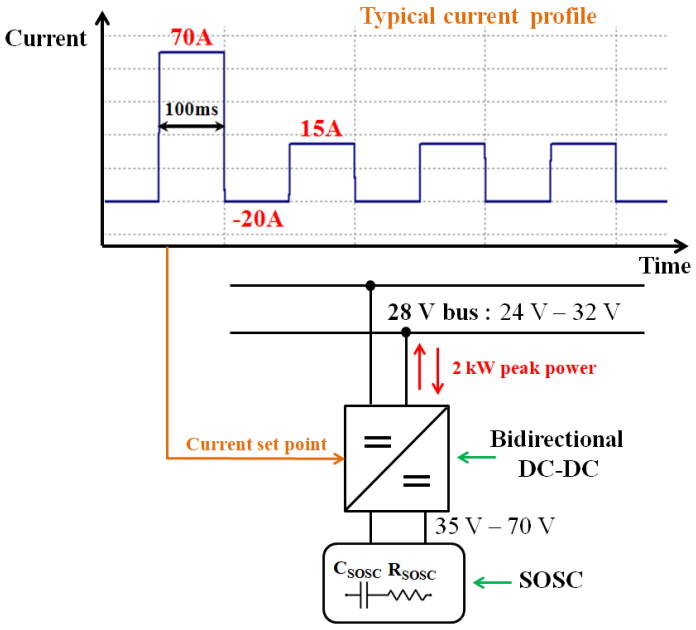

Figure 1. Power system architecture.

2.1. Energy Sources Model

The SOSC voltage lies in the range 35 V–70 V, whereas the nominal DC bus voltage is 28 V. In Table 1 the SOSC parameters and voltage range are reported, where C_{SOSC} and R_{SOSC} are the SOSC equivalent capacitance and resistance. The reported values arise from the considered specific stack, which is supposed to be a 26s11p (26 series–11 parallel) connection of 2.7 V 10 F 35 mΩ ultracapacitor cells (Maxwell Technologies, San Diego, CA, USA).

Table 1. Stack of Super-Capacitors (SOSC) parameters and voltage range.

C_{SOSC}	R_{SOSC}	V_{min}	V_{max}
4 F	70 mΩ	35 V	70 V

Being equal to the product between C_{SOSC} and R_{SOSC}, the SOSC charge/discharge time constant is equivalent to hundreds of ms, so that the SOSC can be considered as a DC power source with respect to a converter switching frequency in the order of tens-of-kHz. For this reason the proposed converter can be analyzed and designed as an actual DC-DC converter.

In Table 2 the DC bus specifications concerning the voltage level are reported.

Table 2. DC bus voltage minimum, nominal and maximum level.

V_{min}	V_{nom}	V_{maz}
24 V	28 V	32 V

2.2. Full Bridge Converter Analysis

In Figure 2, the schematic of the proposed Full Bridge Converter (FBC) is shown. The FBC is an insulated topology, featuring a transformer between the sections connected to the DC voltages V_1 and V_2, representing the SOSC and the bus respectively. As far as the transformer is concerned, L_1 and L_m are the equivalent primary leakage and magnetizing inductances respectively, whereas *n:m* is the turns ratio. Each of the H-bridges in the primary and in the secondary side of the transformer consists of four switches, in this specific case four enhancement n-channel MOSFETs—the primary side H-bridge consists of M1-M2-M3-M4, whereas the secondary side one consists of M5-M6-M7-M8. In this network therefore energy can flow in both directions, either from V_1 to V_2 or from V_2 to V_1—in the first case the primary H-bridge acts as an inverter and the secondary one as a rectifier, in the second case the H-bridges play the opposite roles.

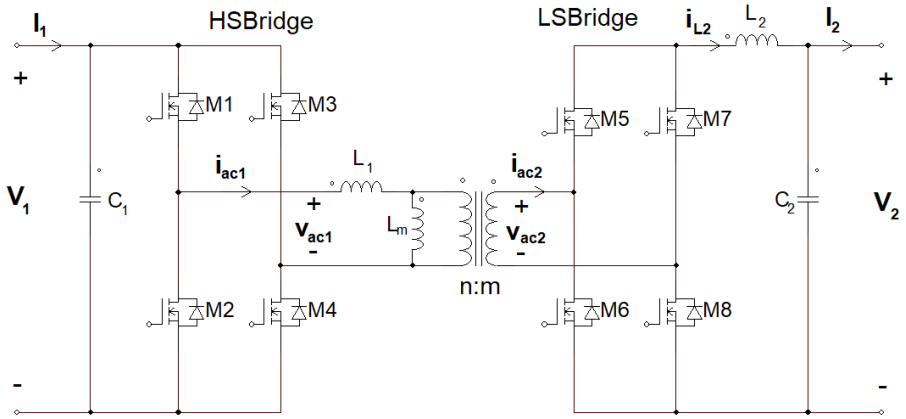

Figure 2. Schematic of the Full Bridge Converter (FBC).

If a voltage source is connected to V_1 port and a load is connected to V_2 port, the proposed converter implements a step-down operation.

The primary and secondary H-bridges can therefore be referenced as High-Side Bridge (HSBridge) and Low-Side Bridge (LSBridge).

L_2 is the converter inductor, placed in series with the LSBridge.

2.3. Possible Modulation Techniques

Two possible modulation schemes have been investigated on the proposed FBC, as shown in Figures 3 and 4, *Vgn* being the logic level applied to the gate-source voltage of the MOSFET Mn—the Pulse Width Modulation (PWM) and the Phase Shift Modulation (PSM).

Figure 3 shows the PWM scheme—M1 and M4 gate signals are in phase, as well as M2 and M3 gate signals and a phase difference occurs between the diagonals M1–M4 and M2–M3; the secondary-side gate signals are obtained by logical negation (NOT) of the primary-side signals, as highlighted in the figure. The on-time of each HSBridge switch is *DTs*, where *D* is the duty-cycle and *Ts* the switching period, being the duty-cycle limited to less than 50% in order to avoid short-circuit at the primary side.

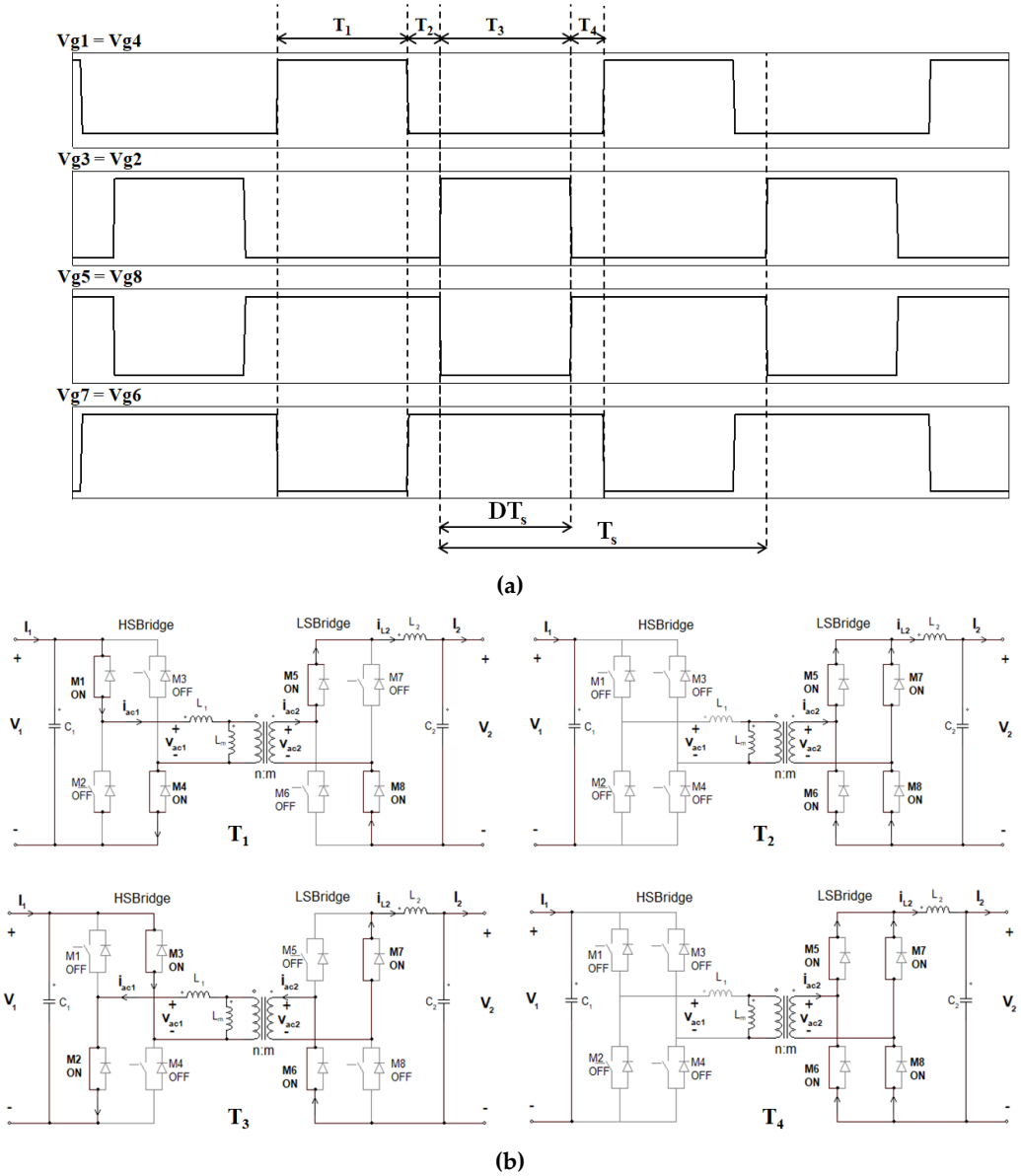

Figure 3. Pulse Width Modulation (PWM) case: (**a**) gate signals; (**b**) modes of operation.

As highlighted by the modes of operation, if D goes higher than 50%, the time windows T_2 and T_4, corresponding to the L_2 discharge towards short circuit, would be deleted, thus avoiding a proper converter working; moreover, the time windows T_1 and T_3 would be in overlap, thus leading to an undesirable short circuit on V_1.

Figure 4 shows the PSM scheme—M1 and M2 are always in phase opposition, as well as M3 and M4; a phase difference, corresponding to the duty-cycle D, occurs between them. The PWM, therefore, is converted into a phase shift modulation.

At the same way as in the PWM, the duty-cycle D is limited to less than 50% in order to avoid open-circuit at the secondary side, which could lead to voltage spikes due to the inductance L_2.

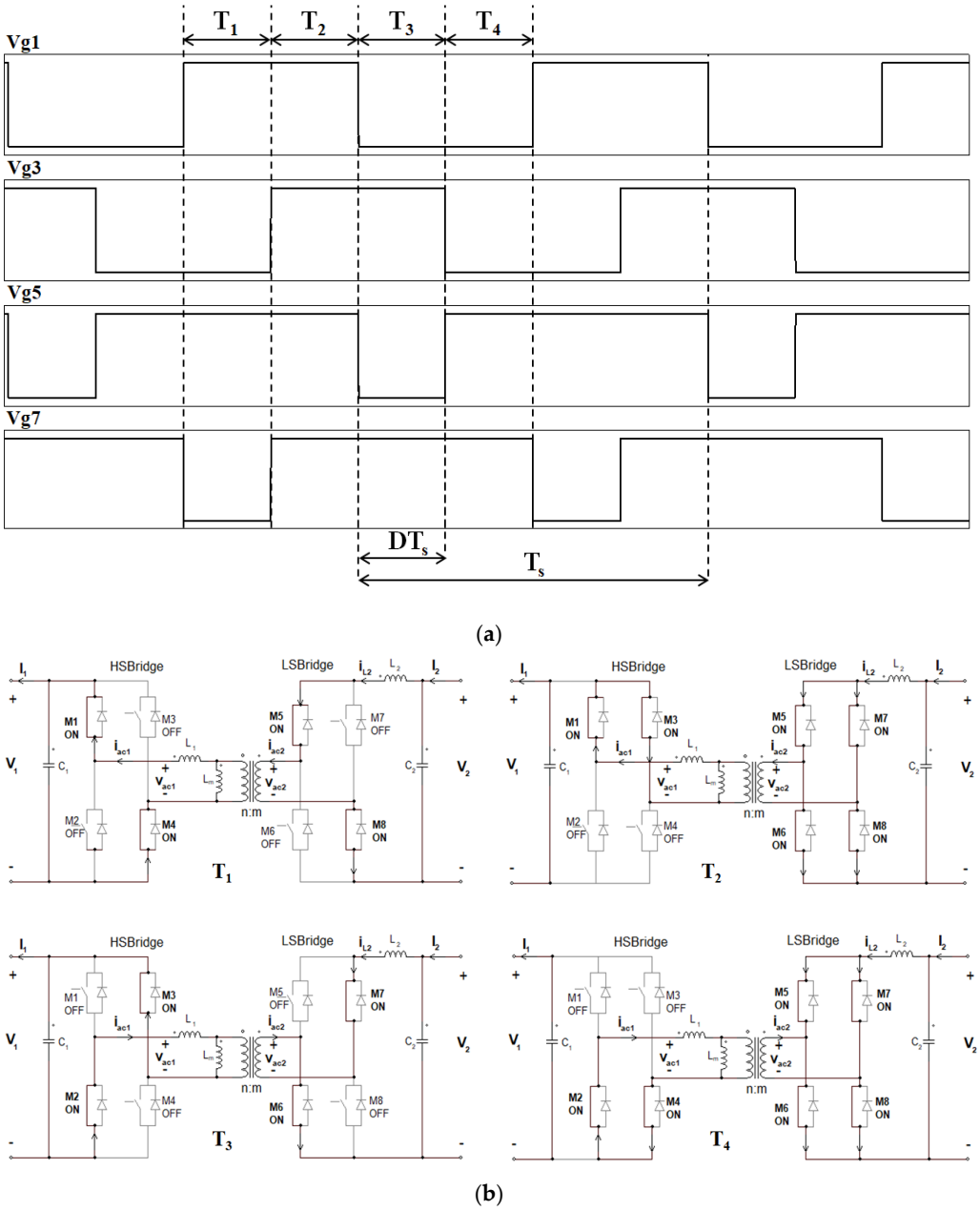

Figure 4. Phase Shift Modulation (PSM) case: (**a**) gate signals; (**b**) modes of operation.

As highlighted by the modes of operation, if D goes higher than 50%, the time windows T_2 and T_4, corresponding to the L_2 discharge towards short circuit, would be deleted, thus avoiding a proper converter working, such as in the PWM mode; moreover, the time windows T_1 and T_3 would be in overlap, thus leading to an undesirable open circuit on L_2.

The PSM scheme has been preferred to the PWM, since the PWM scheme involves higher switching power losses, due to the Zero Voltage Switching (ZVS) condition which is reached in the PSM.

The proposed converter aims at the regulation of the power in terms of both amount and direction.

Considering that V_1 and V_2 are two DC voltage sources—a Stack Of Supercapacitors and a DC bus respectively—the power regulation is therefore consisting in a current regulation.

3. Design and Modulation Strategies for the Proposed Converter

3.1. Choice of the n:m Transformer Ratio

In a conventional full-bridge converter, with a resistive load at its output, the ratio of the output voltage V_2 to the input voltage V_1 is equal to:

$$\frac{V_2}{V_1} = \frac{2mD}{n}. \tag{1}$$

This means that for the designed power converter, where voltage sources are applied at both ports (the V_1 SOSC source at the input and the V_2 bus source at the output), this condition corresponds to a "current balance," meaning that no DC current is flowing.

In order to produce a current flow, this condition shall be modified. If the SOSC has to discharge into the bus, the duty-cycle, representing the control parameter, shall be increased towards the maximum limit, that is $D = 0.5$.

The most critical condition is represented by the minimum voltage difference between SOSC and bus, that is when the SOSC is at its minimum voltage ($V_1 = 35$ V) and the bus is at its maximum voltage ($V_2 = 32$ V). In this condition, the V_2-to-V_1 ratio is at its maximum value, so that, considering that D must be less than 0.5, the secondary-to-primary ratio $m{:}n$ shall be higher than 1 according to (1), especially considering the case of a positive bus current I_2. For this reason, the selected n and m have been chosen according to the following ratio:

$$n : m = 2 : 3. \tag{2}$$

A higher-than-1 turns ratio is even more required considering the voltage drop in the primary side, due to the R_{SOSC}, possibly leading the voltage V_1 from 35 V to less than 32 V and all the voltage drops concerning the different components.

If the leakage inductance effect is neglected, the L_2 average current $I_{L2,av}$, corresponding to the bus current, is the following:

$$I_{L2,av} = \frac{2\frac{m}{n}DV_1 - V_2}{R_{eq} + \left(2\frac{m}{n}D\right)^2 R_{bosc}} = I_2, \tag{3}$$

where R_{eq} refers to all the resistive losses in the converter.

3.2. Modulation Strategies

In Figure 5, all the eight gate signals in the case of the previously described Phase Shift Modulation (PSM) are shown in simulation.

As expected by the modulation law and highlighted by the figure, each LSbridge gate signal event is simultaneous with an HSbridge gate signal event.

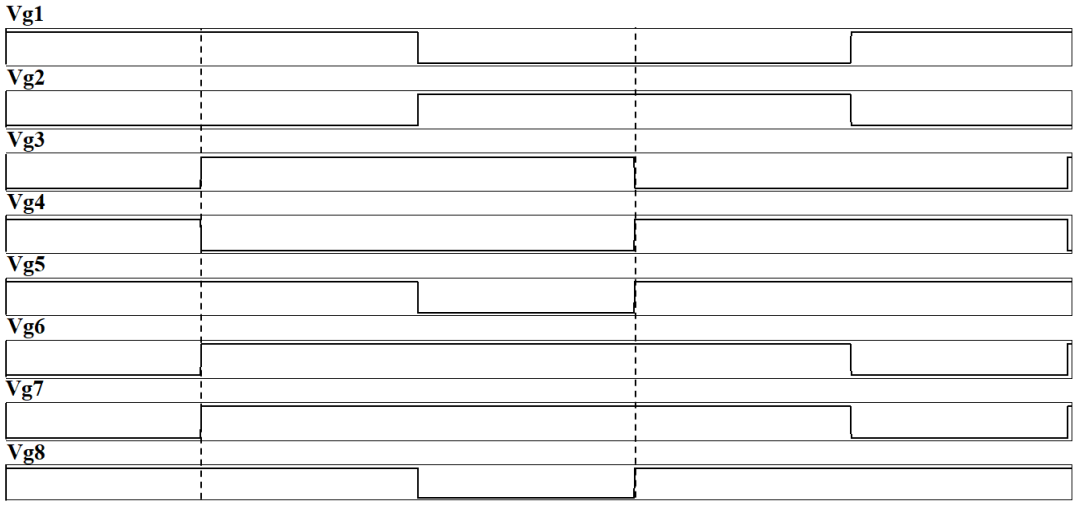

Figure 5. Gate signals in conventional PSM.

In Figure 6, the resulting secondary-side waveforms are highlighted, where V_{L2} is the voltage at the output of the LSbridge and T_s is the switching period.

The considered case concerns the SOSC recharge, that is when I_2 is negative and $I_{L2,av}$ as well. In this case, I_{L2} is divided into the drain-source currents of M5 and M7. Every $T_s/2$, whenever Vg5–Vg8 or Vg6–Vg7 goes low, that is when M5 or M7 is opened, there is no conduction path through the opened MOSFET, due to the reverse direction of the MOSFET-connected diode. Therefore, if before the switch opening the drain-source current on the other switch was negative, a voltage spike on V_{L2} is provoked since the inductor energy is not free to circulate. This is better highlighted in Figure 7.

A useless energy waste is therefore shown in case of energy flow from V_2 to V_1 with the conventional PSM.

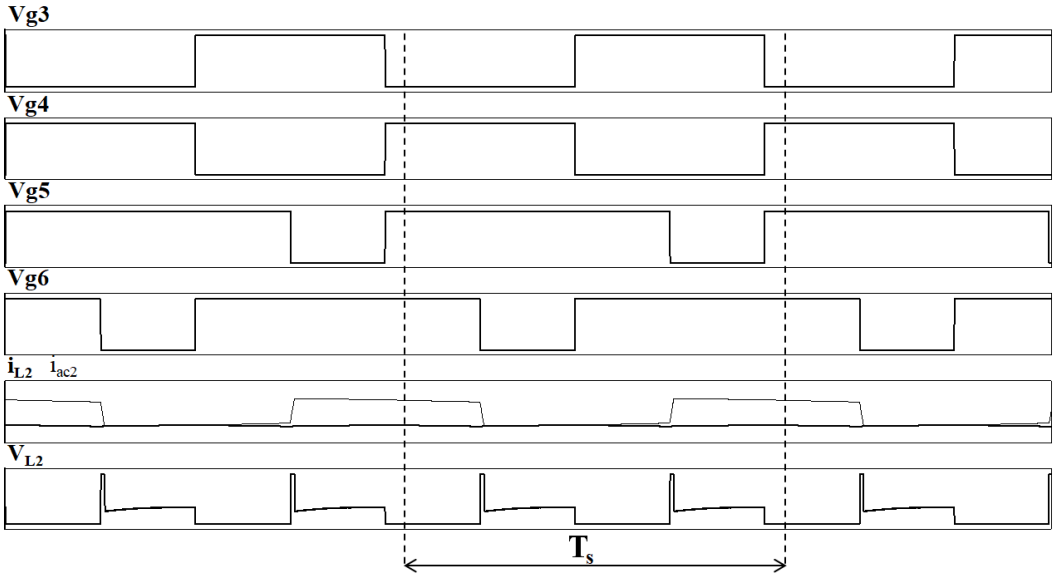

Figure 6. Secondary-side waveforms for the conventional PSM.

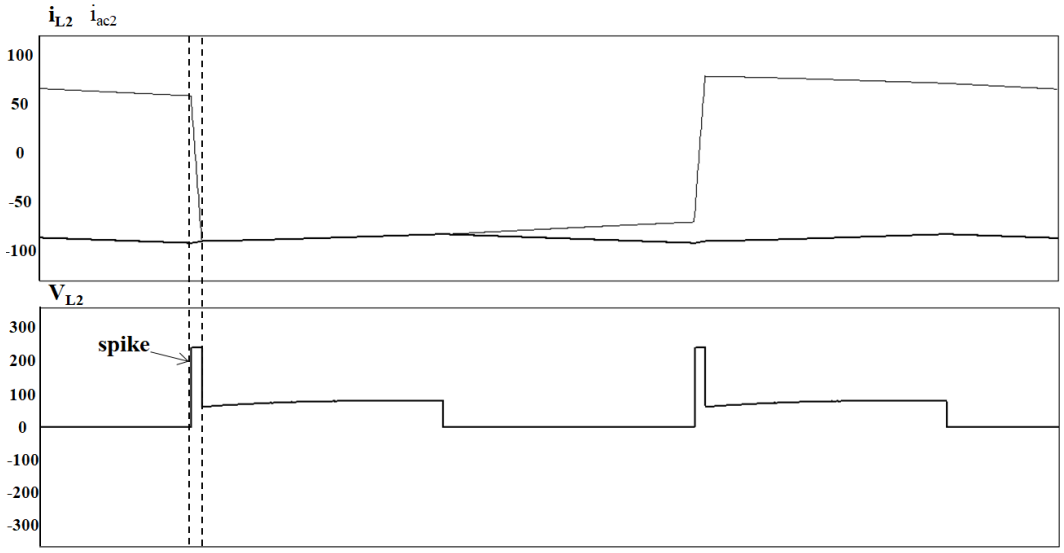

Figure 7. Zoom on the secondary-side waveforms for the conventional PSM.

In order to avoid the mentioned voltage spikes, thus avoiding to limit the overall power system efficiency or to add an expensive clamping network, an improved modulation strategy is proposed in the following.

In Figure 8 the gate signals concerning the proposed modified Phase Shift Modulation (PSM) are shown in simulation.

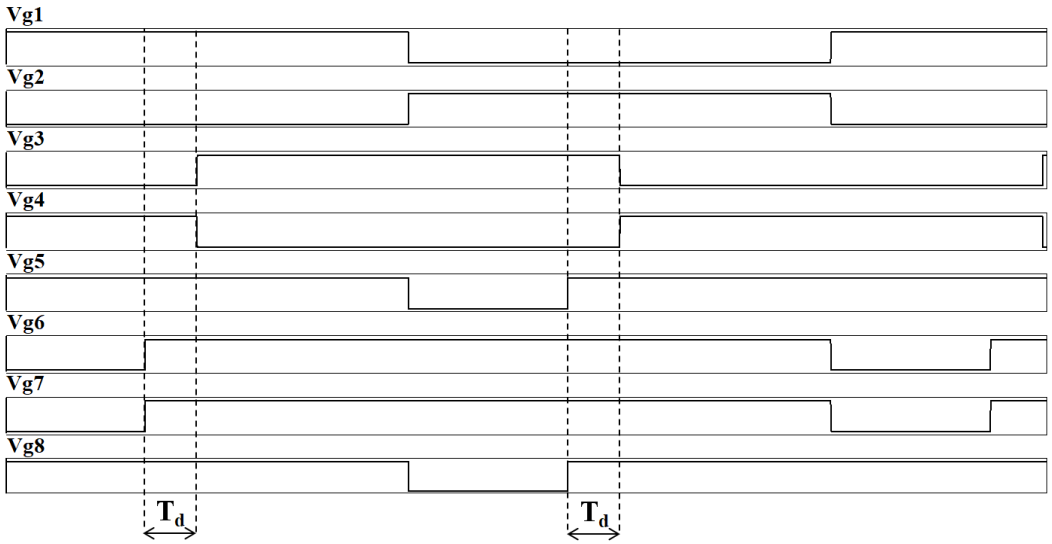

Figure 8. Gate signals in modified PSM.

The aim of the improved control law is to open M5–M8 (M6–M7) when the drain-source current on M6–M7 (M5–M8) is positive (negative), that is when i_{ac2} is positive (negative). In order to reach this goal, the positive events of Vgn concerning the LSbridge are anticipated by a time window, referenced as T_d, so that i_{ac2} has the time to reverse its sign.

In Figure 9, the resulting secondary-side waveforms are highlighted—this time V_{L2} presents the ideal shape, as better highlighted by Figure 10.

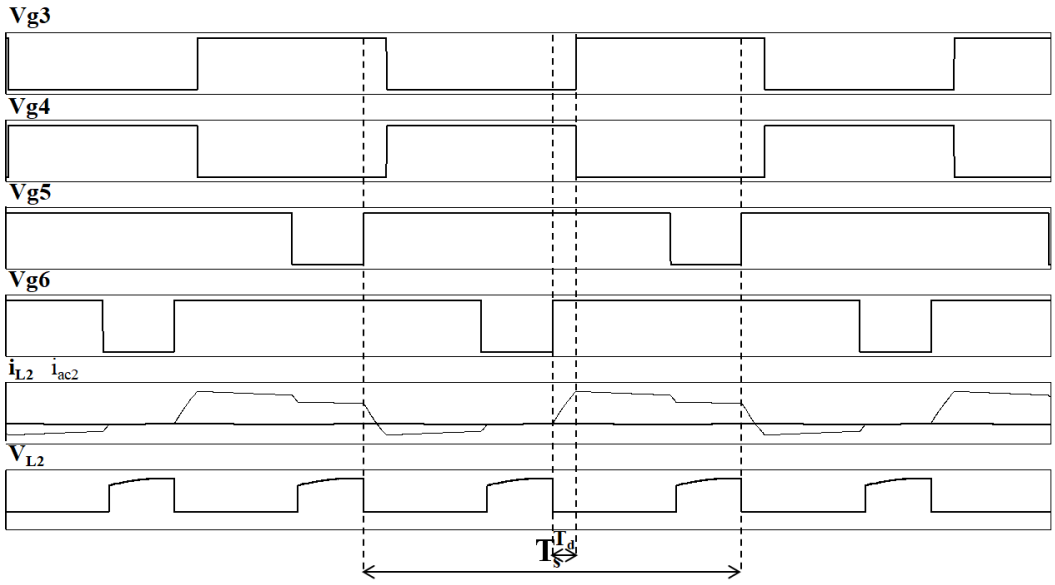

Figure 9. Improved secondary-side waveforms for the modified PSM.

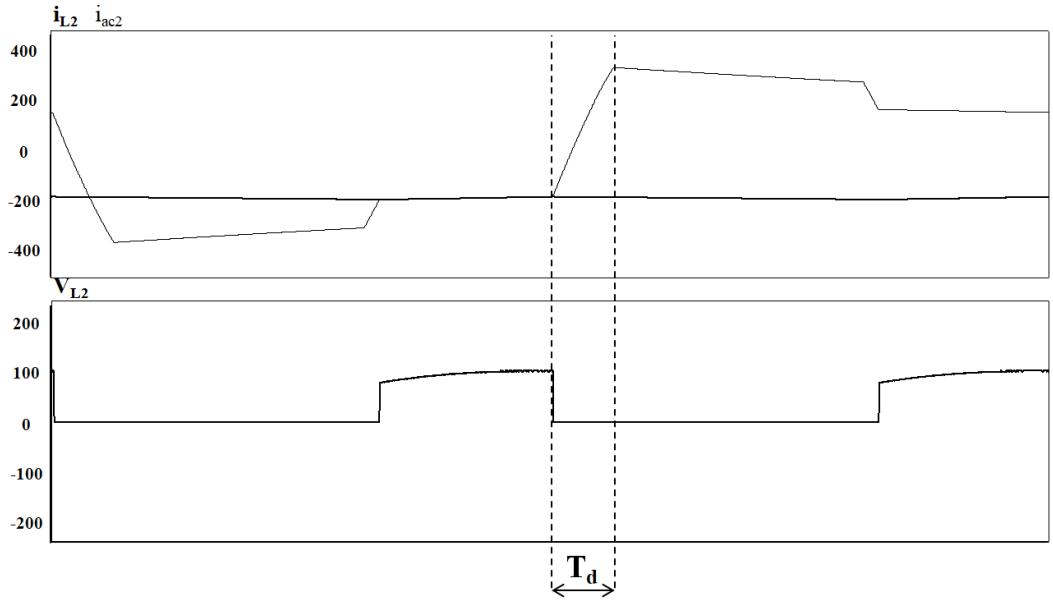

Figure 10. Zoom on the secondary-side waveforms for the modified PSM.

A power efficiency increase is therefore achievable by means of this improved modulation strategy in case of SOSC recharge, as highlighted in Table 3, reporting system efficiency η for conventional and improved PSM, with respect to the extreme values of V_1 and V_2, at full power.

Table 3. Efficiency at full power in case of SOSC recharge, as resulting from simulation.

Conventional PSM			**Improved PSM**		
V_1	V_2	η	V_1	V_2	η
70 V	32 V	0.72	70 V	32 V	0.84
70 V	24 V	0.62	70 V	24 V	0.80
35 V	32 V	0.73	35 V	32 V	0.84
35 V	24 V	0.67	35 V	24 V	0.85

4. Experimental Tests

A FBC has been realized aiming at a 2 kW power target and compliant with the specifications concerning the DC voltage sources and the current requirements. The mounted converter consists of the following parts—the power board, including the actual FBC, filtering networks, protection switches and transducers for telemetries; a control board, including signal conditioning, input/output interfaces, controller and gate signals generation; an auxiliary power supply, including power converters to generate all internal supply lines; a mechanical frame/heatsink for thermal dissipation. The control loop aims at the regulation of the bus current value according to its desired value and it has been entirely implemented through analog components.

In Figure 11 the prototypal breadboard is shown. Auxiliary power supply board and control board on the bottom-left corner and bottom-right position can be noted.

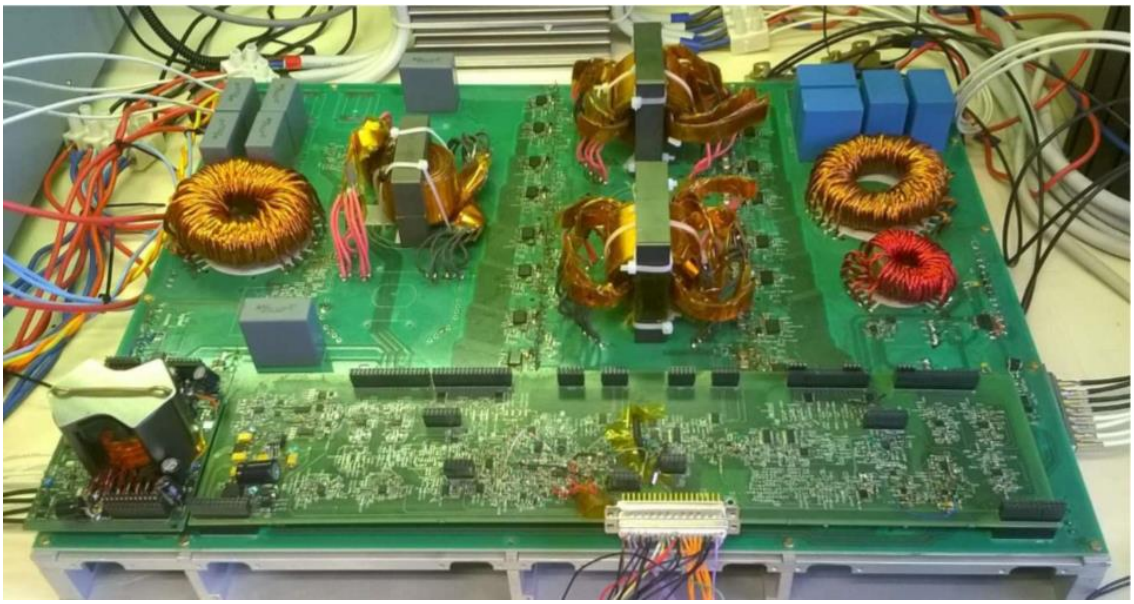

Figure 11. The prototype of the bidirectional FBC, as built and mounted.

4.1. H-bridges Realization

Each power switch in the power board consists of four parallel MOSFETs. The selected components are compliant with Automotive applications and show a TO-247 package. Though-hole type was found convenient as it natively provides connection to multiple PCB layers. In the SOSC-side, AUIRFP4568 nMOSFETs have been used, rated for a maximum 171 A drain current $I_{d,max}$ and for a maximum 150 V source-to-drain voltage V_{DSS}, with a maximum 5.9 mΩ on resistance; in the bus-side, IXFH140N20 × 3 nMSOFETs have been used, rated for a maximum 140 A drain current $I_{d,max}$ and for a maximum 200 V source-to-drain voltage $V_{DSS,}$ with a maximum 9.6 mΩ on resistance.

The bus-side switches have been selected with a higher maximum voltage due to the transformer ratio of the secondary side (bus-side) turns to the primary side (SOSC-side) turns, which is higher than one.

All MOSFETs are driven by means of isolated gate drivers, useful to maintain galvanic insulation between controller and power circuits. The selected component is UCC21521, providing dual independent channels, useful for managing the low-side and the high-side MOSFETs and guaranteeing a 4–6 A (source/sink) current capability and a 16 ns time rise on a 2 nF load capacitance.

4.2. Reactive Components Realization

As far as the used capacitors are concerned, Multi-Layer Ceramic Capacitances (MLCC) are preferred to provide the highest frequency current peaks, since MLCC present equivalent impedances with higher cut frequencies with respect to the electrolytic and Metallized Polyester (PET) ones, which instead contribute to the rms component of the pulsed currents.

The magnetic components with pulsed currents in the tens of A range (the converter inductor L_2 and the transformer) have been implemented with EE-type-cores. For the transformer, two magnetic structures have been used, as highlighted by the figure. Copper foils have been used for the windings and multiple wires for the connections with the PCB, in order to have a large current capability. The material used for the transformer cores is 3C95, a power ferrite with high saturation levels and low losses. For L_2 a powder core with distributed air gap is used, whose material is Kool Mμ® 40 from (Magnetics, Phoenix, AZ, USA).

In Tables 4 and 5 the main characteristics of the designed and realized transformer and L_2 are respectively reported.

Table 4. Characteristics of the realized transformer.

Core	Material	*n*	*m*	Measured L_m	Measured L_1
EE80/38/20	3C95	4	6	60 μH	140 nH

Table 5. Characteristics of the realized inductor.

Core	Material	Turns	Measured L_2
00K7228E040	Kool Mμ® 40	13.5	24 μH

In Table 6, the values of the selected converter switching frequency f_{sw} and reactive components are reported.

For filtering inductors, with DC currents and small ripple, toroidal powder cores are used, with multi-wire windings. The used toroidal core materials are MolyPermalloy Powder (MPP) and High Flux (Magnetics, Phoenix, AZ, USA).

Table 6. Selected values of switching frequency and reactive components for the designed converter.

Parameter	Value
f_{sw}	50 kHz
L_2	24 μH
C_1	130 μF
C_2	200 μH

The choice of L_m is based on specifications concerning the desired magnetizing current, whereas the reactive elements selection is based on specifications concerning the desired current ripple at the input and output sections. Details regarding these specifications are beyond the purpose of this paper.

4.3. Experimental Setup

A schematic of the test setup, proposed for full power (2 kW) transfer, is shown in Figure 12.

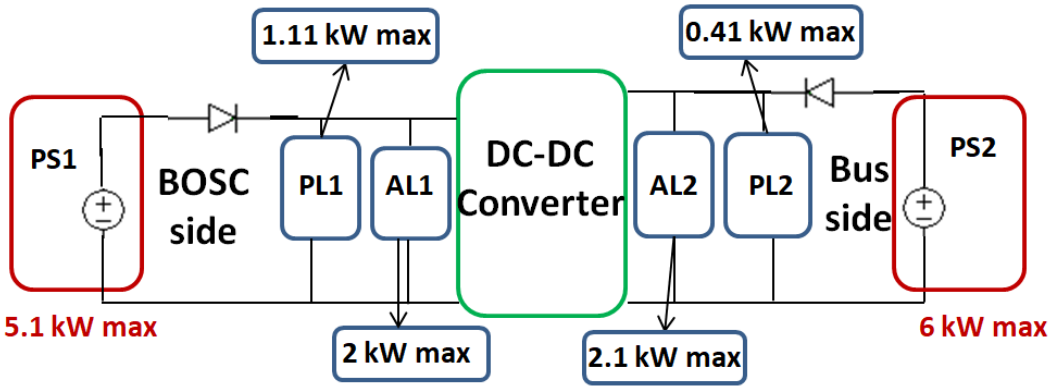

Figure 12. Schematic of the test setup.

Each side (SOSC or bus) is emulated by a 1Q (One Quadrant) Power Supply Stack—PS1 and PS2 for SOSC and bus respectively—and a Load Stack, so that a bi-directional power flow can be tested—when the power flows from the SOSC to the bus, PS1 provides the required energy to the bus-side Load Stack; when the power flows from the bus to the SOSC, the SOSC-side Load Stack adsorbs energy arising from PS2.

In order to avoid a negative current flowing through the power supplies, a protection diode is used between the supply and the load. Therefore, 2 protection diodes are used, one on the SOSC side and one on the bus side. Each of them is able to withstand a maximum 200 A current, considering that a maximum 70 A current is supposed to flow in the converter and a maximum 80 A current is needed to continuously supply the Passive Loads. Therefore, in order to guarantee that both the protection diodes are continuously polarized in direct way, a minimum direct current (supposed to be equal to 5 A) shall flow through each of them. Some Passive Loads are needed for this purpose, in order to guarantee the required power absorption.

4.3.1. SOSC-Side Setup

The goal of the SOSC test setup is to guarantee—(35 V–70 V) voltage range; (−2 kW–+2 kW) power range. The SOSC-side Power Supply (PS1) Stack can provide a total maximum power of 5.1 kW. The SOSC-side Load Stack consists of an Active Load (AL1) and a Passive Load (PL1), for a total maximum power of 3.11 kW.

4.3.2. Bus-Side Setup

The goal of the bus test setup is to guarantee—(24 V–32 V) voltage range; (−2 kW–+2 kW) power range. The bus-side Power Supply (PS2) Stack can provide a total maximum power of 6 kW. The bus-side Load Stack consists of an Active Load (AL2) and a Passive Load (PL2), for a total maximum power of 2.51 kW.

4.4. Experimental Results

In Figure 13 a picture of the arranged test setup is shown, along with the highlighted parts.

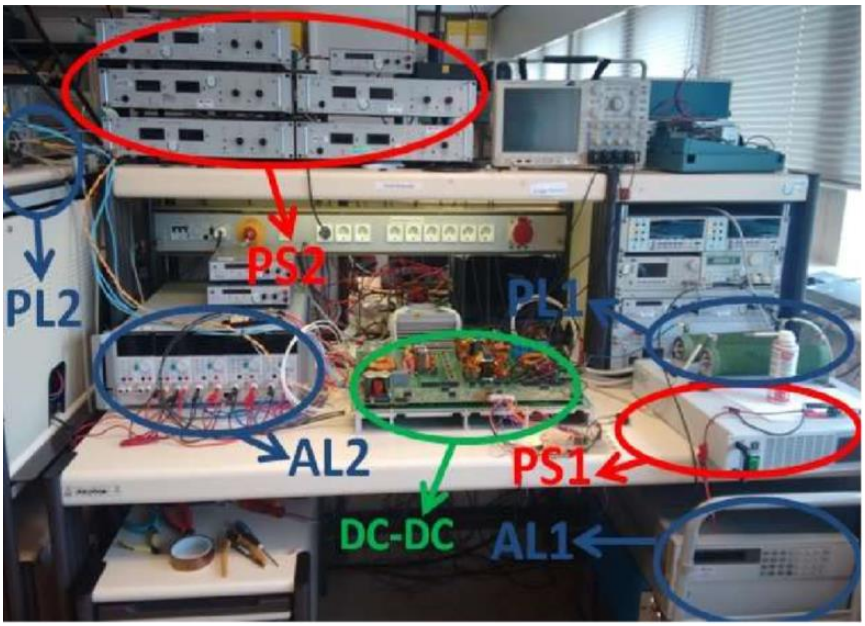

Figure 13. The arranged test setup.

The improved PSM was implemented for the built prototype. The proper behavior of the converter is shown in Figure 14, showing the proper bus current response to a square wave command. The transduction factor in the command and monitoring signals is equal to 1 V/10% of full power, where "full power" corresponds to a 70 A bus current. Therefore, the image refers to a step between two levels corresponding to about 70% of the full negative power (during the SOSC recharge) and of the full positive power (during the SOSC discharge). There are no overshoot phenomena in the transients.

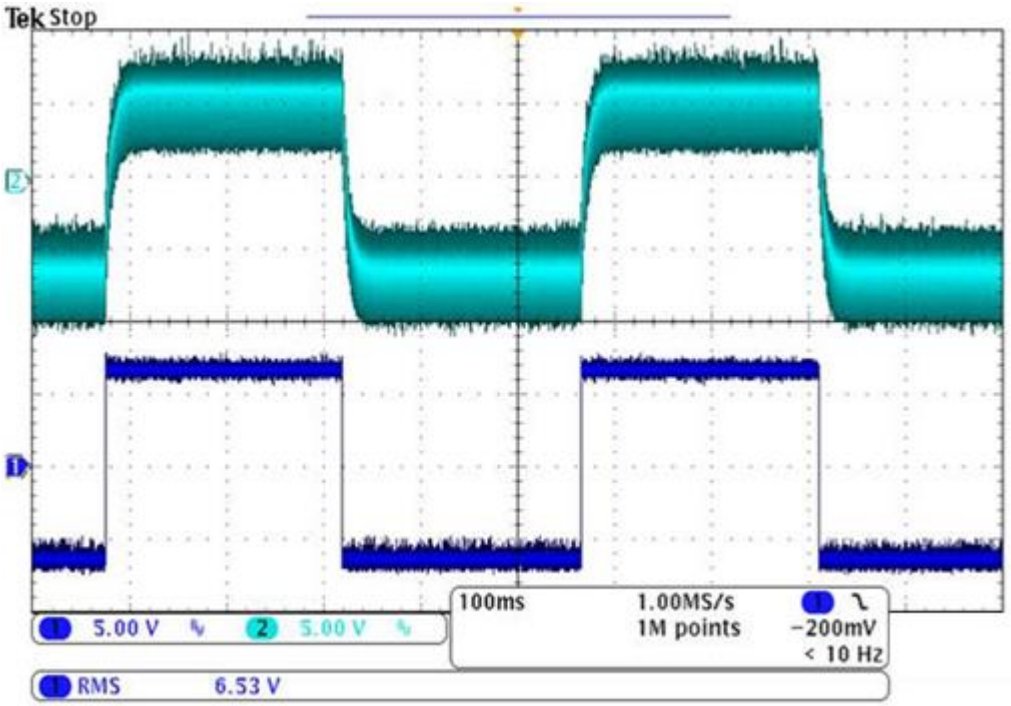

Figure 14. The proposed behavior of the bus current (in light blue), as experimentally tested, corresponding to a given power profile (in blue). For the monitoring signal (light blues) and the command signal (blue) 1 V is equivalent to the 10% of the full power.

Figures 15 and 16 show a zoom of the positive and negative transients respectively. Response time is compliant with the requirements, according to typical applications where 100 ms maximum response times are allowed. A further improvement of the response time is possible through a slight refinement of the control loop

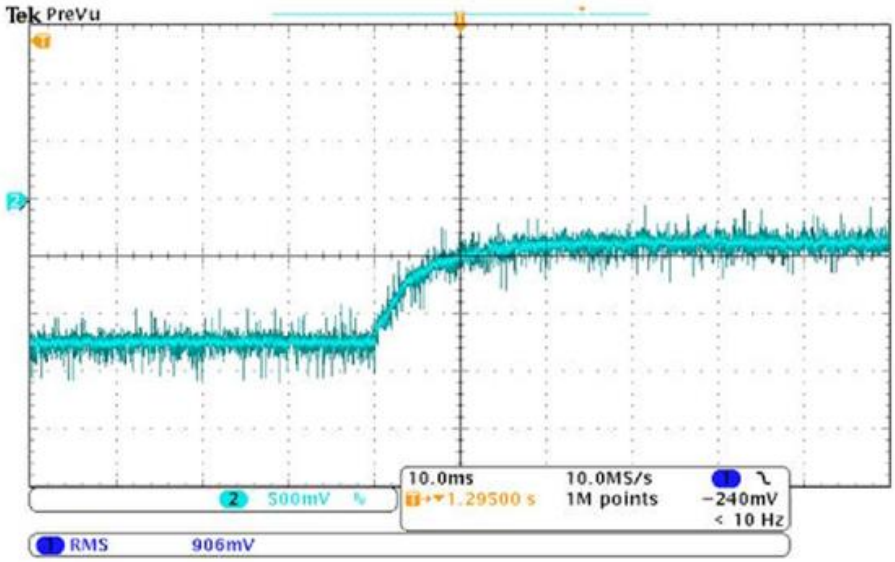

Figure 15. Zoom on a positive bus current transient, responding to an instantaneous positive command.

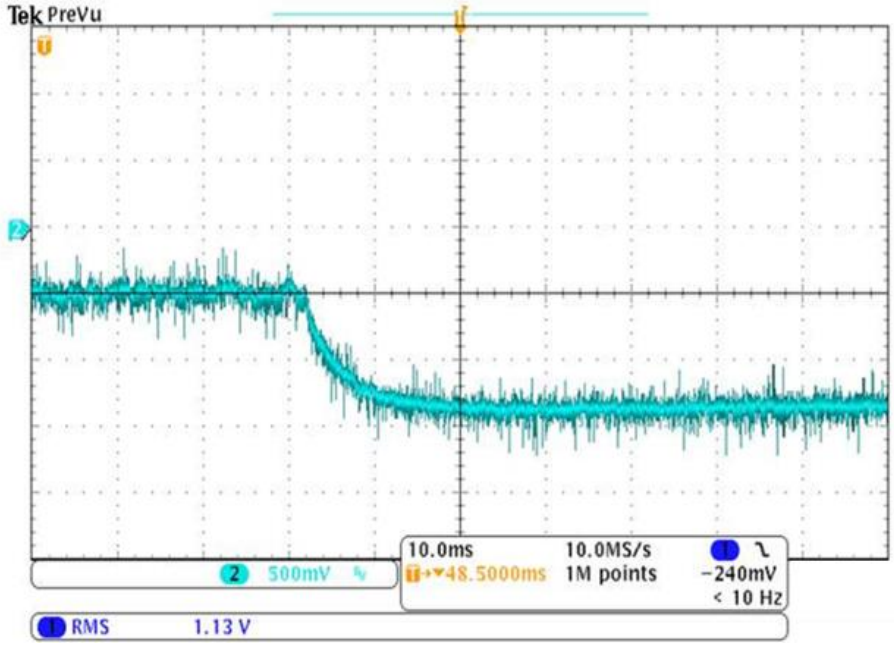

Figure 16. Zoom on a negative bus current transient, responding to an instantaneous negative command.

5. Conclusions

In this paper, an insulated bidirectional DC-DC converter for the management of a storage system is proposed. Electrical Storage Systems find different possible application fields—automotive, zero-energy buildings, aerospace and so forth. The described topology is a Full-Bridge Converter (FBC), connected to a double voltage source—a voltage bus on one side and a Stack of Super-Capacitors (SOSC) on the other side. Analysis, design and modulation strategies of the proposed FBC are discussed.

An improved modulation strategy has been proposed by authors, aiming at avoiding expensive clamping networks and at the power losses reduction. A 2 kW converter prototype, including also control and auxiliary power supply boards and compliant with automotive applications, has been realized and the related experimental results have been presented as well, proving the proper behavior of the converter.

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