Linear, Time-Invariant Model of the Dynamics of a CMOS CC-CP

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***Abstract*—This paper presents the development of a linear dynamic model of a MOS Cross Coupled Charge Pump (CC-CP) suitable for low voltage energy harvesting systems in the form of a Discrete-Time State-Space set of equations considering the resistive behavior of transistor switches. The dynamic model, easily extendable to a CC-CP of an arbitrary number of stages, includes parasitic elements without loss of generality. The validity of the dynamic model is evaluated through the comparison of Matlab simulations of the model to circuit simulations of an ideal CC-CP.**

***Index Terms*—Charge Pumps, FDSOI, Body Bias, DC-DC converter, Energy harvesting.**

I. Introduction

With the advent of the Internet of Things and ultra-low power circuits there is an ever increasing need for efficient on-chip low power voltage regulators. In particular, despite the reduction of power supply voltage needed as transistor sizes shrink, schemes that rely on energy harvesting as power sources might present input voltages too low for an adequate performance of digital circuits [1]. One possible solution is to exploit FDSOI technology with forward body biasing of transistors to increase performance at low voltage supply levels, and for that it is necessary to generate back biasing voltages that extend beyond the supply voltage level. Among other options, switched-capacitors voltage regulators are very attractive due to the absence of inductors.

Nonetheless, circuit design of switched-capacitors voltage regulators has proved trying, given their complex, non-linear nature. The dynamics of the Dickson Charge Pump have particularly fostered extensive analysis, and various methods to determine their transient operation have been provided [2] [3] [4] [5]. However, the models were not directly applicable to the CC-CP considered for the body bias generator of an ultra-low voltage FDSOI circuit.

This paper presents the development of an analytical model describing the dynamics of CMOS CC-CP circuits in a discrete-time model, with transistors acting as resistive switches instead of diodes. This approach allows an easy and intuitive modeling that is helpful to find the circuit parameters to design the regulator with the desired performance characteristics, namely transient response and steady-state voltage. The presented model is valid both for the Slow and Fast Switching Limits. To the best of our knowledge, no such approach has yet been derived for this type of converters.

The paper is organized as follows. Section II introduces the basic phenomena that govern the circuit behavior. Section III employs equations from the previous section to derive the dynamic model in the form of a Discrete-Time State-Space set of matrices. Section IV expands the ideal model to consider parasitic effects. Section V goes on to establish the validity of the previous analysis showing a design example with resistors and FDSOI transistors. Conclusions are finally presented in Section VI.

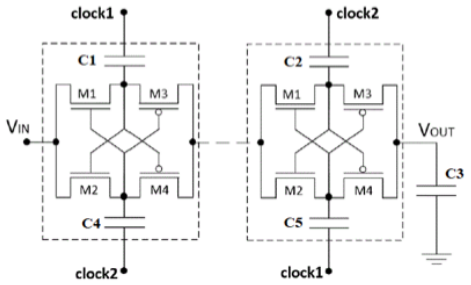

Fig. 1. Schematic representation of an N-Stage CMOS CC-CP with capacitive load, characteristic of FDSOI technology substrate bias.

II. Basis for the Model

Linearization of switched capacitor converters presents some difficulties. The discontinuities introduced by switching topologies coupled with the absence of inductors that would guarantee a mean current flow render traditional methods of linearization of power converters analysis (volt-second balance and small-ripple approximation) unsuited.

In a CMOS charge pump with transistors acting as resistive switches, the charge transfer relation between capacitors can be considered linear. It is then possible to define a set of linear equations stating the change in capacitor voltage as a consequence of linear charge transfer.

A. Circuit operation of the CC-CP

The CC-CP circuit, depicted in Fig. 1, operates with two non-overlapping clock phases. A duty cycle of 50% is assumed for simplicity, albeit the model allows an arbitrary duty cycle. Although the load is considered capacitive, a more general load can easily be considered.

In order to illustrate the operation, the first stage in Fig. 1 is considered. When Clock 2 is active high, the opposite terminal of capacitor C_4 experiences a voltage boost across its terminals equal to the clock source amplitude, V_{clk}. This increase in voltage decreases the resistance of the NMOS

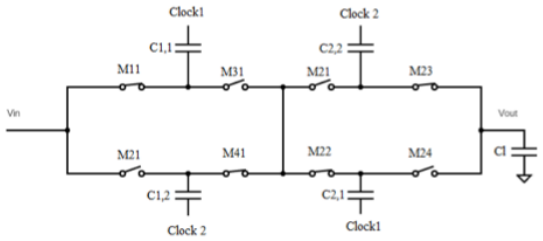

Fig. 2. Schematic representation with transistors as switches of a 2-stage CC-CP when Clock 2 is active high.

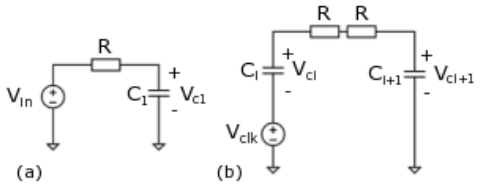

Fig. 3. a) First stage charging topology. b) ith stage topology. Each resistance represents a MOS transistor. Note that the last topology is equivalent to that of b) with only one resistance.

transistor M1 lying opposite to C_4, while increasing that of the PMOS transistor M3 due to the charging of their respective gates. At the same time, Clock 1 becomes active low so that the opposite terminal of capacitor C_1 experiments a voltage decrease that produces the opposite effect to transistors M2 (increased resistance) and M4 (decreased resistance).

This combined effect produces a series of high and low resistance paths that connect the capacitors to different nodes in the circuit, as depicted schematically in the form of open and closed switches in Fig. 2. Assuming that the impedances of the open switches are much higher than the impedances of the closed switches, the circuit operates as a sequence of charge transfer between capacitors that can be modeled as simple RC circuits (Fig. 3).

It is possible to quantify at each step the charge transfer and voltage change across each capacitor of a converter with n stages. In each period, there is a charge transfer $\Delta Q_{(i+1)}$ from capacitors $C_{i,1}$ to $C_{(i+1),2}$ in the first semi period (rising Clock 1, falling Clock 2), and from $C_{i,2}$ to $C_{(i+1),1}$ in the second semi period (falling Clock 1, rising Clock 2), with a charge $\Delta Q'_{(i+1)}$. The voltage across each capacitor ($V_{i,1}$ and $V_{i,2}$ where $i \in \{1..n\}$ is the stage number) after each period K can then be expressed as:

$$V_{i,1}[K+1] = V_{(i,1)}[K] - \frac{\Delta Q_{(i+1)}}{C_{i,1}} + \frac{\Delta Q'_{(i)}}{C_{i,1}} \quad (1)$$

$$V_{i,2}[K+1] = V_{(i,2)}[K] + \frac{\Delta Q_{(i)}}{C_{i,2}} - \frac{\Delta Q'_{(i+1)}}{C_{i,2}} \quad (2)$$

$$V_{out}[K+1] = V_{out}[K] + \frac{\Delta Q_L}{C_L} + \frac{\Delta Q'_L}{C_L} \quad (3)$$

The next section presents the expression for charge transfer in the first and second semi periods.

B. Charge transfer calculation ΔQ, $\Delta Q'$

Fig. 3 depicts the connection between capacitors at different semi periods, for the first and subsequent stages. Both topologies represent linear time-invariant (LTI) systems that can be easily analyzed through Kirchhoff voltage law (KVL) to obtain an expression of current and thus the charge transfer expression for each semi period, SP1, SP2, can be obtained:

a) SP1 from K to K+1/2: Rising Clock 1, Falling Clock 2. Initial conditions for the capacitor voltages are $V_{i,1}[K]$, $V_{i,2}[K]$. The charge transfer over one semi period $T/2$ is, for the first stage, $i = 1$:

$$\Delta Q_1 = C_{1,2}(V_{in} - V_{1,2}[K])(1 - e^{\frac{-T}{2RC_{1,2}}}) \quad (4)$$

And for subsequent stages, $i > 1$:

$$\Delta Q_i = C_{eq}(V_{clk} + V_{(i-1),1}[K] - V_{i,2}[K])(1 - e^{\frac{-T}{4RC_{eq}}}) \quad (5)$$

While for the load charge transfer:

$$\Delta Q_L = C_{eqL}(V_{clk} + V_{n,1}[K] - V_{out}[K])(1 - e^{\frac{-T}{2RC_{eqL}}}) \quad (6)$$

b) SP2 from K+1/2 to K+1: Falling Clock 1, Rising Clock 2. Initial conditions for the capacitor voltages are $V_{i,1}[K+1/2]$, $V_{i,2}[K+1/2]$. The charge transfer over one semi period $T/2$ yields similar expressions as (4)–(6), only changing subindexes $x,1$ by $x,2$ and K by $K' = K + \frac{1}{2}$.

In the previous expressions, V_{clk} represents the clock amplitude, R the equivalent transistor resistance in the ON state, and C_{eq} and C_{eqL} the series association of the two capacitors in each topology (see Fig. 3 b).)

Under the assumption that all stages capacitors are equal in value (C), and that $C_L \gg C$, and assuming that clock amplitude V_{clk} is the power supply voltage, V_{in}, equations for charge transfer are:

$$\Delta Q_1 = C(V_{in} - V_{1,2}[K])a \quad (7)$$

$$\Delta Q_i = \frac{C}{2}(V_{in} + V_{(i-1),1}[K] - V_{i,2}[K])a \quad (8)$$

$$\Delta Q_L = C(V_{in} + V_{n,1}[K] - V_{out}[K])a \quad (9)$$

$$\Delta Q'_1 = C(V_{in} - V_{1,1}[K'])a \quad (10)$$

$$\Delta Q'_i = \frac{C}{2}(V_{in} + V_{(i-1),2}[K'] - V_{i,1}[K'])a \quad (11)$$

$$\Delta Q'_L = C(V_{in} + V_{n,2}[K'] - V_{out}[K'])a \quad (12)$$

with factor $a = (1 - e^{-T/2RC})$.

III. Discrete-time State-space model

Following the equations in section II, all instances of charge transfer in a period of operation must be identified. After some algebra, it is possible to obtain expressions for each capacitor voltage in time step $K+1$ from the previous step, K. This renders $2n+1$ equations, being n the number of stages in the converter. Note that the output capacitor is included in the derivation.

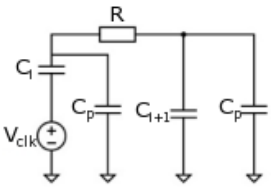

Fig. 4. Schematic representation on the i-th stage showcasing the connection of parasitic capacitances.

It then becomes possible to rearrange all terms in matrix and vector form. With all input and clock voltages being of equal amplitude, the following expression is obtained:

$$\overline{\mathbf{V}}[K+1] = \overline{\overline{\mathbf{A}}} \times \overline{\mathbf{V}}[K] + \overline{\mathbf{B}} \cdot V_{in} \tag{13}$$

Where $\overline{\mathbf{V}}[K+1]$ and $\overline{\mathbf{V}}[K+1]$ are $(2n+1) \times 1$ vectors representing, respectively, the voltage across capacitors at period $K+1$ and at period K. Symbol $\overline{\overline{\mathbf{A}}}$ is a time-invariant $(2n+1) \times (2n+1)$ matrix, and $\overline{\mathbf{B}}$ is a $(2n+1) \times 1$ vector also of constant parameters.

Once the expressions for the matrices are obtained, the model can be built in Matlab or other similar tool for a very fast calculation of the response without costly electrical simulations.

IV. Effects of parasitic capacitances

Parasitic elements in the cross-coupled capacitors can be easily introduced in the model. Two types of parasitic capacitances can be considered: top-plate and bottom plate (Fig. 4).

Bottom plate parasitic capacitances have no impact in the circuit response. They can certainly affect the behavior and efficiency of the clock drivers by increasing power consumption and introducing additional loading effects, but they do not intervene on the charge transfer between stages. On the other hand, top plate parasitic capacitances do alter the behavior of the ideal CP in two ways:

- They modify the effective value of the circuit capacitances, modifying the RC time constants of each topology.
- They capture some amount of charge during the discharging of active capacitances, diminishing the effective gain of each stage.

A. RC time constant

Analyzing the circuit in Fig. 4, the presence of parasitic capacitances cause an increase of the equivalent capacitance that modifies the time constant of the topology. If the intended circuit is to operate under strict Slow Switching Limit (SSL) conditions, this effect can be neglected in the model.

B. Charge redistribution

During its charging, the capacitor C_{i+1} and its top plate parasitic counterpart C_p are connected in parallel to each other (Fig. 4) and thus, both capacitors present the same voltage across them at all times. However, when capacitor C_i enters its discharging semi-period, the clock generator boosts its top plate terminal, which is connected to the top-plate parasitic capacitance. This voltage increase, assumed much faster than the transfer to capacitor C_{i+1} through resistor R, causes a charge redistribution with its parasitic capacitor, giving rise to a voltage $(V_i[K] + V_{in}C_i/(C_i + C_p))$, lower than the ideal case without parasitic capacitance, i.e. $V_i[K] + V_{in}$.

This effect reduces the charge transferred to the next capacitor and thus the efficiency of the stage. With this considerations, the model can take into account the effect of parasitic capacitances so that the transferred charge can be updated as:

$$\Delta Q_i = C_{eq}\left(V_{in}\frac{C_i}{C_i + C_p} + V_i - V_{i+1}\right)a \tag{14}$$

Where C_{eq} is now including the parasitic capacitances as explained above.

V. Comparison between model and electrical simulations

The full Discrete-Time State-Space System for a 3-stage CC-CP is implemented for a case of load cap equal to the stage capacitances. This case was selected to avoid long electrical simulation times, such that the accuracy of the model is emphasized more than its advantage in simulation, which is clear. The system of resulting matrices is introduced in parametrized form in Matlab, converted to a Discrete Space-State object and simulated, obtaining a time representation of the output voltage.

TABLE I
Model parameters.

	C	Cp	Ri	f	Vin
Case 1	6 fF	0 F	25 kΩ	500 MHz	1 V
Case 2	6fF	0,6 fF	25 kΩ	500 MHz	1 V
Case 3	6fF	0,98 fF	25 kΩ	500 MHz	0.3 V

The model is simulated in three cases, with parameters shown in Table I. The transient response of the output stage in the first two cases, only differing in the presence of parasitic capacitance, is compared to a transient simulation of the circuit using the Texas Instruments SPICE-based software (TINA-TI). The third case is compared with an implementation of the CC-CP in an FDSOI IC technology simulated with Cadence Spectre, obtaining the transient response. Note that the input voltage in this case is very low, 300 mV, and it is boosted to approximately 1.07 V with this circuit.

TABLE II
Steady State Voltage results.

	Model	SPICE	%
Case 1	4	3.99	0.25
Case 2	3.73	3.727	0.08
Case 3	1.075	1.074	0.09

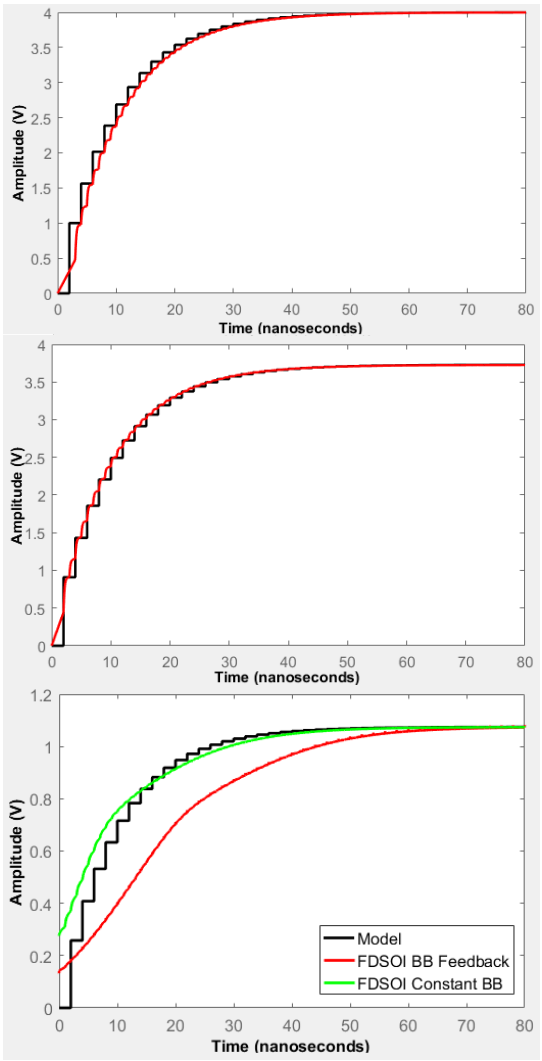

Fig. 5. Transient response simulation results. The black line represents the simulation of the State-Space model. Top) Case 1. Middle) Case 2. Bottom) Case 3, FDSOI implementation. In green, the Back Bias (BB) Is kept constant with ideal voltage sources to 1.1 V. In red, the output voltage feeds back to the Back gate.

The graphs are shown in Fig. 5, where the black line represents the Matlab transient response of the simulated model, while the red line depicts the circuit simulation on the SPICE-based software. In all three cases, it can be seen how the value of the steady state voltage (shown in Table II) predicted by the Matlab model coincides with the value of the SPICE transient response. Furthermore, the transient response until reaching the steady state is also very accurately captured by the model at a very low computational cost. The case of FDSOI simulations depicts two cases: one in which the transistors have a fixed back bias at 1.1 V, and another more realistic case in which the generated voltage is fed back to the substrate. In this latter case, it is seen a larger transient time, but the same steady state voltage.

Note that for a large output capacitance, the transient can be significantly large, as well as the simulation time. This model allows to easily try several circuit parameters (capacitances, transistor sizes) without expensive simulations.

VI. Conclusions

A linear, time-invariant model for the transient behavior of a CC-CP implemented with resistive switches is here presented. The dynamics of the system can be fully summarized in the form of a Discrete-Time State-Space matrix set. The model also includes the effect of parasitic capacitances. The results of the model simulation and the transient response of an ideal representation of the circuit agree significantly for the simulated conditions with a very low computational cost.

A direct expression for the transient response is not presented, given the algebraic complexity required to reach such and expression. However, once the model is built, an analysis of the matrices can help identify the parameters governing the characteristic equation of the system. At the same time, the computational cost of the model is low, and multiple design iterations are then feasible.

The approximation of a constant resistance modeling transistors presents a limitation in accuracy especially regarding the transient behavior before reaching the steady state, although the prediction of the steady state voltage is very good, within 0.5 %. The model can serve as a basis for a Time Variant representation of the system. Also, the model is not limited to the Slow Switch Limit and, as long as an equivalent resistance for the transistors is found, it can operate within a wide range of values without loss of linearity.

Because of this, the model can help orient the required design values to achieve desired start-times. At the same time, the dynamic model can aid in the design of schemes that facilitate the control of the circuit using state-space control techniques

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