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# Performance investigation of an innovative H-bridge derived multilevel inverter topology for marine applications

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An innovative single-phase and three-phase H-bridge derived multilevel inverter topology is being proposed in this manuscript. The proposed topology makes use of relatively fewer switching devices compared to conventional Cascaded H-Bridge (CHB) multilevel inverter. In other words, the proposed inverter topology is capable of producing more number of levels in the voltage waveform with same number of switching devices. It is also established in this paper, that this proposed topology is superior in terms of requirement of lesser number of gate driving circuits and reduction in the harmonic content in the output voltage waveform. The proposed inverter topologies are driven by SPWM modulation technique. These converter topologies are not only beneficial for the power conditioning systems in the power system network but also for the other novel applications like in marine ships. In this manuscript, the performance comparisons of the proposed inverter topologies with that of conventional topology based on simulation results with MATLAB/SIMULINK have been presented.

[**Keywords**: Cascaded H-bridge (CHB), Fixed Frequency Modulation (FFM), Variable Frequency Modulation (VFM), Inverter topology]

## Introduction

The multilevel converters came into existence with the objective to overcome the voltage limit of semiconductor devices[1-6]. These are presently being used in variety of applications like extruders, pumps, fans, reactive power compensation, traction, HVDC transmission, etc.

Of the various multilevel inverters like cascaded H-bridge (CHB)[7-11], neutral point clamped[10-12], flying capacitor[10-12] and others[13-15] as reported in literature, the CHB inverters have been focused more. This is due to the fact that these are modular and simple[9]. The number of output voltage levels in CHB inverters can easily be increased by increasing the number of H-bridges. However, this leads to a complicated multilevel inverter structure. The various modulation techniques have also been proposed for CHB inverters[4,16,17] in the literature.

In this paper, a multilevel inverter extending a CHB cell using switching of isolated DC voltage sources is proposed. In this proposed inverter topology, the connections of several numbers of voltage sources are switched in series by the switching devices. The proposed topology requires lesser number of switching devices and produces output voltage with lower harmonic content which makes it superior. In the proposed inverter topology, number of extended H-Bridge cells can be cascaded in order to have increased number of levels in output voltage waveform. These multilevel inverter topologies are not only beneficial for the power conditioning systems in the power system networks but are also field of interest particularly, in the marine ships[18] where the distribution bus voltage is either 3-phase 400V 50/60Hz alternating current (AC) or 400V direct current (DC). So, suitable power conversion system to meet the AC loads working at 240V or 400V, and DC loads working at 240V or 24V, is highly essential. Even the generation in the marine ships is possible both through conventional diesel generator sets, or through sustainable solar PV arrays[18]. To inter-connect or synchronize these two power sources to meet the total load demand of the marine ship, the role of the proposed power converter topology, is of utmost importance.

## Materials and Methods

### Circuit topologies

Figure 1 depicts the circuit topology of the proposed inverter. DC voltage sources $V_1$-$V_6$ operate

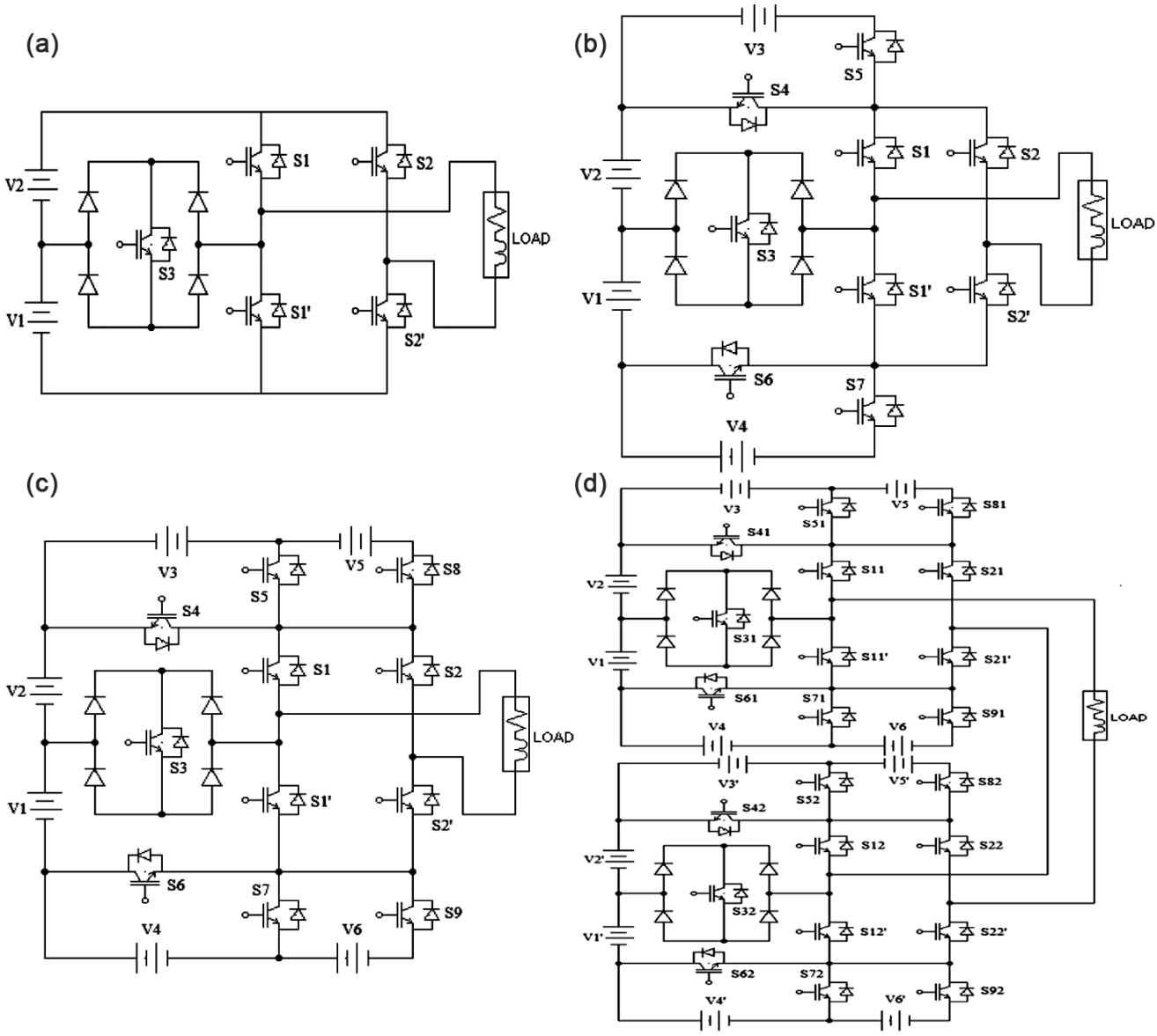


Fig. 1 — Circuit topologies of the proposed inverters (a) 5-level MLI, (b) 9-level MLI, (c) 13-level MLI, (d) 25-level MLI

independent of each other. The switches $S_1$, $S_1$', $S_2$, $S_2$', $S_3$.....$S_6$ have been provided to switch the DC voltage sources in series so as to get the desired voltage level across the load. A fundamental CHB cell can provide 3-levels of output when single DC voltage source is operated using the bridge switches. It is further extended to 5-level by connecting two DC voltage sources $V_1$ & $V_2$ in series but midpoint of the bridge and series connection of sources are connected to each other by a switch $S_3$ so that we can make or break the contact as per our requirement. Switch $S_3$ is used with four diodes so that it can work for both positive and negative cycles.

Further, to get 7, 9, 11 and 13-levels of output by switching the voltage source $V_3$, $V_4$, $V_5$ & $V_6$ through making and braking of switches $S_4$, $S_5$; $S_6$, $S_7$; $S_8$ & $S_9$ is shown in Figure 2.

There are six DC voltage sources present in the proposed topology to get 13-level output voltage. This is in accordance with the conventional CHB topology but we are using less number of switches for the purpose. In classical CHB topology, we use 2n-2 switches to get n-level output voltage. It means we have to use 24 switches to get 13-level output in classical topology but here there is a requirement of only 11 switches.

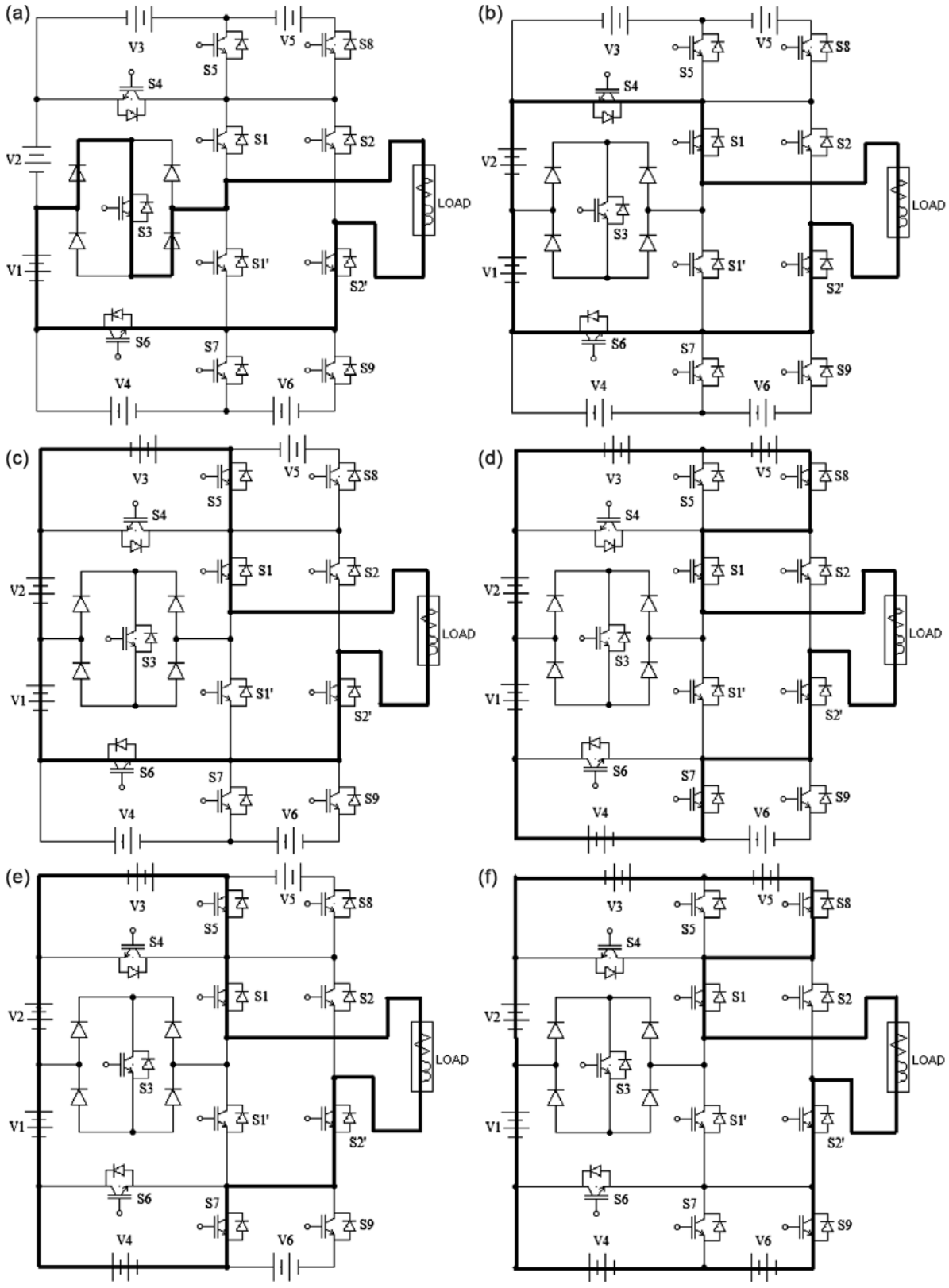


Fig. 2 — Working modes of proposed 13-level cell when Output Level is: (a) $V_0 = V1$, (b) $V_0 = (V_1+V_2)$, (c) $V_0 = (V_1+V_2+V_3)$, (d) $V_0 = (V_1+V_2+V_3+V_4)$, (e) $V_0 = (V_1+V_2+V_3+V_4+V_5)$, (f) $V_0 = (V_1+V_2+V_3+V_4+V_{5+}V_6)$

In the conventional CHB inverter, 12 switching devices are needed for 11 levels[19]. In some other topologies reported in literature[19], has used 11 devices for 11 levels and 14 devices for 15 levels. On the other hand, the proposed inverter topology requires 11 devices for 13 levels.

Further the concept of CHBMLI has been applied by taking the 13-level topology as the fundamental cell and cascading them same as the conventional CHBMLI. In this way, we get a generalized topology in which every addition of fundamental cell in cascading increases the output voltage level by 12.

Therefore, the generalized relation between number of output voltage levels (p), fundamental cells (n), and number of switching devices ($S_w$) are given as follows:

$$p = 12n+1 \quad \ldots (1)$$

$$S_w = p - (n+1) \quad \ldots (2)$$

The advantages of proposed 13-level topology can be realized from Table 1 which clearly depicts the requirement of far less number of components in this topology compared to that for conventional CHB inverters.

**SPWM modulation method:**

In this section, the modulation method of the proposed 13-level inverter is explained. The number of PWM methods are reported in literature[1,5,7,11,16,20], as shown in Figure 3. The conventional sinusoidal PWM scheme is taken as the basis for the modulation method used for the proposed 13-level inverter.

Table 1 — Comparison of proposed & conventional topologies

| Components | Conventional 13-level CHBMLI | Proposed Topology |
|---|---|---|
| Switching devices | 24 | 11 |
| Protection-diodes | 24 | 15 |
| Isolated $V_{DC}$ | 6 | 6 |

As per the conventional modulation scheme, there are (n-1) carrier waves and one reference wave. Triangular waves are taken as the carrier waves and sinusoidal wave is taken as the reference wave. The carrier wave is compared with the reference wave and PWM switching signals are generated. The PWM signals generated by any of the conventional modulation methods are not sufficient for the sequential switching of the switches of proposed 13-level inverter. For this purpose, we have to use a scheme using the generated PWM signals and some digital gates as shown in Figure 4 so that the

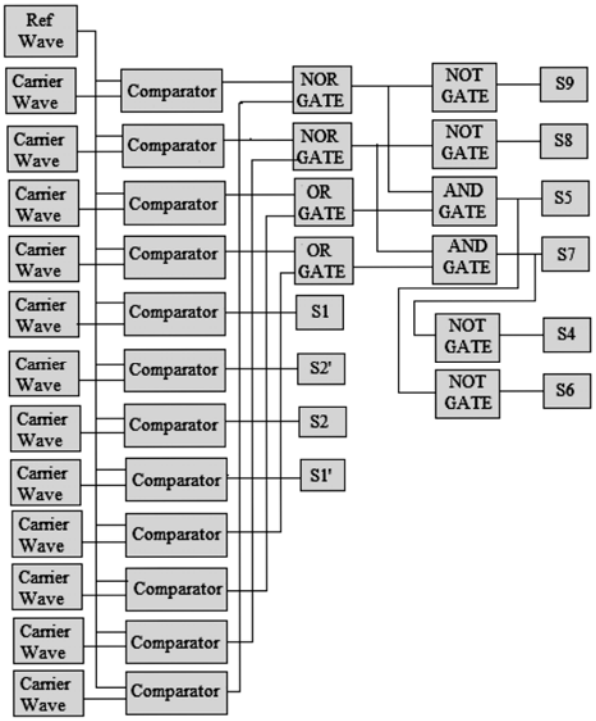


Fig. 4 — Modulation scheme for the proposed 13-level topology

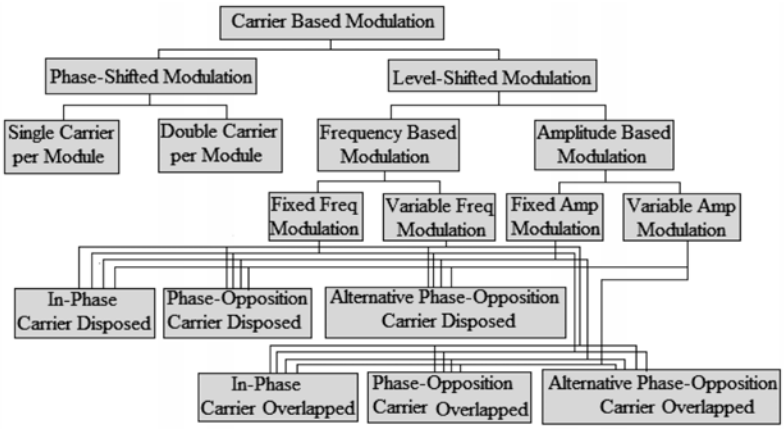


Fig. 3 — Classification-tree of carrier based PWM methods

switches of the proposed circuitry can be switched sequentially to get 13-level output. In-phase disposition SPWM method is applied. However, other SPWM methods available like PO, POD, VF SPWM, etc. can also be applied[6,8].

The Switching PWM generated by the proposed modulation scheme is shown in the Figure 5. The switching PWM for switches $S_4$ & $S_6$ are just complementary to the switching of $S_5$ & $S_7$, respectively.

**Results and Discussion**

The proposed topologies are simulated in MATLAB/Simulink. The results obtained using the proposed topologies have been compared with those of conventional topologies. Table 2 represents the simulation parameters for the proposed topology. Figure 6(a) and 6(b) displays the output voltage and harmonic spectrum at $f_c$ = 5000 Hz, $f_m$ = 50 Hz and $M_a$ = 0.9 for five level proposed topology.

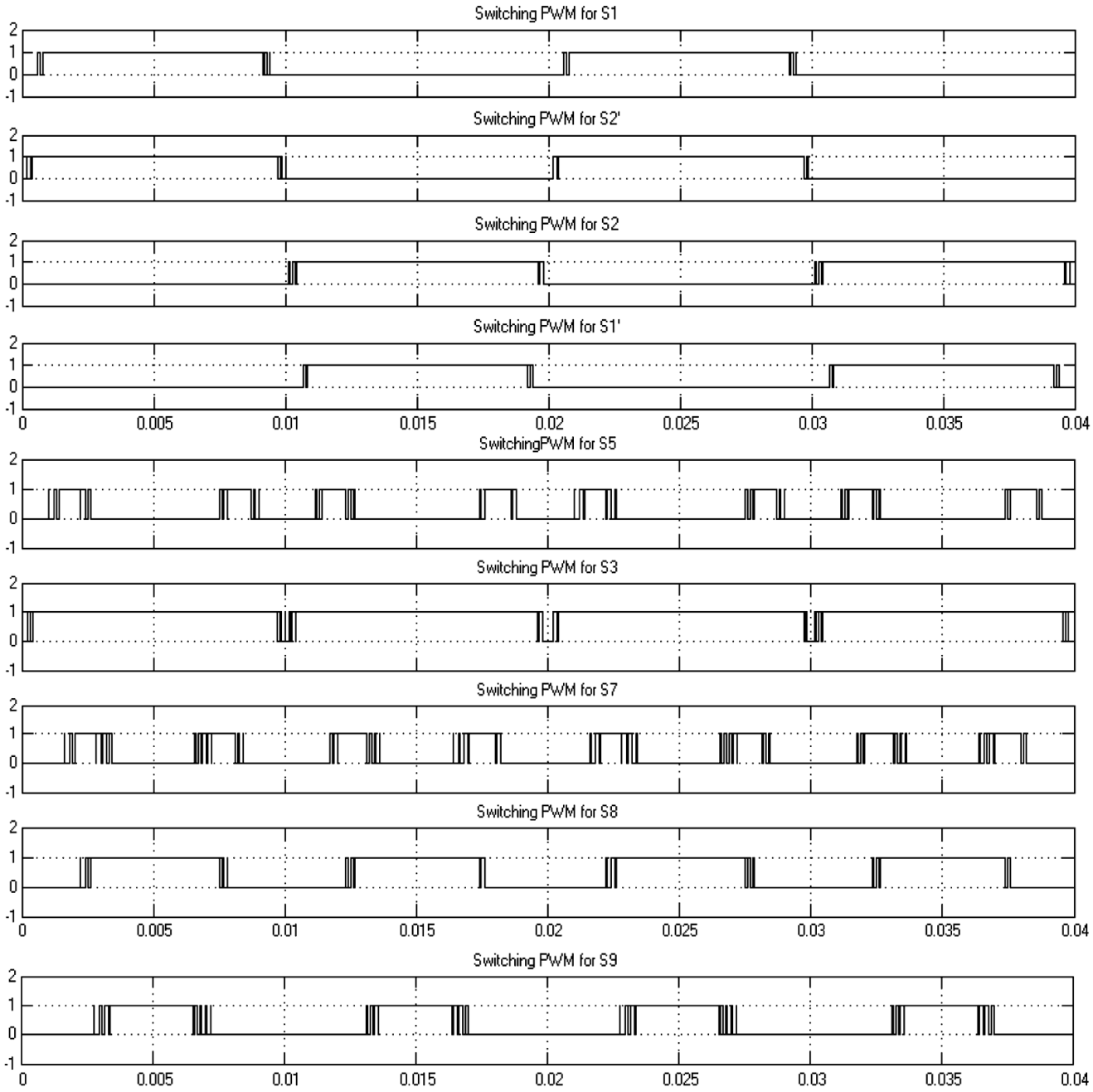


Fig. 5 — Switching PWM generated in the proposed modulation scheme (No. of cycles = 2)

In the same way, Figures 7(a), (b); 8(a), (b) and 9(a), (b) depicts the output voltage and harmonic spectrum at $f_c$ = 5000 Hz, $f_m$ = 50 Hz and $M_a$ = 0.9 for the 9-level, 13-level and 25-level topologies, respectively. For justifiable comparison, performance indices namely total harmonic distortion (THD) and switching losses were chosen to evaluate all the proposed topologies and the comparison chart is plotted for both conventional and proposed topologies using the same IPD modulation in Figure 10 and Figure 11, respectively.

Table 2 — Simulation parameters for the proposed topologies

| Parameter | Values |
|---|---|
| Isolated DC Source voltage | 100V |
| Amplitude Modulation Index ($M_a$) | 0.9 |
| Frequency Modulation Index ($M_f$) | 100 |
| Carrier Frequency ($f_{cr}$) | 5000Hz |
| Reference Frequency ($f_r$) | 50 Hz |
| Rated Output Frequency | 50 Hz |

In this work, the average switching losses are calculated based on the information of the data sheet, turn on energy loss per pulse (Eon), turn off energy loss per pulse (Eoff)[21] including reverse recovery loss and switching frequency $f_s = 1/T_s$ [9]. It can be clearly observed from the various waveforms and the corresponding harmonic profiles that the performance of the proposed topologies is as per the theoretical predictions proposed in this work. Moreover, when similar operational conditions are maintained for the conventional CHB multilevel topologies, the proposed topologies exhibit better performance in terms of THD and switching losses as shown in Figure 10 and Figure 11, respectively. Reduction of losses and THD directly affect the thermal and filter designs of the converter, and impart higher power density to it, resulting in the better electrical performance circuit being used in the marine ship. Moreover, the number of switching devices and protection diodes used in the proposed topology are also less compared to the conventional topology, as given in Table 1.

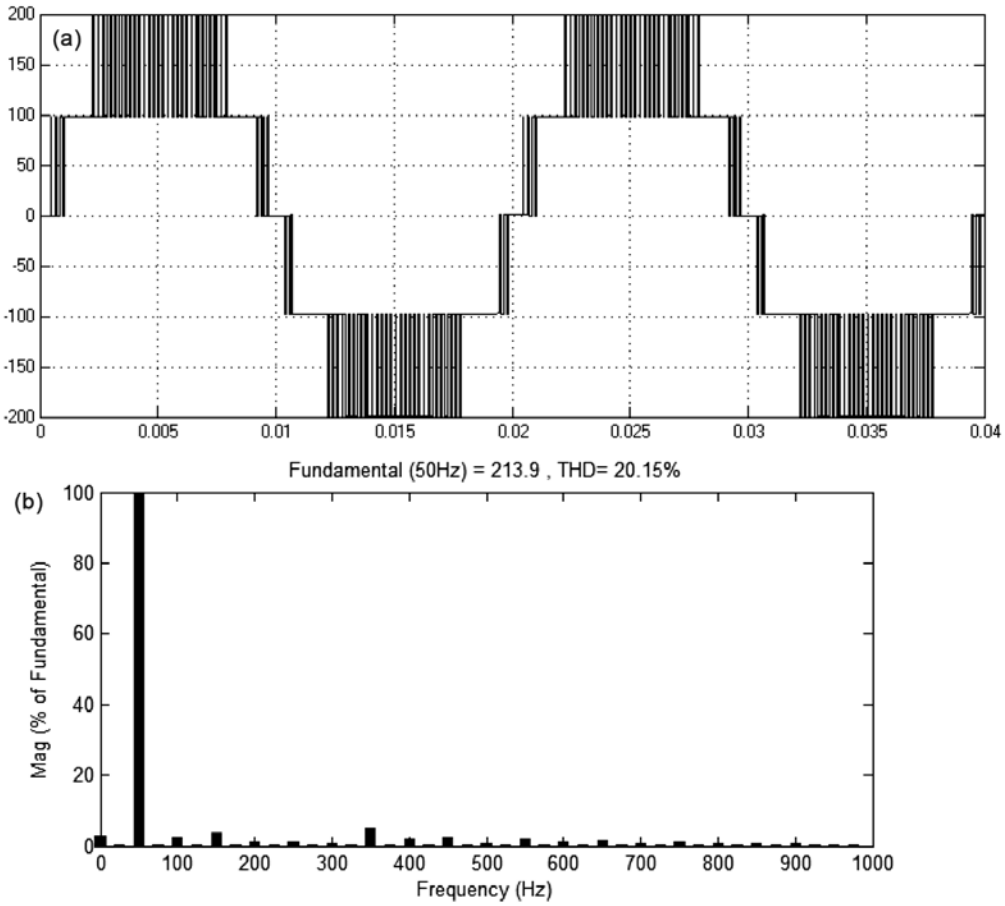


Fig. 6 — (a) Output load voltage waveform for 5-level inverter at Ma = 0.9 & fc = 5000Hz, (b) Harmonic spectrum for output load voltage waveform for 5-level inverter

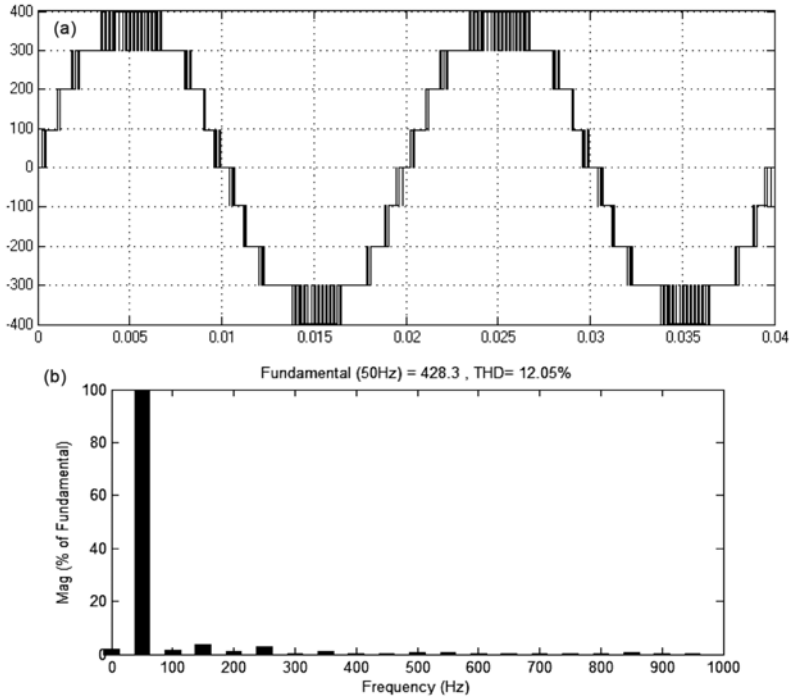


Fig. 7 — (a) Output load voltage waveform for 9-level inverter at Ma = 0.9 & fc = 5000Hz, (b) Harmonic spectrum for output load voltage waveform for 9-level inverter

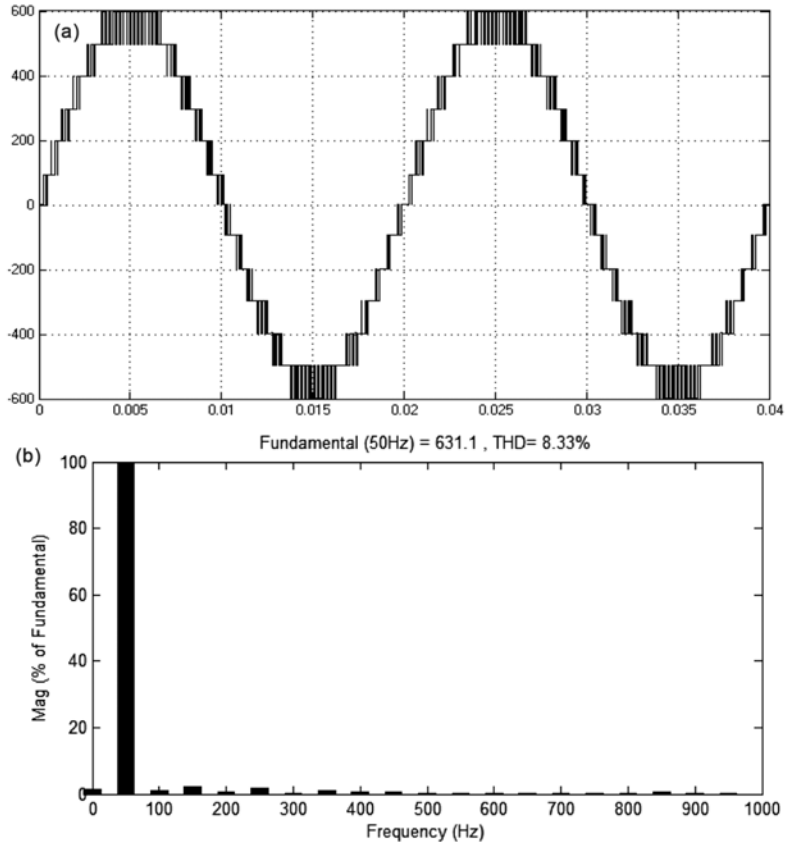


Fig. 8 — (a) Output load voltage waveform for 13-level inverter at Ma = 0.9 & fc = 5000Hz, (b) Harmonic spectrum for output load voltage waveform for 13-level inverter

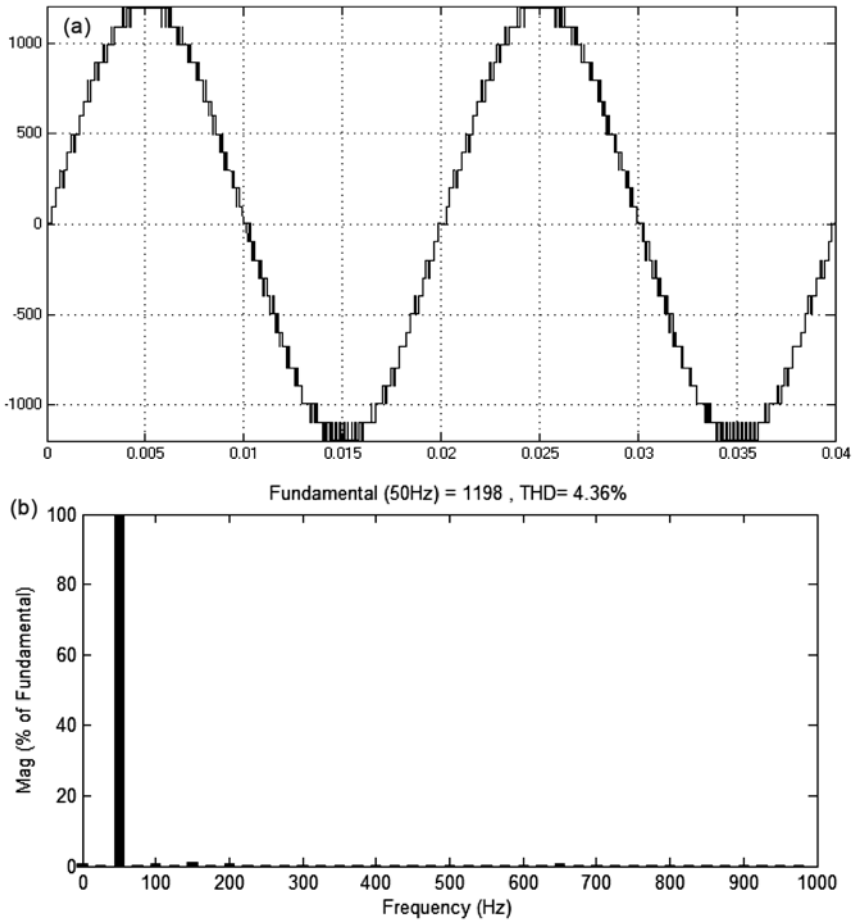


Fig. 9 — (a) Output load voltage waveform for 25-level inverter at Ma = 0.9 & fc = 5000Hz, (b) Harmonic spectrum for output load voltage waveform for 25-level inverter

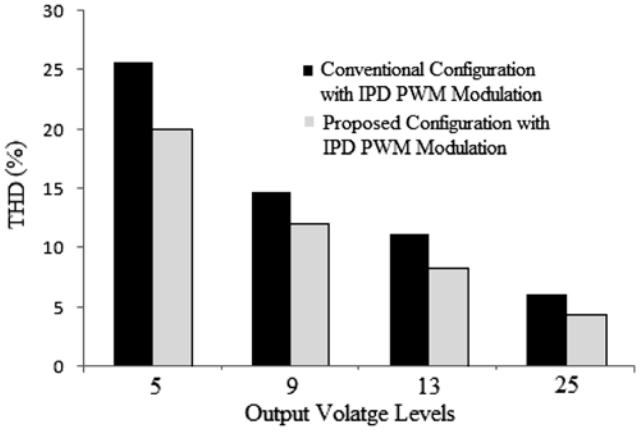


Fig. 10 — THD comparison of the conventional & proposed topologies

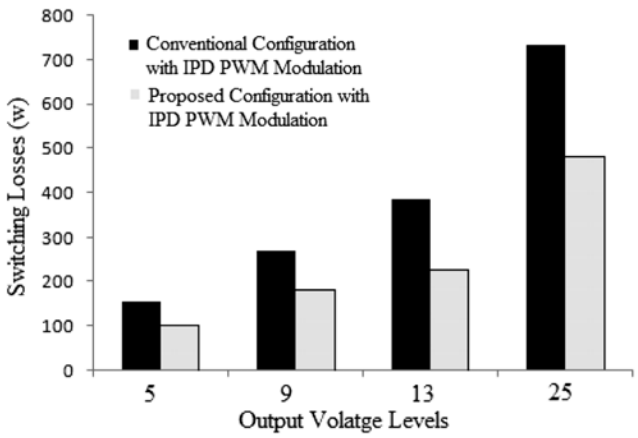


Fig. 11 — Switching losses comparison of the conventional & proposed topologies

## Conclusion

Selected topologies for different levels of output have been presented in this paper. The presented topologies are having so many advantages over conventional topologies in terms of less THD, Low switching losses, better efficiency, less number of components used and less complicated modulation scheme. The above said advantages have been proved

by using MATLAB/Simulink models. The modulation scheme applied is modification of IPD PWM modulation method. The performance of the presented topologies can further be improved by using more suitable modulation methods. The proposed topologies exhibit better performance in terms of THD and switching losses. The above-mentioned advantages clearly justify the superiority of the proposed multilevel inverter topologies over the conventional topologies. The proposed multilevel inverter topologies when used in the conventional power system networks and/or in the novel marine ship applications for power conditioning will definitely improve the overall performance of their electrical system.

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