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ABSTRACT

Wafer bonding is an established technology for the manufacturing of silicon-on-insulator (SOI) substrates, micro-electromechanical systems (MEMS) and microfluidic devices. Low temperature direct bonding techniques can be of particular interest for the fabrication of monolithic radiation sensors. Such techniques allow the joining of various absorbers on the back-side of thinned CMOS circuity without intermediate layers or through vias. This paper presents a method for the electrical characterization of such bonded interfaces based on the Transient Current Technique (TCT). This method can be extended to the investigation of any type of solid-state devices.

I. INTRODUCTION

A technology designed to enable covalent and conductive wafer bonding at low temperature was presented in 2014 by Flötgen et al.[1] It enables the bonding of different types of semiconductors for compound integration by circumventing common processing issues like differences in thermal expansion for different materials. It could also allow to bond already processed wafers (*e.g.* CMOS) between them or to any other type of wafer while preserving electrical conduction at the interface. In this paper, a study of the electrical properties of such bond interfaces is presented. It is performed with the Transient Current Technique, a method initially dedicated to characterize deep traps in bulk semiconductors. For the first time, this technique is used to characterize defects generated at interfaces.

Covalent wafer bonding can be performed at temperatures as low as room temperature. In the standard process the surfaces to be bonded are cleaned, then pressed against each other, and finally annealed at temperatures of the order of 1000°C.[2] The resulting bonding strength may reach the fracture strength of silicon[3] since the crystalline lattice can almost be restored at the interface.[4] Lattice defects density of the same order of bulk substrates can be obtained at such interfaces. The main drawback of this process is the high temperature needed, that prevents its use on silicon wafers with already implemented CMOS circuits, since the temperature should be kept below 450°C in order not to damage the metal connections.[5]

The process reported by Flötgen et al.[1] allows to overcome this problem, since it requires annealing temperatures lower than 450°C. It is similar to the one that has been

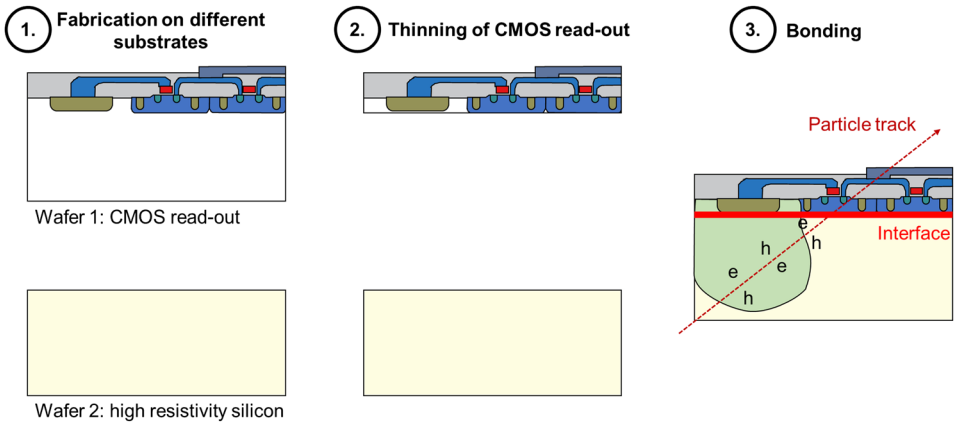

FIG. 1. Monolithic pixel detector fabricated with CMOS compatible covalent bonding.

performed in this work, and it is described as follows: wafers were first placed into a surface treatment module to remove native oxide. Then bonding was performed by applying a pressure of 0.06 MPa while annealing for 60 minutes. For annealing temperatures higher than 200°C, the bulk surface energy of silicon was reached (2.5 J/m^2) with an amorphous silicon layer at the interface whose thickness was around 3 nm.[1] Thin wafers stacking were successfully obtained with this technique[6] and the electrical conduction through this interface was demonstrated by Jung et al.[7] Based on these preliminary results, this technology holds a great potential to fabricate radiation detectors for high energy physics experiments or biomedical applications,[8,9] among other applications, since charges generated by radiations in the sensitive bulk could be collected by the CMOS circuitry by drifting across an electric field (see FIG. 1). In addition, a CMOS-processed wafer could also be bonded with a different semiconductor to optimize the detection performances.

However, even though the conductivity at the interface seems preserved, this does not guarantee that charges can be collected efficiently, since they still need to drift through the bonding interface. For this purpose, the Transient Current Technique (TCT) is used in this work to characterize the trap density and electric field at the bonding interface as modelled by Bronuzzi et. al.[10] TCT is a characterization technique largely used[11] to study the impact of radiation damage in PN junctions and Schottky diodes.[12] In TCT the current induced by non-equilibrium charge carriers, normally generated using a laser, is time resolved. The shape of the current transient is related to the shape of the electric field inside the diode through Ramo's theorem.[13] Two different TCT illumination schemes were used in this work: one in which charges are generated at the surface of the diode using lasers in the visible (normal TCT[14]), and another where charges were injected from the edge with an infrared laser beam (edge TCT or e-TCT[15]). In both cases, the current signal can be used to get information about the effective doping concentration in the silicon bulk,[14] or the presence of interface layers with traps.[10] In e-TCT, a spatially resolved profile of the electric field can be obtained along the depth of the diode.[15,16]

In this work, a method to characterize thin interfaces (in this case generated by the CMOS compatible covalent bonding process) is described in detail through the analysis of the shape of the TCT signal. In the first section, we will explain the technology used for the low temperature silicon bonding. Then, the second part will deal with the integration of the Schottky diodes. Finally, the last section will present the TCT measurements and data analysis.

II. CMOS COMPATIBLE COVALENT BONDING

In this section, bonding of unprocessed wafers, performed by CEA-Leti in Grenoble, will be described. Sixteen highly resistive (HR) P-type doped Czochralski wafers (ρ>5 kΩcm, 200 mm diameter) were used. A sketch of the process flow is summarized in FIG. 2. Wafers were first oxidized based on a wet thermal oxidation process to obtain a 1 μm thick silicon oxide layer. After this process, 14 wafers were divided into two groups depending on their role: top wafers and bottom wafers, sparing 2 of them that were kept

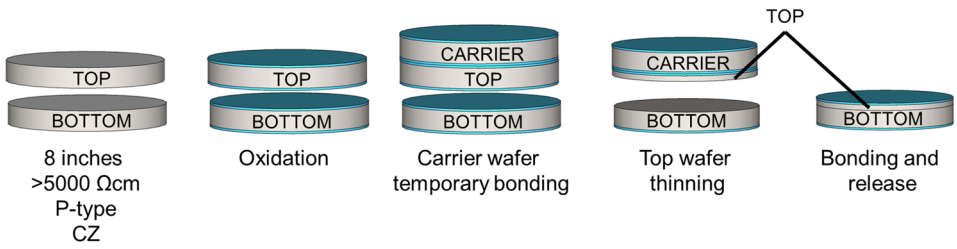

FIG. 2. Scheme of the process flow for CMOS compatible wafer bonding.

TABLE I. list of wafers and bonding parameters for the different bonding tests performed.

	Top wafer			Bottom wafer			
Stack name	Name	Thickness (μm)	Surface preparation	Name	Thickness (μm)	Surface preparation	Annealing temperature
W01	P1	50	Hydrophobic	P8	725	Hydrophobic	400°C
W02	P2	50	Hydrophobic	P9	725	Hydrophobic	400°C
W03	P3	50	Hydrophobic	P10	725	Hydrophobic	Room T
W04	P4	50	Hydrophobic	P11	725	Hydrophobic	Room T
W05	P5	50	Hydrophilic	P12	725	Hydrophilic	400°C
W06	P6	50	Hydrophilic	P13	725	Hydrophilic	400°C
W07	P7	50	Hydrophilic	P14	725	Hydrophilic	Room T
W15	P15				Reference		
W16	P16				Reference		

as reference. Different bonding parameters were chosen (see TABLE I). Top wafers were first bonded to bulk silicon carrier wafers with a direct hydrophilic bonding process before being thinned to the target thicknesses. These were determined through simulations to optimize the sensitivity of TCT to the traps concentration following the analytical model presented in previous works[10] (see TABLE I). After a classical silicon polishing and conditioning (for hydrophobic preparation: standard DiO3/RCA[17] treatment, for hydrophilic preparation: DiO3/RCA/HF 0.5%) the bondable surfaces, top and bottom (for hydrophobic or hydrophilic processing) the bondable surfaces, top and bottom wafers were bonded using the EVG® 580 ComBond® machine using Ar sputtering and a bonding pressure of 0.95 MPa. The particle neutrality of the tool has been check with a surfscan SP2 as shown on FIG. 3.a and b in order to present any bonding defect or uncontrolled interface states. Only 33 adders with a threshold of 90 nm could be detected.

Annealing of bonded substrates (called stacks) was performed at 400°C or at room temperature, as reported in TABLE I. An example of the bonding quality is checked by acoustic scanning microscopy as shown on FIG. 3.c. The last step of the process was the release of the carrier wafer by grinding followed by complete etching of silicon using the 1 μm buried oxide as a convenient etch stop layer. The different batches of bonded wafers are listed in TABLE I.

III. FABRICATION AND CHARACTERIZATION OF SCHOTTKY DIODES

For the analysis of the bonding interface by mean of the TCT method it is necessary to have a diode in order to create an electric field inside the silicon. In previous works,[10] the analysis was performed using a PiN diode. In this case, however, it was not possible to bond a top wafer with diodes already fabricated, and therefore this step had to be done after the bonding process. However, doping was not compatible with the low temperature process since annealing or diffusion, necessary for doping processes, ask for high temperature steps that would also affect the interface state (since the bonding process was already performed). To circumvent this limitation, Schottky diodes were used instead of PN junctions since the processing temperatures did not exceed 160°C (for 2 min).

A. Process flow

Fabrication of Schottky diodes on bonded (and reference) wafers was performed at the Center of Micronanotechnology (CMi) at the École Polytechnique Fédérale de Lausanne (EPFL). To ensure post-bonding low temperature process, the top wafer contact (the Schottky contact) was made of aluminum. Indeed, this metal was chosen since it is a well-known metal, easy to process, that generates Schottky barriers with

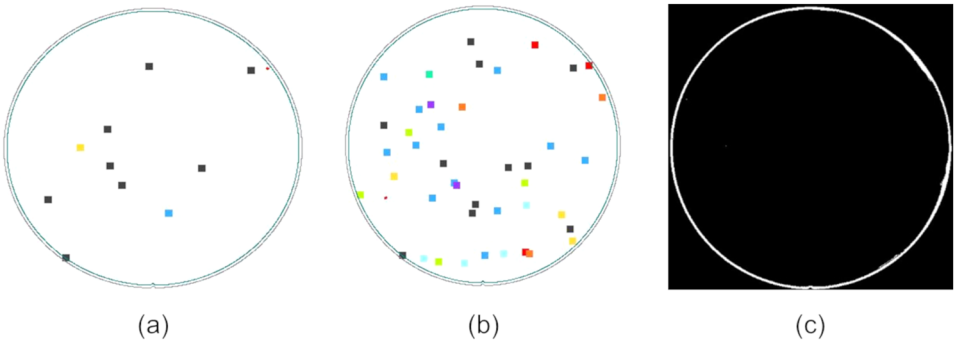

FIG. 3. SP2 particle characterization on 200mm silicon wafer (hydrophilic surface preparation) with a threshold at 90 nm: a) before entering into EVG580CB and b) after the surface activation. c) Scanning Acoustic Microscopy of SAB Si/Si bonding after 400°C annealing.

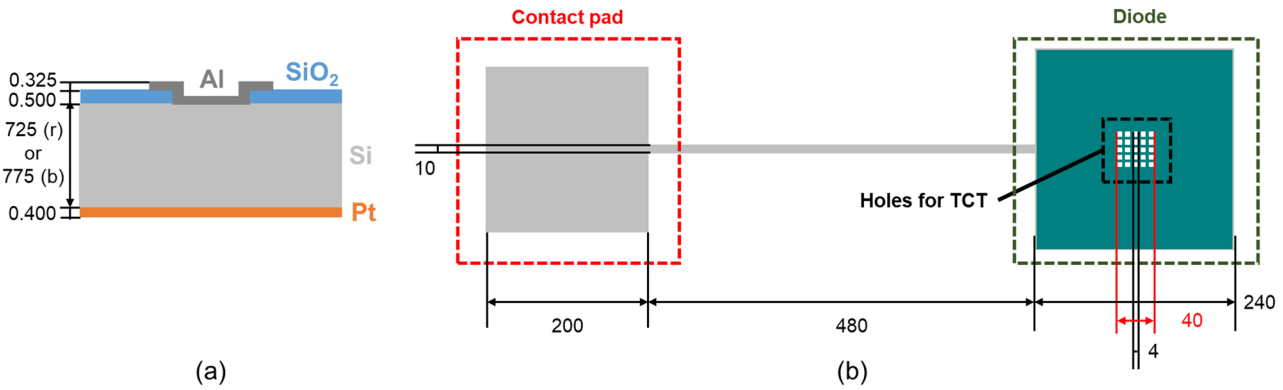

FIG. 4. (a) cross section and (b) layout of a Schottky diode. In (a) cross section, (r) refers to the reference diodes, while (b) to the bonded diodes. All dimensions are expressed in μm.

both N-Type and P-type silicon (Schottky barrier heights are, respectively, 0.69 eV and 0.58 eV).[18,19] Concerning the Ohmic contact, it is known that the potential barrier of platinum silicide with P-type silicon is low (0.25 eV).[20] Platinum was therefore chosen as the metal for the Ohmic contact (bottom side). Preliminary tests were performed to prove that, through this fabrication process, both the Ohmic and the Schottky contacts could be obtained. As expected, platinum generated ohmic contact to silicon, even without a silicidation process, while aluminum generated the desired Schottky contacts (this can also be observed in the results presented in this work, see IV and CV curves in FIG. 5). Wire bonding for signal extraction was done on 200 μm squared contact pads (see Fig. 4.b), connected to the actual diode via a 10 μm wide, 480 μm long aluminum path. The diode itself is a square of 240 μm side. Holes in the aluminum for top light injection were created in the middle of the diode (5×5 matrix, 4 μm side cells). The fabrication process is described as follows. Wafers were cleaned with RCA without cleaning with HF. Then, the silicon dioxide was thinned down to 500 nm by wet etching in BHF 7:1. Next, the first lithography step on the top side (while protecting the bottom side) defining the diodes areas was performed. Etching of silicon dioxide was done in BHF 7:1 to remove completely the oxide on the regions where Schottky contacts will be fabricated. Then, photoresist stripping and RCA cleaning were performed. After argon cleaning, Aluminum was deposited by sputtering (325 nm thick) for Schottky contacts. A second lithography was performed on the top side to pattern the diodes: contact pads for measurements and holes for light injection (wafer was heated up to 160°C for 2 min to eliminate water on Al surface to enhance photoresist adhesion). Aluminum was dry etched and the photoresist stripped. The last step was the deposition (prior argon bombardment cleaning) and sputtering of the 400 nm thick platinum. FIG. 4.a and 4.b show the cross section of the diode at the end of the process and the layout respectively.

B. CV and IV measurements

Before the TCT characterization, the diodes were tested through IV (current versus voltage) and CV (capacitance versus voltage) measurements using a Keithley 2410 voltage generator for biasing, a Keithley 6485 for current measurements, and an Agilent E4980A LCR meter for capacitance measurements. The voltage was applied to the top contact (meaning that, if the voltage is negative, then a negative voltage is applied to the Schottky contact, while if the voltage is positive a positive voltage is applied to the Schottky contact), while the bottom contact was connected to ground. The IV (FIG. 5.a) and

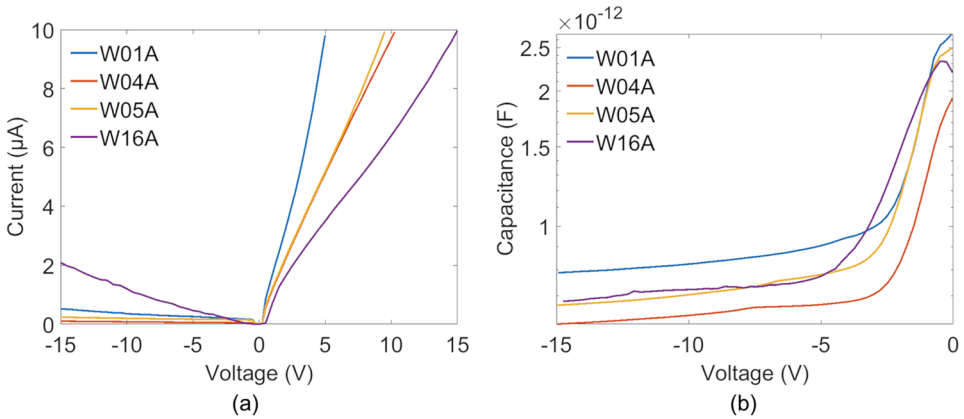

FIG. 5. (a) IV and (b) CV characteristics of Schottky diodes fabricated on different wafers.

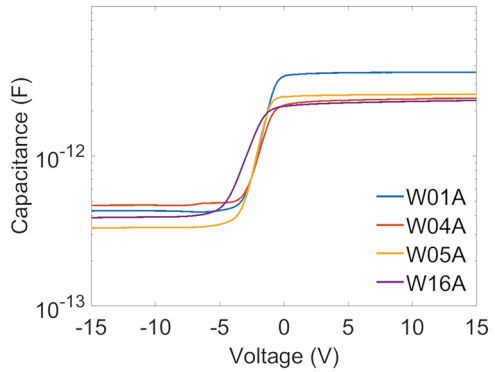

FIG. 6. CV characteristics of MOS fabricated on different wafers.

CV (FIG. 5.b) characterizations confirm a standard Schottky behavior.[21]

Both CV and IV measurements are consistent with standard Schottky diode characteristics composed of an N-type doped substrate, since the reverse biasing is obtained by setting the Schottky electrode to negative values (see FIG. 5). However, since the doping of silicon is expected to be P-type, such a reverse bias configuration should occur with a positive voltage on the Schottky contact. This unexpected behavior is also evidenced in measurements on MOS capacitors fabricated on the same substrates of Schottky diodes (i.e. W01A, W04A, W05A, W16A) in FIG. 6, and by the polarity of the induced current from TCT measurements (see section B). Therefore, it seems that, at a certain stage of the fabrication process, doping type inversion occurred. This surprising finding could be explained by the generation of thermal donors that takes place during the high temperature process prior to the wafer bonding (oxidation) and by the annealing (performed at 400 °C on some wafer). Indeed, as reported by Bruzzi et al.,[22] these rather low temperature processes can activate oxygen in silicon to generate donors, that can reach a concentration high enough to invert the doping type of silicon. The range of temperatures at which this occurs spans from 300°C to 900°C, with two peaks in the donors generation rate at 450°C and 750°C.[23] Therefore, the doping of the silicon bulk at the end of the process happens to be N-type, due to type inversion occurred by the thermal donor generation.

IV. TCT MEASUREMENTS

A. Edge TCT measurements

Schottky diodes and the bonding interface between the 2 wafers were tested using a collimated IR pulsed laser (λ=1064 nm, 10 μm Gaussian waist, with Gaussian pulse duration, FWHM, of 500 ps and power of 0.7 mW) under edge injection.[15] The voltage was applied from the top of the diode (from the Schottky contact), keeping the backside grounded (as in the CV and IV measurements described in Section III). Transients were amplified by means of a broadband current amplifier (CIVIDEC C2HV-TCT, gain 40 dB, bandwidth 2 GHz) and time resolved using an oscilloscope (Agilent DSO9254A). The collected charge was measured by integrating the transient current signal (typically over 25 ns). Two dimensional maps of the collected charge are shown for the diodes W16A (reference wafer, FIG. 8.a) and W01A (bonded wafer, in FIG. 8.b), at -60 V. From these measurements, it is possible to observe the extension of the depletion region under the diode (since the charge generated by the laser is mainly collected in the depletion region). The coordinate reference system is reported in figure FIG. 7.a, where the cross section of the diode is shown as taken along the aluminum wire direction, as shown in FIG. 7.b.

From FIG. 8.a, we observe that diode W16A (reference) is depleted isotropically, since there is no barrier in the bulk. The long tail on the right side of the plot represents an electric field generated by capacitive coupling between the contact pad, the metal line and the underneath silicon (see FIG. 4.b) through the passivation oxide. Calculating the depletion depth from FIG. 8.a., an effective doping concentration (donors) of 10^{12} cm^{-3} is obtained. It is not possible to extract this value from CV measurements shown in FIG. 5.b and FIG. 6, since with this doping value, the capacitance at reverse bias should be on the order of 10^{-14} F, too small to be measured. This value is consistent with previous studies of thermal generation of

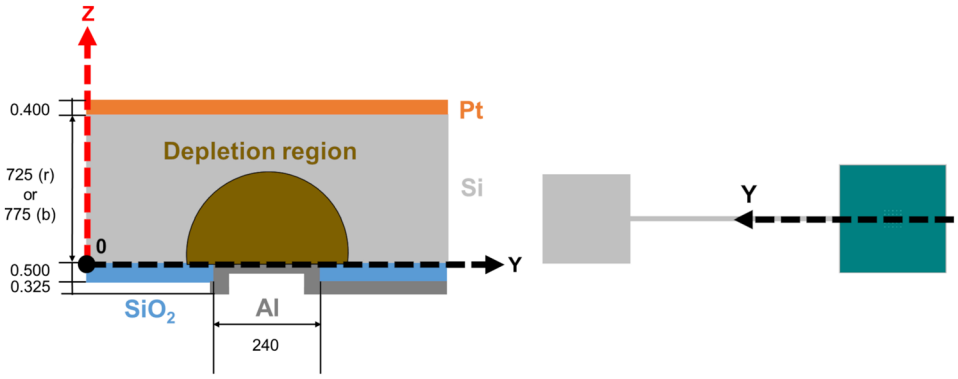

FIG. 7. (a) reference system of 2D plots shown in FIG. 8, based on the cross section of the Schottky diode in FIG. 4.a. The cross section is taken along the direction shown in (b) on the layout. In (a), the black dot indicates the position of the 0, while the brown semicircle shows where the depletion region is located. All dimensions are expressed in μm.

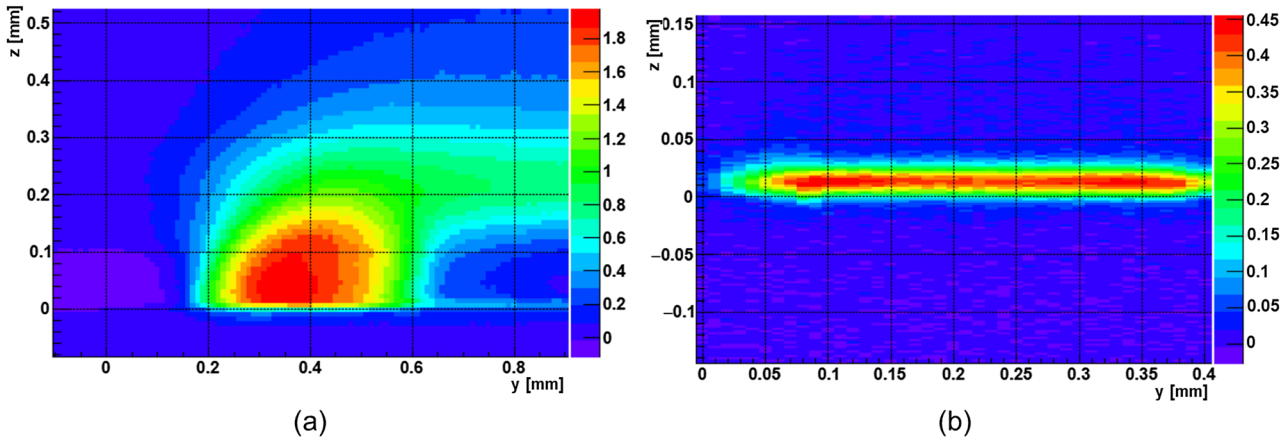

FIG. 8. collected charge in C (color scale) for (a) the reference diode (W16A) and (b) for the bonded wafer (W01A) for an applied voltage of -60V. Note the difference in vertical and horizontal scales.

donors.[22] The bonded wafer, FIG. 8.b, shows a completely different shape of the depletion region. Indeed, this is much more confined than in diode W16A (reference). Since the only difference between the two diodes is the presence of the bonding interface, a first conclusion is that this layer of amorphous silicon limits the electric field at the interface, blocking collection of charges generated in the bottom part of the bonded diode. To obtain more information about the electrical properties of the bonding interface, and to compare different bonding tests, top illumination TCT was performed.

B. Top TCT measurements

Top TCT measurements (meaning that illumination with light is performed from the top side of the diode, where the Schottky contact is implemented) were conducted with a pulsed laser working at a wavelength of 660 nm (with Gaussian pulse duration, FWHM, of 500 ps and power of 1.35 mW). The spot diameter on the surface of the device is focused to 10 μm and illumination occurs through the holes in the metal layer in the center of the diode (see FIG. 4.b). Biasing and readout of the diode was identical to the edge-TCT measurement. In this measurement, only one type of carriers, electrons, traverses the bulk. Indeed, the biasing imposes that holes are instantaneously collected at the Schottky contact (where negative voltage is applied), while electrons drift across the bulk. Due to the high absorption of red light in silicon, the holes drift is too quick to be resolved with a 2 GHz band-width. Results for the diode W16A (reference, FIG. 9.a) are compatible with the TCT of a partially depleted Schottky diode (as it will be shown in FIG. 11, where a comparison between analytical calculations for a partially depleted diode and measurements are presented). In this case, different bias voltages are applied, and the shape of the TCT signal agrees with Ramo's theorem.[13] The situation is different for the bonded wafers W01A where the shape differs from the reference diode (FIG. 9.b). A first peak is observed at around 2 ns, followed by a slowly decaying tail. As in e-TCT, this is a clear signature of the effect of the bonding interface.

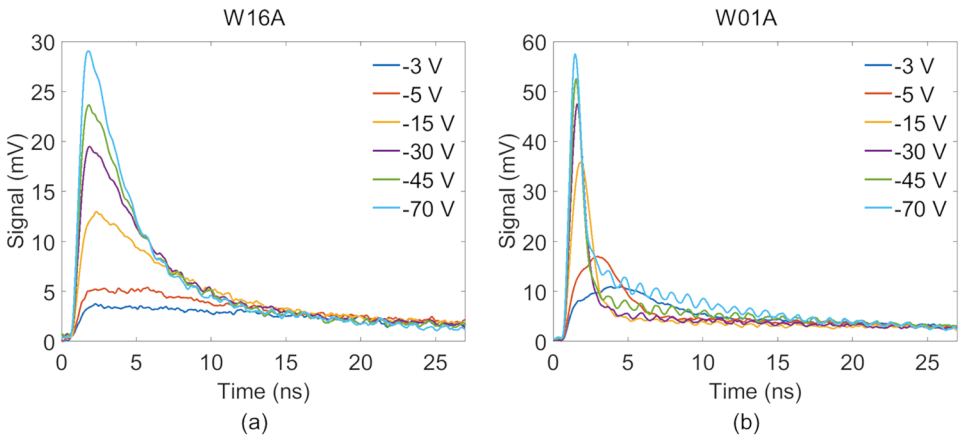

FIG. 9. TCT signals from measurements on diodes (a) W16A (reference) and (b) W01A (bonded), at different bias voltages.

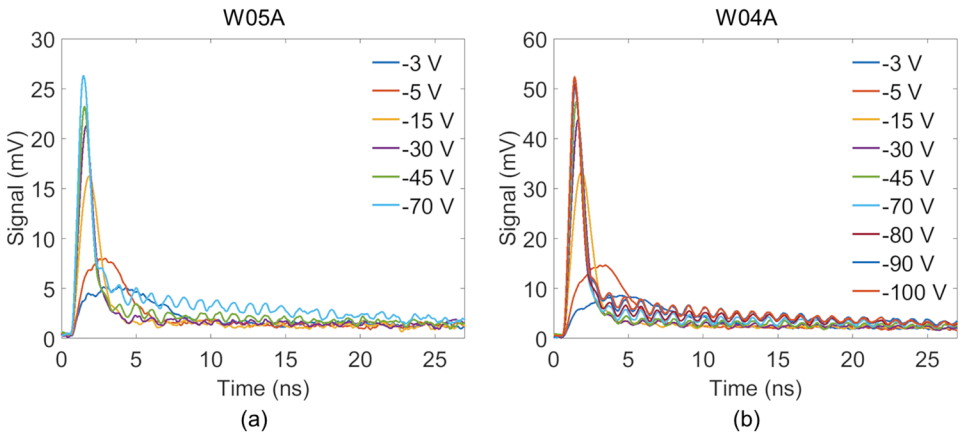

FIG. 10. TCT voltage scans on bonded diodes (a) W05A and (b) W04A.

This behavior is further confirmed in FIG. 10 reporting TCT measurement of two additional bonded diodes, W05A (FIG. 10.a) and W04A (FIG. 10.b). These shapes are similar to the one observed in diode W01A, but W04A is slightly different when looking at the long tail after 3 ns. Indeed, for diodes W01A and W05A the amplitude of the long tail starts to increase with the bias for applied voltages larger than -45 V. For diode W04A, we can also observe such a behaviour, but for voltages larger than -70 V. In the next section, an analysis of TCT curves is performed in details with additional simulations using the analytical model presented by Bronuzzi et al.[10]

C. Discussion

In order to understand the behavior of the bonding interface, the analytical model developed in previous publication[10] is used. This gives a fast and comprehensive analysis of the interface influence on the top TCT signal. In all simulations, electrons and holes mobilities are respectively 1418 m^2/Vs and 470.5 m^2/Vs. A first simulation was performed in order to determine the doping concentration of the silicon bulk, by comparing the results of the analytical model for a standard diode with the measurements on the reference wafer W16A. In FIG. 11 it is possible to observe a good matching (transient current shapes are similar) between analytical model and measurements, for a diode with an N-type bulk doping concentration of 1.5×10^{12} cm^{-3} (close to the value obtained from e-TCT measurements analysis), reverse biased at -70 V.

In the work of Flötgen et al.[1] the bonding interface generated by the wafer bonding technique was found to be an amorphous layer 3 nm thick. Introducing this layer in the developed analytical model,[10] a good matching with experimental data is obtained for an ionized trap density of the order of 3×10^9 cm^{-2} (obtained by introducing bulk traps, 10^{16} cm^{-3}, into the interface layer, and then by multiplying this value by 3 nm). Indeed, simulations of bonded diodes show that the introduction of an interface layer with these traps concentration gives curves with the same shape of measured ones. The most important parameter in this case happens to be the quantity of ionized traps, which influences the electric field profile of the diode by introducing a discontinuity at the interface.[10] In FIG. 12, it is possible to observe 3 simulated curves for different ionized traps densities (2.7×10^{10} cm^{-2}, 5.7×10^{10} cm^{-2} and 8.7×10^{10} cm^{-2}) and compare them with measurements of diode W01A (bonded) at -70 V. Obviously, there is a strong influence of the interface trap density on the whole TCT shape,

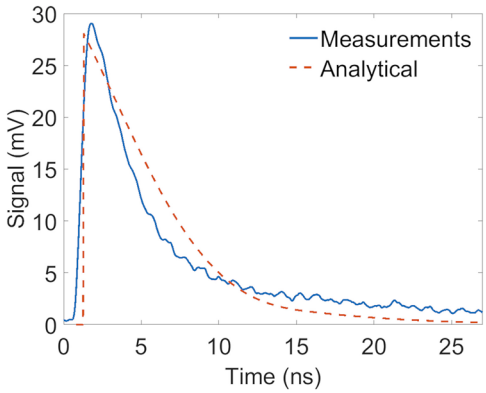

FIG. 11. Comparison between analytical simulations and measurements on diode W16A (reference) at -70 V.

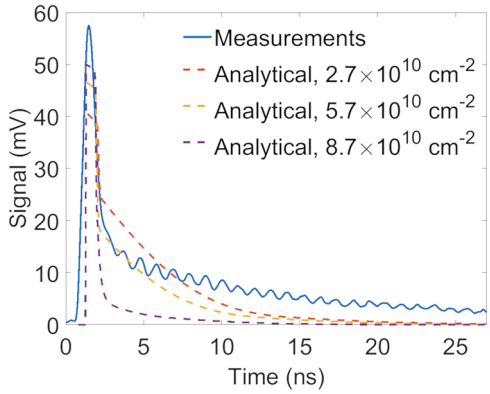

FIG. 12. Comparison between analytical simulations with different ionized traps densities and measurements on diode W01A (bonded) at -70 V.

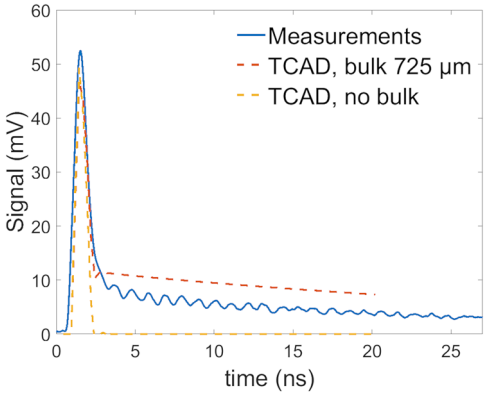

FIG. 13. Comparison between Sentaurus TCAD simulations and measurements, with and without the 725 μm bulk, at -45 V, with 5.7×10^{10} cm^{-2} ionized traps (in case of bonded diode W01A).

and the best matching is obtained for a density of charge of 5.7×10^{10} cm^{-2} (donor traps, positively charged).

Note that the long tail that is visible after 3 ns in measurements (FIG. 9 and FIG. 10) is not present in the analytical model simulations. By performing the same simulations with Sentaurus TCAD, it is possible to deduce that this tail is related to diffusion of electrons in the undepleted bulk, once they reach the end of the depletion region, the only charge transport mechanism possible in absence of electric field. Indeed, in FIG. 13 the simulations performed at -45 V of the Schottky diodes are shown, with 5.7×10^{10} cm^{-2} ionized traps, with the 725 μm thick bulk and without it, compared to measurements. The tail disappears in absence of the bulk.

To add the contribution of the undepleted bulk to the analytical model, the tail from measurements was fitted with an exponential decay such as exp(−βt), with β=0.0203 ns^{-1}. Adding this exponential to the model (in FIG. 14), it is possible to observe good matching (similar shapes of the transient current) between the simulated and the measured data, in both cases, bonded and reference diodes, using the same parameters of simulations in FIG. 11 and FIG. 12.

To explain the reason for which the long tail after 3 ns starts to be influenced by the applied voltage for values higher than a certain threshold, it is necessary to observe the electric field profile, shown in FIG. 15.a for TCT with an ionized trap density equal to 5.7×10^{10} cm^{-2}. From this plot, we observe 2 regimes: one where the discontinuity of the electric field cancels it at the interface (depth of 50 μm), which happens at relatively low voltages, and the other at higher voltages where, the electric field extends beyond the interface, creating a depletion in the subsequent bonded wafer.

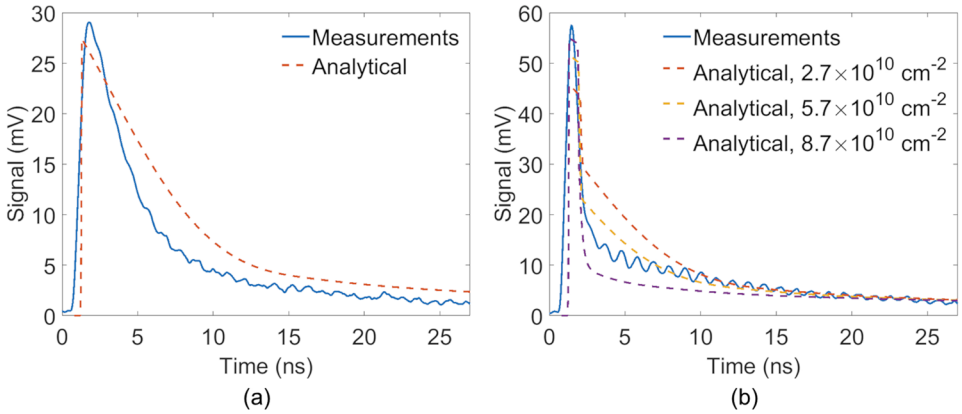

FIG. 14. Comparison between analytical model with exponential tail and measurements, (a) in case of diode W16A (reference) and (b) in case of diode W01A (bonded).

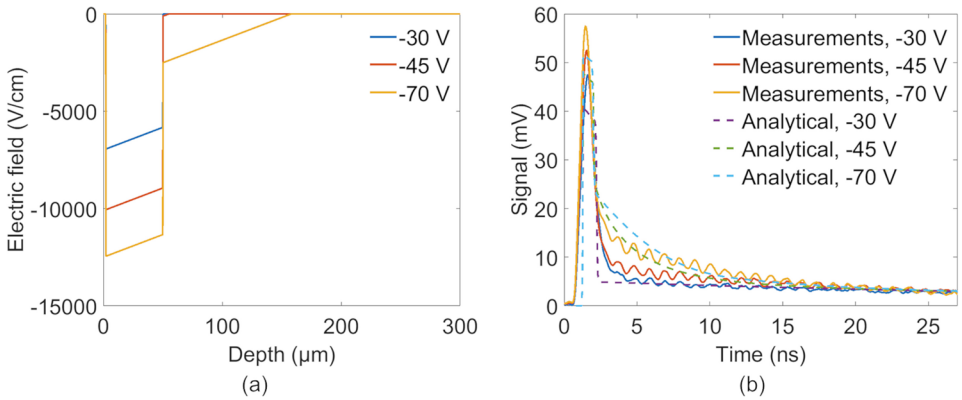

FIG. 15. (a) Electric field profile from analytical simulations of diode W01A (bonded) for different applied voltages, at an ionized traps density of 5.7×10^{10} cm^{-2} and (b) TCT signal simulations with the same parameters.

TABLE II. values of interface traps densities for measured bonded diodes.

Diode	Voltage Threshold (V)	Traps density (cm^{-2})	Surface treatment	Annealing temperature
W01A	-45	5.7×10^{10}	Hydrophobic	400°C
W04A	-70	9.3×10^{10}	Hydrophobic	Room T
W05A	-45	5.7×10^{10}	Hydrophilic	400°C

Indeed, considering measurements on the diode W01A (FIG. 15.b), if the bias voltage is lower than -45 V, the long tail does not depend on the voltage since the bulk of the bottom wafer is not depleted, and it can be explained by diffusion of charges in the undepleted volume. However, when the voltage is higher than -45 V, the electric field is higher than the discontinuity introduced by traps at the interface, and therefore the depletion region will extend in the bottom part of the wafers stack. The presence of an electric field will generate a drift across the bonding interface, meaning that the tail of the TCT signal will now be generated by the electric field. This result is evidenced by the analytical model[10] for two different regimes. The first one is when a diode of 50 μm thick is considered, and is valid for 'low' voltages (-45 V in case of diode W01A) where the depletion region is confined by the charged interface (for instance, -30 V in FIG. 15.a). The second case is when the depletion region extends further in the bottom wafer, which occurs for higher voltages (for instance, -70 V in FIG. 15.a). FIG. 15.b illustrates the currents simulated with the analytical model, compared with measurement done on diode W01A. From these considerations, the density of equivalent ionized traps can therefore be obtained by simulating a TCT curve with the same shape of measurements for voltages where depletion extends over the bonding interface. The values obtained for the diodes considered in this work are presented in TABLE II.

These values give a first hint on the impact of different process bonding parameters. For instance, it seems that annealing at 400°C reduces the density of ionized traps, while the surface treatment prior bonding does not affect this parameter. This could be explained by considering that the ion treatment before bonding completely eliminates the silicon oxide on the surface, even if some oxygen atoms could be displaced inside the silicon during the bombardment of the plasma cleaning (this is the reason why the two cases, hydrophobic and hydrophilic, are studied). Similarly, a lower traps density could be related to a better quality interface, consistent with the fact that stacks W01A and W05A were annealed, while stack W04A was not.

V. CONCLUSION

In this paper, a method for the characterization of amorphous interfaces in bulk silicon wafers generated by a direct bonding process using TCT was presented and discussed in detail. It consist in three main steps: the bonding of silicon wafers, the fabrication of test structures based on Schottky diodes on these wafers, and the measurements and analysis of diodes with different methods: IV, CV, eTCT and top TCT. Results show that despite the fact that the interface is electrically conductive in the common sense, free carriers transport across it is not guaranteed because of electrostatic blockage arising with interface charge traps. Moreover, we prove that an estimation of the charged traps concentration is also feasible. To conclude, the bonding process analyzed in this paper generates an interface which prevents mobile charges to be collected by an active circuit implemented across the interface. Combining the approach exposed in this work with additional experiments should give an in-depth understanding of interface charge density generated during wafer bonding.

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