SILICON n-CHANNEL METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR FABRICATION AND ITS EFFECT ON OUTPUT CHARACTERISTICS

MOHD MARZAINI BIN MOHD RASHID

UNIVERSITI SAINS MALAYSIA

2012

SILICON n-CHANNEL METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR FABRICATION AND ITS EFFECT ON OUTPUT CHARACTERISTICS

By

MOHD MARZAINI BIN MOHD RASHID

Thesis submitted in fulfillment of the requirements
for the degree of
Master of Science

UNIVERSITI SAINS MALAYSIA

October 2012

ACKNOWLEDGEMENTS

My highest gratitude is to Allah S.W.T whom without His guidance and will I would not have been able to complete this thesis. I would like to express my sincere gratitude to my main supervisor, Prof. Dr. Kamarulazizi Ibrahim for his valuable guidance, ideas and support throughout the whole period of my work in this project. I am equally grateful to Associate Prof. Dr. Azlan Abdul Aziz for being my second supervisor and giving valuable inputs for this research project. I am very thankful to the Dean of School of Physics, Prof. Dr. Zainuriah Hassan for her support towards the completion of this thesis.

I would like to express my special thanks to the technical staff from Solid State Lab and NanoOptoelectronic Research and Technology Laboratory (N.O.R) for their technical support that keeps the research going. My appreciation goes to fellow colleagues Ooi Poh Kok, Zamir Pakhuruddin and many others who have shared ideas, experience and taught me the experimental aspects of research.

I am most grateful with the financial assistance provided for me via the ASTS (Academic Staff Training Scheme) by School of Physics, Universiti Sains Malaysia and Ministry of Higher Education.

Last but not least, I would like to thank my wife, parents and family who have always supported me, endured with me and motivated me to complete this research work.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLE

LIST OF SYMBOLS

A	Area
B	Parabolic rate constant
B/A	Linear rate constant
C_{OX}	Oxide capacitance /maximum capacitance in accumulation
D	Diffusion coefficient
D_o	Frequency factor
E_A	Activation energy
E_C	Conduction band
E_F	Fermi level
E_{Fi}	Fermi level of intrinsic semiconductor
E_g	Energy bandgap
ε_S	Permittivity of silicon
ε_{OX}	Permittivity of oxide
E_v	Valence band
g_d	Output conductance
g_m	Transconductance
I	Current
I_{DS}	Source to drain current
I_s	Saturation current
k	Boltzmann's constant
μ	Carrier mobility
n	Ideality factor
N	Carrier concentration
N_A	Acceptor concentration
N_B	Substrate carrier concentration
N_D	Donor concentration

N_i	Intrinsic carrier concentration
N_o	Dopant concentration at wafer surface
ϕ_F	Bulk potential
ϕ_S	Surface potential
q	Electronic charge
Q	Dose of dopant
Q_T	Effective oxide charge
R_s	Sheet resistance
T	Absolute temperature
t	time
τ	Oxidation time for initial oxide thickness
T_m	Diffusion temperature
t_m	Diffusion time
T_{ox}	Oxide thickness
V	Voltage
V_{DS}	Source to drain voltage
V_{FB}	Flatband voltage
V_{GS}	Gate to source voltage
V_T	Threshold voltage
W/L	Transistor width/channel length
W_M	Modified Al metal workfunction
W_{MS}	Metal to semiconductor workfunction difference
x	Distance from wafer surface
X_j	Junction depth
X_O	Oxide thickness
χ_S	Modified substrate electron affinity

LIST OF ABBREVIATIONS

AFM	Atomic force microscope
Al	Aluminium
BOE	Buffered oxide etchant
CMP	Chemical mechanical planarization
C-V	Capacitance-voltage
CVD	Chemical vapor deposition
DCS	Dichlorosilane
DI water	Deionised water
DWD	Dry/wet/dry
EBL	Electron beam lithography
EDX	Energy dispersive X-ray
FILOX	Fillet local oxidation
FTIR	Fourier transform infrared spectroscopy
HCl	Hydrochloric acid
HF	Hydrofluoric acid
H_2	Hydrogen gas
H_2SO_4	Sulphuric acid
H_2O	Water
H_2O_2	Hydrogen peroxide
HMDS	Hexamethyldisilazane
HNO_3	Nitric acid
I-V	Current-voltage
LPCVD	Low pressure chemical vapor deposition
MBE	Molecular beam epitaxy
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NH_4OH	Ammonium hydroxide
O_2	Oxygen gas
PLA	Pulsed laser annealing
PMA	Post metallization anneal
PSG	Phosphosilicate glass
RTD	Rapid thermal diffusion
SEM	Scanning electron microscope
Slm	Standard litre per minute
Si	Silicon
SiH_4	Silane
SiO_2	Silicon dioxide
SDE	Source drain extension
SOD	Spin on dopant
SSD	Solid source diffusion
TEOS	Tetraethylorthosilicate
TMAH	Tetramethylammonium hydroxide

VMOSFET	Vertical Metal Oxide Semiconductor Field Effect Transistor
VRG	Vertical Replacement Gate

LIST OF PUBLICATIONS/CONFERENCES

1. Rashid, M., Ibrahim, K., Abdul Aziz, A., Ooi, P. K. (2009) Impact of Silicon Surface Roughness upon MOS after TMAH and KOH Silicon Etching. American Institute of Physics Conference Proceedings Vol. 1250 PP. 85-88

2. Rashid, M., Ibrahim, K., Abdul Aziz, A., Ooi, P. K. (2010) Silicon Anisotropic Wet Etching Using TMAH In Sidewall Fabrication of VMOSFET. 3rd International Conference On Functional Material and Devices (ICFMD), 13-17 June 2010, Terengganu, Malaysia (Oral).

FABRIKASI TRANSISTOR SEMIKONDUKTOR LOGAM OKSIDA KESAN MEDAN SALURAN n-SILIKON DAN KESANNYA TERHADAP CIRI-CIRI KELUARAN

ABSTRAK

Fabrikasi transistor semikonduktor logam oksida kesan medan saluran n-silikon, "n-channel metal oxide semiconductor field effect transistor (n-MOSFET)" memerlukan teknologi khusus dan berkos tinggi seperti penanam ion, endapan wap kimia dan gas-gas berbahaya seperti silane, asid hidroklorik dan hidrogen. Topeng foto berkos rendah dengan lebar saluran 35 μm digunakan di dalam projek ini. Bagi mengurangkan lebar saluran dan supaya tidak tertakluk kepada had dimensi pada topeng foto, dua kaedah telah diguna pakai. Yang pertama, adalah melalui cara lebihan cetakan pada fotorintang dan kedua melalui fabrikasi struktur MOSFET yang berbeza iaitu MOSFET menegak atau "vertical MOSFET (VMOSFET)" yang mana lebar saluran dikawal melalui punaran Si menggunakan "tetramethylammonium hydroxide (TMAH)" dan tidak bergantung kepada fotolitografi.

Proses-proses yang perlu dalam fabrikasi MOSFET tersebut dikaji seperti punaran Si, pengoksidaan Si dan pendopan fosforus menggunakan teknik "spin on dopant (SOD)" secara resapan terma. Permukaan Si yang rata pada 20 nm rms selepas punaran telah diperolehi menggunakan TMAH pada kepekatan 18 % berat dengan kadar punaran pada 0.3 μm/minit. Bagi pendopan fosforus melalui teknik SOD, suhu proses resapan terma pada 950˚C diguna pakai bagi mengurangkan kebocoran pada simpang p-n. Bagi menuruti proses

penghidrogenan pada antara muka Si-SiO_2, pengoksidaan get kering/basah/kering disusuli dengan proses sepuh lindap selepas perlogaman Al pada suhu 450˚C dalam persekitaran N_2 telah dilakukan. Voltan pecah tebat yang lebih tinggi dan rintangan terhadap kebocoran oksida dilihat lebih baik pada oksida kering/basah/kering berbanding oksida kering. Bagi mendapatkan ciri-ciri jajar-diri pada topeng oksida untuk pendopan fosforus pada dinding sisi Si (111), proses pengoksidaan Si pada suhu 900˚C menunjukkan ketebalan oksida yang lebih tinggi pada 30% bagi nisbah SiO_2 (111)/SiO_2 (100) berbanding hanya 12% pada suhu 1000˚C kerana pemalar kadar lelurus yang sensitif pada orientasi kristal lebih dominan pada suhu pengoksidaan yang rendah. Sebuah peranti MOSFET saluran n Si dengan lebar saluran 20 µm yang berfungsi telah difabrikasi dan mempunyai arus pacu sebanyak 13.8 µA/µm, kealiran sebanyak 2.93 mS/mm dan mobiliti saluran pada 217 cm^2/V.sec. Ini membuktikan kaedah lebihan cetakan fotoresis dalam mendapatkan lebar saluran yang lebih kecil (pengurangan sebanyak 15 µm) daripada topeng foto boleh dilaksanakan. Voltan ambang yang diperolehi pada -4V adalah rendah mungkin dipengaruhi oleh kebocoran voltan balikan pada simpang p-n, laluan pengaliran dalam substrat Si ataupun disebabkan kesan saluran bocor di permukaan. Tiada tindakan transistor ditunjukkan dalam ciri-ciri keluaran VMOSFET dan ini dikaitkan kepada penembusan fosforus melalui topeng oksida pada dinding sisi. Kesan kebocoran get oksida dan rintangan tinggi terhadap ciri-ciri keluaran n-MOSFET telah dicerap dan diterangkan yang mana arus negatif pada I_{DS} dan kenaikan I_{DS} yang lambat berlaku pada voltan V_{DS} yang rendah bagi setiap keadaan yang tersebut.

SILICON n-CHANNEL METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR FABRICATION AND ITS EFFECT ON OUTPUT CHARACTERISTICS

ABSTRACT

n-channel metal oxide semiconductor field effect transistor (n-MOSFET) fabrication requires specialized and expensive technologies such as ion implantation, chemical vapor deposition (CVD) and hazardous gases such as silane (SiH_4), HCl and hydrogen. Low cost emulsion photomask with 35 µm channel length is used in this work. To reduce the device's channel length, and not be dependent on the dimensional limitation of the photomask, two methods are employed. One is by overdeveloping of photoresist and fabricating a different MOSFET structure namely the vertical MOSFET (VMOSFET) where channel length is defined by anisotropic Si etching using tetramethylammonium hydroxide (TMAH) instead of lithography. Required processes for fabrication which are Si etching, Si oxidation and phosphorus doping by spin on dopant (SOD) technique were studied. Smooth etched Si surface at 20 nm rms was obtained for TMAH concentration of 18 wt% having etch rate at 0.3 µm/min. In SOD phosphorus diffusion, 950˚C diffusion temperature was used to minimize p-n junction leakage. To emulate hydrogenation of Si-SiO_2 interface, dry/wet/dry gate oxidation follow by post Al metallization anneal at 450˚C in N_2 ambient was done. Higher oxide breakdown and better retention to oxide leakage was observed for dry/wet/dry gate oxide compared to dry gate oxide. For a self

aligned oxide doping mask on VMOSFET Si (111) sidewall, oxidation at lower temperature 900˚C achieved 30% thicker SiO_2(111)/SiO_2(100) compared to 12% at higher temperature of 1000˚C due to the crystal orientation-sensitive oxidation linear rate constant dominating at lower temperature. A functioning 20 µm channel length planar n-MOSFET has been fabricated having drive current of 13.8 µA/µm, transconductance at 2.93 mS/mm and channel mobility at 217 cm^2/V.sec. This validates the feasibility of photoresist overdevelopment to reduce channel length so that it is narrower than defined by the photomask. Obtained threshold voltage V_T was low at -4V suspected due to p-n junction reverse bias leakage, conduction paths in Si substrate or due to surface channel leakage effects. No transistor action occurred in VMOSFET output characteristics suspected due to phosphorus dopant penetration through the oxide mask on its sidewall. Effects of gate oxide leakage and high resistance on planar n-MOSFET's output characteristics were observed and explained where negative drain to source current (I_{DS}) and slower I_{DS} increase at low drain to source voltages (V_{DS}) occurred for the respective conditions.

CHAPTER ONE

INTRODUCTION

1.1 Field effect transistor fabrication in Malaysia

The advancement in computing, power management and telecommunications as we know it would not have been possible without the small yet powerful transistors that drive these technologies. The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the most produced transistor and has been continuously downscaled following Moore's Law to increase its performance while reducing cost. Its importance is widespread and is used for both digital and analog applications ranging from small hand held gadgets to microprocessors and motor controllers.

Malaysia has long been a major exporter of semiconductor devices, being mainly focused on test and assembly. Only a decade ago, the country has shifted to front end processing involving the fabrication of transistors with foundries exporting Malaysian made integrated circuits overseas; strengthening the country's competitiveness in the industry [1]. These foundries utilized the latest technologies in a class 10 and below cleanroom to fabricate sub micron gate transistors. The technology of today employs the polysilicon gate that allows self aligned doping of the MOSFET's source and drain region using ion implantation. Device patterns are miniaturized from reticles using projection aligners and do not require human intervention.

Academic and research institutions in Malaysia have also carried out research related to transistors even before the industry step foot in the country [2,3]. The processing method in the university labs differ due to safety concerns which avoid hazardous materials such as silane and hydrogen, and also restricted from certain technologies due to the exorbitant price of the equipments used in production such as ion implanters. In the absence of chemical vapor deposition (CVD) processes to fabricate polysilicon gate, metal gate technology can be used instead. The metal gate technology used in MOSFET fabrication has the source and drain doping process before the gate is fabricated, therefore loses the advantage of self aligned process where the gate could serve as the doping mask. A good control of layer to layer alignment would be required to ensure the overlapping of gate over the source and drain region**.**

In order to achieve short channel lengths custom made chrome masks that could define 1 µm line widths are required. These masks however are costly. Another alternative is fabrication using electron beam lithography (EBL) to achieve sub micron gate lengths at the expense of throughput. For academic purposes and faster learning curve, several labs prefer the use of low cost photomasks plotted on photosensitive films as an alternative at the expense of resolution which is typically within 20-30 µm minimum structure size [4,5]

Numerous university fabrication labs in Malaysia have developed their fabrication technologies unique to the environment and facilities available to each institution [6,7]. Some are working towards sub micron technologies in their fabrication work.

1.2 Problem Statement

In n-MOSFET fabrication, a metal gate can be used in replacement for polysilicon gate which requires silane gas and chemical vapor deposition. A simpler thermal evaporation process is used for the metal gate. In metal gate technology where self aligned source and drain doping process is not available, the mask alignment plays a more critical role to ensure proper placement of the source and drain regions.

To mitigate alignment error a workable alignment scheme is warranted. The conventional alignment marks for transistor fabrication are boxes over crosses and vice versa with minimum allowable tolerances designed in the spaces between the marks. The split field technique is a standard procedure to align distant alignment marks to aid the overlaying with previous layers. In this work, a refined alignment mark with dimension smaller than provided by the mask is etched using Si wet etchant tetramethylammonium hydroxide, TMAH. The mask to be used for transferring patterns has minimum structure size of 35µm. Therefore a modification in process would be required to achieve a narrower channel length than that defined by the mask. One method is by the overdevelopment of photoresist during source and drain definition. The other is by a different MOSFET design, forming an etched vertical channel in the VMOSFET (Vertical MOSFET) instead of a planar channel. In this structure the channel length is not defined by the mask, but determined by the depth of the Si etch. In VMOSFET fabrication the conventional methods utilizes Si epitaxy and insitu doping or by means of

Si sidewall etching in combination with spacer technique to cover the sidewall as doping mask. The spacer technique requires chemical vapor deposition (CVD) for a controlled spacer thickness. An alternative to be explored in this work is to achieve self aligned doping mask on the Si (111) sidewall etched using anisotropic tetramethylammonium hydroxide (TMAH) and achieving thicker SiO_2 on the sidewall compared to the planar surface. The thicker oxide is dependent on crystal orientation of the sidewall.

Amongst methods used to improve the properties of gate oxide is by incorporating Cl into the oxide using hydrochloric acid (HCl), tetrachloroethylene (TCE) or tetrachloroethane (TCA). However Cl is corrosive to metallic parts of the furnace and harmful if exposed to people in a lab environment. Another known method is through hydrogenation where H_2 anneals the Si-SiO_2 interface using forming gas (10% H_2 + N_2). The setback is that H_2 gas is explosive and poses safety hazards. As an alternative, it has been known that the post metallization anneal at low temperature (350˚C -500˚C) using Al as metal gate on top of SiO_2 can provide Si-SiO_2 annealing effect. It is akin to hydrogenation where Al react with moisture in the oxide to produce H_2. In this work, moisture or Si-OH is purposely added to the oxide to assist annealing effect in the post metallization anneal using dry/wet/dry gate oxidation.

1.3 Research Objectives

Without ion implantation and chrome photomask, the main objective is to reduce channel length smaller than defined by the mask, improving gate oxide Si-SiO_2 interface quality for higher breakdown voltage and facilitate gate overlapping the source and drain regions in metal gate technology. The following sub objectives are laid out to achieve them;

1. To fabricate Si (111) sidewall by anisotropic Si etching, achieve n-type Si doping by spin on dopant (SOD) technique and use silicon dioxide (SiO_2) as etching and diffusion barrier in fabrication process.
2. To fabricate planar n-MOSFET with channel length defined by overdeveloped photoresist, Si etched alignment marks, dry/wet/dry gate oxidation, Al post metallization anneal and observe resulting output characteristics.
3. To fabricate n-channel VMOSFET with channel length defined by wet anisotropic Si etching, design for self aligned oxide doping mask by thicker oxide on Si (111) sidewall and observe resulting output characteristics.

1.4 Scope of Research

In this work the semiconductor used was specifically silicon (Si) and the device fabricated was n-channel MOSFET. Chrome photomask, ion implantation and chemical vapor deposition (CVD) were not utilized. Five layer masks were designed in AutoCAD for planar n-MOSFET with feature size of 35 μm and plotted onto photosensitive films. VMOSFET required two different photomasks for its diffusion and sidewall etch to define its channel length. Global and local alignment marks were designed to minimize alignment errors. TMAH as the Si anisotropic etchant was used to etch alignment marks into the p(100) 1-10 Ω.cm Si substrate. Local alignment marks were etched at every device area and the alignment is refined based on the lateral edge width of the etched Si (111) sidewall.

For planar n-MOSFET, the channel length was defined by the overdeveloped photoresist controlled by developing time of the doping mask and verified through the optical microscope to obtain smaller dimension than the mask but avoiding broken photoresist. The doping process was by thermal diffusion using the phosphorus spin on dopant technique (SOD).

At the same time, VMOSFET structure was fabricated to have channel length independent of the lithography process but dependent on the Si TMAH etching time. The SiO_2 doping mask (on sidewall) was based on Si orientation dependent oxidation to achieve thicker oxide on VMOSFET sidewall compared to its planar surface.

The gate oxide was thermally grown using the atmospheric thermal furnace using dry/wet/dry sequence to incorporate moisture in the dry oxide and promote annealing

effect at low temperature (450˚C) Al post metallization anneal (PMA) step as alternative to hydrogenation process.

Al metallization was performed using thermal evaporation and patterning done by lift off technique. The final Al annealing (PMA) was done using the thermal anneal furnace.

1.5 Organization of Thesis

Chapter 1 introduces the importance and role of MOSFETs in the electronics industry and the participation of higher education institutions in the MOSFET fabrication technology. The limitations and issues related to MOSFET fabrication and problem statement is highlighted. Scope and objectives of the research is outlined in this chapter.

Chapter 2 includes literature review on MOSFET fabrication history, its fabrication trend and the techniques available and feasible in lab environment to fabricate MOSFET device.

Chapter 3 covers the basic theories underlying the processes and standard techniques used in MOSFET fabrication, the physics in p-n junction, metal-oxide-semiconductor capacitor and MOSFET device operation.

Chapter 4 presents the materials and equipments used to realize the fabrication of MOSFET. Methods and details of step by step fabrication sequences are included in this chapter.

Chapter 5 shows the experimental data, observations during experiment and discussions on the findings based on the flow of fabrication process.

Chapter 6 concludes on the overall findings and assesses the results of experiment. Recommendations for improvements in future work are given.

1.6 Originality of work

Originality of this work reside in combination of two processes to emulate hydrogenation namely the dry/wet/dry gate oxidation process to incorporate moisture in the dry oxide and the post Al metallization anneal (PMA) at 450˚C. As alternative to the spacer technique in VMOSFET fabrication, a different processing method to achieve self aligned doping by enhancing Si (111)/ Si (100) oxide thickness ratio was explored.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter the current role of MOSFET in advancing technology, its history and fabrication trends are presented. The adaptation of MOSFET fabrication technology without ion implantation and feasible techniques for its fabrication is discussed.

2.2 Metal Oxide Semiconductor Field Effect Transistor's dominant role in information and communication technology revolution

The metal oxide semiconductor field effect transistor (MOSFET) is the most common transistor fabricated for use in logic, memory and analog devices in both digital and analog circuits as a switch, memory cell or amplifier. Its dominance is due to its increasing performance and reduced cost when its dimensions are made smaller. Its low power consumption, increasing speed, more devices and functions at lower cost per device as its dimensions are scaled down has placed its primacy in the integrated circuits used in microprocessors and memories of computers [8,9]. The inception (patents in 1928 by Lilienfeld and further work by Shockley/Bardeen/Brattain in 1947) and invention of modern day MOSFET by Kahng and Atalla (1959) was an evolution but its impact towards information and computer technology was a revolution until at one point the

single MOSFET transistor dynamic random access memory (DRAM) is the most abundant man made object on earth [10]. The electronics revolution is driven by Moore's law (made by founder of Fairchild Semiconductor and Intel) stating that number of transistors double every 18 months. This exponential growth is translated to a USD 2 trillion electronics industry [10] benefitting from miniaturization that increase number of transistors per unit Si area consequently producing better and cheaper transistors.

2.3 MOSFET fabrication technological history and trend

In its humble beginning back in the 1950's, the MOSFET was lagging behind the bipolar junction transistor (BJT) and was considered not having a future due to electrical instabilities it was experiencing. Shockley's initial fabricated field effect transistors were unstable and had unsuccessful conduction modulation due to surface states. The instabilities associated to effect of surface states are now referred to as interface and oxide traps (interface of Si-SiO_2). This is closely related to the electrically active region of MOSFET at the surface (surface inversion as opposed to bulk conduction) where the periodic Si lattice is terminated and dangling bonds or defects mostly occur. Reverse leakage current in Si diode was observed by Kleinknecht and Seiler in 1954 where generation of holes and electrons by thermal excitation at electronic traps (atomic Si lattice imperfections) in space charge layer of p-n junction occurred through Shockley-Read-Hall generation-recombination mechanism.

There was a call for stabilizing the surface of Si. Growing SiO_2 on Si surface where p-n junction intersect with thickness 150Å-300Å (920˚C for 10-30 min) was

performed by Atalla [11,12] with reported 10-100 times reduction in diode reverse leakage current. This Si surface stabilization by oxide passivation was considered the triggering point of technology advance paving MOSFET's domination in IC fabrication beyond 1970's. The grown oxide however can be unstable due to sodium ion migration in the oxide. Pieter Balk at IBM in 1965 indicated that hydrogen can anneal out interface traps by reacting at both Si dangling bond and oxygen bond through hydrogenation (Balk's hydrogen bond model of deactivating interface and oxide traps) [11, 13]. The observed low state density after steam oxidation (wet oxidation) was probably caused by hydrogen as a by product during oxidation and retained in the oxide. Similar annealing mechanism in Al-SiO_2-Si in N_2 at 300˚C (post metallization anneal) was attributed to hydrogen created in reaction between Al and hydroxyl groups in the oxide. This observation was further supported when annealing effects were absent in 'ultra dry' oxide. Additional experiments by Deal *et al.* [14] where Si_3N_4 was placed in between Al and SiO_2 concluded that hydrogen migration was blocked and thus no annealing effect occurred supporting the reaction between Al and SiO_2 theory. It was observed that active metals like Al and Mg rather than less actives ones like Au and Pt reduced more interface traps at temperatures 350˚C-500˚C. This had brought about the common practice of annealing in forming gas (10% H_2 + 90% N_2) in today's wafer foundries.

Other techniques in improving oxide quality is by incorporating chlorine through hydrochloric acid (HCl), trichloroethylene (TCE) or trichloroethane (TCA) [15] flow with oxygen during dry oxidation. Cl was recognized to trap and immobilize sodium ions in the gate oxide. Gettering by phosphosilicate glass (PSG) [11,16] on top of gate oxide was another alternative to suppress sodium and metallic contamination. Dry oxide was

found to have higher density than wet oxide (2.27 g/cc for dry oxide compared to 2.18 g/cc for wet oxide grown at 1000˚C) where dielectric strength was observed to increase with increasing oxide density [17]. The wet oxide density can be increased with higher oxidation temperature. The advantage of dry oxidation is that dry oxygen has a cleaner ambient than water vapor where water having high dielectric constant can leach out impurities from surfaces it comes in contact with, which can later contaminate wafers. Nonetheless, dry oxide without post oxidation annealing has oxide fixed charge density higher than wet oxide without annealing. With post oxidation annealing or low temperature post metallization anneal, the final Si-SiO_2 interface can be similar between dry and wet oxides [14].

To change the conductivity type of Si, initial techniques used was junction alloying and later replaced by chemical sourced impurity diffusion in forming p-n junctions. Using SiO_2 as diffusion mask was a technique demonstrated by Frosch and Derrick (1957) [18] and its modeling provided by Sah, Sello and Tremere (1958) [19]. Doping by impurity diffusion became widespread practice until 1980's since transistor downscaling had not reached a critical point to control shallow junctions.

The ion implantation technique was proposed by Shockley in 1954 and had tremendous advantage over the other earlier techniques since controlled number of ionic impurities (B or P ion beams) can be placed at desired locations (lateral and depth) by controlling the beam energy. Ion implantation however warrant some requirements to work; that wafers were tilted 7˚ away from <110> direction to avoid channeling effects, implantation through a masking oxide to reduce Si sputtering and using pure P and B ions (mass separated). Wafers must be heated above 800˚C after implantation to repair Si

damage (amorphous to crystalline state) and to place implanted ions into substitutional sites (electrical activation) [20]. When shallow junctions were required, manufacturers converted from phosphorus diffusion to arsenic diffusion, however arsenic solid source created particle issues while chemical source arsenic showed lower levels of electrical activation (electrically neutral arsenic vacancy complexes at surface) compared to ion implanted arsenic. By the 1980's the industry adopted arsenic ion implantation for source/drain doping.

Kerwin, Klein and Sarace (Bell labs) introduced polysilicon gate technology in 1963 and using silicon nitride (Si_3N_4) as diffusion mask in 1968. These two innovations still dominate in today's MOSFET fabrication process. Prior to polysilicon gate, the planar process require the gate to be placed after source and drain diffusion since Al gate with melting point 660˚C could not withstand diffusion temperatures exceeding 900˚C. Accordingly, lithographic alignment was necessary to align the gate in between the source and drain with certain overlay tolerance to accommodate uncertainty of about one third of the placed feature's dimension [21]. As a result, the gate would have to overlap the source and drain region by about the uncertainty of the registration. This gate alignment dilemma was solved when using polysilicon gate that provided self alignment of gate over the source and drain regions. The doping of the source and drains can be done after the gate was grown (polysilicon gate served as source/drain doping mask), saving one lithographic mask step. This was possible as polysilicon (melting point 1410˚C) can withstand high temperatures necessary for the doping or high temperature activation (>800˚C) after ion implantation. Polysilicon gate could also be doped n-type or

p-type to adjust its workfunction catering for different threshold voltages in n-MOSFET or p-MOSFET.

Nowadays, the manufacturing equipments and processing of MOSFETs have matured into state of the art. The technology has progressively moved on from sub 130 nm nodes to sub 32 nm node. The lithography minimum feature size reduces by 0.7x every generation (every 3 years) [22]. To improve MOSFET's performance, the gate oxide has been continuously thinned down to below 20Å and new materials (high k dielectrics) are being explored such as hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) to increase capacitance without the oxide leakage. Si strain engineering using strained Si on relaxed SiGe are explored to increase channel mobility and increase the I_{DS}. Another trend is to explore on new MOSFET architecture such as the planar Ultra-Thin-Body MOSFET (UTB-MOSFET) which uses a 5 nm Silicon-On-Insulator (SOI) as a channel to reduce bulk resistance. Multi gate MOSFETs with 2 or more gates surrounding the channel provide better control of gate over the channel. One of these types of multi-gate MOSFET is the Fin-FET where the current flow parallel to Si wafer surface through a thin Si fin capped by gates on both sides of the fin [23,24].

The other class of non-classical MOSFET architecture is the Vertical MOSFET (VMOSFET) where the source, channel and drain are rotated 90˚ resulting in carriers flowing perpendicularly to Si wafer surface. This configuration does not depend on lithography to define the channel length. Instead the channel length is defined by the thickness of a grown layer or etching of the Si sidewall. The typical techniques used to fabricate VMOSFETs are insitu doped Si epitaxy, outdiffusion from doped layers into

vertically grown Si epitaxial layer or ion implantation on a spacer nitride/polysilicon protected etched Si sidewall.

There are two approaches in forming the Si channel of a VMOSFET. One is to grow the Si channel by epitaxy while the other is by etching the bulk Si wafer forming a mesa or Si sidewall. The growing of Si by epitaxy open up more possibilities of fabrication techniques. The npn configuration of the grown vertical Si channel can be done by insitu doping or outdiffusion from doped oxide multilayers of precise thickness. This method allow for precise control of the channel length and source/drain regions by controlling epitaxial growth rate and doped layer growth rate without being hindered by mask dimension or lithography limitations. As shown in Fig. 2.1, the Vertical Replacement Gate (VRG) n-MOSFET was fabricated by Hergenrother *et al.* [25] which featured gate length controlled by film thickness and self aligned source drain extension (SDE) formed by solid source diffusion (SSD), hence no ion implantation. The main feature of VRG process was to firstly grow a PSG/nitride/undoped sacrificial oxide layer/nitride/PSG stack. The thickness of the undoped sacrificial layer determines the channel length. A trench with vertical walls were etched into this stack. Then an insitu boron doped Si epitaxial process by Rapid Thermal Chemical Vapor Deposition (RTCVD) at 850˚C using dichlorosilane (DCS) and HCl was used to grow p-type single crystal Si into the trench. The doping of the channel by solid source diffusion occurred concurrently with the Si epitaxy process at 850˚C where dopants diffused out from the PSG. The extra Si cap on top was planarized by Chemical Mechanical Planarization (CMP) process. After CMP, polysilicon and nitride spacer was formed and the sacrificial

oxide was removed using buffered HF. Gate oxidation was done on the exposed Si followed by phosphorus doped amorphous Si deposition (later recrystallized) as the gate.

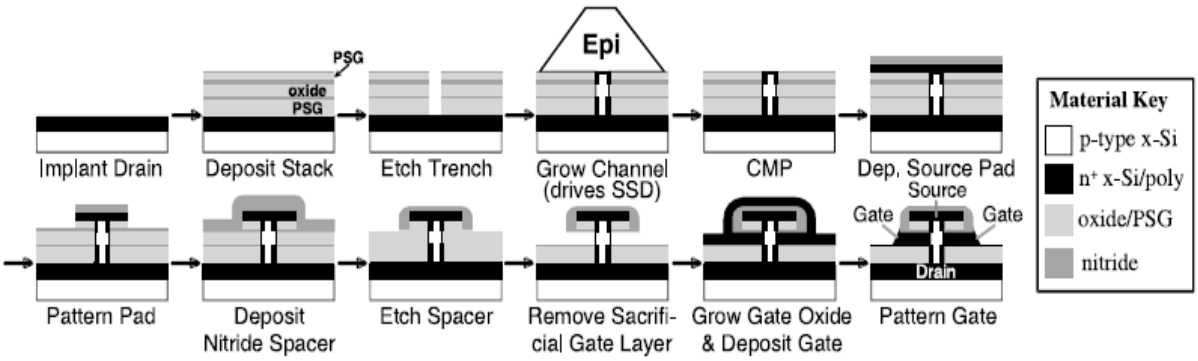

Fig. 2.1 Outline of Vertical Replacement Gate (VRG) n-MOSFET process flow. (Hergenrother *et al.* [25])

Risch *et al.* [26] utilized Si epitaxy by Low Pressure Chemical Vapor Deposition (LPCVD) at 900˚C with dichlorosilane, SiH_2Cl_2 (DCS) and insitu doped using diborane, B_2H_6 for p-type and arsine, AsH_3 for n-type Si. The source, channel and drain stack was grown in a single process step then etched prior to gate oxidation. In another work, Gossner *et al*. [27] used Molecular Beam Epitaxy (MBE) to grow a mesa with Si (111) sidewall at 470˚C and recrystallization at 625˚C at growth rate 0.1nm/sec at $2x10^{-9}$ mbar pressure. The thermally grown gate oxide 150Å (wet oxidation) at 700˚C had experienced low breakdown voltage of 4V. The breakdown was improved to 30V when a LPCVD Si_3N_4 layer was deposited on top of gate SiO_2.

One of the inherent problems in VMOSFET structure is the high overlap capacitance between gate and source/drain electrodes and the Si pillar plasma damage by dry etch process. This is circumvented by employing Fillet Local Oxidation (FILOX) that provides a thick oxide which reduces capacitance at source/drain regions and also

protects the Si pillar from dry etch damage [28]. A nitride spacer is first formed on the Si sidewall followed by thermal oxidation for thick oxide on source/drain regions and at the edges of the sidewall.

The second approach of creating Si channel of VMOSFET by Si etching a mesa or sidewall is depicted in Fig. 2.2. The attraction to this method is its simplicity where epitaxy process is not required. However, a method is required to cover the sidewall during doping the souce/drain region where spacer technique is commonly used to form sidewall spacers. This is achieved by polysilicon or nitride deposition followed by anisotropic dry etching. In a work done by Schulz *et al*. [29], tetraethylorthosilicate (TEOS) mask was used for dry etching the Si trench (Fig. 2.2). After the Si trench was formed, gate oxidation was done followed by an insitu doped n+ polysilicon deposition. The polysilicon gate was formed by spacer technique (anisotropic dry etch leaving polysilicon on sidewall edge). The polysilicon gate spacer then served as a self aligned implantation (arsenic) mask for the source/drain regions. The implantation was activated at 1050˚C for 10 seconds.

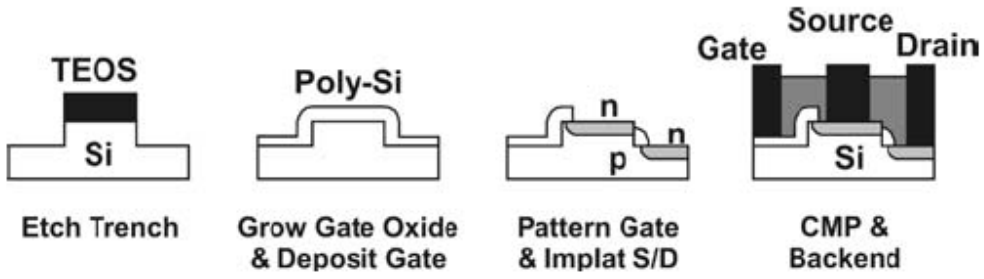

Fig. 2.2 Process flow for vertical sidewall MOSFET (Schulz *et al.* [29])

The etching of the Si sidewall by Reactive Ion Etching (RIE) which is a dry etch process is often followed by sacrificial oxidation where the SiO_2 is later removed to

reduce dry etch damage on the etched Si surface [28]. An alternative Si etching process that maintains anisotropy but without the etching damage could be the alkaline wet etchant, tetramethylammonium hydroxide (TMAH) [30]. Sacrificial oxidation is not required when etched by this method due to the smooth surface it produces.

2.4 MOSFET fabrication adaptation without ion implantation

In a lab environment that do not have access to technologies similar to the ones found in wafer foundries due to the high cost of resources (such as ion implanters) and safety issue concerns (use of silane for polysilicon deposition in chemical vapor deposition); different MOSFET fabrication methods need to be looked into. For hands on fabrication experience be made widely available to students (to support the growing Malaysia's front end processing electronics industry) and avoiding high cost becoming a deterrent to research, several techniques are used by researchers as alternatives for its fabrication.

Alternatives are sought for low cost photomasks in replacement of the more expensive chrome on glass masks. For this purpose emulsion photomasks can be used. Despite the economical solution, the masks would have limitations in the smallest feature size that can be printed depending on the resolution of printers. The photomasks are transparent films that can be printed on by laser printers or photosensitive plastic films exposed by higher resolution photoplotters. The emulsion photomasks allow for fast turnaround of design improvements by tests in the lab and new design in the AutoCAD

software. Morsin *et al*. [4] utilized AutoCAD 2002 to design 6 layer masks (alignment mark, source/drain PMOS, source/drain NMOS, gate, contact, metallization) for Complementary Metal Oxide Semiconductor (CMOS) MOSFETs and printed using Hewlett Packard Laser Printer. MOSFETs with channel lengths 300 µm, 400 µm and 500 µm were designed and successfully fabricated.

In the production wafer fab, registration and alignment has been converted to automation where alignment marks are automatically detected using bright field and darkfield optical detection systems [31,32]. In contrast, manual alignment is highly reliant on the operator's judgment, skill, emotions or physical deficiencies that affect the overall alignment work. Useful alignment marks are required to reduce and account for human error. Alignment mark in the form of cross in bars can be transferred to the first layer for subsequent layers to follow. Difficulties in manual alignment may result in repeated trials and rework of lithography process consuming resources and time [4]. This in part is contributed by the metal gate MOSFET process (in contrast to polysilicon gate) being used which does not allow self aligned source/drain doping. To ensure control of gate over the channel, the gate must overlap the source and drain regions. A requisite measure to address this problem is by incorporating an overlay tolerance, as done by Hashim *et al.* [5] where 80 µm gate oxide mask is overlayed on 50 µm source/drain separation allowing at least +/- 15µm tolerance to ensure the overlap. Another point to consider in mask design is that in lithography there is a pattern edge uncertainty arising from process variation attributed to over/under develop of photoresist or over/under etch of patterned layer. This can result in changing the initial pattern design or alignment mark itself, exacerbating overlaying work. As precaution, redundant alignment marks are made

or transferred at each layer in case of damage to the marks in subsequent processes. Another way is to anisotropically etch the alignment marks into the Si substrate. In this work, a controlled Si (111) sidewall (54˚ angle) with 3 µm etch depth will result in a consistent lateral sidewall edge width (2 µm) as added accuracy to the alignment scheme.

Techniques that can be used to fabricate dimensions smaller than defined by the photomask are subtractive technique or overexposure of photoresist experimented by Andhare *et al.* [33]. In order to reduce the channel length, through subtractive technique, the photoresist was exposed twice using the source/drain photomask. The first exposure used the original alignment and developed to obtain a channel length L1. This was followed by a second lithography process but with a controlled displacement of the wafer. After development the obtained channel length L2, is narrower than the original channel length L1. The other technique of photoresist overexposure involves increasing the UV exposure time until a desired narrower linewidth is obtained. The researcher was able to fabricate a 1 µm MOSFET using a 5 µm photomask utilizing this method [33]. Another possibility is by overdeveloping the photoresist (source/drain mask) to reduce channel length. Structure wise, changing the planar architecture into vertical structure (VMOSFET) by Si etching using TMAH will open possibility to define channel length by etching rather than depending on the photomask. However, in the absence of chemical vapor deposition (CVD), a controlled thickness by spacer technique to mask the Si sidewall during doping could not be emulated. Etching a Si (111) sidewall and benefitting its higher oxidation rate than planar Si (100) to grow a self aligned sidewall doping mask may be plausible to replace the spacer technique.

Without using ion implantation, other available doping methods include pulsed laser annealing (PLA), rapid thermal diffusion (RTD), and conventional thermal diffusion in the furnace. Pulsed laser annealing utilizes an excimer laser source with short wavelength (< 400μm) and pulse widths (< 200 ns) [34] in order to briefly melt both the dopant source (on Si) and the Si surface. The dopants diffuse in liquid state and are activated in Si once they solidify. This method is suitable for fabricating devices on substrates with low melting points such as glass and plastic or when high temperature processing is not permissible. It requires good control of laser fluence and beam profile.

Many applications in shallow junction MOSFET and Si solar cells employ rapid thermal diffusion (RTD) using spin on liquid dopant source (SOD) for the benefit of low thermal budget and enhancement of dopant diffusivity (activated by tungsten halogen lamp radiation) [35,36]. Diffusion processing in RTD using the spin on dopant (SOD) phosphorus employs temperatures ranging in 800˚C -950˚C for durations 2-120 seconds achieving sheet resistances of 40-140 Ω/ square. In MOSFET fabrication point of view, RTD would be useful when the channel length is scaled down requiring shallow junction depths that are hard to achieve by diffusion in furnace.

When shallow junction is not a priority the commonly used doping method is thermal diffusion in the furnace due to the theories and mechanism of dopant diffusivity in Si by this method is well established. However diffusion in the furnace requires higher temperatures (>900˚C) and longer diffusion time (minutes to hours) to achieve lower sheet resistances [35]. The diffusion furnace being reliable and easy to operate and maintain is widely used for work in the lab. Safe dopant sources are the solid source discs or spin on liquid dopant (SOD).

Gate oxidation is one of the critical processes in MOSFET fabrication. HCl is commonly mixed together with oxygen during dry oxidation to reduce defect density, stacking faults, mobile ion charges, interface state and improve dielectric breakdown [15]. Thermal dry oxidation with HCl is generally accepted to produce high quality and dense SiO_2. However, HCl is corrosive when mixed with moisture; damaging to the valving system of the furnace and harmful to people. Without HCl, there needs to be a different process treatment to improve gate oxide quality. One of the critical parameter determining oxide quality is its breakdown voltage. There are three regions of oxide breakdown modes. A-mode breakdown (dielectric strength $<1x10^6$ V/cm) is generally related to gross defects in the oxide, B-mode breakdown (dielectric strength $2\text{-}6x10^6$ V/cm) is tied to weak spots in the SiO_2, whereas higher dielectric strengths are associated to the C-mode (intrinsic breakdown) [37]. It has been reported that wet oxide is better than a dry oxide (without HCl) where the former exhibited better intrinsic breakdown [38] attributed to water related traps in the oxide that reduces high localized electric field which can lead to premature oxide breakdown. Murakami *et al*.,[39] reported on wet oxides having lower B-mode failure rates and higher B-mode breakdown fields compared to dry oxides. Generally the breakdown voltage increases with increasing oxide thickness and dielectric strength increases with decreasing oxide thickness [40]. Oxide breakdown voltage can be increased by appropriate oxidation conditions and appropriate subsequent annealing. Eric Ciantar *et al.* [41] noted that a dry/wet/dry oxide stack have a higher resistance towards electron injection, an improvement related to higher electron trapping.

To further improve the $Si\text{-}SiO_2$ interface, a hydrogenation process in forming gas anneal (10% H_2 + 90 % N_2) at the post metallization step anneal can be done. H_2 gas

however is explosive and poses a safety issue in the lab. A suggested alternative in this work is to enhance moisture level or increase hydroxyl groups (Si-OH) in the dry oxide by a dry/wet/dry oxidation sequence combined with a post metallization annealing (PMA) using Al as the gate. In the post metallization anneal (N_2 ambient at 450˚C), as Al react with hydroxyl in the SiO_2 forming Al_2O_3 layer at the interface, atomic H is released to react and passivate unsatisfied Si bonds at the Si-SiO_2 interface [14]

2.5 Summary

In this chapter MOSFET fabrication history has been reviewed encompassing developments in Si oxidation, passivation of Si surface, Si doping, diffusion masking and gate alignment methods. New trends in fabrication as the technology advances lead to new architectural structures as the Vertical MOSFET (VMOSFET) to increase packing density and not dependent on lithography to define its channel length. Adaptation of fabrication technology without ion implantation include low cost emulsion photomask, metal gate technology, doping by spin on dopant (SOD), dry/wet/dry oxidation and post Al metallization annealing as feasible techniques for MOSFET fabrication.

CHAPTER THREE

BASIC PROCESSES AND THEORY

3.1 Introduction

This chapter discusses on the basic processes used for Metal Oxide Semiconductor Field Effect Transistor (MOSFET) fabrication. The theories for p-n junction, MOS capacitor and MOSFET are also included.

3.2 Silicon as semiconductor of choice

Silicon (Si) is the most widely used semiconductor material in the integrated circuit fabrication since the 1960's until today. It is abundant in the earth's crust. Si is a group IV elemental semiconductor (having 4 valence electrons) with a diamond crystal structure. A Si atom is surrounded by 4 neighbouring Si atoms. Each neighbor shares 1 valence electron all together forming 4 covalent bonds that completes 8 valence electrons in outer shell for the center Si atom. The 4 neighbors form a tetrahedral structure as the basic building block of the diamond lattice. Si has a high melting point at 1415˚C. Its advantage lie in its high quality Si-SiO_2 interface unrivalled by other semiconductors' native oxide. This makes Si highly suitable for MOSFET high temperature processing with high quality gate insulator.

SiO_2 is easy to grow; in fact readily grown even at room temperature producing an oxide of about 25Å. It is chemically stable with high melting point at 1700˚C. The oxide could be used as insulator for gate oxide, masking against dopant diffusion and as