LOW POWER DESIGN TECHNIQUES AND ITS IMPLEMENTATION ON DIRECT MEMORY ACCESS (DMA)

By

SHABAGRAN A/L GANDI

Thesis submitted in fulfillment of the requirements
for the degree of
Masters of Science

August 2012

ACKNOWLEDGEMENT

First and foremost I offer my deepest gratitude to my supervisor, Mr. Zulfiqar Ali who has guided me throughout this research. It would be impossible for me to complete this thesis without his guidance and suggestions.

Next, I would like to thank my field supervisor from Intel Corporation, Dr. Suphachai Sutanthavibul. I truly appreciate his willingness to spend some of his time to guide me, despite of his busy schedule. I also would like to thank my manager Mr. Wong Chong Wai for being very supportive in order for me to complete this research.

Last but not least, I would like to thanks my family members and my colleagues for their extraordinary support which motivated me to complete this research.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ASIC:	Application Specific Integrated Chips
CMOS:	Complementary Metal-Oxide Semiconductor
CGE:	Clock Gating Efficiency
DRC:	Design Rule Check
EDA:	Electronic Design and Automation
ERC:	Electrical Rule Check
FGCG:	Fine-Grain Clock Gating
GCG:	Global Clock Gating
IC:	Integrated Circuit
ICG:	Integrated Clock Gating Cell
ITRS:	International Technology Roadmap for Semiconductors
LVS:	Layout versus Schematic
m-FGCG:	modified-Fine-Grain Clock Gating
MOSFET:	Metal-oxide semiconductor field effect transistor
RTL:	Register Transfer Level
SoC:	System-on-Chip
VLSI:	Very Large Scale Integration

LIST OF NOTATIONS AND SYMBOLS

C_L:	Load Capacitance
I_{SW}:	Switching Current
P_{DYN}:	Dynamic Power
P_{INT}:	Internal Power
P_{LEAK}:	Leakage Power
P_{SC}:	Short circuit Power
P_{SWI}:	Switching Power
P_{TOT}:	Total Power
V_{DD}:	Supply Voltage
V_{TH}:	Threshold Voltage

LIST OF PUBLICATIONS

S. Gandi, Z. Ali & S. Sutanthavibul (2011) Clock Gating Implementation on Direct Memory Access. *International Conference on Electronic, Networks, and Computer (ICENC)*. p.1 – 8.

S. Gandi, Z. Ali & S. Sutanthavibul (2011) Clock Gating Implementation on Direct Memory Access. *International Journal of Computer and Electrical Engineering (IJCEE)*.

TEKNIK REKABENTUK KUASA RENDAH DAN PELAKSANAANNYA PADA CAPAIAN INGATAN TERUS (DMA)

ABSTRAK

Bilangan transistor dalam SoC yang meningkat secara mendadak telah menyebabkan kerumitan integrasi turut meningkat pada masa yang sama. Selain kerumitan integrasi, pereka IC juga menghadapi beberapa cabaran termasuk untuk mengekalkan kuasa, prestasi dan keluasan IC. Antara cabaran-cabaran ini, pengekalan kuasa telah menjadi satu aspek yang mustahak yang perlu diperhatikan. Daripada meningkatkan kualiti pembungkusan untuk mengekalkan kuasa, sebaliknya, pereka IC mengamalkan teknik reka bentuk VLSI kuasa rendah untuk mengatasi isu ini. Secara umum, terdapat beberapa teknik reka bentuk kuasa rendah, termasuk penggetan jam, penggetan kuasa, voltan bekalan pelbagai dan sebagainya. Perbincangan dalam tesis ini akan berdasarkan teknik penggetan jam yang dilaksanakan pada capaian ingatan terus (DMA) untuk pengurangan kuasa dinamik. Daripada menggunakan teknik penggetan jam halus (FGCG) yang sedia ada, beberapa penggubahsuaian telah dilakukan pada litar ini dengan menggunakan isyarat set semula sebagai pin tambahan sebagai syarat tambahan untuk mengaktifkan isyarat jam pada litar dan ini dicadangkan sebagai ‘modified-FFCG’ (m-FGCG). Pendekatan bagi pengubahsuaian dan kaedah untuk mengenal pasti calon-calon penggetan jam yang bersesuaian juga telah dibincangkan dengan beberapa ilustrasi. Sebanyak 38% pengurangan kuasa dinamik telah dicapai dengan pelaksanaan teknik m-FGCG dan penggetan jam global (GCG). Satu lagi teknik iaitu penggetan jam saluran (CCG), yang khususnya untuk tujuh saluran dalam DMA telah dicadangkan juga. Kebiasaannya, semua isyarat jam pada setiap saluran DMA akan aktif sepanjang masa tanpa mengira ia digunakan atau tidak. Oleh itu, teknik CCG mempunyai

keupayaan untuk mengatasi masalah ini dengan menggetkan isyarat jam pada saluran yang tidak digunakan. Jika tiada sebarang saluran diperlukan, keseluruhan isyarat jam pada pengawal DMA (DMAC) akan digetkan dengan teknik CCG. Seperti teknik m-FGCG, teknik CCG ini juga bertujuan untuk mengurangkan kuasa dinamik pada DMA. Sebanyak 28% pengurangan kuasa dinamik diperoleh dengan pelaksanaan teknik CCG dan GCG secara serentak.

LOW POWER DESIGN TECHNIQUES AND ITS IMPLEMENTATION ON DIRECT MEMORY ACCESS (DMA)

ABSTRACT

As the number of transistors in a SoC has been increasing rapidly, the integration complexity has increased as well. Besides complexity, IC designers also faced some other challenges including maintaining the power, performance and area of an IC. Among these challenges, maintaining power has been an important aspect that needs attention. Instead of enhancing the packaging quality to preserve power consumption, IC designers practice low power design techniques for a VLSI design to overcome this issue. There are quite a number of low power design techniques including, clock gating, power gating, multi-supply voltage and others. In this thesis, the discussion will be based on the clock gating technique which is implemented on direct memory access (DMA) for dynamic power reduction. Instead of using the normal fine-grain clock gating (FGCG), some modifications have been done to the circuit by utilizing the reset signal as an additional enable pin to trigger the clock and this was proposed as modified-FGCG (m-FGCG). The modification approach and the method to identify appropriate clock gating candidates have been also discussed with some illustrations. 38% of dynamic power reduction has been achieved when m-FGCG is implemented with global clock gating (GCG). Another technique, channel clock gating (CCG) which is specifically for seven channels in DMA, has been proposed as well. By default, all the clock signals in each of the channel will toggle all the time irrespective, it is used or not. Hence, CCG technique has the ability to overcome this redundant event by gating the clock signals when the channel is not being used. If none of the channels are requested, the entire clock signal for the DMA controller (DMAC) will

be gated with CCG technique. As m-FGCG technique, this CCG technique is also meant for dynamic power reduction. A total of 28% of dynamic power reduction is gained by simultaneous implementation of CCG and GCG techniques.

CHAPTER 1

BACKGROUND

1.0 Introduction

This chapter one is the research background which gives a brief overview about the research and some information on the thesis content.

Section 1.0 is the introduction and Section 1.1 will be discussing about the VLSI theory. The theory of Moore's Law and introduction of DMA were also covered in this section.

Section 1.2 discusses about the research rationality that being a trigger to conduct this research. The discussion includes some power issues in VLSI design and brief explanation about the proposed design techniques. Furthermore, the reason for direct memory access to be chosen was included as well.

Section 1.3 will be discussing about the tasks that need to be done in this research. The discussion includes some information about the studies that have been done prior to this research. Besides, the implementation details were also included in this section.

Section 1.4 will provide the details of objectives that are expected to achieve from this research. This will also provide the main purpose of this research. The scope of this research is discussed in Section 1.5 and the last section, Section 1.6 will be providing the complete details of the contents in this thesis.

1.1 VLSI Technology

VLSI is a technology that integrates transistors into a chip for an application. Most of the electronic systems that being used in our daily life are generated from this VLSI technology. Evolution of VLSI technology can be seen through the innovation and rapid improvement of portable devices, such as, cellular and computers (W. Wolf, 2008).

The main driving factor for this VLSI technology evolution is the shrinking of the transistors' size. As the transistors' size shrink, the number of transistors in an integrated circuit (IC) increases as well.

In 1960s, Gordon Moore, the co-founder of Intel corporation has predicted that the number of transistors in a single chip would double every two years. This prediction is known as Moore's Law (W. Wolf, 2008; S. Rusu, 2001). Figure 1.1 shows the trend of transistors count based on Moore's Law.

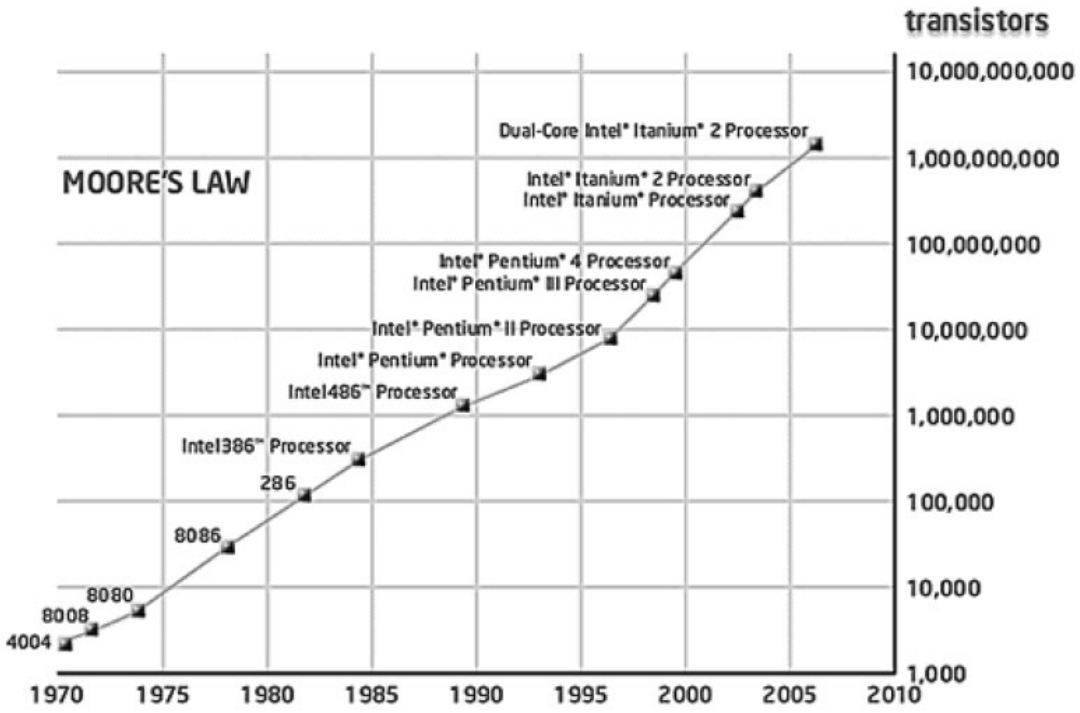

Figure 1.1 Trend of transistors' count based on Moore's Law (A. Heavey 2007)

On average, today's common ICs have billions of transistors (P. Zhao & Z. Wang, 2009). ICs here include Application Specific Integration Circuits (ASICs) and System on Chips (SoCs). SoC is a system that integrates numerous analog and digital designs onto a single chip. In other words, designs that were located separately in a computer are now in a single chip via SoC (D. White, 2003). Figure 1.2 shows an example of a SoC block diagram.

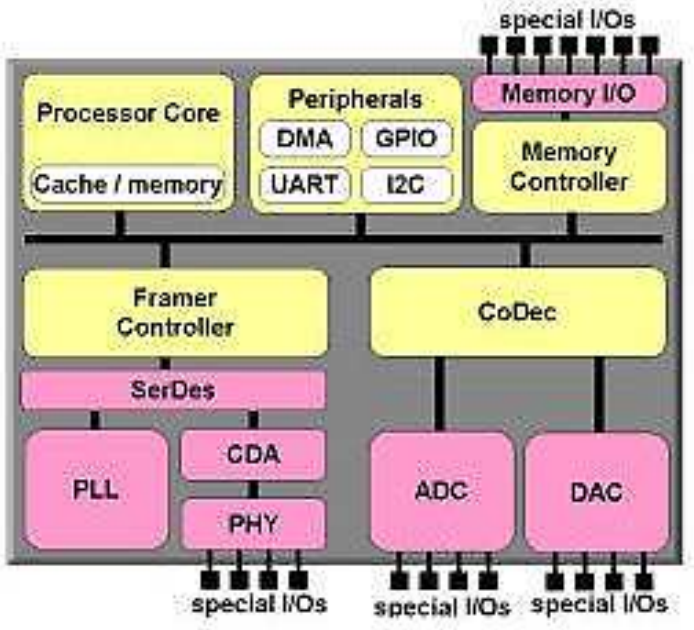

Figure 1.2 Block diagram of a SoC (Intellectual Properties (IP), 2009)

Direct memory access (DMA) is one of the common legacy designs that have been used in most of the digital design including SoC. DMA is one of the data transfer mechanism besides polling and interrupts (A.F. Harvey, 1994). All the data transfer in a computer or via its input or output (I/O) devices is operated at high speed (S. Ball, 2003; A.F. Harvey, 1994; Section 38. Direct Memory Access (DMA) (Part III), 2008).

DMA can be defined as a high speed data transfer mechanism which transfers data from one location to another without the intervention from central processing unit (CPU) (S. Ball, 2003; A.F. Harvey, 1994). The data transfer can be either from I/O devices to memory or vice versa. Under certain circumstances, the data transfer also occurs from memory to memory (Chapter 9 DMA, 1997; DMA, 1994).

For a DMA operation, the role of the CPU is to initiate the DMA transaction. Once the DMA has been initiated, then CPU will simultaneously perform other tasks or operation independently. Both CPU and DMA can operate simultaneously, but only one of them will be able to communicate with the memory (DMA Support in KMDF Drivers, 2007; TMS320VC5505/5504 DSP Direct Memory Access (DMA) Controller, 2009).

Since there will be only one address bus and one data bus, hence CPU and DMA has to take their turn to access the memory. This is the main reason for the CPU and DMA to operate independently. Figure 1.3 depicts a diagram that explains the orientation of CPU, DMA and memory together with the address and data buses. It can also be seen that either CPU or DMA can access the memory at a time (S. Ball, 2003). This is due to the availability of the data and address busses.

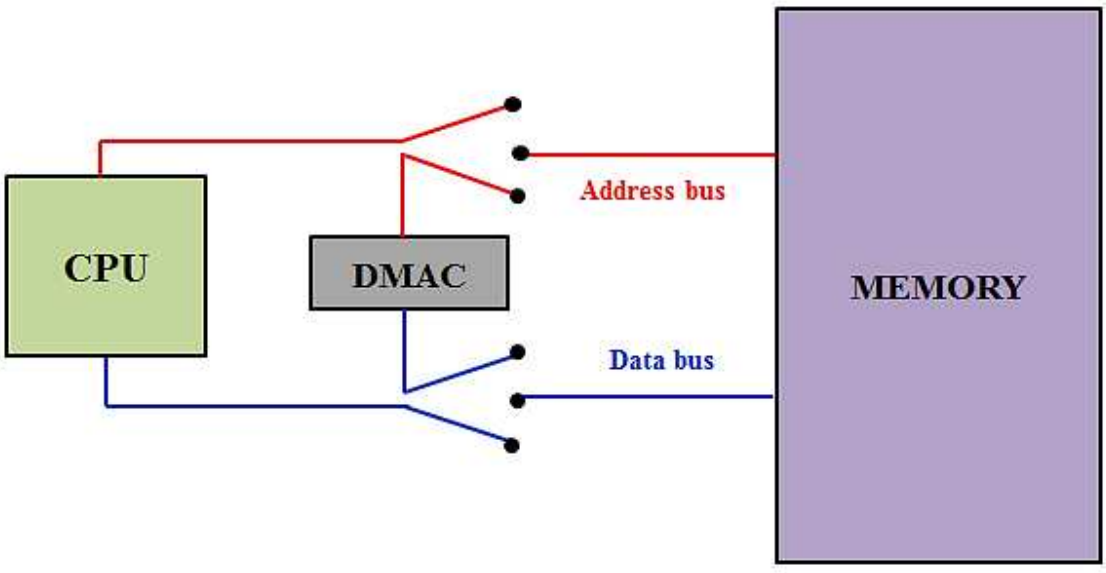

Figure 1.3 Data transfer via DMA

A very important characteristic of DMA is its ability to perform read and write operation. This means, DMA can be programmed either to write data into memory or read data from the memory.

The main advantage of DMA is its ability to perform data transfer in a fast manner. Operation of DMA is fast due to the presence of DMA controller (DMAC), which has a dedicated software to trigger the hardware to perform all the DMA data transfers (A.F. Harvey, 1994).

Besides that, the data transfer latency can be minimized via DMA. I/O devices can directly communicate to memory through DMA. This shows that, I/O devices does not need to depend on CPU for data transfer. And, this will reduce the transfer latency. Since both CPU and DMAC can operate simultaneously, the overall utilization of a computer system is maximized.

1.2 Research Rational

As discussed in previous section, the integration complexity in IC designs increases when more features and applications need to be mounted in the design (S. X. H. Jian, 2008). Besides integration complexity, the other main challenges that need to be faced by IC designers are to fairly maintain the power, performance, and area of the design (W. Wolf, 2008; S. X. H. Jian, 2008; J. Frenkil, 1997). Among these factors, uphold the power consumption has been a great challenge for IC designers (S. X. H. Jian, 2008; F.N. Najm, 1997).

Power has become a crucial factor to consider as more and more portable devices invented. Longer battery life is highly significant in order to make the portable devices to sustain more firmly in the market (S. X. H. Jian, 2008). In 2008, International Technology Roadmap for Semiconductors (ITRS) has listed that IC power consumption as one of the top three challenges faced by designers (P. Zhao & Z. Wang, 2009).

Figure 1.4 illustrates the trend of power consumption with respect to time. It can be concluded that currently, power is one of the major issues in IC design.

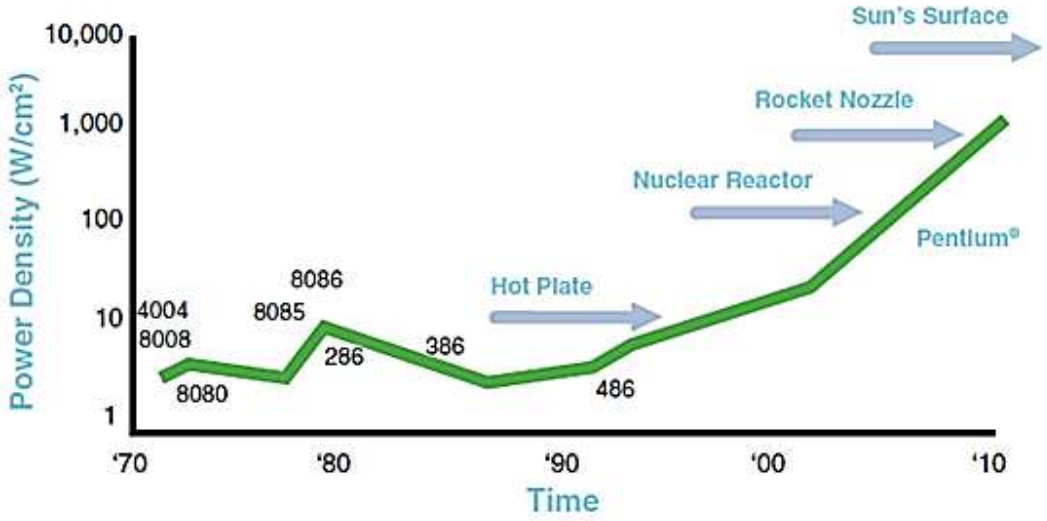

Figure 1.4 Chart of power density with respect to time (A Practical Guide to Low-Power Design, 2009)

The trend of power consumption without a low power design is shown in Figure 1.4. It reflects the importance of low power design practice in VLSI design. As a part of contribution to low power VLSI design, two low power design techniques have been proposed in this research.

The first proposed technique is very much similar to original clock gating technique. Instead of using the clock gating technique directly, modification has been done to it. The modification is about the utilization of the reset signal of a register as an additional enable pin to trigger the clock.

Figure 1.5 shows an example chart of chip power distribution. It can be seen that registers on clock tree consumes most power in a chip. This was the main reason to propose a technique that will be able to reduce the clock power. Besides, clock gating can be implemented through RTL modification and this is tally with the requirement of the proposed technique.

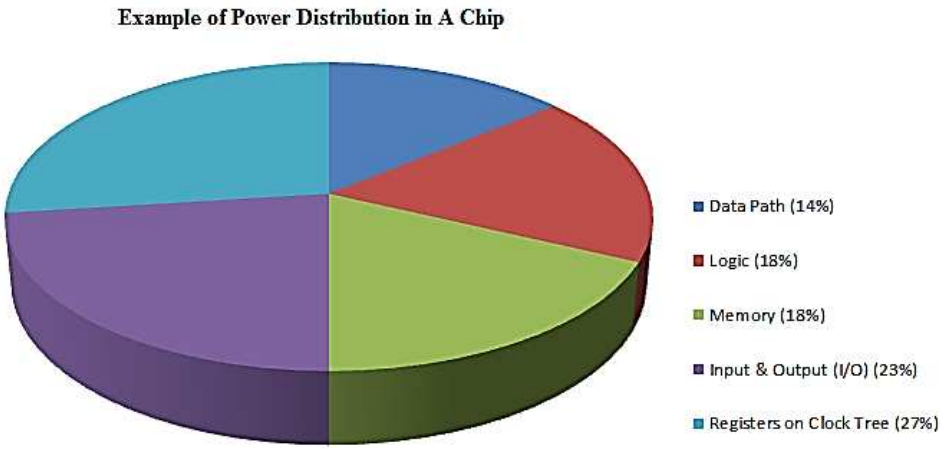

Figure 1.5 Chart of an example of power distribution in a chip (L. Chen et al., 2010)

After some studies, direct memory access (DMA) was finalized to justify the theory of the proposed design technique. The studies to select DMA include the number of registers and also the design size. The size of DMA which is moderate is suitable to test out the proposed technique.

Design size is an important factor to consider as an implementation may consume more time if the design is complex. Implementation time is vital because the technique has to be manually implemented at RTL level. All these criteria made DMA to be used as the test case.

The second proposed technique, channel clock gating (CCG), is a technique that closely tied with the architecture of DMA. DMAC has seven channels to perform the data transfer and, only one channel will be used at a time. This has been detected while implementing the first proposed technique.

The clock signal for each of the channels will be toggling continuously regardless the usage request. It can be considered as redundant if the clock signal toggles when it is not needed. Hence, this undesired toggling of clock signal motivates to propose the CCG technique which is specifically to overcome this event.

1.3 Tasks to Be Done

The research was initiated with some studies on VLSI technology and its challenges. Although there are quite a number of challenges, only power is focused in this research.

Since the implementation of the proposed techniques will be on DMA, the studies about DMA and low power design techniques is vital before begin the implementation. Studies on clock gating technique will be emphasized as the proposed techniques are based on the clock gating theory.

The main focus of this research is dynamic power reduction through proposed techniques implementation. And, the implementations of this research will be through manual modifications of RTL. EDA tools will be used for power estimation purposes.

1.4 Research Objectives

These are the primary objectives or goals that are desired to be achieved from this research. They are:-

i. To propose and implement a low power design technique called modified fine grain clock gating (m-FGCG) on DMA to achieve dynamic power reduction.

ii. To propose channel clock gating (CCG) technique and implement it to gate the clock signal of the DMA controller block and its seven channels. This will be specifically for the scenario when there is no request being made to it. Dynamic power reduction is expected to be achieved after this implementation.

iii. To implement global clock gating (GCG) technique together with the proposed techniques, m-FGCG and CCG, to identify the combination of techniques that can contribute the highest dynamic power reduction.

The major contribution that intends to be delivered from this research is the combination of proposed techniques that can achieve the highest dynamic power reduction.

1.5 Research Scope

This section will be discussing on how this research accomplished. Figure 1.6 illustrates the details about the scope of the research. This research is initiated with literature review.

Studies about low power design, clock gating, and architecture of DMA have been done for this literature review.

Stage 1 of this research is the implementation stage of GCG technique. The implementations of the proposed techniques, m-FGCG and CCG techniques will be done respectively in stage 2 and stage 3 of this research.

After the each of the techniques being implemented, the functionality of the DMA will be validated. The validation will be performed until the all the proposed techniques which implemented on DMA pass all the validation tests.

The stages shown in Figure 1.6 are not an actual order that needs to be obeyed as the GCG and the proposed techniques can be implemented in any order. The implementation order in this research is independent before results are collected.

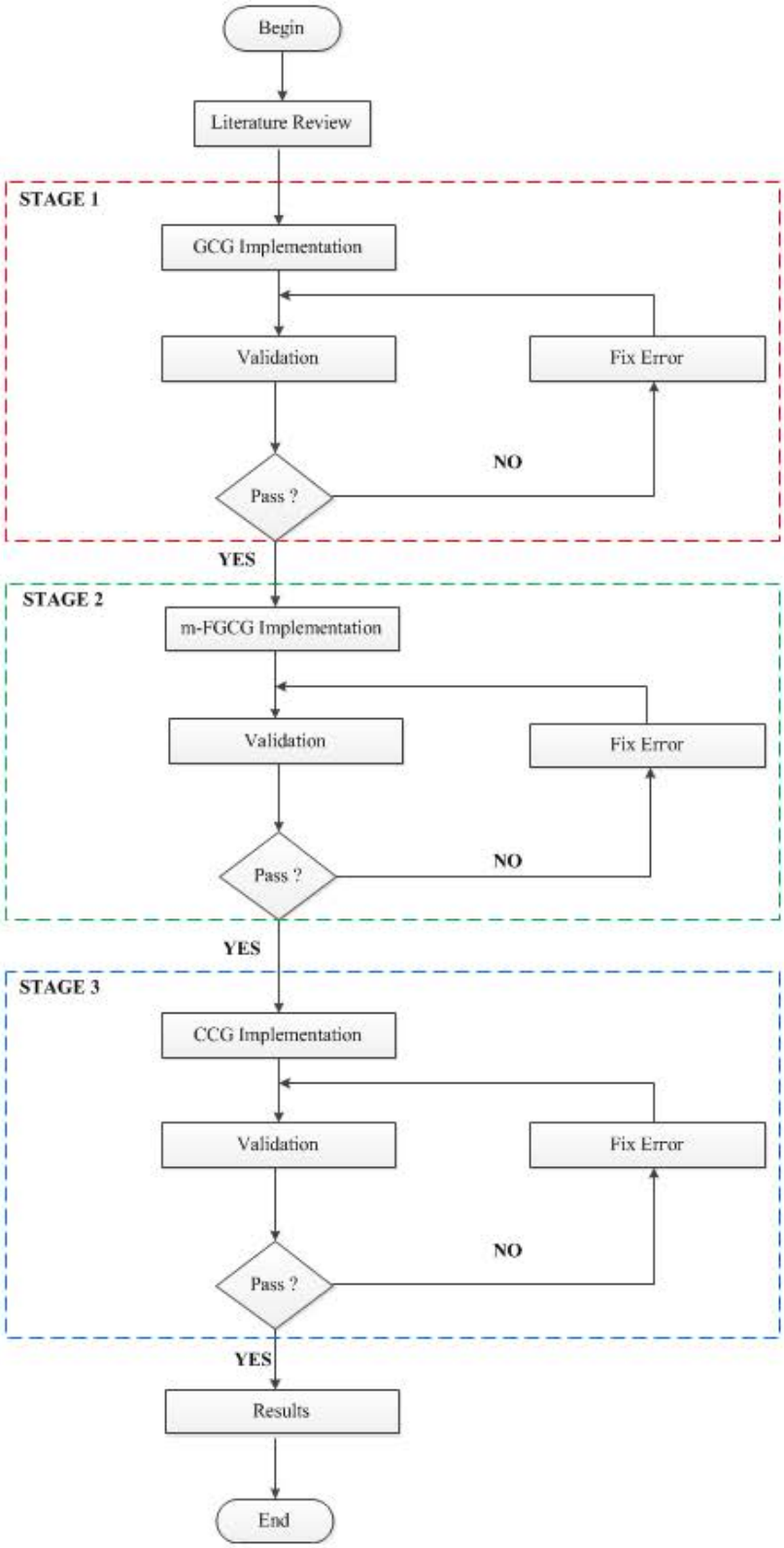

Figure 1.6 Flow chart to represent research scope

1.6 Thesis Organization

Chapter two is the discussion of the literature review which covers the related theories to this research. The theories include the power dissipation of CMOS in DMA. Each of the power components were discussed as well. Furthermore, the features of DMA were discussed as well.

Chapter three will be discussing about the methodology that was used to implement the proposed design. The background details of each of the proposed techniques were included in this chapter

Chapter four covers the discussion of the results that were obtained from the proposed techniques. The result factors that were focused were discussed as well. Some details about the clock gating efficiency were discussed. The general recommendations regarding the applicability of the proposed techniques and the validation strategy were also included in this chapter.

Chapter five is the complete conclusion that can be made from this research. Besides that, the future work that can be carried out as a subsequent from this research was included in this chapter as well.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

Chapter two will be discussing on the basic theories and concepts that are related to the research. This discussion is vital in order to give a brief overview of certain subjects including the operation of DMA.

Section 2.0 is the introduction of this chapter and followed by Section 2.1 which discusses about CMOS technology in DMA. Definition of CMOS and its technology in DMA will be discussed in this section.

The power dissipation of CMOS transistors in DMA will be discussed in Section 2.2. This section also has three additional subsections, 2.2.1 to 2.2.3 which will be respectively discussing about each of the power components.

Section 2.3 will be discussing about the low power VLSI design techniques. Several examples of techniques are mentioned in this section. The techniques are divided in two different groups.

Section 2.4 is the discussion of the dynamic power reduction techniques. The subsections 2.4.1 to 2.4.4 will be covering some detailed information of the dynamic power reduction techniques.

Conversely, Section 2.5 will be the discussion of the leakage power reduction techniques. Additional information about the leakage power reduction techniques were discussed in subsections 2.5.1 to 2.5.2.

Section 2.6 will be discussing about the features of DMA. There are three subsections under this section. Subsection 2.6.1 is the discussion about the DMA controller (DMAC) and channels. The discussion on this subsection will provide the information about the DMAC channels.

Subsection 2.6.2 and subsection 2.6.3 will be respectively discussing about the transfer types and transfer modes of DMA. In brief, the discussion on Section 2.6 is vital to understand more about the characteristics of the DMA.

2.1 CMOS Technology in DMA

The overview of the test case, DMA has been discussed in Section 1.1. It is also important to cover some detail information on how does the DMA is built. Almost all the digital designs, including DMA is built by using the complementary metal-oxide semiconductor (CMOS) transistors.

CMOS transistors are one of the important technologies in most of the IC designs. CMOS transistors are widely used due to its reliable characteristics including cost advantage as it is well-known as one of the low cost architecture (CMOS, The Ideal Logic Family, 1998; W. Maly, 1994).

The reason for the CMOS transistors are to be cost competitive is because of the small size. In addition to that, CMOS transistors are less complex for distribution of power supply (D. Money & N. H. E Weste, 2010; CMOS, The Ideal Logic Family, 1998).

CMOS technology is designed by using two types of MOSFET transistors, pMOS and nMOS. Figure 2.1 illustrates the building block and the corresponding circuit for both pMOS and nMOS respectively (D. Money & N. H. E Weste, 2010; J.M. Rabaey et al., 2003).

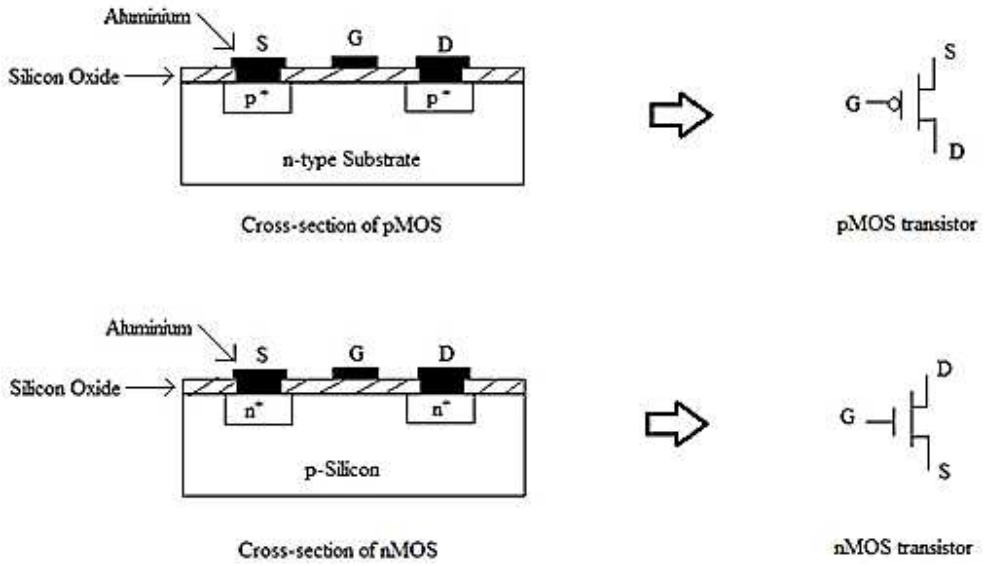

Figure 2.1: Cross section and circuit for pMOS and nMOS transistors (Mosfet Technology, 2010)

From the same figure, it can also be seen that both nMOS and pMOS has three terminals. The terminals are source, gate, drain and substrate (body). The main difference of these transistors is the configuration to enable them. nMOS transistors need high voltage to enable them and low voltage is needed to enable the pMOS transistors.

Both, pMOS and nMOS transistors will be the base circuits to construct all other logics including NAND, and NOR logics. CMOS inverter is the most basic logic which will be used to configure other logic gates.

The CMOS inverter circuit structure is made of the integration of one pMOS and one nMOS transistors. Figure 2.2 illustrates the CMOS inverter circuit (D. Money & N. H. E Weste, 2010; V.B. Zeghbroeck, 2011).

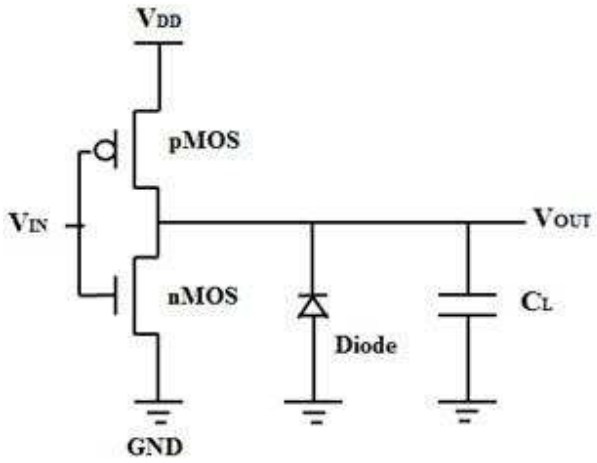

Figure 2.2: CMOS inverter

When an input, either high or low is fed to a CMOS inverter, either pMOS or nMOS will be enabled. For instance, when the input is high, based on the pull-up and pull-down theory, only nMOS transistor will be enabled therefore the load capacitance, C_L will be discharged and resulting the output to be low.

When the input is low, the pMOS will be enabled and the current from the V_{DD} supply, will flow to C_L. C_L will be charged and causing the output to be high (D. Money & N. H. E Weste, 2010; J.M. Rabaey et al., 2003; V.B. Zeghbroeck, 2011).

2.2 Power Dissipation of CMOS Transistors in DMA

Since the research is related to low power design techniques, it is vital to understand the power components that being dissipated in DMA. As discussed in previous section, most of the digital designs including DMA are built by CMOS transistors. Hence, by discussing the information of power dissipation in CMOS circuits, it will be the power dissipation of DMA as well.

The total power consumption in a CMOS circuit, $P_{TOT,}$ can be classified into two different categories, dynamic power (P_{DYN}) and leakage power (P_{LEAK}) (J. Frenkil, 1997; F.N. Najm, 1997). P_{DYN} is the summation of switching power (P_{SWI}) and short-circuit power (P_{SC}). P_{SC} is also known as internal power (P_{INT}). Equation 2.1 and 2.2 explains the mathematical expressions for total power dissipation in a CMOS circuit (P. Zhao & Z. Wang, 2009; S. X. H. Jian, 2008; Y. Zhi-guo & W. Jing-he, 2008; D.I. Lazorenko & A.A. Chemeris, 2006).

$$P_{TOT} = P_{LEAK} + P_{DYN} \tag{2.1}$$

Since, $P_{DYN} = P_{SWI} + P_{SC}$

therefore,
$$P_{TOT} = P_{LEAK} + (P_{SWI} + P_{SC}) \tag{2.2}$$

CMOS has two types of modes or states, active and idle. P_{DYN} is dissipated when it is in active state or operating state. P_{LEAK} is dissipated during the system in idle state. Although the circuit is in idle but there will be certain amount of P_{LEAK} dissipated (P. Zhao & Z. Wang, 2009; Y. Zhi-guo & W. Jing-he, 2008). Hence, these different states are the one causing the P_{TOT} to be the summation of P_{LEAK} and P_{DYN} (K. Usami, 2007; M. Keating et al., 2007). Further explanation for each of the power components are discussed in the following subsections.

2.2.1 Switching Power (P_{SWI})

P_{SWI} is dissipated due to charging and discharging activity of the output capacitance, C_L in a CMOS circuit (P. Zhao & Z. Wang, 2009; J. Frenkil, 1997). Figure 2.3 illustrates a CMOS circuit with its switching current flow, $I_{SW.}$

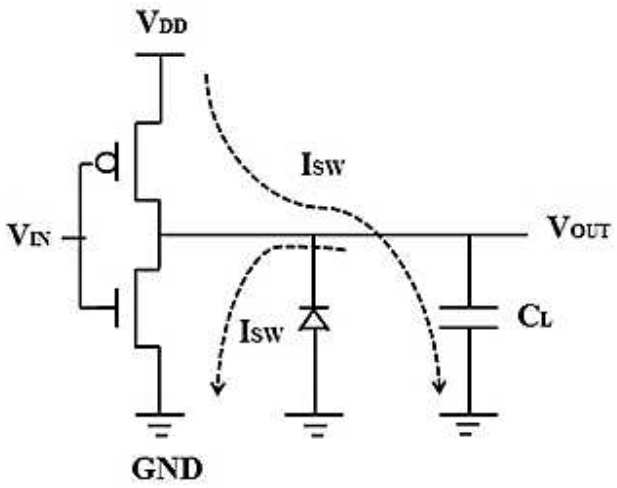

Figure 2.3: Switching currents flow

The dotted lines in Figure 2.3 show the flow of switching currents, Isw which contributes to P_{SWI} dissipation. The charging and discharging of the C_L is occurred due to the varying of

input values, either from high to low or vice versa. The charging and discharging activity of C_L have been discussed in Section 2.1 (P. Zhao & Z. Wang, 2009; J. Frenkil, 1997; P. Agrawal et al., 2007). Equation 2.3 represents the mathematical expression to compute $P_{SWI.}$

$$P_{SWI} = C_L \times (V_{DD})^2 \times f \times \alpha \quad (2.3)$$

where C_L is the output capacitance, V_{DD} is the supply voltage, f is the operating frequency and α is the switching activity. Switching activity is a data dependent function and it provides an average number on how many times the data toggling occur, either from high to low or vice versa.

2.2.2 Short-circuit Power (P_{SC})

As explained in Section 2.1, theoretically, only one of the CMOS transistors, either nMOS or pMOS will be enabled. This is under the ideal condition. But, in real design, there will be a short interval of time where both of the CMOS transistors will be enabled simultaneously (P. Zhao & Z. Wang, 2009; D.I. Lazorenko & A.A. Chemeris, 2006; J. Frenkil, 1997).

This event occurs when the input is in the middle of transition from high to low or vice versa. Figure 2.4 graphically explains the flow of I_{SC} when both the CMOS transistors are enabled.

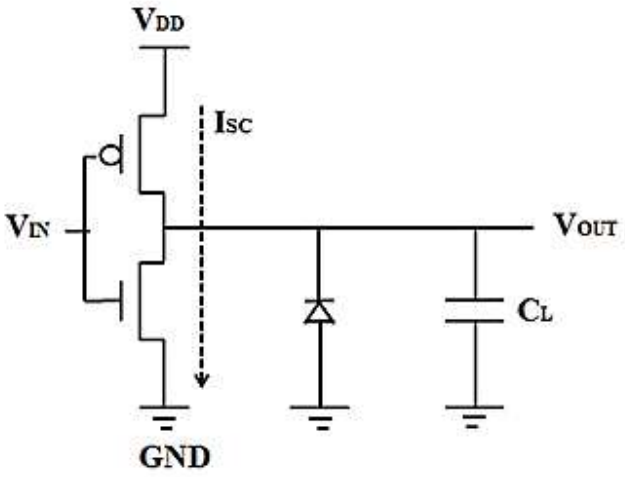

Figure 2.4: Short-circuit current flow

Although this event occurs only for very short interval, but it is important as it dissipates $P_{SC.}$ The mathematical expression for this P_{SC} is described in equation 2.4 below

$$P_{SC} = I_{SC} \times V_{DD} \tag{2.4}$$

where I_{SC} is the short-circuit current and V_{DD} is the supply voltage.

2.2.3 Leakage Power (P_{LEAK})

The two power components that were discussed in the previous sub-sections are the components of $P_{DYN.}$ As represented in equation 2.1, the other power component that contributes to P_{TOT} is $P_{LEAK.}$ P_{DYN} is dissipated only when a circuit is in active mode whereas P_{LEAK} dissipated all the time, including when a circuit is in idle state.

As the size of the transistors is getting smaller, P_{LEAK} dominates the total power consumption. This is being a biggest concern for IC designers to control the $P_{LEAK.}$ Chart in Figure 2.5 shows the trend of P_{LEAK} and P_{DYN} as the transistor size reduces.

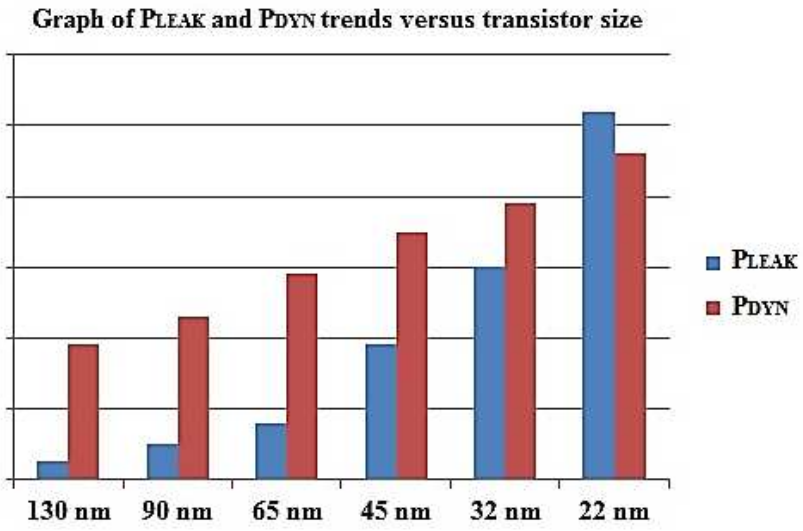

Figure 2.5: Trend of P_{LEAK} and P_{DYN} versus transistor size (A. Anand, 2012)

The mathematical expression for P_{LEAK} is shown in equation 2.5. The detailed expression is represented in equation 2.6

$$P_{LEAK} = I_{LEAK} \times V_{DD} \tag{2.5}$$

$$P_{LEAK} = (I_{SUB} + I_{GIDL} + I_{GOX} + I_{DREV}) \times V_{DD} \tag{2.6}$$

where I_{LEAK} is the leakage current, I_{SUB} is the sub-threshold leakage current, I_{GIDL} is the gate induced drain leakage current, I_{GOX} is the gate oxide leakage current, I_{DREV} is the diode reverse leakage current and V_{DD} is the supply voltage. Figure 2.6 illustrates the outline of CMOS circuit with all the leakage currents flow.

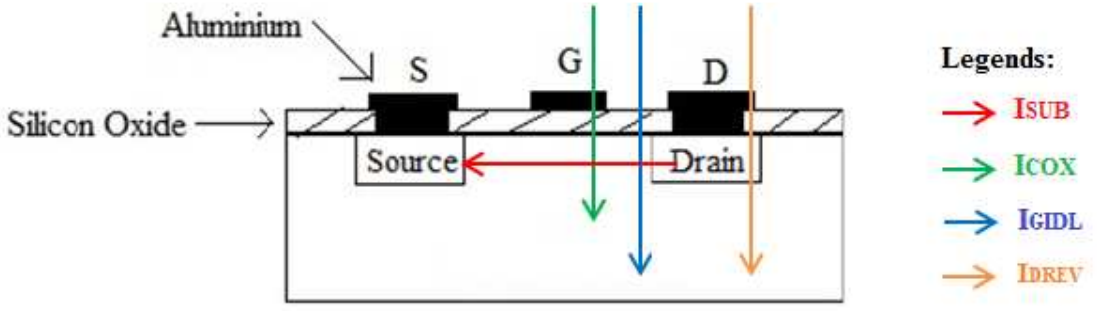

Figure 2.6: Leakage currents flow in CMOS

2.3 Low Power VLSI Design Techniques

The power issue in VLSI design has been discussed in previous chapter. In order to resolve the power issue, the packaging technology of an IC can be enhanced. However, due to cost, this might not be an efficient solution (J. Frenkil, 1997). Hence, designers tackle this power issue by using various low power design techniques at different design levels (P. Zhao & Z. Wang, 2009; S. X. H. Jian, 2008).

Table 2.1 summarizes some of the low power design technology at each design levels with their respective percentages of power reduction (P. Zhao & Z. Wang, 2009; D.I. Lazorenko & A.A. Chemeris, 2006). From Table 2.1, it can be seen that it is efficient to practice low power design techniques at the early stage of the design as it has higher opportunities for power savings.

These techniques can be further divided into two categories, dynamic power reduction techniques and leakage power reduction techniques. Figure 2.7 illustrates some of the low power

design technique according to its group. The details of these groups will be covered respectively in section 2.4 and section 2.5.

Table 2.1 Summary of Power Savings at each Design Level

	Design Levels	Low Power Technique	Power Savings (%)
1.	System Level	Dynamic Voltage Scaling	50-90
2.	RTL	Clock gating, operand isolation	30-50
3.	Gate Level	Technology mapping, gate resizing	20-30
4.	Circuit Level	Pass gate logic, transistor sizing	10-20

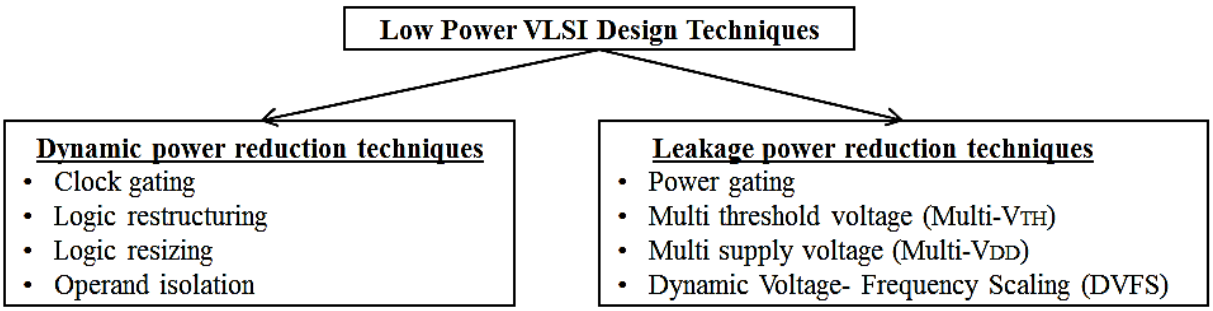

Figure 2.7: Examples of low power design techniques

2.4 Dynamic Power Reduction Techniques

2.4.1 Clock Gating

Clock gating is one of the typical low power design technique that has been used for most of the IC designs. Simple implementation and flexibility of this technique made clock gating to be a compulsory low power design technique to be implemented in most of the IC design (S. Huda et al., 2009; M. Saint-Laurent & A. Datta, 2010).