Performance improvement of MO surge arrester using high gradient arrester block against VFTOs

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***Abstract*— It is well known that the metal oxide surge arrester is inoperative against very fast transient overvoltages (VFTO) because of its strong stray capacitive effect. This stray effect causes a time lag between the peak of residual voltage and peak of the current surge and so there is a delay its response. In order to reduce the stray effect, high gradient material is used for preparing metal oxide arrester blocks with different compositions. For simulation study, the required electrical parameters of high gradient arrester blocks are calculated with estimated height of arrester. This model is simulated using Electromagnetic transient program (EMTP) for different arrester ratings against switching, lightning, steep and very fast transients. The simulated value of residual voltages are compared with experimental values. From the observed results, it is perceived that the newly developed high gradient arrester decreases the delay and so the dynamic performance of the arrester is improved especially against very fast transients.**

Keywords*— *very fast transient overvoltages, surge arrester, residual voltage, Electromagnetic transient program

I. INTRODUCTION

In contemporary years, the evolution of extra high voltage (EHV) and ultra-high voltage (UHV) transmission technology has been rapidly augmented across the world [1]. On account of this, the magnitude of VFTO vastly exceeding the standard lightning impulse withstand voltage (LIWV) for UHV systems, and it upsets the insulation of connected equipment, such as transformers, bushings, and secondary equipment because of the high rate of rise in voltage (dU/dt) [2]. Hence, the overvoltage phenomenon due to very fast transients become one of the life threatening factor of such equipment. Therefore, suppression of these surges becoming mandate to ensure the complete protection of power system.

It is a known fact that the metal oxide surge arresters have superior protection capability in power system network against surges, especially for switching and lightning. It encompasses of series connected ZnO blocks with respect to voltage rating, offers admirable V-I characteristics which warrant the protection of connected equipment. Therefore, for higher voltage rating, the height of arrester is more. This causes a higher stray capacitance effect which affects the successful operation of arrester especially during invading of nanosecond surges [3]. This is also supported by Valsalal et al. [4, 5] who described that the arrester may not be operated successfully since arrester capacitance plays an important role under very fast transients. This capacitive effect of the arrester block is not allowing the arrester to turn on from capacitive into resistive mode under VFTO [6, 7]. So, a time lag happens between the peak of residual voltage and current surge (current takes a peak before voltage peak). Therefore arrester takes a delay in its initial response to conduct against VFTO because of failure of successful transition of capacitive into the resistive mode. In order to accomplish successful conduction, the residual voltage must take a peak before the current peaks. This is possible with a notable reduction of stray capacitive effect. The most effectual way to decrease the stray capacitive effect is reducing the length of arrester column using high gradient material. With this context, two high gradient arrester blocks are developed and their dynamic behavior is compared with conventional arrester.

II. ANALYSIS OF CONVENTIONAL ARRESTER

The conventional surge arrester from the manufacturer (M1) is considered for the analysis. The collected rating, length and experimental value of the residual voltage of different ratings of surge arresters are given in Table 1.

TABLE I. MANUFACTURER DATA FOR CONVENTIONAL ARRESTER (M1)

Arrester rating	**Length of assembly (mm)**	**Residual voltage (kV)**		
		30/60µs, 2kA	**8/20µs, 10kA**	**1/10µs, 10kA**
132kV	1397	272	311	348
198kV	2105	408	466	520
330kV	3216	680	776	866

The cross-sectional view of arrester assembly consist of a series arrangement of ZnO blocks is shown in Figure 1 (a). The performance of arrester against surges highly depends on the microscopic formation of single ZnO grain and its boundary. With this in mind, the microscopic investigation of ZnO block is obtained using Scanning Electron Microscope (Tescan-Vega 3) after magnifying thousands of times and the observed image is shown in Figure 1 (c).

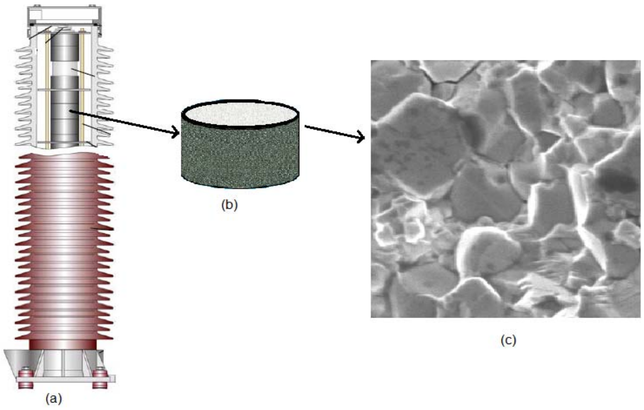


Figure 1 (a) Cross-sectional view of arrester assembly (b) Metal oxide block (c) Microscopic image of conventional arrester block (M1)

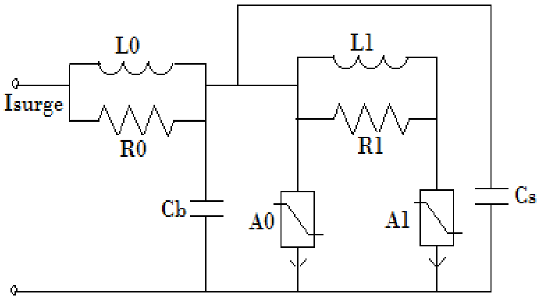


Figure 2 Modified IEEE arrester model for VFTO

From the surface image of conventional ZnO block, boundary formation between the grains is found greatly along with small spinal particles. The average grain size grows of the order of 12.53μm. This grain size decides the voltage gradient of the arrester block and is found to be 140V/mm. In order to study the dynamic behavior of conventional arrester against surges, simulation study is carried out by using the arrester model for VFTO.

A. *Arrester model*

The frequency dependent arrester model recommended by IEEE working group (WG) [8] is taken for this study. This model consists of two non-linear resistors separated by RL filter. For slow rising current surge, the impedance of RL filter is extremely low and so A0 and A1 are practically connected in parallel. While for a high rising time, the impedance of RL filter takes the significant role and A0 derives more current than A1. Since the capacitance of arrester plays a major role for very fast transient [6] and therefor block (Cb) and stray (Cs) capacitance are included in the IEEE WG model to analyze the arrester behavior especially under very fast transients as shown in Figure 2. The parameters of model such as R0, R1, L0 and L1 are computed based on the formula suggested by IEEE WG. The capacitances (Cb and Cs) are computed using finite element method (FEM) [3].

B. *Dynamic behavior against microsecond surges*

The model for VFTO is simulated for different ratings of conventional surge arrester (M1) for switching, lightning, and steep current surges. From the simulated waveforms, the residual voltage (Ur) and conduction time (tc-time taken to attain the peak of residual voltage) are observed and shown in Table 2.

TABLE II. SIMULATED UR AND TC FOR DIFFERENT ARRESTER RATINGS

Arrester Rating	30/60μs, 2kA		8/20μs, 10kA		1/10μs, 10kA	
	U_r (kV)	t_c (μs)	U_r (kV)	t_c (μs)	U_r (kV)	t_c (μs)
132kV	271.6	27.4	310.7	1.89	347.0	0.21
198kV	407.4	27.4	466.3	1.89	520.6	0.21
330kV	679.0	27.9	775.8	1.92	866.4	0.25

1) *Residual voltage (Ur)*

The voltage clamped across the arrester terminal during conduction of surge is known as residual voltage or clamping voltage. During invading of the surge, the voltage across each grain exceeds, breaks the potential barrier, and allows a current start to flow into ZnO grain. To accomplish a complete successful conduction of arrester during the surge, the potential breakdown takes place completely as early as possible to warrant the successful suppression of current surge. This operation is justified from the occurrence of the peak of residual voltage before current surge peaks. From Table 2, it is observed that the simulated values of residual voltages are well matched with manufacturer type test report (Table 1).

2) *Conduction time (tc)*

Surge arresters behave as capacitor during non-conduction mode [5]. While facing a surge, the capacitance must be wiped out as quickly as possible and turns the arrester into a resistive mode to conduct the surge successfully. Furthermore, time taken to diminish the capacitive effect must be less than the front time (tf) of the current surge to ensure the successful conduction of arrester. In this line, the time taken to reach the peak of residual voltage is called conduction time (tc). Table 2 shows the computed value of conduction time of 132kV rated arrester, in which the residual voltage attain a peak (tc = 27.40μs) prior to the current peak (30μs) during invading of switching surge. Likewise, same trends are observed during invading of lightning and steep current surges. This shows the successful operation of arrester during microsecond current surges.

C. *Dynamic behavior against nanosecond surges*

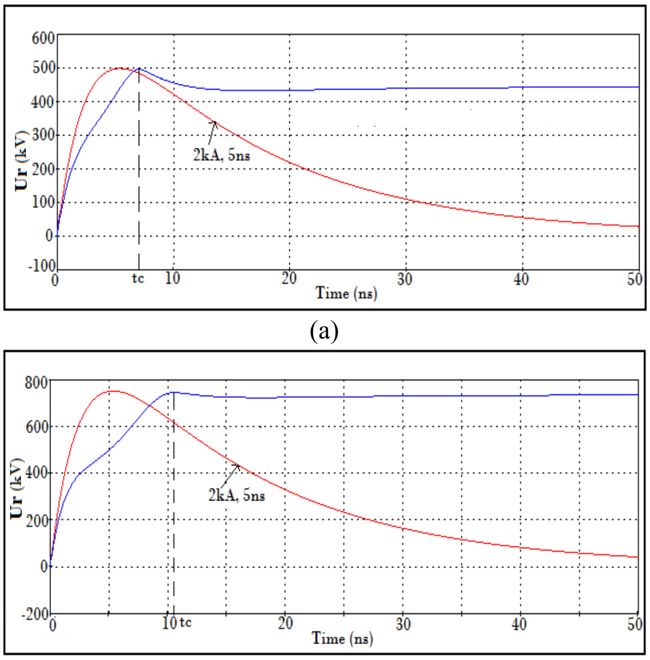
By contrast with the operation of arrester against microsecond surges, the dynamic behavior of arrester during invading of nanosecond surge is not yet given a clear vision on it. This fact throws a bad light on the successful arrester operation against all types of current surges, especially VFTO. To shows this, the simulation study is carried out with conventional arrester against nanosecond current surges.

A current surge of 2kA, 5ns is applied to 132kV, 198kV and 330kV rated conventional arresters. From the simulation, residual voltages and conduction times are observed and shown in Table 3. The 132kV rated arrester (M1) takes 6.015ns to break the potential barrier completely. On the other hand, current surge takes a peak in 5 ns and therefore arrester fails to conduct the surge. In other words, the occurrence of the peak of residual voltage is after the peak of the current surge. So there is a delay in its response (time lag) for successful conduction of arrester. Further increase of arrester rating, there is a rise in tc and so delay in its response is increased to 5.560ns for 330kV arrester (Figure 3).

Above all, it seems pertinent that the surge arresters are not operating successfully against nanosecond surges because of its capacitance effect. In light of this evidence, the stray capacitance must be reduced and this can be possible by using high gradient material causing a reduction in its height, resulting in the reduction of delay in its response.

TABLE III. UR AND TC OF ARRESTERS (M1) FOR 2KA, TF=5NS CURRENT SURGE

Arrester rating	**M1**		
	U_r(kV)	**t_c (ns)**	**t_d(ns)**
132kV	347.97	6.015	+1.015
198kV	494.55	6.990	+1.990
330kV	743.03	10.56	+5.560



(a)

(b)

Figure 3 Ur and current surge waveforms (a) 198kV (b) 330kV

III. SIGNIFICANCE OF HIGH GRADIENT ZNO ARRESTER BLOCK

Metal oxide arrester blocks are polycrystalline multicomponent ceramics comprise of ZnO with other minor additives namely Bi2O3, Sb2O3, Co2O3, Cr2O3, MnO2, etc [9]. The sintered disc denotes the voltage and current rating with their height and diameter respectively. Shingo Shirakawa et al. [10] stated that high gradient arrester block increases the reference voltages about twice or thrice and contribute a great compactness and better protection performance [11-17]. Consequently, the height of the arrester reduces greatly to attain a less stray capacitive effect [3]. The conceivable course of succeeding high gradient arrester is an amendment of material composition and its molarity, sintering process and advanced material processing.

IV. PREPARATION AND CHARACTERIZATION OF HIGH GRADIENT ARRESTER BLOCK

This work identifies two different arresters block (S1 and S2) with the new composition to accomplish high gradient arrester. For S1, the composition consists of ZnO with additives such as Bi2O3, Sb2O3, Co2O3, Cr2O3, MnO2, and Sc2O3. The rare earth element likely Scandium oxide tends to hinder the growth of ZnO grain during sintering along with antimony oxide. The powders are processed with a conventional method like ball milling, calcination, granulation, pressing, sintering, and grinding as shown in Figure 4.

Similarly, for S2, the same procedure is followed with different composition namely ZnO with additives such as Bi2O3, Sb2O3, Co2O3, Cr2O3, MnO2, V2O5, and Gd2O3. The addition of Vanadium oxide increases the density of the arrester block even at low temperature and Gadolinium oxide inhibits the grain growth during sintering because of strong pinning effect. The sintering temperature of both S1 and S2 are 1000°C. The behavior of developed blocks is compared with conventional arrester collected from the manufacturer (M1).

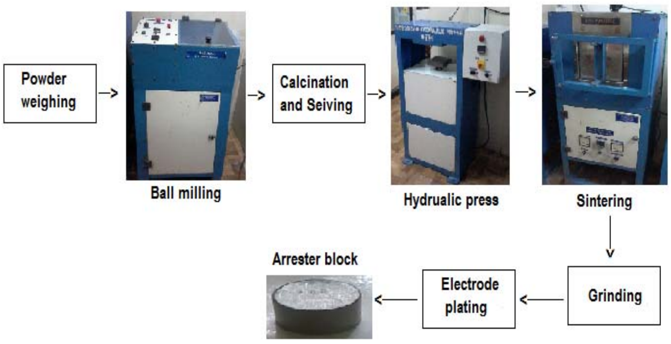


Figure 4 Production process of arrester blocks

A. *Microstructural properties*

The microstructural image of developed arrester blocks is observed and shown in Figure 5. From this image, the variations in grain sizes among the arrester blocks (S1 and S2) are observed and its average sizes are about 5.56µm and 4.96µm respectively. These values are much lesser than the conventional arrester and so attains a higher voltage gradient. From the DC test of both blocks, the voltage gradient of S1 and S2 are found to be 550V/mm and 605V/mm respectively.

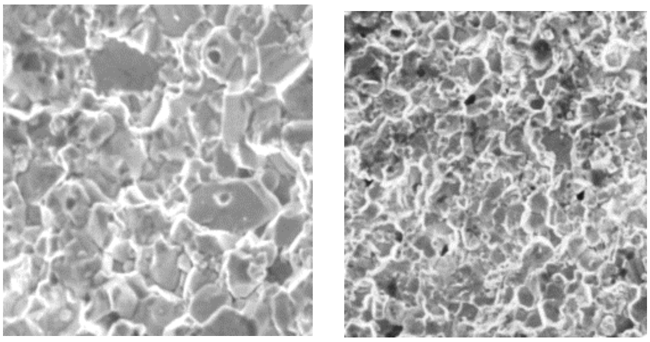

(a) (b)

Figure 5 SEM images of (a) S1 and (b) S2

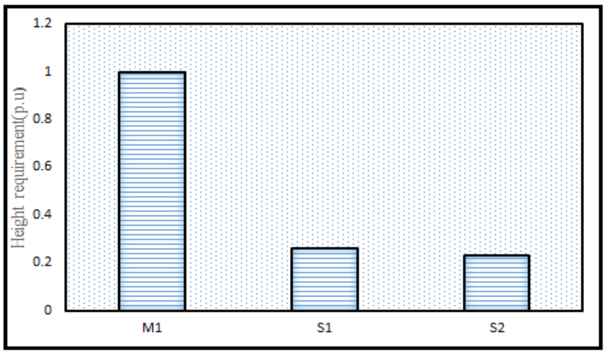


Figure 6 Comparison of required height in per unit

B. Reduction in height of arrester

The consequence of higher gradient arrester S1 and S2, compactness of arrester assembly can be achieved greatly. With the reference of the height of conventional arrester, the sample S1, and S2 concede a reduced assembly height of about 4-5 times because of its greater voltage gradient. The comparison between the conventional arrester and developed samples are shown in Figure 6.

Because of reduction in height of the developed arrester, the stray capacitance of the arrester assembly is reduced significantly. Consequently, the delay in its response may also reduce considerably. In other words, the transition speed from capacitive (non-conduction) to resistive mode (conduction) might be increased. This causes the time required to turn on the arrester against nanosecond surge may reduce greatly.

V. PERFORMANCE OF DEVELOPED ARRESTER AGAINST NANOSECOND SURGES

The electrical parameters of developed samples (S1 and S2) for VFTO model are computed with the estimated height of arrester assembly (132kV, 198kV, and 330kV). Subsequently, simulation is carried out by applying a nanosecond current surge (2kA, 5ns). From the waveform, the residual voltage, conduction time and delay time are computed and shown in Table 4.

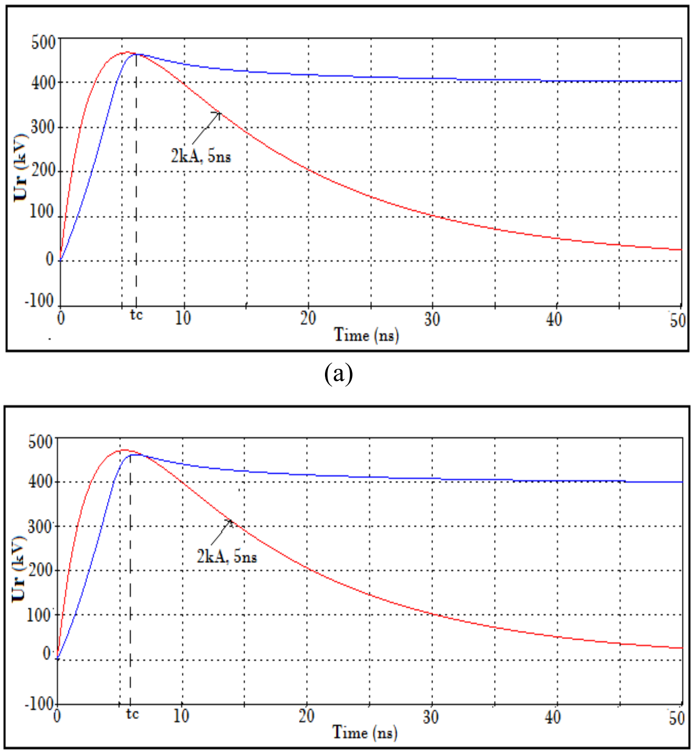
It is seen that there is a notable reduction in delay in its response of arresters (S1 and S2) compared with conventional arrester (M1). This is because of a decrease in stray capacitive effect. Owing to this, incoming surge with 2kA, 5ns charges the arrester (capacitive effect) quickly and subsequently breakdown of potential barrier happens quickly. Hence clamping of voltage takes a peak much faster than conventional arrester M1. Figure 7 and Figure 8 give the time lag (td) between the peak of residual voltage and current surge for 198kV and 330kVarresters respectively against 2kA, 5ns current surge. Summarizing the results of above, it is evidently shown that the high gradient arrester reduces the delay in arrester's response.

TABLE IV. UR AND TC OF S1 AND S2 FOR 2KA, TF=5NS SURGE CURRENT

Arrester rating	**S1**			**S2**		
	U_r(kV)	**t_c (ns)**	**t_d (ns)**	**U_r(kV)**	**t_c (ns)**	**t_d (ns)**
132kV	314.9	5.9	+0.9	314.0	5.91	+0.91
198kV	462.4	6.2	+1.2	461.0	6.20	+1.20
330kV	751.4	7.0	+2.0	749.4	6.97	+1.97

TABLE V. PERCENTAGE OF DECREASE IN DELAY

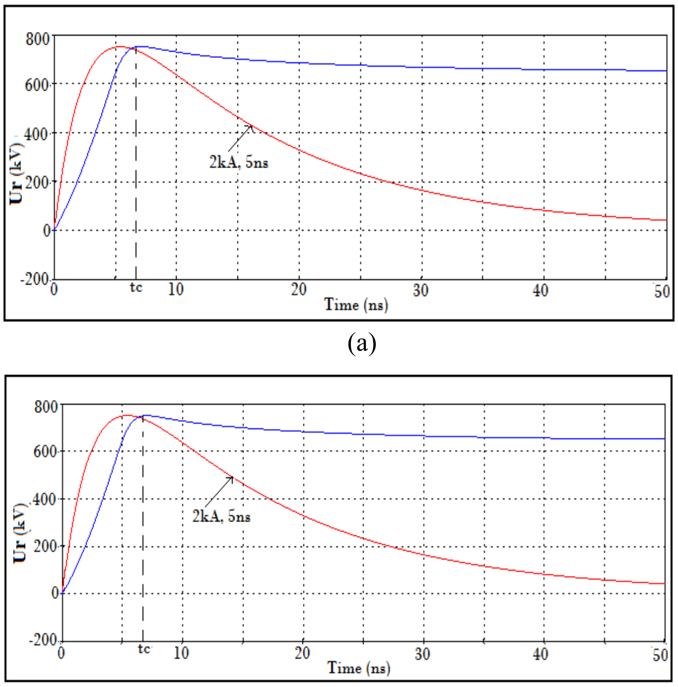
Arrester rating	**% Delay reduction**	
	S1	**S2**
132kV	10.68	11.53
198kV	62.31	65.69
330kV	73.48	80.94



(a)

(b)

Figure 7 U_r and current surge waveforms of 198kV arrester (a) S1and (b) S2



(a)

(b)

Figure 8. U_r and current surge waveforms of 330kV arrester (a) S1and (b) S2

VI. DISCUSSION

The dynamic behavior of conventional and developed arrester samples were studied against different surges. From this, it was perceived that the high gradient arrester block had a tendency to reduce the delay time for successful arrester operation against nanosecond surges. The percentage decrease in delay for S1 and S2 with respect to conventional arrester (M1) was computed as demonstrated in Table 5.

From Table 5, it is observed that the percentage delay for 132kV arrester is decreased by 11.53%. Similarly, for 198kV and 330kV arrester, delay percentages are condensed by 65.69% and 80.94% respectively. On paralleling both samples, S2 afford a better protection for VFTO applications because of its reduced percentage delay. In a nutshell, higher rated arrester with high gradient material consequences a total height requirement of arrseter as well as its stray capacitive effect. As a significance of this outcome, there is an improvement in its response which triggers the transition speed from capacitive to resistive mode of the arrester especially against VFTO.

VII. CONCLUSION

Applications of high gradient arrester blocks for different rating are studied and the same are compared with the performance of the conventional surge arrester using electromagnetic transient program (EMTP) under various current surges. It is found that the residual voltage of the high gradient arrester is less against VFTO over conventional arrester. Consequently, height requirement of high gradient arrester is reduced by 4-5 times compared with conventional arrester. Furthermore, transition delay from capacitive to resistive mode also reduced. The newly developed high gradient arrester (S2) decreases the transition delay by 11.53%, 65.69% and 80.94% for 132kV, 198kV and 330kV respectively and therefore transition speed of arrester is enhanced. All things considered, it is conclude that S2 could afford ample protection of power system against VFTO.

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