

Low-Power And High Performance Of An Optimized FinFET Based 8T SRAM Cell Design

Nurul Ezaila Alias
School of Electrical Engineering
Faculty of Engineering
Univeristi Teknologi Malaysia
81310 Johor, Malaysia
ezaila@fke.utm.my

Usman Ullah Sheikh
School of Electrical Engineering
Faculty of Engineering
Univeristi Teknologi Malaysia
81310 Johor, Malaysia
usman@fke.utm.my

Afiq Hamzah
School of Electrical Engineering
Faculty of Engineering
Univeristi Teknologi Malaysia
81310 Johor, Malaysia
mafiq@fke.utm.my

Munawar A. Riyadi
Department of Electrical Engineering
Diponegoro University
Semarang, Indonesia
munawar@elektro.undip.ac.id

Michael Loong Peng Tan
School of Electrical Engineering
Faculty of Engineering
Univeristi Teknologi Malaysia
81310 Johor, Malaysia
michael@fke.utm.my

Abstract—The development of the nanotechnology leads to the shrinking of the size of the transistors to nanometer region. However, there are a lot of challenges due to size scaling of the transistors such as short channel effects (SCEs) and threshold voltage roll-off issues. Fin-Type Field Effect Transistor (FinFET) is another alternative technology to solve the issues of the conventional MOSFET and increase the performance of the Static Random Access Memory (SRAM) circuit design. FinFET based SRAMs are faster and more reliable which are often used as memory cache for high speed operation. However, 6T SRAM cell suffers from access transistor sizing conflict resulting in a trade-off between read and write stability. This paper presents an investigation of the stability performance in retention, read and write mode of 22nm FinFET based 8T SRAM cell. The performance comparison of 22nm FinFET based 6T and 8T SRAMs were made. The simulation of the SRAM model are carried out in GTS Framework TCAD tool based on 22nm technology. In 8T SRAM cell, two n-FinFETs are added to the conventional 6T SRAM cell which will be controlled by the Read Word Line (RWL) to isolate the read and write operation path for better read stability. FinFET based 8T SRAM cell gives better performance in Static Noise Margin (SNM) and power consumption than 6T SRAM cells. The simulation results affirms the proposed FinFET based 8T SRAM improved read static noise margin by 166.67% and power consumption by 76.13% as compared to the FinFET based 6T SRAM.

Keywords—FinFET, SRAM, TCAD, Butterfly curve, SNM

I. INTRODUCTION

The miniaturization of the transistor through scaling process will affect the performance of the transistor. Meaning that the scaling of the transistor size becomes a challenge to maintain the leakage current, subthreshold conduction and reduce the short channel effects. Therefore, innovations or methods must have done in the transistor to save the future of Moore's law and generate the new performance. These new approaches include by designing new structure and introduce a new material for the transistor [1]. For example, the novel structures of the transistor are Triple Gate Transistor, Pi-FET, SiNW tri-gate, FinFET (Fin Field Effect Transistor), Triple Gate Transistor and GAA (Gate-all-around) can improve the performance of the devices in term of the lower power consumption and speed performance [2]. The

novel materials such as GaAs, high k-dielectric and strained silicon may enhance the performance of the devices that give a better gate control for transistor devices and reduce the short channel effect. Therefore, the FinFET structure is proposed to overcome the limitation of the conventional planar MOSFET and increase the performance of the device at nanometer region [3]. The design dimension and structure of the FinFET will determine its electrical performance and differentiate its performance from the conventional planar MOSFET. The parameters of FinFET that need to be considered are Fin thickness, oxide thickness, channel doping, Fin height and gate length. Static Random Access Memory (SRAM) hold the data as long as the power is provided. DRAM (Dynamic Random Access Memory) composed of a capacitor and a transistor in each memory cell for data storage function while SRAM consists of 6 transistors in its memory cell as shown in Figure 1.

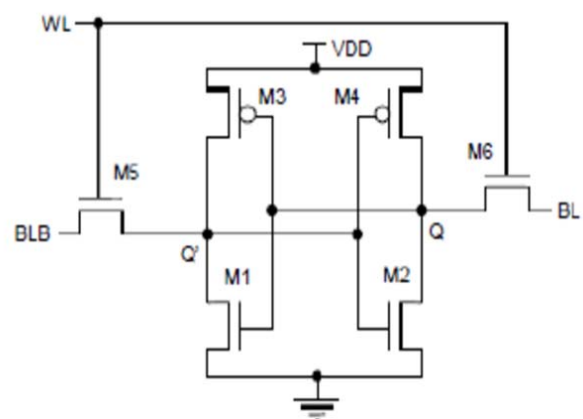


Fig. 1. The schematic of 6T SRAM cell

The cross couple of the 6T SRAM cell makes the performance of the SRAM faster than DRAM because refresh cycles did not exist in its operation. The area and stability of the SRAM cell are two important factors in the design of the SRAM cell [4]. The static noise margin (SNM) is one of the methods to determine the stability of the SRAM cell and measure the noise that exists in SRAM cell. There are three type of the operation that occurs in the SRAM cell which is retention mode, read mode and

write mode. The retention mode is the condition when the access transistor is disconnected from both bit lines and the logical '0' value of the word line. The read mode is the condition when the access transistors connected to both bit lines with pre-charged to V_{DD} and the logical '1' value of the word line. The write mode is the condition when one of the access transistors connects to the bit lines that connected to ground. However, the 6T SRAM cell scheme faces the degradation of performance during the read operation. Therefore, another topology of 8T SRAM cell is proposed to solve the destructive read problem that occurs in the conventional 6T SRAM cell by separating the read and write operation [5-8]. The storage nodes of the 6T SRAM cell are used to store the logical values '0' and '1'. During the read operation of the 6T SRAM cell, the word line turn on the access transistor and increase the output voltage of the inverter that store the logical values '0'. When the increased voltage turn on the pull-down transistor of the opposite inverter, the output voltage of the inverter that store logical values '1' will be reduced. However, when the output voltage decline below the threshold voltage of the transistor, it will destroy the read operation of the 6T SRAM cell. Besides, the external noise easily destructed and influence the stored data in the nodes of the 6T SRAM cell because of the direct path between storage nodes and bit lines.

The other important issues in SRAM cells are the power consumptions during read/write mode of operations [9-10]. There are two types of the power consumption in the SRAM cell which are static power and dynamic power also known as switching power. The total power of the SRAM cell is affected by the FinFET device structure itself, capacitance, supply voltage and switching activity. The static power is the power consumed when the SRAM cell is the inactive state. There is four dominant leakage current in the FinFET structure which are reverse biased junction leakage, subthreshold leakage current, gate-induced drain leakage and gate direct tunnelling leakage [11]. Thus, in this paper, FinFET-based 8T SRAM cell is proposed to solve the problem of the instability in read operation (RSNM) in 6T SRAM cell. The SNM in hold mode, read mode and write mode and power consumption were identified to determine the performance of FinFET based 8T SRAM cell. On top of that, in this work, the power consumption in 6T and 8T SRAM cells were estimated during read operation due to the dynamic power dissipation. Finally, their overall performances were compared and validated with the literature review.

II. METHODOLOGY

A. Device Structure of 22nm FinFET

The aims of this work are to design and simulate a 22nm n-channel and p-channel FinFET device using GTS framework software, to evaluate the electrical characteristic of the 22nm FinFET such as threshold voltage, V_{th} , I_{on}/I_{off} ratio, subthreshold swing and Drain Induced Barrier Lowering (DIBL).

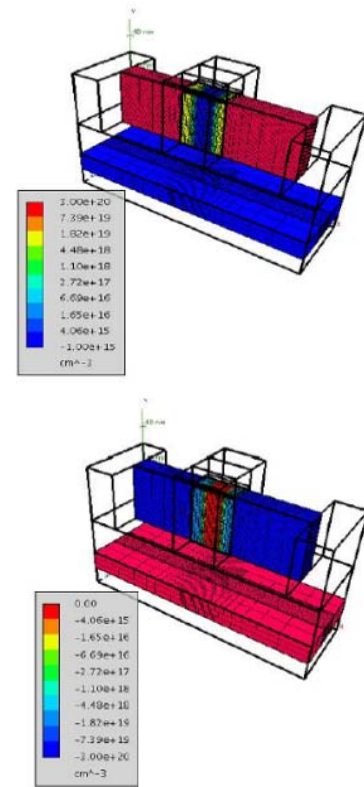


Fig. 2. Device structure of 22nm FinFET (top) n-channel (bottom) p-channel

TABLE I. THE DIMENSION OF FINFET DEVICE STRUCTURE

Device Parameter	Dimensions
Gate Length, L_g	22 nm
Oxide Thickness, t_{ox}	1.6 nm
Fin Depth	10 nm
Fin Thickness, T_{fin}	30 nm
Channel Doping, N_{ch}	$1 \times 10^{15} \text{ cm}^{-3}$

Then, to simulate a 22nm FinFET based 6T SRAM cell and 8T SRAM cell, compare and analyze their performances. The device structure of 22nm n-channel and p-channel FinFETs were simulated by GTS framework software as shown in Figure 2. Their device parameters are as listed in Table 1.

B. Design of FinFET Based Inverter

The inverter circuit was designed by using optimized device of 22nm n-channel and p-channel FinFET. The output characteristics of a FinFET based inverter are simulated. The voltage transfer characteristics (VTC) of the inverter were obtained. Next, the optimized FinFET based inverter were integrated in the design of the 6T SRAM cell circuit. The 6T SRAM cell consists of two inverter circuits plus additional two n-FinFET. Finally, the butterfly curve of the 6T SRAM cell are simulated and the performance of the 6T SRAM cell in retention mode, read mode and write mode were evaluated respectively. While, the 8T SRAM cell consists of 6T SRAM cell with two additional n- FinFET to separate the read operation. Figure 3 shows a FinFET based inverter in 3D structure.

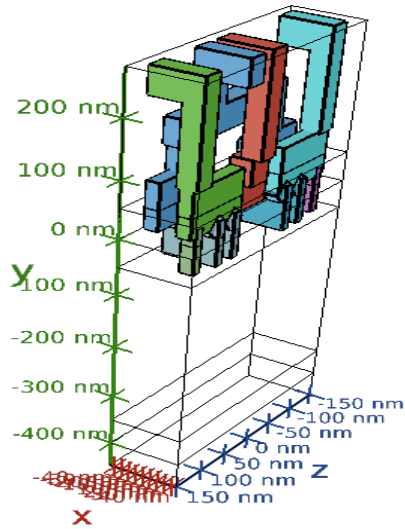


Fig. 3. FinFET based inverter in 3D structure

C. FinFET Based 6T and 8T SRAM cell

The 6T SRAM cell is constructed by two back to back connection of FinFET inverters and two n-channel access FinFET as shown in Figure 4. The data element stored in the Bit Line (BL) and Bit Line Bar (BLB), while the internal storage nodes of the SRAM cell represented by the output port of the two opposite inverters pair, Q and Qn. The FinFET configuration mode applies Low-Power (LP) FinFET mode in the design of the conventional 6T SRAM structure. The control signal, Word Line (WL) is used to control the on/off operation of the two pass transistors. The function of the turn-on WL is enabled, then, the 6T SRAM cell undergo either read operation or write operation.

Figure 5 illustrates the 8T SRAM circuit. There are two separate signals where the Write Word Line (WWL) and Read Word Line (RWL) are used to control the write mode and read mode of 8T SRAM cell respectively. An 8T SRAM configuration is proposed to enhance the read stability issue in 6T SRAM cell with the help of two additional n-FinFET (as in red dotted box) to isolate the read port of the 8T SRAM from the write bit lines.

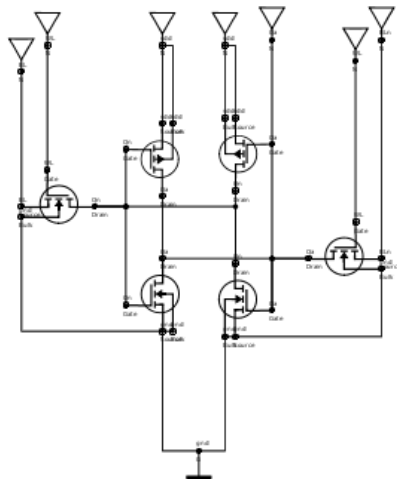


Fig. 4. FinFET based 6T SRAM cell.

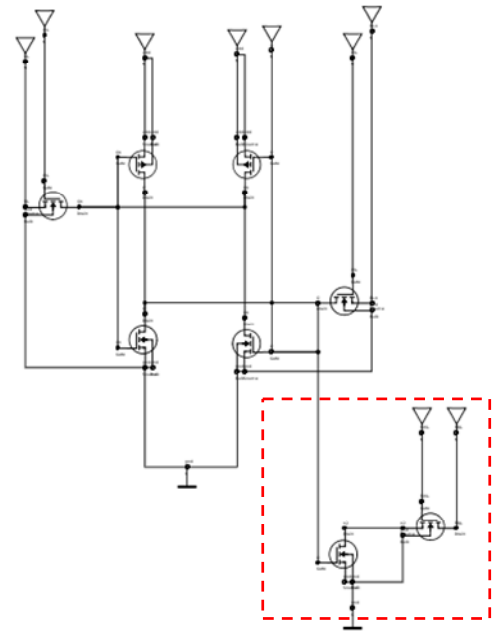


Fig. 5. FinFET based 8T SRAM cell. 2 additional transistors (red box) to develop an 8T cell.

III. RESULT AND DISCUSSION

A. Electrical Properties of 22nm FinFETs

The electrical properties of 22nm FinFETs for both p-channel and n-channel are shown in Table 2.

TABLE II. THE ELECTRICAL PROPERTIES OF N-CHANNEL AND P-CHANNEL 22NM FINFET

Type of device	n-channel		p-channel	
	V _{DS} (V)			
Electrical Properties	0.05	1.00	0.05	1.00
V _{th} (V)	0.34	0.19	0.27	0.12
I _{on} (×10 ⁻⁵ A)	3.06	6.26	1.35	3.69
I _{off} (×10 ⁻¹¹ A)	9.08	482	5.45	293
Ratio (×10 ⁵)	3.37	0.13	2.48	0.126
SS (mV/dec)	91.45	93.36	93.48	94.99
DIBL (mV/V)	148.76		155.88	

The typical value SS of the conventional n-MOSFET and p-MOSFET are 106.44 mV/dec and 135.94 mV/dec. When the length of the gate decrease to 22nm, the subthreshold swing of the n-channel FinFET and p-channel FinFET are degraded to 91.45mV/decade and 93.48mV/decade. Based on Table 2, the SS of the proposed FinFET devices approaches to the reference's SS which is less than 100mV/dec [3]. This proves that the proposed FinFET device has better control over the channel and hence improve in the power consumption due to low leakage current in the FinFET device as presented in Table 2.

B. Static Noise Margin (SNM) of 22nm FinFET based 6T SRAM

The performance of the 6T SRAM configuration in this work were analyzed through DC analysis. SNM is a type of the DC analysis to investigate the stability of the SRAM cell. The SNM is extracted graphically through the measuring the length side of the maximum square that can fit into the butterfly curve. From Figure 6(a), the SNM of the 6T SRAM cell is 400mV. The value is better than the others work [5], [7], [8]. It verifies that FinFET based 6T SRAM has higher ability to retain stable data during standby mode operation. The WSNM is a metric that obtains the writing stability of the 6T SRAM cell. Figure 6(b) represents the extraction of WSNM which is about 550mV.

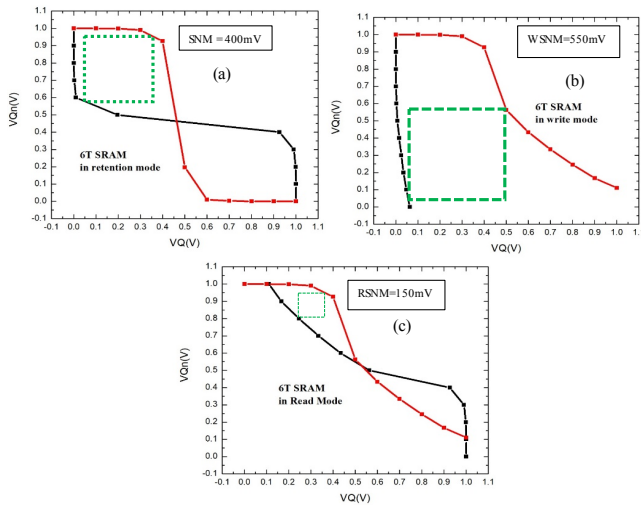


Fig. 6. SNMs of FinFET based 6T SRAM cell for (a) retention (b) write and (c) read mode

The RSNM can be obtained from the butterfly curve when the condition of the access transistors turns on and both bit lines are pre-charged to V_{DD} . RSNM is a measurement that determines the read stability of the 6T SRAM cell. In other words, the RSNM is the metric that measures how the SRAM cell itself maintain its stable state in the presence of pre-charged voltage bit line. Due to the voltage dividing effect through the drive transistor and the access transistor, the zero voltage at the storage node of 6T SRAM cell gets increase across the pass transistor results degrade in the RSNM. The RSNM during the read operation of the proposed work is about 150mV as obtainable in Figure 6(c).

C. Static Noise Margin (SNM) of 22nm FinFET based 8T SRAM

From the simulation result, the SNM during retention and write modes of the 8T SRAM topology is similar to 6T SRAM topology which is about 400 mV and 550mV, respectively. An 8T SRAM topology was proposed to address the problem of reading storage destruction that occurs in the 6T SRAM cell. During the read operation, both bit line is pre-charged to V_{DD} . However, the read operation of 8T SRAM only executed when the Word line (WWL) has no accesses the pass transistor to disable the flow of the in/out data of the internal storage port of the 8T SRAM cell. There is no connection between the

reading path and internal storage port of the 8T SRAM cell due to the isolation of the data output element and data retention element. Hence, the proposed 8T SRAM offers a free disturb read operation and then yield a non-destructive read operation. During the read operation, BL, BLB, WL set to low, RBL will be pre-charged to V_{DD} and at the same time the RWL is set to high to turn ON the access transistor. From the result, it indicates that the proposed FinFET based 8T SRAM has higher stability during the read mode with about 400mV as shown in Figure 7. Figure 7 shows the butterfly curve's comparison between 6T and 8T SRAM cells.

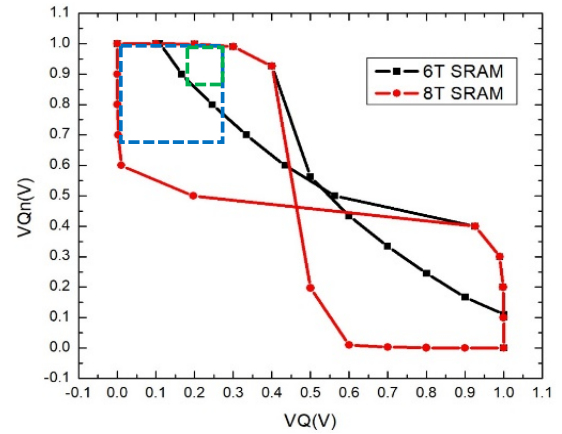


Fig. 7. SNMs of proposed 22nm FinFET based 8T SRAM cell. Comparison between 6T and 8T SRAM cells

From the comparison, 8T SRAM cell shows better read stability compared to 6T SRAM cell. There is no difference in SNM and WSNM except significant improvement in the RSNM for 8T SRAM cell. The isolated two access n-FinFETs act as the read operation causes 166.67% improvement in RSNM. The stability of the read operation in 8T SRAM configuration enhanced due to there is no discharging path from reading Bit Line to ground.

Table 3 shows the summary of the comparison between proposed work and others' work in terms of SNM, RSNM, WSNM and power consumption. From the comparison, it shows the proposed 22nm FinFET based 6T and 8T SRAM cells have better stability and less power consumption than the previous works.

TABLE III. PERFORMANCE COMPARISON OF THE PROPOSED WORK AND OTHERS

SRAM Cell	6T			Power Con. (pW)	8T			Power Con. (pW)
	Noise Margin (mV)				Noise Margin (mV)			
	SNM	RSNM	WSNM		SNM	RSNM	WSNM	
[6] 32nm	172	125	-	1.36	220	181	-	0.68
[7] 24nm	-	223	278	0.72	-	375	210	0.53
[8] 16nm	-	65	219	-	-	262	274	-
Prop. work 22nm	400	150	550	1.16	400	400	550	1.16

As in this Table 3, the major contribution of the proposed work is the static noise margin during read operation is greatly improved in FinFET based 8T SRAM cell. Besides, the power consumption of the previous works have not been reported. However, in this work, the power consumption during read mode is presented and shows the least power is consumed with only 1.16pW to obtain the maximum read stability of 400mV for FinFET based 8T SRAM cell.

IV. CONCLUSION

As a conclusion, FinFET is another alternative solution to solve the obstacles and challenges that occur in the conventional planar MOSFET beyond 22nm technology. The electrical properties of the n-channel and p-channel of 22nm FinFET have been carried out, successfully designed and simulated by using GTS TCAD Framework tools. The Different mode of the operation of the 6T and 8T SRAM cell have been compared. The proposed FinFET based 8T SRAM cell shows better RSNM than conventional 6T SRAM cell. The 8T SRAM configuration is outperformed by obtaining larger RSNM with 166.67% improvement as compared to 6T SRAM cell due to the isolation of the read path from the storage node. In read mode, the read power consumption of 8T SRAM cell is greatly dropped by 76.13% as compared to 6T SRAM cell. It can be concluded that the proposed FinFET based 8T SRAM cell show significant improvement in its performance with better stability and low power consumption in read operation mode.

ACKNOWLEDGMENT

Authors would like to acknowledge the financial support of the Ministry of Higher Education (MOHE), Malaysia under the Research University Grant (GUP) Project No. Q.J130000.2651.16J19. Also thanks to the Research Management Center (RMC) of Universiti Teknologi Malaysia (UTM) for providing an excellent research environment in which to complete this work.

REFERENCES

- [1] Lidow, A. (2011). Is it the End of the Road for Silicon in Power Conversion? IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp. 1-6.
- [2] Ho, B. (2012). Evolutionary MOSFET Structure and Channel Design for Nanoscale CMOS Technology, University of California.
- [3] Lourts Deepak A and Likhitha Dhulipalla, A. B et al. (2013). Performance Comparison of CMOS and FinFET based SRAM for 22nm Technology. International Journal of Conceptions on Electronics and Communication Engineering, 1(1), 6-10.
- [4] Chang Y. J., Lai F., Yang C. L. (2004). Zero-Aware Asymmetric SRAM Cell for Reducing Cache Power in Writing Zero. IEEE Transactions on Very Large Scale Integration Systems, 12(8), 827-836.
- [5] Wei Lim, A. B et al. (2014). Performance Evaluation of 14 nm FinFET-Based 6T SRAM Cell Functionality for DC and Transient Circuit Analysis. Journal of Nanomaterials, pp. 1-8.
- [6] Young Bok Kim, Yong-Bin Kim and Lombardi, F. (2008). Low power 8T SRAM using 32nm independent gate FinFET technology. IEEE International SOC Conference, pp. 247-250.
- [7] Farkhani, H., Peiravi, A., Kargaard, J. and Moradi, F. (2014). Comparative study of FinFETs versus 22nm bulk CMOS technologies: SRAM design perspective. 27th IEEE International System-on-Chip Conference (SOCC), pp. 449-454.
- [8] Monica M., Chandramohan P. (2008). A Novel 8T SRAM Cell using 16nm FinFET Technology. RUAS-SASTech Journal, 1(1), 5-8.
- [9] Arash A-M., Mohammad T. M. S., Hamid B. and Ali B. (2008). Delay and Energy Consumption Analysis of Conventional SRAM. International Journal of Electronics, Circuits and Systems. 2(1), 35-39.
- [10] Medha Chhillar, Geeta Yadav, and Neeraj Kr. Shukla. (2013). Average and Static Power Analysis of a 6T and 7T SRAM Bit-Cell at 180nm, 90nm, and 45nm CMOS Technology for a High Speed SRAMs. Proc. in Int. Conf. on Advances in Electrical & Electronics, pp. 75-79.
- [11] Himanshu Asija, Vikas Nehra, Pawan Kumar Dahiya. (2015). Leakage Power Reduction Technique In Cmos Circuit: A State-Of-The-Art Review. IOSR Journal of VLSI and Signal Processing, 5(4). Ver. I, 31-36.