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Arquiteturas Paralelas Avançadas para Transmissores 5G Totalmente Digitais

Advanced Parallel Architectures for 5G All-Digital Transmitters

MAP tele DOCTORAL PROGRAMME IN TELECOMMUNICATIONS

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Advanced Parallel Architectures for 5G All-Digital Transmitters

Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Telecomunicações, realizada sob a orientação científica do Prof. Doutor Arnaldo Silva Rodrigues de Oliveira, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e do Prof. Doutor José Manuel Neto Vieira, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Palavras-Chave

Transmissores RF Totalmente Digitais, Arquiteturas de Transmissão Reconfiguráveis, Rádios Definidos por Software, FPGA, Modulação Delta-Sigma, Modulação por Largura de Pulso

Resumo

A quinta geração de comunicações móveis (5G) está a ser preparada e deve ser comercializada nos próximos anos. Algumas das características inovadoras esperadas passam pelo uso de um número massivo de *font-ends* de Rádio-Frequência (RF), taxas de pico de transmissão de dados de 10 Gbps (em todos os lugares e em todas as ocasiões), latências inferiores a 10 mseg e elevadas densidades de dispositivos. Ao mesmo tempo, as gerações anteriores não podem ser ignoradas, fomentando o design de novos transceptores de rádio flexíveis e altamente integrados, capazes de suportar a transmissão simultânea de sinais multi-banda e multi-standard. O conceito de transmissão totalmente digital é considerado como um tipo de arquitetura promissora para lidar com esses requisitos desafiantes, devido ao seu *datapath* de rádio totalmente digital. Esta tese é focada na proposta e validação de arquiteturas de transmissores digitais totalmente integradas e avançadas que ultrapassam o estado da arte em diferentes figuras de mérito, como largura de banda de transmissão, pureza espectral, agilidade de portadora, flexibilidade e capacidade multibanda. A primeira parte desta tese introduz o conceito de transmissores de RF totalmente digitais. Em particular, os fundamentos inerentes a esta linha temática são apresentados, juntamente com os avanços mais recentes do estado-da-arte. O núcleo desta tese, contendo os principais desenvolvimentos alcançados durante o trabalho de doutoramento, é então apresentado e discutido. A primeira contribuição fundamental para o estado da arte é o uso de arquiteturas em cascata com moduladores $\Delta\Sigma$ para relaxar os requisitos de filtragem analógica dos transmissores RF totalmente digitais convencionais, mantendo a forma de onda envolvente constante. Em seguida, é apresentada a primeira arquitetura em que agregados de antenas são excitados diretamente por transmissores digitais de um único bit inseridos num único *chip*, com resultados promissores em termos de simplificação dos *front-ends* de RF e flexibilidade em geral. Posteriormente, é proposto o primeiro transmissor totalmente digital *RF-stage* relatado que pode ser incorporado dentro de um único Agregado de Células Lógicas Programáveis. Novas técnicas para permitir o desenho de transmissores RF totalmente digitais de banda larga são também apresentadas. Finalmente, o desenho de transmissores simultâneos de múltiplas bandas é exposto. Em particular, é demonstrado o desenho de transmissores de duas e três bandas ágeis e flexíveis, que é um tópico essencial para cenários que exigem agregação de múltiplas bandas.

Keywords All-Digital RF Transmitters, Reconfigurable Transmitter Architectures, Software-Defined Radios, FPGA, Delta-Sigma Modulation, Pulse-Width Modulation

Abstract The fifth generation of mobile communications (5G) is being prepared and should be rolled out in the early coming years. Massive number of Radio-Frequency (RF) front-ends, peak data rates of 10 Gbps (everywhere and everytime), latencies lower than 10 msec and huge device densities are some of the expected disruptive capabilities. At the same time, previous generations can not be jeopardized, fostering the design of novel flexible and highly integrated radio transceivers able to support the simultaneous transmission of multi-band and multi-standard signals. The concept of all-digital transmission is being pointed out as a promising architecture to cope with such challenging requirements, due to its fully digital radio datapath.

This thesis is focused on the proposal and validation of fully integrated and advanced digital transmitter architectures that excel the state-of-the-art in different figures of merit, such as transmission bandwidth, spectral purity, carrier agility, flexibility, and multi-band capability.

The first part of this thesis introduces the concept of all-digital RF transmission. In particular, the foundations inherent to this thematic line are given, together with the recent advances reported in the state-of-the-art architectures.

The core of this thesis, containing the main developments achieved during the Ph.D. work, is then presented and discussed. The first key contribution to the state-of-the-art is the use of cascaded Delta-Sigma ($\Delta\Sigma$) architectures to relax the analog filtering requirements of the conventional All-Digital Transmitters while maintaining the constant envelope waveform. Then, it is presented the first reported architecture where Antenna Arrays are directly driven by single-chip and single-bit All-Digital Transmitters, with promising results in terms of simplification of the RF front-ends and overall flexibility. Subsequently, the thesis proposes the first reported RF-stage All-Digital Transmitter that can be embedded within a single Field-Programmable Gate Array (FPGA) device. Thereupon, novel techniques to enable the design of wideband All-Digital Transmitters are reported. Finally, the design of concurrent multi-band transmitters is introduced. In particular, the design of agile and flexible dual and triple bands All-Digital Transmitter (ADT) is demonstrated, which is a very important topic for scenarios that demand carrier aggregation. This Ph.D. contributes with several advances to the state-of-the-art of RF all-digital transmitters.

Acronyms

C_{eff} Coding Efficiency.

$\Delta\Sigma$ Delta-Sigma.

$\Delta\Sigma$M Delta-Sigma Modulator.

ACPR Adjacent-Channel Power Ratio.

ACPR-L Adjacent-Channel Power Ratio Lower.

ACPR-U Adjacent-Channel Power Ratio Upper.

ADAAT All-Digital Antenna Array Transmitter.

ADT All-Digital Transmitter.

ASIC Application-Specific Integration Circuit.

AWG Arbitrary Waveform Generator.

BB Baseband.

BBU Base Band Unit.

BN Beamforming Network.

BP-$\Delta\Sigma$M Band-Pass Delta-Sigma Modulator.

BPF BandPass Filter.

BRAM Block Random-Access Memory.

BW Bandwidth.

C-RAN Cloud Radio Access Network.

CA Carrier-Aggregation.

CDM Code-Division Multiplexing.

CIC Cascaded Integrator-Comb.

CIFB Cascaded-of-Integrators, Feedback Form.

CIFB/F Cascaded-of-Integrators, FeedBack/FeedForward.

CIFF Cascaded-of-Integrators, Feedforward Form.

CMCD Current-Mode Class-D.

CORDIC COordinate Rotation DIgital Computer.

CRFB Cascaded-of-Resonators, Feedback Form.

CRFB/F Cascade-of-Resonators, FeedBack/FeedForward.

CRFF Cascaded-of-Resonators, Feedforward Form.

DAC Digital-to-Analog Converter.

DC Direct Current.

DDS Digital Direct Synthesis.

DFT Discrete Fourier Transform.

DSP Digital Signal Processor.

DUC Digital Up-Conversion.

EF Error-Feedback.

EVM Error-Vector Magnitude.

FFT Fast Fourier Transform.

FIFO First-In First-Out.

FIR Finite Impulse Response.

FoM Figures of Merit.

FPGA Field-Programmable Gate Array.

HP-$\Delta\Sigma$M High-Pass Delta-Sigma Modulator.

I/Q In-phase/Quadrature.

IC Integrated Circuit.

IF Intermediate Frequency.

IFFT Inverse Fast Fourier Transform.

IO Input-Output.

IoT Internet-of-Things.

IP Intellectual Property.

LFSR Linear Feedback Shift Register.

LO Local Oscillator.

LP Low-Pass.

LP-ΔΣM Low-Pass Delta-Sigma Modulator.

LPWM Limited Pulse-Width Modulation.

LTE Long-Term Evolution.

LUT Look-up table.

MASH Multistage Noise Shaping Modulator.

MER Modulation Error Ratio.

MGT Multi-Gigabit-Transceiver.

MIMO Multiple Input Multiple Output.

NMSE Normalized Mean Square Error.

NTF Noise-Transfer Function.

NZ Nyquist Zones.

OSR OverSampling Ratio.

PA Power Amplifier.

PAPR Peak-to-Average-Power Ratio.

PLM Pulsed Load Modulation.

PWM Pulse-Width Modulation.

QAM Quadrature Amplitude Modulation.

QPSK Quadrature Phase-Shifting Keying.

QPWM Quantized Pulse-Width Modulation.

RAM Random-Access Memory.

RAN Radio Access Network.

RBW Resolution Bandwidth.

RF Radio-Frequency.

ROM Read-Only Memory.

RRC Root-Raised Cosine.

RRH Remote Radio Head.

SDR Software-Defined Radio.

SFDR Spurious-Free Dynamic Range.

SMPA Switched-Mode Power Amplifier.

SNR Signal-to-Noise Ratio.

SoA State-of-the-Art.

SoC System on Chip.

SQNR Signal-to-Quantization Noise Ratio.

SR Symbol Rate.

SSB Single-Side Band.

TDM Time-Division Multiplexing.

TX Transmitter.

VBW Video Bandwidth.

VMCD Voltage-Mode Class-D.

VSA Vector Signal Analyzer.

ZOH Zero-Order Hold.

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Chapter 1

Introduction

Outline

This chapter starts by providing the scope and main motivation for this work. Then, the thesis main contributions are presented and finally, the chapter is concluded with the presentation of the document organization.

1.1 Scope and Motivation

Since the start of this decade, mankind has been watching a global spread of handsets, such as smartphones, tablets, as well as new network-dependent devices boosted by the omnipresence of wireless networks. This trend has led to successive generations of standards with higher throughput and mobility support. In just over three decades, mankind has witnessed four generations of mobile communications, imposing heavy modifications to the cellular infrastructures, and the fifth generation (5G) is being prepared and should be rolled out in the early coming years. Massive number of Radio-Frequency (RF) front-ends, peak data rates of 10 Gbps (everywhere and everytime), latencies lower than 10 msec (to support hard real-time applications) and huge device densities (in the so-called Internet-of-Things (IoT) scenarios), are some of the expected disruptive capabilities [A$^+$15, 5G 17]. Increasingly, this implies that the next generation of radios must be carefully designed in order to provide a smooth transition for the next generations of standards and technologies, at the same time that the performance of the previous generations must be maintained. Thus, it makes sense that features such as multi-standard support, flexibility, agility, real-time reconfigurability and upgradeability shall be valued.

At the same time, as analog RF components do not follow Moore's Law, their integration raises major constraints that have induced radical change of mindsets: moving from the analog- to the digital-centric design of RF transceivers together with a new type of software-centric paradigm. Agility, real-time reconfigurability, flexibility and the possibility of inte-

grating all the analog front-ends into a single core have been preferred over the conventional counterparts.

Interestingly though, this rising trend in the digitalization of conventional analog front-ends has motivated the radio research in a concept idealized in the later '90s: the Software-Defined Radio (SDR) [Mit95]. This idea envisioned a novel architecture for the radio systems, with the waveforms completely synthesized in the digital domain, achieving greater flexibility, reconfigurability and efficiency. The opportunities arising from this paradigm are unimaginable. The idea of having only one radio transceiver front-end completely independent from the standard, from the number of frequency bands, and completely agile, together with the capability of being real-time reconfigurable and upgradeable, is so ambitious that has caused a significant interest among all the research community. However, to accomplish this, the RF signal generation and analysis need to move closer to the antenna.

In view of the foregoing, if this change of mindset from the analog to the digital design has all the inherent advantages that the next generation of radios should have, one can foresee that the digitalization of the radios will underlie the future generation of wireless and mobile communication systems. This suggests that the ultimate target for these systems may be the All-Digital Transceivers, where everything is digital from end to end. In them lies the possibility of designing radio datapaths completely digital from the baseband up to the RF stage, leading to the development of flexible, reconfigurable, multi-band, multi-standard and highly-efficient transceivers [MSL05, HHNG08, SOC13a, POC15]. Focusing on the transmission side, without loss of generality, the underlying idea explores the quantization of an n-bit digital signal into a 2-level pulsed representation resulting in constant-envelope output signals, which can be directly amplified by highly-efficient Power Amplifiers (PAs), such as Switched-Mode Power Amplifiers (SMPAs). After the amplification, a reconstruction filter is required to reconstruct the signal before being fed to the antenna. With this approach, external and commercial n-bit Digital-to-Analog Converters (DACs) can be dismissed and on-chip 1-bit versions can be chosen instead. This ultimately leads to low-complex, flexible and reconfigurable transmitters with the potential to leverage the scalability and the integration-capability of such systems. Consequently, the analog front-end can be highly minimized and therefore, unprecedented massification in the number of transceivers can be achieved. Promising architectures have been demonstrated both into Field-Programmable Gate Arrays (FPGAs) or Integrated Circuits (ICs), in the sense of having full support for whole transmitter chains embedded within a single chip [MSL05, SOC13a]. In all of the related architectures, are notorious and evident all the attempts in moving all the analog functional blocks to the digital domain, as well as in pushing the digital blocks closer to the antenna element, as it was conceived in the original Mitola's work.

It should also be mentioned that integration of more and more RF front-ends, or equivalently, the massification in the number of RF front-ends, is one of the main flagship character-

istics from the novel generation of communication systems (5G). This has been a consequence of the renewed interest in the spatial domain that is being pointed out as a key enabler to improve radio resource efficiency at the same time that more capacity is enabled and, the use of multiple antennas have shown improvements in that domain [A+15]. As the conventional RF architectures are too bulky and too costly to provide an effective answer to these new trends, the use of All-Digital Transmitter techniques in this field in the next few years may also be a promising research track.

1.2 The Problem

As pointed out in the Scope and Motivation, All-Digital RF Transmitters are being presented as promising techniques for the next generation of communication systems. However, up to now, the Figures of Merit (FoM) of such systems in terms of achievable bandwidth, agility, flexibility, multi-band support, together with the challenging requirements in terms of analog filtering, have hindered the full adoption of this new paradigm in the design of commercial radio systems.

1.3 The Thesis

The main research work done in the scope of this Ph.D. was devoted to supporting the following hypothesis: *Can all-digital transmitter architectures compete with the conventional counterparts in terms of Figures of Merit within the context of 5G systems?* That is to say, the overall objective of this Ph.D. thesis is the exploration of highly parallel structures to support the design of innovative all-digital transmitters with enhanced FoM in terms of bandwidth, spectral purity, agility, flexibility, and multi-band capability, using highly integrated digital reconfigurable hardware.

Given the presented hypothesis, and after introducing the main research topics within this research field, the remaining chapters of this manuscript will be focused on the proposal and validation of fully integrated and advanced digital architectures that excelled the state-of-the-art in the most pressing FoM. Also, the main focus of this work is to propose the best-in-class architectures, not to provide high power implementations. This allows the author to perform general analysis that are not limited to certain amplifier topologies or implementation concepts from the RF front-ends. In addition to that, it must be highlighted that all the demonstrated concepts are built and tested in the lab. The thesis develops and presents systematic design methods of fully digital RF transmitters focused on the most pressing research challenges. This thesis follows a practical and pragmatic approach by defining the different research challenges, proposing innovative solutions, and experimentally validating them. FPGAs were used as prototyping and evaluation platforms by their cost- and time-effective inherent characteristics. Nonetheless, all the concepts and architectures can be

directly transferred and integrated to any other specialized application-specific circuit-level techniques.

1.4 Original Contributions

The concept of all-digital transmission is being pointed out as a promising architecture to cope with the foreseen challenging requirements of the future generations of mobile communications, due to its fully digital radio datapath. This Ph.D. work aims precisely in addressing some of the current limitations of such concept, by proposing and implementing innovative all-digital transmitter architectures with higher flexibility and integration, as well as improved figures of merit such as Signal-to-Noise Ratio (SNR), usable bandwidth and multi-band capability.

This manuscript is based on work presented in papers published in top journals and conferences in the field of this thesis and containing original contributions to the state-of-the-art. In particular, one can highlight the following ones:

- The relaxing of the analog filtering requirements in single-bit All-Digital Transmitters (ADTs). Specifically, cascaded Delta-Sigma ($\Delta\Sigma$) architectures were proposed as a way to drastically reduce the out-of-band noise around the carrier frequency while maintaining the constant envelope waveform;

- The design of Antenna Arrays based on single-chip and single-bit ADTs. In particular, the first real and complete system, experimentally validated in terms of beamforming and beamsteering capabilities, was demonstrated, with promising results in terms of flexibility and integration capability;

- The synthesis of RF-stage modulators within an FPGA. To accomplish this, the exploration of highly parallelized structures was presented to achieve high global sampling rates. This enabled the design of frequency-agile and real-time reconfigurable RF transmitters;

- The design of wideband ADTs. It was demonstrated that the fully parallel RF-stage architecture can be improved to enable the design of wideband RF transmitters;

- The design of frequency-agile and real-time reconfigurable dual- and triple-band RF modulators. In particular, a set of architectures suitable for concurrent multiple-band transmission was proposed and experimentally validated. Moreover, a pre-compensation scheme was also proposed to minimize the amount of out-of-band noise that may be folded back to the interest bands in multi-band Baseband (BB)-stage modulators.

1.5 Publications

Several important contributions to the wireless systems communication community were performed in the scope of this Ph.D., in the fields of all-digital RF transmitters, $\Delta\Sigma$/Pulse-Width Modulation (PWM) architectures and fully digital front-ends for antenna arrays. This thesis is based on the work presented in the following contributions:

- Journal Papers:

  J1 Daniel C. Dinis, Rui Cordeiro, Filipe M. Barradas, Arnaldo S. R. Oliveira, and José M. N. Vieira. Agile Single- and Dual-band All-Digital Transmitter based on a Pre-compensated Tunable Delta-Sigma Modulator. *IEEE Trans. Microw. Theory Tech.*, 64(12):4720–4730, Dec. 2016

  J2 Daniel C. Dinis, Rui Cordeiro, Arnaldo S. R. Oliveira, José M. N. Vieira, and T. O. Silva. A Fully Parallel Architecture for Designing Frequency-Agile and Real-Time Reconfigurable FPGA-based RF Digital Transmitters. *IEEE Trans. Microw. Theory Tech.*, 66(3):1489–1499, Mar. 2018

  J3 Daniel C. Dinis, Rui Ma, Shintaro Shinjo, Koji Yamanaka, Koon H. Teo, Philip Orlik, Arnaldo S. R. Oliveira, and José M. N. Vieira. A Real-time Architecture for Agile and Concurrent FPGA-based Triple-Band All-Digital RF Transmission. *IEEE Trans. Microw. Theory Tech.*, 66(11):4955–4966, Aug. 2018

  J4 Daniel C. Dinis, Arnaldo S. R. Oliveira, and José Vieira. Recent advances on All-Digital Antenna Array Transmitters. *Submitted to IEEE Microwave Magazine*, pages 1–6

- Conference Papers:

  C1 Daniel C. Dinis, Rui Cordeiro, Arnaldo S. R. Oliveira, and José M. N. Vieira. Tunable Delta-Sigma Modulator for Agile All-Digital Transmitters. In *IEEE MTT-S International Microwave Symposium Dig.*, pages 1–4, San Francisco, CA, USA, May. 2016

  C2 Daniel C. Dinis, R. Cordeiro, Arnaldo S. R. Oliveira, and José M. N. Vieira. Towards an All-Digital Antenna Array Transmitter. In *IEEE Field Programmable Logic Dig.*, pages 1–2, Lausanne, CH, Aug. 2016

  C3 Daniel C. Dinis, Arnaldo S. R. Oliveira, and José M. N. Vieira. All-Digital Transmitter Based on Cascaded Delta-Sigma Modulator for Relaxing the Analog Filtering Requirements. In *Proc. IEEE MTT-S International Microwave Symposium*, pages 145–148, Honolulu, HI, USA, Jun. 2017

  C4 Daniel C. Dinis, Arnaldo S. R. Oliveira, and José M. N. Vieira. All-Digital Transmitter Based Antenna Array with Reduced Hardware Complexity. In *Proc. IEEE*

MTT-S International Microwave Symposium, pages 153–156, Honolulu, HI, USA, Jun. 2017

C5 Daniel C. Dinis, Rui Cordeiro, Arnaldo S. R. Oliveira, José M. N. Vieira, and Tomás O. Silva. Improving the Performance of All-Digital Transmitter based on Parallel Delta-Sigma Modulators through Propagation of State Registers. In *Proc. IEEE International Midwest Symposium on Circuits and Systems*, pages 1133–1137, Boston, MA, USA, Aug. 2017

C6 Daniel C. Dinis, Rui Ma, Koon H. Teo, Philip Orlik, Arnaldo S. R. Oliveira, and José M. N. Vieira. An FPGA-based Multi-level All-Digital Transmitter with 1.25 GHz of Bandwidth. In *IEEE MTT-S International Microwave Symposium Dig.*, pages 1–4, Philadelphia, PA, USA, Jun. 2018

Other contributions were also performed within this Ph.D. period:

J5 Jorge Santos, Daniel C. Dinis, Diogo Riscado, Gustavo Anjos, Daniel Belo, Arnaldo S.R. Oliveira, Paulo Monteiro, and Nuno B. Carvalho. A Flexible Physical Layer and Fronthaul Research Testbed for C-RAN. *Microprocessors and Microsystems*, 52:480–490, Jul. 2017

C7 Andre Prata, Rui Cordeiro, Daniel C. Dinis, Arnaldo S. R. Oliveira, José M. N. Vieira, and N. B. Carvalho. All-Digital Transceivers - Recent Advances and Trends. In *Proc. IEEE CAS-S International Conference on Electronics, Circuits and Systems*, pages 233–236, Monte Carlo, Monaco, Dec. 2016

C8 Daniel C. Dinis, N.B Carvalho, J. M. N. Vieira, and Arnaldo S. R. Oliveira. Over the Air Characterization for 5G Massive MIMO Array Transmitters. In *Proc. IEEE MTT-S International Microwave Symposium*, pages 1441–1444, Honolulu, HI, USA, Jun. 2017

C9 Daniel C. Dinis, Arnaldo S. R. Oliveira, and José M. N. Vieira. FPGA-based All-Digital Antenna Array Transmitter. In *XIV Jornadas sobre Sistemas Reconfiguráveis Dig.*, pages 1–6, Lisbon, PT, Feb. 2018

C10 Daniel C. Dinis, Rui Ma, Koon H. Teo, Philip Orlik, Arnaldo S. R. Oliveira, and José M. N. Vieira. Towards Analog Filter-Free All-Digital Transmitters Through Hybrid Estimation and Cancellation of Delta-Sigma Modulation's Quantization Noise. In *IEEE MTT-S International Microwave and Radar Conference Symposium Dig.*, pages 1–4, Poznan, Poland, May. 2018

C11 Samuel S. Pereira, Abel Lorences-Riesgo, Daniel C. Dinis, Arnaldo S. R. Oliveira, José Vieira, and Paulo P. Monteiro. Millimetre-wave Real-time All-Digital Transmitter with Electro-Optical Upconversion. In *International Conf. on Transparent Optical Networks Dig.*, pages 1–4, Roma, Italy, Sept. 2018

C12 Abel Lorences-Riesgo, Samuel S. Pereira, Daniel C. Dinis, José Vieira, Arnaldo S. R. Oliveira, and Paulo P. Monteiro. Real-Time FPGA-Based Delta-Sigma-Modulation Transmission for 60 GHz Radio-over-Fiber Fronthaul. In *European Conference on Optical Communication Dig.*, pages 1–4, Bucharest, Romania, July 2018

1.6 Document Organization

This document is organized into eight different chapters, described and listed as follows:

- Chapter I, **Introduction**, starts by laying out the background and motivation for this different reality of RF transceivers. Then, presents the problem's description that underlies the thesis, as well as the general objectives and the structure of this document;

- Chapter II, **State-of-the-art**, aims to provide a full overview on Digital Transmitter Architectures, spanning from the Classical RF Transmitter Architectures, to the All-Digital Transmitter Architectures, passing through the foundations on Pulse Encoding Techniques and the main research challenges associated to this type of techniques;

- Chapter III, **Relaxing the Analog Filtering Requirements**, demonstrates that the use of cascaded $\Delta\Sigma$ architectures can have a profound impact in relaxing of the analog filtering requirements from the conventional ADTs;

- Chapter IV, **All-Digital Antenna Array Transmitters**, reports one promising architecture where Antenna Arrays are directly driven by single-bit All-Digital Transmitters. Promising results are demonstrated in the simplification of the RF front-ends and in the overall system flexibility;

- Chapter V, **Fully Agile Modulators**, presents the use of highly parallel structures to design fully agile RF-stage modulators embedded into an FPGA. As will be seen throughout this document, the proposed architecture is quite scalable and flexible, leading to a high OverSampling Ratio (OSR), without an extra increase in the output serializer's bitrate;

- Chapter VI, **Wideband Delta-Sigma Modulators**, presents a set of architectures based on multicore-$\Delta\Sigma$ modulators that can have a significant impact on the design of wideband modulators;

- Chapter VII, **From Single- to Concurrent Multi-Band Transmission**, reports a set of BB- and RF-stage architectures that leverage the design of concurrent multi-band transmitters. In particular, the design of agile and flexible dual and triple bands ADTs is demonstrated;

- Chapter VIII, **Conclusions**, states a final conclusion, possible applications and gives an outlook on future work.

It must be highlighted that the all architectures proposed from chapter III up to chapter VII are covered in author's contributions. Similarly, the structuring and the text from these chapters were adapted from the same contributions in order to provide a clearer understanding of the research topics.

Chapter 2

RF Transmitter Architectures

Outline

This chapter provides a theoretical overview of the most relevant transmitter architectures. The starting point is related with the conventional architectures that are mostly used for single- and multi-output transmitters. Then, some new paradigms based on fully digital transmitters (referred to as ADTs) are briefly introduced, and to conclude, a brief state-of-the-art is presented.

2.1 Classical RF Single-band Transmitter Architectures

One interesting track in research and development is the design and optimization of conventional RF transmitter architectures. As the massification of RF front-ends starts to be faced as a near-term reality in different application scenarios (such as basestations, active antenna arrays, among others), it is of paramount importance to take a look into the classical RF architectures with single- and multi-outputs. As this Ph.D. work is devoted to the design and proposal of novel transmitters, this document will just focus on the RF transmitters architectures.

2.1.1 Single-Input Single-Output Architectures

The majority of the wireless transmitters is based on a baseband DAC pair followed by an In-phase/Quadrature (I/Q) modulator together with a 2-stage upconversion scheme, referred to as heterodyne architecture (Figure 2.1a). The I/Q digital signal is converted to an analog one by a DAC pair, filtered, upconverted to an Intermediate Frequency (IF) carrier and filtered, and upconverted again to the RF or microwave carrier. After this, the signal must be filtered before being amplified by a PA. If the amplifier's behavior is not fully linear, another filter must be included before radiation to reduce the out-of-band distortion that may cause interference issues. This approach suffers from several problems, such as the requirement

for complex image rejection filters, I/Q imbalance, and due to the large number of external components, it is a costly and complex solution that does not fit well on System on Chips (SoCs)'s integration [MSL05].

Similar to the heterodyne architecture, but with only one upconversion and filtering stage, the homodyne architecture depicted in Figure 2.1b can be introduced. Even though the significant reduction in the number of external analog circuits, the truth is that the main disadvantages from the heterodyne counterpart are still present, such as the I/Q imbalance and the need of complex image rejection filters. Nonetheless, it is one of the most well-known and dominant architecture in typical RF systems.

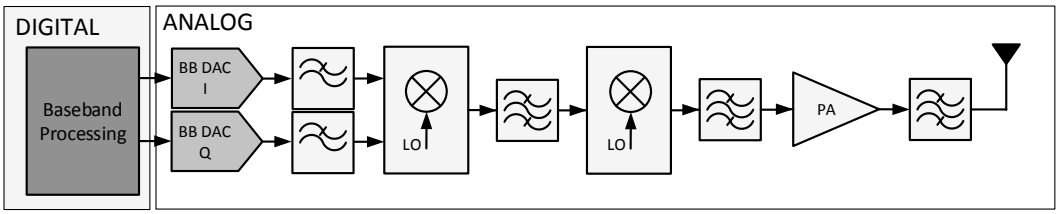
As the DACs' sampling rates have been increased, the inherent flexibility from the digital domain has been valued and preferred over the traditional analog chains, causing the DACs to be brought closer to the antennas. For some applications where the DAC's sampling rate is high enough to generate signals in the RF range, the analog I/Q modulator can be dismissed, and the signal produced from the RF DAC is just filtered and amplified before being radiated. This architecture is depicted in Figure 2.1c, where one can see that the upconversion stage was included in the digital domain (referred to as Digital Up-Conversion (DUC)). It must be mentioned that throughout this manuscript, and despite not explicit in the figure, this DUC may comprise a digital interpolation to adjust the involved sampling rates as first-stage, before performing the frequency shifting. In addition to the flexibility of designing the signals in the digital domain, several other advantages can be pointed out, such as: no amplitude and phase imbalances in the modulator, elimination of the unwanted image at the output of the upconverting mixer which eases the filtering requirements, reduced area footprint, lower costs in the analog front-end, among others.

After reviewing the different transmitter architectures, it is understandable that the DAC is their core. The analog front-end is completely conditioned by the DAC's characteristics and, in the extreme case if the DAC is able to reach the RF or microwave range, the analog front-end can be reduced to only filtering, amplification and radiation.

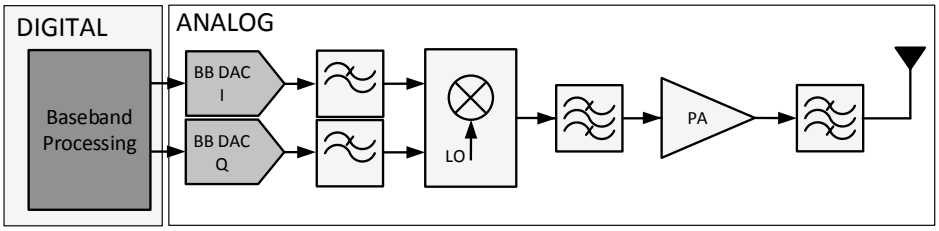
2.1.2 Scaling to Multiple Elements

As antenna arrays are indispensable components in high data-rate wireless communication systems, it is of utmost importance to highlight how the classical RF transmitter architectures can be adapted to perform the driving of such systems.

Antenna array define any system with more than one radiant element. They were firstly proposed as an innovative way to design antennas with a very high gain, without an extra increase in the electrical size. Beamforming, or also referred to as Spatial Filtering, is one of the most well-known applications of antenna arrays, and one of the most complex ones, due to the challenging synchronization between multiple outputs. By this reason, this document will just focus on the beamforming architectures.



(a)



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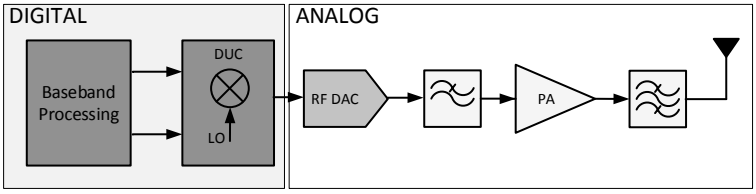


(c)

Figure 2.1: Illustration of the different Transmitter (TX) architectures: (a) heterodyne upconversion; (b) homodyne upconversion; (c) direct-RF upconversion.

To accomplish this spatial capability, a Beamforming Network (BN) must be included within the RF front-ends. The BN is required to distribute the power to each element, at the same time that it adjusts the amplitude and phase of each output. These adjustments are typically performed with resort to phase shifters and amplifiers/attenuators. Depending on the placement of this BN, different architectures have emerged in the literature [PT12, XWTL14, FYT$^+$16].

RF-path Beamforming Architecture

The most well-known architecture is referred to as RF-path Beamforming Architecture and is depicted in Figure 2.2a. As the name states, the BN is directly applied in the RF domain (more precisely, before the amplification to achieve higher efficiencies). One of the main advantages from this architecture is that, as the BN is placed close to the radiation elements, all the remaining components/systems to the left of it can be shared among all the radiant elements. This architecture is particularly suitable for millimeter and sub-millimeter wave systems, where the integration of phase shifters is simpler and cheaper [PT12]. At lower frequencies, phase shifters are normally bulky, and noise and nonlinearities may be

introduced.

Baseband-path Beamforming Architecture

In the BB-path Beamforming Architecture, the BN is directly applied to the analog BB signal, before any up-conversion stage (Figure 2.2b). This leads to the finest phase resolution with lowest power penalties [PT12]. However, the different Local Oscillators (LOs) and mixers may cause significant I/Q imbalances that may jeopardize the system performance. This typically implies the use of feedback loops for each TX chain for calibration purposes. Thus, the scalability of such systems in large-scale arrays is typically limited [PT12].

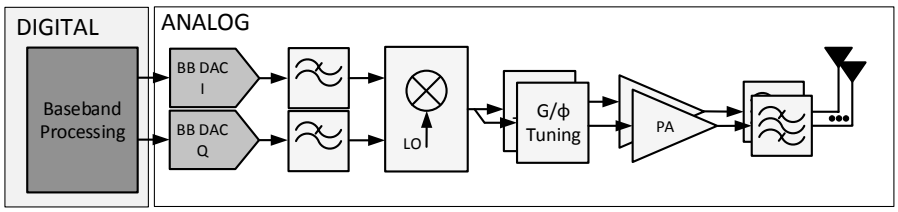
Digital Beamforming Architecture

The Digital Beamforming Architecture is one of the most promising techniques. It is quite similar to the BB-path one, with the difference that the BN is placed in the digital domain, within a Digital Signal Processor (DSP) (Figure 2.2c). Thus, this architecture shares the advantages of the latter one, at the same time that enables a simplification of the RF circuit design. However, two DACs per each array element are required and besides that, other issues such as I/Q mismatch and different group delays for I- and Q-path can also be pointed out [PT12].

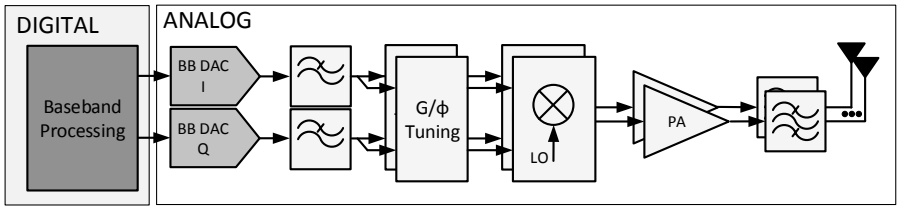
The Ideal Beamforming Architecture

After reviewing the conventional architectures for antenna arrays, one can stress that the inclusion of BNs leads to a twofold reality: a desired flexibility and reconfigurability can be achieved, at the expense of an extra level of complexity that may bound the system scalability.

Looking into all the aforementioned architectures, the importance of digital beamforming techniques has been emphasized throughout all the literature [XWTL14, FYT$^+$16] and they are being pointed out as the key enabling technology to provide high performance allied with high flexibility and reliability [GCG15]. This recent interest is due to the fact that, by including the BN in the digital domain, the RF circuit/layout design is relaxed, at the same time that the software can start to play a leading role in the design and control of antenna arrays. However, one can recognize that the need of two external DACs per radiant element, together with the use of analog upconversion stages, is too burdensome and hampers the scalability and integration-capability of such systems from the area footprint's viewpoint. At least, theoretically, it is possible to formulate an ideal architecture that does not jeopardize the system scalability. Such architecture is depicted in Figure 2.2d. It is based on the Digital beamforming techniques, to enable the long-awaited reconfigurability and flexibility. However, the upconversion stages were moved into the digital domain, at the same time that the external DACs were removed. This leads to a neat layout and, in practice, just amplification, filtering



(a)



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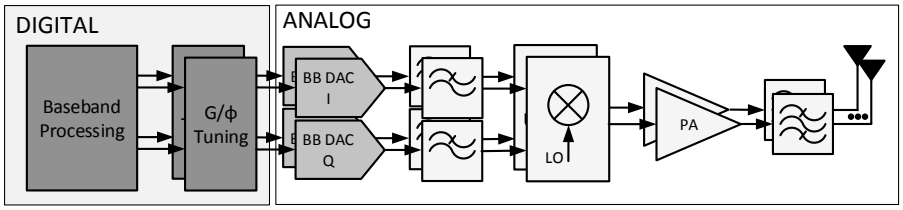

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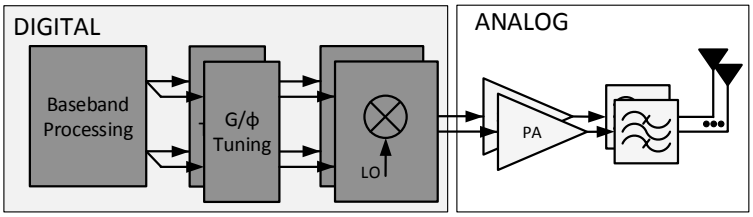

(d)

Figure 2.2: Illustration of the different TX beamforming architectures for antenna arrays: (a) RF-path beamforming; (b) BB-path beamforming; (c) digital beamforming; (d) ideal beamforming.

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and radiation is required. As will be seen in Chapter 4, the concept of ADTs may be a promising solution to try to reach this ideal architecture. Lastly, it must be emphasized that Figure 2.2d aims at illustrating the conceptual idea and thus, for convenience, the embedded buffer that converts the digital into an analog single-bit waveform was omitted.

2.2 All-Digital RF Transmitters

As previously introduced, the rising trend in the digitalization of conventional analog front-ends has opened the doors to the concept of SDR. This concept aims at having one agile radio

transceiver front-end completely independent from any specific standard, and able to deal with any number of frequency bands. Relevant state-of-the-art is pointing towards ADTs as the ultimate target for this technology, due to the inherent fully digital behavior from end to end. The research on this class of transmitters is focused on the development of reconfigurable, agile, multi-band, multi-standard and highly-efficient solutions [HHNG08, SOC13a]. The recent advances in the architectures of these transmitters have undoubtedly contributed to this, largely by enabling the transmission of radio signals using a fully digital datapath. This section elaborates the main foundations of this concept as well as the research and development tracks that have been followed by the research community.

2.2.1 General Architecture

All-Digital RF Transmitters are a particular subset of the SDR techniques that has attracted much and renewed interest from both the industrial and academy parties. The underlying idea is the encoding of an n-bit digital signal into a representation with lower number of bits, enabling the removal of external DACs and external upconversion stages. Most of the reported transmitters explore the use of reconfigurable and on-chip 1-bit topologies to transmit signals [CRJZ11, SOC12b, SOC13a]. The use of single-bit transmitters leads to signals with constant time envelope which can be amplified by highly-efficient and non-linear amplifiers, such as SMPAs. With such a concept, the analog front-end is reduced to only amplification, filtering and radiation.

The first attempts to achieve single-bit and efficient power amplification through the utilization of $\Delta\Sigma$ or PWM modulators were applied to low-frequency applications [HS93]. These implementations have shown that highly-efficient and non-linear amplifiers can be used which motivated the exploration of the RF scenario and several academic researches have started. The need to achieve the GHz frequency range has triggered arduous research in this topic. In [NL07], pulse encoding techniques were applied to the signal magnitude to change the power amplifier bias. Others have designed a pulse shaping stage to the in-phase and quadrature components of the signal followed to analog wideband mixers, through the multiplication of the signal with a binary waveform representation of the carrier frequency [Mor98], or with bulky and high-cost external high-speed multiplexers [HHNG08, GHA+10b, WMR+04].

While some opted for the implementation of these type of modulators in IC [MSL05, CRJ+12], others have emphasized the FPGAs inherent flexibility and upgradeability. Among the latter, the idea of discarding the external components required for the upconversion stage (either analog wideband mixers or high-speed multiplexers) unleashed intense investigation in the sense of going further and facing the design of DUC stage within a single FPGA. This idea was achieved through the utilization of Multi-Gigabit-Transceivers (MGTs) that are present in the medium/high range FPGAs [SOGC12a, SOGC12b]. These MGTs are power-efficient

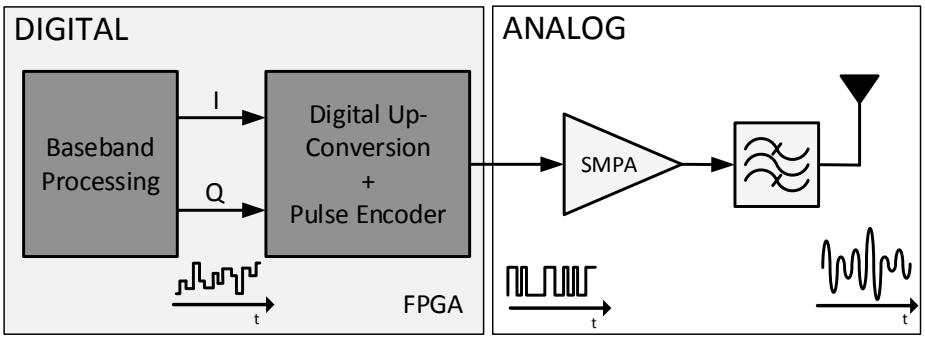

Figure 2.3: Illustration of the general all-digital transmitter architecture. For convenience the mixed-domain serializer that converts the digital into an analog pulsed waveform was omitted.

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transceivers, with embedded serializers, highly configurable and tightly integrated with the FPGA's programmable logic resources. As an example, line rates from 500 Mbps up to 32.75 Gbps are available in the GTY Transceivers from Xilinx Ultrascale+ FPGAs [Xil17]. This small step was of paramount importance to get closer to the goal of having completely flexible and integrated transmitters.

The general block diagram of an FPGA-based ADT is depicted in the Figure 2.3. The baseband complex input signal is divided into the I/Q data components before being converted into a 2-level representation. This conversion is done with an oversampled Pulse Encoder. As will be seen throughout this document, the DUC can be placed either before or after the Pulse Encoder. In short, the output from the ADT is a pulsed waveform which contains the digitally modulated signal at a given RF carrier frequency, together with the out-of-band noise. After amplification, a BandPass Filter (BPF) is required to reconstruct the desired modulated signal before radiation.

2.2.2 Oversampled Converters

As the concept of fully digital transmission relies on the use of 1-bit waveforms, without significant degradation of the system performance, it is of paramount importance to quantify the quantization impact.

In the case of Nyquist-Rate Converters, assuming a full-scale sine wave input, the Signal-to-Quantization Noise Ratio (SQNR) is given by [JM08]:

$$SQNR = 6.02N_{bits} + 1.76 \tag{2.1}$$

where SQNR is in dB and N_{bits} is the number of bits from the converter. Eq. (2.1) demonstrates that the hard truncation to 1-bit leads to an inferior system performance due to the low achieved SQNR (= 7.78 dB). Thus, the use of such hard truncation seems to be ill-suited

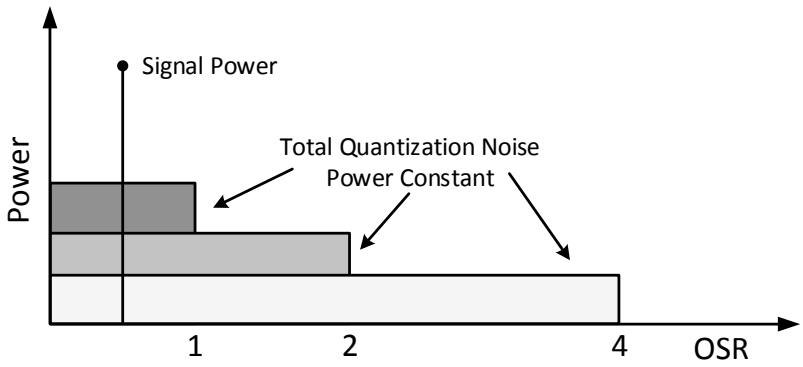

Figure 2.4: Illustration of the SQNR gains in oversampled converters. One can see that the oversampling just affects the noise spectral density, not changing neither the signal power nor the total quantization noise power [JVR11].

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to the design of the desired transmitters. Therefore, in an attempt to achieve better performance, oversampling has been successfully applied to data converters. Oversampling is the process of acquiring more samples per second than those required by the Nyquist-Shannon criterion. The underlying idea is that, even though the total quantization noise power does not change with the sampling rate, its distribution will be changed [JVR11]. Thus, this means that the same noise power will be spread in a larger frequency range, reducing the spectral density of the quantization noise (Figure 2.4). Under the assumption of a full-scale sine wave input [JM08]:

$$SQNR = 6.02N_{bits} + 1.76 + 10\log(OSR) \tag{2.2}$$

where OSR is given by $fs/(2BW)$ and, fs is the sampling rate and BW is the signal bandwidth. In practice, the spectral density of the quantization noise is reduced by 3 dB/octave where 1 octave is the double of the sampling rate. Equivalently, this means 0.5 bits/octave [JM08].

In addition to the enhancement in the system performance, oversampled converters have the potential to relax the accuracy requirements from the analog components at the cost of added digital circuitry. As the advancement of digital IC technologies is leading to cheaper digital circuitry, this generation of converters is increasingly receiving more attention from the industry community in different scenarios and applications [ST05]. However, as can be seen in Figure 2.5, challenging OSR can be required when 1-bit quantization is used. While such techniques are suitable for low-frequency applications (such as audio [GS86], or power electronics [RME92]), they are not an ideal solution for the case of RF/microwave systems. Even though, as will be seen, this SQNR enhancement due to the OSR will be the starting point in the design of Pulse Encoders that can provide a reasonable system performance.

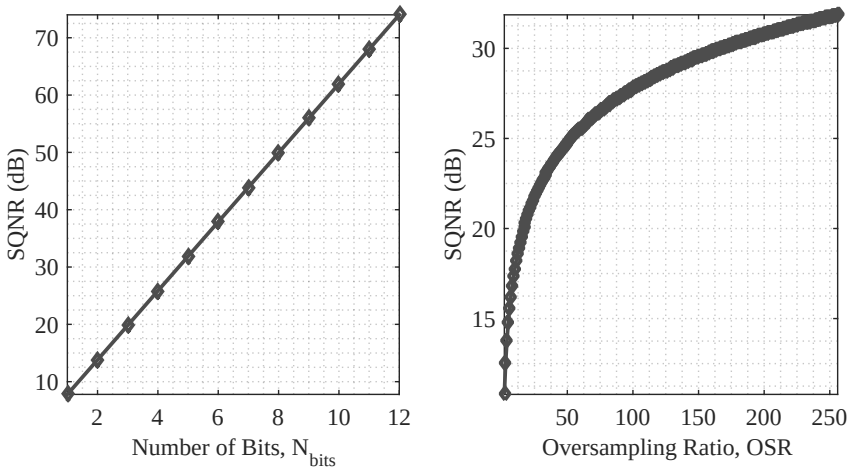

Figure 2.5: SQNR in a Nyquist-Rate converters (a), and in an 1-bit Oversampled converters. It is understandable that the OSR provides an extra degree of freedom in the enhancement of the SQNR.

2.2.3 Pulse Encoding Techniques

In the context of ADTs, Pulse Encoding Techniques refer to a set of architectures that perform the reduction of the number of levels, while trying to maximize the in-band signal integrity. All of them are based on oversampling converters, and most of them employ Delta-Sigma Modulator ($\Delta\Sigma$M), PWM or some combination thereof.

Delta-Sigma Modulation

One well-known pulse encoder is the $\Delta\Sigma$ architecture that was firstly introduced in the '60s [IYM62]. This type of mechanism is widely used to transform a time envelope varying signal into a low-resolution equivalent (typically in a bi-level representation as illustrated in Figure 2.7). To achieve this, these modulators employ signal oversampling, quantization and a feedback loop for shaping the quantization noise in frequency (referred to as *Noise Shaping*). As will be seen, this Noise Shaping will break the spectral uniformity of the quantization noise, providing an SQNR enhancement in the in-band signal [EHG13]. Figure 2.6 is an illustration of the impact of the Noise Shaping in terms of increasing the in-band signal performance.

An illustration of the typical spectrum of a modulated signal encoded by a $\Delta\Sigma$M is depicted in Figure 2.7. One can see that the distortion and quantization noise are pushed away from the input signal.

The non-linear behavior of the quantizer presented in the $\Delta\Sigma$M hinders the mathematical analysis in a deterministic way. The simplest technique to analyze such systems replaces the quantizer by just an additive white noise source, treating the system as a linear model. Even though this model lacks in robustness by assuming that the quantization noise has certain

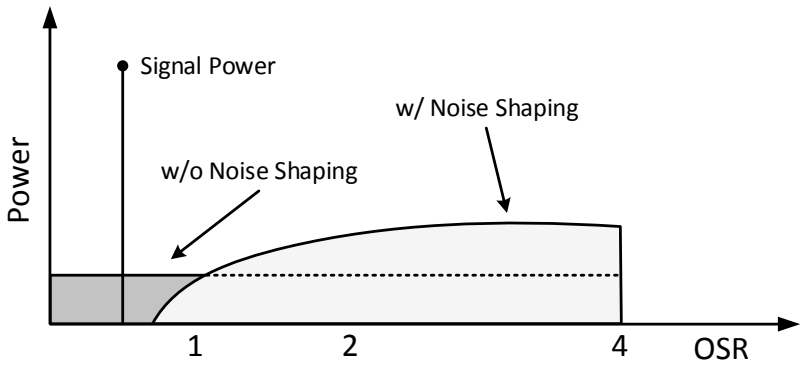

Figure 2.6: Illustration of the oversampled gain in terms of the SQNR with, and without, noise shaping.

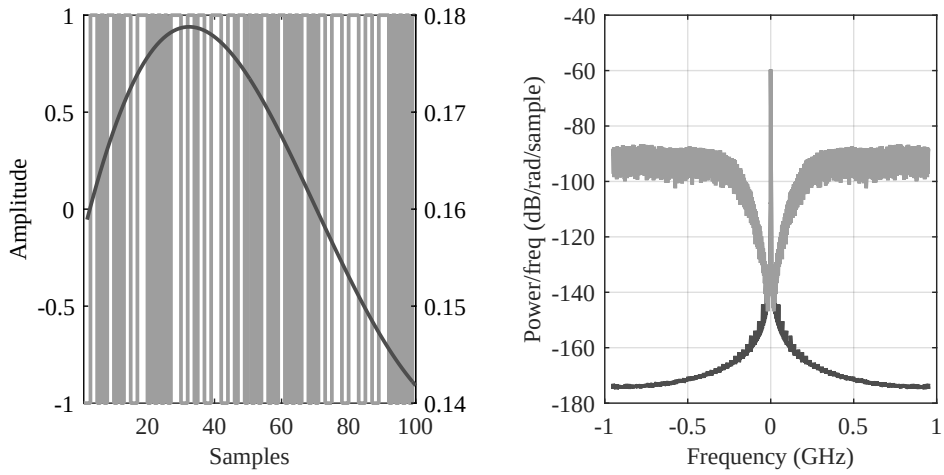

Figure 2.7: Illustration of the time-domain (left) and frequency spectrum (right) of an ΔΣM-encoded signal. One can see the original interpolated signal (black) and the ΔΣM-encoded signal (gray).

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convenient properties (such as white spectrum or uniform distribution) [Sch91], it is the most well-known model and the one applied by every designer to come up with preliminary insights.

Figure 2.8 illustrates the general block diagram of a ΔΣM. Replacing the quantizer by an additive white noise source, the output signal is given by:

$$\begin{aligned} Y(z) &= STF(z)X(z) + NTF(z)E_q(z) \\ &= \left[\frac{G(z)}{1+G(z)H(z)}\right] X(z) + \left[\frac{1}{1+G(z)H(z)}\right] E_q(z) \end{aligned} \tag{2.3}$$

where $STF(z)$ and $NTF(z)$ are referred to *Signal Transfer Function* and *Noise Transfer Function*, respectively. The key idea is the application of different transfer functions to both the input signal and the quantization error with the overall aim of minimizing the spectral

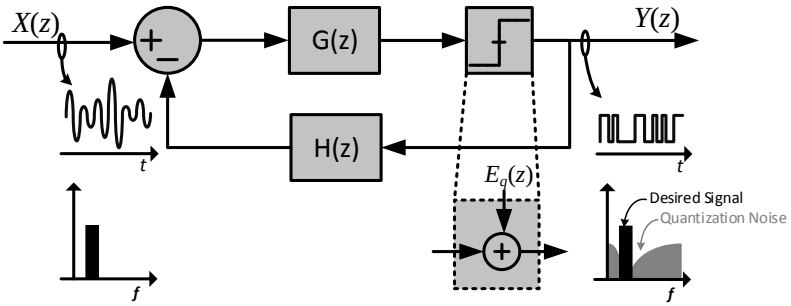

Figure 2.8: Block diagram illustrating the general model of a ΔΣM.

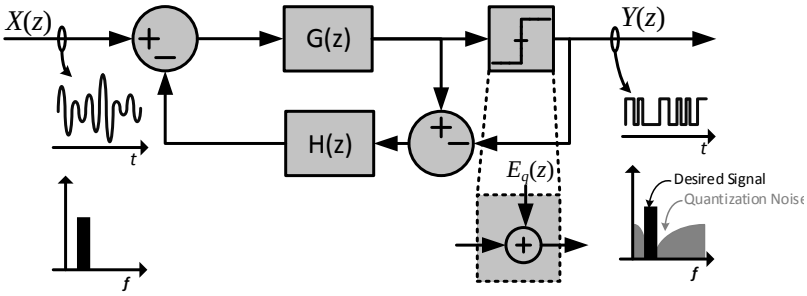

Figure 2.9: Block diagram illustrating the general model of an Error-Feedback ΔΣM.

overlap between them. In this way, it is possible to reshape the quantization noise to be pushed away from the signal band.

A slightly different architecture opts by directly computing the quantization noise and forwarding it to the transfer function from the feedback loop. This architecture is designated as Error-Feedback ΔΣM and is illustrated in Figure 2.9.

Based on the figure, and through the replacement of the quantizer by an additive white noise source, the output signal is given by:

$$\begin{aligned} Y(z) &= STF(z)X(z) - NTF(z)E_q(z) \\ &= G(z)X(z) - (1 + G(z)H(z))\, E_q(z) \end{aligned} \tag{2.4}$$

As will be seen throughout this document, this architecture leads to low-complex modulators, with the shortest critical paths. Critical path in digital design stands for the path in the entire design with the maximum delay. Taking into account that the maximum sampling rate for any architecture is inversely proportional to its critical path, this is of paramount importance.

Regardless of the chosen architecture, the signal's SQNR is proportional to the order of the Noise-Transfer Function (NTF) (simply referred to as modulator order), and to the OSR. As increasing the sampling rates may not be very practical, in most cases, one solution could be the SNR's improvement at the expense of designing higher-order modulators [KK03].

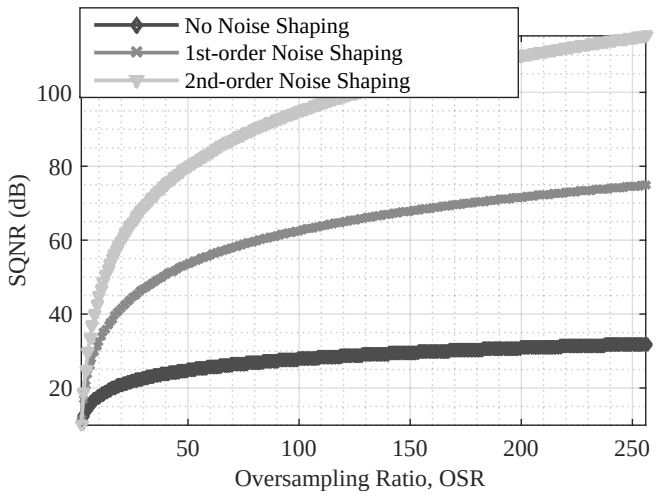

Figure 2.10: SQNR in 1-bit Oversampled converters for different order of noise shaping.

Under the assumption of a full-scale sine wave input for an oversampled converter with 1st-order noise shaping [JM08]:

$$SQNR = 6.02N_{bits} + 1.76 - 5.17 + 30\log(OSR) \tag{2.5}$$

It provides extra 9 dB or, equivalently, a gain of 1.5 bits/octave.

In the case of a 2nd-order noise shaping, and under the same input characteristics [JM08]:

$$SQNR = 6.02N_{bits} + 1.76 - 12.9 + 50\log(OSR) \tag{2.6}$$

It provides extra 15 dB or, equivalently, a gain of 2.5 bits/octave. This should be compared with the 0.5 bits/octave in the oversampled converters with no noise shaping (Figure 2.10).

One can demonstrate that an Lth-order noise shaping modulator improves the SQNR by $6L + 3$ dB/octave, or equivalently, $L + 0.5$ bits/octave [JM08].

To achieve higher-order modulators, two typical structures are used - the interpolative, and the Multistage Noise Shaping Modulator (MASH). On the one hand, the interpolative architecture simply relies on the replacement of low-order transfer functions by high-order ones. Unfortunately, specifically for input signals with higher Peak-to-Average-Power Ratio (PAPR), and for single-bit quantizers, the high NTF's gain typically leads to unstable systems. And once unstable, they may never return to stability even when the large input signals are not present anymore [JM08]. This implies the insertion/placement of poles to control the NTF's gain, leading to the common architectures such as Cascaded-of-Integrators, Feedback Form (CIFB), Cascaded-of-Integrators, Feedforward Form (CIFF), Cascaded-of-Resonators, Feedback Form (CRFB) and Cascaded-of-Resonators, Feedforward Form (CRFF) [ST05]. For some particular input signals, the stability is ensured in such techniques, but at the

expense of an increased interconnection complexity. This ultimately increases the critical path from the modulator, reducing the achievable sampling rate, and, consequently, the achievable OSR. Moreover, the introduction of poles also leads to a significant reduction of the notch bandwidth, that leads to a drop in the overall encoded bandwidth [STN97]. On the other hand, the MASH architectures rely on the use of a cascade-type structure where the overall higher-order modulator is built upon the use of lower-order modulators [CWG89]. Then, all the different outputs are filtered and combined, leading to the desired Lth-order global transfer function. As low-order (hence, more stable) modulators are the essential blocks of this architecture, it ends being more robust to stability issues [MUI+87]. Unfortunately, the final combination network leads to a higher number of levels, which hinders the applicability of these architectures in the design of single-bit ADTs.

So far, it was assumed that the interest signal was placed at BB, requiring an NTF working as a high-pass filter to ensure a proper noise shaping. This is one of the most common cases, also referred to as baseband $\Delta\Sigma$ architecture, and it can be found in [CRJ+12, COVS14, GHA+10b, Gha10a, GEN+12, HHGP14, HHNG08, SOC13b]. If the interest signal is in another carrier frequency, the concept of bandpass $\Delta\Sigma$M must be applied. In this case, the NTF is designed as a bandstop filter. Examples of such topology can be found in [GHA+10b, KHM+01, RKL+14, JS06a, JS08].

Pulse Width Modulation

Another well-known pulse encoder is the PWM architecture that was firstly introduced in the '40s [KO47]. The underlying idea is the encoding of amplitude and phase information in the width and timing of pulses. The traditional mechanism to generate a PWM signal is based on the comparison between the modulating signal $x(t)$, and the reference signal $r(t)$, which can be described by:

$$y(t) = sign(x(t) - r(t)) \tag{2.7}$$

where $sign$ is the sign function.

A thorough mathematical formulation of the PWM is out of the scope of this thesis. However, in an attempt to shed some insight into this technique, let us briefly demonstrate why this technique is suitable to be used as a Pulse Encoder. A mathematical model that enables the approximation of 2.7, for every $x(t)$, was proposed in [MMHW14] and is reported in [POC16]:

$$\begin{aligned} y(t) &= x(t) + n_q(t) \\ &= x(t) + \frac{2}{\pi} \sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \frac{1}{m} e^{jmw_c t} \sin\left(\frac{m\pi}{2}(1 + x(t))\right) \end{aligned} \tag{2.8}$$

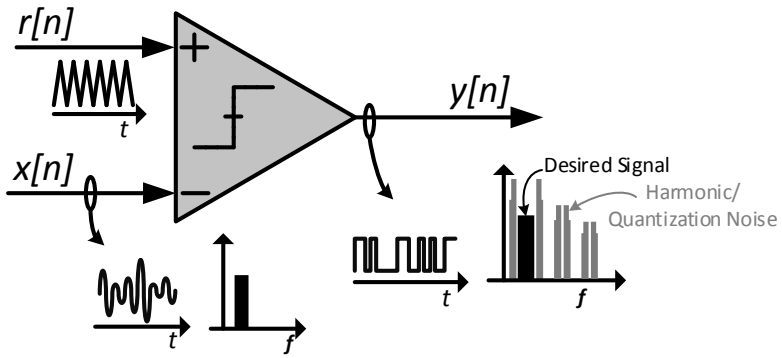

Figure 2.11: Illustration of the PWM concept: the comparison between the input signal with a reference waveform that produces a 1-bit output signal.

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where w_c is the angular frequency from the reference signal, and $n_q(t)$ is the non-linear distortion.

It is understandable from (2.8) that the output signal $y(t)$ is composed by the original input signal $x(t)$ together with some non-linear distortion. This non-linear distortion is composed of distorted replicas of the input signal, centered at multiples of the reference frequency, along with the inherent noise from the quantization process [CVS10, MMHW14]. At Direct Current (DC), the equation also demonstrates that there is no noise-distortion, and thus, the in-band signal integrity can be reasonably maintained.

This technique can be transferred to the digital domain. Figure 2.11 illustrates the block diagram of the digital PWM. In this case, the digital PWM can be seen as a sampled version of the above-described analog PWM. This means that spectral aliasing will occur due to the infinite bandwidth of $y(t)$ [TMT17b]. This, depending on the placement of the aliases, may cause performance degradation of the digital PWM as compared to the analog version [HCSV13].

An illustration of the typical spectrum is shown in Figure 2.12. One can see the distorted replicas that corrupt the spectrum. The suitability of this technique to be used as a Pulse Encoder falls in the ideally intact copy of the input signal that is generated between the first harmonic distortion peaks. Several relevant works for this technique have been reported in the literature [SOC12b, SOC13b, ZMD+14a, COV15].

Note that due to the open-loop characteristic inherent to the PWM operation principle, the concept of noise-shaping is not present. Nonetheless, there are some reported works where feedback loops were integrated to provide a noise-shaping behavior [BTM+09, RAM12, MHH+14].

In the previous paragraphs, it was assumed that the input signal was low-pass. However, the same technique can be applied for bandpass signals [FNDR13, NRD14, HMFP13, Oze14, WMR02, TMT17a, POC15]. Two different approaches are typically followed in the State-of-the-Art (SoA). On the one hand, the upconversion can be seen as part of the PWM process

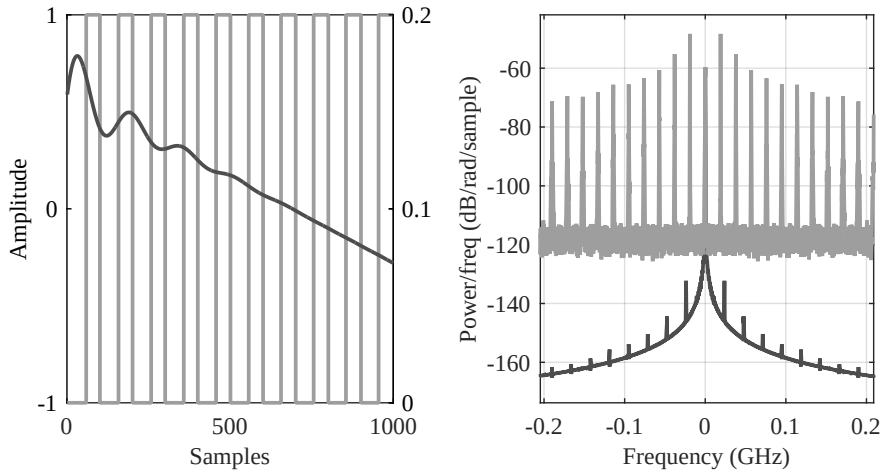


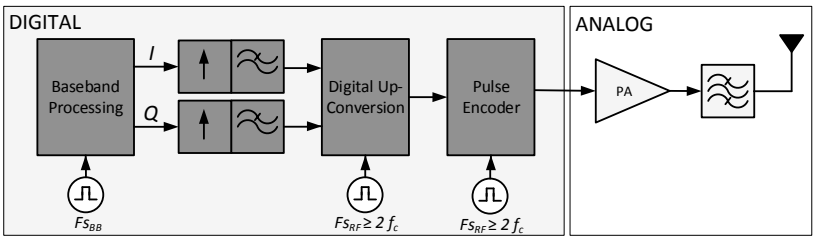
Figure 2.12: Illustration of the time-domain (left) and frequency spectrum (right) of an PWM-encoded signal. One can see the original interpolated signal (black) and the PWM-encoded signal (gray).

by considering one of the harmonics as the fundamental signal, instead of distorted replicas [NRD14]. In this case, it is required to perform some pre-compensation in the input signal to compensate the fact that the RF amplitude of the first harmonic is proportional to the sin function and not to the input signal itself [TMT17a]. On the other hand, the PWM process can be applied to an upconverted RF signal instead of the BB signal [POC15]. In this case, depending on the location of the input signal, frequency components from other Nyquist Zones may fold back into the band of interest, which may jeopardize the in-band signal's integrity. As firstly pointed out in [POC15], and as further demonstrated in this work, the noise distribution is highly dependent on the reference signal frequency.

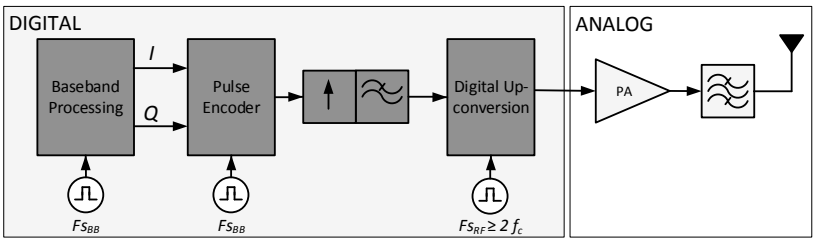
2.2.4 BB- vs RF-stage Modulators

All-digital RF transmitters can be split into two main classes, BB- or RF-stage, depending on the placement of the Pulse Encoder (in relation to the DUC module), and on the clock rate at which the quantization is done.

As the name suggests, RF-stage modulators perform the pulse encoding directly at RF rates, after the input signal is upconverted to the RF carrier. The block diagram of such modulators is illustrated in Figure 2.13a). This leads to a required sampling rate of at least twice the desired RF carrier frequency, in both the pulse encoder and in the DUC modules (hereinafter referred to as Fs_{RF}). This requires the use of high sampling rate pulse encoders capable of transforming the m-bit upconverted data to a 1-bit equivalent. The design of such encoders results in layout constraints and timing closure difficulties, leading to the costly and time-consuming development of specific custom integrated circuits [FFS+09, OGSM09, SGH+09, OGOS12, MYHF17]. In addition to this, as all the logic needs to be clocked at



(a)



(b)

Figure 2.13: Illustration of the general block diagram of a BB-stage ADT (a) and an RF-stage ADT (b). In these specific figures, and for the sake of shedding some insights on the practical implementations of such architectures, it was decided to explicitly include the digital interpolators before the DUC. However, one must highlight that throughout this dissertation, the digital interpolations may be included within the DUCs.

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these sampling rates, the power consumption may be typically too high.

To avoid this complex design process, BB-stage modulators were proposed in the literature [HHNG08]. This type of modulators applies the pulse encoder at low sampling rates (hereinafter referred to as Fs_{BB}), digitally interpolates the signal to Fs_{RF} and, subsequently, upconverts it to the RF carrier frequency (Figure 2.13b). As a conventional DUC would lead to a non-constant envelope waveform, a "special" DUC must be used to perform the signal upconversion while maintaining the signal with two levels. The only technique reported in the literature to design this specific DUC is based on the replication and combination of 1-bit BB samples ($x_I[n]$ and $x_Q[n]$) together with their inverted equivalents ($-x_I[n]$ and $-x_Q[n]$), simply referred to as *Select&Combine* [RAM12, RAM13, RALM14, COVS14]. In an attempt to shed some insight into this technique, it is of paramount importance to demonstrate why this technique is suitable to be used as a DUC. Formally, this operation can be described with three main blocks: an L-factor up-sampler followed by a Zero-Order Hold (ZOH) filter and together with a real upconverter module (depicted in Figure 2.14). The data is firstly up-sampled from the pulse encoder's sampling frequency (Fs_{BB}) to the serializer's sampling frequency (Fs_{RF}), resulting in an up-sampler factor of $L = Fs_{RF}/Fs_{BB}$. In practice, this operation is done by inserting L-1 zero-valued samples between the original samples with the aim of increasing the sampling rate. However, a major disadvantage emerges: undesired spectral images are created and centered on multiples of the original sampling rate. After

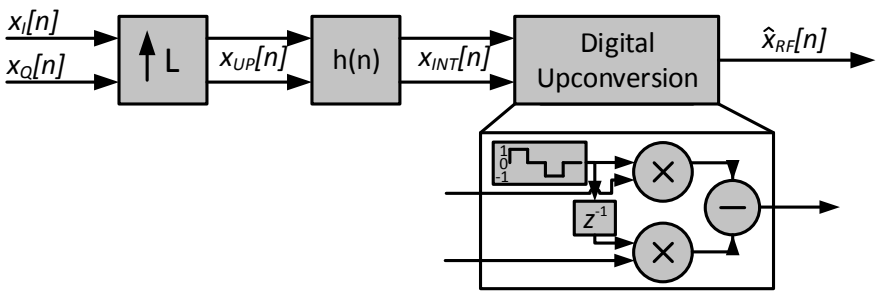

Figure 2.14: Block diagram of the specific digital upconverter module used in BB-stage modulators.

that, an ideal lowpass filter should be included to smooth the discontinuities out, replacing the zeros with medium values and minimizing the undesired spectral images. However, its application is not possible owing to the need of maintaining the signal with only two levels, which means that a discrete rectangular filter, with the following impulse response, must be applied: [RALM14]

$$h[n] = \begin{cases} 1, & 0 \leq n \leq (L-1) \\ 0, & n \geq L \end{cases} \tag{2.9}$$

After this interpolation, an upconversion is required to translate the carriers from BB/IF to RF. In a more formal way, the complex data is multiplied by an RF carrier and just the real part is considered:

$$\begin{aligned} \widehat{x}_{RF}[n] &= Re\left(x_{INT}[n]e^{jw_c n}\right) = \\ & x_{INT_I}[n]\cos(w_c n) - x_{INT_Q}[n]\sin(w_c n) \end{aligned} \tag{2.10}$$

By just considering the real part, the complex multiplier comes down to just two multiplications. Moreover, considering the RF center frequency as one-fourth of the sampling frequency, the design of the upconversion chain can be even more simplified. In this frequency, $e^{\frac{j\pi n}{2}} = \cos\left(\frac{\pi n}{2}\right) + j\sin\left(\frac{\pi n}{2}\right)$, which results in the tristate pulsed quadrature signals $\cos(\frac{\pi n}{2}) = [1, 0, -1, 0]$ and $\sin(\frac{\pi n}{2}) = [0, 1, 0, -1]$. Replacing these signals in (2.10) leads to a signal in the form of $[x_I[n], -x_Q[n], -x_I[n], x_Q[n]]$ with the inherent advantage that the multipliers can be replaced by logical inverters. Thus, one can conclude that this strategy can effectively perform the digital upconversion from BB to one fourth of the serializer's sampling rate.

Despite the neatness and elegance of the BB-stage modulators, these architectures possess inherent drawbacks. First, the change of the carrier frequency means that the serializer's sampling rate must be changed. This leads to an unintentional variation of the modulator's OSR, which will considerably modify the system FoM. Second, as the pulse encoder is being

operated at very low sampling rates, the OSR is inherently quite limited, which, ultimately, bounds the modulator's performance. Finally, the agility and the multi-band capability in these techniques are quite limited, which is also a consequence of the low sampling rate from the pulse encoder, which leads to a limited 1st Nyquist Zone.

2.2.5 System-level Figures of Merit

As in every system design, there are some important FoM that must be valued and taken into consideration to assess the system performance. The design of an ADT is not an exception and thus, the most important FoMs for the research line will be introduced.

It was decided to split the FoM into two main categories - in-band performance and out-of-band performance - depending on the part of the spectrum that must be assessed. The key performance indicators in terms of in-band signal are:

- Modulation Error Ratio (MER) is a measure of the SNR in digitally modulated signals. It is computed over N symbols, and is defined as [ETR97]:

$$MER = \frac{\sum_{j=1}^{N} |S(j)|^2}{\sum_{j=1}^{N} |Z(j) - S(j)|^2)} \tag{2.11}$$

  where Z is the actual received symbol, and S is the ideal symbol.

- Error-Vector Magnitude (EVM) is another measure of modulation quality and error performance in digitally modulated radios [CS13]. It is proportional to the difference between the measured and the ideal symbols, and inversely proportional to the MER [GGS04]:

$$EVM = \sqrt{\frac{\sum_{j=1}^{N} |Z(j) - S(j)|^2)}{\sum_{j=1}^{N} |S(j)|^2}} \times 100 \tag{2.12}$$

In terms of out-of-band performance FoM, one can state:

- Coding Efficiency (C_{eff}) is typically used to quantify the quantization noise on the transmitter efficiency [EHG13], and is computed in the frequency domain, by integrating the in-band power, P_{fund}, over the total output power without filtering P_{tot}.

$$C_{eff} = \left(\frac{P_{fund}}{P_{tot}}\right) \times 100 \tag{2.13}$$

  C_{eff} can provide an initial insight about the spectral purity of the transmitter. Moreover, some authors consider that it is also relevant for the prediction of the average efficiency

of a given RF transmitter, with a bi-level output [GHA+10b]:

$$\eta_{Average} = C_{eff}\, \eta^{BW}_{PA_{peak}}\, \eta_{duty-cycle} \tag{2.14}$$

where $\eta^{BW}_{PA_{peak}}$ is the peak efficiency of the PA averaged over the signal bandwidth, and $\eta_{duty-cycle}$ is the duty-cycle efficiency effect. However, the impact of the C_{eff} is still quite dependent on the PA stage, because depending on matching bandwidths, not every out-of-band power will be dissipated. Taking into account this issue, some authors introduced the Limited Coding Efficiency (C_{eff1-5}),, which is the coding efficiency within the range of one tenth of the carrier frequency up to 5 times the carrier frequency [MYHF17].

- Adjacent-Channel Power Ratio (ACPR) provides the ratio between the total output power in the fundamental zone, P_{fund}, to the total power integrated in a lower, P_{LA}, and upper, P_{UA}, adjacent-channel bands [CS13]. Can be mathematically described as:

$$ACPR_T = \frac{P_{fund}}{P_{LA}+P_{UA}} = \frac{\int_{\omega_{L2}}^{\omega_{U1}} S_o(\omega)d\omega}{\int_{\omega_{L1}}^{\omega_{L2}} S_o(\omega)d\omega + \int_{\omega_{U1}}^{\omega_{U2}} S_o(\omega)d\omega} \tag{2.15}$$

where $S_o(\omega)$ is the power spectral density.

In the context of this thesis, all the reported results are quantified either in terms of EVM-MER pairs when the in-band performance is the dominant indicator that needs to be highlighted, or in ACPR when the out-of-band noise is the key factor to be focused on. C_{eff} is not presented as a performance indicator, because again, its impact is quite dependent on the amplification stage (stage that is not focused in the context of this thesis).

2.3 Main Research Topics on All-Digital RF Transmitters

This section tries to provide an overview on the relevant works from the SoA in the research field of ADTs. The main research topics that have been followed by the research community will be reported, together with the specific and relevant works that have been proposed. It was decided to organize the relevant reported works from the SoA into a set of main research topics that have been addressed by the research community.

2.3.1 Transmission Bandwidth

To meet the high-data-rate requirements from the new wireless communication standards in an efficient way, the first step involves the increase of the available bandwidths. The achievable bandwidth in ADTs is proportional to the Pulse Encoder's sampling rate and is also dependent on the notch bandwidth from the ΔΣM (or spectral gap in the PWM case).

Thus, it is understandable that one of the most relevant research topics that has attracted considerable attention is related to novel techniques to achieve higher pulse encoder's sampling rates.

As the increase of sampling rates through the use of single-rate approaches requires the custom design of Application-Specific Integration Circuits (ASICs), the use of multi-rate methodologies started to be valued, particularly in the presence of feedback loops, such as in $\Delta\Sigma$Ms. The typical technique to achieve this is based on polyphase decomposition applied to a specific modulator's subsystem [PJ93], or to the whole modulator [COVS14]. However, the SoA has also demonstrated that the scalability of this technique is very limited, because pipeline stages in the $\Delta\Sigma$ architectures can not be included [COVS14]. This implies an inherent trade-off between the number of phases and the sampling rate of each phase. As the number of phases times the sampling rate of each phase defines the modulator's global sampling rate, and ultimately, its OSR, this means that the maximum global sampling rate is bounded.

A similar alternative is based on deriving novel modulators based on the node equations [KK00], but it has also been demonstrated that, for a high number of phases, the sampling rate gains are limited [MFKC15].

A single-bit semiparallel processing structure to accomplish the high-frequency processing is also proposed in [HHGP14]. The proposed structure achieves a higher OSR, by processing N constant samples in parallel by combining N closed-loop processing blocks of a regular $\Delta\Sigma$M. However, the last processing element of the proposed architecture leads to an increased critical path, resulting in reduced sampling rates. Thus, even though the promising results for low bandwidths (around 0.4 MHz and 1.6 MHz), the proposed architecture is not scalable with the bandwidth.

Another pseudo-parallel $\Delta\Sigma$ was proposed in [JS14]. The architecture is based on the previous one [HHGP14], but the block-to-block dependence that limits the clock speed was removed. To accomplish this, the authors proposed the use of speculation to alleviate the connection between the modulator critical path and the clock frequency. Thus, there is no need to wait for the results from the previous iterations, at the expense of replicating logic for each possible set of output bits. However, for a large set of output bits, the area and power overheads can be too heavy.

Then, a fully parallel architecture was proposed in [COVS16] with N multiple modulators running in parallel, each one processing independent slices (of size K) of the same input signal. This architecture reached the usable Bandwidth (BW) of 125 MHz (it is important to emphasize that at the publication date, the maximum BW was far below 50 MHz). In particular, two new subsystems - deinterleaving and interleaving modules - responsible for performing the temporary storage of samples as well as their re-arrangement were introduced. However, as a downside, the discontinuities in every K samples cause impulsive noise that

degrades the overall system's performance. As a workaround, the length of each slice must be increased. The main drawback is a considerable digital processing resources usage allied with a higher latency that may be problematic for such systems.

Then, an optimized 2nd-order Time-Interleaved $\Delta\Sigma$M with 488 MHz of BW was reported in [THTK17]. In addition to the use of speculation, bit separation was also proposed to enable higher sampling rates. Bit separation enables the use of smaller accumulators to accommodate the higher- and the lower-order bits, leading to a reduction of the overall critical path. As a downside, the achievement of such wide bandwidths entails the use of challenging serializer sampling rates of around 20 Gbps. In addition to the increased complexity and cost, the design of analog front-ends for such high sampling rates becomes quite challenging. The need for high serializer's sampling rates is quite common in the majority of the SoA, due to the application of the DUC after the pulse encoder (the concept of BB-stage modulator). In particular, 28 Gbps was reported in [THT+16], 20 Gbps in [THTK17] and 60 Gbps in [MYHF17].

Chapter 6 will demonstrate that the design of RF-stage modulators allied with fully parallel $\Delta\Sigma$M can demonstrate promising results in terms of bandwidth with reasonable serializer's sampling rates. In particular, 125 MHz of bandwidth will be demonstrated with a single-bit architecture, and 1.25 GHz of bandwidth with a 3-bit architecture.

2.3.2 Carrier Agility

To accomplish the Radio Access Network (RAN) expectations in a compact and efficient way, there is a strong need for the development of flexible, agile and reconfigurable radio transceivers, with native support for multiple standards [FBBM+15]. Real-time frequency agility is one of the main research topics in the field of ADTs, and it can be split into two main sub-areas, depending on the type of modulator: BB- or RF-stage.

On the one hand, the carrier agility in the BB-stage modulators is quite limited by several reasons. As introduced before, in this class of modulators, the DUC is based on the combination and replication of the I/Q samples together with the inverted versions. This leads to the carrier frequency to be one fourth of the serializer's sampling rate. The most straightforward way to transmit at other carrier frequencies is based on the real-time adaptation of the number of I/Q samples [SOGC12a]. However, the agility continues to be limited to a set of possible carrier frequencies ($Fs_{RF}/4$, $Fs_{RF}/8$, $Fs_{RF}/16$ and so on). Equivalently, the serializer's sampling rate can also be changed in real-time [SOC12a]. Again, even though the serializer sampling rate can be in theory updated to achieve the desired carrier frequency, there is a drastic consequence: the OSR from the Pulse Encoder will be changed as well. Thus, any change in the serializer's sampling rate leads to an unintentional variation of the modulator's sampling frequency, resulting in a change of the OSR, which will considerably modify the system's FoM. A novel technique which allows continuous adjustment of f_c in

digital domain was proposed in [RAM12]. The technique comprises a quadrature bandpass noise shaping stage in addition to a closed-loop PWM that enables the quantization noise shaping around the desired IF. A similar architecture composed of a two-stage upconversion chain together with an IF image rejection was also proposed in [SOC13a]. Nonetheless, the tunability on the placement of the carrier is still limited to a small 1st Nyquist Zone, due to the low pulse encoder's sampling rate.

On the other hand, the agility on the RF-stage modulators can be quite wide, because the DUC is placed before the Pulse Encoder. Thus, the pulse encoder is being clocked at a higher sampling rate (typically equal to the serializer's sampling rate), which means that it has a higher 1st Nyquist Zone. Thus, the carrier agility would only be limited by the frequency resolution from the DUC (typically imposed by the number of the bits from the phase accumulators from the Digital Direct Synthesis (DDS)). However, as far as FPGA-based modulators are concerned, there is no architecture suitable for the design of such modulators, because it is not possible to clock the programmable logic subsystems within the FPGAs at at least two times the desired RF carrier frequency (when focusing the typical range of 500 MHz up to 6 GHz). Thus, the wideband carrier agility is only found in specific custom ICs [FFS+09, OGSM09, SGH+09, OGOS12].

Chapter 5 will demonstrate the first architecture that enables the synthesis of an RF-stage modulator within an FPGA. The underlying idea falls into the exploration of highly parallelized structures to achieve high global sampling rates. In particular, real-time agility in the range from 100 MHz up to 6 GHz with a maximum frequency resolution of 1.5625 MHz will be demonstrated.

2.3.3 Multi-band Capability

To meet the data-rate requirements in an efficient way, the first step involved the increase of the available bandwidths in the 3G systems [IEhF+10]. Then, in an attempt to achieve scalable wider bandwidths, without spectrum allocation constraints, the concept of Carrier-Aggregation (CA) was introduced in 4G systems, such as Long-Term Evolution (LTE)-Advanced [IEhF+10]. By standardizing the contiguous and the non-contiguous CA capabilities, the combination of multiple frequency bands to conduct high-speed data transmission was enabled. Due to the commercial success of Long-Term Evolution (LTE)-Advanced features, it is expected that they will continue to be evolved, as a part of 5G technologies [LKK+16]. Nevertheless, despite the apparent ideal and native support for the multi-band capability, design challenges associated with the non-contiguous CA transmission have hampered the proposal of multi-band solutions.

The reported literature on non-contiguous CA ADTs is quite scarce. Generally speaking, multi-band transmission can only be achieved with integer multiples of the modulators sampling frequencies [SOC12a], or with reduced sampling rate topologies [KI10, MTKS13].

Others, employ bulky and inefficient power combiners to join different bands before transmission [KI10, BCHG13]. All these difficulties in designing multi-band transmission arise from the placement of the DUC after the pulse encoding (recall Figure 2.13b). Following this approach, as the bandwidth of encoded signals is technically infinite, the upconversion to the different bands typically leads to degraded system performance.

In addition to that, as far as the FPGA-based architectures are concerned, the limited sampling rate from the programmable logic subsystems (typically less than 200 MHz) limits the 1st Nyquist Zones (NZ). This considerably limits the maximum distance between different bands to twice this value [assuming complex Single-Side Band (SSB) upconversions schemes]. Thus, the only methodology to achieve higher spans between bands is based on the utilization of replicas from different NZs [SOC12a]. However, the inherent decrease in terms of SNR, associated with the need for maintaining an integer multiplicity in all the involved sampling rates/frequencies leads to reduced performance.

Chapter 7 will demonstrate a set of different architectures suitable for concurrent dual-band and triple-band transmission. Moreover, a pre-compensation is also proposed to minimize the amount of out-of-band noise that may be folded back to the interest bands in BB-stage modulators. As will be seen, in the dual-band case, real-time agility in the placement of up to two bands in the range of 300 MHz around the carrier frequency is demonstrated. In the triple-band case, up to three bands can be located in the range from 100 MHz up to 2.5 GHz with a frequency resolution of 4.88 MHz.

2.3.4 Analog Filtering Requirements

Recalling Figure 2.13, the BPF is of utmost importance to reconstruct the analog signal before radiation and to minimize the out-of-band noise that is radiated. As the design of tunable filters with high Q-factor is quite challenging, there has been an interest in proposing novel strategies to relax the analog filtering requirements, either through the integration of embedded reconstruction filtering techniques, or through easing the Q-factor requirements.

Concerning the development of architectures with an embedded filtering capability, one can refer to the use of power combiners to combine different outputs, and somehow, to generate a mixed-domain combination filter. Related to this, different architectures were proposed in the literature. Silva *et al.* proposed one multiple-output architecture where the signal's phase is kept constant contrary to the phases of the unwanted noise [SOC13b]. A similar approach was followed in [TCBK06, COV16, GFK16] where the delay and the weight from each output were carefully chosen to implement an embedded Finite Impulse Response (FIR) filtering scheme. Nonetheless, all these architectures are not quite appealing in terms of efficiency, due to the need for using multiple SMPA and a power combiner, or a power combiner and a linear PA.

As far as the relaxing of the Q-factor is concerned, a method for canceling the bandpass

quantization noise in envelope pulsed transmitter architectures (also called *carrier bursting*) was proposed in [GEN+12]. The architecture explores the overlap of a controlled amplitude component in the pulses. Nonetheless, this techniques leads to fluctuations in the signal envelope, hindering the use of SMPA. A similar architecture was proposed in [EH13, CMST15, CMS+17] for quadrature transmitters. However, the architecture requires the use of one extra PA, and one power combiner placed after the PAs, which from the viewpoint of the efficiency, can be problematic. A method for reducing the Q-factor requirements was proposed in [SOC12a] for architectures based on Look-up tables (LUTs) (such as PWM). The idea is based on the random circular shifting of the pulsed waveforms in order to maintain the same energy, but with different words. As well, a new PWM technique based on an optimized LUT that reduces the PWM harmonic distortion near the transmitted carrier frequency was proposed in [COV15]. This approach enables the utilization of low stringent bandpass filters for the output RF reconstruction filter, which allows for an increase of signal bandwidth. The increase of the modulator's order to push the quantization noise away from the carrier frequency in $\Delta\Sigma$ architecture was also proposed in [RKR15]. However, this tends to increase the modulator's critical path which means that lower sampling frequencies are achieved. Furthermore, instability problems may also appear.

Chapter 3 will demonstrate an architecture that maintains the single-bit output while achieving a drastic reduction of the out-of-band noise around the carrier frequency. The proposed architecture relies on the use of a 2-stage $\Delta\Sigma$M with different output levels and different sampling rates.

2.3.5 System Efficiency

All-digital transmitters rely on the exploration of the Class-S transmitter architecture, where a constant-envelope waveform is driving SMPAs [CMS+15]. Ideally, in SMPAs, the transistor acts as a closed switch with a zero resistance during the ON-state, and as an open switch with an infinite resistance during the OFF-state. By doing this, no overlap between the drain current and voltages occurs and, ultimately, the power dissipation is zero, leading to an efficiency of 100%. The typical SMPAs fall in the classes D, E and F of amplification [Ser12]. In short, Class-D amplification employs two transistors as switches and two subclasses can be designed - Voltage-Mode Class-D (VMCD) or Current-Mode Class-D (CMCD) - according to the type of the waveform of the voltage and current (square and sinusoidal, or vice-versa, respectively). Class-E amplification employs a single transistor as a switch. The drain-voltage waveform results from the sum of the DC and RF currents charging the drain-shunt capacitance. Class-F enables higher efficiency by employing harmonic resonators in the output network that shapes the drain waveforms [RAC+02].

Although Class-S operation can ideally achieve 100% of power efficiency independent of power back-off due to the non-overlap of the voltages and current waveforms [WMH10], there

are a set of characteristics that cause significant degradation. First, one should point out the presence of design impairments (such as finite length transmission lines connections, and the skew in the switches input signal [Pir14]) as well as the switch impairments (such as non-zero internal resistance [JS06b]). Second, the inclusion of a high-Q BPF with narrower bandwidth than the PA behaves like a complex, time-varying load impedance to the PA [WJ12]. This may cause an overlap between the voltage and current waveforms, reducing the system efficiency [Mu09]. To minimize this effect, the Pulsed Load Modulation (PLM) amplifier architecture was proposed in [JW08] by replacing the SMPA by 2 class-B PA controlled by the same envelope modulator. However, it must be pointed out that this class of amplification falls out of the scope of the Class-S operation, which is the reason why this research line will not be further elaborated. However, implementations for such modulators can be found in [JHG16, JEHG17]. At last, one should also emphasize that the duty-cycle from the pulsed waveform also leads to a modulation of the load seen by the PA. One promising way to minimize this effect is proposed in [Oze14] in which the imaginary part of the load impedance is varied along with the input duty-cycle, in order to maintain the high-efficiency independent from the input signal.

Also related to the interconnection between pulsed modulators and SMPAs is the minimum width that an input pulse must have to be correctly amplified. In this sense, some RF-PWM variants were investigated [MHH+14]: Limited Pulse-Width Modulation (LPWM) and Quantized Pulse-Width Modulation (QPWM). While in the first, pulses shorter than the minimum width are skipped, in the second, only N discrete and non-zero pulse-widths are allowed in the SMPA input.

The dependence between C_{eff} and the overall system efficiency was investigated in [JS06b] and [GHA+10b] (recall (2.14)). As an example, one ADT with a highly-efficient SMPA of around 80% and a overall system efficiency of 5% is reported in [GHA+10b]. Even though the research community also points out that the impact of the C_{eff} in the system efficiency can not be so straightforwardly generalized, because depending on matching bandwidths, not every out-of-band power will be dissipated [MYHF17], one can understand that the C_{eff} can not be neglected. Thus, in this sense, it is quite important the proposal of new techniques to reduce the out-of-band noise, or in other words, increasing the C_{eff}. While some authors presented the development of architectures with an embedded filtering capability based on analog power combiners as promising solutions for the enhancement of the C_{eff}, and ultimately, the increase of the system efficiency [SOC13b, COV16, JCOC16], the fact is that these claims are not entirely true, due to the inclusion of the analog power combiner after the SMPAs which may jeopardize the entire system efficiency. However, such architecture can be interesting if the power combination is performed in an efficient way, such as with extended H-bridges SMPAs [ZMD+14a, ZMD+14b]. Nonetheless, up to now, the complexity inherent to the development of efficient multi-level Class-S PAs has limited the number of levels to less than

three [CMS+15]. Similarly, techniques to reduce the quantization noise around the carrier frequency were proposed in [EH13]. The work demonstrates that by just removing a certain part of the quantization noise, while the signal envelope is kept quasi-constant, it is possible to improve the C_{eff} without imposing nonlinearity and distortion to the system.

2.3.6 Applications

The potential of ADTs modulators has also been widespread for other scenarios, such as the centralized RAN architectures, antenna arrays, and radars.

The current trend in RAN architectures is to move the baseband processing to the cloud to achieve centralized signal processing and management. Cloud Radio Access Network (C-RAN) architecture is an example of these new cellular network architectures designed for the future mobile network infrastructures, which focuses on the separation of the digital Base Band Units (BBUs) from the Remote Radio Heads (RRHs). The interface between the BBUs and the RRHs is typically based on optical links and is referred to as *fronthaul*. ADTs have been proposed as promising solutions to reduce the complexity of the RRH. By sending optical pulses with the encoded RF information, the RRH is just responsible for filtering, amplification and radiation. Relevant works were reported in both the downlink [COV14] and in the uplink [MKH+11, POC16]. Similarly, Pulse Encoders are also being pointed out as the key enablers for the throughput explosion in digital mobile fronthauls [WYY+17, VKBL+17]. The overall idea is to encode the BB I/Q data (with no upconversion to RF) into pulsed waveforms before being sent to the optical link. In this way, the throughput in the fronthaul can be maximized, because fewer bits are transmitted per user, without a significant loss of performance.

The exploration of all-digital RF transmission techniques in antenna arrays have also been targeted by the research community, for both non-communication and communication purposes. On the one hand, the design of radars based on Pulse Encoders were firstly introduced in [WCMA04]. The key idea is to reduce the number of external DACs to boost the development of scalable radars, without challenging requirements in the analog front-end design. Similar relevant implementations have been proposed in [FPS14, NAK17, NK17]. On the other hand, the integration of ADTs in antenna arrays for communication purposes was firstly introduced by the author's group in [DCOV16a]. The major idea is to relax the challenging requirements in the design of multiple front-ends for antenna arrays. Afterwards, [MYHF17] also proposed the same idea as the main foundation for the design of Massive-Multiple Input Multiple Output (MIMO) front-ends. Chapter 4 will further develop on this research topic, by demonstrating the first real and complete system, experimentally validated in terms of beamforming and beamsteering capabilities, where antenna arrays are directly driven by multiple ADTs fully integrated into the same FPGA.

2.4 Summary and Concluding Remarks

This chapter provided a review on the RF transmitter architectures, starting from the conventional architectures to the novel concept of All-Digital Transmitters. The main foundations of this new concept were presented, together with the relevant works reported from the SoA and the associated research challenges. Thus, the next chapters will provide a succinct description of the main achievements during the development of this Ph.D. work. In that sense, each chapter contains a modular description of a novel architecture that has excelled the reported SoA in the aforementioned research challenges. In the overall, all the proposed architectures allow the development of innovative FPGA-based all-digital transmitters with improved FoMs.

Chapter 3

Relaxing the Analog Filtering Requirements

Outline

The stringent requirements for the output reconstruction filter pose several constraints in the deployment of the ADTs into realistic scenarios. This is essentially due to the need of having a high-Q analog reconstruction filter which, ultimately, hinders the flexibility and agility of the digital radio transmitter. Thus, in this chapter, this research line is addressed and a promising architecture that relaxes the requirements for the reconstruction filter is proposed.

This chapter is supported by the conference paper [DOV17b]. The chapter presents a BB-stage ADT architecture that combines cascaded $\Delta\Sigma$Ms with different sampling rates with the underlying idea of relaxing the analog filtering requirements.

3.1 Contextualization

The relevant ADTs presented in the SoA typically rely on the use of a single-stage modulator, with a single-bit quantizer in the output. However, by doing this, a huge amount of quantization noise is generated and shaped according to the modulator's NTF, with a considerable part located around the BB signal. The typical way to improve the available processing bandwidth is to increment the modulator's order, by including more zeros and poles [RKR15]. However, this tends to increase the modulator's critical path, which means that lower sampling frequencies are achieved. Furthermore, instability problems may also appear [ST05].

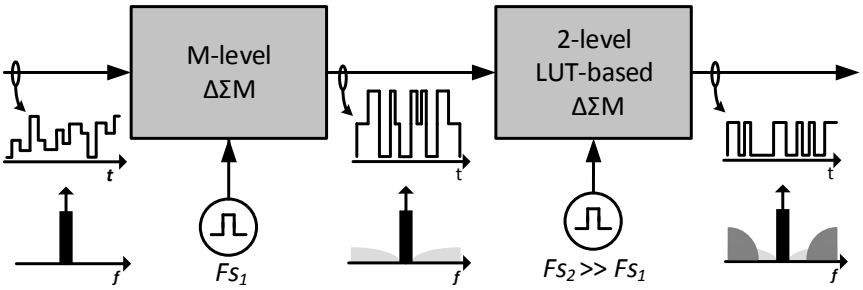

Figure 3.1: Conceptual idea of the proposed architecture.

3.2 Proposed Architecture

In this work, to relax the analog filtering requirements, the use of a cascaded 2-stage ΔΣ architecture with different quantization levels and sampling frequencies is proposed. As the modulator's order of each modulator is maintained, stability and critical path issues are no longer a problem.

The cascaded ΔΣM equivalents involve the same architecture divided into two modulators: a multi-bit modulator, followed by a faster single-bit ΔΣM. The illustration of this conceptual idea is depicted in Figure 3.1. On the one hand, the use of a multi-bit modulator as a first stage results in lower quantization noise. In fact, the quantization noise decreases by 6 dB for each added bit to the quantizer [ST05]. On the other hand, the ΔΣM NTF's processing bandwidth is proportional to the sampling rate. Thus, a faster 1-bit modulator as the last stage implies that the BB signal together with the low quantization noise generated by the first modulator around the signal carrier will be transmitted with less distortion, alleviating the analog filter's constraints. Nonetheless, the apparent simplicity of this concept masks the fact that the design of modulators with higher sampling rates is quite challenging. This difficulty stems from the fact that the sampling rate is inversely proportional to the maximum critical path. As pipeline stages can not be introduced in ΔΣM, under penalty of corrupting the transfer functions, the sampling rates are always bounded by the system designer's expertise and by the technological process.

For the purpose of this proof-of-concept, the chosen architectural solution for the last stage relied on the use of LUT-based approximations to ΔΣMs, as proposed in [RHP$^+$07]. These, try to emulate the typical ΔΣM's behavior using offline-computed LUTs, avoiding feedback loops, with the inherently gains in terms of sampling rates. However, the modulator's finite memory imposes several discontinuities in the output signal, worsening FoMs, such as the in-band signal integrity. These discontinuities will affect the performance of the modulator, but as will be seen, the effect in the FoM will not be so dominant.

Another drawback arising from the use of LUTs (either in ΔΣM or in PWM) are the spurious tones that tend to corrupt all the spectrum in well-defined frequencies. This appears due to the implicit determinism in the chosen patterns that are transmitted.

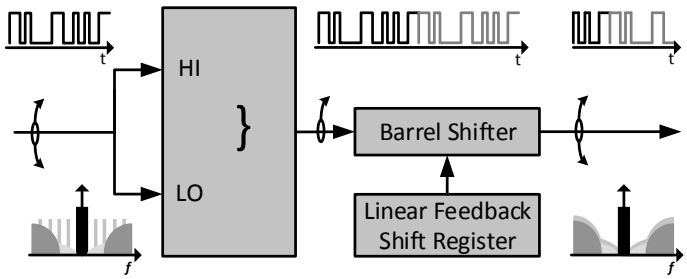

Figure 3.2: Illustration of the implemented dithering mechanism.

To overcome this issue, a methodology similar to the one proposed in [SOC13b] for PWM randomization is followed, to smooth the spurious out using dithering. The underlying idea is the random circular shifting of each LUT's output word. In this way, the energy of each word is maintained without the deterministic pattern, spreading the spurious tones' energy across the out-of-band spectrum. To accomplish this in a practical way, a 20-bit Linear Feedback Shift Register (LFSR) was connected to a Pipelined Barrel-Shifter Module. The block diagram is depicted in Figure 3.2. The incoming data is concatenated with itself, generating a word with the double of the input length. Then, it is forwarded to the Pipelined Barrel-Shifter Module that shifts the data word by a specified number of bits. The number of bits is in the range of 0 to the length of the input data and is given by the LFSR.

Overall, it may be said that the first stage provides an adequate SNR and reduces the number of output combinations. The second stage should be as fast as possible to relax the analog filtering requirements. The maximum achievable bandwidth is imposed by the combination between the two stages, but most dominantly, by the quantization noise imposed by the first stage.

3.3 Prototype Validation

To demonstrate the potential and flexibility of the proposed design, two different cascaded $\Delta\Sigma$Ms and a conventional single-stage modulator were embedded into a single FPGA. The block diagram is depicted in Figure 3.3. In the cascaded topologies, 11 (2.8 bit) and 101 (6.65 bit) quantization levels are used at the first modulator, defining the LUT's depth of the second stage. As the typical input values from the baseband I/Q samples have 10 bit, it was decided to choose these values to uniformly cover the range from 1 to 10 bits.

The samples are continuously transmitted from the BB Interface to the different modulators. Thereafter, they are combined and replicated by the *Select&Combine* module to generate a parallel output word that contains the four components $[I, \overline{Q}, Q, \overline{I}]$ and inverted versions) of the desired signal. This output word is transmitted by the MGT. The LUT-based Low-Pass Delta-Sigma Modulator (LP-$\Delta\Sigma$M) has an equivalent sampling rate equal to the MGT's bit-rate.

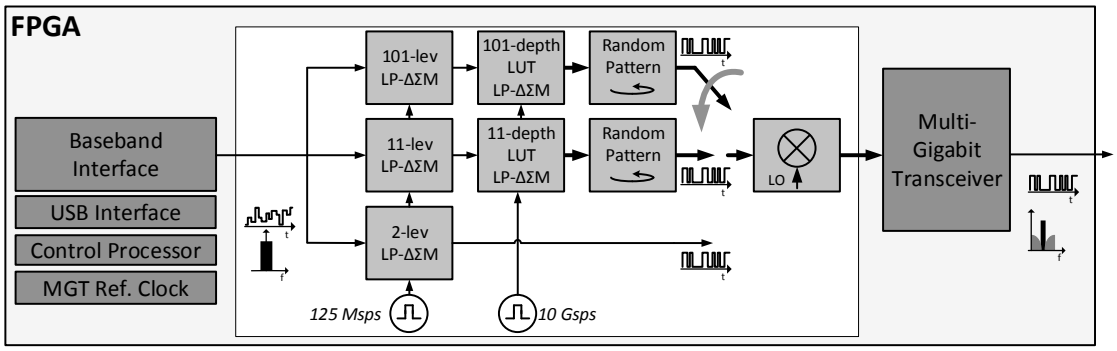

Figure 3.3: Block diagram of the implemented All-Digital Transmitter used to explore different combinations of cascaded modulators (conventional single-stage [*2-lev*], cascaded with 11 levels at the first stage [*11-lev*] and with 101 levels [*101-lev*]).

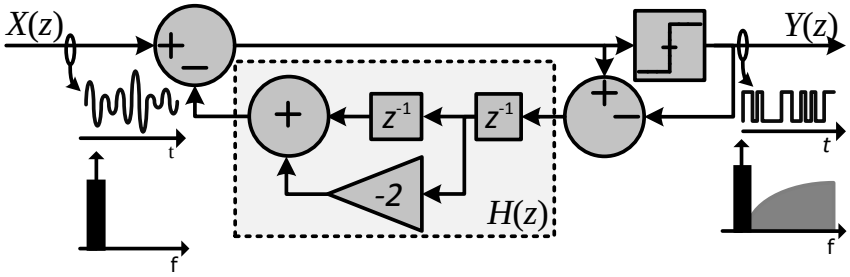

Figure 3.4: Representation in z-domain of the single-bit LP-ΔΣM.

The implemented LP-ΔΣM is based on an Error-feedback structure. It was chosen due to its short critical path, leading to higher sampling rates. Its block diagram is shown in Figure 3.4. The modulator's transfer function can be computed by modeling the quantizer by a noise source ($E_q(z)$):

$$Y(z) = STF(z)X(z) - NTF(z)E_q(z) \tag{3.1}$$

where $STF(z) = 1$ and $NTF(z) = 1 - 2z^{-1} + z^{-2}$. This NTF is a high-pass filter, resulting in a ΔΣM with a low-pass response.

The same modulator was used for the generation of the LUT's bitmap. In particular, the ΔΣM processes each input word, whose result is written in the respective LUT row. The offline generated LUTs are depicted in Figure 3.5.

To validate the proposed idea, an ADT was fully implemented into a Virtex Ultrascale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. The experimental setup is depicted in Figure 3.6.

The MGT line rate was configured to 10 Gbps to obtain a carrier frequency at 2.5 GHz, and was then connected to the Vector Signal Analyzer (VSA) R&S FSW 8 for signal analysis and demodulation. In particular, spectrum and EVM measurements were obtained for the

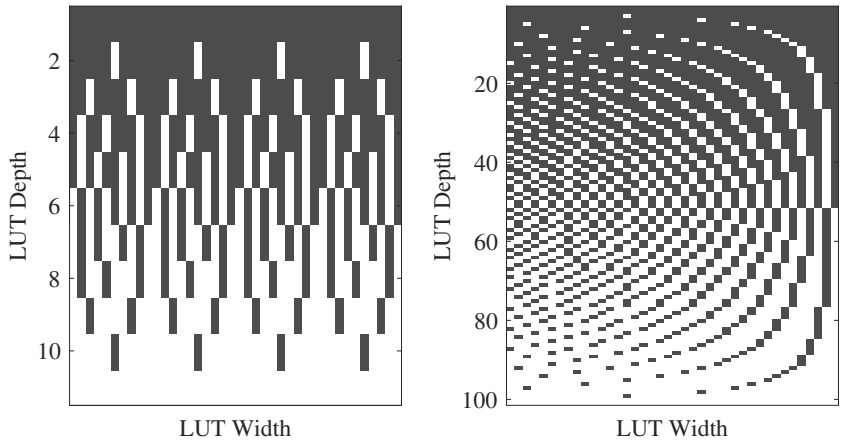

Figure 3.5: ΔΣMs LUT bitmap representations, with 11 (left) and 101 levels (right).

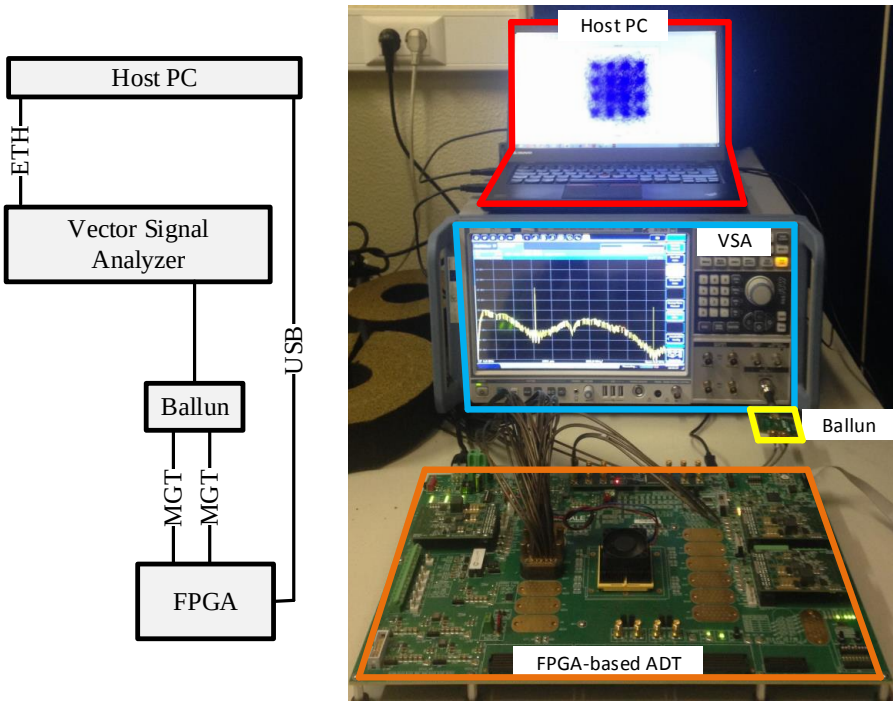

Figure 3.6: Photo of the experimental setup.

three architectures: the *2-lev*, the *11-lev* and the *101-lev*.

The obtained spectra illustrating the difference between the conventional and the proposed architectures are shown in Figure 3.7, where a 16-Quadrature Amplitude Modulation (QAM) was transmitted with a Symbol Rate (SR) of 3.125 Msps. It can be concluded that for the proposed modulators, the LUT's NTF has a large notch which preserves the BB signal together with the quantization noise (around the signal) from the first stage. Thus, the higher the number of levels in the first stage, the lower the analog filtering requirements will be.

The importance of dithering in the output spectrum is depicted in Figure 3.8. The pattern

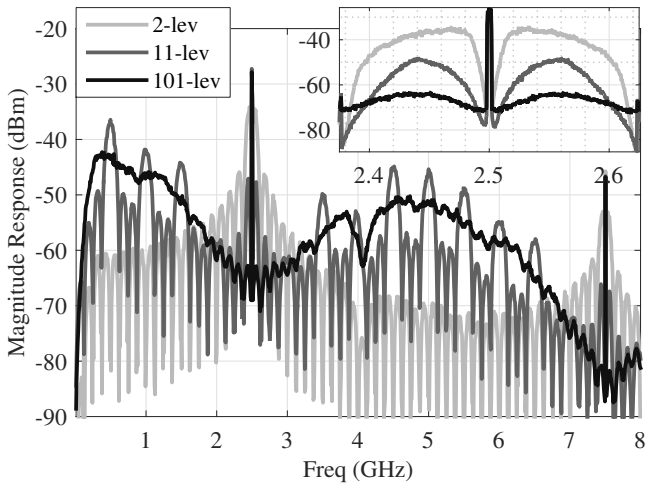

Figure 3.7: Comparison between the different spectra: single-stage *2-lev*, cascaded *11-lev* and cascaded *101-lev*.

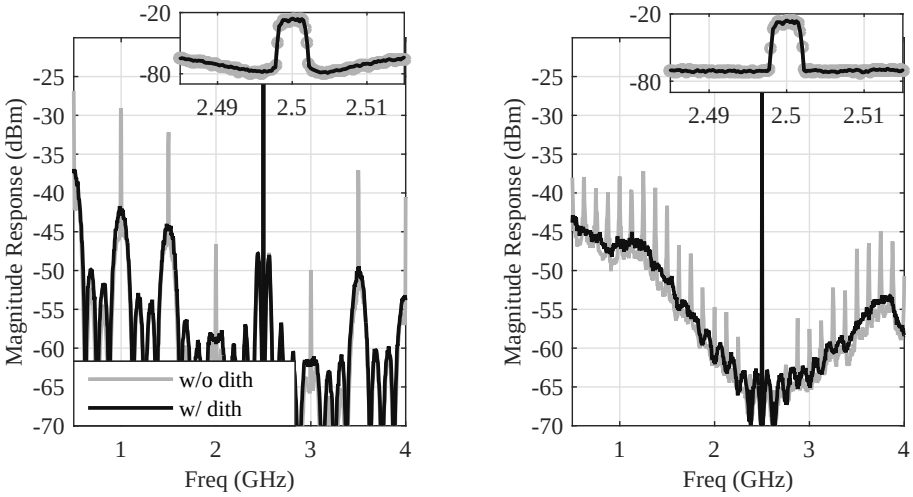

Figure 3.8: Impact of pattern randomization (dithering) in the spectrum: cascaded with *11-lev* (left) and with *101-lev* (right).

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randomization effectively removes the spurious tones, with an inherently increase in the noise floor, but with no degradation of the in-band signal's integrity.

Table 3.1 summarizes the comparison between the conventional LP-$\Delta\Sigma$M and the two cascaded modulators. Different SRs were tested, with a 16-QAM signal. As can be seen, by reducing the quantization noise around the carrier frequency, higher bandwidths can be accommodated and demodulated in the same spectral notches, which is another advantage arising from the proposed architecture. In particular, all the experimental results present EVM values below 3.3%, even for the case of 31.25 Msps (37.5 MHz of signal's bandwidth).

At last, the occupied resources for both the architectures are presented in Table 3.2. The major conclusion that can be derived is that the increase in hardware complexity for choosing

Table 3.1
Comparison between a single-stage *2-lev* vs two cascaded modulators with dithering, with a 16-QAM signal. Symbol rate is in Msps, EVM in % and MER in dB.

	Conventional		11 Levels		101 Levels	
SRate	EVM	MER	EVM	MER	EVM	MER
3.125	1.08	39.3	0.96	40.3	1.10	38.5
6.25	1.35	37.3	1.18	38.5	1.46	36.7
12.5	4.53	26.8	2.04	33.8	2.37	32.5
15.625	7.78	22.1	2.46	32.2	2.84	30.9
31.25	n/a	n/a	2.94	30.6	3.30	29.5

Table 3.2
Comparison between the different ΔΣM occupied resources: the single-stage *2-lev*, the cascaded *11-lev* and the cascaded *101-lev*.

		Conventional		11 Levels		101 Levels	
Logic Resources	Total	Used	%	Used	%	Used	%
Flip Flops	1075200	261	0.02	1519	0.14	1519	0.14
LUTs	537600	328	0.06	1235	0.23	4286	0.80
Memory LUT	76800	141	0.18	167	0.22	167	0.22
GTHs	28	1	3.57	1	3.57	1	3.57

the cascaded ΔΣMs instead of the conventional one is almost negligible, even if considering the specifications from the low-/mid-range FPGAs's available in the market.

3.4 Summary and Concluding Remarks

In this chapter, a novel architecture based on cascading two ΔΣMs with different sampling frequencies and quantization levels was presented as a possible core for the development of novel BB-stage ADTs. It was shown that instead of designing a pulse encoder based on a single-stage 1-bit LP-ΔΣM, the system's FoMs are greatly improved if a cascaded 2-stage ΔΣM architecture is chosen instead. In particular, the quantization noise near the transmitted carrier frequency can be highly reduced, avoiding the need for a high-quality factor analog output filter.

This novel concept has been successfully implemented and validated on an FPGA-based transmitter and compared with the conventional architectures that perform a single-bit quantization into a single stage. The proposed technique is fairly simple and requires just minor changes in the modulator's hardware.

All the experimental results attest the validity of the proposed architecture and clearly demonstrate that the RF reconstruction filter's quality factor requirements can be relaxed with just minor modifications in the hardware. Moreover, the proposed technique is com-

pletely independent of the modulator's topology, and thus, stability and critical path issues are no longer a concern. At last, even though LUT-based $\Delta\Sigma$Ms were used in this proof-of-concept, another type of modulators can be used. To effectively take advantage of this proposed architecture, the focus should always be in increasing the sampling rate of the cascaded modulator's last stage. That, together with the number of output levels from the first stage, will dictate the final output spectrum's shape, and, therefore, the analog filtering constraints.

The next chapter will introduce an innovative architecture that takes advantage of the integration and flexibility capabilities of the All-Digital RF Transmission to leverage the design of low-complex and highly-integrated RF front-ends for Antenna Arrays.

Chapter 4

All-Digital Antenna Array Transmitters

Outline

Both scientific and industrial communities have been putting significant efforts in the development of novel antenna technologies where antenna arrays are their core system, with integration and massification being the underlying watchwords. However, it is widely known that even though the vast opportunities that massive antenna arrays enable, several issues such as complexity, cost and energy efficiency become particularly problematic. Thus, in this chapter, this research line is addressed and a promising architecture for the design of scalable and fully integrated RF front-ends for antenna arrays is proposed.

This chapter is supported by the conference paper [DOV17a] and by the journal [DOV]. The chapter presents a BB-stage ADT architecture that combines eight independent ADTs to perform the direct driving of an antenna array. By removing the need for external DACs and external upconversion stages, the reported solution presents a high-level of scalability.

4.1 Contextualization

The typical design methodology of an antenna array involves the integration of M dedicated RF front-ends to interface with M radiating elements. However, this leads to heavy, bulky and complex systems, which, ultimately, precludes the integration of a massive number of RF front-ends. The use of a single RF front-end with multiplexing techniques [Time-Division Multiplexing (TDM) and Code-Division Multiplexing (CDM)] has been proposed by some authors [MG11, VPA$^+$17]. However, these techniques show a limited available bandwidth, high noise levels, and an increased system complexity [MG11]. Other alternatives propose the use of hybrid beamforming architectures for the design of large-scale antenna arrays [HlIXR15, SY16]. The aim is to reduce the number of RF chains without decreas-

ing the beamforming gains. However, even though some design requirements are relaxed, there is a higher system complexity to design and conveniently operate the digital and analog beamformers in a proper way.

4.2 Proposed Architecture

The proposed idea falls into the exploration of reconfigurable all digital transmitters integrated into a single FPGA to implement antenna array systems with massive number of elements: the concept of All-Digital Antenna Array Transmitter (ADAAT). The high number of FPGA's Input-Output (IO) pins jointly with the FPGA-based reconfigurable all-digital transmitters techniques can be explored for, together with miniaturized antennas and band-pass filters, implementing scalable and compact massive antenna array transmitters. The target is to minimize the number of external components, and taking into account the relevant literature, one can verify that the FPGA's resource utilization factor to implement an ADT is usually very low [SOC13b]. Therefore, as far as the scalability is concerned, there are enough logic resources to include more stages in the digital datapath. In particular, the main objective is to minimize the beamforming's network inherent complexity, maximizing the digital physical subsystems that are built-in into a single FPGA. In addition to the appealing scenario of having the majority of the chains integrated into a single chip, the potential of having software defined antenna array transmitters is very promising and may be a key to enable a seamless migration path for the future large-scale antenna arrays.

The conceptual model of this ADAAT is depicted in Figure 4.1 and intends to demonstrate the physical interaction between all the subsystems in the final system.

4.2.1 Block Diagram

The general block diagram is depicted in Figure 4.2, and one can see that it is based on the parallelization of multiple ADTs.

The system comprises M independent ADTs, each one performing the direct driving of a single radiating element. In addition to the typical ADT subsystems, a new one was included: the *G/ϕ Tuning* module. This module works in low sampling rates and is responsible for performing the amplitude scaling as well as the BB phase shifting of each ADT's output. Its core (depicted in Figure 4.3) is based on two digital gain blocks and a COordinate Rotation DIgital Computer (CORDIC) in rotation mode. The two modules have different functionalities. On the one hand, the digital gain blocks enable an inter-lane amplitude calibration, as well as the amplitude scaling of each radiant element in real-time. On the other hand, the CORDIC enables the inter-lane phase calibration, as well as the phase shifting of each radiant element, also in real-time. This real-time reconfigurability is essential to enable the inclusion of beamsteering algorithms. It must be highlighted that for the transmission of

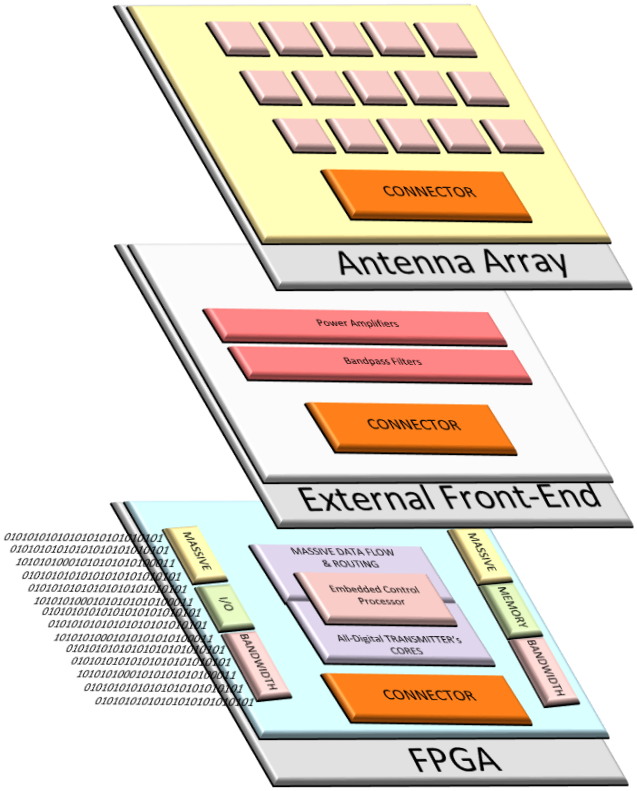

Figure 4.1: Conceptual model for the ADAAT.

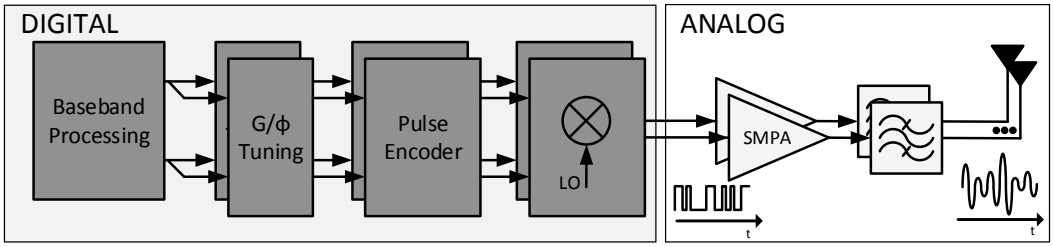

Figure 4.2: Conceptual block diagram of an ADAAT.

wide bandwidths, the narrowband assumption is no longer valid, and the CORDIC must be changed to a digital filter.

4.2.2 Calibration Procedure

The existence of a calibration procedure for this type of system is mandatory due to the inherent timing mismatches between the different MGT lanes worsened by the different cables, connectors and other components with different electrical lengths. In addition to that, all the transceivers' output power must also be equivalent to avoid unbalances.

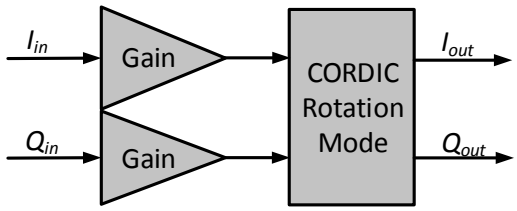

Figure 4.3: Block diagram of the digital *G/ϕ Tuning* module.

Phase Calibration

For the sake of simplicity, one can restrain the chosen calibration procedure to just two elements before moving to the M elements, and one can also consider the continuous time domain. If a low-frequency complex exponential tone ($x(t) = e^{j(\omega_{IF}t)}$) feeds two ADTs, after being modulated by the LP-ΔΣMs and upconverted to a given RF frequency, the two outputs will be $y_1 = Ae^{j(\omega_{RF}t+\phi)} + n_1(t)$ and $y_2 = Be^{j(\omega_{RF}t+\theta)} + n_2(t)$, where ϕ and θ are the phase deviation specific to each transmitter, A and B represent some gain/attenuation inherent to the DUC, and $n_1(t)$ and $n_2(t)$ are the quantization noise generated by the respective modulators. For this analysis, A and B can be ignored, as well as the out-of-band noise due to the noise-shaping property. Thus, the combination of the two outputs can be simply expressed as $y \simeq e^{j(\omega_{RF}t+\phi)} + e^{j(\omega_{RF}t+\theta)} = 2\cos\left((\phi-\theta)/2\right)e^{j(\phi+\theta)/2}e^{j\omega_{RF}t}$. Taking into account that the maximum magnitude occurs for $\theta = \phi$, an indirect procedure to estimate the phase deviation between two lanes could rely on performing a phase sweep in one of the BB incoming signals, while monitoring the output power in the bins of interest. Moreover, as the output waveform is *a priori* known, the curve fitting can be done with just a few iterations, which decreases the calibration time.

An external M to 1 power combiner can be used to accommodate the M MGTs. Even though all the outputs are directly connected, just two can be turned on at the same time, and one of them must be used as reference to ensure a relative calibration. Without loss of generality, by considering the first port as the reference, the result is: $e = \begin{bmatrix} 0 & p_{12} & \dots & p_{1M} \end{bmatrix}$, where each variable represents the estimated phases between each two lanes. After all the power combiner's phase unbalances are characterized in the Vector Network Analyzer $\left(c = \begin{bmatrix} p_{1s} & p_{2s} & \dots & p_{Ms} \end{bmatrix}\right)$, each CORDIC reference input must be updated according to: $p = (e - c)\,\%\,2\pi$. A flowchart summarizing the implemented phase calibration method is depicted in Figure 4.4.

Magnitude Calibration

The most straightforward way to correct the amplitudes mismatches, without external amplification circuitry at RF, is to adjust the BB gain of each input signal. To ensure an automated calibration procedure, all the M MGT's outputs can be connected to a power

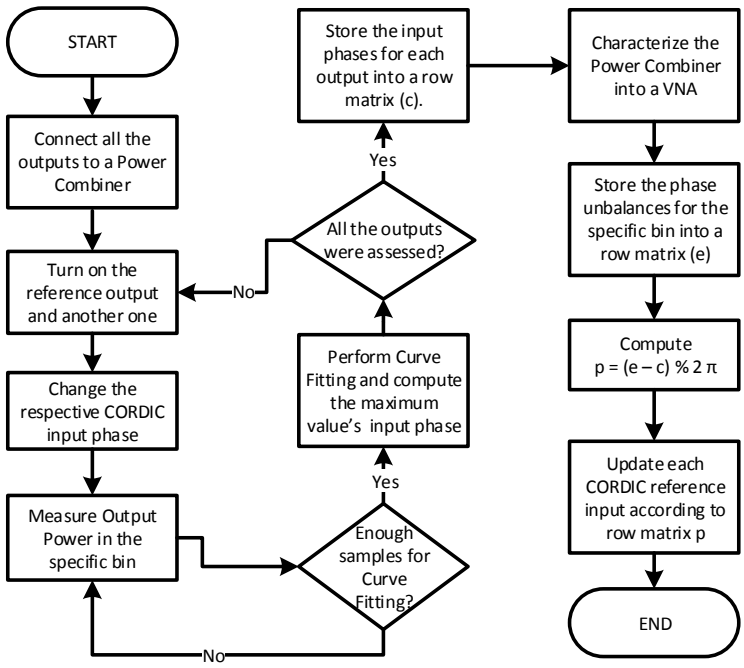

Figure 4.4: Flowchart of the implemented phase calibration method.

combiner and just one element can be turned on at each moment. After comparing the output power from each lane, a low-complex control loop can be implemented to attenuate all the BB input signals until the same output power is present in all the outputs. Depending on the case, the power combiner's insertion losses must also be assessed to verify if they are negligible or if their correction must be done in the digital domain. A flowchart summarizing the implemented magnitude calibration method is depicted in Figure 4.5.

4.3 Prototype Validation

To validate the proposed idea, the proposed block diagram from Figure 4.6 was fully implemented into a Virtex Ultrascale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. The experimental setup is depicted in Figure 4.7.

For the purpose of this proof-of-concept, eight independent ADTs are fully integrated into the same FPGA. Even though more elements could be included into the same FPGA, board interface limitations precluded the integration of more than eight elements.

After integrating the eight independent ADTs in the same FPGA, the BB test signals are stored in the FPGA's internal memory. Afterwards, the BB signals feed all the G/ϕ *Tuning* subsystems. After that, a Polyphase Interpolation FIR Filter increases the sampling rate by a factor of five, with the samples divided into five different branches. Therefore, the signals feed a polyphase equivalent 5-path LP-$\Delta\Sigma$M sampled at a clock frequency of

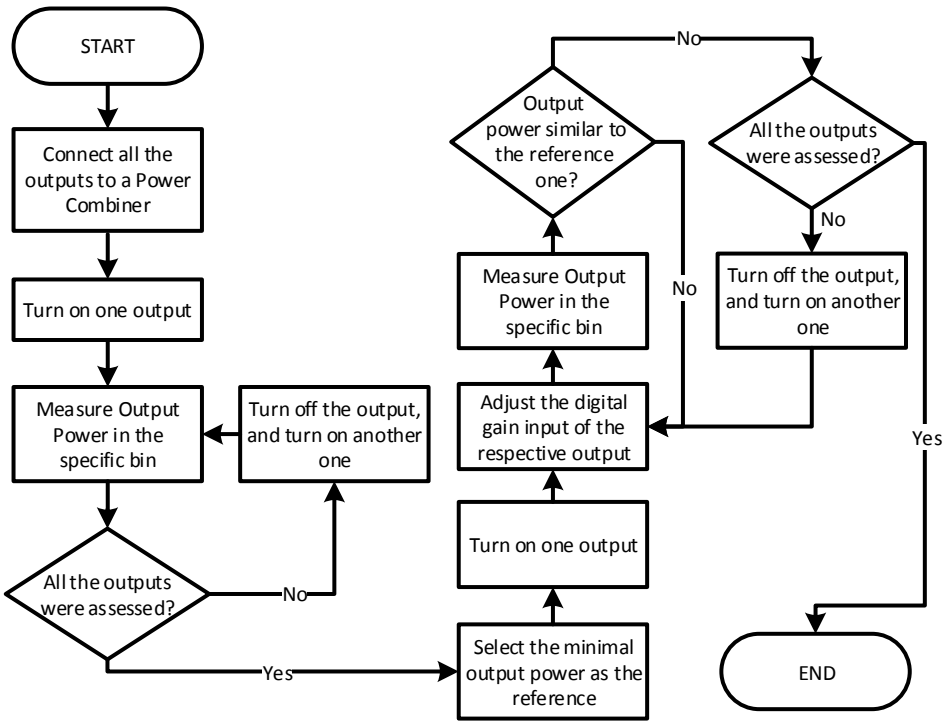

Figure 4.5: Flowchart of the implemented magnitude calibration method.

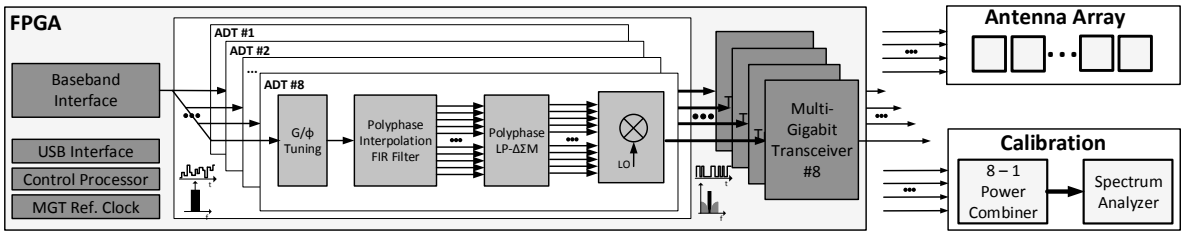

Figure 4.6: Block diagram of the implemented FPGA-based ADAAT.

125 MHz, resulting in a global sampling rate of 625 Msps. The polyphase equivalent ΔΣM was designed according to the theory discussed in [Vai93]. The choice of the five phases was done taking into account the trade-off between the number of phases and the overall critical path [COVS14]. As a ΔΣM contains a feedback loop, polyphase techniques may significantly impact the critical path. Thus, the number of paths must be chosen as a trade-off between global clock frequency and LP-ΔΣM's complexity. The chosen LP-ΔΣM is based on an error-feedback structure previously depicted in Figure 3.4.

As usual, the corresponding samples are then combined and replicated to generate a parallel output word with the four components of the RF signal ($x_I[n]$, $x_Q[n]$, and inverted versions), that is serialized by the FPGA's MGTs.

The calibration procedure introduced in the previous section was implemented. It must be highlighted that the proposed calibration procedure does not require extra modules/subsystems

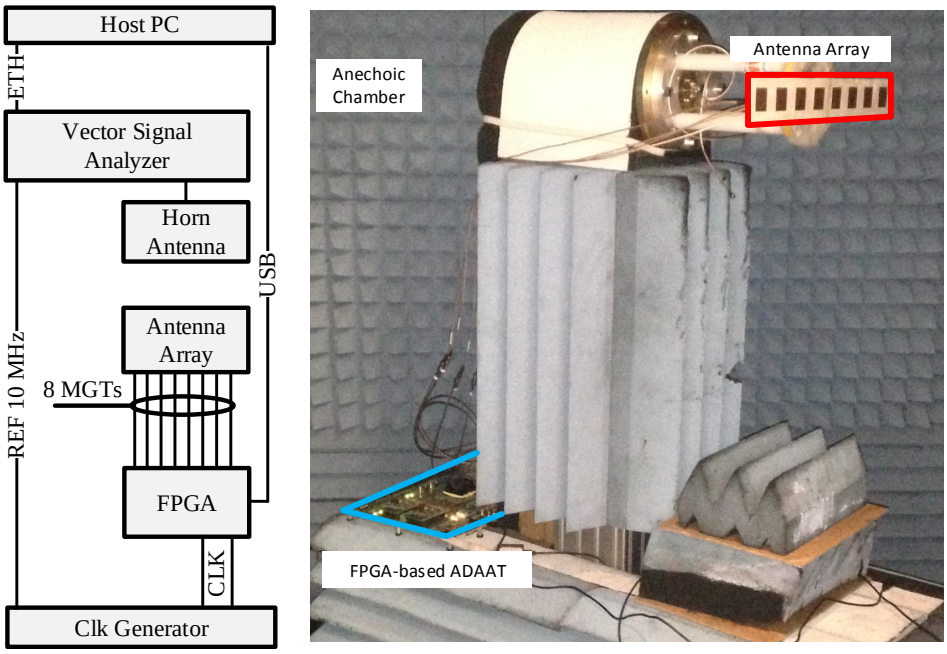

Figure 4.7: Experimental setup in the anechoic chamber: the ADAAT connected to one in-house developed linear 8-element microstrip patch antenna array.

apart from the ones that are already present in the design. In particular, the *G/ϕ Tuning* module is used for both the calibration procedure and for the beamsteering operation. The functionality of this module is controlled by the *Control Processor*. The Power Combiner was a ZN8PD1-53S+ from Mini-Circuits. It must be emphasized that, depending on the system's constraints, the inclusion of an external power combiner may not be convenient. Thus, the same calibration procedure was successfully validated in far-field conditions, within a controlled environment, with spatial power combination replacing the external power combiner. Regardless of the scenario, in the end, phase and magnitude calibrations were performed in a straightforward way, without the need for manual interaction.

All the measurements were performed in an anechoic chamber with a distance of four meters between the ADAAT (depicted in Figure 4.6b) and the horn measurement antenna (to ensure the far-field region). The ADAAT comprises an in-house developed 14.47 dBi linear 8-element microstrip patch antenna array matched for 2.5 GHz that was developed to demonstrate the capability to control the amplitude/phases of each transmitter in a real-life scenario. Connected to the measurement antenna is a VSA R&S FSW 8. In particular, two different experimental results were obtained:

- Radiation pattern diagrams based on peak gain measurements (Figures 4.8 and 4.9);
- Measured EVM and MER values for different symbol rates in different steering angles (Table 4.1).

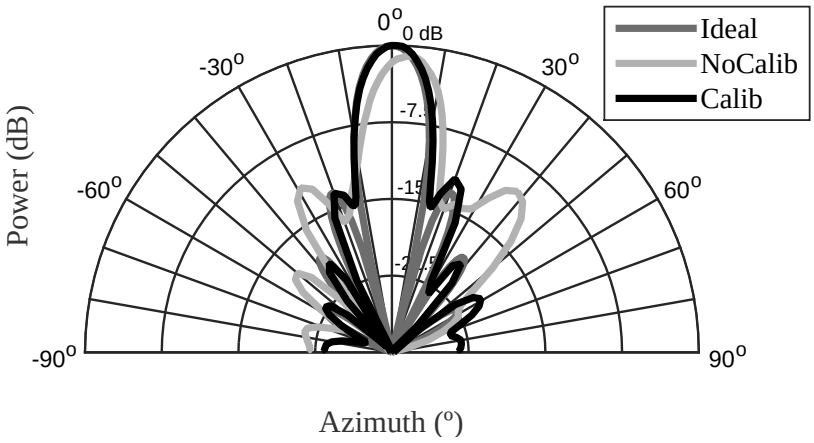

Figure 4.8: Impact of the calibration procedure in the radiation pattern.

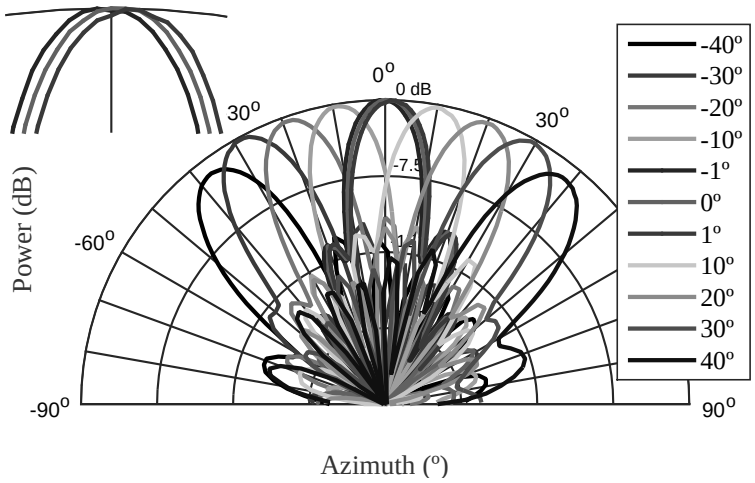

Figure 4.9: Normalized radiation patterns for different steering angles. The 1-degree resolution is shown in the left corner.

The calibration procedure is validated in Figure 4.8, where the measured radiation pattern matched the simulated one.

To assess the beamsteering capability, the typical progressive phase method with constant amplitude was applied, and each computed value updated the respective CORDIC phase value. Normalized radiation patterns are depicted in Figure 4.9 for azimuth angles in the range of -40° to 40° with emphasis on the 1° resolution. Due to the use of a 16-bit register for the CORDIC module, the authors believe that sub-degree resolution can be achieved. However, limitations in the measurement procedure precluded its experimental validation.

All experimental results present EVM values below 5% for a distance of 4 meters (without external amplification circuitry) which resulted in a well-defined constellation (Table 4.1). As usual, for higher symbol rates, the patches' available bandwidth (around 25 MHz assessed

Table 4.1
Measured performance with a 16-QAM in far-field (4 m). Symbol rate is in Msps, EVM in % and MER in dB.

	Steering Angles (°)							
	-40		-20		20		40	
SRate	EVM	MER	EVM	MER	EVM	MER	EVM	MER
3.125	1.93	34.4	1.63	35.7	1.67	35.6	1.92	34.4
7.8125	2.56	31.9	2.40	32.4	2.54	32.5	2.57	31.9
12.5	3.10	30.1	3.02	30.4	3.00	30.5	3.13	30.1
15.625	3.44	29.3	3.42	29.6	3.42	29.6	3.43	29.3
25	4.77	26.4	4.84	26.2	4.78	26.4	4.87	26.2

Table 4.2
ADAAT occupied resources.

Logic Resources	Used	Total	Percentage (%)
Flip Flops	30401	1075200	2.83
LUTs	23701	537600	4.41
Memory	256	1728	14.81
DSP	560	768	72.92
GTHs	8	28	28.57
GTYs	0	26	0

in the patch's S_{11} parameters) together with the LP-$\Delta\Sigma$M's processing bandwidth starts to worsen the signal integrity.

Table 4.2 reports the ADAAT resources usage. The higher percentage of resources ($\simeq$ 73% of DSP slices) is being used in the non-optimized polyphase interpolation FIR filters. However, this percentage can be lowered with resort to multiplier-less FIR, Cascaded Integrator-Comb (CIC) filters. In most cases, a simple average FIR filter can be used. This is one of the most resource-efficient topologies because no arithmetic operations are required. Thus, from a system designer's point-of-view, novel filtering methodologies should be followed in order to ensure the integration of more RF front-ends. Taking into account the used FPGA chip, the resources usage from the proposed implementation and an interpolation based on a ZOH (0% of DSP occupation), one can estimate that fifty-four parallel ADTs can be easily integrated into the same chip.

4.4 Summary and Concluding Remarks

In this chapter, a novel architecture for an FPGA-based All-Digital Antenna Array RF Transmitter was proposed and validated. In particular, eight complete digital-RF transmitters were optimized and integrated into the same FPGA.

The proposed concept presents a lower complexity than the state-of-the-art counterparts. By enabling the design of antenna array transmitters without external DACs and external upconversion stages, the overall system's layout can be highly simplified, and consequently, more radiating elements can be integrated.

This novel concept has been successfully implemented and validated on an FPGA-based transmitter. Radiation patterns and the transmission of modulated signals for different steering angles attest the validity of the proposed architecture.

The next chapter elaborates on the carrier agility research line, by proposing the first reported RF-stage ADT that can be embedded within a single FPGA device.

Chapter 5

Fully Agile Modulators

Outline

Real-time frequency agility is one of the key limitations of current ADTs. Thus, in this chapter, this research line is addressed and a promising architecture is proposed.

This chapter is supported by the journal article [DCO+18]. In particular, the chapter proposes a fully parallel and digital architecture that can be embedded into an FPGA. This architecture was the first one reported to enable the design of RF-stage modulators within an FPGA.

5.1 Contextualization

Wideband frequency agility requires a high sampling rate at the pulse encoder, and only RF-stage modulators can claim it. These sampling rates must be at least twice the desired carrier frequency. As the programmable logic subsystems from the FPGAs have a limited sampling rate (typically below 300 MHz), the SoA was unanimous to assume that FPGAs were not suitable to design RF-stage modulators. Thus, all the ADT techniques from the SoA fall in the implementation of BB-stage modulators, by placing the DUC stage after the Pulse Encoder [COVS16, THTK17, MYHF17]. As aforementioned, this specific DUC is entangled to the serializer's sampling rate. Thus, the frequency agility in those architectures is only accomplished through the real-time reconfiguration of the serializers, which, as introduced in 2.2.4, may jeopardize the overall FoM.

5.2 Proposed Architecture

In order to embed an RF-stage modulator into an FPGA, the proposed idea falls into the exploration of highly-parallelized architectures. In these architectures, aggregated high-sampling rates are possible while maintaining lower individual sampling rates. Thus, as a

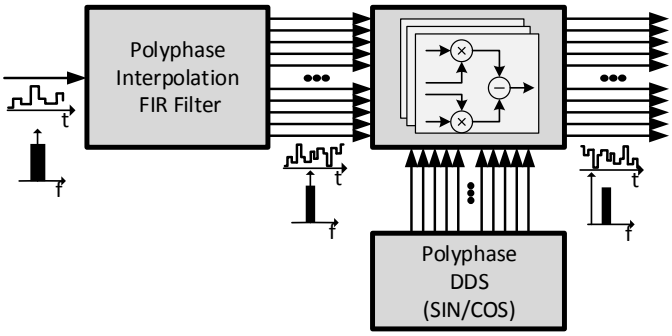

Figure 5.1: Block diagram of the proposed DUC.

high global sampling rate at the pulse encoder can be maintained, the RF waveforms can be synthesized in the digital domain before the pulse encoder, and unprecedented frequency agility can be achieved.

5.2.1 Digital Upconversion Stage

To ensure a high level of carrier agility, the signal must be upconverted before the pulse encoding.

Considering the strict timing constraints of the commercial FPGAs, common digital circuits designed within the programmable logic can typically be clocked up to 300 MHz. Due to this, a single-rate upconversion from BB up to the RF stage is not a feasible option. To overcome this limitation, multi-rate techniques were applied to the DUC stage. In particular, a polyphase equivalent is designed with N different paths to achieve a global sampling frequency N times higher than the BB sampling rates.

The proposed DUC is depicted in Figure 5.1 and consists of a polyphase interpolation FIR filter, a polyphase I/Q DDS, working as a digital LO, and parallel digital mixers. The polyphase interpolation FIR filter increases the sampling rate of the BB signal from Fs_{BB} to Fs_{RF}, while dividing the samples in N different phases [Vai93]. The polyphase I/Q DDS is the core of this DUC stage and is illustrated in Figure 5.2. In view of the aforementioned FPGA's timing constraints, a classic single-rate DDS can not be used in this particular case, because it is not possible to achieve a sampling rate equal to the serializer's sampling frequency (Fs_{RF}). To overcome this problem, a polyphase equivalent was designed. Since the DDS is a feedforward system, polyphase techniques do not significantly impact the critical path. In its essence, it combines N conventional and single-rate DDS modules. Each DDS has a specific phase accumulator and two Read-Only Memories (ROMs) containing the sine and the cosine waveforms. The DDS modules work in parallel to simultaneously generate N samples of the required carrier frequency (ω_c) waveform. Each of the DDS is actually working at a rate N times lower than the equivalent global sampling rate. Thus, it is possible to achieve a global sampling rate equal to the serializers sampling frequency Fs_{RF} with N different phases being

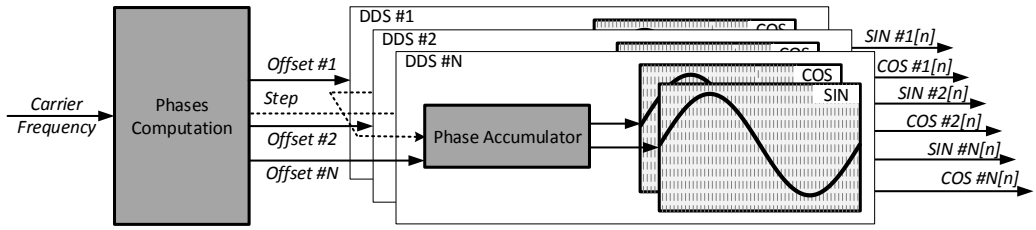

Figure 5.2: Functional block diagram of the polyphase DDS module.

clocked at Fs_{BB}. The Phase Computation block, depicted in the same figure, performs the mapping between the desired carrier frequency, the phase step, and the respective DDS phase offset. The minimum frequency resolution (Δf) is computed as in the classical single-rate DDS, but now with a sampling rate N times higher:

$$\Delta f = \frac{Fs_{BB}\,N}{2^L} = \frac{Fs_{RF}}{2^L} \tag{5.1}$$

where L is the number of bits from each phase accumulator. The last module of the proposed DUC is a digital mixer, which performs the element-wise multiplication and subtraction between the interpolated samples and the different samples from the cosine and sine waveforms, according to (2.10).

It is worth mentioning a few notes regarding the efficient design of the polyphase DDS modules. The block diagram of Figure 5.2 aims to provide a simplistic and conceptual overview of the polyphase DDS. However, depending on the system requirements, several optimization techniques and novel subsystems could be included. For instance, efficient memory usage can be achieved by exploiting the symmetry of sinusoidal waveforms. Interpolation or phase dithering can also be applied to increase the Spurious-Free Dynamic Range (SFDR). Moreover, the required SFDR is also dependent on the system application, as well as on the pulse encoding mechanism. In fact, generally speaking, the SFDR will be imposed by the pulse encoding mechanism which will generate a substantially higher amount of noise than the DDS. These optimization techniques are typically embedded into the DDS Intellectual Property (IP) cores from the FPGA's vendors [Xil15]. For this reason, their implementation is out of the scope of this work.

5.2.2 RF Pulse Encoder

To validate the proposed architecture, an RF Pulse Encoder to perform the single-bit quantization must be designed and integrated after the DUC. This RF Pulse Encoder must be embedded into an FPGA, with no specialized application-specific circuit-level techniques. In this sense, the two next subsections will address this topic, and two parallel architectures will be proposed and implemented: a quadrature RF-PWM and a tunable RF-$\Delta\Sigma$M.

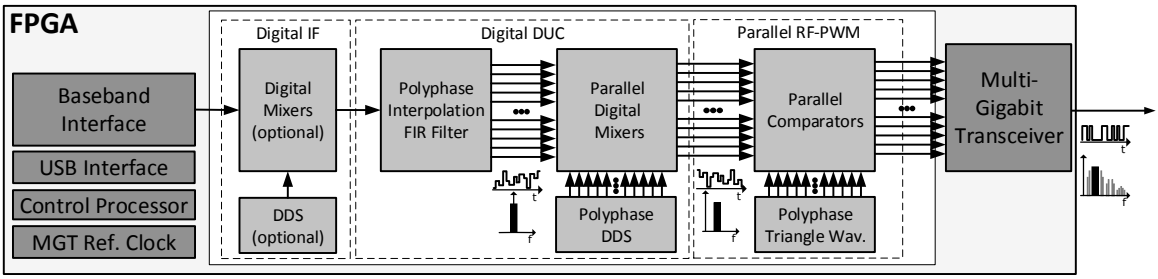

Figure 5.3: Block diagram of the implemented FPGA-based RF-PWM Digital Transmitter.

RF-PWM Architecture

The design proposed in this work is based on the traditional PWM generation mechanism, introduced in Section 2.2.3. Nonetheless, instead of synthesizing the two signals ($x[n]$ and $r[n]$) at low sampling frequencies (Fs_{BB}) (as performed in the literature [RAM12]), the signals are generated in a multi-rate approach with a global sampling frequency of Fs_{RF}. In addition to this, the reference waveform's frequency F_{ref} is lower than the RF carrier frequency, but higher than the signal's bandwidth (at least twice the bandwidth). An optimization procedure in the frequency of the reference waveform must be done to ensure a clean spectrum in the band of interest. To guarantee a global sampling frequency of Fs_{RF}, this reference waveform is also synthesized using a polyphase DDS with N different phases (using a triangular waveform stored in the Read-Only Memory (ROM)).

The overall architecture is illustrated in Figure 5.3. For the purpose of this proof-of-concept, the BB samples are continuously transmitted from the Baseband Interface to the Polyphase Interpolation FIR filter. This module increases the sampling rate by a factor of N, distributed into N different phases, which are then upconverted according to (2.10). The frequency resolution from the whole modulator is given by (5.1). However, depending on the system requirements, a fine frequency resolution may be needed. While increasing the phase accumulators' resolution seems to be the most intuitive way to accomplish this, it leads to an unnecessary level of high resources usage. To avoid this, a single-rate Digital-IF can be included together with a high-resolution DDS before the Polyphase Interpolation FIR filter, as depicted in Figure 5.3. In this way, the resolution of the phase accumulators from the polyphase DDS can be significantly reduced, leading to savings in the memory-primitive resources usage, while the single-rate digital-IF provides the fine frequency resolution. The trade-off is the bandwidth of the Polyphase Interpolation FIR filter, which must accommodate the IF-modulated signal.

After having the desired signal interpolated and upconverted to a given carrier frequency, it will be directly compared with the reference waveform, according to:

$$y_{RF}[n] = sign(r[n] - x_{RF}[n]) \tag{5.2}$$

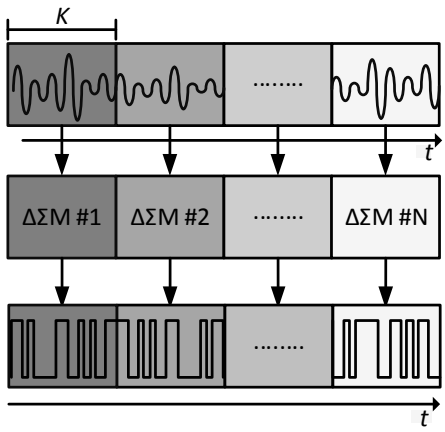

Figure 5.4: Illustration of the multicore ΔΣ modulators proposed in [COVS16].

At last, the resultant 1-bit signals from each branch are concatenated to generate a parallel output word that will be serialized by the MGT, running at Fs_{RF}.

RF-ΔΣM Architecture

One of the main advantages from the use of ΔΣM is the inherent noise shaping that preserves the in-band integrity. Thus, there is a strong motivation for the design of a parallel RF-ΔΣ architecture. The architecture proposed in this work relies on the replication and combination of multiple ΔΣ modulator cores running in parallel, as proposed in [COVS16]. However, instead of modulating an incoming BB signal, several tunable bandpass modulators are included in parallel to enable the encoding of an upconverted RF signal, with a global sampling frequency equal to Fs_{RF}.

This multicore-based architecture is chosen because, up to now, it is the closest approach to an ideal parallel representation of a ΔΣ modulator. The underlying idea is illustrated in the Figure 5.4 and is based on slicing the input signal in blocks of size K that will feed each of the N modulators in parallel. Even though all the modulators are running at a lower clock, the resultant behavior approaches the ideal modulator running at a global sampling frequency N times higher. In addition to that, in a careful design, the resultant critical path (that binds the maximum global sampling rate) is imposed by the modulator itself, and not by the system as a whole. This is of paramount importance to achieve higher sampling rate gains. To implement such architecture, two new subsystems - Deinterleaving and Interleaving modules - were introduced. A graphical illustration of the Deinterleaving and the Interleaving modules is depicted in Figure 5.5. As the temporal progression in a multi-rate system unrolls between the different phases every clock tick, the Deinterleaving module is required to re-arrange the incoming samples in order to force the temporal continuity within each phase. This is of paramount importance to make sure that the ΔΣMs cores are processing contiguous samples. The Interleaving module is in charge of performing the inverse operation: to convert

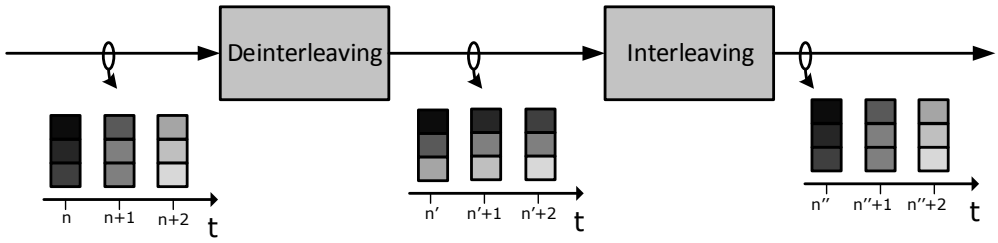

Figure 5.5: Graphical illustration of the Deinterleaving/Interleaving functions for the case of $N = 3$ phases and $K = 3$ samples. In the case of N equal to K, one can see that the Deinterleaving/Interleaving modules are simply matrix transposers. In the figure, n' and n'' refer to the clock instant $n + L$, where L is the latency of each module.

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from a temporal continuity within a phase to a temporal continuity between different phases.

Nonetheless, it must be pointed out that this is not an error-free architecture, because the discontinuities caused in every K samples degrade the system's performance. Hence, the higher this value is, the better will be the modulators FoM. However, this increases the amount of resources required to temporarily store all the samples in the Deinterleaving/Interleaving modules.

The overall architecture is illustrated in Figure 5.7, and as can be seen, the block diagram is quite similar to the RF-PWM case (Figure 5.3). The main difference is the last stage, the RF Pulse Encoder, that is based on multicore $\Delta\Sigma$ modulators. In particular, Deinterleaving and Interleaving modules must be designed to accommodate and re-arrange the input/output data from N tunable bandpass $\Delta\Sigma$ modulators. Similar to the RF-PWM case, the resultant 1-bit signals from all phases are concatenated to generate a parallel word that will be serialized by the MGT, running at Fs_{RF}.

Focusing on the $\Delta\Sigma$ topology, the design has fallen in the Error-feedback structure, whose illustration is depicted in Figure 5.6. This architecture presents a high level of simplicity, stability and has a short critical path, which eases the process of implementation as well as leverages the use of higher sampling rates. Modeling the quantizer by a noise source ($E_q(z)$), one can derive:

$$\begin{aligned} Y(z) &= X(z) - (1 + H(z))E_q(z) \\ &= STF(z)X(z) - NTF(z)E_q(z) \end{aligned} \tag{5.3}$$

where $STF(z) = 1$, $NTF(z) = (1 + H(z))$ and $H(z) = \alpha z^{-1} + z^{-2}$. To determine the range of the gain α, the frequency response's magnitude of the transfer function must be assessed, which can be easily done by evaluating the $NTF(z)$ on the unit circle, $z = e^{j\theta}$.

$$\begin{aligned} |NTF(e^{j\theta})| &= |1 + \alpha e^{-j\theta} + e^{-2j\theta}| \\ &= |2\cos(\theta) + \alpha| \end{aligned} \tag{5.4}$$

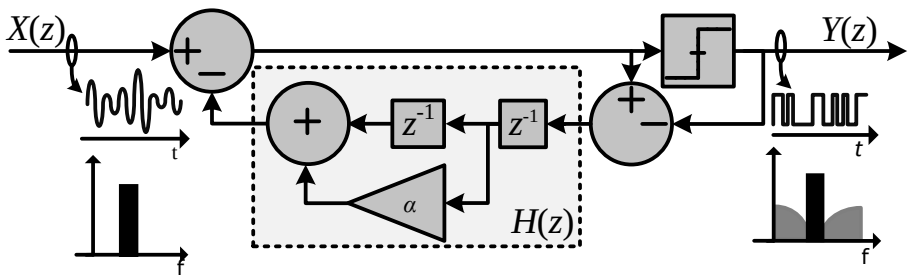

Figure 5.6: Z-domain representation of the tunable Error-feedback ΔΣM.

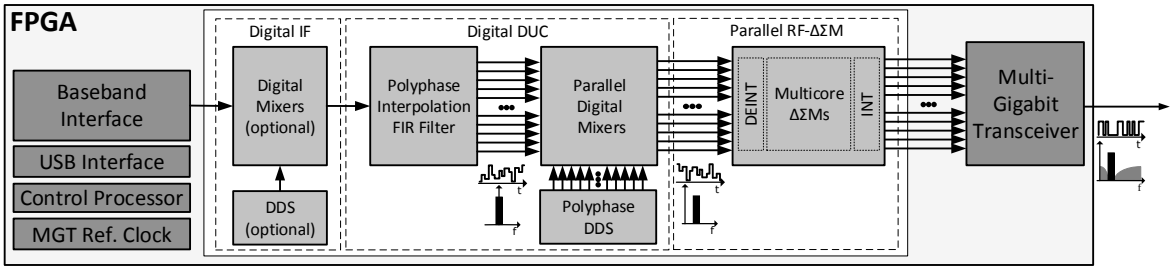

Figure 5.7: Block diagram of the implemented FPGA-based RF-ΔΣM Digital Transmitter.

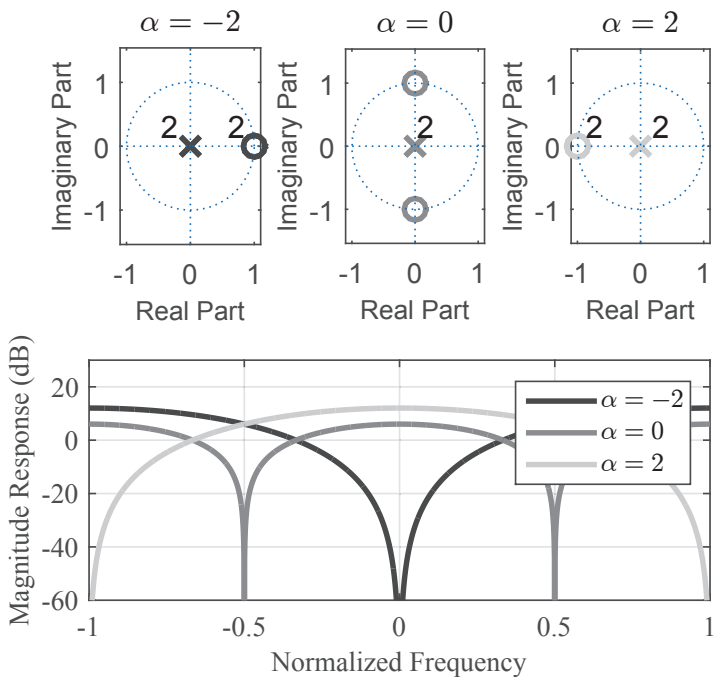

Figure 5.8: NTF's frequency response according to different α values.

The notch frequency(ies) can be found when the magnitude of the frequency response is zero, which leads to $\alpha = -2\cos(\theta)$. In particular, as depicted in Figure 5.8, the NTF's frequency response can be fully reconfigured from a low-pass filter ($\alpha = -2$) up to a high-pass filter ($\alpha = +2$), passing through a band-pass filter with tunable center frequency ($-2 < \alpha < +2$).

5.3 Prototype Validation

To validate the proposed parallel direct-conversion architecture, the two different ADTs (depicted in Figures 5.3 and 5.7) were implemented in a Virtex Ultrascale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. For the sake of a proof-of-concept, the polyphase DDS modules were designed with custom phase accumulators and custom LUTs, and not with Xilinx-provided IP cores. For the same reasons, the optional Digital-IF modules were not included as well. In both projects, the number of phases is equal to 64. In the $\Delta\Sigma$M case, an implementation with K configured to 256 samples was chosen, taking into account the maximum resource usage and the system performance.

In the proposed architectures, the MGT bitrate defines the modulator's 1st Nyquist Zone (from 0 to $Fs_{RF}/2$). This means that the carrier frequency can be located in any bin from the frequency grid given by the DDS' frequency resolution within this Nyquist Zone. Nonetheless, it is therefore clear that the higher the MGT bitrate, the better will be the system's FoM due to the increased OSR. However, this will impact the carrier frequency resolution, according to (5.1). For the RF-PWM case, the maximum timing constraints imposed a maximum Fs_{BB} of 200 MHz, and consequently, the bitrate of 12.8 Gbps was chosen. For the RF-$\Delta\Sigma$M, the feedback caused a reduction of the maximum BB sampling rate down to 160 MHz, leading to the serializer's bitrate of 10.24 Gbps. The frequency resolutions can be computed by using (5.1). In particular, the different bitrates together with the 13-bit resolution of the DDS' phase accumulator lead to 1.5625 MHz and 1.25 MHz, for the RF-PWM and RF-$\Delta\Sigma$M, respectively.

The MGT differential outputs were directly connected through a balun to the VSA R&S FSW 8 for signal analysis and demodulation. The experimental setup is depicted in Figure 5.9. The host computer controls and manages the FPGA-based ADT through a USB connection. At the same time, it controls and requests the data captures from the VSA. This automated testbed can sweep different carrier frequencies, modulations and bandwidths; and record such FoM as spectrum, MER and EVM.

5.3.1 RF-PWM-based ADT

As also introduced in Sec. 2.2.3, in the discrete PWM encoder, several expanded replicas or quantization noise from other Nyquist Zones may fold back into the first one. The distribution and placement of this noise are dependent on the choice of the reference waveform frequency. To validate this assumption, a given carrier frequency was fixed, and the reference frequency was changed from 43.75 MHz to 76.5625 MHz. The results are depicted in Figures 5.10 and 5.11, in the form of MER/EVM pairs and obtained spectrum, respectively. The results successfully demonstrate that, depending on the reference waveform's frequency, harmonic distortion and quantization noise may interfere with the desired signal, negatively

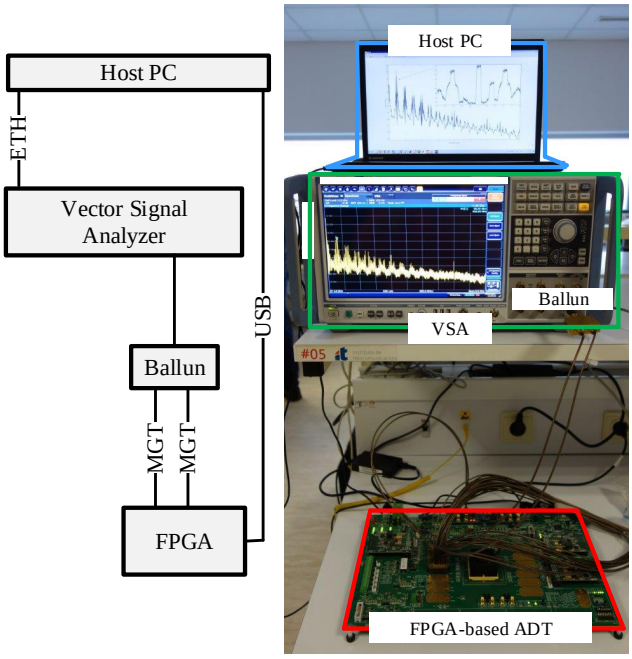

Figure 5.9: Block diagram and photo of the experimental setup.

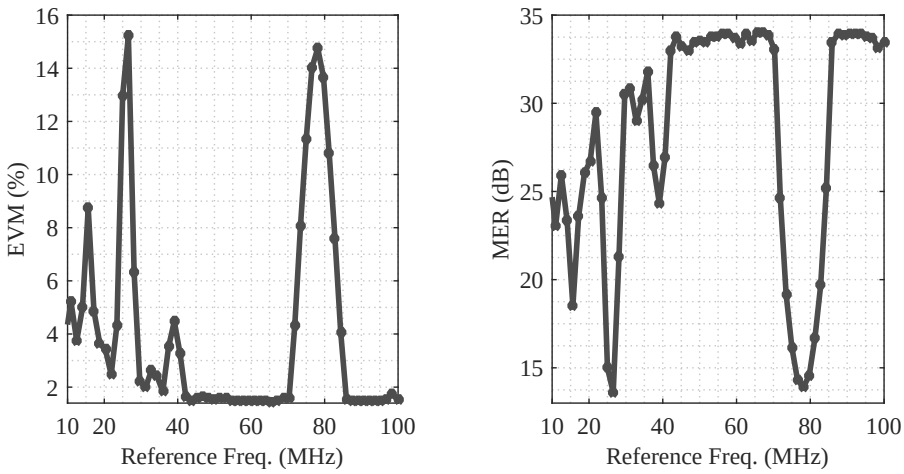

Figure 5.10: Measured results of a sweep in the reference waveform frequency for a carrier frequency of 4240.625 MHz with a 16-QAM 6 MHz modulated signal.

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impacting the signal's in-band quality. Thus, one can conclude that the frequency of the reference waveform must be carefully chosen to ensure optimum performance for all the carrier frequencies.

In this system, the frequencies of the reference waveforms were *a priori* defined as 29.6875 MHz and 40.625 MHz, for two different symbol rates of 5 Msps and 10 Msps, respectively. These values were chosen to allow a considerable distance between the in-band signal and the first expanded harmonics. Then, to ensure a high-performance system, and to minimize the amount

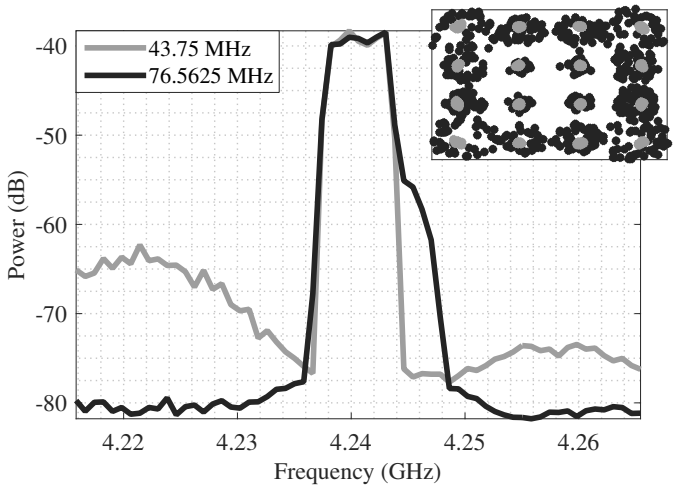

Figure 5.11: Obtained spectra for two of the points from Figure 5.10. 43.75 MHz corresponds to EVM 1.48% and 76.5625 MHz to EVM 14.03% (RBW=100 kHz, VBW=2 kHz, SPAN=50 MHz).

of in-band distortion from higher Nyquist Zones, a simple optimization methodology was designed. This low-complex methodology consists of sweeping the reference waveform frequency (in a small set of frequencies around the *a priori* defined ones), at the same time that the main FoM are measured in the VSA. Then, the reference frequencies that provide reduced in-band distortion for each carrier frequency are stored in the FPGA. This is a one-time procedure for a given signal bandwidth.

Figure 5.12 shows the measured results of a sweep of carrier frequencies in the range of 100 MHz up to 6.4 GHz, with a step of 78.125 MHz, for two different symbol rates: 5 Msps and 10 Msps. Focusing on the specific FoM, the maximum obtained MERs were 39 dB and 36 dB for the 5 Msps and the 10 Msps symbol rates, respectively. As expected, the reduction of the signal power as the frequency increases results in a lower MER. Nonetheless, even at 6.4 GHz, the average MER is close to 30 dB, which results in well-defined constellations.

The spectrum in a span of 8 GHz for a carrier frequency of 500 MHz is depicted in Figure 5.13. This is the spectrum resultant from the *sign* operation in the PWM.

Finally, the occupied resources in the FPGA for the proposed architecture are presented in Table 5.1. A high percentage of DSP slices ($\simeq$ 49%) are being used in the polyphase interpolation FIR filters. These filters were designed with a 3-tap transposed direct-form architecture per phase. Nonetheless, this percentage can be lowered with resort to multiplierless FIR or CIC filters.

5.3.2 RF-$\Delta\Sigma$M-based ADT

Figure 5.14 shows the measured results of a sweep of carrier frequencies in the range of 100 MHz up to 5.12 GHz, with a step of 62.5 MHz for four different symbol rates: 5 Msps,

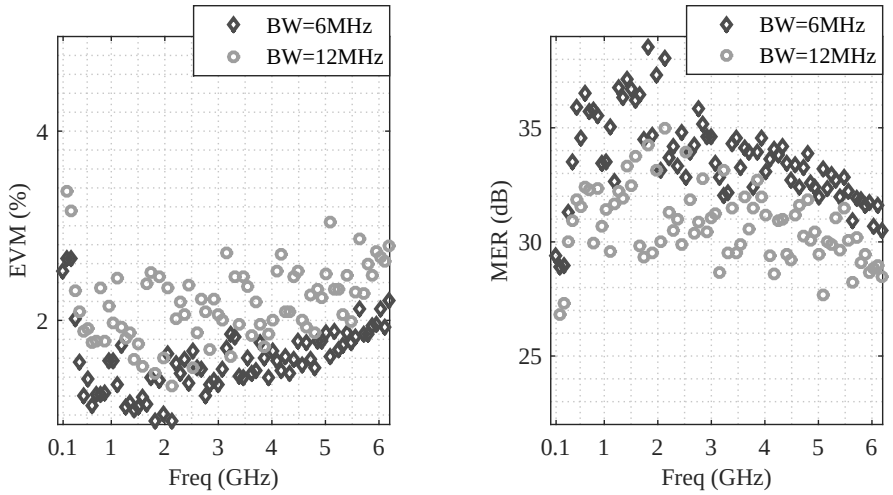

Figure 5.12: Measured results of a sweep in the carrier frequency with 16-QAM 5 Msps and 10 Msps modulated signals, which correspond to an available transmission bandwidth of 6 MHz and 12 MHz (roll-off factor of 0.2).

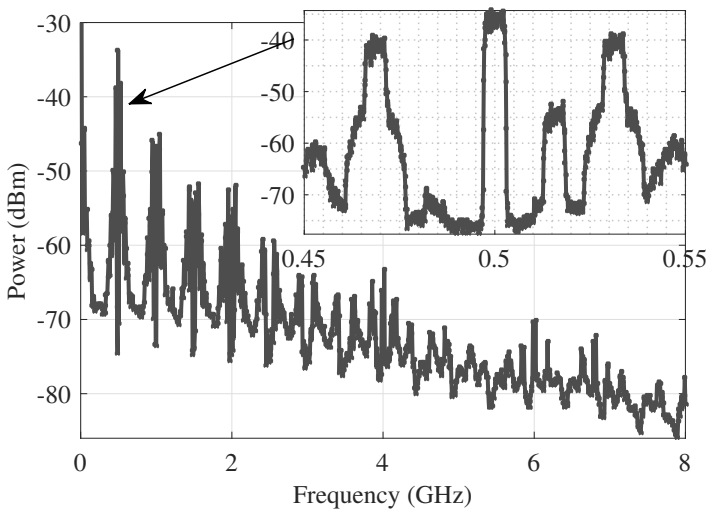

Figure 5.13: Obtained spectrum with a full span of 8 GHz for a carrier frequency of 500 MHz (RBW=100 kHz, VBW=2 kHz).

Table 5.1
Occupied resources for the proposed RF-PWM transmitter design

Logic Resources	Used	Total	%
Flip Flops	15256	1075200	1.42
LUTs	20677	537600	3.85
Memory LUT	640	76800	0.83
BRAM	96	1728	5.56
DSP48	372	768	48.44
GTHs	1	28	3.57

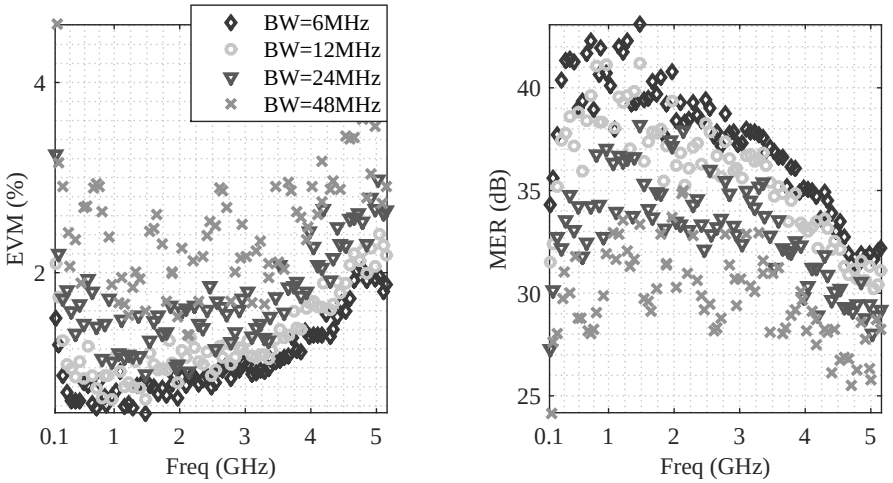

Figure 5.14: Measured results of a sweep in the carrier frequency with 16-QAM 5 Msps, 10 Msps, 20 Msps and 40 Msps modulated signals, corresponding to available transmission bandwidths of 6 MHz, 12 MHz, 24 MHz and 48 MHz (roll-off factor of 0.2).

10 Msps, 20 Msps, and 40 Msps. Focusing on the specific FoM, the maximum obtained MERs were 43 dB, 42 dB, 38 dB and 35 dB, respectively. Also, similarly to the PWM case, the signal power tends to reduce as the frequency increases, resulting in lower MERs. Nonetheless, even in the 5.12 GHz of carrier frequency, the average MER is close to 25 dB (for 40 Msps of symbol rate), resulting in well-defined constellations.

The spectrum in a span of 8 GHz for a carrier frequency of 2.475 GHz is shown in Figure 5.15. Additionally, Figure 5.16 shows the comparison between the different bandwidths in terms of spectrum and modulated constellation. The signal replicas in the spectrum presented in Figure 5.15 are distanced by $Fs/2$. This evidences a global sampling rate of 10.24 Gsps. The noise shaping capabilities from the $\Delta\Sigma$M can also be observed in Figure 5.15. Moreover, the image in the 2nd Nyquist Zone also presents a reasonable MER, meaning it could be used to achieve higher carrier frequencies [FFS+09]. The spurs around the desired carrier (and around the image) are caused by the inefficient interpolation FIR filter based on ZOH [PM01]. This interpolation technique was chosen due to its simplicity, efficiency in terms of occupied resources (no arithmetic operations are required) and low-complexity; making it ideal for application in a proof-of-concept. Nonetheless, other topologies could have been selected, depending on the requirements of the system.

Finally, the occupied resources for the RF-$\Delta\Sigma$M case are shown in Table 5.2. In this case, the Deinterleaving and the Interleaving modules are responsible for using a high percentage of BRAM primitives. These modules are required to temporarily accommodate all the incoming/outgoing data, before performing the required re-arrangements. Furthermore, a high percentage of DSP slices is used in the parallel $\Delta\Sigma$ modulators. Contrasting with the PWM case, the interpolation filter does not occupy a significant amount of resources. This is due

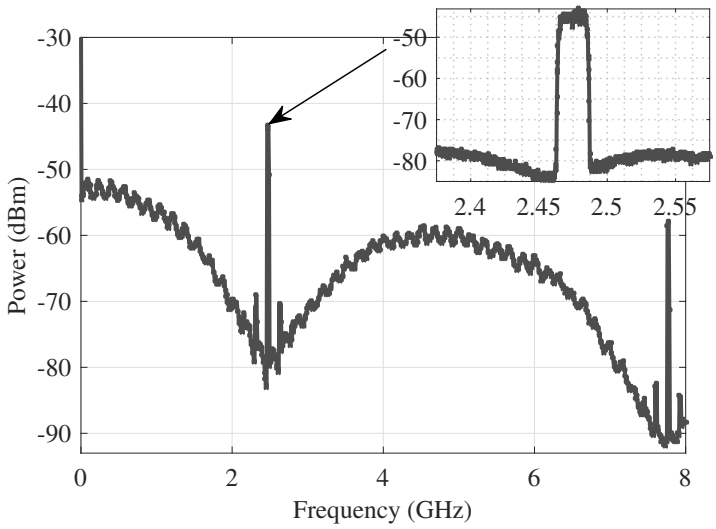

Figure 5.15: Obtained spectrum with two different spans (8 GHz and 100 MHz) for a 16-QAM modulated signal with 24 MHz of bandwidth at 2.475 GHz (RBW=100 kHz, VBW=2 kHz).

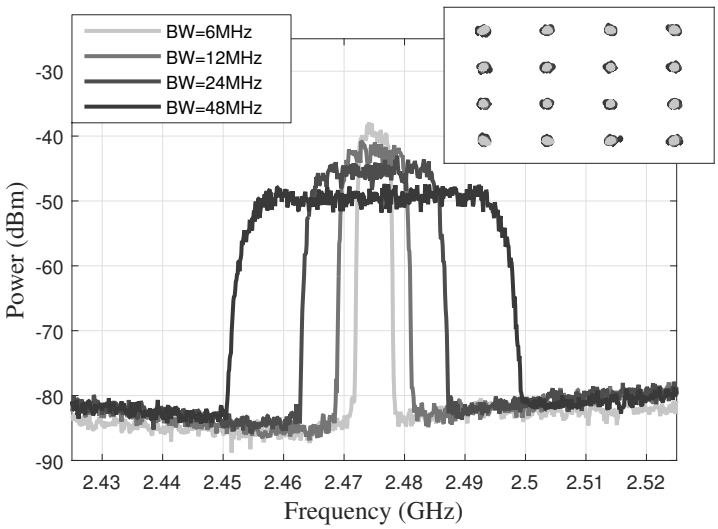

Figure 5.16: Different obtained spectra and respective constellations for bandwidths of 6 MHz, 12 MHz, 24 MHz and 48 MHz in a carrier frequency of 2.475 GHz (RBW=100 kHz, VBW=2 kHz).

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to the use of the ZOH topology.

5.3.3 Comparison to the SoA

Table 5.3 presents an overview of the relevant modulators presented in the literature. The comparison focuses on the frequency agility (Min. Fc and Max. Fc), together with the modulator's specifications: output sampling frequency (Fout), signal's bandwidth (BW), frequency resolution, modulator's type (Mod. Type) and modulator's implementation (HW

Table 5.2
Occupied resources for the proposed RF-ΔΣM transmitter design

Logic Resources	Used	Total	%
Flip Flops	25222	1075200	2.35
LUTs	54516	537600	10.14
Memory LUT	2438	76800	3.17
BRAM	1443	1728	83.51
DSP48	256	768	33.33
GTHs	1	28	3.57

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Table 5.3
Comparison of the proposed architectures with some relevant modulators from the SoA[1]

Reference	Min. Fc (MHz)	Max. Fc (MHz)	Max. Fout (Gsps)	Max. BW (MHz)	Freq. Res. (MHz)	Mod. Typ	HW Impl.	Agility
This (Impl. 1)	**100**	**6200**	**12.4**	**12**	**1.5625**	**RF-PWM**	**FPGA**	**Yes**
This (Impl. 2)	**100**	**5120**	**10.24**	**48**	**1.25**	**RF-ΔΣM**	**FPGA**	**Yes**
[MYHF17] (Impl. 1)	-	983	63	5	-	BB-ΔΣM-PWM	ASIC	No
[MYHF17] (Impl. 2)	-	2620; 5240	24.5	20	-	BB-ΔΣM-PWM	FPGA	No
[THT+16]	-	5200	20.8	20	-	BB-ΔΣM	FPGA	No
[DCB+16]	2375	2625	10	3.75	0.05	BB-ΔΣM	FPGA	Yes
[COVS16]	-	1600	6.4	122	-	BB-ΔΣM	FPGA	No
[CMS+15]	-	856; 1450	25	20	n/a	RF-PWM	AWG	Yes
[ZMD+14b]	-	1905	7.9	20	-	BB-PWM	FPGA	No
[SG14]	-	900; 1950	n/a	5	-	RF-PWM	ASIC	No
[COVS14]	-	900; 1000	4	15	-	BB-ΔΣM	FPGA	No
[OGOS12]	2100	2200	5	5	(Analog)	RF-ΔΣM	ASIC	Yes
[FFS+09]	-	650; 950	4	5	n/a	RF-ΔΣM	ASIC	No
[OGSM09]	2100	2200	9	5	(Analog)	RF-ΔΣM	ASIC	Yes
[SGH+09]	1550	2450	7.5	20	(Analog)	RF-ΔΣM	ASIC	Yes

[1]In the table, "-" and "n/a" stand for "not-applicable" and "not-available", respectively.

Impl.). By agility (last column), one is referring to implementations or techniques that allow the adjustment of the carrier frequency without changing the output's sampling rate. Even though all the published works have a certain degree of frequency agility, achieved by reconfiguring the output sampling frequency, this solution is not ideal. As first introduced in Section 2.2.4, this reconfiguration is limited (or not feasible at all), and will impair the system's performance by unintentionally varying the modulator's OSR. This is why the frequency

agility of the solutions presented in this work is considerably higher than that of their SoA counterparts. Moreover, this work has demonstrated the generation of signals centered around a maximum carrier frequency of $Fs/2$, showing that the carrier frequency and the output sampling frequency do not need any OSR (generation is possible up to the Nyquist Limit). Ultimately, this will relax the final system requirements, and, at the same time, will minimize the switching losses from the amplifier stage. In addition to that, this work also presents the first design of RF Pulse Encoders with no dedicated and custom application-specific devices. In particular, the fully parallel approach enables the integration of pulse encoders working at RF frequencies into an FPGA, constrained to a maximum sampling rate of less than 200 MHz in the programmable logic part.

Finally, when considering the two different implementations that were proposed in this work, it can be mentioned that there is a trade-off between performance and resource occupation. On the one hand, the RF-PWM case is a minimalist architecture, with a low degree of resource occupation, but with a number of drawbacks: the dependence on the reference waveform's frequency, the low available bandwidth, and the high requirements for the analog filtering. On the other hand, the multicore-based RF-$\Delta\Sigma$M is a more robust solution, with relaxed analog filtering requirements, with a reasonable MER, and a scalable solution (in the sense that any topology can be chosen for the modulator itself). However, to achieve superior performance, a reasonable number of contiguous samples are required, leading to an excessive resource occupation.

One final note related to the scalability of this architecture must be highlighted. The main focus of this work was to demonstrate a parallel RF-stage transmitter that could be synthesized and embedded into programmable logic. This limits the sampling rate to be significantly inferior to the required RF carriers. Thus, to validate the aforementioned architecture, two different RF pulse encoders were designed and integrated as a proof-of-concept. Consequently, the amount of logic resources that were reported in both implementations should not be taken as the minimum required values to design and implement this architecture. Several different optimization techniques, in the critical subsystems, could be done according to different requirements. For instance, one possible implementation that relaxes the amount of resource usage in multicore-based $\Delta\Sigma$M was recently proposed in [DCO+17].

5.4 Summary and Concluding Remarks

This chapter presented a new architecture for designing agile and real-time reconfigurable RF-stage ADTs. The technique was proposed and validated in an FPGA-based transmitter. By enabling the synthesis of a fully parallel RF-PWM/$\Delta\Sigma$M transmitter, an unprecedented frequency agility was enabled (in the range of 100 MHz up to 6 GHz, with a maximum frequency resolution of 1.5625 MHz). This is a considerable improvement compared to the

conventional single-rate counterparts working directly in the RF stage. These single-rate architectures require sampling rates much higher than the carrier frequencies. The proposed architecture exceeds the SoA in terms of simplicity and flexibility. The system's behavior in terms of carrier frequency, symbol rate and modulation type, can be updated in real-time, by adjusting the set of variables that control the whole system.

In the end, it can be concluded that the proposed parallel architecture has a large potential for the design of real-time reconfigurable digital RF Transmitters. The experimental results show that it is possible to generate signals with high MER at the desired carrier frequency, reconfigurable in real-time. The real-time reconfiguration involves a small change in the set of variables that control the polyphase DDS and the polyphase reference waveform generator (in the RF-PWM case). Thus, the MGT's bitrate can be optimized and maintained constant during the system's operation to provide the adequate OSR and, ultimately, the ideal FoM.

The next chapter will introduce a set of architectures based on multicore-$\Delta\Sigma$ modulators that can have a significant impact on the design of wideband modulators.

Chapter 6

Wideband Delta-Sigma Modulators

Outline

Bandwidth is another of the key limitations of current ADTs. Thus, in this chapter, this research line is addressed and a promising architecture is proposed.

This chapter is supported by the conference papers [DCO+17, DMT+18a]. In particular, the chapter starts by proposing an enhanced multicore-$\Delta\Sigma$ architecture that relaxes the resources usage by propagating the state registers of adjacents $\Delta\Sigma$M, with no performance degradation. Then, the architecture will be embedded with the RF-stage architecture presented in the Chapter 5 to demonstrate the first reported multi-level ADT with an available bandwidth of 1.25 GHz.

6.1 Enhanced Multicore-$\Delta\Sigma$M Architecture

6.1.1 Contextualization

Even though the architectures that have been proposed in the SoA are promising, the transmission BW tends to be limited. To reach higher bandwidths, the sampling rate of the Pulse Encoder must be increased. The use of polyphase decomposition techniques, particularly within feedback loops have been proposed [PJ93, COVS14]. However, as the inclusion of pipeline stages typically impairs the transfer functions of the modulators, the scalability of this technique is quite limited [COVS14]. A promising alternative based on the parallelization of $\Delta\Sigma$M was also reported in [COVS16]. It aims at deploying N multiple modulators running in parallel, each one processing independent slices (of size K) of the same input signal. However, as introduced in Section 2.3.1, the discontinuities between slices will cause impulsive noise that can be reduced by increasing the size K of the slices. This means that, as a downside, this architecture has an implicit trade-off between performance and memory resources usage.

6.1.2 Proposed Architecture

Simulations were carried out in the multicore-based $\Delta\Sigma$ architecture proposed in [COVS16]. It was possible to understand that the impulsive noise in the discontinuities among slices is caused by the initial conditions of each modulator that do not take into account the final state conditions from the subsequent modulators. Thus, to enhance the performance of this architecture the proposed idea falls into the propagation of the state registers among adjacent modulators. This leads to a reduced periodicity in the generation of impulsive noise. The idea is similar to the propagation of error values proposed in [ASC14], but instead of propagating the error values in a continuous way, which can lead to stability issues, the state registers from the previous modulators are just taken into consideration during m clock cycles (where m is the order of the $\Delta\Sigma$M) within K clock cycles. By doing this, it is possible to ensure a high level of performance even for small length sizes, ultimately relaxing the system's requirements in terms of implementation resources.

Figure 6.1 illustrates the comparison between the conventional multicore-based $\Delta\Sigma$ architecture and the one proposed in this work. By displacing the modulators in a diagonal matrix, with delayed inputs/outputs, the periodicity of the impulsive noise can be reduced by a factor of N. In other words, the only discontinuities will occur from the last phase (N) to the first one. Thus, in practice, the impulsive noise will occur in every $N \times K$ clock cycles, instead of occurring in every K cycles. This is of utmost importance to maintain the same system performance with relaxed memory requirements.

From an implementation point of view, in addition to the displacement of the modulators, a new module must be introduced to deal with the propagation of the state registers. This module (referred to as *Synchronous Start-up Control Logic*) is in charge of monitoring the final state registers of every modulator, in every K clock cycles, and to transfer this information to the next one. This exchange of information occurs in every transition and just by a limited number of clock cycles. Thus, extra concerns about stability issues are not raised.

6.1.3 Prototype Validation

The block diagram of the implemented ADT is illustrated in Figure 6.2. The BB interface is continuously transmitting the samples to the modulator. As previously introduced, the modulator is based on N different $\Delta\Sigma$Ms according to the architecture presented in Figure 6.1b. Thereafter, the modulated samples are combined and replicated by the *Digital Upconversion Stage* to generate a parallel output word containing the four components $[I, \overline{Q}, \overline{I}, Q]$ of the desired signal. This output word is serialized by the MGT.

To assess the performance of the proposed architecture, the full architecture was firstly simulated. To accomplish this, a 2nd-order Low-Pass (LP)-$\Delta\Sigma$ topology based on an Error-feedback structure (previously depicted in Figure 3.4) was chosen and replicated sixteen times ($N = 16$). This topology has a short critical path, leading to higher sampling rates, and

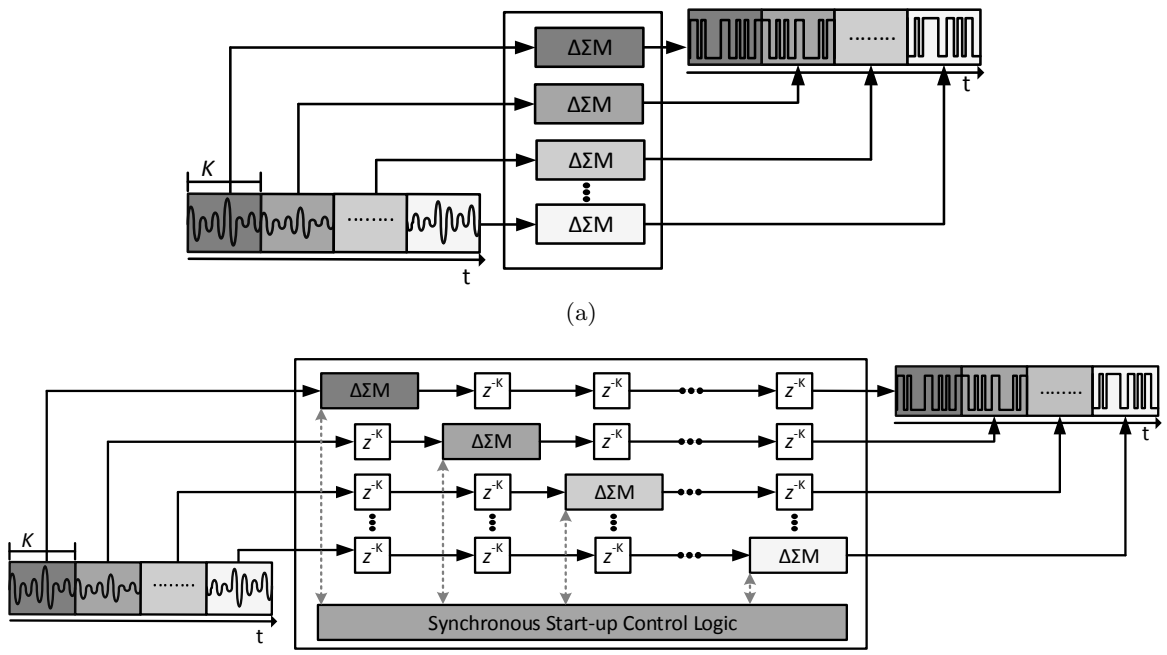

Figure 6.1: Comparison between the multicore-based ΔΣM presented in [COVS16] (a) and the one proposed in this work (b) (herein referred to as "Conventional" and "Proposed", respectively).

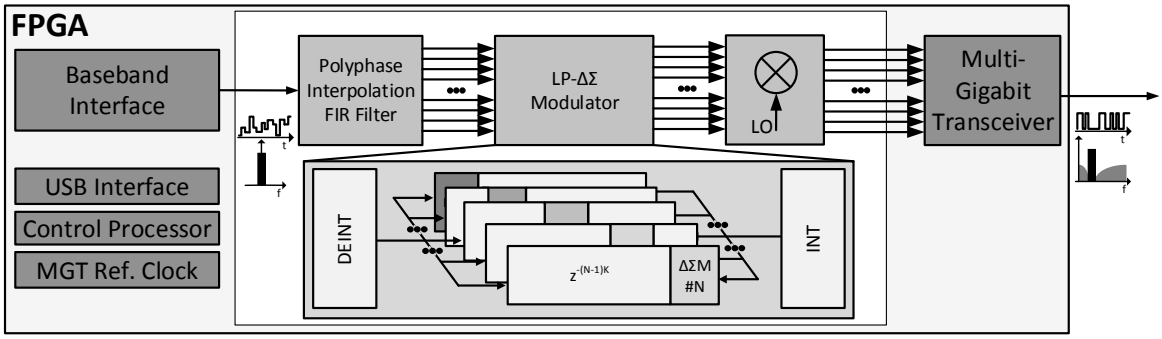

Figure 6.2: Block diagram of the implemented All-Digital Transmitter.

just two delays in the feedback loop. This means that only two state registers need to be propagated, reducing the complexity of the module *Synchronous Start-up Control Logic*.

To assess the difference between the conventional and the proposed architecture, the different approaches were simulated and compared to a single-rate and ideal modulator. The comparison in terms of the spectrum is demonstrated in Figure 6.5, where a 5 Msps 16-QAM signal is transmitted with the different approaches with a K of sixteen contiguous samples. It is clear that the proposed architecture shows better performance and approaches the ideal spectrum. Thereafter, the in-band signal was filtered and the error signal between the ideal and the two different approaches was computed (Figure 6.3). All the signals' magnitude are in

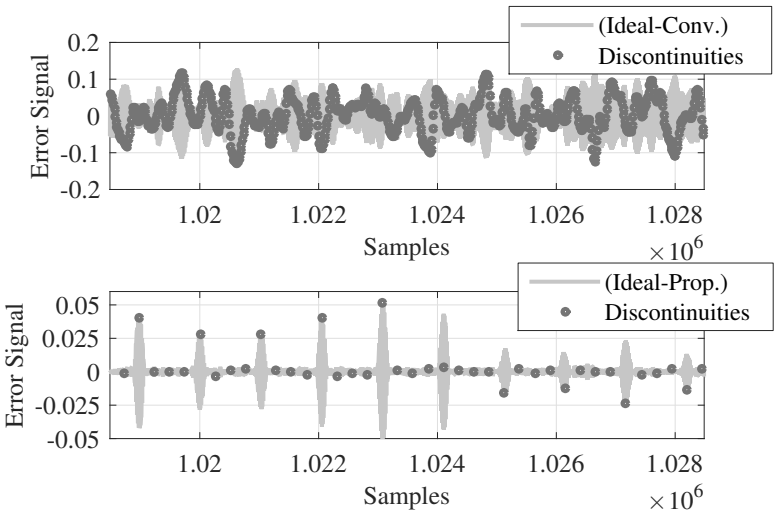

Figure 6.3: Simulated temporal evolution of the error signals for the different architectures with a K of 16 samples, together with the discontinuities' instants, for a 5 Msps 16-QAM signal.

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the range of [-0.8,0.8]. As can be seen, while 16 contiguous samples ($K = 16$) are insufficient for the conventional architecture to recover from the discontinuities, the proposed architecture is quite superior maintaining a small and limited error signal. It is also demonstrated that the periodicity of the discontinuities was considerably decreased. In practice, it was changed from K cycles in the conventional one to $K \times N$ clock cycles in the proposed architecture.

The signal's in-band performance, as well as the adjacent noise power, were also simulated and quantified in terms of Normalized Mean Square Error (NMSE) and ACPR, respectively. The results are depicted in Figure 6.4. It is clear that the performance of the proposed architecture is quite superior to the conventional one: NMSE always less than -30 dB and ACPR always higher than 30 dBc. In particular, this superior performance is higher for a small number of contiguous samples, which was the main objective of this work.

The proposed architecture was also implemented into a Virtex Ultrascale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. The modulator was optimized to enable a BB sampling frequency of 200 MHz, leading to an MGT sampling rate of 12.8 Gbps. In this way, the obtained carrier frequency is 3.2 GHz. The MGT was then connected to the Vector Signal Analyzer R&S FSW 8 for signal analysis and demodulation.

In addition to the simulated results, experimental results were also obtained and in particular, spectrum and EVM measurements are reported. Different obtained spectra and respective constellations for BWs of 6 MHz, 60 MHz and 120 MHz are presented in Figure 6.6 for a small span. A comparison between different spans (8 GHz and 600 MHz) for a BW of 120 MHz is also depicted in Figure 6.7. The spurs around the carrier frequency are caused by an inefficient interpolation FIR filter based on ZOH that was implemented as a

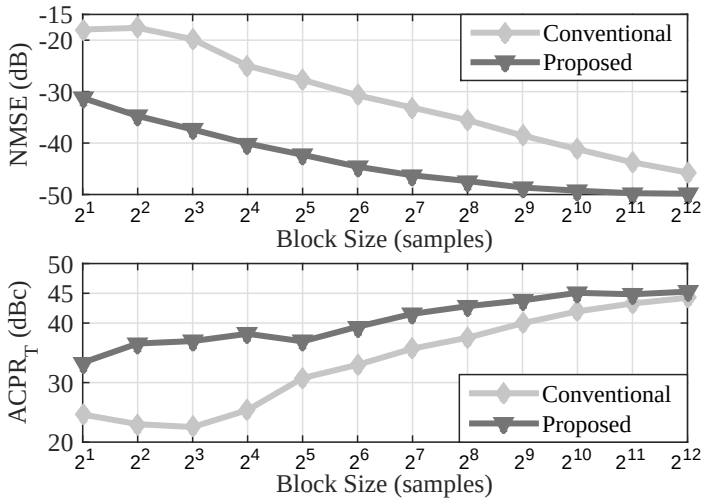

Figure 6.4: Simulated NMSE and ACPR figures of merit of the different architectures with different block sizes K. The input signal was a 5 Msps 16-QAM modulated signal.

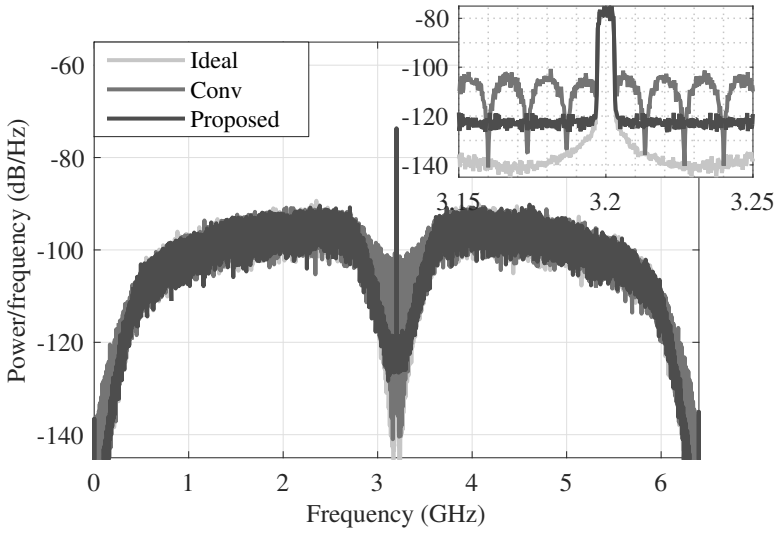

Figure 6.5: Comparison of the different simulated spectra with N of sixteen phases and K of sixteen contiguous samples for a 5 Msps, 16-QAM signal.

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proof-of-concept.

Table 6.1 a) summarizes the obtained EVM-MER pairs obtained for the different BWs. All the experimental results present EVM values below 3%, even for the case of 120 MHz of BW, attesting the validity of the proposed architecture. At last, the occupied resources are depicted in Table 6.1 b). The FPGA presents a resources usage quite inferior to the conventional approach, with all the major primitives below 6%, fulfilling the typical specifications from the mid-range FPGA's available in the market.

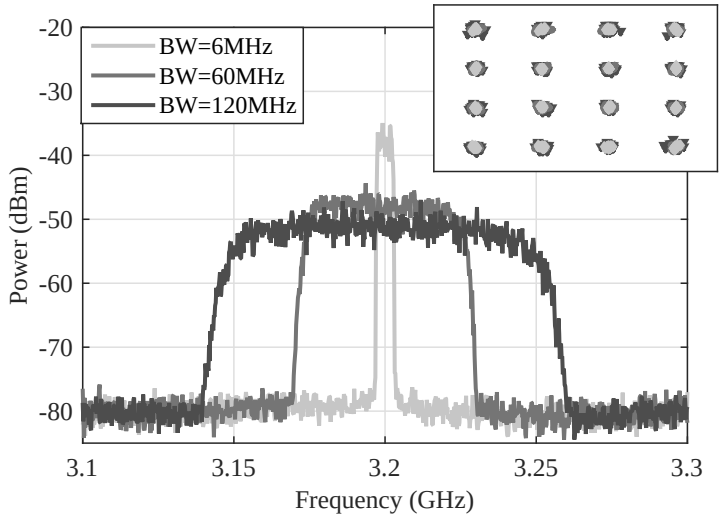

Figure 6.6: Different obtained spectra and respective constellations of a 16-QAM signal with BWs of 6 MHz, 60 MHz and 120 MHz (RBW = 100kHz, VBW = 2kHz).

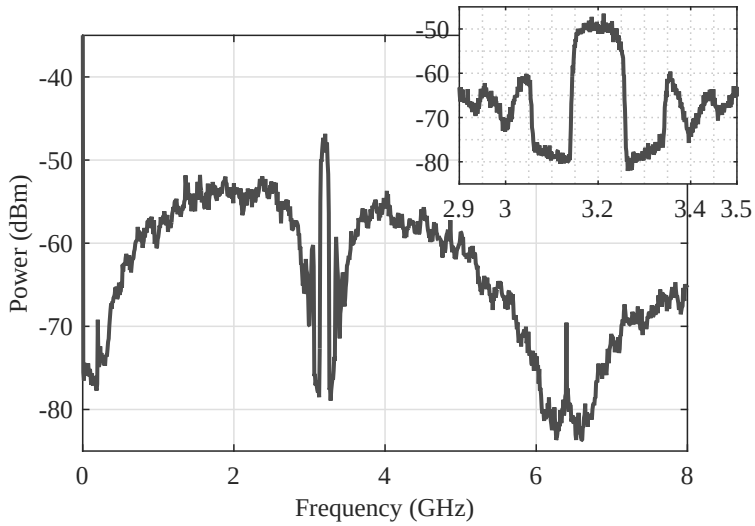

Figure 6.7: Obtained spectrum with different spans of a 16-QAM signal with 120 MHz of BW (RBW = 100kHz, VBW = 2kHz).

6.2 Multi-level Architecture with 1.25 GHz of Bandwidth

6.2.1 Contextualization

Even though the promising architectures that have been proposed in the SoA, the transmission BW is tendentially limited. As far as FPGA-based ADTs are concerned, the use of multicore-based ΔΣMs was proposed in [COVS16], leading to the usable BW of 125 MHz. Then, an optimized 2nd-order Time-Interleaved ΔΣM with 488 MHz of BW was reported in [THTK17]. However, in all the typical SoA works, the use of BB-stage ADTs requires an

Table 6.1
(a) MER/EVM pairs for a 16-QAM signal. BW is in MHz, EVM in % and MER in dB. (b) Comparison of the resources usage of the proposed ($K = 16$) and the conventional ($K = 256$) ADT (Ks were chosen according to Figure 6.4 to ensure the same performance).

(a)

BW	MER	EVM
6	36.6	1.12
12	35.8	1.20
24	33.5	1.59
48	31.3	2.04
60	30.9	2.13
120	28.0	2.97

(b)

		Proposed		Conventional	
Resources	Total	Used	%	Used	%
Flip Flops	1075200	7084	0.66	15423	1.43
LUTs	537600	8558	1.59	36347	6.76
Mem. LUT	76800	2311	3.01	29641	38.60
BRAM	1728	96	5.56	608	35.19
GTHs	28	1	3.57	1	3.57

extra OSR of at least 4 times for the DUC which, ultimately, leads to challenging serializer sampling rates (e.g. 20, 28 and 60 Gbps in [THTK17, THT+16, MYHF17], respectively). Nonetheless, in addition to the increased complexity and cost, the design of analog front-ends becomes quite challenging. Thus, novel strategies must be found to enable the transmission of wider bandwidths, which are increasingly appealing for the next generation of communication systems.

6.2.2 Proposed Architecture

The proposed idea to achieve higher bandwidths is based on the integration of a high-order $\Delta\Sigma$ topology with the RF-stage ADT architecture proposed in chapter 5. First, the high-order $\Delta\Sigma$M has a higher notch bandwidth, enabling the accommodation of higher bandwidths. Second, the RF-stage ADT is the architecture that achieves a given OSR with the minimum serializer's sampling rate. From an implementation point of view, the propagation of state-registers must be integrated into the multicore-based $\Delta\Sigma$ architecture as well, in order to relax the memory resources usage.

Focusing on the $\Delta\Sigma$ topology, its design must be done according to the required notch BW. However, at the same time, the critical path must be as short as possible, whic his the reason why such architectures as CRFF, CRFB, CIFF or CIFB are not suitable. Thus, the generic Error-Feedback (EF) $\Delta\Sigma$ architecture with a FIR feedback loop (depicted in Figure 6.8) was selected as a starting point. This architecture was derived from the conventional tunable $\Delta\Sigma$M based on the Error-Feedback topology (recalling Figure 5.6), by adding two complex zeros per required notch. For the sake of simplicity, let us limit the number of notches to 3. We model the quantization noise as random noise signal and we use:

$$NTF(z) = \left(1 + \alpha z^{-1} + z^{-2}\right) . \left(1 + \beta z^{-1} + z^{-2}\right) . \left(1 + \gamma z^{-1} + z^{-2}\right) \quad (6.1)$$

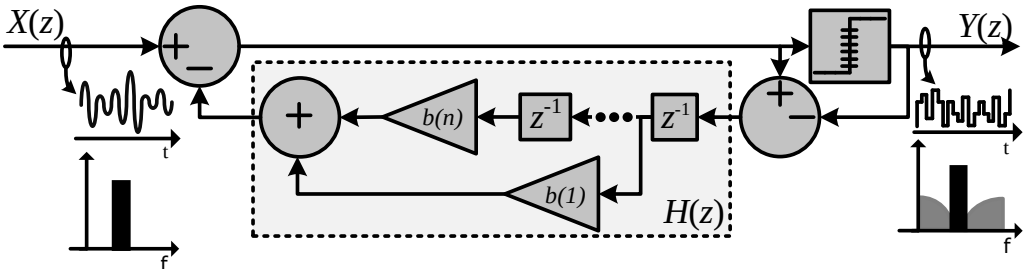

Figure 6.8: Representation in z-domain of an Error-Feedback ΔΣM with FIR feedback loop.

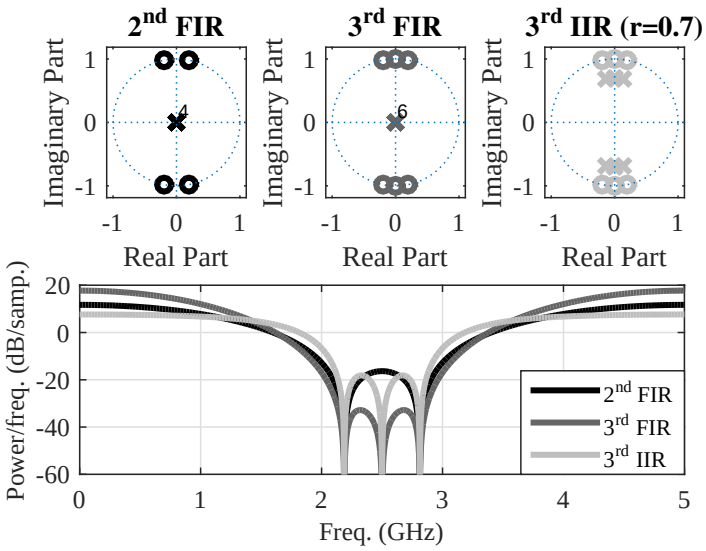

Figure 6.9: NTF's frequency response and zero-poles placement according to the different feedback-loop transfer functions.

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where α, β and γ are defined as $-2\cos(2\pi Fc/Fs)$, Fs is the sampling frequency, and Fc is the required notch frequency. As $NTF(z) = 1 + H(z)$, where $H(z)$ is the feedback loop transfer function, $H(z)$ can be computed as:

$$H(z) = b(1)z^{-1} + b(2)z^{-2} + b(3)z^{-3} + b(4)z^{-4} + b(5)z^{-5} + b(6)z^{-6} \tag{6.2}$$

where $b(1) = (\alpha + \beta + \gamma)$, $b(2) = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $b(3) = (2(\alpha + \beta) + \gamma(2 + \alpha\beta))$, $b(4) = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $b(5) = (\alpha + \beta + \gamma)$, and $b(6) = 1$.

After deriving the coefficients, simulations were carried out in Matlab to choose a suitable feedback loop's order to achieve around 1.25 GHz of usable bandwidth (Figure 6.9).

The notches were uniformly distributed into the desired bandwidth. While comparing the 2nd and 3rd FIR curves, it can be realized that the latter is the only that fulfills the specification with better performance. However, the typical wireless modulated signals (briefly specified in terms of PAPR, the order of the modulation, and bandwidth) preclude the imple-

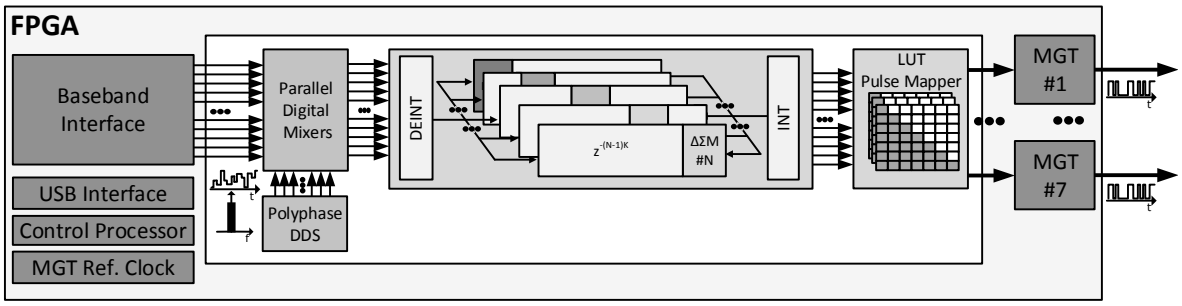

Figure 6.10: General block diagram of the implemented All-Digital RF Transmitter, embedded into an FPGA.

mentation of this architecture with a single-bit output, due to stability issues. While the SoA proposes the inclusion of poles to ensure the stability, as it is also depicted in Figure 6.9, their inclusion reduces the achievable bandwidth. Thus, the proposed solution solves the stability issue by reducing the quantization error, through the use of more bits in the quantizer (in particular 8 levels were considered for the sake of proof-of-concept).

The block diagram of the implemented ADT is depicted in Figure 6.10. The BB data is interpolated to the serializer's sampling rate, divided into N phases and forwarded to the polyphase DUC. This division into multiple phases is required when the signal BW is higher than the FPGA programmable logic subsystem's sampling rate. Each phase is clocked at Fs_{BB}, providing an equivalent sampling rate of $Fs_{MGT} = NFs_{BB}$. The DUC is composed of a polyphase DDS, working as LO. The resultant data is forwarded to a Deinterleaving module, that temporarily stores and re-arranges the data into N blocks of size K. These blocks feed the N phases to the Multi-core 8-level $\Delta\Sigma$ architecture. The computed encoded equivalents are temporarily stored and re-arranged again by the Interleaving Module. It must be stated that the *Synchronous Start-up Control Logic* was included to ensure the propagation of the state-registers as presented in [DCO+17]. This enables a reduction of K while maintaining a given performance. Ultimately, the latency is improved, as well as the memory resources usage. Moreover, in this work, K was forced to be equal to N, in order to replace the First-In First-Out (FIFO) memories (proposed by the authors to be used in the Deinterleaving/Interleaving modules [DCO+17, DCO+18]) by just registers and multiplexers. Afterwards, a LUT-based mapper encodes the 3-bit samples into seven single-bit streams, that will be serialized by seven different MGTs.

6.2.3 Prototype Validation

To validate the proposed approach, an ADT was fully implemented into a Virtex Ultrascale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. The carrier frequency was chosen to be 2.5 GHz and the architecture is based on sixty-four different phases ($N = 64$). The MGTs' sampling rate were configured to operate at 10 Gbps, and lane-to-lane deskew

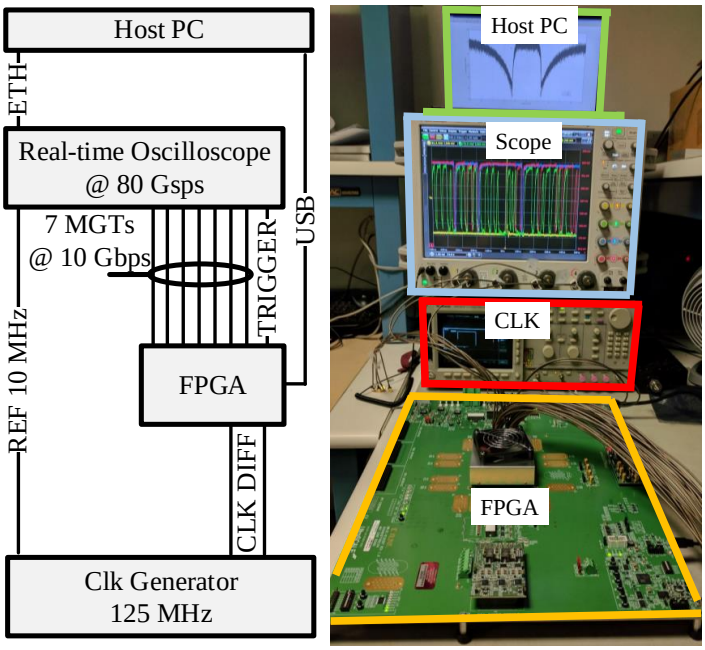

Figure 6.11: Block diagram and photo of the experimental setup.

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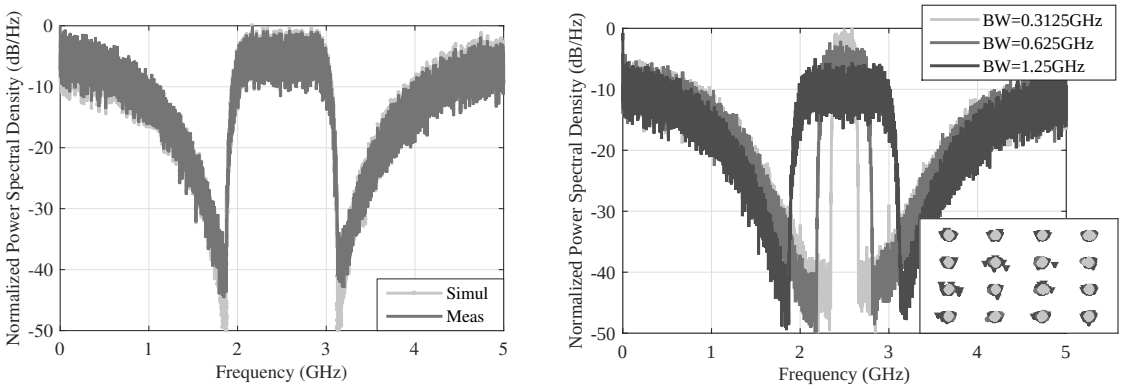
techniques were implemented in the digital hardware, as well as extra phase alignment cables were attached to some MGTs to ensure the lane-to-lane synchronization.

The experimental setup is depicted in Figure 6.11. Due to the challenges of measuring the seven MGT channels at the same time, an extra MGT was included as an embedded trigger in the acquisition of all the channels with a 4-port Real-time Oscilloscope (Keysight DSA-X 92504Q). The Tektronix AWG610 generates the FPGA reference clock and forwards a 10 MHz reference to the oscilloscope. After having all the channels acquired, the seven streams are simply combined (note that no post-processing, such as timing/amplitude corrections, is applied) and the signal analysis and demodulation is done through the LabView VSA Software from National Instruments.

Experimental results were obtained and, in particular, spectrum and EVM measurements are reported. The comparison between the simulated and the measured 16-QAM modulated signal with 1.25 GHz (symbol rate of 1 Gsps and Root-Raised Cosine (RRC) of 0.25) is demonstrated in Figure 6.12a. It can be observed the good agreement between both data. The performance drop in terms of MER (also observed in the same figure) results from the amplitude mismatch between the different MGTs. Different measured spectra and respective constellations for bandwidths of 312.5 MHz, 625 MHz and 1.25 GHz are presented in Figure 6.12b. These measurements were obtained from three different hardware implementations, with a uniform placement of the three notches to cover the required bandwidth.

Table 6.2 (a) summarizes the obtained EVM-MER pairs obtained for the different BWs. All the experimental results present EVM values below 2.5%, even for the case of 1.25 GHz



(a) (b)

Figure 6.12: (a) Comparison of the simulated and measured spectra with a 16-QAM modulated signal with 1.25 GHz; (b) Different measured spectra and respective constellations with BWs of 312.5 MHz, 625 MHz and 1.25 GHz.

Table 6.2
(a) MER/EVM pairs for a 16-QAM signal. BW is in GHz, EVM in % and MER in dB. (b) Resources usage of the proposed architecture

(a)

BW	MER	EVM
0.3125	36.90	1.05
0.625	36.58	1.10
1.25	30.51	2.23

(b)

Resources	Used	Total	%
Flip Flops	35411	1075200	3.3
LUTs	94627	537600	17.6
Mem. LUT	57882	76800	75.3
BRAM	0	1728	0
DSP48	128	768	16.6
GTHs	8	28	28.5

of bandwidth, attesting the validity of the proposed architecture. Moreover, to the best of author's knowledge, this is the maximum bandwidth ever reached with an FPGA-based ADT architecture (the maximum value of 488 MHz was previously reported in [THTK17]). The occupied resources are depicted in Table 6.2 (b). It should be mentioned that the Block Random-Access Memory (BRAM) primitive could be used to balance the high utilization of the Memory LUT.

6.3 Summary and Concluding Remarks

This chapter presents two different works related to the design of wideband ADTs.

The first part of the chapter reports an enhancement of the multicore-based $\Delta\Sigma$ architecture. In particular, it was demonstrated that the propagation of state registers between adjacent modulators can have a significant impact in relaxing the memory resources usage

with no performance degradation. This technique was implemented and validated into an FPGA-based ADT. All the experimental results attest the validity of the proposed architecture. In addition to achieve superior performance in terms of wideband capability with a small resources usage occupation, the technique is almost independent of the modulator's topology.

The second part of the chapter combines the aforementioned architecture with the RF-stage ADTs presented in Chapter 5, to achieve 1.25 GHz of BW. The technique was implemented and validated into an FPGA-based ADT as well. All the experimental results attest the validity of the proposed architecture. For the sake of this proof-of-concept, the assessment of the outputs was performed with a high-speed oscilloscope. However, the promising results in terms of signal integrity anticipate that analog combining networks based on power combiners or in asymmetric extended H-bridges can also be incorporated. In this case, the analog impairments (in terms of phase imbalances, or magnitude mismatches) can be easily compensated in the digital domain. Thus, the most stringent requirement, from a designer point-of-view, is the synchronization between multiple lanes that must be ensured. In addition to achieve a superior performance in terms of wideband capability, the fully digital behavior of this architecture shows a strong potential to be synthesized in custom ASICs.

The next chapter reports a set of BB- and RF-stage architectures that leverage the design of concurrent multi-band transmitters. In particular, the design of agile and flexible dual and triple bands ADTs will be demonstrated.

Chapter 7

From Single- to Concurrent Multi-Band Transmission

Outline

This chapter addresses the contributions of this Ph.D. work to design concurrent multi-band digital transmitters.

This chapter is supported by the conference paper [DCOV16b], and by the journal articles [DCB+16, DMS+18]. The chapter starts by proposing an architecture for a BB-stage ADT that can be real-time reconfigured to transmit one or dual bands of modulated data, with a maximum distance between bands of almost 300 MHz. Then, the proposed architecture has evolved to include a linear pre-compensation mechanism that can improve the dual-band FoM of the dual-band scenario. The chapter is concluded with the proposal of an RF-stage architecture aimed for the design of one up to three bands that can be digitally generated in the range of 100 MHz up to 2.5 GHz.

7.1 Contextualization

Despite the apparent ideal and native support for the multi-band capability, design challenges associated with the non-contiguous CA transmission in ADT have hampered the proposal of multi-band solutions. Thus, the reported literature on non-contiguous CA ADTs is quite scarce. Generally speaking, multi-band transmission can only be achieved with integer multiples of the modulators sampling frequencies [SOC12a], or with reduced sampling rate topologies [KI10, MTKS13]. Others, employ bulky and inefficient power combiners to join different bands before transmission [KI10, BCHG13]. All these difficulties in designing multi-band transmission arise from the placement of the DUC after the pulse encoding.

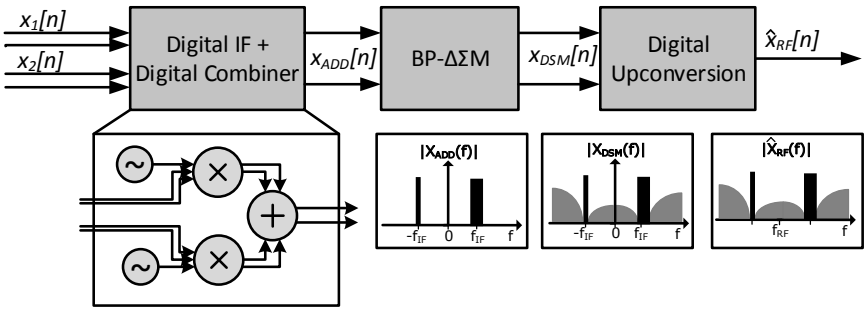


Figure 7.1: General block diagram with the transmitter's architecture demonstrating the use of this modulator into single- or/and dual-band scenarios.

7.2 Single- and Dual-Band Transmission with Tunable Bandpass ΔΣM

This section is related to the design of an ADT able to simultaneous transmit up to two non-contiguous frequency bands.

7.2.1 Proposed Architecture

The proposed idea is based on the use of a low-complex and tunable ΔΣ architecture to perform the real-time encoding of different frequency bands with negligible degradation of the in-band signals. In particular, the underlying idea explores the real-time displacement of the spectral notches of a ΔΣM to configure the system as a LP-ΔΣM, a Band-Pass Delta-Sigma Modulator (BP-ΔΣM) with tunable center frequency or a High-Pass Delta-Sigma Modulator (HP-ΔΣM). On the one hand, the use of low-/high-pass topologies enables the development of single-band transmitters. On the other hand, by configuring the system as a bandpass modulator, the two notches in the spectrum can be exploited to develop concurrent dual-band digital transmitters. Focusing on the BP-ΔΣM without loss of generality, the fact that one is dealing with real coefficients means that the frequency response is symmetric, which gives origin to symmetrical notches around the DC component. Thus, in this sense, taking into account that these two bands will preserve their integrity due to the noise shaping property, they can be used to place up to two different bands (one at $+f_{if}$, one at $-f_{if}$ or two at $\pm f_{if}$) before the digital upconversion stage to RF, such as depicted in Figure 7.1.

The block diagram of the proposed architecture is presented in Figure 7.2. For the purpose of this proof-of-concept, one or two baseband test signals (for single- or dual-band, respectively) are transmitted to the FPGA's internal BRAM memory through the interface with the baseband processing. The signals are continuously transmitted through a Polyphase Interpolation FIR filter, which increases the sampling rate by a factor of M distributed across M different paths. Thereafter, the two signals are upconverted to two symmetric intermediate frequencies around the DC component (SSB up-stage comprising reconfigurable polyphase

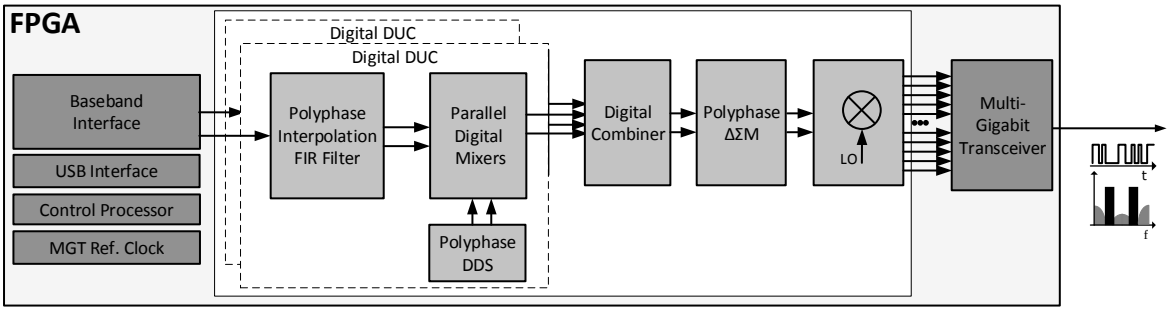


Figure 7.2: Block diagram of proposed tunable all-digital transmitter implemented in the FPGA, adapted from [DCOV16b].

DDS modules), which correspond to the frequency notches of the tunable ΔΣM. After that, they are combined and fed to the polyphase M-path tunable ΔΣM, whose output samples will then be combined and replicated to generate a parallel output word with the four components of the RF signal ($x_I(n)$, $x_Q(n)$ and their inverted versions), and serialized by the FPGA's MGT.

7.2.2 Prototype Validation

An ADT was fully implemented into a Virtex UltraScale XCVU095 FPGA using the Xilinx VCU1283 Characterization Kit.

Focusing on the ΔΣ topology, the design has fallen in the Error-feedback structure, whose illustration was already depicted in Figure 5.6. As introduced in Chapter 5, this modulator has one direct application: to design RF digital transmitters with a tunable IF. Moreover, taking into account that in the transition from LP-ΔΣM/HP-ΔΣM to BP-ΔΣM, two symmetric NTF's zeros arise, they can be exploited to perform dual-band transmission rather than transmitting just one band. Thus, by varying the α constant the system's configuration is changed, enabling the use of this modulator both in single- and dual-band applications.

After deriving the α variable, this modulator was optimized, with the aim of increasing the modulator's sampling frequency and, consequently, the maximum distance between bands. To accomplish this, the transfer function $H(z)$ was decomposed into a polyphase equivalent with two different phases and two outputs ($M = 2$) according to the theory discussed in [Vai93] and [COVS14].

The experimental setup of the FPGA-based ADT is depicted in Figure 7.3. The MGT was connected to a PA (ZHL-1042J), and then to a VSA R&S FSW 8. The MGT's sampling frequency was adjusted to 10 Gbps to provide a center frequency of 2.5 GHz and the ΔΣM's sampling frequency is 312.6 MHz divided into two different phases.

Experimental results in terms of spectrum and EVM measures were obtained with the VSA for two different scenarios: single-band and dual-band after the PA.

The table 7.3 shows the results obtained in a single-band scenario with different SRs. Con-

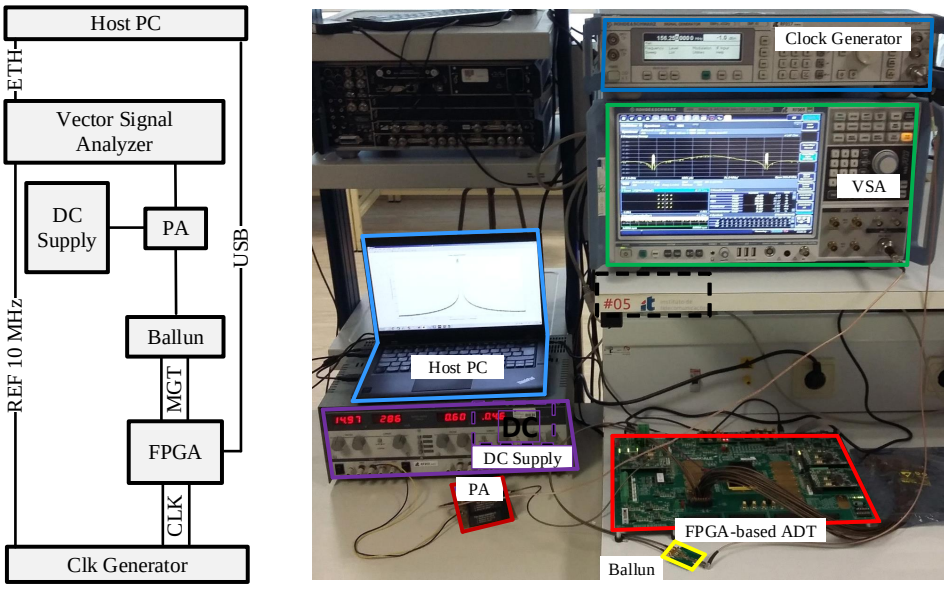


Figure 7.3: Photo of the experimental setup.

cerning the dual-band scenario, two symmetrical bands with different modulations (Quadrature Phase-Shifting Keying (QPSK) and 16-QAM) were tested for different frequencies and the results are depicted in table 7.2. Both tables present EVM values always below 4.5% resulting in a well-defined constellation.

Additionally, measurements after the polyphase $\Delta\Sigma$M block were carried out, showing that there was a degradation of approximately 1.5% introduced by the analog front-end (output buffer and PA). The choice of higher SR values for the single-band scenario is explained by the location of its $\Delta\Sigma$M's zeros (recall Figure 5.8). In this case, the $\Delta\Sigma$M is tuned to a low-pass configuration, resulting in two overlapped zeros in the NTF, which increases the processing bandwidth, accommodating carriers with higher SR. In the dual-band scenario, any two carrier frequencies may be chosen through the adequate selection of the central frequency and the spacing between the two carriers, provided that the distance between them does not exceed the modulator's sampling frequency. Moreover, if the hardware complexity is kept low, the sampling frequency can be raised at the expense of increasing the number of paths in the polyphase decomposition, resulting in higher frequency separation between the two different carriers.

For the used FPGA, the proposed system enables the design of a single-carrier tunable transmitter at 2.5 GHz of carrier frequency, or a dual-band configuration with a central frequency of 2.5 GHz and a separation between carriers up to 300 MHz. The carrier frequency can also be changed. However, as previously introduced, it is entangled with the serializer's sampling rate, and thus, its change is quite limited and leads to a modification of the Pulse Encoder's OSR.

Figure 7.4 shows the obtained spectrum after the PA for two modulated signals with a

Table 7.1
Single band scenario: EVM values for different SRs. (a) After ΔΣM (before DUC and serializer). (b) After serializer and PA.

(a)

	Symbol Rate (Msps)			
Modulation	3.125	6.250	13.021	15.625
QPSK	0.47	0.41	0.78	1.02
16-QAM	0.32	0.30	0.51	0.89
64-QAM	0.30	0.52	0.52	1.1

(b)

	Symbol Rate (Msps)			
Modulation	3.125	6.250	13.021	15.625
QPSK	1.33	1.79	2.23	2.60
16-QAM	1.50	1.88	2.49	3.01
64-QAM	1.44	1.89	2.66	2.91

Table 7.2
Dual Band scenario: EVM values for different carrier frequencies. (a) After ΔΣM (before DUC and serializer). (b) After serializer and PA.

(a)

	Upper Carrier Frequency (GHz)			
Modulation	2.506	2.538	2.568	2.600
QPSK	0.600	0.940	0.880	1.160
	Lower Carrier Frequency (GHz)			
Modulation	2.494	2.463	2.431	2.400
16-QAM	0.510	0.800	0.750	1.020

(b)

	Upper Carrier Frequency (GHz)			
Modulation	2.506	2.538	2.568	2.600
QPSK	1.67	2.52	2.660	3.47
	Lower Carrier Frequency (GHz)			
Modulation	2.494	2.463	2.431	2.400
16-QAM	1.77	2.46	3.15	4.34

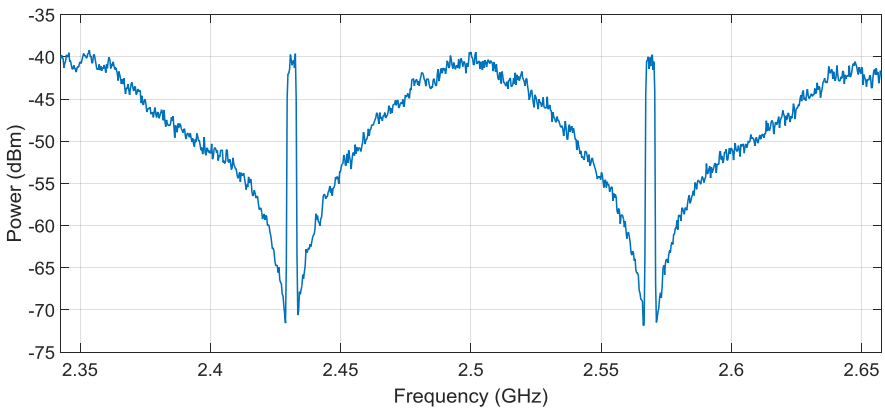


Figure 7.4: Spectrum of the transmitted signal in a dual-band scenario (RBW = 100 KHz, VBW = 2 KHz, SPAN = 315 MHz).

SR of 3.125 MHz: a QPSK at 2.5688 GHz and a 16-QAM at 2.431 GHz.

7.3 Enhancing the Dual-Band Figures-of-Merit through Pre-compensation

The previous section shows that the proposed architecture presents a significant degradation of the FoM in the dual-band experiment. In order to enhance the system performance in the dual-band scenario, it is worthwhile to deepen the DUC, taking into account that it is the only module between the ΔΣM and the serializer that can cause performance degradation.

7.3.1 Analysis of the Digital Upconversion Chain

In Section 2.2.4, the DUC used in BB-stage modulators was briefly introduced and, subsequently, it was demonstrated why the replication and combination of the encoded signals in the form of $[x_I[n], -x_Q[n], -x_I[n], x_Q[n]]$ leads to the upconversion from BB to one fourth of the serializer's sampling rate. However, an issue must be pointed out regarding this upconversion chain. Recalling 2.10, one should denote that just the real part of the output signal is considered. This leads to:

$$\begin{aligned} \widehat{x}_{RF}[n] &= Re\left[x_{INT}[n]e^{jw_c n}\right] \\ &= \frac{x_{INT}[n]e^{jw_c n} + x^*_{INT}[n]e^{-jw_c n}}{2} \end{aligned} \tag{7.1}$$

Equation (7.1) demonstrates that, by using this upconversion scheme, the spectral content of a conjugated signal image will be overlapped with the original spectrum, possibly corrupting the band of interest. This problem is exacerbated in the case of ADTs, due to the use of a discrete ZOH filter with accentuated sidelobes extending across the entire spectrum of frequencies. As it is graphically illustrated in Figure 7.5, when using an IF shifted from the carrier frequency, an aliased image appears in the symmetric IF value. Until now, this problem ended up being unknown and disregarded because the aliased image is hidden behind the quantization noise. However, this is not the case when symmetric bands are operated either for transmission/reception of different bands.

To minimize this problem, the first step involves modelling the whole system. In terms of frequency domain, the first two modules (upsampler and discrete ZOH filter) have the following frequency response: [Lyo10]

$$H_{zoh}(k) = e^{-j\left(\frac{\pi k(L-1)}{N}\right)} \left(\frac{\sin(\frac{\pi k L}{N})}{\sin(\frac{\pi k}{N})}\right) \tag{7.2}$$

where N is the length of the interpolated signal and k ranges from -$N/2$ to $N/2$-1. Considering

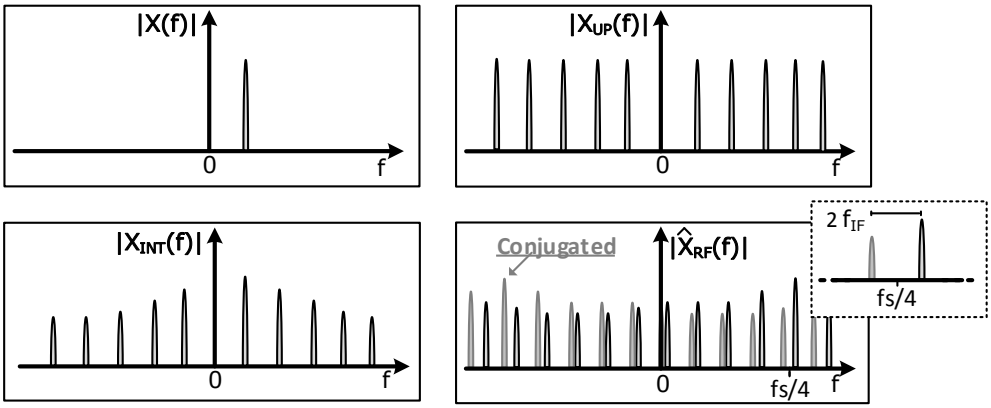


Figure 7.5: Illustration of a single-tone excitation considering the blocks from Figure 2.14.

that $f = \frac{k.Fs_{RF}}{N}$, the previous equation can be reinterpreted in order to get a function of f:

$$H_{zoh}(f) = e^{-j\left(\frac{\pi f}{Fs_{RF}}\left(\frac{Fs_{RF}}{Fs_{BB}}-1\right)\right)} \left(\frac{\sin(\frac{\pi f}{Fs_{BB}})}{\sin(\frac{\pi f}{Fs_{RF}})}\right) \tag{7.3}$$

To include the final upconversion stage that is required to translate the carriers from BB/IF to RF, this equation can be shifted to the center frequency w_c. The Discrete Fourier Transform (DFT) of $e^{jw_c n}$ is $\delta(w - w_c)$, resulting in:

$$H_{zoh}(f - f_c) = e^{-j\left(\frac{\pi(f-f_c)}{Fs_{RF}}\left(\frac{Fs_{RF}}{Fs_{BB}}-1\right)\right)} \left(\frac{\sin(\frac{\pi(f-f_c)}{Fs_{BB}})}{\sin(\frac{\pi(f-f_c)}{Fs_{RF}})}\right) \tag{7.4}$$

Finally, as previously introduced in (7.1):

$$\begin{aligned} \widehat{X}_{RF}(f) \quad = \quad & \frac{X(f) * H_{zoh}(f - f_c)}{2} + \\ & \frac{X^*(-f) * H^*_{zoh}(-f + f_c)}{2} \end{aligned} \tag{7.5}$$

7.3.2 Proposed Architecture

As previously introduced in the last subsection, the poor system's performance of the previous dual-band architecture is caused by a weak interpolation filter which introduces crosstalk between the two modulated bands.

In practical terms, focusing on the proposed dual-band scenario with two symmetric notches around a center frequency of $(Fs_{RF}/4)$, one can model this issue assuming that two modulated signals are being injected in two different and symmetrical bands (X_1 and X_2) around the DC component (f_i and $-f_i$, respectively), which will be propagated along

the upconversion chain and will result in two different and symmetrical bands (Y_1 and Y_2) around the center frequency ($Fs_{RF}/4+f_i$ and $Fs_{RF}/4-f_i$). In an ideal situation, no crosstalk would happen and, because of that, the system could be simply modeled as:

$$\begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} = I(z) \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \tag{7.6}$$

where Y_1 and Y_2 are the modulated signals from X_1 and X_2, respectively, merely translated into different carriers ($X_1 \rightarrow Y_1$ and $X_2 \rightarrow Y_2$).

The consideration of only the real-valued modulated signals results in the use of a *widely linear* or *linear-conjugate-linear* transformation which depends linearly on the variable and its conjugate [SS10]. In particular:

$$\begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} = H(z) \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} + C(z) \begin{bmatrix} X_1^* \\ X_2^* \end{bmatrix} \tag{7.7}$$

And, in this case:

$$\begin{aligned} H(z) &= \begin{bmatrix} H_{11} & 0 \\ 0 & H_{22} \end{bmatrix} \\ C(z) &= \begin{bmatrix} 0 & C_{12} \\ C_{21} & 0 \end{bmatrix} \end{aligned} \tag{7.8}$$

Both the $H's$ and $C's$ coefficients are linear transfer functions intrinsic to the upconversion chain and, because of that, invariant with the signal excitation. In practice, H_{11} and H_{22} characterize the attenuation/gain suffered by the modulated signals (namely, $X_1 \rightarrow Y_1$ and $X_2 \rightarrow Y_2$, respectively), while C_{21} and C_{12} characterize the amount of the conjugate input signals that is aliased to the opposite and symmetric band (namely, $X_1^* \rightarrow Y_2$ and $X_2^* \rightarrow Y_1$, respectively). According to the given formulation and neglecting an equalization (assuming the output should be $Y_1 = H_{11}X_1$ and $Y_2 = H_{22}X_2$), two input signals can be computed in order to perform a pre-compensation to minimize this cross-signal overlap between the two different bands:

$$W_1 = \frac{H_{11}^* H_{22} X_2 - C_{21} H_{11}^* X_1^*}{H_{11}^* H_{22} - C_{12}^* C_{21}} \tag{7.9}$$

$$W_2 = \frac{H_{11} H_{22}^* X_1 - C_{12} H_{22}^* X_2^*}{H_{11} H_{22}^* - C_{12} C_{21}^*} \tag{7.10}$$

Moreover, the crosstalk effect (C_{12}, C_{21}) is substantially lower than the system gain (H_{11}, H_{22}). This means that $|H_{11}H_{22}| >> |C_{12}C_{21}|$, and so, $H_{11}^* H_{22} - C_{12}^* C_{21} \simeq H_{11}^* H_{22}$

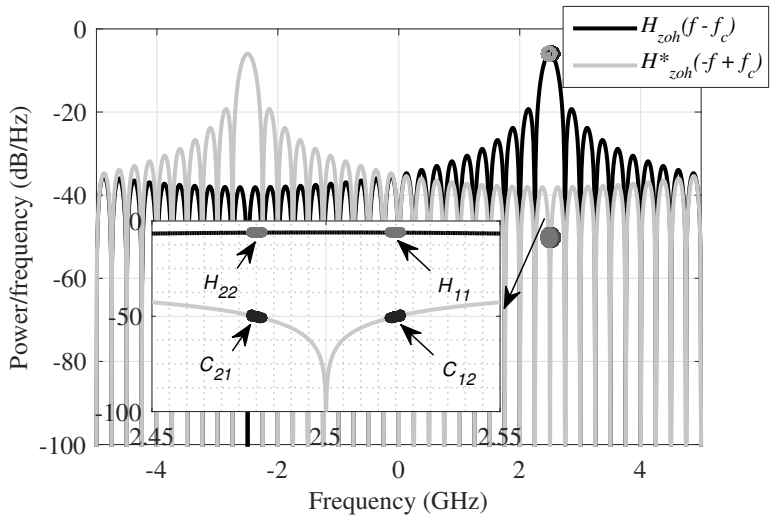


Figure 7.6: Frequency response of the upconversion chain (focusing in the addition between the complex-part with its conjugated to produce the real-part, as demonstrated in (7.5)) together with the interest bins of each transfer function (H_{11}, C_{12}, C_{21}, H_{22}) for an IF of 20 MHz and a SR of 3.125 Msps.

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and $H_{11}H_{22}^* - C_{12}C_{21}^* \simeq H_{11}H_{22}^*$, leading to:

$$W_1 \simeq X_2 + G_{21}X_1^* \tag{7.11}$$

$$W_2 \simeq X_1 + G_{12}X_2^* \tag{7.12}$$

with the pre-compensation filters $G_{21} = -\frac{C_{21}}{H_{22}}$ and $G_{12} = -\frac{C_{12}}{H_{11}}$. From the implementation point of view, the proposed pre-compensation scheme is based on a simple interconnect matrix between the two modulated bands that must be applied in the baseband processing before the upconversion chain.

To summarize, since one is dealing with just linear effects, the proposed solution is to minimize the crosstalk overlap between the two different bands with the inclusion of a pre-compensation signal in each band. To accomplish this, each signal's transfer function must have the same frequency response as the aliased image that one wants to remove (with an opposite phase) and must be amplified by the same amount that is lost along the upconversion chain.

To proceed with the validation of this pre-compensation method, the first step is the identification of the $H's$ and $C's$ transfer functions and, to do that, the frequency response from the whole DUC chain must be taken into account (7.4). In particular, one can verify that the transfer functions H_{11} and H_{22} are the magnitude/phase pair from all the bins of interest evaluated in $H_{zoh}(f - f_c)$, while, on the other hand, C_{12} and C_{21} are evaluated in $H_{zoh}^*(-f + f_c)$ (as can be seen in Figure 7.6).

Frequency-domain Filtering

The most straightforward implementation to assess the performance of this compensation method is based on frequency-domain filtering, where frequency sampling is performed to select the bins of interest, instead of relying on continuous-time solutions. Basically, all the operations between the transfer functions G_{12}, G_{21} and the input signals X_1 and X_2 are algebraically performed in the frequency-domain. To perform this, after selecting the bins of interest of each transfer function, a Fast Fourier Transform (FFT) (with the RF signal's length) is applied to the conjugate of each input signal (X_1^* and X_2^*) before upconversion to IF. After having the modulated signals in the frequency-domain, frequency domain filtering is applied, and then, an Inverse Fast Fourier Transform (IFFT) is required to get the two compensation signals (w_1 and w_2) in the time-domain:

$$w_1[n] = x_1[n] + \mathrm{IFFT}(\mathrm{FFT}(x_2^*[n])G_{12}) \tag{7.13}$$

$$w_2[n] = x_2[n] + \mathrm{IFFT}(\mathrm{FFT}(x_1^*[n])G_{21}) \tag{7.14}$$

An offline implementation of this compensation technique is completely straightforward due to the fact that no additional hardware is required. The pre-compensation signals must be computed in the baseband processing and combined with the input signals. Thus, the overall architecture from Figure 7.2 can be maintained. However, considering real-time constraints, an implementation of this technique is not particularly attractive in terms of required hardware. In this case, FFT/IFFT modules with a large number of points included within the FPGA may be required.

Time-domain Filtering

Rather than performing all the operations in the frequency-domain, the filters can be transferred to the time-domain and applied directly to the conjugate of the input signals:

$$w_1[n] = x_1[n] + x_2^*[n] * \mathrm{IFFT}(G_{12}) \tag{7.15}$$

$$w_2[n] = x_2[n] + x_1^*[n] * \mathrm{IFFT}(G_{21}) \tag{7.16}$$

A major advantage of this implementation is that as previously introduced, G_{12} and G_{21} are intrinsic transfer functions of the upconversion, which confers to the system the capability of performing online pre-compensation schemes.

The respective filtering topologies were optimized with the Parks-McClellan algorithm to just four complex coefficients for the filter ($g_{12,x}$ and $g_{21,x}$). More information related to the computation of these taps can be found in [DCB+16].

In conclusion, a pre-compensation method which requires computing and reloading four different complex coefficients for each filter ($g_{12,x}$ and $g_{21,x}$) for each IF value was proposed as

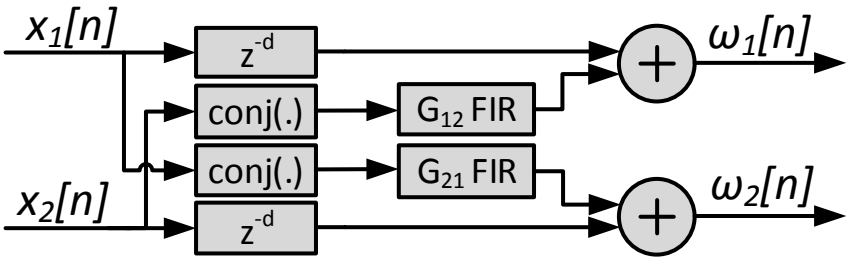

Figure 7.7: Block diagram of the pre-compensation mechanism that was included in the FPGA's hardware between the FPGA's internal memory (storing a baseband test signal) and the polyphase interpolation filters. The pre-compensation filters were designed with a 4th-order Transposed FIR filter topology, which presents a short critical path.

an architectural solution to enhance the dual-band FoM. Thus, the module responsible for the pre-compensation mechanism (depicted in Figure 7.7) must be included between the FPGA's internal memory (that are emulating the BB interface) and the polyphase interpolation FIR filters (recall Figure 7.2). The main block of this module comprises two complex-coefficient 4th-order filters, which, from the implementation point of view, is almost negligible.

7.3.3 Prototype Validation

To validate both the single- and the dual-band agile transmitter, as well as to assess the performance of the proposed pre-compensation method, the overall architecture was fully implemented into a Virtex UltraScale XCVU095 FPGA using the Xilinx VCU1287 Characterization Kit. The MGT's output was connected to a PA (ZHL-1042J), and then to a VSA R&S FSW 8 (as previously depicted in the photo of the experimental setup in Figure 7.3).

Spectrum and EVM measurements were obtained with the VSA for three different scenarios:

- Single-band with a LP-ΔΣM with no IF for different SR values (Table 7.3);
- Single-band with a BP-ΔΣM for different IF values (Figure 7.8);
- Dual-band with a BP-ΔΣM for different IF values (Figure 7.9). Measurements with the pre-compensation mechanism are also included in the same figure.

Changing the IF value is done in a straightforward way and in real-time by updating the set of variables that control the DDS, compensation filters and ΔΣM.

In all the experiments, the MGT's sampling frequency was adjusted to 10 Gbps to provide a center frequency of 2.5 GHz and the ΔΣM's global sampling rate is 250 MHz (2 phases running at 125 MHz). In the dual-band scenario, two symmetrical bands were tested with different modulations (QPSK and 16-QAM) and for different frequencies.

Table 7.3
Single-band performance with a LP-ΔΣM at 2.5 GHz. The results demonstrate the EVM (in %) after serializer and PA.

	Symbol Rate (Msps)			
Modulation	3.125	6.250	12.5	15.625
QPSK	0.76	0.90	1.36	1.70
16-QAM	0.78	0.92	1.33	1.82
64-QAM	0.78	0.93	1.37	1.83

All the experimental results present EVM values below 2.6% resulting in a well-defined constellation (Table 7.3, and Figures 7.8 and 7.9). In particular, the single-band with a LP-ΔΣM shows the best results with EVMs always below 2% even for an SR of 15.625 Msps. Concerning the dual-band scenario, two symmetrical bands were transmitted in different IF values. In Figure 7.9 one can verify the effectiveness of this pre-compensation mechanism with both implementation strategies (frequency-domain and time-domain). In fact, it was possible to decrease the EVM values down to the single-band ones, used as a baseline for proper comparison. It must be noted that to perform a fair comparison between the dual-band scenario with the single-band one, the input range of the latter was reduced to half, explaining the EVM's increase compared to the Figure 7.8. Furthermore, the EVM's periodical pattern is also expected and it can be explained through the illustration in Figure 7.6. The amount of noise from the transfer function $H_{zoh}(-f + f_c)^*$ will interfere more or less with the original band, depending on the IF value. Thus, the periodical pattern in the transfer function's magnitude response will directly affect the signal's quality. In particular, the signal's quality will be higher (lower EVM's value), every time the frequency value matches one of the sinc zeros.

For understanding the pre-compensation scheme's operation in a more straightforward way, a final measurement was performed with pre-compensation applied in a single-band scenario with a BP-ΔΣM, whose results are shown in Figure 7.10. In this experiment, the aliased image from the complex upconverted carrier in the symmetric band is almost completely eliminated when the pre-compensation is turned on, lowering the noise floor almost 15 dB in this specific band.

Figures 7.11 and 7.12 show two obtained spectra and constellations of a single-band with LP-ΔΣM and of a dual-band with a BP-ΔΣM, respectively.

7.4 Achieving the Concurrent Three-Band Transmission

In order to design a three-band modulator, the use of a BB-stage ADTs with a very limited NZ starts to become problematic. The maximum span between bands is always limited to the global sampling rate from the Pulse Encoder. Namely, the spans of 300 MHz and 250 MHz

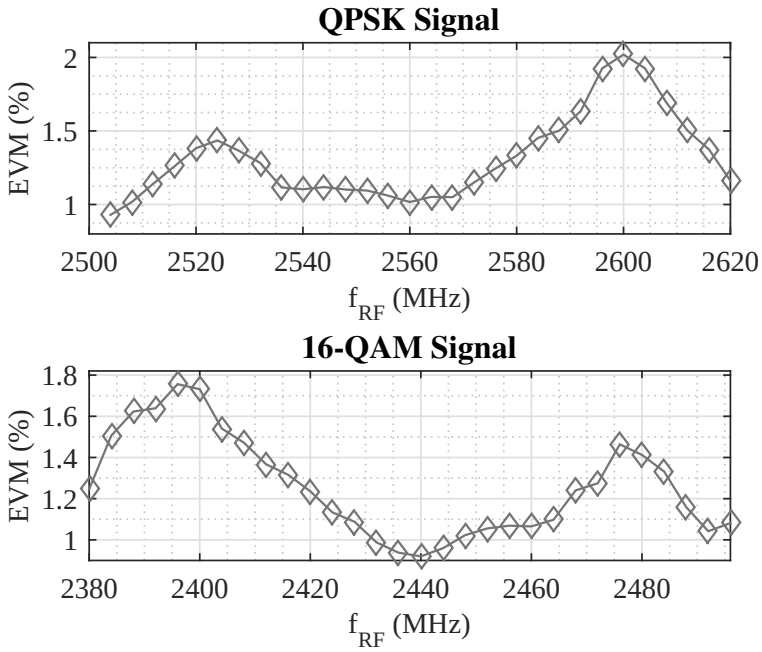

Figure 7.8: Single-band performance in a BP-ΔΣM scenario with a center frequency of 2.5 GHz and an IF ranging from ±2 MHz to ±120 MHz.

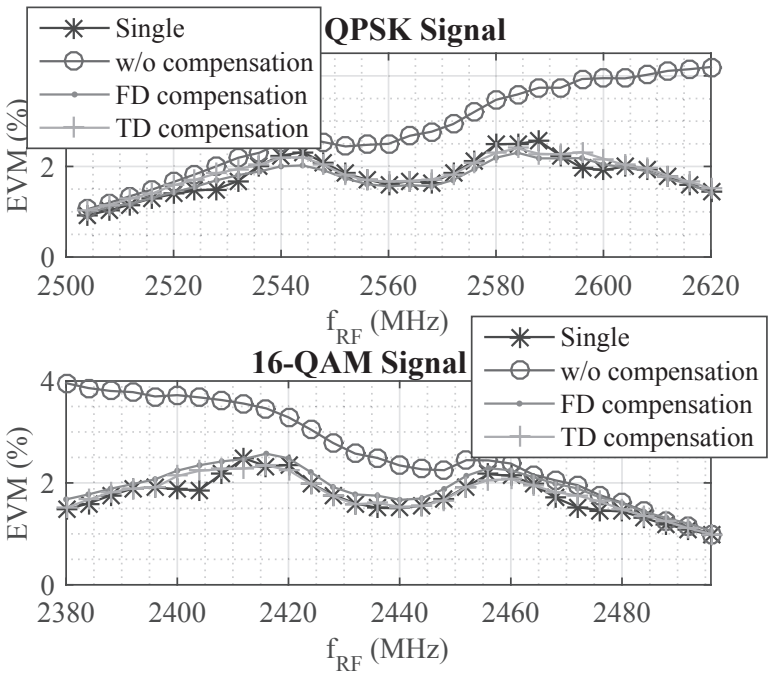

Figure 7.9: Dual-band performance in a BP-ΔΣM scenario with a center frequency of 2.5 GHz and an IF ranging from ±2 MHz to ±120 MHz. *FD compensation* and *TD compensation* represent the EVM results with the two compensation implementations (frequency- and time-domain, respectively).

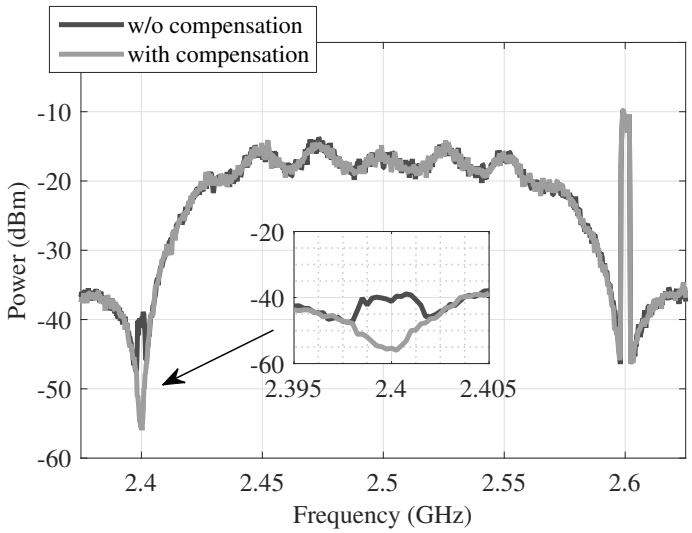

Figure 7.10: Pre-compensation mechanism applied into a single-band with a BP-ΔΣM. The transmitted signal is a QPSK with an SR of 3.125 Msps at 2.6 GHz (Resolution Bandwidth (RBW) = 100 kHz, Video Bandwidth (VBW) = 2 kHz and SPAN = 250 MHz).

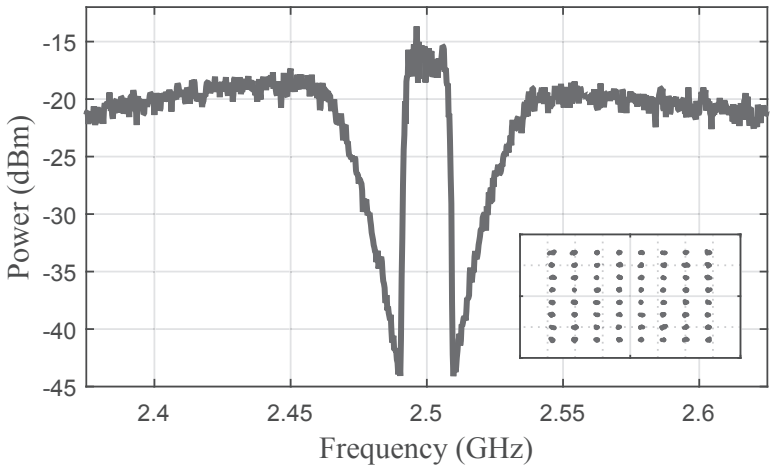

Figure 7.11: Spectrum of the transmitted signal (64-QAM with an SR of 15.625 Msps at 2.5 GHz) in a single-band scenario with a LP-ΔΣM (RBW = 100 kHz, VBW = 2 kHz and SPAN = 250 MHz).

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were achieved in the two previous sections. If three bands must be included, one can conclude that the span is too limited for a non-contiguous transmission. Thus, novel strategies must be explored to achieve a higher NZ, while taking into account the physical limitations imposed by the FPGA. For this reason, the architectures presented in the two previous sections cannot be considered, and a different one must be pursued.

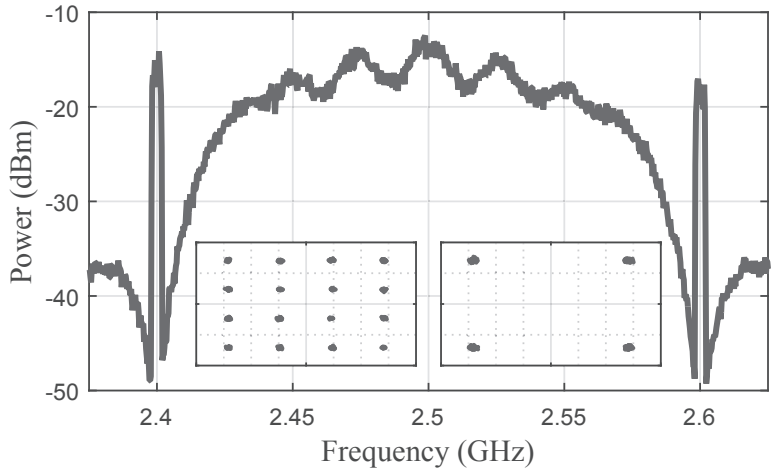


Figure 7.12: Spectrum of the transmitted signal in a dual-band scenario (QPSK at 2.6 GHz and 16-QAM at 2.4 GHz, both with an SR of 3.125 Msps) with a BP-ΔΣM (RBW = 100 kHz, VBW = 2 kHz and SPAN = 250 MHz).

7.4.1 Proposed Architecture

The proposed idea is to extend the single-band all-digital RF-stage architecture (proposed in [DCO+18] and introduced in Chapter 5) to enable the synthesis of triple-band RF transmitters. By taking advantage of the direct synthesis of RF waveforms in the digital domain before the Pulse Encoder, unprecedented frequency agility is achieved. To meet the specifications, highly parallelized architectures, which allow high equivalent sampling rates, must be explored.

At the same time, as the RF-stage architecture has an intensive utilization of the logical resources, the replication of fully digital RF chains to enable the multi-band capability is only possible with novel design methodologies and optimization techniques. Thus, two major modifications are proposed: the integration of the propagation of state-registers in the ΔΣ architecture (proposed in [DCO+17]) as a way to relax the resources usage; and the replacement of the FIFOs by a *Corner-Bender Matrix Transposer* from the Deinterleaving/Interleaving modules. The following subsections will briefly review the overall proposed architecture.

Digital Up-conversion Stage and Bands Combination

To enable the transmission of three different bands, the DUC stage must be replicated three times. The block diagram of each DUC was already introduced in Chapter 5. Similarly to the single-band architecture, the final bitrate Fs_{RF} defines the modulator's 1st Nyquist Zone (from 0 to $Fs_{RF}/2$). This means that the carrier frequency from each band can be located in any bin from the frequency grid given by the DDS' frequency resolution 5.1 within this Nyquist Zone.

Subsequently, the three interpolated and upconverted bands are combined to generate

an equivalent representation with N different phases that contains the three different bands. At the same time, the resultant signal must be scaled down to the suitable Pulse Encoder's dynamic range.

RF-stage Enhanced Multicore-based $\Delta\Sigma$M

The Pulse Encoder must be designed to reduce the number of output levels while ensuring minimal distortion in the three different bands. Moreover, the three different bands must be independently controlled and tunable, which typically implies the use of feedback loops to ensure some sort of noise-shaping. To accomplish these requirements, $\Delta\Sigma$ techniques were selected due to their inherent noise-shaping property that minimizes the amount of in-band distortion.

The propagation of state-registers is included in the Pulse Encoder to relax the resources usage. By adopting this technique, the periodicity of the impulsive noise can be reduced by a factor of N. In addition to this, this architecture allows the matching of the number of phases N with the number of contiguous samples K. This is of utmost importance because the Deinterleaving/Interleaving modules can be reduced to simply matrix transposers. When N is different from K, the design of Deinterleaving/Interleaving modules is typically done with resort to FIFOs. However, the allocation of distributed/block Random-Access Memory (RAM) for FIFOs typically leads to a low-occupancy rate. On the other hand, the design of matrix transposers is quite simple. The use of a *Corner-Bender Matrix Transposer* [A$^+$91] is proposed to maintain the desired functionality by just using registers and multiplexers.

The Corner-Bender Matrix Transposer is depicted in Figure 7.13. This design does not use any FIFO memories, it is fully synchronous, does not require any control signal and it only uses fixed size shift register delays. The latency is the minimal possible and equal to the number of contiguous samples (K). Moreover, the same module can be used to the Deinterleaving and Interleaving operations. In short, it will be seen that the inclusion of this module enabled a drastic reduction in BRAM primitive resource usage. In order to provide a clearer understanding, an example with four phases and four contiguous samples ($N = 4$ and $K = 4$) is also illustrated in Figure 7.14.

General Block Diagram

The general block diagram of the proposed architecture is depicted in Figure 7.15a. The detailed illustration of the Pulse Encoder is depicted in Figure 7.15b. One can clearly visualize the utilization of the Corner Bender Matrix Transposers as Deinterleaving and Interleaving Modules (referred to in the illustration as *DEINT/INT*). In addition to this, the displacement of the $\Delta\Sigma$Ms, together with the *Synchronous Start-up Control Logic* module, to enable the propagation of state registers [DCO$^+$17] is also illustrated.

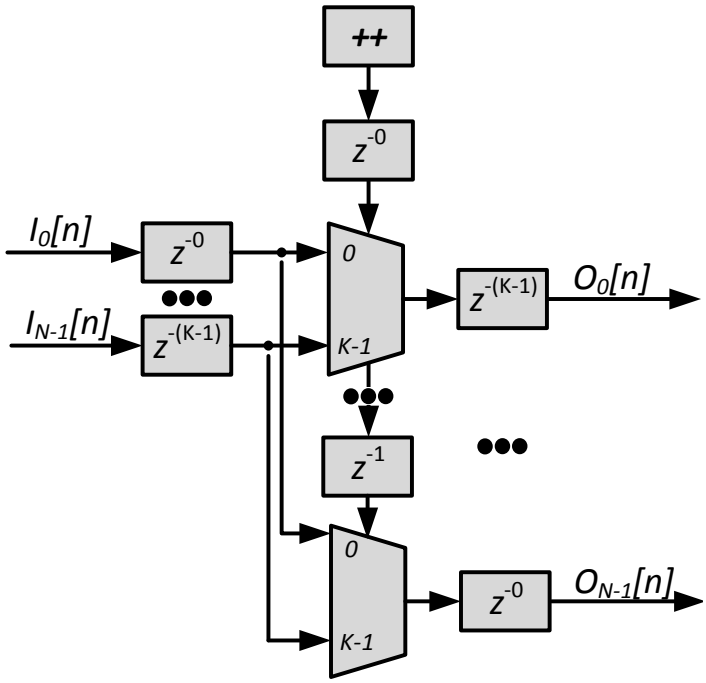


Figure 7.13: Illustration of the block diagram of a Corner-Bender Matrix Transposer. The designed Interleaving and Deinterleaving modules are based on this transposer.

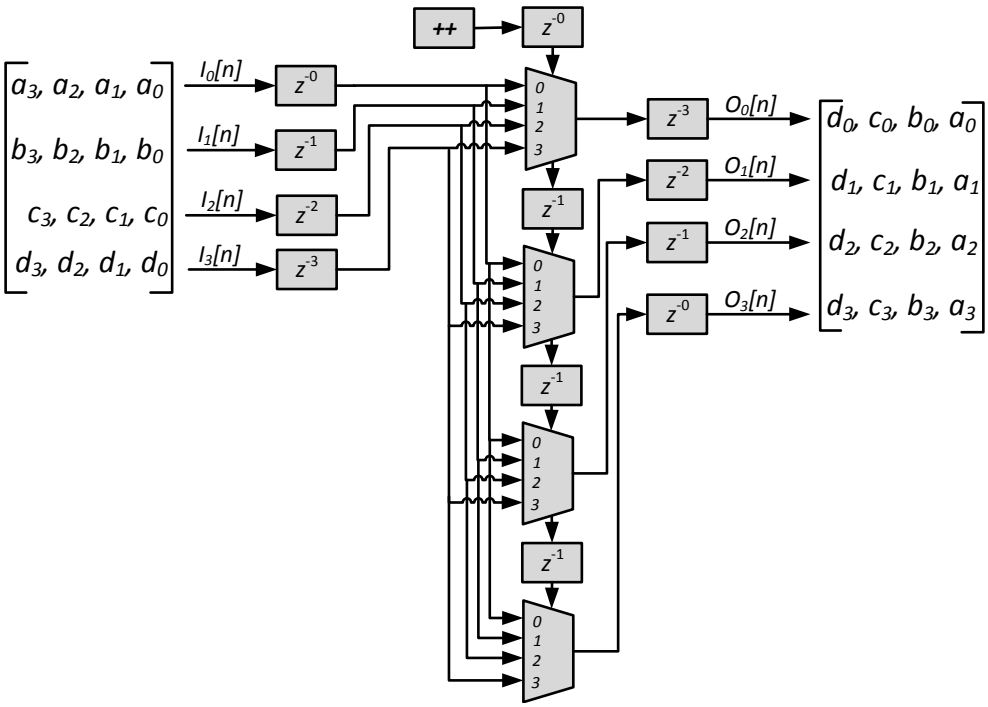


Figure 7.14: Illustration of a Corner-Bender with four phases and four contiguous samples ($N = 4$ and $K = 4$).

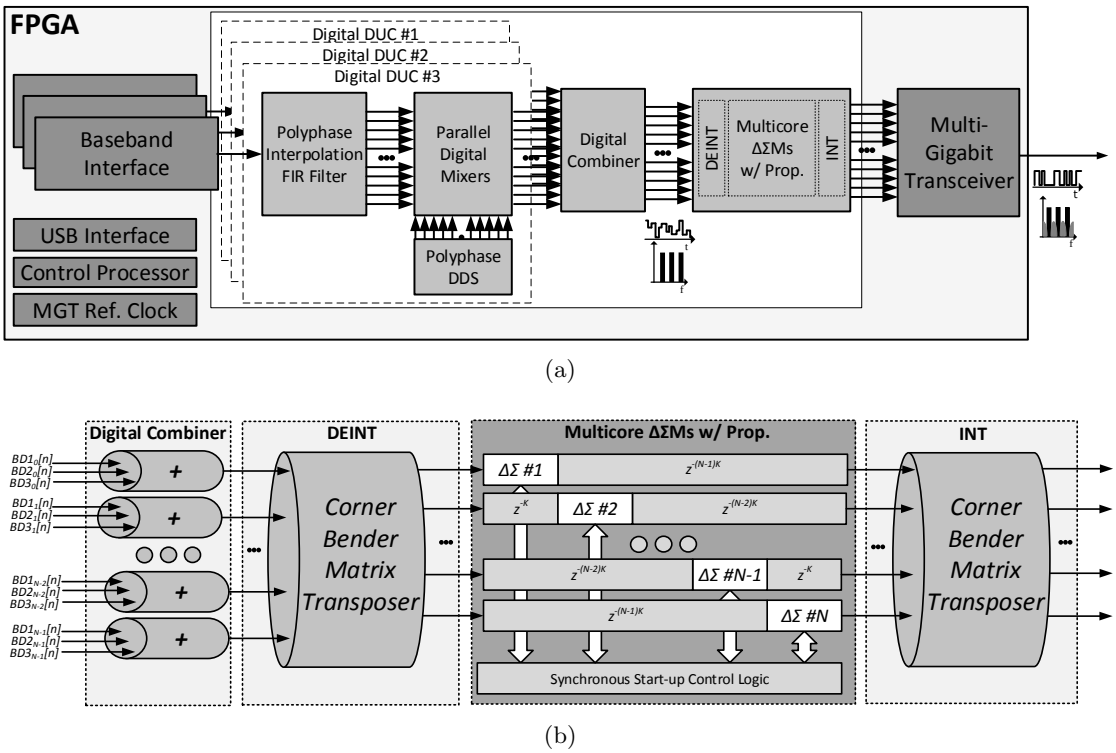


Figure 7.15: (a) General block diagram of the implemented All-Digital RF transmitter, embedded into an FPGA; (b) Detailed illustration of the Digital Combiner and the ΔΣM with N parallel stages, presented in (a).

A ΔΣ modulator must be designed and replicated N times, according to the architecture introduced in the last subsection. The choice of it must be done according to two different requirements. First, the architecture must present an NTF with three well-defined notches, to ensure the integrity of the three different bands. Second, the notches must also be tunable and independently controlled, to provide the desired real-time agility to the overall system. At last, the modulator's critical path must be as short as possible, which is the reason why the architectures such as Cascade-of-Resonators, FeedBack/FeedForward (CRFB/F) or Cascaded-of-Integrators, FeedBack/FeedForward (CIFB/F) can not be chosen.

Thus, the Error-Feedback ΔΣ architecture (depicted in Figure 5.6) was selected as a starting point for this work. By modelling the quantization noise as a random noise signal ($E_q(z)$), the following transfer function can be derived:

$$Y(z) = STF(z)X(z) - NTF(z)Eq(z) \tag{7.17}$$

where $STF(z) = 1$, $NTF(z) = (1+H(z))$ and $H(z) = \alpha z^{-1} + z^{-2}$. The modulator's behavior depends on the variable α, defined as $\alpha = -2\cos(2\pi F_{c1}/Fs)$, where F_{c1} is the notch center frequency and Fs is the modulator's sampling rate. In particular, it has two complex zeros

that allow the adjusment of the notch carrier as desired. An intuitive approach to achieve a triple band modulator could involved the inclusion of 2 pairs of other complex zeros, defined by β and γ:

$$NTF(z) = \left(1 + \alpha z^{-1} + z^{-2}\right) . \left(1 + \beta z^{-1} + z^{-2}\right) . \left(1 + \gamma z^{-1} + z^{-2}\right) \tag{7.18}$$

where $\beta = -2\cos(2\pi F_{c2}/Fs)$, $\gamma = -2\cos(2\pi F_{c3}/Fs)$ with F_{c2} and F_{c3} being the notches center frequencies.

However, for the used wireless modulated signals, this architecture may lead to stability issues, specifically depending on the notches placement. Thus, to control the NTF's gain, 6 complex poles were also included in the architecture. Each pair of poles closely follows each pair of zeros, to ensure the stability of the system, according to [RKR15]. This leads to:

$$NTF(z) = \frac{1 + \alpha z^{-1} + z^{-2}}{1 + r\alpha z^{-1} + r^2 z^{-2}} . \frac{1 + \beta z^{-1} + z^{-2}}{1 + r\beta z^{-1} + r^2 z^{-2}} . \frac{1 + \gamma z^{-1} + z^{-2}}{1 + r\gamma z^{-1} + r^2 z^{-2}} \tag{7.19}$$

where r ranges from 0 to 1, and controls the closeness between poles and zeros. This equation can be simplified to:

$$NTF(z) = \frac{1 + A_0 z^{-1} + B_0 z^{-2} + C_0 z^{-3} + D_0 z^{-4} + E_0 z^{-5} + z^{-6}}{1 + F_0 z^{-1} + G_0 z^{-2} + H_0 z^{-3} + I_0 z^{-4} + J_0 z^{-5} + K_0 z^{-6}} \tag{7.20}$$

where $A_0 = (\alpha + \beta + \gamma)$, $B_0 = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $C_0 = (2(\alpha + \beta) + \gamma(2 + \alpha\beta))$, $D_0 = (3 + \alpha\beta + \gamma(\alpha + \beta))$, $E_0 = (\alpha + \beta + \gamma)$, $F_0 = r(\alpha + \beta + \gamma)$, $G_0 = r^2(3 + \alpha\beta + \gamma(\alpha + \beta)$, $H_0 = r^3(2(\alpha + \beta) + \gamma(2 + \alpha\beta)$, $I_0 = r^4(3 + \alpha\beta + \gamma(\alpha + \beta)$, $J_0 = r^5(\alpha + \beta + \gamma)$ and $K_0 = r^6$.

In turn, the feedack loop transfer function ($H(z)$) can also be computed:

$$H(z) = \frac{A_1 z^{-1} + B_1 z^{-2} + C_1 z^{-3} + D_1 z^{-4} + E_1 z^{-5} + F_1 z^{-6}}{1 + F_0 z^{-1} + G_0 z^{-2} + H_0 z^{-3} + I_0 z^{-4} + J_0 z^{-5} + K_0 z^{-6}} \tag{7.21}$$

where $A_1 = (\alpha + \beta + \gamma)(1 - r)$, $B_1 = (3 + \alpha\beta + \gamma(\alpha + \beta))(1 - r^2)$, $C_1 = (2(\alpha + \beta) + \gamma(2 + \alpha\beta))(1 - r^3)$, $D_1 = (3 + \alpha\beta + \gamma(\alpha + \beta))(1 - r^4)$, $E_1 = (\alpha + \beta + \gamma)(1 - r^5)$ and $F_1 = (1 - r^6)$.

The impact of placing poles in $H(z)$ in terms of magnitude of the NTF is depicted in Figure 7.16. The magnitude is reduced, reducing the stability issues. However, as a drawback, the notches' bandwidth becomes lower.

Extension to Multi-Level Output

To enhance the system performance (assessed in terms of ACPR, EVM and SNR), a final stage that performs an extension to a multi-level output can also be included. The synthesis of this multi-level output is based on the combination of pulsed trains. The final architecture is depicted in Figure 7.18. Three major differences can be pointed out: the single-bit quantizer from each $\Delta\Sigma$M was replaced by a 7-level quantizer; 7 different MGTs were activated instead

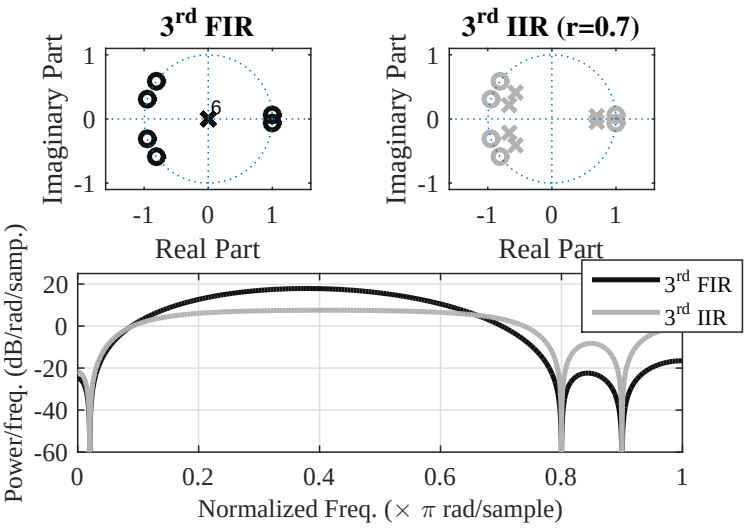


Figure 7.16: NTF's frequency response and zero-poles placement according to the different feedback-loop transfer functions.

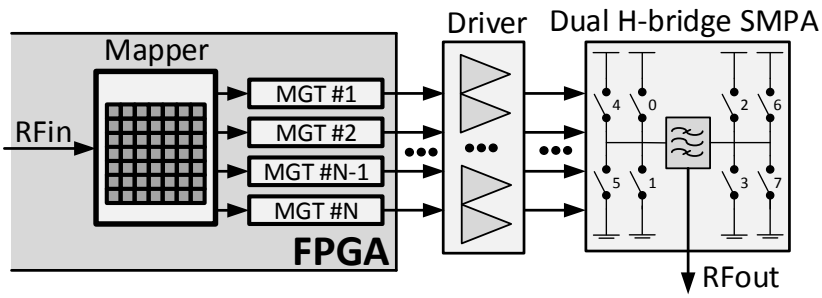


Figure 7.17: Detailed illustration of the proposed amplification scheme based on a dual H-bridge SMPA.

of just 1; and a Look-Up Table Mapper was included before the MGTs. This Look-Up Table Mapper is the core of this last stage and converts a multi-level input signal into a combination of 7 different pulsed train sequences. The mapper must be designed according to the used analog combination network.

The envisioned combination network to be applied in this architecture was firstly proposed in [CWK10], and an extension to 5-level was later reported in [ZMD+14a]. This increase in the number of levels is possible due to the use of an Asymmetric Extended H-bridge Combining Network, whose conceptual diagram is depicted in Figure 7.17. In particular, the switches from 4 up to 7 must have double size transistors when compared to the remaining ones. In the case of this combining network, the mapper is depicted in Table 7.4. In particular, one can realize that this mapper can generate a 3-level output (dark gray background), a 5-level output (dark gray and light gray background), or a 7-level output (by using all the table).

Table 7.4
Proposed mapper for the amplification scheme depicted in Figure 7.17.

RF_{in}	0	1	2	3	4	5	6	7
3	1	0	0	1	1	0	0	1
2	0	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0
-1	0	1	1	0	0	0	0	0
-2	0	0	0	0	0	1	1	0
-3	0	1	1	0	0	1	1	0

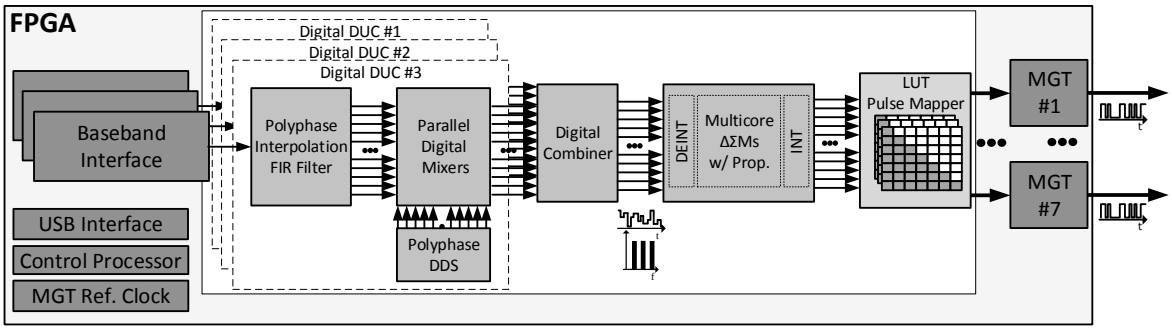


Figure 7.18: General block diagram of the implemented All-Digital RF transmitter, embedded into an FPGA with an extension to a multi-level output.

7.4.2 Prototype Validation

To validate the proposed multi-band architecture, the two different ADTs (depicted in Figures 7.15 and 7.18) were implemented in a Virtex 7XC7VX485T FPGA using the Xilinx FPGA VC707 Evaluation Kit.

The maximum timing constraints in the single-bit project imposed a maximum Fs_{BB} of 78.125 MHz, and consequently, with 64 different phases ($N = 64$), the bitrate of 5 Gbps was chosen. For the multi-level case, the implementation of a multi-bit quantizer caused a reduction of the maximum BB sampling rate down to 62.5 MHz, leading to the serializer's bitrate of 4 Gbps. The frequency resolutions can be computed by (5.1). In particular, the different bitrates together with the 10-bit resolution of the DDS' phase accumulator lead to 4.8828 MHz and 3.906 MHz, for the single-bit and 8-level case, respectively.

Due to the lack of a proper combining network based on this proposal, another option had to be chosen for the sake of validating the proof-of-concept. Thus, a conventional RF Power Combiner was utilized to perform the combination of the different serializers' outputs. In this case, the mapper had to be updated to Table 7.5. This new mapper can be simply seen as the linear combination of the pulse trains in order to achieve a higher number of output levels. One can also realize from Table 7.5 that the column related to the MGT_0 is constant.

Table 7.5
Implemented mapper for the use of assessment of the multi-level output with a Power-Combiner.

RF_{in}	MGT_0	MGT_1	MGT_2	MGT_3	MGT_4	MGT_5	MGT_6	MGT_7
3	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	0	0	0
-1	1	1	1	1	0	0	0	0
-2	1	1	1	0	0	0	0	0
-3	1	1	0	0	0	0	0	0

This means that one of the serializers could be removed. However, it was decided to keep it to maintain the coherency with the ideal combining network based on the H-bridge.

The experimental setups are depicted in Figure 7.19a and 7.19b, for the single- and multi-bit projects, respectively. In the first one, the MGT was directly connected to a VSA Keysight EXA N9010A. In the multi-bit project, lane-to-lane deskew techniques were implemented in the digital hardware, as well as extra delay lines were attached to some MGTs to ensure the lane-to-lane synchronism. Moreover, the amplitude swing of each MGT was slightly changed to ensure the same output power. Afterwards, the 7 MGTs were combined into a Power Combiner ZN8PD1-63W+ from Mini-Circuits. The combined output was connected to the same VSA. The VSA was configured to perform ACPR measurements as well as to record the I/Q data to be further analyzed in the VSA LabView Software running in the computer.

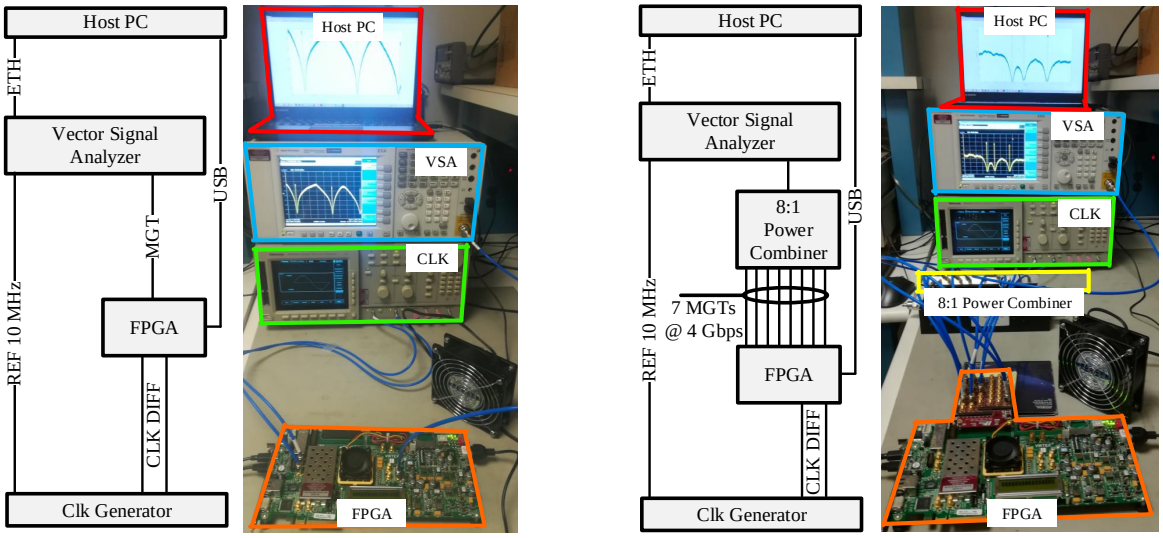
To enable the sweep of different carrier frequencies, modulations, bandwidths, and to record such FoM as spectrum, MER and EVM, an automated testbed was designed. This testbed has the host computer controlling/managing the FPGA-based ADT through a USB connection and connected to the VSA through an Ethernet connection. The different experimental setups are depicted in Figure 7.19. More information related to the sweep of carrier frequencies can be found in [DMS$^+$18].

Single-bit RF Transmission

This section details the experimental results for the single-bit project.

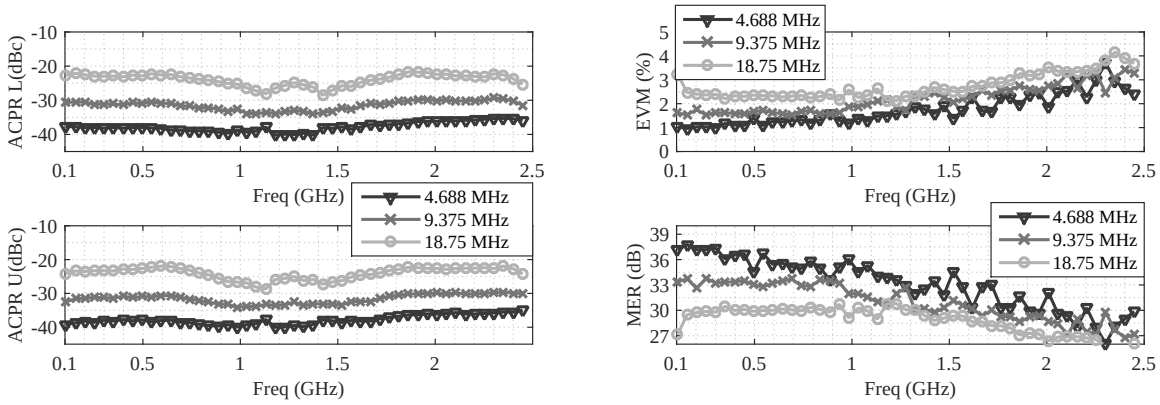
Figure 7.20a shows the measured ACPR results (lower and upper) in the range of 100 MHz up to 2.5 GHz, with a step of 48.828 MHz for three different bandwidths per band: 4.688 MHz, 9.375 MHz and 18.75 MHz. It can be seen that all the measurements maintain the same coherency: the increase of the bandwidth leads to higher quantization noise around the carrier frequencies, which consequently, increases the ACPR values. The signals with higher bandwidth present the worst results in terms of ACPR: between -20 and -30 dBc.

MER and EVM obtained pairs are reported in Figure 7.20b. Again, the same intuitive



(a) (b)

Figure 7.19: Photo of the experimental setup in the single-bit architecture (a) and in the 7-level architecture (b).

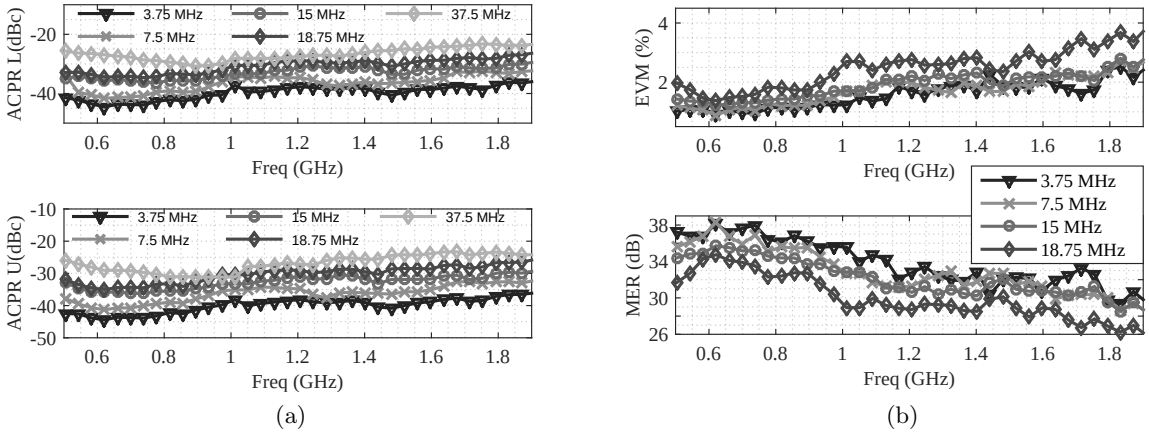


(a) (b)

Figure 7.20: Measured results of a sweep in the carrier frequency with a 16-QAM modulated signal with 4.588, 9.375 and 18.75 MHz in terms of: (a) Adjacent-Channel Power Ratio Lower (ACPR-L) and Adjacent-Channel Power Ratio Upper (ACPR-U); (b)EVM and MER.

conclusions can be extracted. Narrow bandwidths provide better FoMs. In particular, the maximum obtained MERs were 38, 35 and 31.5 dB, for the aforementioned bandwidths.

The spectrum in a span of 2.5 GHz, for carrier frequencies of 600.59 MHz, 2.002 and 2.4023 GHz, is shown in Figure 7.22a.



(a) (b)

Figure 7.21: Measured results of a sweep in the carrier frequency with a 16-QAM modulated signal with with 3.75, 7.5, 15 and 18.75 MHz in terms of: (a) ACPR-L and ACPR-U; (b)EVM and MER.

7-Level RF Transmission

This subsection details the experimental results for the concurrent 7-level 3-Band RF Transmission.

Figure 7.21a shows the measured ACPR results (lower and upper) in the range of 100 MHz up to 2.0 GHz, with a step of 39.062 MHz for five different bandwidths per band: 3.75 MHz, 7.5 MHz, 15 MHz, 18.75 MHz and 37.5 MHz. It can be seen that all the measurements maintain the same coherency: the increase of the bandwidth leads to higher quantization noise around the carrier frequencies, with the inherent increase in the ACPR values. The signals with higher bandwidth present the worst results in terms of ACPR: between -20 and -30 dBc. By comparing this figure with the single-bit one (Figure 7.20a), it is possible to understand the impact of using a multi-bit quantizer: the same results were achieved with twice the signal bandwidth.

MER and EVM obtained pairs are demonstrated in Figure 7.21b. Due to the limited available I/Q bandwidth from the VSA (25 MHz), it was not possible to get some measurements for the 37.5 MHz case. Again, the same intuitive conclusions can be extracted. Narrow bandwidths provide better FoMs. In particular, the maximum obtained MERs were 38, 37, 36 and 34 dB, for the aforementioned bandwidths.

The spectrum in a span of 2.0 GHz, for carrier frequencies of 500 MHz, 1.6016 and 1.9219 GHz is shown in Figure 7.22b.

Finally, the occupied resources in the FPGA for the single-bit and multi-level architectures are presented in Table 7.6. A high percentage of DSP slices is used in the parallel $\Delta\Sigma$M, as well as in the polyphase interpolation FIR filters. These filters were designed with a four-tap transposed direct-form architecture per phase. The inclusion of the Corner-Bender Matrix

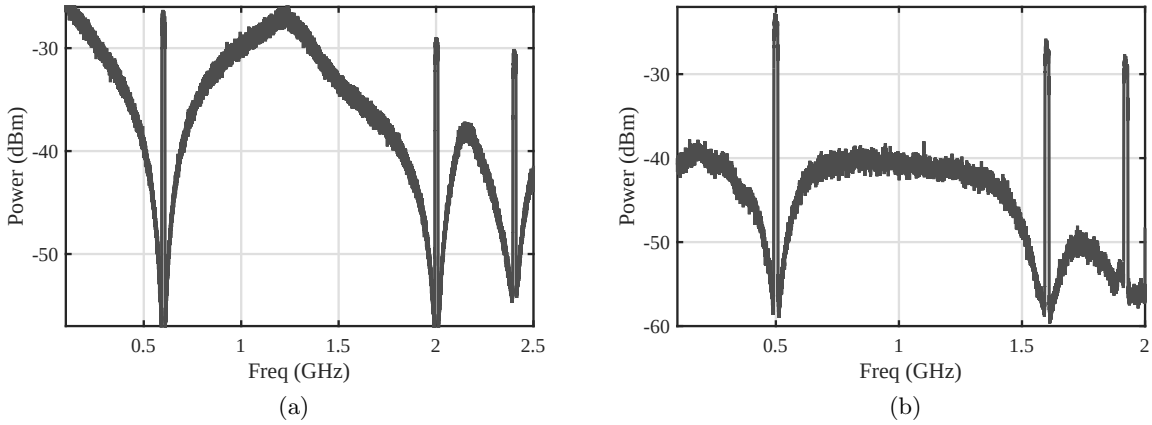


Figure 7.22: (a) Obtained spectrum in the single-bit architecture, with a full span of 2.5 GHz for carrier frequencies of 600.59 MHz, 2.002 and 2.4023 GHz, with a bandwidth of 18.75 MHz. ;(b) Obtained spectrum in the 7-level architecture, with a full span of 2 GHz for carrier frequencies of 500 MHz, 1.6016 and 1.9219 GHz, with a bandwidth of 18.75 MHz.

Table 7.6
Occupied resources for the single-bit and multi-level RF transmitter design

		Single-bit		Multi-level	
Logic Resources	Total	Used	%	Used	%
Flip Flops	607200	164944	27.16	174533	28.58
LUTs	303600	113123	37.26	140027	46.12
Memory LUT	130800	60045	45.91	74004	56.58
BRAM	1030	192	18.64	192	18.64
DSP48	2800	1876	67.00	1876	67.00
GTXs	27	1	3.7	7	25.9

Transposer enabled considerable savings in the BRAM primitive, as expected. In particular, in this project, the BRAM is just being used to accommodate the DDS's ROMs. Nonetheless, depending on the requirements, there is enough margin to implement an even more efficient memory usage through the exploration of the symmetry of the DDS' sinusoidal waveforms.

Comparison to the SoA

Table 7.7 presents an overview of the relevant modulators presented in the literature. The table aimed to focus on the number of transmitted bands, the achieved bandwidth per band, the maximum span between bands, the serializer's sampling rate, the modulator type, the number of levels from the output signal, the number of transmitters, the dependence of the carrier frequency with the serializer bitrate, the hardware implementation and, last but not least, the agility. By agility, one is referring to implementations or techniques that allow the

.

Table 7.7
Comparison of the proposed architectures with some relevant modulators from the SoA[1]

Reference	No. Bands	BW per Band (MHz)	Max. Span (GHz)	Fout (Gbps)	Mod. Type	No. Lev.	No. Tx	Fc indep. Fout	HW. Impl.	Agility
This (Impl.1)	**3**	**18.75**	**2.5**	**5**	**3rd EF RF-BPDSM**	**2**	**1**	**Yes**	**FPGA online**	**Yes**
This (Impl.2)	**3**	**37.5**	**2**	**4**	**3rd EF RF-BPDSM**	**7**	**7**	**Yes**	**FPGA online**	**Yes**
[MTKS13] (Impl.1)	2	5	0.7	3.9	6th CRFB RF-BPDSM	2	1	Yes	FPGA offline	No
[MTKS13] (Impl.2)	3	5	1	3.9	6th CRFB RF-BPDSM	2	1	Yes	FPGA offline	No
[CMS+17]	3	10	1.8	7	4th CRFB RF-BPDSM	32	2	Yes	AWG offline	No
[CMS+15]	2	20	0.60	24.5	6th CRFB RF-BPDSM	3	2	Yes	AWG offline	No
[DCB+16]	2	3.75	0.25	10	1st EF BB-BPDSM	2	1	No	FPGA online	Lim.
[SOC12a]	2	2	0.45	7.2	2nd CIFB BB-LPDSM	2	1	No	FPGA online	Lim.
[SOC13a]	3	<2	0.378	9	2nd CIFB BB-LPDSM	2	2	No	FPGA online	Lim.
[KI10]	2	10	0.6	6.14	8th CRFB BB-BPDSM	4	3	No	Simul.	-

[1]In the table, "n/a" and "-" stand for "not-available" and "not-applicable", respectively.

adjustment of the carrier frequency without changing the output's sampling rate.

Clearly, the two proposed implementations surpass the SoA in several aspects. In the first place, they are the first architectures to synthesize three different bands with maximum spans of 2.5 and 2 GHz with an online FPGA implementation. The maximum spans from the SoA (1 and 1.8 GHz) were achieved with offline FPGA/Arbitrary Waveform Generator (AWG)-based implementations [MTKS13, CMS+17].

The proposed architectures also demonstrate the highest bandwidth per band (18.75 and 37.5 MHz), leading to the highest aggregated bandwidth (56.25 and 112.5 MHz) from all the SoA. The previous maximum aggregated bandwidth (40 MHz) was reported in [CMS+15] with an offline AWG-based implementation and with 32 output levels.

In addition to that, it must be pointed out that this work is the first to present no additional OSR between the maximum span and the output sampling rate (generation is possible up to the Nyquist limit). Ultimately, this leads to a minimal output sampling rate, which is essential to minimize the switching losses from the amplification stage.

Lastly, one can also recognize that the proposed architectures are the first from the SoA to achieve real-time agility. This means that the three bands can be located in any bin from the

frequency grid given by the DDS' frequency resolution within the first Nyquist Zone (2.5 and 2 GHz, in the single-bit and multi-bit implementations, respectively). All the other approaches based on FPGA online implementations do not possess this capability, due to the fact that the DUC is applied after the Pulse Encoder (the concept of BB-stage ADTs introduced in [DCO+18]). It must be also stated that, as proposed in [DCO+18], when a fine frequency resolution is required, a single-rate digital-IF together with a single-rate high-resolution DDS should be included before the polyphase interpolation FIR filters.

One final note related to the scalability of this architecture must be highlighted. The main focus of this work was the proposal of a fully agile multi-band RF-stage transmitter, suitable for contiguous/non-contiguous CA scenarios, that could be embedded into programmable logic. First, even though a triple-band RF transmitter was implemented, the formulated design methodology is independent of the number of bands. However, each time that more bands are included, there is an additional increase in the critical path that forces the reduction of the serializer's sampling rate. In addition to this, more resources are also required. Thus, from a system designer's point-of-view, the inclusion of optimization techniques in terms of timing/area must be adopted. As far as the resources usage is concerned, it must be highlighted that the amount of logic resources that were reported in both implementations should not be taken as the minimum required values. Several different optimization techniques, in the critical subsystems, can always be done according to different requirements.

7.5 Summary and Concluding Remarks

This chapter presents three different works related to the design of concurrent multi-band ADT.

The first part of the chapter reports a BB-stage architecture that proposes the real-time displacement of the notches from a $\Delta\Sigma$ architecture to perform the single- or dual-band transmission of modulated data. The technique was proposed and validated in an FPGA. The system is able to change the distance between bands, provided that their maximum span cannot be higher than the modulator's sampling rate (300 MHz).

The proposed architecture is evolved in the second part of the chapter. Its major limitations were reported and theoretically formulated, and a precompensation technique is proposed and experimentally validated. The presented precompensation technique achieved a substantial improvement in terms of signal quality, comparatively with the previous dual-band work. Moreover, the precompensation technique was optimized in order to be implemented with minor modifications in the proposed hardware.

The chapter is concluded with the proposal of an RF-stage architecture aimed for the design of one up to three bands that can be digitally generated in any place in the range of 100 MHz up to 2.5 GHz. This architecture is particularly suited for the design of agile and

real-time reconfigurable ADTs for contiguous or noncontiguous CA scenarios. The technique was proposed and validated in an FPGA. The reported results demonstrate superior performance in terms of agility, the maximum span between bands (up to 2.5 GHz) and aggregated bandwidth (up to 56.25 MHz). To enhance the system performance, an extension to a multilevel architecture was also proposed, enabling the achievement of 112.5 MHz of aggregated bandwidth. In addition to the superior performance, as compared to the SoA counterparts, the fully digital behavior of this architecture shows strong potential to be synthesized in custom application specific integrated circuits.

In all the proposed architectures, the whole system frequency response can be updated in real time, allowing one to choose between single-band scenarios (with tunable carrier frequency), dual-band and triple-band scenarios (with tunable separation between bands).

The next chapter will introduce the main conclusions of this Ph.D. as well as the future work research lines that can be addressed.

Chapter 8

Conclusions and Future Work

The main motivation for this work was the proposal of innovative techniques that could leverage the concept of ADT to compete with the conventional counterparts in terms of the most important Figures of Merit within the context of 5G systems such as, transmission bandwidth, spectral purity, carrier agility, flexibility, and multi-band capability.

In this sense, Chapter 3 demonstrated an architecture that maintains the single-bit output, while achieving a drastic reduction of the out-of-band noise around the carrier frequency. The proposed architecture relies on the use of a 2-stage $\Delta\Sigma$M with different output levels and different sampling rates.

Chapter 4 reported on the first real and complete system, experimentally validated in terms of beamforming and beamsteering capabilities, where antenna arrays are directly driven by multiple ADTs fully integrated into the same FPGA.

The first architecture that enables the synthesis of an RF-stage modulator within an FPGA was proposed in Chapter 5. The underlying idea falls into the exploration of highly parallelized structures to achieve high global sampling rates. In particular, real-time agility in the range from 100 MHz up to 6 GHz with a maximum frequency resolution of 1.5625 MHz was demonstrated.

Chapter 6 demonstrated the design of RF-stage modulators combined with fully parallel $\Delta\Sigma$M with promising results in terms of bandwidth with reasonable serializer's sampling rates. In particular, 125 MHz of bandwidth were demonstrated with a single-bit architecture, and 1.25 GHz of bandwidth with a 3-bit architecture.

A set of different architectures suitable for concurrent dual- and triple-band transmission are reported in Chapter 7. Moreover, a pre-compensation was also proposed to minimize the amount of out-of-band noise that may be folded back to the interest bands in BB-stage modulators. In particular, in the dual-band case, real-time agility in the placement of up to two bands in the range of 300 MHz around the carrier frequency was demonstrated. In the triple-band case, up to three bands can be located in the range from 100 MHz up to 2.5 GHz with a frequency resolution of 4.88 MHz.

At last, one can conclude that this Ph.D. work successfully proposed innovative architectures that surpassed the SoA in the major research topics on the All-Digital RF Transmission.

As future work, and relying on the works presented in this thesis, one can highlight a set of research lines that could be followed aiming to explore and improve the characteristics of ADT in key aspects of future 5G communications systems, namely: massive MIMO, agility and transmission bandwidth.

First, advanced digital hardware optimization techniques could be explored in the design of ADTs with higher baseband sampling rates. Different state-of-the-art techniques, such as Look-Ahead Techniques, Borrow-Save Logic, and Vector Quantization could be studied, simulated and implemented into the presented designs. These optimizations could enhance the capabilities of the presented ADTs allowing to achieve even higher bandwidths (more than 1 GHz). To accomplish this, recent high-speed FPGAs with high-bitrate transceivers (such as GTY from Xilinx with 28 Gbps) should be physically assessed and integrated into the optimized designs.

Second, the proposed ADAAT could be further elaborated in both transmission bandwidth as well as in carrier frequency. As far as transmission bandwidth is concerned, the integration of RF-stage modulators in the ADAAT architecture would lead in a straightforward way to higher bandwidths. In terms of the carrier frequency, novel circuit-level techniques based on the integration of optical systems/circuits could be studied, proposed and experimentally validated, to enable the migration to high carrier frequencies with a massive number of radiant elements.

Lastly, novel techniques and architectures targeting increased system efficiency could be addressed. This inherently requires sound expertise in the design and implementation of analog components/subsystems as well as good control of the interfaces between the digital and analog domains.

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