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The STiC ASIC
High Precision Timing with Silicon Photomultipliers

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Abstract

In recent years, Silicon Photomultipliers are being increasingly used for Time of Flight measurements in particle detectors. To utilize the high intrinsic time resolution of these sensors in detector systems, the development of specialized, highly integrated readout electronics is required. In this thesis, a mixed-signal application specific integrated circuit, named STiC, has been developed, characterized and integrated in a detector system. STiC has been specifically designed for high precision timing measurements with SiPMs, and is in particular dedicated to the EndoTOFPET-US project, which aims to achieve a coincidence time resolution of 200 ps FWHM and an energy resolution of less than 20 % in an endoscopic positron emission tomography system. The chip integrates 64 high precision readout channels for SiPMs together with a digital core logic to process, store and transfer the recorded events to a data acquisition system.

The performance of the chip has been validated in coincidence measurements using detector modules consisting of $3.1 \times 3.1 \times 15\,\mathrm{mm}^3$ LYSO crystals coupled to Silicon Photomultipliers from Hamamatsu. The measurements show an energy resolution of 15 % FWHM for the detection of 511 keV photons. A coincidence time resolution of 213 ps FWHM has been measured, which is among the best resolution values achieved to date with this detector topology. STiC has been integrated in the EndoTOFPET-US detector system and has been chosen as the baseline design for the readout of SiPM sensors in the Mu3e experiment.

Zusammenfassung

Silizium Photomultiplier werden aufgrund ihrer hohen intrinsischen Zeitauflösung zunehmend für Laufzeitmessungen in Teilchendetektoren eingesetzt. Um die hohe Zeitauflösung der Sensoren den Detektorsystemen zugänglich zu machen ist die Entwicklung spezieller hochintegrierter Ausleseelektronik notwendig. In der vorliegende Arbeit wurde ein mixed-signal Application Specific Integrated Circuit, genannt STiC, entwickelt, charakterisiert und in einem Detektorsystem integriert. STiC wurde speziell für präzise Zeitmessungen mit SiPMs entwickelt, insbesondere für den Einsatz im EndoTOFPET-US Projekt, welches eine Koinzidenzzeitauflösung von 200 ps FWHM und eine Energieauflösung von 15 % in einem endoskopischen Positronen Emissions Tomographen anstrebt. Der Chip integriert 64 hochpräzise Auslesekanäle für SiPMs zusammen mit digitalen Schaltungen, welche die Signaldaten verarbeiten, speichern und an ein Datenauslesesystem senden.

Für die Bestimmung der Zeit- und Energieauflösung des Auslesesystems wurden Koinzidenzmessung mit Detektormodulen bestehend aus $3.1 \times 3.1 \times 15\,\mathrm{mm}^3$ LYSO Kristallen und Silizium Photomultiplier von Hamamatsu durchgeführt. Die Messungen weisen eine Energieauflösung von 15 % FWHM für die Detektion von 511 keV Photonen auf. Die dabei erzielte Koinzidenzzeitauflösung von 213 ps FWHM ist einer der bislang besten Werte für die Auflösung, welcher mit dieser Detektortopologie erreicht wurde. STiC wurde in dem EndoTOFPET-US Detektorsystem integriert und ist für Laufzeitmessungen mit SiPM Sensoren in dem Mu3e Projekt vorgesehen.

Contents

Chapter 1

Introduction

Particle physics aims at satisfying our curiosity as to what makes up the universe. The experimental exploration of the laws of particle physics relies on particle detectors, which are the tools that allow us to visualize elemental particles to measure their properties and interactions. The discoveries made with these machines refine our knowledge of particle physics and help to verify or disprove theoretical models with experimental data.

One of the first detectors developed is the Wilson cloud chamber [1], which uses a saturated water vapour as a detection medium to visualize the tracks of charged particles in a magnetic field. The vapour tracks left by particles traversing the chamber are observed with the naked eye, and photographs of the tracks are used for the analysis. Lacking a trigger mechanism to take only pictures of interesting events, these experiments required the manual evaluation of the photographs to find particle tracks for the analysis. As the interesting physical processes became more and more rare, these detectors became less practical due to the large amount of time required to find and analyse the relevant events.

This limitation was resolved by detector concepts that allow an electrical readout of particle events. Although their precision was, at first, inferior to that of cloud chambers, the possibility to trigger on event signatures and process their signals in a fraction of seconds provided an invaluable advantage. Since then, the manual readout of detectors has become obsolete and the electrical readout methods more and more sophisticated. As we advance in our knowledge of particle physics, the processes we want to observe become even more rare and the required measurement precisions become higher. In order to cope with these increasing requirements, a constant research and development effort has to be conducted in the field of particle detector physics. This effort is fostered by the rapid technological advancement of semiconductor technologies. The design of application-specific integrated circuits (ASICs), tailored to the parameters of the detector modules they are to read out, allows to uncover their full potential. They also provide the possibility to digitize analog electrical signals read from the modules at an early stage, eliminating the inevitable deterioration of the signal during an analog transmission to the outside of the system.

Apart from the improvements in the electronic readout of particle detectors, the development of solid state detectors, based on semiconductor technology, provides new sensors with a high precision and readout speed. One such device that has been developed in the recent years and that is used in this thesis is the Silicon Photomultiplier (SiPM) [2].

Many particle detectors rely, at least in part, on the conversion of energy depositions by particles into visible light pulses using scintillating materials. These scintillators are

subsequently read out by photo sensors providing an electrical signal proportional to the amount of detected light. The conventional device for this light readout is the photomultiplier tube, which was invented in 1930 by L.A. Kubetsky [3, 4]. This device uses the photo effect and an amplification mechanism which exploits the emission of secondary electrons to generate a measurable electrical signal from even a single photon. However, the dimensions of photomultiplier tubes are relatively large and their structure makes it impossible to operate the devices in strong magnetic fields.

Silicon Photomultiplier are solid state photo sensors with an amplification factor similar to photomultiplier tubes. In contrast to their conventional counterpart, the sensors are very compact and inherently insensitive to magnetic fields. In addition, their design makes them robust and cheap to manufacture. Because of this, they have become the method of choice for the readout of light in detector systems. Their small size allows a direct coupling to the scintillator medium and promotes the concept of highly integrated granular detector systems. In addition, Silicon Photomultiplier are able to provide a high timing resolution, which can be exploited to further increase the sensitivity of a detector system by also including the signal timing in the analysis.

The technological developments in the field of particle detectors have not only led to many important discoveries in particle physics, but are also used in many other research fields such as nuclear medicine. The detection of high energetic photons from positron annihilations is the fundamental principle of positron emission tomography (PET), a medical imaging technique capable of monitoring the metabolic activity in a body. In combination with a radioactive tracer substance, this technique allows to locate tumor cells in a body and has become a state of the art diagnosis tool for cancer treatment. The continuous improvement of detector technologies provides an increased sensitivity of PET systems and thus resolution of this imaging technique. The higher sensitivity also reduces the amount of required radioactive dose injected into the patient. Because of their insensitivity to magnetic fields, Silicon Photomultipliers provide the possibility to integrate detectors for PET imaging together with magnetic resonance imaging (MRI), allowing to simultaneously record an image of the body tissue overlaid with the information of the metabolic activity. A combined image of these complementary imaging techniques usually requires the acquisition of two separate images, which have to be manually overlaid and aligned. The high timing resolution possible with SiPMs is furthermore exploited in Time-of-Flight (ToF) PET systems, where the measurement of the arrival time of the annihilation photons is used to significantly increase the sensitivity of the image reconstruction.

The full potential of Silicon Photomultipliers can only be provided to a detector system by the development of dedicated readout electronics. Especially the high timing resolution possible with the sensors has not yet been fully exploited in larger detector systems. In this dissertation, the development of the Silicon Photomultiplier Timing Chip (STiC), a mixed mode readout ASIC for SiPMs is presented. The chip has been developed at the Kirchhoff-Institute in Heidelberg in the framework of the EndoTOFPET-US[5] project to provide a very high timing resolution to applications in medical imaging and particle physics using SiPMs as light sensors.

Due to the complexity of such a highly integrated system, the development, characterization and system integration of the ASIC has been performed by a collaboration of people at the Kirchhoff-Institute Heidelberg and within the EndoTOFPET-US project. In the context of this thesis, the author has made essential contributions to all development steps, from the design of the chip up to its integration in the EndoTOFPET-US detector system.

During the design process of STiC, the author has developed the digital circuits as well as the mixed-signal back-end design of two generations of the STiC chip. This comprises the integration of analog signal processing blocks together with the digital logic in a combined readout system. The digital and mixed-signal systems have been verified by the author in simulations before submitting the ASIC for production.

The configuration of the chip and the readout of event data requires a dedicated data acquisition (DAQ) system, which has been designed using existing field-programmable gate array boards. The author has developed the firmware and software of this DAQ system, in order to communicate with the ASIC and analyze the recorded events. With this readout system, characterization measurements have been performed to verify the performance of STiC in Time-of-Flight detector systems.

For the integration of the developed ASIC in the EndoTOFPET-US detector system, the author took part in the assembly of readout modules using STiC and the commissioning of the modules in the detector system. In this context, an automated characterization procedure has been devised and all produced detector modules were tested before the assembly in the system. During the commissioning, the author also contributed to the development of the firmware and software of the detector DAQ system.

The first chapter of this dissertation presents two applications which are currently using the STiC ASIC for timing measurements with Silicon Photomultiplier. In Chapter 3, the design of SiPMs and the important aspects of timing measurement with these sensors, including the implications for the readout electronics are discussed. The design and characterization of the developed readout chip is presented in Chapter 5 and 6. The last chapter presents the integration of detector modules hosting the STiC ASIC in the detector system of the EndoTOFPET-US project.

Chapter 2

Time of Flight Experiments

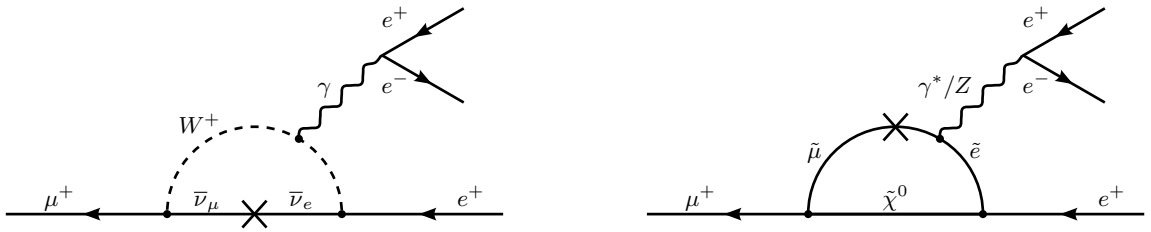
Many state-of-the-art detector systems utilize the event timing of detected particles in order to push their sensitivity to the possible limits. By including the time information for coincidence or Time-of-Flight measurements in the analysis, a significant portion of background processes can be distinguished from the desired signal events. This provides a higher signal-to-noise ratio (SNR) and thus sensitivity of the detector system.

For nuclear medicine applications, especially positron emission tomography, the possibility to achieve higher detector sensitivities translates to faster image reconstruction times and a smaller amount of the required radioactive tracer molecules, without sacrificing the image quality and resolution. Most radioactive isotopes used for PET imaging have to be produced on-sight of the hospital due to their short half-lives, which makes them expensive. Therefore, in addition to reducing the radioactive strain on the patients, which has to be kept as low as possible, the increased detector sensitivity also reduces the cost of a PET scan. The reduced radioactive dose and application cost could promote the use of this powerful diagnosing technique for a wider range of medical cases.

In this chapter, two projects using the STiC ASIC for high precision timing measurements with Silicon Photomultipliers are presented. The EndoTOFPET-US project [5] is developing a novel endoscopic positron emission tomography detector system for early stage pancreas and prostate cancer diagnosis. STiC has been developed in the framework of this project and its specifications are derived from the requirements of the corresponding detector system, which will be described in more detail in Section 2.2. The very high timing resolution achievable with this chip is a common requirement for many applications and it is consequently evaluated for the readout in several different projects, such as the Mu3e experiment. A brief summary of this project based on the corresponding research proposal [6] is presented in the next section.

2.1 Mu3e

In the Standard Model (SM) of particle physics, the lepton numbers L_e, L_μ, and L_τ of the individual lepton flavours are conserved at tree level. However, lepton flavour violation has been observed in neutrino oscillations by several experiments, such as Super-Kamiokande [7] and Sno [8]. Consequently, lepton flavour is a broken symmetry. Although the neutrino oscillations also introduce flavour mixing to charged leptons, charged lepton flavour violation (CLFV) is heavily suppressed in the standard model due to the negligible mass of the neutrinos. The observation of CLFV transitions would therefore be a clear signal of new physics beyond the



(a) Dominant neutrino mixing loop diagram in SM theory.

(b) Loop diagram for CLVF involving supersymmetric particles.

Figure 2.1: Loop diagrams for the charged lepton flavour violating μ^+ decay into two positrons and one electron.

standard model.

The charged lepton flavour violating decay $\mu \to eee$ is the focus of the Mu3e experiment. It's dominant SM loop diagram is shown in Figure 2.1a. The vanishing branching ratio of $\mathrm{BR}(\mu \to eee) \ll 10^{-50}$ predicted by the SM makes this decay an ideal probe for new physics. New particles beyond the standard model, such as super symmetric particles, would contribute to the loop diagrams as shown in Figure 2.1b, thereby significantly increasing the branching ratio of this decay channel. The goal of the Mu3e experiment is therefore to search for the $\mu \to eee$ decay with an unprecedented sensitivity of 10^{-16}. Even in the case that no CLFV decay is observed, the experiment would still improve the current exclusion limit of $\mathrm{BR}(\mu \to eee) < 1.0 \times 10^{-12}$ [9] by 4 orders of magnitude, putting stringent limits on lepton flavour violating theory models. The indirect search is complementary to direct searches conducted for example at the Large Hadron Collider (LHC), providing an additional probe sensitive to energy scales above the ones currently accessible by direct measurements.

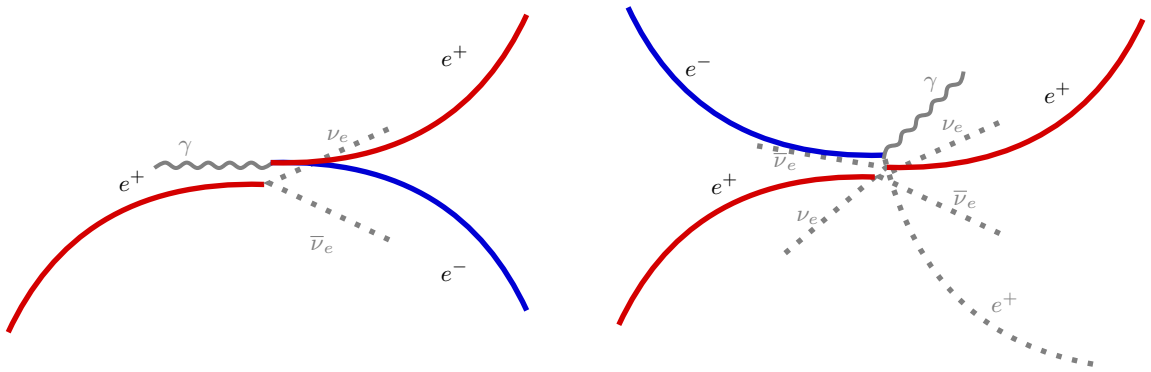
To achieve the high sensitivity of 10^{-16}, the Mu3e experiment will make use of a new high intensity muon beam line to be installed at the Paul Scherrer Institute (PSI) in Zürich. The new beam line will deliver more than 10^9 muons/s, which are stopped in a target and decay inside the detector volume. The detector system itself has to be able to reject the various irreducible and accidental background sources at very high event rates. The decays contributing to background events and the foreseen detector design, as presented in the research proposal, will be summarized in the following sections.

2.1.1 The $\mu \to eee$ Decay

The signal of the $\mu^+ \to e^+e^+e^-$ decay consists of two positrons and an electron, with a total energy equal to the muon mass. Since the muons are stopped in a target and decay at rest, the vectorial sum of the individual electron momenta has to vanish. These conditions can also be written as

$$\begin{aligned} &\textstyle\sum_i E_i = m_\mu \,, \text{ and} \\ &\textstyle\sum_i p_i = p_{tot} = 0 \,. \end{aligned} \tag{2.1}$$

Several decay processes exist which can fake this signal and contribute to background



(a) Michel decay and photoconversion **(b)** 2 Michel decays and photoconversion

Figure 2.2: Accidental background sources to the $\mu \to eee$ signal.

events. These can be grouped into irreducible and accidental background sources. To the irreducible background sources belongs the internal conversion decay $\mu^+ \to e^+e^+e^-\nu_e\overline{\nu}_\mu$. By enforcing the conditions in Equation 2.1, internal conversion decays can be separated from the true signal events by the missing energy and momentum of the escaping neutrinos. The energy and momentum resolution are therefore a critical parameter of the detector design, as they determine how well these background events can be distinguished from the real signal.

The dominant muon decay is the so called Michel decay $\mu^+ \to e^+\overline{\nu}_\mu\nu_e$. Although no negatively charged electrons are generated in this process, misidentified positron tracks together with other Michel decays in the detector could lead to background events. Another allowed decay channel of the muon is the radiative decay $\mu^+ \to e^+\gamma\overline{\nu}_\mu\nu_e$. Via photoconversion, the additional photon can generate an e^+e^- pair, introducing negatively charged electrons to the events. In addition to photon conversion, positrons undergoing Bhabha scattering, and the decay of pions polluting the muon beam can generate electrons in the detector volume and contribute to accidental background events. However, the individual processes can only contribute to the background, if several decays occur almost simultaneously, as it is shown in Figure 2.2. Since the events are not correlated, the decay products have the possibility to pass the energy and momentum selections from Equation 2.1. Only the vertex reconstruction and the time difference between the contributing decay processes can distinguish such events from a real signal, which would proceed promptly. The rate of accidental background events increases with the intensity of the muon beam, and the probability to measure several decays within a short time frame rises. At a rate of more than 10^9 muon decays per second, a high timing resolution in the picosecond range has to be achieved for the event timing to disentangle the individual decay origins from one another and reject the combinatorial background sources.

2.1.2 The Mu3e Detector

A sketch of the envisioned Mu3e detector design and its individual subsystems is shown in Figure 2.3. It uses a cylindrical shape around a cone shaped target, which is placed inside a 1 T solenoid magnet. The length of the final detector system will be 2 m. Two double layers of a

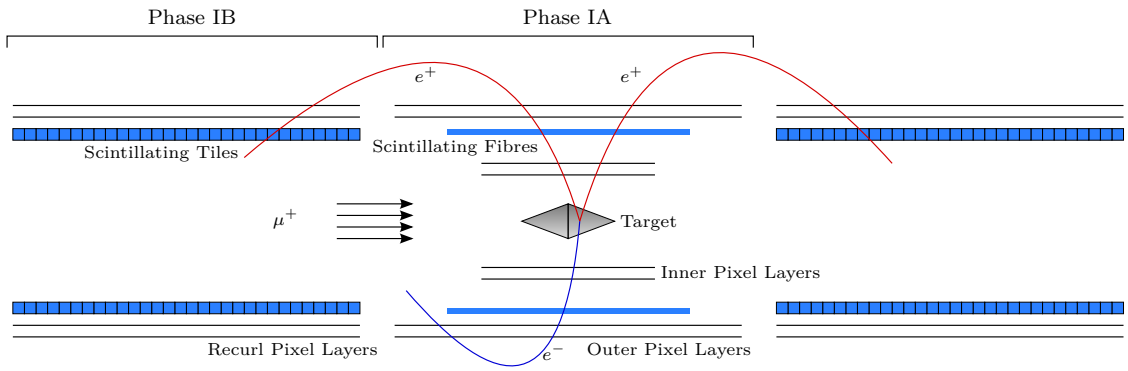


Figure 2.3: Concept of the envisioned Mu3e detector [6].

silicon pixel tracker based on novel high-voltage monolithic active pixel sensor (HV-MAPS) [10] provide a high precision measurement of the particle tracks and their momenta inside the magnetic field. The outer silicon pixel layers are extended in the longitudinal directions to further increase the precision of the momentum measurement by using tracking information of recurling electrons. Since the momentum resolution in the relevant electron energy range is limited by multiple Coulomb scattering, the project pursues an ambitious approach of HV-MAPS sensors thinned to a thickness of 50 μm, mounted on Kapton foils of 25 μm thickness. In this way, the material inside the detector volume, and thus the probability of Coulomb scattering, is significantly reduced.

The timing resolution of approximately 20 ns of the pixel layers is however not sufficient to suppress the accidental background sources. Because of this, the silicon tracker is supplemented by two additional timing systems, consisting of scintillating fibres and tiles coupled to Silicon Photomultipliers. Due to the constraints on the material budget inside the detector volume, the scintillating fibres between the inner and outer silicon trackers modules consists of 250 μm thick fibres stacked in up to 5 layers. The timing resolution achievable with the scintillating fibre readout is expected to be $\sigma < 300$ ps. As the last detector module to be hit by recurling electron tracks, the scintillating tiles are not subject to the severe material constraints. The tile geometry can therefore be optimised to provide the best timing performance possible. The currently foreseen tiles consist of $6.5 \times 6.0 \times 5.0\,\text{mm}^3$ segments, using BC418 as an organic scintillator material. The targeted timing resolution for the tile detector is $\sigma < 100$ ps to provide sufficient background rejection power at high muon decay rates.

The design of the entire detector system is kept modular, allowing to commission it in several phases, as it is also indicated in Figure 2.3. The very first phase (phase IA) will consist only of the silicon tracker modules, without the recurl pixel layers. In this minimal configuration, the detector is already able to reconstruct tracks and decay vertices, which is sufficient to begin the search for the $\mu^+ \to e^+e^+e^-$ decay at lower muon beam intensities. In the second phase (Phase IB), the timing systems and recurl pixel layers will be added, increasing the momentum resolution and allowing the detector to cope with the additional accidental background at higher event rates. In phase II, which is not shown in Figure 2.3, the

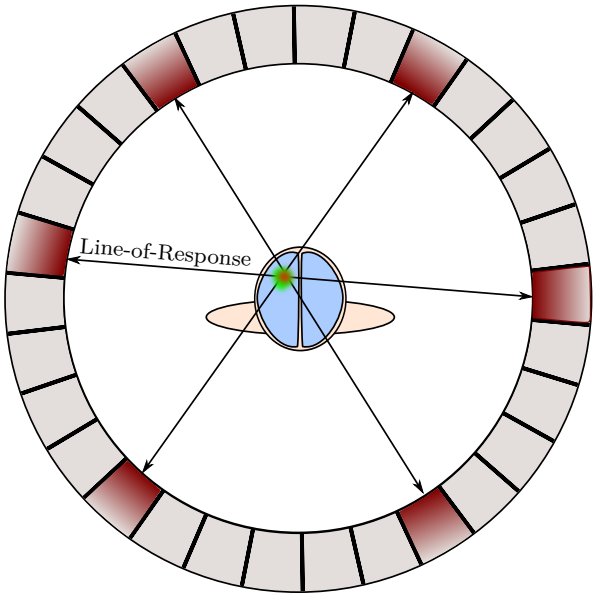


Figure 2.4: Concept of image reconstruction in PET scanner.

detector is extended on each side by another segment of recurl pixel layers and tile detectors to allow measurements at very high muon decay rates.

The high timing resolution of the STiC ASIC is used in the Mu3e detector system for the readout of the scintillating fibres and tiles. Detailed studies of the tile detector timing performance using STiC and various tile geometries in test beam measurements have been performed in [11]. Timing resolutions of less than 100 ps have been achieved in these studies, showing that STiC can provide the required performance to the system.

2.2 The EndoToFPET-US project

Positron emission tomography is a non-invasive medical imaging technique that allows to reconstruct the functional processes inside a body. In this it is complementary to anatomical imaging techniques such as magnetic resonance imaging (MRI) or computer tomography (CT). The possibility to monitor the metabolism and indicate regions of abnormal cell growth provides important information to the physicians for the diagnosis and treatment of diseases such as cancer.

In order to build an image of the functional processes, a PET scanner reconstructs the distribution of tracer molecules that are injected into the body. The tracer substance is chosen to partake in the metabolic functions of the body. Due to their increased cell growth, tumor cells require a higher amount of glucose. Radiopharmaceuticals, such as the glucose analog Fluordeoxyglucose (FDG), can be used to mark such areas of high glucose uptake in the body and in this way indicate tumors.

The radioactive isotope of the tracer molecule (^{18}F in the case of FDG) decays via the

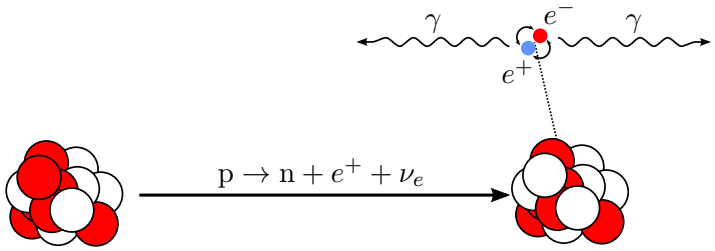


Figure 2.5: Illustrated decay of a positron emitting isotope with subsequent positron annihilation.

emission of positrons, which in turn annihilate with electrons inside the body. The two resulting 511 keV photons are emitted in opposing directions due to momentum conservation. In a conventional PET system, the annihilation photons are registered in a symmetric detector ring surrounding the patient, as it is shown in Figure 2.4. Since the photons are emitted simultaneously and in opposite directions, the origin of the annihilation, and thus also the isotope which emitted the positron, has to be located along a so called Line-of-Response (LoR) connecting the two detector modules. The distribution of the tracer compound can be measured by recording the intersections of many LoRs. Areas with a high tracer uptake will have many intersecting lines, indicating an increased metabolism in this region.

Although the basic reconstruction principle of positron emission tomography is straightforward, there are many challenges that limit the spacial resolution and image quality of the system. In order to understand these limitations, the physics of the positron decay and the interaction of photons with matter have to be explained in more detail. A more comprehensive overview of the technologies and image reconstruction methods used in PET system ,which is beyond the scope of this thesis, can be found in [12].

2.2.1 Position Reconstruction of Positron Decays

Positron emission occurs during the decay of a proton-rich radioactive isotope. During this process, a proton in the nucleus is converted into a neutron, a positron and a neutrino, which is shown in Figure 2.5.

The excess energy of the decay is transferred as kinetic energy to the individual decay products. As a consequence, the positron is not at rest after the emission and loses its kinetic energy in scattering processes while moving through the surrounding matter, until it finally annihilates with an electron. The scattering processes cause the positron to take a random path to its final annihilation point. Since a PET detector measures the position of the annihilation, the mean distance the positron travels before finally annihilating fundamentally limits the precision of the image reconstruction. Isotopes with a smaller excess energy provide a better image reconstruction, because the annihilation points are closer to the emitting nuclei. Table 2.1 lists isotopes used in positron emission tomography and their properties. The positron emitted in the decay of the commonly used tracer FDG has a relatively low mean range in water and thus provides a sharper image of the tracer distribution in the human body.

As mentioned before, the positron annihilates with the electron predominantly into two

photons [13]. Momentum conservation forces these photons to be emitted in opposite directions and this collinearity is exploited in PET systems for the image reconstruction. Two photons are considered to originate from the same annihilation process if they arrive simultaneously within a coincidence time window of a few nanoseconds. For each coincidence event the corresponding Line-of-Response is recorded. Because of the collinearity, the decay must have occurred on a point along this line. The precision of this information depends on the size of the detector modules. A higher detector granularity with smaller scintillator modules allows to reconstruct a more precise LoR, thereby improving the spacial resolution of the PET system.

The remaining momentum of the positron when annihilating disturbs the collinearity and the generated photons are not emitted at precisely 180°. Although the deviation from a strict back to back emission is only $\sim 0.25°$, the error on the position reconstruction can be significant, depending on the distance between the coincidence detector modules.

The combined impact of the described factors poses a lower limit on the image resolution, which can be described by an empirical formula as proposed by Moses and Derenzo [14]:

$$\sigma^2 \propto r_{e^+}^2 + \frac{d}{2}^2 + (0.0022D)^2. \tag{2.2}$$

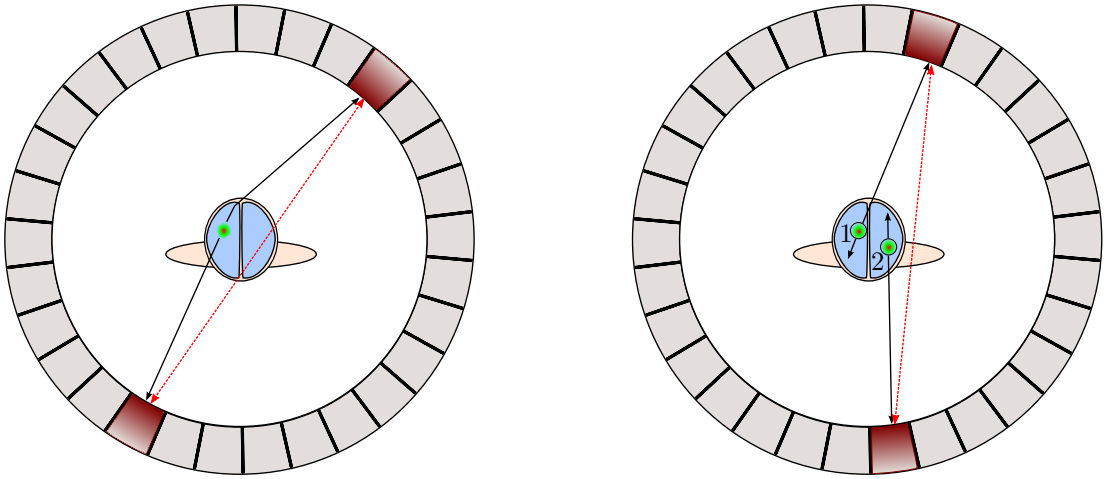
r_{e^+} describes the range of the positron in the surrounding tissue and d is the size of the detector modules. The effect of the non-collinearity of the annihilation photons is included by the distance of the detector modules D with $(0.0022D) = \frac{1}{2}tan(0.25°)D$.

Before being detected in the detector modules, the photons have to pass the surrounding tissue of the patient. Since the energy of the 511 keV photons is too small for pair-production, there are only two processes by which they interact with matter. They can be absorbed by the photo-electric effect or undergo Compton scattering. Both cases can lead to misidentified coincidences that will decrease the image contrast.

Compton scattering with electrons of the surrounding matter can divert one or both annihilation photons from a direct path to the detector modules, as it is shown in Figure 2.6a. The resulting Line-of-Response of such events is displaced and contributes to the signal background. Since the mean free path of a 511 keV photon in body tissue is about 7 cm, the contribution of scattered coincidences to the image reconstruction is significant. To improve the image contrast, these events have to be identified and if possible excluded from the reconstruction data.

Isotope	$\tau_{\frac{1}{2}}$ **[min]**	**Mean e^+ energy [keV]**	**Range in Water [mm]**	
			Maximum	Mean
^{11}C	20.4	326	4.1	1.1
^{13}N	9.96	432	5.1	1.5
^{15}O	2.03	696	7.3	2.5
^{16}F	109.8	202	2.4	0.6

Table 2.1: Properties of positron emitting isotopes used in PET applications [12].



(a) Scattered coincidences. **(b)** Random coincidences.

Figure 2.6: Reconstruction of fake coincidence events.

During the scattering process, the photon transfers energy to the electron and the remaining energy of the scattered photon can be calculated by [15]:

$$E_{\gamma'}(\phi) = \frac{E_\gamma}{1 + \frac{E_\gamma}{m_e c^2}(1 - cos(\phi))}\,. \tag{2.3}$$

The equation shows, that the energy depends on the scattering angle ϕ. The maximum energy is E_γ for an angle of 0° which corresponds to no scattering, whereas the minimal energy is reached at an angle of 180°. An ideal detector with perfect energy resolution would allow to discard all scattered coincidence events by only selecting coincidence events where both detected photons have an energy of 511 keV. Since this ideal case can never be achieved in a real detector system, a minimum scattering angle exists that the system can resolve from unscattered photons. A better energy resolution allows to define a more precise cut on the photon energy and thus reject smaller scattering angles. Assuming an energy resolution of 10 %, the smallest angles the detector can distinguish are approximately 30°. A detector with a resolution of 20 % can only reject angles larger than 40°. This simple calculation shows that, even with a good resolution, many scattered events are still undistinguishable from true coincidence events and additional techniques have to be used to reduce their contribution to the image background [16].

Random or accidental coincidences can occur if more than one positron annihilates within the coincidence time window. If one or two photons from different annihilations are absorbed in the body tissue or are not detected in the PET ring, as it is shown in Figure 2.6b, the resulting LoR is not related to either annihilation point and contributes to the signal noise. The rate of random coincidences is correlated to the length of the coincidence time window. A longer window will build more coincidences from separate annihilation events than a short window. A

high time resolution of the detector allows to constrain this coincidence window to shorter time intervals. However, it has to be large enough to cover the full detector Field-Of-View (FOV), which sets a lower limit to the window length. For a full body PET system with a diameter of 1 m the minimal window that does not constrain the FOV is 1 m/c = 3.4 ns, where c is the speed of light. Due to this minimal coincidence time window, an improved time resolution of the detector will not yield a better rejection of random events beyond the minimal time window. Still, a sufficiently high resolution can be used for Time-of-Flight measurements of the photons to further improve the sensitivity of the detector.

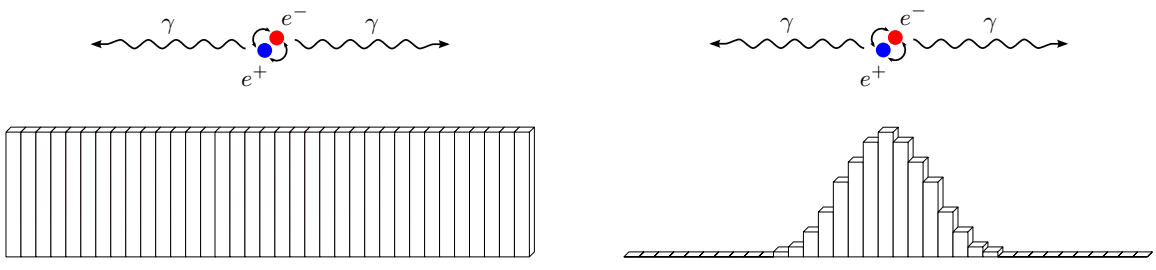
2.2.2 Time-of-Flight PET

The image reconstruction of a conventional PET system suffers from a large amount of statistical noise since the annihilation position of the positron along the reconstructed Line-of-Response is unknown. Due to this obscurity, every point along the line has to be considered as a potential origin of the annihilation and included with the same weight in the image reconstruction. By measuring the arrival time of the 511 keV photons with a high precision, the decay point along the LoR can be estimated, as it is shown in Figure 2.7b. A direct position reconstruction with a precision of ~ 3 mm would require a timing resolution of 10 ps which is impossible to achieve with our current technology in a large scale system. Despite the fact that the additional Time-of-Flight information does not improve the spatial resolution, the system can exclude most of the possible annihilation points along a Line-of-Response and improve the contrast as well as the reduce acquisition time of an image.

The principle of rejecting background events and ambiguous intersections of different Lines-of-Response by using the ToF information is depicted in Figure 2.8. The additional position information allows to recognize the marked intersections as artificial points and distinguish them from true tracer concentrations.

The impact of the timing resolution on the signal-to-noise ratio has been the focus of many research publications [17–19]. They show that the signal-to-noise ratio of the image increases with better timing and thereby spatial resolution of the positron decay [20]:

$$\mathrm{SNR}^2_{\mathrm{ToF}} = \mathrm{SNR}^2_{\text{non-ToF}} \frac{2S}{\Delta t \cdot c} \,. \tag{2.4}$$



(a) Conventional LoR. **(b)** LoR with Time-of-Flight.

Figure 2.7: Weighted Line-of-Response reconstruction using Time-of-Flight measurements.

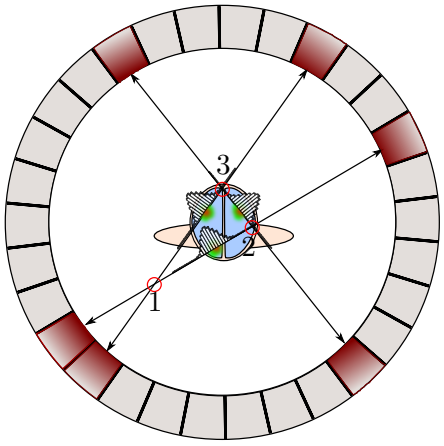


Figure 2.8: Exclusion of ambiguous intersection points with ToF weighted Line-of-Response.

The variable S denotes the effective diameter of a patient. For a Time-of-Flight resolution of 500 ps and an effective diameter of 40 cm the SNR already increases by a factor of 2.3 .

Although the asset of ToF measurements in positron emission tomography has already been known and investigated since the 1980s [21], the lack of suitable scintillator materials prevented the feasibility of ToF-PET systems. Sufficiently fast scintillators such as BaF_2 lack the required stopping power to detect the 511 keV. The loss in detector sensitivity because of this outweighs the gain from the additional Time-of-Flight information resulting in an overall lower signal-to-noise ratio. The ongoing research of fast inorganic scintillating crystals such as Lutetium Yttrium Ortho-Silicate (LYSO) and Lanthanum Bromide ($LaBr_3$) have rekindled the research of ToF-PET systems [22]. It has been shown that timing resolutions of down to 100 ps FWHM can be achieved with these novel scintillator materials in combination with Silicon Photomultiplier readout [23].

In addition to the high timing resolution, the features of SiPMs, in particular their small form factor and insensitivity to magnetic fields, have paved the way for the development of new detector concepts. These systems require a combined development effort for the whole detector chain consisting of scintillators, light sensors and readout electronics to fully exploit the possible advantages of the new technologies.

2.2.3 EndoTOFPET-US System Design

The EndoTOFPET-US project is developing a novel multi-modal endoscopic detector system combining anatomical ultrasound imaging with high resolution functional PET imaging. The motivation of the project is to provide a tool for the diagnosis and treatment of pancreatic and prostatic cancer. Such a PET device must provide the capability to recognize small tumors while rejecting a large amount of background radiation from the tracer uptake in the surrounding organs such as liver and bladder. In order to achieve this, the project aims to achieve a spatial resolution of less than 1 mm and a Time-of-Flight resolution of 200 ps FWHM to provide the required background rejection.

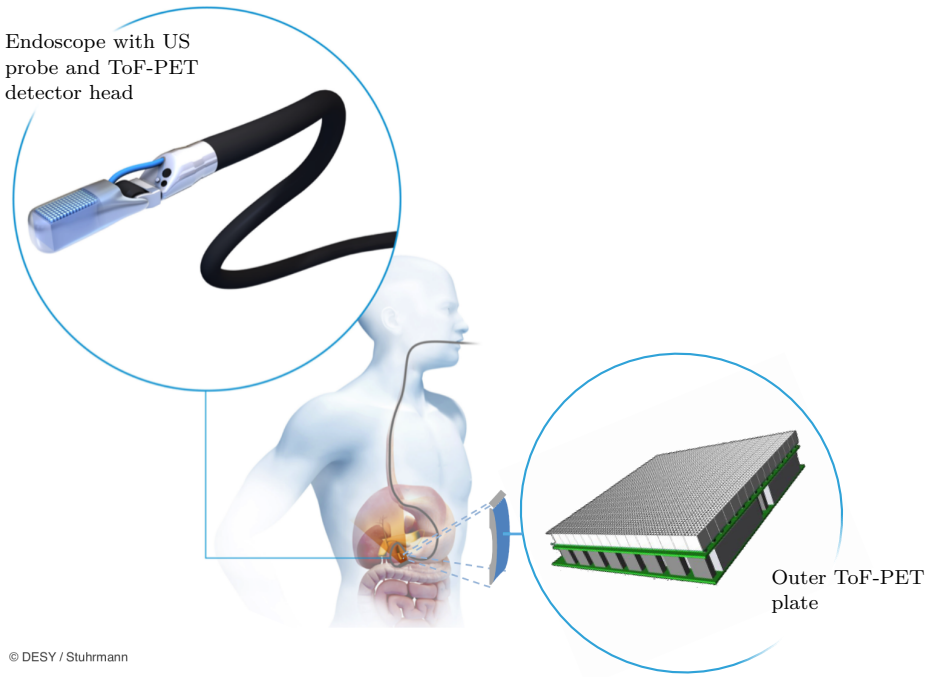
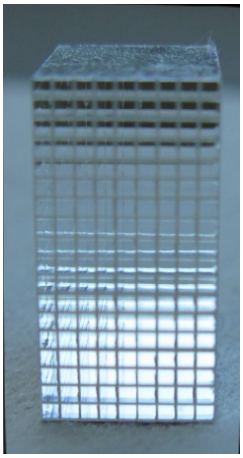


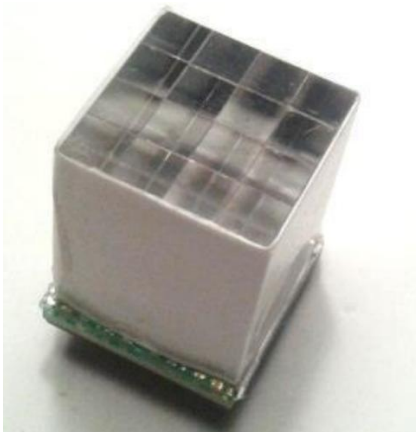
Figure 2.9: Artist sketch of the EndoTOFPET-US design. Original image source: DESY/Stuhrmann.

Figure 2.9 shows an artists sketch of the envisioned detector system. The anatomical imaging of the tissue will be handled by a commercially available endoscopic ultrasound probe. Instead of a conventional PET detector ring, the project pursues the more ambitious approach of an endoscopic PET detector head that will be attached to the ultrasound probe. The coincidence photons from positron annihilations will be reconstructed between this PET head and an outer detector plate. The asymmetric endoscopic design allows to position the detector head close to the region of interest, in this case the pancreas or the prostate. From Equation 2.2 it is evident that this allows to reduce the contribution of the detector distance D to the spatial resolution to achieve the design goal of sub-millimeter resolution.

The endoscopic design poses many technical challenges. The probe has to stay compact enough to be inserted into the patient, while providing a high granularity of scintillator crystals to determine the position of a detected 511 keV photon on the detector head. Since the endoscope is moving during the data acquisition, its position has to be measured by and accurate tracking method. This is complicated further by the fact that precise optical tracking methods can not be employed, since they would require a direct line-of-sight to the detector head inside the patient. Instead, electro-magnetic tracking methods have to be used to evaluate the position of the probe, which are limited in the achievable spacial resolution [24]. In addition, the tight space constraints require highly integrated readout electronics capable of providing the required Time-of-Flight resolution. The PET modules foreseen for the endoscopic probe are shown in Figure 2.10a and consist of 9×18 LYSO crystals. The crystals have a size of $0.71 \times 0.71 \times 15\,\mathrm{mm}^3$ and are coupled to custom digital



(a) Inner probe crystal matrix.



(b) Outer plate crystal matrix.

Figure 2.10: EndoTOFPET-US detector modules [5].

SiPM sensors developed at TU Delft [25]. These novel sensors integrate pixels of photo-diodes used for the photon detection on the same chip-die as the readout electronics. This allows to measure the arrival time of individual photons on the sensor. The timing information of these individual pixels can be combined to achieve an improved timing resolution compared to standard photo-sensors.

The mechanical design constraints of the outer plate are more relaxed, but the requirements to the readout electronics are as challenging as for the endoscopic head. The detector modules of the external plate consist of 16 $3.5 \times 3.5 \times 15\,\mathrm{mm}^3$ LYSO crystals coupled to 4×4 Silicon Photomultiplier arrays manufactured by Hamamatsu (S12643-050CN(X)). In total, 256 detector modules are integrated in an area of $23 \times 23\,\mathrm{cm}^2$ providing 4096 readout channels. The readout electronics for the detector modules has to provide the desired high timing resolution while maintaining a good energy resolution for the event reconstruction. This high level of system integration can only be achieved by custom designed mixed signal ASICs, which digitize the time and energy information on-chip and transfer them to the readout data acquisition (DAQ) system. The STiC ASIC presented in this thesis has been specifically developed to meet the requirements of the EndoTOFPET-US project and is currently being commissioned in the outer plate detector system, which will be presented in Chapter 7.

Chapter 3

Silicon Photomultipliers

The detection of small amounts of light down to single photons became possible with the invention of the photomultiplier tube (PMT) by L.A. Kubetsky in 1930, which has become an integral part of many detector systems. Although the design of the PMT has been continuously improved and adapted to various applications, their large and fragile structure, expensive manufacturing, and sensitivity to magnetic fields are inherent drawbacks that cannot be fully resolved. For the design of complex and highly granular detector systems with thousands of channels, an alternative photo-sensor device had to be found.

Solid-state sensors have matured in recent years to provide a performance comparable to conventional photomultiplier tubes. Because of their small and robust design, low-cost, and insensitivity to magnetic fields, they have become a popular choice to replace PMTs in many applications. In this chapter, the design of solid-state photo-sensors is described with a focus on Silicon Photomultipliers. A model to describe the electrical response of these sensors to incoming light pulses and the requirements for high-precision timing measurements are discussed.

3.1 Solid-State Photo-Sensors

Solid-state sensors exploit the small energy-gap between the valence and conduction band in semiconductor materials such as Silicon or Germanium to detect photons. As for insulators, the Fermi-energy in these materials lies in between the two energy bands, resulting in a filled valence band and an empty conduction band. In contrast to insulating materials however, the gap is with several eV sufficiently small to be bridged by the thermal excitation of electrons, producing a small concentration of electrons and holes in the conduction and valence band. These charge carriers contribute to the electrical conductivity of the material. The required energy to excite electrons to the conduction band can also be provided by the absorption of light or radiation with sufficient energy, thereby increasing the conductivity of the material. This absorption mechanism is used by solid-state photo-sensors for the detection of light signals.

The electrical properties of a semiconductor can be influenced by implanting atoms of a chemical group above or below the intrinsic material into to crystal lattice. The impurities in the lattice create additional energy states inside the energy gap of the semiconductor. This process called doping is the basis of fabricating electronic devices within semiconducting materials. Dopants adding quasi-free electrons and thereby increasing the concentration of

electrons in the conduction band are called donors. Conversely, acceptors are dopants that can bind an additional electron, increasing the concentration of positive charge carriers, called holes. The regions doped with donor or acceptor atoms are called n- or p-doped, respectively. Semiconductors are the focus of many literature sources, describing the theoretical background from solid state physics, the production process, and the design of semiconductor electrical components [26, 27]. In this chapter only PIN-diodes and other sensor devices, which are used for the detection of light, are investigated.

3.1.1 PIN Diodes

The design of PIN-diodes is based on the pn-junction that is formed when n-doped and p-doped regions of a semiconductor are connected. In addition to the pn-junction, PIN-diodes contain an additional intrinsic or lightly doped region, as it is shown in Figure 3.1. To understand the functionality of this device, one can first neglect this layer of intrinsic material and investigate only the pn-junction.

The different concentrations of free charge carriers in the individual doping regions create a diffusion current of holes and electrons between the anode (p-doped region) and the cathode (n-doped region). Since the donor and acceptor atoms are bound in the crystal lattice, they cannot follow the free charge carriers, which leads to an accumulation of positive charge at the interface to the n-doped region, and a negative charge at the p-doped region. The result is an electrical field which opposes the diffusion current. Eventually, an equilibrium is established between the diffusion current and the potential of the electrical field. Between anode and cathode, a depletion or space charge region has formed which is devoid of free charge carriers.

The depletion zone can be influenced by applying an external bias voltage V_{bias} to the terminals of the device. If the voltage at the cathode is lower with respect to the anode, the electrons in the n-doped region are pushed into the depletion zone. The same occurs with holes in the p-doped material. If the voltage is large enough to overcome the built-in electric potential of the junction, the diode becomes conductive and a current flows through it. For

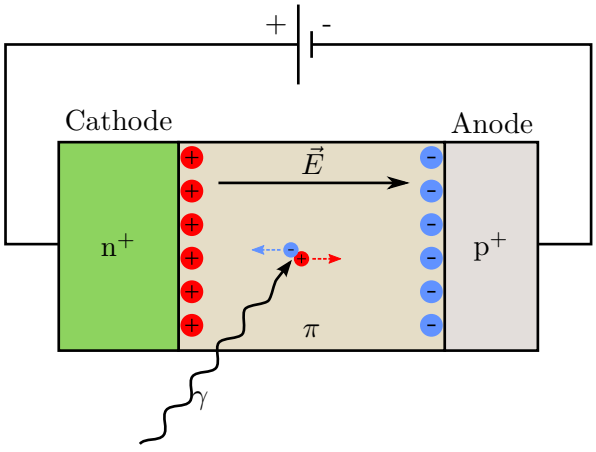


Figure 3.1: Light detection with a pin-diode in reversed bias mode.

radiation and light detection, a reverse bias voltage is applied, as it is shown in Figure 3.1. The electrical field caused by the external bias has the same polarity as the field opposing the diffusion current, effectively increasing the size of the space charge region. In this mode, only a negligible reverse saturation current I_S is flowing between the terminals. Electron hole pairs created in the depletion zone by thermal excitation or the absorption of photons contribute to the current flowing through the diode. In the case of photon absorption, the additional generated photocurrent is proportional to the incident light power,

$$I_{ph} \propto P_\lambda \,. \tag{3.1}$$

Since it is not possible to measure currents in the order of a few electrons without an intrinsic amplification mechanism, charge-sensitive pre-amplifiers have to be used to sense the additional photocurrent I_{ph}. The noise level after amplification limits the minimal measurable light power of these photo-diodes to a few hundred photons.

The additional undoped intrinsic region of PIN-diodes is introduced to increase the size of the depletion region between the n- and p-terminal, and thus the detection volume for photons. This improves the spectral response of the diode, since photons with lower energies have a longer absorption length, and the probability to absorb them in the deeper depletion zone rises.

3.1.2 Avalanche Photodiodes

Avalanche photodiodes (APD) improve the concept of PIN-diodes by introducing an internal amplification mechanism. The doping profile of an APD is shown together with the resulting electrical field strength in Figure 3.2. In addition to the intrinsic semiconductor material acting as an absorption region, a p-doped layer is added at the interface to the cathode. As a result, a strong electric field is generated by the modified space charge distribution in this area. As in the PIN-diode, electron hole pairs generated in the absorption region are separated by the electric field. While the holes are extracted at the anode, the electrons can gain sufficient

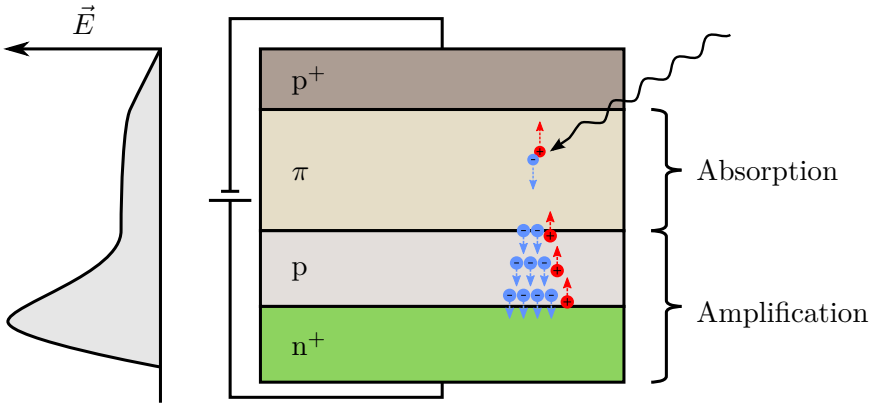


Figure 3.2: Doping profile and electric field in an APD.

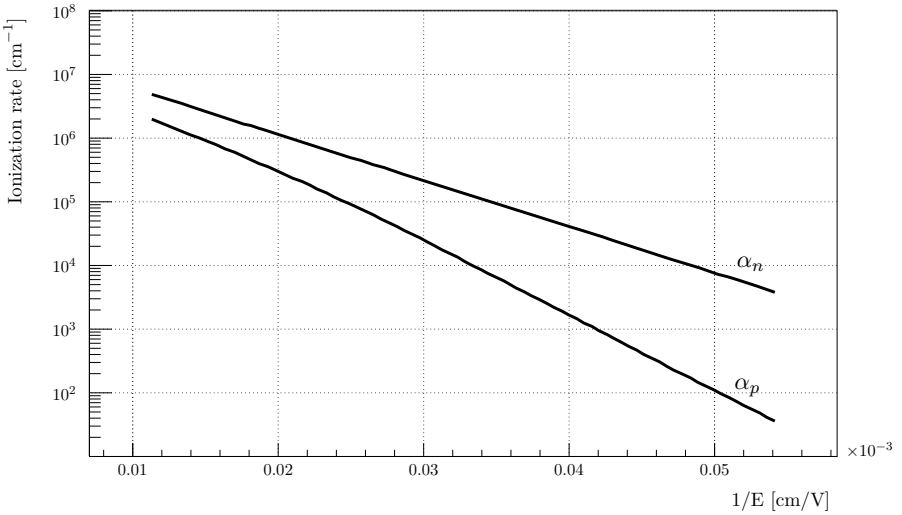


Figure 3.3: Ionization rates for electrons and holes in silicon. Data taken from [28].

energy to create further electron hole pairs by impact ionization.

The probability for a charge carrier to ionize a lattice atom strongly depends on the strength of the electric field and is different for electron and holes. This probability is expressed by the ionization rate α_n and α_p for electrons and holes, respectively. Figure 3.3 shows measurements of the ionization rates in silicon [28, 29]. The rates for both positive and negative charge carriers increase exponentially with the electric field. Because of the lower mobility of holes, the ionization rate α_p is generally lower than α_n. For strong electric fields however, α_n and α_p converge, which is evident in the measurement data.

If the bias voltage is sufficiently high, the probability to ionize atoms in the multiplication region becomes large enough for electrons to create an avalanche of secondary electron hole pairs. The resulting diode current I_{APD} is a multiple of the initially generated photocurrent:

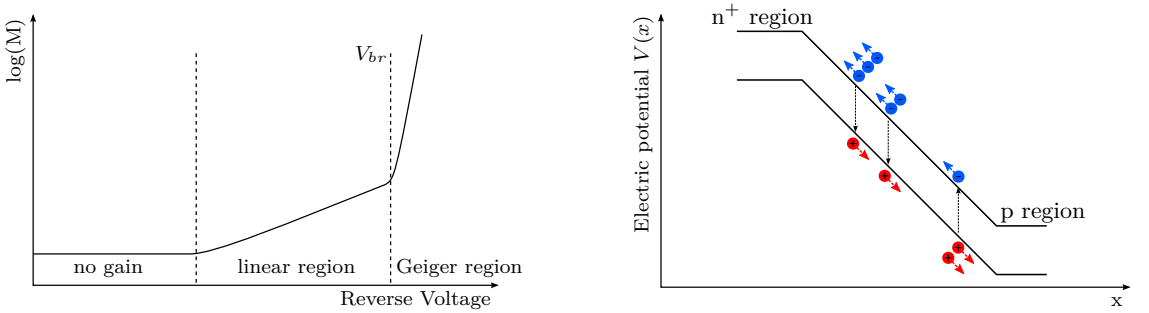
$$I_{APD} = M \cdot I_{ph}\,, \tag{3.2}$$

with the multiplication factor, or gain, M.

As the ionization rate depends on the strength of the electrical field, so does the gain of an APD. The field strength is in turn determined by the applied bias voltage. A key characteristic of APDs is therefore the correlation between the gain and the bias voltage, which is shown for a hypothetical sensor in Figure 3.4a. The dependence of the gain can be subdivided in three different regions. At low voltages, the electrical field is not strong enough to accelerate electrons to the minimal energy required for impact ionization. As a consequence, no signal amplification occurs and

$$I_{APD} = I_{ph}\,. \tag{3.3}$$

By increasing the bias voltage and therefore creating a stronger electrical field, the gain is



(a) Individual gain regions of an APD sensor.

(b) Self-sustained avalanche in the Geiger-mode.

Figure 3.4: Different operation modes of an avalanche photodiode.

sufficient to create secondary electron hole pairs in the multiplication region. The logarithm of the gain M in this region is proportional to the applied reverse voltage. Due to their lower ionization rate, the generated holes do not gain sufficient energy for ionization processes in this bias region, and the avalanche eventually stops. The voltage range in which the APD is in the linear mode depends on the doping profile and can start at voltages below 100 V. The gain changes in this region from values in the order of $M \approx 5$ to $M \approx 30$ [30]. The amplification of the original photocurrent allows to detect light pulses with less than 100 photons. However, for the detection of single photons the gain is still insufficient in this operation mode.

If the bias voltage is increased further, the ionization rate of the secondary holes becomes comparable to that of electrons and they too generate further electron hole pairs inside the amplification zone. Since the holes are moving in opposite direction to the electrons, the avalanche becomes self-sustaining and a constant current is flowing through the APD. This situation is depicted in Figure 3.4b. The voltage at which the self-sustaining process occurs is called the break-down voltage V_{br} with typical values of 100 V to 150 V, again depending on the doping profile of the diode. In this so-called Geiger mode, the current flowing during the avalanche process is only determined by the difference between V_{bias} and V_{br} and no longer related to the incident light power. The over voltage V_{ov}, defined as

$$V_{ov} = V_{bias} - V_{br}\,, \tag{3.4}$$

is therefore a key parameter for the operation of APDs in the Geiger mode.

Although the Geiger mode does not allow to measure the initial photocurrent generated by the incident light pulse, it does provide the possibility to detect the absorption of even a single photon. Special avalanche photodiodes operated in this mode are also called single-photon avalanche diode (SPAD) or Geiger-mode APD (G-APD).

Once an avalanche process has been triggered, the diode current does not change with further photon absorptions. To stop the avalanche and detect another light pulse, the bias voltage must be reduced below the breakdown voltage V_{br}. This process is called quenching and can be performed with an active circuit or a passive resistor. For active quenching, an

electric circuit monitors the current I_{APD} of the diode to decide if an avalanche breakdown has occurred. The circuit then immediately reduces the bias voltage below V_{br} and applies the original over voltage a short time later. The active quenching can happen very fast, allowing a fast recovery time of the sensor, but requires additional logic and biasing circuits.

The simpler quenching technique is an additional passive resistor in the order of 100 kΩ, connected in series to the current output of the diode, as it can be seen in Figure 3.5a. The current produced by the avalanche will cause a voltage drop over this quench resistor and the voltage at the diode decreases automatically to V_{br}. After the avalanche has been quenched, the voltage of the diode slowly recovers to the applied bias voltage. The resulting output signal of a SPAD with passive quenching is a current pulse of defined charge Q with a fast rise time and a slow recovery time.

With the generated signal charge Q contained in one detection pulse, the gain of an APD operated in the Geiger mode can be calculated by

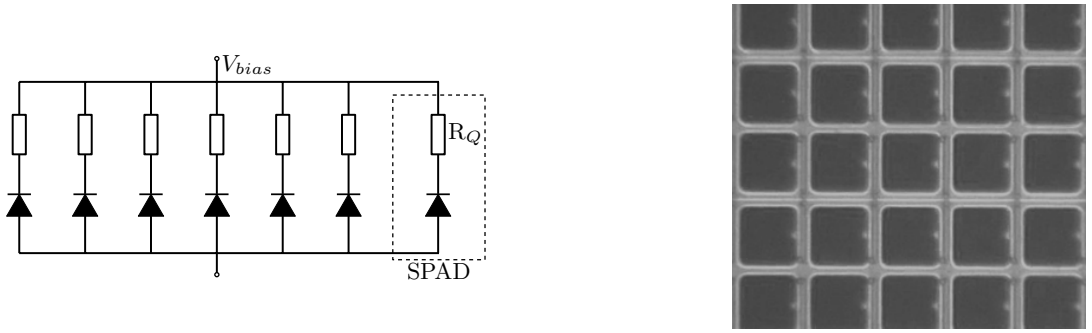
$$M = \frac{Q}{e}\,, \tag{3.5}$$

where e denotes the single electron charge. Typical values for the gain are in the range of 10^5 to 10^6, which is comparable to the gain of photomultiplier tubes. Unlike PMTs however, the amplification is not disturbed by magnetic fields, since the strong electric field is limited to the interface between the n- and p-doped material and extends over a range of approximately 1μm. The path of the charge carriers in an avalanche experiences no significant deviation by even strong magnetic fields and the avalanching process stays unaffected.

3.1.3 Silicon Photomultiplier

APDs operated in the Geiger mode provide the possibility to detect single photons. However, it is not possible to measure how many photons have triggered the avalanche process, since the output signal does not depend on the photocurrent. Silicon Photomultiplier solve this limitation by using an array of parallel connected SPAD microcells simultaneously, as it is shown schematically in Figure 3.5a. The individual cells consist of a SPAD and a passive quenching resistor, bi-dimensionally arranged on a common die surface. A microscopic picture of a Silicon Photomultiplier can be seen in Figure 3.5b. The size of the individual cells typically measures between $10 \times 10\,\mu\text{m}^2$ and $100 \times 100\,\mu\text{m}^2$. Sensors with a surface area in the range of $1 \times 1\text{mm}^2$ to $3 \times 3\,\text{mm}^2$ provide sufficient area for several thousand pixels. The diodes share a common die-substrate as anode and the cathodes are connected over the quench resistor R_q to a common bias line. The probability that all photons of an unfocused light pulse are absorbed in the same pixel of the sensor is very small. Instead, several microcells will be triggered, and due to the parallel connection, the generated output signal is the sum of all fired pixel signals.

For a thorough understanding of the SiPM response, it is therefore necessary to investigate the contributing physical processes to the signal formation in the individual pixels. An instrumental method to achieve this goal is the representation of a Silicon Photomultiplier by



(a) Schematic diagram of the pixel connection.

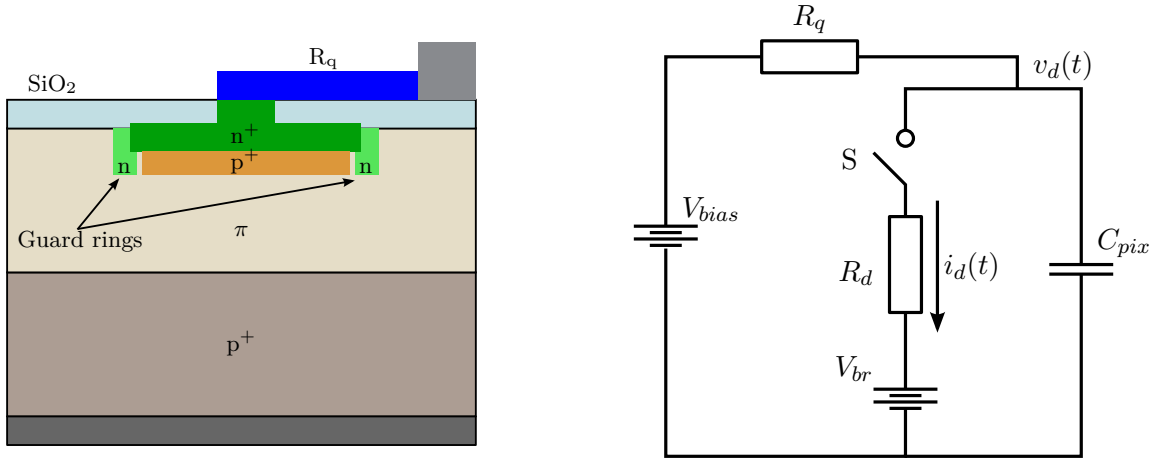
(b) Microscopic picture of a SiPM with $50 \times 50\mu\text{m}^2$ pixels.

Figure 3.5: Parallel connection of avalanche photodiodes operated in Geiger mode.

an equivalent electrical circuit, which models the processes during an avalanche breakdown and allows an analytical description of the sensor. A detailed analysis of the sensor would require a sophisticated model, which also includes second order effects from parasitic capacitances and the connected biasing and readout electronics. These effects become important for the high precision timing measurements, and will be the topic of Section 3.2. To investigate the basic characteristics of a SiPM, higher order effects can be neglected and a simplified model is used.

As the development of SiPMs has brought forth a multitude of different implementations, the electrical models have to be tailored to represent the individual designs. Figure 3.6a shows the doping profile of a SiPM microcell with the often used reach-through structure and the corresponding simplified equivalent circuit, based on the model introduced by Corsi et al. [31]. The doping profile is similar to that of an avalanche photodiode, consisting of an intrinsic area for the absorption of photons and a multiplication region, where the high electric field is generated. Guard rings are introduced between the individual pixels to suppress undesired high electrical fields in the pixel border regions. Since an active quenching scheme would require to much space on the die surface, a passive resistor R_q is used to quench the avalanche after a pixel has fired. This resistor can be fabricated in a very small area of the die, allowing to maximize the sensitive surface of the device.

The equivalent circuit shown in Figure 3.6b models an avalanche breakdown as the discharge of a capacitor C_{pix}. The value of C_{pix} is determined by the junction capacitance of the diode. Before an avalanche is triggered, the switch S is open and the capacitance is charged to the bias voltage V_{bias}. An incoming photon triggering an avalanche closes the switch and C_{pix} is discharged over the resistance R_d, which describes the series resistance of intrinsic and depletion region in the diode. During the discharge of the capacitor, the voltage in point v_d will decrease until it reaches a minimal value. The asymptotic minimum of this voltage can be calculated by applying Kirchhoff's law to the circuit when S is closed and C_{pix} has been discharged. In this case, the current i_d flowing through R_q and R_d is solely determined by the



(a) Doping profile of a pixel with reach-through structure [32].

(b) Equivalent circuit of a SiPM pixel. [33]

Figure 3.6: Simplified electrical model of a SiPM.

two resistors and the voltage difference between V_{bias} and V_{br}:

$$\lim_{t\to\infty} i_d(t) = \frac{V_{bias} - V_{br}}{R_q + R_d} \tag{3.6}$$

The voltage in the point V_d can then be calculated by:

$$\begin{aligned} \lim_{t\to\infty} v_d(t) &= V_{bias} - \frac{R_q(V_{bias} - V_{br})}{R_q + R_d} \\ &= V_{bias} - \frac{V_{ov}}{1 + \frac{R_d}{R_q}} \end{aligned} \tag{3.7}$$

In the case $R_d \ll R_q$, which holds true for most Silicon Photomultipliers, Equation 3.7 shows that V_d will approximate the breakdown voltage V_{br}. Using this approximation, the transient behaviour of the diode voltage can be expressed as the exponential discharge of the capacitor C_{pix} over R_d from the initial voltage V_{bias} to V_{br}:

$$v_d(t) = V_{br} + V_{ov} \cdot \exp(-\frac{t}{R_d C_{pix}}) \,. \tag{3.8}$$

The same exponential decay is also reflected in the diode current $i_d(t)$, which changes from its initial value V_{ov}/R_d to the final value given by Equation 3.6:

$$i_d(t) = \frac{V_{ov}}{R_d + R_q} + (\frac{V_{ov}}{R_d} - \frac{V_{ov}}{R_d + R_q}) \cdot \exp(-\frac{t}{R_d C_{pix}}) \,. \tag{3.9}$$

The avalanche process requires a minimal threshold current $i_d(t) > I_{th}$ of a few μA to sustain itself. Once $i_d(t)$ drops below this value, the avalanche is quenched. This cutoff is

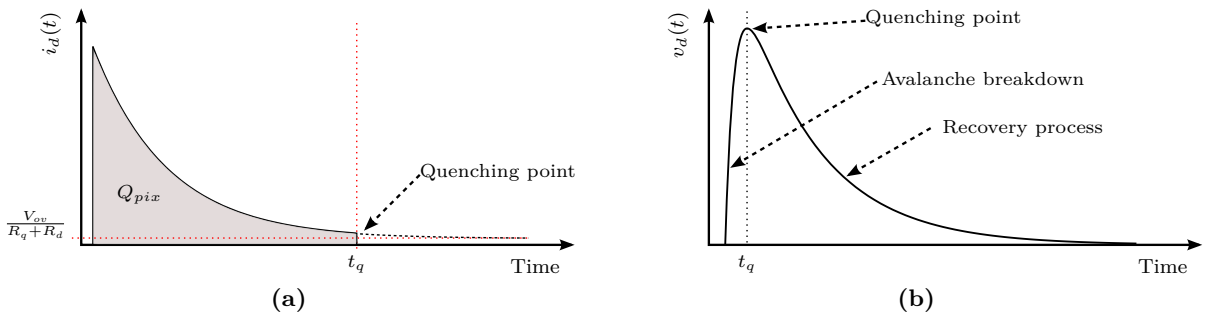


Figure 3.7: Pulse shapes of $i_d(t)$ and $v_d(t)$ based on the evaluation of the simplified electrical circuit.

modeled by opening the switch S again at the quenching time t_q, when i_d passes the threshold. As soon as the switch S is opened, no current can flow through R_d, causing i_d to drop instantly to 0 A at time t_q. Consequently, the charge generated by the avalanche breakdown can be calculated by integrating $i_d(t)$ from time $t = 0$ at which the switch is closed until the quenching time t_q:

$$Q_{pix} = \int_0^{t_q} i_d(\tau)d\tau = \left[\frac{V_{ov}}{R_d + R_q}\tau - V_{ov}\frac{R_q}{R_d + R_q}C_{pix} \cdot \exp(-\frac{\tau}{R_d C_{pix}})\right]_0^{t_q} . \tag{3.10}$$

The parameter values for C_{pix}, R_d, R_q, and t_q can be extracted from measurements of the SiPM and are summarized in Table 3.1. Because of the fast quenching time t_q, the first term in Equation 3.10 can be neglected. Using $R_q \gg R_d$ and $\exp(-t_q/(R_d C_{pix})) \approx 0$, the generated charge can be approximated as

$$Q_{pix} \approx V_{ov} \cdot C_{pix} . \tag{3.11}$$

Together with Equation 3.5, the gain of a pixel can then be expressed as a function of the overvoltage:

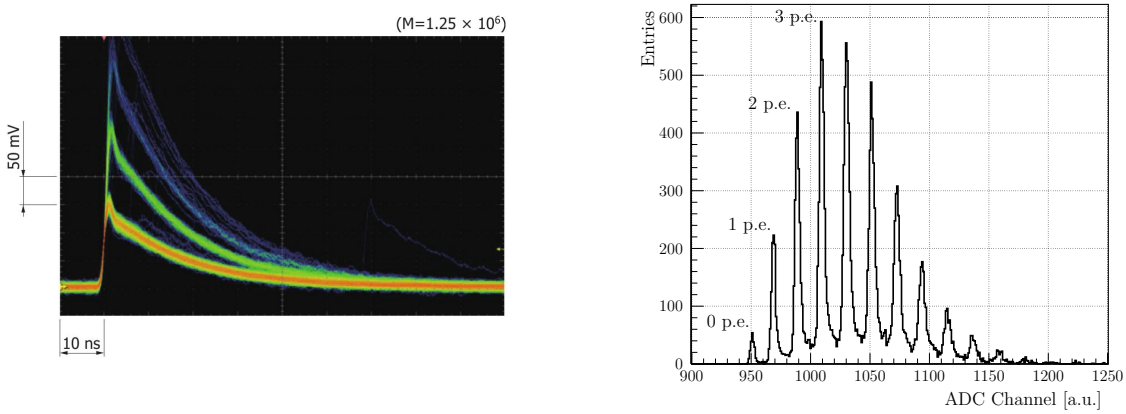
$$M = \frac{V_{ov} \cdot C_{pix}}{e} . \tag{3.12}$$

Due to the statistical nature of the ionization process, the threshold current I_{th}, and thus the quenching time t_q, are subject to fluctuations. As is evident from Equation 3.10, these uncertainties in t_q affect the generated signal charge Q_{pix} for each event, causing in turn a small variation of the pixel gain M for each triggered avalanche.

After the quenching point, the capacitance C_{pix} is again charged to the bias voltage over the quenching resistor. This charging process has with $R_q C_{pix}$ a much larger time constant

C_{pix}	R_q	R_d	t_q
25 fF	250 kΩ	1 kΩ	150 ps

Table 3.1: Typical parameters extracted from SiPM measurements using an equivalent electric circuit. Values taken from [33]



(a) SiPM current pulses as superposition of individual SPAD pulses [34].

(b) Single pixel spectrum measured with the KLauS ASIC [35].

Figure 3.8: Signal response of a SiPM to low intensity light pulses.

than the discharge of the pixel. The resulting pulse shapes of $v_d(t)$ and $i_d(t)$, based on the analysis of the equivalent circuit are drawn in Figure 3.7. If several pixels are simultaneously triggered, the sensor response is the superposition of these individual pulse shapes. Figure 3.8 shows this case of multiple triggered pixels as a response to a low intensity light signal. The superposition of the individual SPAD pulses is clearly visible in this measurement. Under the assumption that the gain of all SPAD cells is uniform, an individual pulse generated by N_f triggered pixels contains a charge of

$$Q_{sipm}(N_f) = \sum_{\mathrm{n}=0}^{N_f} Q_{pix} = N_f \cdot V_{ov} \cdot C_{pix}\,. \tag{3.13}$$

Measuring Q_{sipm} for individual output pulses yields a single photon spectrum, in which the number of fired pixels contributing to the current pulse can be distinguished as individual peaks. It is evident from Equation 3.13, that the gain of the sensor is equal to the gain of a single pixel and can be easily extracted from the single photon spectrum by measuring the charge difference between the individual peaks. As with SPADs, the gain is in the order of $\sim 10^6$ and comparable to photomultiplier tubes. Because of variations in the manufacturing process and the already mentioned uncertainty in the quenching time, the gain is not fully uniform, a fact that is reflected in the width of the individual peaks in the charge spectrum. These and other error sources contributing to the width of the peaks can be extracted from measurements using sensitive charge readout circuits, such as the STiC sibling KLauS (Kanäle zur Ladungsauslese von SiPM)[36].

Because of their structure, Silicon Photomultiplier inherit all advantages of APDs operated in the Geiger mode, enhancing it with the capability to detect several thousand photons simultaneously. The growing popularity of Silicon Photomultiplier in the detector community

has led to a significant number of characterization studies which investigate and quantify the performance of these sensors, and provide a basis for the comparison of different SiPM designs [37–39]. Although the solid-state technology provides many improvements compared to conventional PMTs, such as the small form factor and insensitivity to magnetic fields, there are also several drawbacks that have to be taken into account. The most important characteristics of a SiPM will be explained in the following paragraphs.

Temperature Dependence

The temperature of a Silicon Photomultiplier has a strong influence on many parameters of the pn-junction in the SPAD cells, among others the width of the depletion zone, the recovery time, the resistivity of the semiconductor material, and first and foremost the breakdown voltage, which typically changes linearly by roughly $50\,\mathrm{mV}/K$ [40]. Therefore, the stable operation of a detector system requires the stabilization of the sensor temperature at the level of 1 K. If such a control is not feasible, the temperature has to be monitored and the bias voltage V_{bias} adjusted such that

$$V_{ov} = V_{bias} - V_{br}(T)\,, \tag{3.14}$$

ensuring that the over voltage and thereby the sensor gain stays constant.

Photon Detection Efficiency

The photon detection efficiency (PDE) describes the probability that an incident photon of a given wavelength will be absorbed and trigger an avalanche process generating a detectable current pulse at the output terminal of the sensor. The PDE can be expressed as

$$\mathrm{PDE} = \epsilon_{geo} \cdot QE \cdot \epsilon_{trigger} \cdot (1 - R_S)\,. \tag{3.15}$$

QE is the quantum efficiency and describes the probability that an electron hole pair is generated by the photon. Since the quantum efficiency is dependent on the photon energy, it also determines the spectral response of the Silicon Photomultiplier. The reflectivity of the sensor surface is given by R_S and is taken into account by the factor $1 - R_S$. $\epsilon_{trigger}$ is the probability that a generated electron-hole pair will actually trigger an avalanche breakdown in the pixel. The remaining parameter ϵ_{geo} describes the geometrical fill factor, which is determined by the ratio between the area covered by sensitive pixels and the total surface area of the sensor. Due to the minimal space required between pixels, the area of the quenching resistors, and the metal interconnections, the fill factor has an upper limit and increases with larger pixel sizes. Because of all the factors contributing to the PDE, the detection efficiency differs significantly between individual SiPM models. Typical values are in the range of 10 % to 40 % [37].

Gain

The high gain of 10^6 allows SiPMs to detect single photon signals. As already discussed, it is determined by the amplification factor of the individual SPAD cells and can be calculated by Equation 3.12. The capacitance C_{pix} is mainly defined by the size of the pixel, causing the gain to increase with larger pixel dimensions. The insensitivity of the amplification factor to magnetic fields is retained from the Geiger-mode APD design, which allows SiPMs to operate inside detector systems, rendering the necessity of light guides almost obsolete.

Dark Count Rate

Apart from photon absorption, electrons can reach the conduction band by thermal excitation and the quantum mechanical tunneling effect between the n- and p-doped layers. The resulting electron hole pairs can trigger an avalanche breakdown which is indistinguishable from the signal generated by photon absorption. Such events are called dark noise events and the dark count rate (DCR) is a key characteristic of Silicon Photomultiplier.

The probability for thermal excitation rises exponentially with the temperature of the sensor [38]. Cooling the sensor to lower temperatures can therefore significantly decrease the DCR. The thermal excitation of electrons is additionally increased by impurities in the crystal lattice, which add additional energy states in the band gap. Purer silicon as base material for the manufacturing process consequently reduces the dark noise of the sensor. Current SiPM models from Hamamatsu achieve a DCR of less than $100\,\mathrm{kHz/mm^2}$ at a temperature of 25°C [34].

The tunneling of electrons to the conduction band is primarily determined by the strength of the electrical field, and therefore by the applied over-voltage. At high bias voltages, it becomes the predominant process generating dark noise. In contrast to thermal excitation, it is independent of the temperature and cannot be reduced by cooling of the device.

Cross-Talk

Cross-talk can occur if photons generated during an avalanche breakdown are detected in a neighbouring pixel. The emission and absorption of the photons happens on a short time scale of less than 1 ps and hence it is impossible to discern cross-talk events from the absorption of two separate photons of a light pulse. The generation of photons in the pn-junctions has been investigated by Akil et al. [41], showing that the three processes contributing to the photon-emission during an avalanche breakdown are direct and indirect interband recombinations, and radiation of Bremsstrahlung. A higher over-voltage, and therefore a higher sensor gain, produces more charge carriers contributing to the avalanche. This results, in turn, in an increased number of emitted photons from the pixel, and the cross-talk probability increases accordingly. Larger pixel sizes increase the chance that an emitted photon is again absorbed within the same pixel, reducing the cross-talk effect. By adding deep trenches between the pixels, the emission of photons to neighbouring pixels can be further inhibited. However, the

additional space required for trenches reduces the fill factor of the sensor, and by this the photon detection efficiency. Detailed measurements show a cross-talk probability of up to 50 %, with a strong dependence on the overvoltage [37].

Afterpulses

Afterpulsing describes the generation of a secondary avalanche process after the bias voltage of a pixel has sufficiently recovered for another breakdown. Two processes are currently considered to be the cause of afterpulsing. First, the emitted photons during the initial avalanche process can be absorbed in the intrinsic material of the Geiger-mode APD and generate an electron hole pair in this region. If the diode voltage is above the breakdown voltage when the electron arrives after the drift time in the multiplication region, a secondary avalanche process is triggered. The second method is the temporary trapping of charge carriers in trapping centers caused by impurities in the silicon substrate. The lifetime of such a trapped state can be longer than the recovery time of the pixel. Once the electron is released again, it can re-trigger the avalanche process resulting in the observed afterpulse.

Dynamic Range

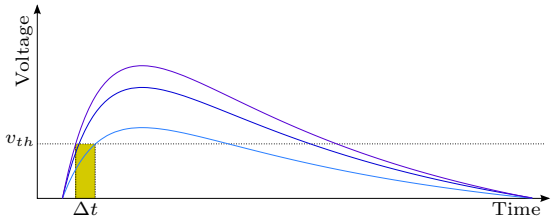
After a pixel has been triggered and the avalanche quenched, the bias voltage has to recover sufficiently before the pixel can detect another photon. If another photon is absorbed in the same pixel during the recovery time, the generated output signal of the sensor will be identical to a single photon signal. As long as the number of incident photons is sufficiently small compared to the number of pixels on the sensor, the response of the SiPM is linear to the incident light power. As the number of incident photons increases, the probability for two photons to be absorbed in the same pixel rises. This results in a saturation effect of the photo-sensor response, with the number of pixels as the maximum possible amount of simultaneously detectable photons. This saturation effect can be expressed by [42]:

$$N_{\text{firedcells}} = N_{\text{total}} \left(1 - \exp\left(-N_{\text{photon}} \cdot \text{PDE}/N_{\text{total}}\right)\right) . \tag{3.16}$$

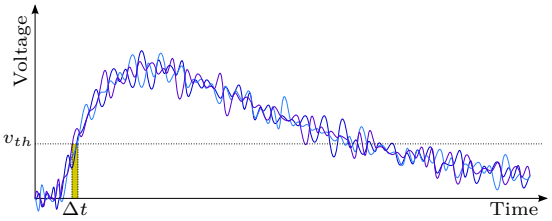
$N_{\text{firedcells}}$ denotes the number of triggered SiPM pixels, N_{total} the number of pixels on the sensor, and N_{photon} the number of incident photons. In order to increase the dynamic range of a Silicon Photomultiplier, the number of pixels has to be increased, which requires smaller pixel sizes. As a result, a trade-off between dynamic range and photon detection efficiency has to be made, since the PDE decreases with smaller pixel sizes.

3.2 Timing Measurements with SiPMs

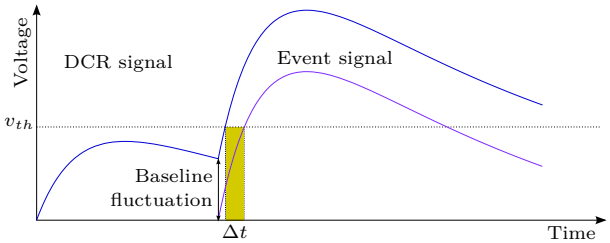
In many applications, such as the projects presented in Chapter 2, the measurement of the arrival time of incident photons with a high precision is of utmost importance. Typically a discriminator circuit is used to generate a logical trigger signal, which marks the point in time



(a) Timewalk effect for different signal amplitudes.



(b) Trigger jitter due to statistical noise.



(c) Timing error due to pile-up effects causing a baseline shift of the signal.

Figure 3.9: Error contributions to the precision of a time trigger.

at which the sensor output signal has passed a certain threshold value. The precision with which the trigger signal corresponds to the signal timing is determined by the noise of the system, the slope of the sensor signal, as well as the fluctuation of the signal rise time. The contribution of the error sources to the trigger precision are shown in Figure 3.9.

For a fixed signal rise-time, the time-walk effect describes the shift in the trigger timing due to different signal amplitudes, as it is shown in Figure 3.9a. Since the shift of the trigger signal has a fixed relation to the amplitude of the detector signal, this effect can be characterized by measurements and corrected.

The noise affecting the signal introduced by the detector and readout system can cause the signal to cross the discrimination threshold at an earlier or slightly delayed point in time. This *timing jitter* effect is shown in Figure 3.9b. The error of the timing measurement Δt caused by the jitter effect is the ratio of the system noise level σ_{sys} to the slope of the detector signal at the threshold level. Since most noise sources contributing to the signal have a random distribution, the timing jitter cannot be corrected for. To reduce its contribution to the timing resolution, a fast signal rise-time has to be ensured and the noise level reduced as much as possible.

The precision of the generated trigger signal is also affected by the baseline shift due to signal pileup, as it is shown in Figure 3.9c. Especially in large devices with a high dark count rate, the pileup of DCR signals with the event signal is one of the main factors limiting the time resolution. New sensors with purer silicon and lower DCR therefore provide a better resolution, which can be further improved by cooling the SiPM to lower temperatures. The influence of the pileup effect on the signal timing can also be reduced by software methods [43]

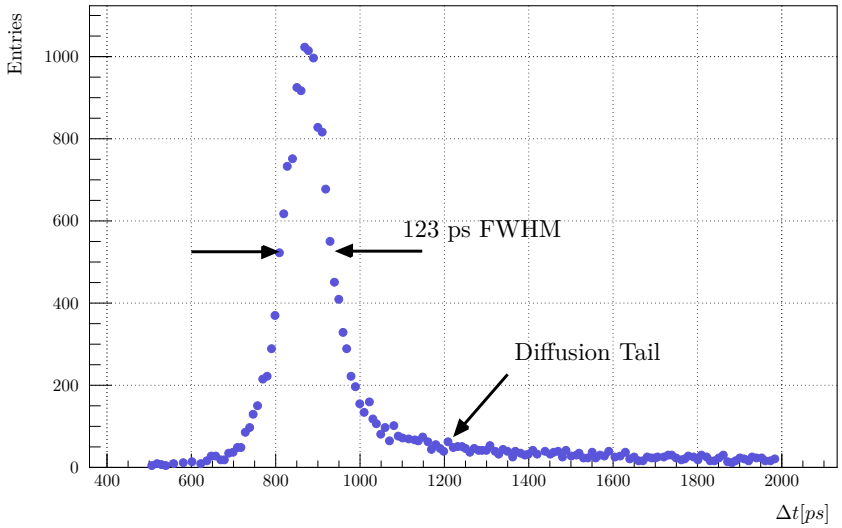


Figure 3.10: Measurement of the single photon timing resolution for a SiPM. Data taken from [45].

or tail cancellation circuits in the readout electronics [44].

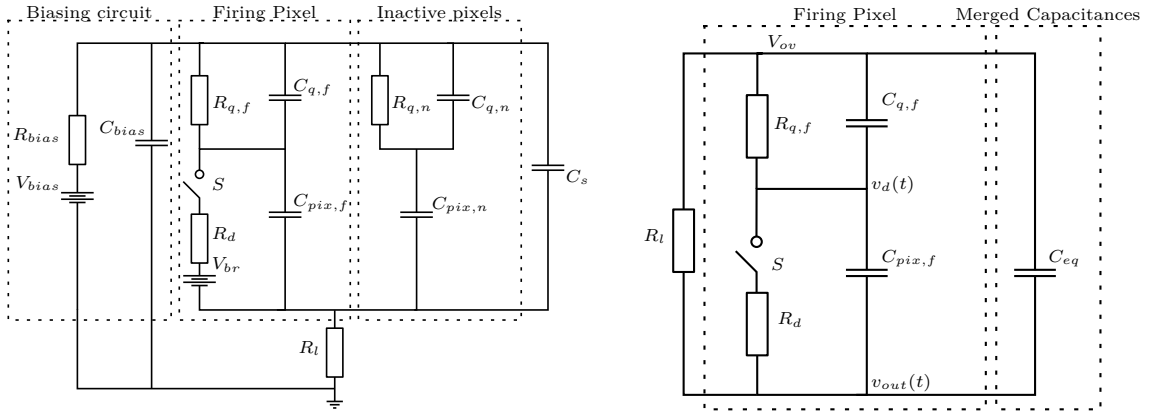
The fast avalanche process of Silicon Photomultipliers results in a fast signal rise-time and thus provides a high intrinsic timing resolution. For timing measurements in the picosecond regime, many effects become important which have been so far neglected, such as fluctuations in the development of the avalanche process and the contributions from parasitics of the sensor design. The impact of these characteristics on the timing resolution will be discussed in the following sections.

3.2.1 Avalanche Fluctuations

The physical limit of the timing resolution is determined by the fluctuation of the time required for the output current of a SPAD cell to cross a defined current threshold. Two main factors are contributing to the uncertainty of this response time, namely the time required by the generated charge carriers to drift from the absorption region to the multiplication region, and statistical fluctuations of the ionization processes creating the avalanche breakdown.

A delayed triggering of the avalanche breakdown can occur, if the photon is not absorbed in the multiplication region, but in the intrinsic absorption region. The charge carriers generated in this region will slowly diffuse to the multiplication region, where they can then start the avalanching process in the high field region. Since the absorption coefficient is wavelength dependent, the depth of the photon absorption and thus the average diffusion time also has a spectral dependence [46].

The fluctuations of the statistical ionization process have been investigated for shallow junction SPADs by Spinelli et al. [47]. Their analysis shows that the fluctuations in the build up process of the generated diode current are dominated by the lateral and photon



(a) Detailed equivalent model of a SiPM.

(b) AC model used for the calculation of the fast avalanching process.

Figure 3.11: Detailed models used for the analytical analysis of the SiPM response [49].

assisted spreading of the avalanche. The fluctuation of the vertical avalanche build up in the direction of the electrical field have only a minor influence on the timing resolution. Due to the finite pixel size, the lateral spreading is limited by the pixel borders. Consequently, the timing resolution becomes worse for avalanche seed points at the pixel borders compared to breakdowns originating in the center of the pixel [48].

Using high precision readout electronics to measure the single photon timing resolution (SPTR) of a SiPM, the two effects become visible in the resulting time spectrum. Figure 3.10 shows the measurement of a SiPM SPTR conducted by Buzhan et al. [45]. The main peak shows an SPTR of 123 ps FWHM. The long diffusion tail visible in the spectrum is caused by the drift time of electrons to the multiplication region.

3.2.2 Detailed Equivalent Circuit

For the development of high precision front-end electronics with the goal of achieving picosecond timing resolution, a detailed electric equivalent model of Silicon Photomultipliers is mandatory. Figure 3.11a shows the equivalent circuit of a SiPM, including additional components to describe the contributions from the external biasing circuit, detector parasitics, untriggered pixels, as well as the load of the front-end electronics used to process the sensor signal.

The avalanche breakdown of the SPAD cell is again modeled by the discharge of a capacitor $C_{pix,f}$ over the sensor resistance $R_{d,f}$. The quench resistor fabricated on the sensor surface adds a significant parasitic capacitance $C_{q,f}$, which has a strong impact on the signal formation, especially during the fast discharge and quenching operations after a pixel has been trigger. The switch S is open at all times for passive pixels. The circuit modeling these untriggered pixels therefore only contains the quenching resistor $R_{q,n}$ with its parasitic capacitance $C_{q,n}$, and the pixel capacitance $C_{pix,n}$. The metal interconnections used for the parallel connection of the pixels are distributed over the sensor surface and add an additional parasitic capacitance

C_{pix}	C_q	C_s	R_q	R_d
78 fF	8 fF	1 fF	250 kΩ	1 kΩ

Table 3.2: Extracted electrical parameters for a Hamamatsu MPPC (S11828-3344MX) at 25.5°C. Values taken from [50].

C_s. The biasing circuit consists of a resistor R_{bias} and a capacitor C_{bias} with typical values of 10 kΩ and 100 nF respectively. Neglecting bandwidth limitations of the readout electronics, the input impedance of the readout front-end electronics is described in the equivalent circuit by the resistor R_l. The values for inductances, capacitors and resistors in the model can be extracted using LCR meters and typical values are given in Table 3.2.

An extensive analysis of the detector response has been performed by Marano et al. [50], including the breakdown and quenching processes, as well as the recharging operation of the pixel. For the evaluation of the fast timing response of the sensor, only the fast rising edge and quenching process of the generated current pulse in the analysis are of interest. In this high frequency domain, the equivalent circuit can be simplified to allow an easier analytical analysis. The schematic of the simplified AC model is shown in Figure 3.11b. Because of the fast rise time of the signal, the impedance offered by the unfired microcells is solely determined by their capacitive elements in the equivalent circuit. Assuming $R_l \ll R_{q,n}$, the capacitances can be conveniently merged into an equivalent capacitance C_{eq}, describing the impedance of the passive pixels and the parasitics of the metal grid, with

$$C_{eq} = \frac{C_{pix,n} \cdot C_{q,n}}{C_{pix,n} + C_{q,n}} + C_s = (N - N_f)\frac{C_{pix} \cdot C_q}{C_{pix} + C_q} + C_s \,. \tag{3.17}$$

N denotes the total number of pixels and N_f the number of fired pixels.

As in the previous model, the avalanche breakdown is modelled by the closing of switch S at the time $t = 0$. The initial voltage at node v_d before the breakdown is $v_d(0) = V_{ov}$. After the switch is closed, the capacitor C_{pix} is discharged over the resistor R_d.

To analyse the circuit, the Lorentz-transformation of the corresponding differential equations into s-space is an instrumental method to solve the equations and gain more insight into the circuit behaviour than possible in the time domain. The individual steps of the calculations for this analysis have been performed in [49] and are summarized below. The differential equations corresponding to the simplified circuit in Figure 3.11b and their initial conditions are:

$$\begin{aligned}
&C_q \tfrac{dv_d(t)}{dt} + \tfrac{v_d(t)-V_{ov}}{R_q} + C_{pix,f}\left(\tfrac{dv_d(t)}{dt} - \tfrac{dv_{out}(t)}{dt}\right) + \left(\tfrac{v_d(t)}{R_d} - \tfrac{v_{out}(t)}{R_d}\right) = 0 \\
&C_q \tfrac{dv_d(t)}{dt} + \tfrac{v_d(t)-V_{ov}}{R_q} + C_{eq}\tfrac{dv_{out}(t)}{dt} + \tfrac{v_{out}(t)}{R_l} = 0 \\
&v_d(0) = V_{ov}\,, \\
&v_{out}(0) = 0\,\mathrm{V}\,.
\end{aligned} \tag{3.18}$$

Since all discrete components in the differential equations have constant values, the Lorentz transformations are determined by

$$\mathcal{L}(v(t)) = V(s)\,, \quad \mathcal{L}(\tfrac{v(t)}{dt}) = sV(s) - V(0)\,\text{and} \quad \mathcal{L}(V_{ov}) = V_{ov}/s\,.$$

This makes the transformation of the differential equations in 3.18 to the s-domain straight forward:

$$\begin{aligned} C_q \cdot sV_d(s) + \tfrac{V_d(s)-V_{ov}/s}{R_q} + C_{pix,f} \cdot s\,(V_d(s) - V_{out}(s)) + \left(\tfrac{V_d(s)}{R_d} - \tfrac{V_{out}(s)}{R_d}\right) &= 0 \\ C_q \cdot sV_d(s) - C_q \cdot V_{ov} + \tfrac{V_d(s)-V_{ov}/s}{R_q} + C_{eq} \cdot sV_{out}(s) + \tfrac{V_{out}(s)}{R_l} &= 0 \end{aligned} \tag{3.19}$$

After the Lorentz transformation, the former differential equations can be solved arithmetically, and the transient circuit behaviour in the time domain can then be determined using the inverse Laplace transformation on the functions in the complex s-space. Solving Equation 3.19 for the output voltage $V_{out}(s)$ yields

$$V_{out}(s) = \frac{R_l \cdot V_{ov} \cdot (1 + s \cdot C_q R_q)}{s \cdot (a_0 + a_1 s + a_2 s^2)}\,, \tag{3.20}$$

with

$$\begin{aligned} a_0 &= R_d + R_q + R_l\,, \\ a_1 &= R_d \cdot (C_q R_q + C_{eq} R_l) + R_l(C_{pix} R_d + C_q R_q) + R_q(C_{pix} R_d + C_{eq} R_l)\,, \\ a_2 &= C_{pix} R_d \cdot C_q R_q \cdot R_l + C_{eq} R_l \cdot C_q R_q \cdot R_d + C_{pix} R_d \cdot C_{eq} R_l \cdot R_q\,. \end{aligned}$$

With the extracted parameter values from Table 3.2, the constants a_0 to a_2 can be approximated with

$$a_0 \approx R_q\,, \quad a_1 \approx R_q(C_{pix} R_d + C_{eq} R_l)\,, \quad a_2 \approx C_{pix} R_d \cdot C_{eq} R_l \cdot R_q\,.$$

With the definitions $\tau_q = C_q R_q$, $\tau_l = C_{eq} R_l$, and $\tau_d = C_{pix} R_d$, the inverse Laplace transformation of $V_{out}(s)$ then results in

$$v_{out}(t) = \mathcal{L}^{-1}(V_{out}(s)) = \frac{R_l \cdot V_{ov}}{R_q}\left(1 + \frac{\tau_d - \tau_q}{\tau_l - \tau_d} \cdot \exp(-\frac{t}{\tau_d}) - \frac{\tau_l - \tau_q}{\tau_l - \tau_d} \cdot \exp(-\frac{t}{\tau_l})\right) \tag{3.21}$$

Since the time-jitter of a timing measurement is determined by the slope of the signal, the interesting quantity is the first derivative of the output current $i_{out}(t)$ at time $t = 0\,s$, when the avalanche has been triggered. With $i_{out}(t) = v_{out}(t)/R_l$, the first derivative is given by

$$\frac{d}{dt} i_{out}(t) = \frac{V_{ov}}{R_q}\left(\frac{\tau_q - \tau_d}{\tau_d(\tau_l - \tau_d)} \cdot \exp(-\frac{t}{\tau_d}) + \frac{\tau_l - \tau_q}{\tau_l(\tau_l - \tau_d)} \cdot \exp(-\frac{t}{\tau_l})\right)\,, \tag{3.22}$$

and at the avalanche starting point, the slope of the current through the readout resistor R_l is

$$\frac{d}{dt} i_{out}(0) = \frac{V_{ov}}{R_q} \cdot \frac{\tau_q}{\tau_d \tau_l} = \frac{C_q \cdot V_{ov}}{R_l \cdot C_{pix} R_d \cdot C_{eq}} \,. \tag{3.23}$$

This equation provides insight in the separate factors affecting the timing resolution of a SiPM. Factors in the numerator increase the slope of the signal and thereby the resolution, while factors in the denominator reduce it. As one would expect, the slope of the current signal increases with rising over-voltage V_{ov}. However, an increased bias voltage also increases other parameters which have a negative impact on the time resolution, such as the DCR. Consequently, an optimal over-voltage exists, which provides the best timing performance for the sensor. The parasitic quench capacitance C_q is also beneficial for the timing response of the sensor. This relation can be exploited by artificially increasing the parasitic C_q in the layout by using wider quench resistors, thus improving the time resolution of the single pixel signals.

The combined equivalent capacitance of not-fired pixels and parasitic interconnect capacitance in the denominator reduces the slope of the current output. Inserting relation 3.17 in Equation 3.23 shows that both, the pixel capacitance and the parasitic capacitance of the interconnections decrease the timing resolution. Sensors with smaller pixel size and smaller total surface area reduce these capacitances and thereby provide a better timing performance.

As can be seen by the relation of $\frac{d}{dt} i(t)$ to R_l, a large input impedance decreases the signal slope. This shows that a high timing resolution can only be achieved, if the input impedance of the front-end readout electronics is reduced as much as possible. In the analog design, Equation 3.23 can be used to optimize the input impedance for the best possible timing resolution. Since the input impedance has in general a limited bandwidth, the results using Equation 3.23 only give an indication for the optimization. A more accurate assessment of the performance is only possible by using simulations of the detailed electrical equivalent model together with the front-end readout circuits.

Chapter 4

Mixed-Signal ASIC Design

With the development of ASICs, it is possible to design optimized readout electronics tailored to the specific requirements of a detector system. The development of ever smaller feature sizes allows to continuously improve the performance of the circuits and integrate more functionality on the same die area. Modern deep-submicron fabrication processes allow to combine the analog readout electronics together with digital processing circuits in a System-on-Chip (SoC). In this way, the performance and integration required by state-of-the-art detectors can be achieved.

In such mixed-signal ASICs, the information of the processed analog sensor signals is digitized and stored inside the chip. The integrated digital logic is used to process the recorded data before the transmission to an external DAQ system. In contrast to analog signals, the digital data signal is not deteriorated during transmission, and the early digitization can thus preserve the performance of the analog readout circuits. The digital logic is also used to configure the settings of the analog processing, allowing to fine-tune the circuit for the best performance after the production.

The highly complex design of mixed-signal ASICs can only be handled with electronic design automation (EDA) methods and tools for the development of the electronic circuits. Because of the complex manufacturing process of integrated circuits, the production typically requires several months and is expensive. As a consequence, the design must be extensively validated before the production, or *tape-out*, to minimize the risk of a non-functional circuit.

This chapter presents the general design steps from the start of a chip concept to the final sign-off verifications, required to ensure a working design. The design flow used in this thesis is based on the dissertation of Andreas Grübl [51]. Before the individual steps are described in detail, an overview of the whole design process is presented.

4.1 Design Flow Overview

In the first step of an integrated circuit design, the electronic specifications have to be defined. These are typically derived from the requirements of the detector system, which pose constraints on power consumption, performance of the system, required event rate, system clock frequencies, and many more. Often these requirements oppose each other, such as power consumption and performance, and a compromise has to be found.

During the design process, the defined specifications are implemented in the analog and digital logic circuits. The design flow for the development of mixed signal ASICs is shown

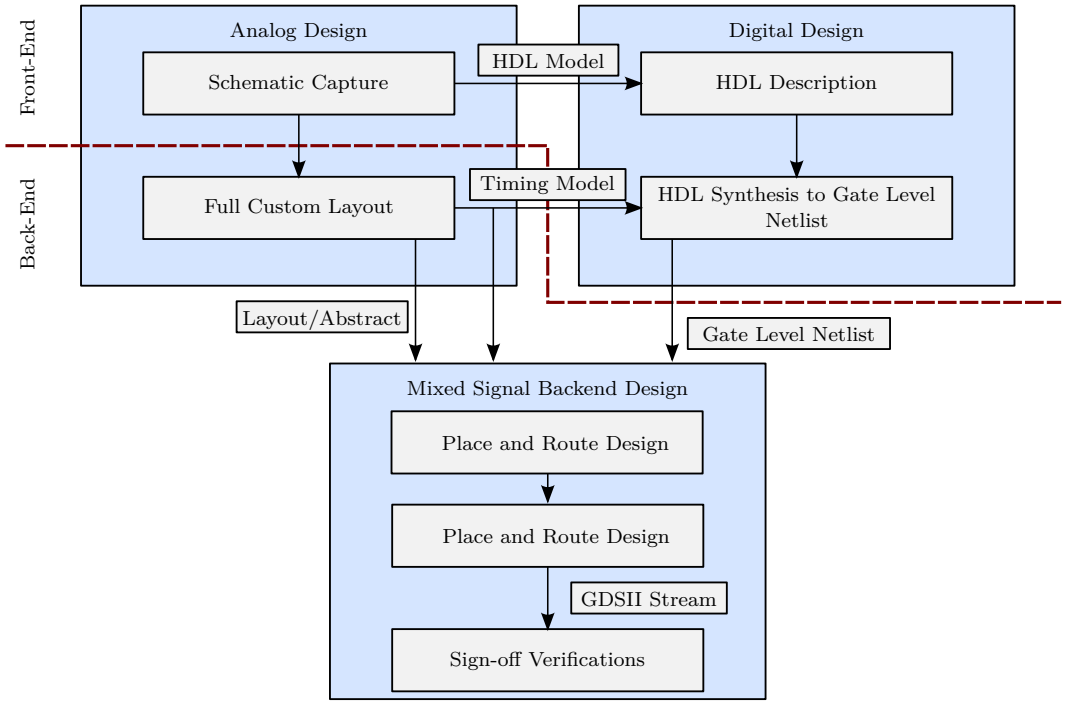


Figure 4.1: Mixed signal ASIC design flow.

in Figure 4.1. The process can be divided into two steps, which are called *front-end* and *back-end* [1] design. Front-end refers in this context to the description of the analog and digital circuits, whereas the back-end describes their physical implementation in the semiconductor technology.

During the front-end design phase, the analog signal processing is developed using schematic diagrams, in which the individual components of the circuit, such as the transistors are manually defined and connected. Since all parameters of the circuit can be controlled by the designer, the full custom approach of the analog design allows to fully optimize the critical analog circuits.

The complexity of modern digital circuits is too high to be conveniently described using schematic diagrams. The digital circuit of the design is therefore developed at a higher abstraction level using a hardware description language (HDL) such as VHDL[52] or Verilog[53]. The HDL is also used to describe the top-level of mixed-signal designs, which describes the instantiation of the analog and digital modules and their interconnection. For the physical implementation, the logic described in the HDL code is automatically synthesized into a gate-level netlist using the logic elements of a predefined standard-cell library. The EDA tools will automatically optimize the described logic during synthesis based on the provided system constraints and the available logic gates.

[1] The term front-end is is also used for the front-end readout electronics, which refer to the first signal processing stage of the readout electronics. In this chapter, front-end and back-end refer exclusively to the design flow stages.

A critical point in mixed-signal designs is the interface between analog and digital circuits. To correctly define the interconnections at this interface and verify the digital logic in combination with the analog signal processing, the behaviour of the analog circuits is introduced to the digital front-end design using HDL simulation models.

To correctly implement the described interface between the digital and analog circuits, the signal timing of the digital input and output ports of the analog macro blocks has to be characterized by timing models. The detailed information contained in these models is used during the digital synthesis and the back-end design process to generate the correct timing of the signals at the analog-digital interfaces.

The implementation of the ASIC into a physical layout takes place in the back-end phase. For the analog design, the circuit components described in the schematics are manually instantiated and connected. As with the schematic capture, the manual control of all semiconductor device geometries allows a full optimization of the analog circuit. The geometric informations of the finished layout are exchanged between the EDA tools using abstract views which contain only the necessary informations for the further physical implementation, such as the cell geometry, pin positions and allowed space for metal routing within the module.

During the mixed-signal back-end design, the individual components are arranged in a floorplan of the chip, which defines the positions of the analog modules and the areas for digital logic cells. Based on the digital logic defined in the gate-level netlist and the design constraints, the digital cells are placed in their respective areas of the floorplan and the metal interconnections, except for critical analog signal paths, are routed automatically.

In the last step, the abstract views of the analog and digital cells used during the physical implementation are replaced by their physical layouts and combined into a single output file. After this design passes all sign-off verification procedures, the chip is ready for production and can be submitted to the foundry. The individual steps of this design process are complex and will be described in more detail in the following sections.

4.2 Analog Design Implementation

The design of analog integrated circuits requires a detailed understanding of the underlying signal processing theory, which is covered extensively in literature [27, 54, 55]. Often the same functionality can be achieved in many different ways, and the designer has to decide which solution fits best to the system requirements. For the design of analog readout circuits providing a high precision timing trigger such as the STiC ASIC, the relevant theory is summarized in the dissertation of Wei Shen[49].

The performance of analog circuits is sensitive to second-order effects of transistors, as well as noise and crosstalk sources in the layout, which interfere with the signal processing. In addition, the behaviour of the circuit is influenced by variations in the manufacturing process, the temperature during operation and the supply voltage, which are denoted as PVT effects.

The design of robust analog circuits therefore poses a challenging task to the designer. It

requires knowledge of the manufacturing processes to minimize the device variations after the production already during the layout phase of the circuit. In order to also take the characteristics of the chip environment into account the electrical properties of the external connections to the chip, such as resistivity and inductance of bonding wires or the chip package have to be considered.

Although some EDA tools provide algorithms to support the optimization of a circuit based on parameters and target constraints, analog integrated circuit designs still require a manual work flow, which puts the control of all component parameters and physical layout geometries in the hands of the designer. The design of the STiC ASIC has been developed with the Cadence Virtuoso tools, which provide a complete tool chain for the conception and simulation of analog schematic diagrams, as well as their transfer to the physical implementation.

4.2.1 Schematic Circuit Capture

To cope with large analog designs, a hierarchical structure is used to subdivide the circuit into smaller cells, as illustrated in Figure 4.2 for a simple design example. The hierarchical approach allows to concentrate the development effort on critical key components in the circuit and develop the individual modules in parallel by several analog designers. The reduced complexity of the sub-blocks makes them accessible to analytical analyses of the corresponding circuit transfer functions using Laplace transformations. Like the electrical model for SiPMs, this analytical calculation gives a better insight into the parameters affecting the relevant circuit behaviour, allowing a well-directed optimization of the design.

The separate blocks are developed using a schematic representation of the circuit components, their parameters, and their interconnection. At the lowest level of the hierarchy, the schematic contains only basic components such as transistors, diodes, capacitors and resistors. This transistor level schematic is shown in Figure 4.3a for a simple inverter module.

Electrical simulation programs allow to calculate the transient behaviour of the circuit by solving the differential equations describing the circuit with numerical algorithms. Most simulators are based on the Simulation Program with Integrated Circuit Emphasis (SPICE) simulator, which has been introduced by Nagel and Pederson in 1973[56]. For the simulation, the instantiated components and their interconnections are described in a SPICE netlist, corresponding to the circuit schematics. The netlist of the simple inverter module mentioned before is given in Figure 4.3b as an example. Component models of the instantiated devices

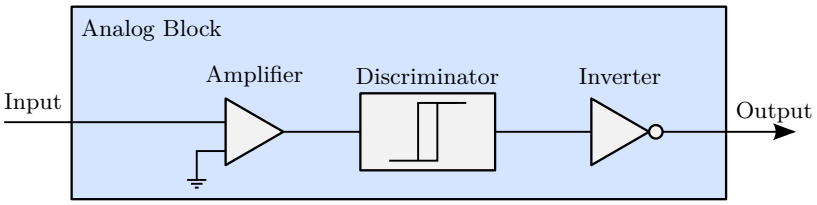
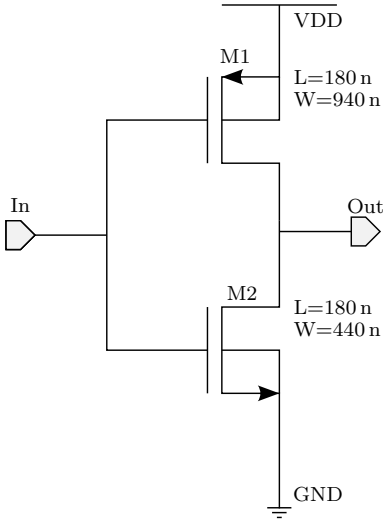


Figure 4.2: Block level diagram of an analog design.



(a) Schematical representation.

```
1  .SUBCKT INV In Out
2  *.PININFO in:I Out:O
3  M1 Out In vdd! vdd! PMOS_18
     W=940.0n L=180.0n M=1.0
4  M2 Out In gnd! gnd! NMOS_18
     W=440.0n L=180.0n M=1.0
5  .ENDS
```

(b) Spice netlist for simulation.

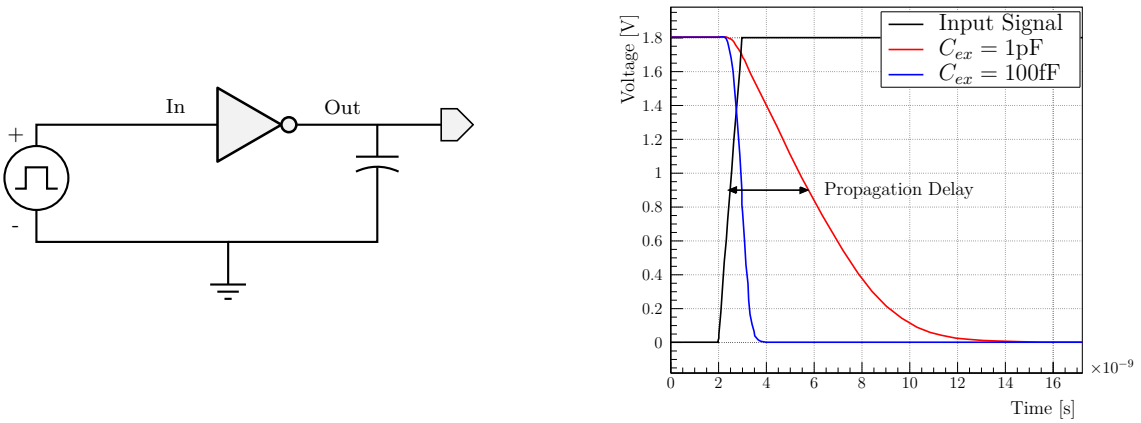
Figure 4.3: Example of a simple inverter circuit. The parameters L and W denote the length and width of the transistor geometry.

in the circuit are used during the simulation. These models are typically supplied by the semiconductor foundry, containing detailed information about the electrical behaviour of the devices as well as their known parasitics.

The variations of the fabrication parameters are represented by different models for the so called production corners. A typical naming convention for the different models is the two letter representation of the carrier mobilities for n-MOS and p-MOS transistors, also called Front-End-Of-Line (FEOL) corners. Five corners exist in this convention, representing the extreme points in the statistical fluctuation of the production process. They are called fast-fast (ff), slow-slow (ss), slow-fast (sf), fast-slow (fs), and typical-typical (tt). The first letter refers to the mobility in n-MOS transistors, the second letter to the mobility in p-MOS devices. To ensure a robust design and high production yield, the designed circuit has to pass the simulations in every process corner. For the design of sensitive analog signal processing, more extensive Monte-Carlo models can be used to verify the design against random variations of individual component parameters in the circuit.

An accurate simulation also has to take the influence of the connections at the input and output terminals of the module into account. The modules are therefore instantiated in a simulation testbench, which emulates a simplified electrical environment of the circuit.

The SPICE simulation of the inverter transient response is shown in Figure 4.4. To simulate the capacitive load of connected components at the output terminal, a capacitor has been added in the simulation testbench, which is shown in Figure 4.4a. The size of the capacitor has a strong influence on the transition times of the output signal. With a larger capacitor, the transition time also increases. In addition, the response of the inverter also depends on



(a) Simulation testbench

(b) Simulated transient response

Figure 4.4: SPICE simulation of the inverter module presented in Figure 4.3.

the signal shape at the input terminal. As it will be described in Section 4.4, the timing models of analog circuits used in mixed-signal designs are based on such simulations. They characterize the signal properties, such as the propagation delay of a signal through the cell or the transition time of the output signal with respect to the output load capacitance and the transition time of the input signal.

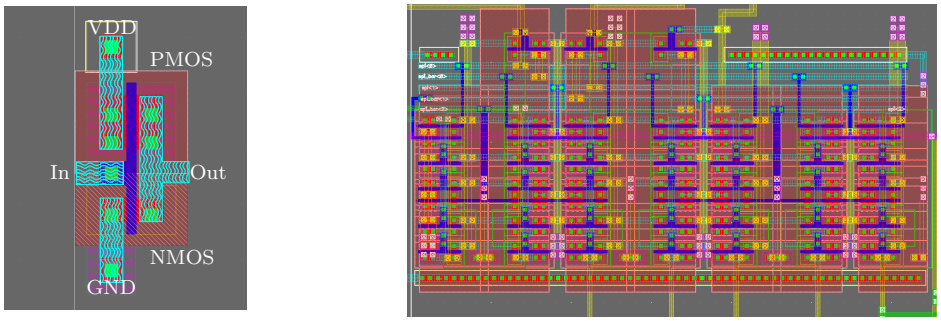
The influence of input signal characteristics and output load on the behaviour of the module also shows that, although the submodules in the hierarchy of an analog block can be designed individually, the validation of the circuit behaviour has to be performed at the top-level including all sub-modules, as well as a sensible estimation of the external electronic environment.

4.2.2 Analog Layout

For the fabrication of the circuit in the chip, the components defined in the schematics are transfered into the physical layout of the analog module, which describes the geometrical shapes of semiconductor material, metal and oxide layers that make up the integrated circuit. The layout significantly affects the design performance, since it introduces additional parasitic capacitances and resistances[2] to the circuit. A careful layout can minimize the introduced parasitics and also cancel out parameter fluctuations of devices which have to match closely. Figure 4.5 shows examples for the layout of the inverter circuit and a more complex analog design as examples. The different aspects of the analog layout process affecting the circuit performance are described in [57].

Before the production, the layout has to pass several verification processes. The mentioned parasitics caused by the metal interconnects can be extracted from the layout and introduced

[2]Both parasitic contributions are in general referred to as parasitics.



(a) Simple inverter layout. **(b)** Example layout of a larger analog block.

Figure 4.5: Analog design layout examples.

to the SPICE simulations of the circuit. These post-layout simulation are mandatory to ensure a working circuit. Often the design process contains several iterations of post-layout simulations, modifications in the circuit schematics, and changes in the physical layout before the desired performance is achieved.

For the manufacturing process, the design layout also has to pass physical verifications which are explained for the full chip layout in Section 4.5.5. After successful verification of the design, the analog macro block is ready to be implemented in the mixed-signal design. The required informations for instantiation in the mixed-signal design flow, and how they are passed to the back-end tools will be described in Section 4.5.

4.3 Digital Design Implementation

The digital design of a mixed-signal ASIC has to perform a multitude of different tasks simultaneously. It handles the signal processing of the digitized analog signals, provides control logic to steer the operations of the analog design and is responsible to provide a communication interface to the external DAQ system controlling the chip. To ensure a stable operation of the system, the logic circuit has to be tolerant of invalid data generated by the communication interface, the analog modules, or by accidental bit flips due to cross-talk or irradiation of the chip. Especially in high radiation environments, the probability to generate bit-errors in a random part of the module is high, and the development of radiation-hard digital designs has become an active field of research[58, 59].

In contrast to analog circuits, the size and complexity of the digital logic is too large to be developed within a reasonable timescale using a manual work flow. Because of this, the digital design is described using high level hardware description languages such as Verilog and VHDL. Together with constraints defining clock frequencies and signal timing, and a library of standard cells providing logic functions and storage elements, the EDA tools can automatically synthesize a gate-level netlist for implementation in the chip. This abstraction of the circuit to a behavioural description allows the designer to concentrate on the development

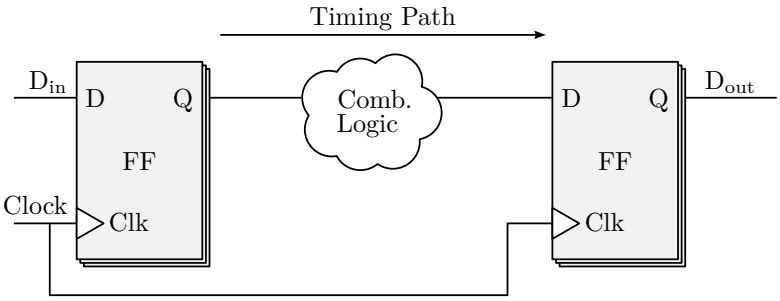


Figure 4.6: Synchronous digital design at the RTL level. The data of a register stage is processed by combinatorial logic and stored at the next clock cycle in the subsequent register stage.

and optimization of the complex digital logic independently of it's implementation in the hardware. Since the digital netlist for implementation is generated automatically based on the interpretation of the HDL code, a detailed knowledge of the used EDA software and the underlying synthesis process is required to ensure that the logic circuit is created as intended. The analog modules and their interconnections to the digital part also have to be defined in the netlist of the design. The flow used in this thesis allows to instantiate the analog modules directly in the HDL description based on HDL models and the timing models extracted from the analog design.

4.3.1 Register Transfer Level Description

Digital circuits are typically described at the register transfer level (RTL), which describes the circuit by the data flow between register elements. These storage elements are mostly implemented as Flip-Flops, which store the logic state of a signal at the rising or falling edge of a clock signal. At the RTL, which is graphically shown in Figure 4.6, the output of a register stage is processed by combinatorial logic, and the result of this boolean operation is stored in a subsequent register stage. In this way, the data processing advances in each clock cycle from one register stage to the next.

Hardware description languages are used to describe digital logic at the register transfer level. Based on the HDL source, the logic design can be simulated, as well as synthesised to a lower abstraction level. Large digital designs use a hierarchical approach to subdivide the design into smaller entities, which provide distinct logic functions. These entities can be parametrized to create flexible modules for regularly used logic functions. Using the behavioural description, digital designs ranging from simple control logic to fully fledged microprocessors can be conveniently described and tested.

Unlike SPICE simulations of analog circuits, the simulation of digital designs at the register transfer level can be simplified to the calculation of the logic signal states at the next clock cycle. This leads to a much faster simulation speed for digital circuits. Furthermore, simulators can evaluate statements inside the HDL code which are only executed during simulations, but will not enter the synthesised design. This allows to automatically check for invalid signal conditions and perform an extensive validation of the circuits functionality. To increase

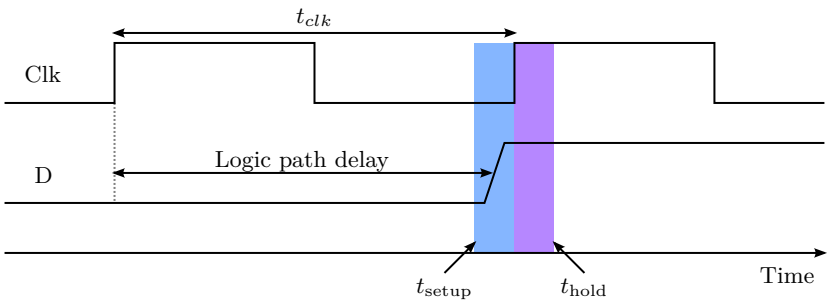


Figure 4.7: Setup and hold time windows at the register stages in synchronous digital circuits.

the coverage of possible logic states, constrained random verification methods [60] are used to generate random stimuli at the input of the digital circuit, testing not only anticipated conditions, but also unexpected situations and logic states.

In a synchronous digital design, not only the logic functionality but also the signal timing has to be investigated. To ensure that the data is correctly stored in the register stages, the digital signals have to be stable in a time window around the active clock edge. The timing violations that can arise from this restriction are depicted in Figure 4.7. Setup violations occur, if the data at the input port D of a register changes within the setup time t_{setup} before the active clock edge. Similarly, the signal has to be stable during the hold time t_{hold} after the clock edge. Setup and hold time violations can cause metastable states of the storage elements, leading to an undefined value of the output signal of the register. The required setup time limits the maximal clock frequency, at which the circuit still meets the timing requirement. This frequency is determined by the longest logic path between two subsequent register stages, which is also called *critical timing path*. The validation of the correct signal timing is performed during the implementation process and is described in Section 4.4. Despite the missing delay information of the signal paths during the behavioural description, long combinational logic paths can already be subdivided by pipelining the signal processing steps with additional register stages. Taking long paths already at this early stage of the design process into account reduces the difficulty to achieve the timing requirements during the implementation process.

4.3.2 Circuit Synthesis

The logic synthesis of a digital design is the process of converting the abstract RTL description of the logic into an optimized gate-level netlist. The gate-level netlist is mapped to a standard cell library, which contains a predefined set of logic gates for the physical implementation in the specific fabrication process. The general steps of the synthesis design flow are shown in Figure 4.8 for the Synopsys Design Compiler, which has been used for the design of the STiC ASIC. A full description of the design flow can be found in the Design Compiler® User Guide[61].

The synthesis process can be separated into two steps. In the first step, the HDL code of

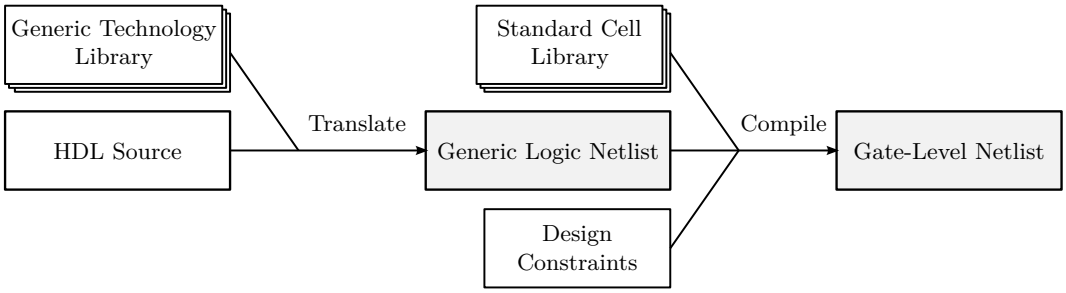


Figure 4.8: Digital Synthesis Flow with Synopsys Design Compiler®.

the design is read and translated into an intermediate netlist of logic gates using a generic technology (GTECH) library. The GTECH library contains basic logic gates and storage elements.

During the compilation step, this intermediate netlist is optimized and mapped to the standard cell library, which is also referred to as target technology library. This library has to contain the required informations about the characteristics of each provided logic gate to allow a correct mapping and optimization of the circuit. According to the specifications described in the Library Compiler User Guide from Synopsys[62], a technology library has to contain the following informations:

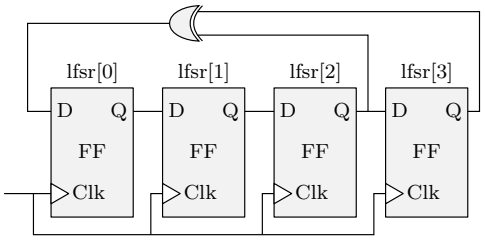
- The provided logic function of the logic cell, i.e. the state of the output signals of the cell as a function of the input signals. This information is used to map the generic netlist to a netlist of standard cells.
- The timing information, describing the pin-to-pin timing relationships and propagation delays of the cells. As described later, the cell timing is a critical information since it is used for the timing analysis and optimization of the design.
- The structural informations, describing the geometry of the cell and it's pin and bus connections to the outside world, which are essential for the physical implementation.
- Environmental information, describing the effects of variations in the manufacturing process, the supply voltage, and the layout on the efficiency of the design.

For commercially available standard cell libraries, these informations are already provided by the manufacturer. In a mixed-signal design, the technology library of instantiated custom analog modules has to be extracted from SPICE simulations and the analog layout. Special attention has to be paid to the correct definition of the timing information, as it specifies how the digital part has to interface to the analog modules.

The compile process is driven by design constraints, which contain timing and environmental restrictions, such as clock frequencies, which have to be met during the synthesis process. The standard cell library provides multiple cells which differ in size and driving strength for the logic functions. The EDA tools can exchange logic gates with an equivalent cell of different size to meet the design constraints and avoid design rule violations. In addition, buffer cells

```
1  fb <= lfsr(3) xor lfsr(2)
2  process(clk)
3  begin
4    if rising_edge(clk) then
5      lfsr<=lfsr(2 downto 0) & fb;
6    end if;
7  end process;
```

(a) RTL description.



(b) Synthesized design.

Figure 4.9: VHDL example for a linear feedback shift register.

which do not change the logic functions can be automatically added where necessary, to reduce the fan-out of signal nets with a high load. Figure 4.9 shows the example of a 4 bit linear feedback shift register described in VHDL and the gate-level netlist of the synthesis process, depicted by it's schematic representation. The Design Compiler software provides a graphical analysis of the required cell area for the design, the power consumption and the delay of the logic paths between registers based on the cell characteristics provided by the technology library. With this information, the RTL code can be optimized to improve the result after the synthesis process.

The generated logic in the gate-level netlist has to be verified to ensure the design still performs the desired functions. Two methods are typically used for this verification step. The design can be tested by simulating the response of the gate-level netlist with the testbenches used to simulate the behaviour of the RTL description. Another procedure is to transfer both, the RTL description and the gate-level netlist, to a mathematical representation of their boolean equations. By formally proving the equivalency of the two circuits the gate-level netlist can be verified [63]. The formal verification method provides the advantage of an exhaustive verification of the synthesis result, but has to rely on the correct verification of the described register transfer level logic as a reference.

In addition to the functional verification, the known cell delays from the standard cell library can be used to verify the timing of the digital design at the gate-level. A detailed description of the used timing analyses will be presented in the next section. Although the delay information at this point does not include delays introduced by the metal interconnections, a timing analysis can already identify the critical logic paths and verify the overall feasibility of the design. Logic paths violating the timing constraints at this design stage have to be fixed in the RTL code and the resynthesised design has to be verified again.

The synthesized and verified gate-level netlist is the starting point for the back-end design of digital and mixed-signal ASICs.

4.4 Static Timing Analysis

As already mentioned in the previous sections, the timing analysis of the digital design is, beside the functional verification, one of the most important steps in the design process of digital and mixed-signal ASICs. It calculates the delays of the combinational logical paths to ensure that the timing requirements, such as setup and hold times of the register stages are met. Two methods are used to validate the signal timing in digital designs: the timing simulation and the static timing analysis (STA).

In the timing simulation, the calculated signal delays are introduced to the functional simulations. A logic stimulus is applied to the input ports of the design and the propagation of the logic signals through the circuit is simulated with the included propagation delays. Although this approach allows to validate both the functionality and the timing of the circuit simultaneously, the coverage of the possible digital states depends on the used testbench generating the input stimulus and might not be exhaustive.

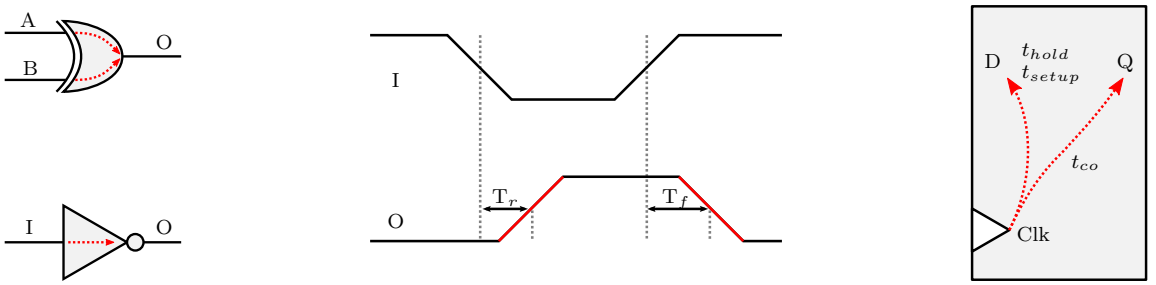
The purpose of a static timing analysis is to verify whether the described digital design can operate at the clock frequencies specified in the provided system constraints. As already mentioned in Section 4.3.1, the timing of a logic path has to meet the setup and hold times of the flip-flops, to ensure that the data is correctly stored in the cell. In addition, the design has to meet design rules specified in the standard cell library, which define a maximum transition time and a maximum capacitance for the signals connected to the gate terminals. The static timing analysis calculates the characteristics of the signal timing of every synchronous logic path and validates whether these constraints are met. In this way, the STA performs an exhaustive verification of the correct timing behaviour and provides reports on the critical paths in a design for optimization.

The STA is used by the front-end and back-end software to verify and optimize the design with respect to the timing restrictions. After the physical implementation, the design has to pass a detailed full chip STA verification before it can be submitted for manufacturing. The following sections provide a summary to understand the basic concepts of the static timing analysis. An extensive description of the used methods beyond the scope of this thesis is available in [64].

4.4.1 Logic Cell Timing Models

In order to perform a timing analysis of the digital circuit, accurate timing models of the logic cells have to be provided to the EDA tools. The Liberty format from Synopsys is the most widely adopted library format for exchanging timing models in the semiconductor industry. These models specify the maximum allowed capacitance at a cell output, signal transition design rules, the terminal capacitances, as well as the signal timing relations between the pins of a logic cell.

For a full-scale analysis, the propagation delays for every possible signal path between an input and output pin of a logic cell must be known. These so-called timing arcs are shown for



(a) Timing arcs of different combinational logic cells.

(b) Definition of the signal propagation delays through the inverter cell.

(c) Timing arcs of a sequential logic cell.

Figure 4.10: Definition of signal propagation delays in the timing library of standard cells.

an inverter and an XOR logic cell in Figure 4.10a. Since the signal timing behaves differently for 0-to-1 and 1-to-0 logic transitions, the delay and transition times of the output signal are specified separately for rising and falling signals. Figure 4.10b illustrates the definition of the signal propagation delays in the timing library using the example of the inverter cell. The output rise and fall delay times T_r and T_f are typically defined as the time difference between the output and input signal crossing the 50 % threshold between the logic 0 and logic 1 states. Similarly, the transition time, or slew rate of the output signal is defined as the time required for the voltage at the cell output to change from 30 % to 70 % of the logic high voltage.

Two parameters affect the propagation delays and the output slew rate of a logic cell, namely the transition time of the input signal and the capacitive load at the output terminal. While the slew of the output signal is in first approximation only determined by the capacitive load, the propagation delay is also affect by the transition time of the corresponding input signal. Consequently, the timing models have to characterize the cell parameters as a function of the input slew rate and the capacitance connected at the output terminal. Although linear models can be used to estimate the propagation delay and transition time from a simple linear combination of the parameters, these models are not precise enough for deep submicron semiconductor technologies. A more accurate model is provided by non-linear delay models (NLDM), which use two-dimensional lookup tables to specify the timing characteristics of the output signal for different combinations of input signal slew rate and capacitive load. The propagation delay and slew rate values entering the lookup tables are extracted from analog simulations using appropriate testbenches to simulate the analog response of the logic cell, as it has been shown in Figure 4.4b. The full timing characterization of a logic cell requires many analog simulations for the different parameter combinations and fabrication process corners. Software tools such as Variety from Altos Design Automation facilitate the characterization process by automatically performing the necessary SPICE simulations and extracting the required information into a Liberty library format.

For sequential storage elements such a flip-flops, the timing arcs are typically defined

between the clock input and the data output of the cell as it is depicted in Figure 4.10c. The clock to output delay t_{co} describes the time delay for the signal output to change after the active edge of the clock, at which the data is stored in the cell. In addition, a timing arc between the clock and data input is defined, specifying the required setup and hold times of the storage element.

4.4.2 Delay Calculation

The timing models of the standard cells are used to calculate the delay of a logical signal propagating from the output of a register through a combinational path to the input of the subsequent register stage and check if the timing requirements are met. Figure 4.11 illustrates the delay calculation for a logic path in the already presented $4-bit$ linear feedback shift register. As described in the previous section, the timing models require the signal transition time and the capacitive load at the output terminals of a standard cell to calculate the delay and slew rate of the corresponding output signal. The capacity connected to a cell output pin is the sum of the terminal capacitances of the connected cells and the parasitic capacitance of the metal interconnection. This parasitic capacitance of the metal traces is only known after the physical implementation of the design. For a timing analysis in earlier design stages, so-called wire-load models can be used, which estimate the additional parasitic capacitance from the signal fan-out. The parameters of externally driven logic signals entering the digital design have to be specified in the design constraints.

A timing report for the indicated logic path in Figure 4.11 can be generated after the design synthesis by the Synopsys Design Compiler software:

```
Point                              Cap     Trans      Incr       Path
---------------------------------------------------------------------------
clock sys_clk (rise edge)                             0.00       0.00
clock network delay (ideal)                           0.00       0.00
s_lfsr_reg[2]/CK (DFF)                    0.00        0.00       0.00 r
s_lfsr_reg[2]/Q (DFF) <-
                                  0.02    0.08        0.24       0.24 f
U5/O (XOR2)                       0.01    0.08        0.15       0.39 r
s_lfsr_reg[0]/D (DFF)                     0.08        0.00       0.39 r
data arrival time                                                0.39

clock sys_clk (rise edge)                             2.00       2.00
clock network delay (ideal)                           0.00       2.00
s_lfsr_reg[0]/CK (DFF)                                0.00       2.00 r
library setup time                                   -0.09       1.91
data required time                                               1.91
---------------------------------------------------------------------------
data required time                                               1.91
data arrival time                                               -0.39
---------------------------------------------------------------------------
slack (MET)                                                      1.52
```

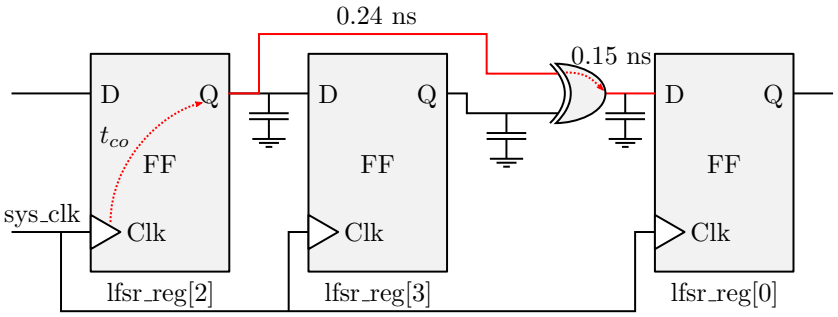


Figure 4.11: Delay calculation for a logic path in the 4 bit LFSR module.

The time unit used in the report is nanoseconds, the capacitances are given in picocoulomb. The frequency of the clock signal in this example has been constraint to 500 MHz. Two separate delay calculation are reported after the analysis.

The data required time is the time at which the data has to be stable at the destination flip-flop. It is calculated as the difference between the clock network propagation delay and the setup time of the register. The clock signal after the synthesis process is assumed to be ideal and arrives simultaneously at all storage elements. Because the clock signal is connected to thousands of register cells, a clock buffer tree has to be generated, which tries to equalize the propagation delay of the clock signal to all register cells. This step is typically done during the physical implementation of the design in the clock tree synthesis (CTS) step. The delays of the clock signal to the registers are thereafter known and included in the timing analysis steps.

The data arrival time is the time at which the logical signal as propagated through the combinatorial logic and changes at the input port of the register. The report also lists the estimated capacitance from the wire-load model and transition times for the logic signals in each propagation step. The slack of the timing path is the difference between the data required and arrival time. If the slack is positive, the required setup time is met and the digital circuit can operate at the specified clock frequency. In the various optimization steps during the implementation process, the EDA tools try to meet the design constraints and maximize the slack of critical timing paths. This process is referred to as *timing closure*.

After physical implementation, the design has to pass an extensive static timing analysis verification for all process corners using detailed parasitic extractions of the metal interconnections including crosstalk effects between signal lines. In this thesis, the Synopsys PrimeTime® software has been used to perform the final sign-off STA verification.

4.5 Mixed Signal Back-End Design

For the back-end design of digital and mixed-signal systems, the Cadence Encounter Digital Implementation System has been used. This software provides a complete solution for the

Figure 4.12: Encounter Digital Implementation System design flow.

implementation of the gate-level netlist to a verified GDSII [3] stream for fabrication, including design exploration and feasibility analysis, floorplan synthesis, power routing and analysis, clock-tree synthesis, full-chip digital implementation, and sign-off verifications. The Encounter software also includes the RTL compiler for digital HDL synthesis, providing a complete tool chain from the RTL description to the final GDSII stream. The fast development of the semiconductor industry is reflected in the many features which have been successively added in this software, ranging from design-for-manufacturability, on-chip variation, yield-analysis and optimization tools, to 3-D Through-Silicon-Via (TSV) design support. A full list of the extensive tool capabilities can be found in the Encounter User Guide[65].

The design flow used in this thesis for the back-end implementation is shown in Figure 4.12. All operations are controlled by tool command language (Tcl) scripts. This allows to create a reproducible and automatic implementation flow from the gate-level netlist to the final chip layout. The results of the individual steps can be monitored by the generated log files. To control the build process, GNU makefiles[66] are used, based on the original design flow from Andreas Grübel[51]. The individual steps will be described in the following sections.

4.5.1 Data Preparation

The back-end tools require detailed informations about the fabrication process, the instantiated cells, and the design constraints for the correct physical implementation of the ASIC. The following data sets have to be available for Encounter prior to the back-end design process[65]:

- A technology file providing design rules for the placement and routing of cells, as well as detailed information about the metal interconnections, including metal resistance and line-to-line capacitances between metal layers for a parasitic RC extraction during the timing analysis of the design.
- Physical libraries containing abstract geometrical information of the instantiated logic cells and analog macros.
- Timing libraries for all standard cells, I/O pad cells, partitioned blocks and analog macros.
- Timing constraints of the design, describing the restrictions on the clock frequencies, signal timing and special logic timing paths. This file has to be consistent with the constraints used during the synthesis process of the digital front-end.

[3] The GDSII stream format is a database file format which has become the standard format for the exchange of IC layout artwork in the semiconductor industry.

- The synthesized gate-level netlist of the design.
- Input/Output (I/O) assignment file, which contains the positions and rules for the input/output pad cells of the chip. Usually, the exact positions of the pad cells are not fixed at the beginning of the design and will be changed iteratively during the floorplan of the design.
- Capacitance tables are used to provide accurate capacitance extraction results in the different process corners of the IC fabrication.
- The layout files of all instantiated cells, in order to merge the layouts into a single GDSII stream at the end of the design flow.

The technology file of the fabrication process and physical libraries are typically provided in a Library Exchange Format (LEF) database. The LEF file describes the physical information in a human readable ASCII format, containing the relevant data for physical implementation by the EDA tools and providing an abstract view of the instantiated cells. In this view, the information about the cell geometry, routing blockages on the individual metal layers, and the pin geometries are contained. Associated to the described pins is also information about the pin purpose, such as power, ground, analog, or signal pins, and the signal direction. Based on this information, the interconnections of signal lines to the cells are generated during the automatic routing step.

For the technology information of the chosen semiconductor process and the standard cell library, this information is already provided by the foundry and the distributor of the logic cells, respectively. The LEF database for custom analog macros has to be extracted from the analog layout. Cadence provides the *Abstract Generator* software to generate the required abstract from the layout view of the analog module and store it in the Library Exchange Format. The abstract generation process of the software is controlled by parameters described using the SKILL[67] scripting language. To achieve the desired routing to the analog macro and prevent metal blockages from interfering with the pin connection, the parameters of this process have to be adjusted for each individual analog block.

As described in Section 4.4, the timing libraries contain the informations required to calculate the timing behaviour of signal paths connected to the cell. Since the synthesis of the gate-level netlist, the physical implementation, and the sign-off timing analysis of the final design are all based on the signal timing described in these libraries, a correct definition of the timing library is mandatory. Errors generated due to a bad library or faulty constraints will neither be recognized during the physical implementation or the timing verifications.

4.5.2 Floorplan and Power Infrastructure

After the design has been imported into the Encounter software, the floorplan of the design can be started. In this step, the geometry of the chip die and the positions of the I/O pads for the electrical interconnection of the circuit to the outside world are defined. The analog

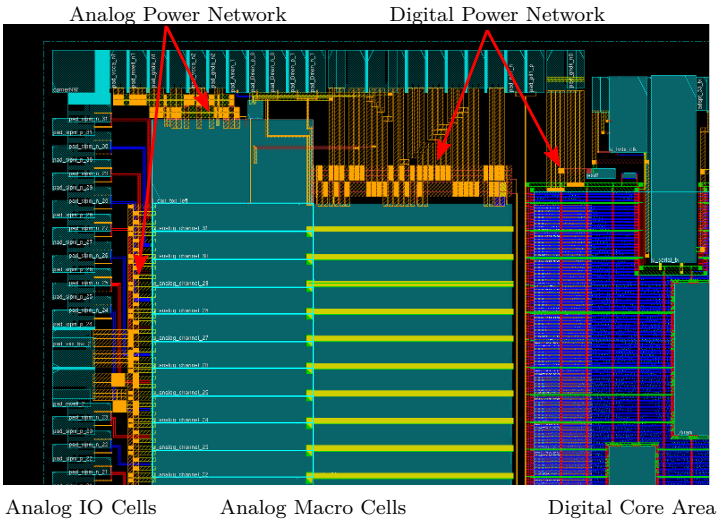


Figure 4.13: Part of the back-end design of the STiC ASIC after the floorplan step.

blocks instantiated in the netlist are then arranged on the available surface, and the areas for the standard cell placement are specified. Regions where individual sub-modules of the digital design are to be placed can also be defined in the floorplan. Critical analog signals, which are not connected to digital logic are already routed during this step. This routing is performed either manually, or by defining routing constraints for the signals and using special routing tools included in the Encounter software. The switching of digital signal lines can introduce noise to the sensitive analog circuits through capacitive coupling between digital and analog signal lines. Therefore, blockages are defined to prevent the routing of digital interconnections in the vicinity of analog modules and critical signal lines. The floorplan of the ASIC is typically developed iteratively to accommodate necessary changes during the subsequent stages in the design process.

After the floorplan of the chip has been defined, the power distribution network (PDN) has to be created to supply the analog and digital logic with power. Since the gate-level netlist only defines the signal interconnections, the power connections are specified in Encounter. To avoid the coupling of noise polluting the digital power supply to the analog modules, the power domains for analog and digital circuits have to be clearly separated.

The physical infrastructure of the PDN is created in a semi-automatic way. First, wide metal traces are manually created to predefine a general structure of the power distribution. For the standard cells, a power ring is created around the core areas defined in the floorplan. The structure of the analog power distribution has to be tailored to the needs of the macros, which can require a complete manual routing to the power pads of the analog cells. If the power connection from the I/O cells of the chip to the coarse power structures is not obvious, i.e. if it cannot be done with straight interconnections, the routing between to I/O cells and the PDN also has to be done manually. The remaining interconnections of the cell power pins to the power structures are then automatically routed by the EDA tool.

The width of the metal traces has to be sufficient to supply the current required by the

connected circuits. The maximal currents which can be sustained by the individual metal layers are specified by the semiconductor foundry. For digital circuits, the estimated power consumption can be extracted from the gate-level netlist and is usually reported during or after the synthesis process. To allow a more accurate estimate, a realistic switching activity of the storage elements in the digital logic, which consumes most of the power, can be extracted from digital simulations and supplied for the calculation of the power consumption. The analog power consumption is known from the full custom design of the circuit. If the delivered current is too large to be supported by the designed power distribution network, the metal traces will eventually break due to electromigration.

An example of the back-end design for the STiC ASIC after the floorplan step showing the arrangement of analog macro blocks, digital core area and power routing is given in Figure 4.13.

4.5.3 Design Placement and Routing

The implementation of the digital design consists of several phases. In the first step, the digital logic gates are placed in the standard cell areas defined in the floorplan. During the timing driven placement, the placement tools arrange the cells based on the specifications in the floorplan, their interconnections, and the design constraints. After the placement, a fast trial-routing of the design estimates the congestion of signal lines, which is the percentage of nets that could not be routed because the interconnection density in the area is too high. A bad trial route result requires an iterative rework of the floorplan to reduce the congestion. Before the next implementation step, a static timing analysis of the trial-routed design is carried out. Nets violating the maximum transition or maximum capacitance design rules are fixed at this point, and the setup slack of the timing paths is optimized.

The clock signals in a synchronous digital design have to drive many flip-flop clock pins simultaneously. As explained earlier, a buffer tree is therefore required to distribute the clock signal to the destination flip-flops. In modern nanometer designs, the clock-trees are generated automatically by algorithms which use the design constraints to create a balanced buffer tree, minimizing the skew between the signal at the endpoints. More sophisticated clock-tree algorithms also take the delays of the data paths into account. In this way, less buffer cells are required, reducing the power consumption of the digital circuit while still achieving the timing closure of the design. After the buffer-tree generation, the timing of the design is again optimized. In addition to the maximization of the setup slack, this process includes fixing hold time violations by adding additional logic buffers to the data paths.

The detailed signal routing of the metal interconnection between the cells is performed after the clock tree synthesis. The algorithms for the detailed routing of the design take the timing constraints into account and will iteratively improve the metal routing to achieve the timing closure of the design.

4.5.4 Finalizing the Design

In the last step of the back-end design, the remaining free space in the digital core area is filled up with filler cells to fix design rule violations of the production process. Since the fabrication also requires a defined metal density on the die surface, metal fillers can be added for the fabrication of the chip. If the fillers are not included during the back-end design, they will be added by the foundry before fabrication. Including the metal fill in the back-end design provides an accurate parasitic extraction for the timing verifications. The resistance and capacitance values from this sign-off RC extraction are written to a file in the standard parasitics exchange format (SPEF), which is used for the final timing verifications.

The design is exported to a GDSII stream by merging the layouts of all instantiated cells into a single output stream, which is used for the final physical verification and the production by the foundry.

4.5.5 Design Verification

The design has to pass several physical and timing verifications, which ensure that the chip can be produced without errors, and that the digital design can operate at the rated frequencies.

Physical Verifications

The physical verification of the design encompasses three separate design tests, namely design rule checking (DRC), antenna violation checks and layout versus schematic (LVS) verification.

Design rules are specified by the semiconductor foundry and contain geometric and connectivity restrictions to the layout in order to provide sufficient margin for fluctuations in the fabrication process. If the design rules are violated, the layout will not be accepted by the foundry since it cannot be produced.

During the fabrication process, the metal interconnections are produced layer by layer. Although in the final design a signal net will consist of a cell driving the net and a receiver, long metal traces connected to isolated transistor gates can exists during the layered manufacturing process. Such terminals are termed *antennas* and can accumulate electric charge during the fabrication, which has no electrical path to discharge. The voltage at the gate dielectric can thus exceed the normal operating voltage of the device and cause plasma induced gate oxide damage to the transistors. This effect can be avoided by adding diodes to the signal line, providing a discharge path, or by switching between metal layers to reduce the length of the metal trace connected to the isolated gate.

To ensure that the physical layout of the GDSII stream matches the described mixed-signal design, a LVS check has to be performed. For this comparison, the SPICE netlist of the physical layout is extracted from the GDSII stream. The corresponding circuit description only exist as a Verilog netlist, which defines the interconnections between the modules. This netlist can be directly converted to the SPICE syntax, while the transistor level information of the circuits are added to this source by include statements, referencing the SPICE netlists of

all instantiated cells, including analog macros, digital standard cells, as well as I/O and power pads. The global power net names are appended and the ground nets, which are shorted in the physical layout by the semiconductor substrate, are virtually connected in the source netlist. The source and layout netlists are then compared and discrepancies between circuit description and physical layout are reported.

During the design of the STiC ASIC the Mentor Graphics software Calibre has been used to perform all physical verifications.

Timing Verification

The final design has to achieve timing closure, i.e. it has to satisfy the specified timing constraints. To achieve this goal, the design has to be verified by a static timing analysis as described in Section 4.4, and pass a backannotated simulation using a testbench.

For the sign-off STA of STiC, the Synopsys PrimeTime® software has been used. It uses the detailed RC extraction of the physical layout for the signal delay calculations. In this analysis, also higher order effects affecting the signal delay like cross-talk from capacitive couplings between signal nets are taken into account. The analysis has to be performed for all available process corners to ensure that variations in the fabrication process do not lead to timing errors in the design.

As already mentioned in the previous section, the propagation delays for every signal path from the driving cell to the endpoints of the logic path are calculated during the timing analysis and can be exported to a standard delay format (SDF) file. This delay information is introduced into the gate-level netlist of the circuit for a backannotated timing simulation. This allows to verify the functional as well as timing behaviour of the final circuit.

The critical interface between the analog modules and the digital circuit of a mixed-signal design requires a manual verification. A full-scale analog simulation of the complete circuit at the transistor level is too time consuming and only feasible for small designs. The EDA tools therefore provide the possibility to perform mixed-signal simulations. The interface between the analog and digital parts is in this simulation specified by voltage thresholds, which determine the analog-to digital conversion for the translation of analog signals to the digital domain. Similarly, the digital signals are characterized by their rise and fall time and introduced to the analog simulation. In this way, only the circuits of the analog modules require detailed SPICE simulations, and the full mixed-signal design can be simulated.

After the design has passed all sign-off verification procedures, the layout is submitted to the foundry for production.

Chapter 5

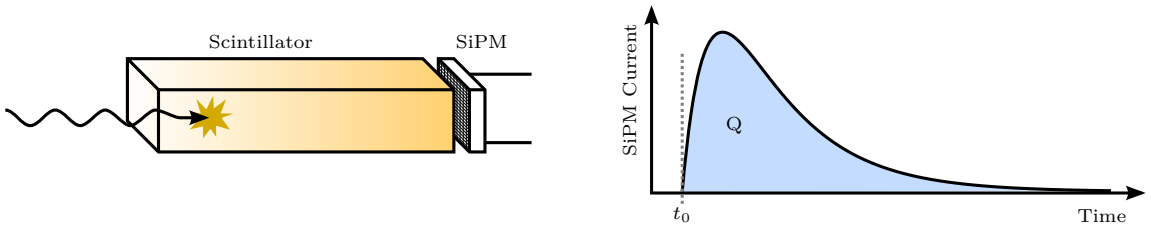
STiC Design Concept

The focus of the STiC development is to achieve the high timing resolution required by Time-of-Flight applications. Three generations of the STiC ASIC family have been developed so far. The first version was produced in 2009 using the AMS 0.35 μm CMOS technology [68]. This prototype chip consists of four analog readout channels, which were used as a concept study to investigate the performance of the input stage readout structure and the different discrimination methods. In the framework of the EndoTOFPET-US project, the characterization results of this chip have been used in the development of the next ASIC generations. The second STiC version implements 16 SiPM readout channels in a mixed-signal ASIC, which has been developed in the UMC 0.18 μm CMOS process. The analog input stages in this chip have been complemented with a precise Time-to-Digital Converter (TDC) to measure the signal timing, and a digital control logic. The features and interfaces of the digital logic have been developed according to the specifications of the EndoTOFPET-US DAQ system and provide a Serial Peripheral Interface (SPI) for the chip configuration and a 160 MBit/s serial link to transmit the event data to the DAQ system. After detailed characterization studies of this prototype [69, 70], the 64 channel version of STiC has been developed, which is currently being commissioned in the outer plate of the EndoTOFPET-US project.

Although both mixed-signal versions of the chip were developed as part of this thesis, only the design of the latest STiC generation will be described. In this chapter, the design concept of the readout ASIC will be presented. After the description of the signal processing methods for the readout of SiPM signals, the features of the implemented analog input stage are presented. The integrated TDC module has been developed at ZITI Heidelberg and is also used in the PETA ASICs [71]. This module will be introduced in Section 5.2.2. The last sections will cover the signal processing in the digital control logic and the back-end ASIC design of STiC.

5.1 Signal Processing Methodology

For the design of high precision readout electronics, not only the electrical properties of the sensor device are relevant, but also the physical processes contributing to the signal formation have to be taken into account. A typical scintillation detector module using Silicon Photomultipliers is shown in Figure 5.1a. When traversing the scintillator, a particle looses energy by excitation of the atoms or molecules of the material. During the de-excitation of these states, low energetic photons in the visible region are emitted isotropically. The number



(a) Particle detector module consiting of a scintillator coupled to a SiPM.

(b) SiPM current output pulse of a detected particle. The charge Q of the signal corresponds to the particle energy deposited in the scintillator.

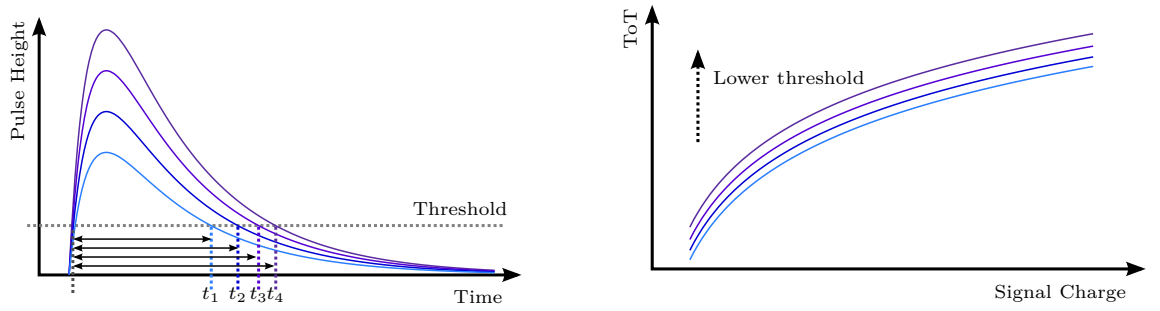
Figure 5.1: Response of a detector module used for particle detection.

of generated scintillation photons is proportional to the energy deposited in the material by the particle. The correlation between the average number of generated photons and the deposited energy is specified by the light-yield of the scintillator material. For the readout of the generated photons, the light is collected on a SiPM coupled to the surface of the scintillator. The number of photons reaching the sensor depends on the quality of the optical coupling to the scintillator and the light collection efficiency. The collection efficiency is usually improved by enclosing the scintillator surface in a reflecting material. The photons reaching the SiPM surface are detected in the individual pixels of the sensor, as described in Chapter 3. The resulting output current pulse of the SiPM is illustrated in Figure 5.1b. Since the number of generated scintillation photons depends on the particle energy, so does the number of fired SiPM pixels. The charge of the generated current pulse is consequently correlated to the energy loss of the particle in the scintillator. In addition to the energy information from the signal, Time-of-Flight experiments require a high precision measurement of the time of arrival t_0 of the particle for the event reconstruction.

5.1.1 Charge Measurement Methods

In order to measure the energy of a detected particle, the charge information has to be extracted from the signal. Depending on the required signal-to-noise ratio, resolution, and the constraints of the detector system, different methods can be used for this measurement, the most straightforward being the digitization of the signal waveform. Using oscilloscopes or special readout electronics such as the DRS chip [72], the full output signal of the SiPM can be digitized and the charge calculated offline by integrating the waveform over time. Sophisticated waveform analyses of the recorded output signals can provide very accurate measurements, but for large systems comprised of thousands of readout channels, the amount of recorded data and the power consumption of the readout electronics makes this solution not feasible.

Another method is the integration of the signal charge on a capacitor using charge sensitive preamplifiers. The amplitude of the generated output pulse is proportional to the charge, and can be digitized by a peak-sensing Analog-to-Digital Converter (ADC). Many charge sensitive



(a) ToT measurement for charge determination.

(b) Non-linear response of the ToT method calculated for different thresholds.

Figure 5.2: Illustration of the Time over Threshold method to determine the charge of a SiPM signal.

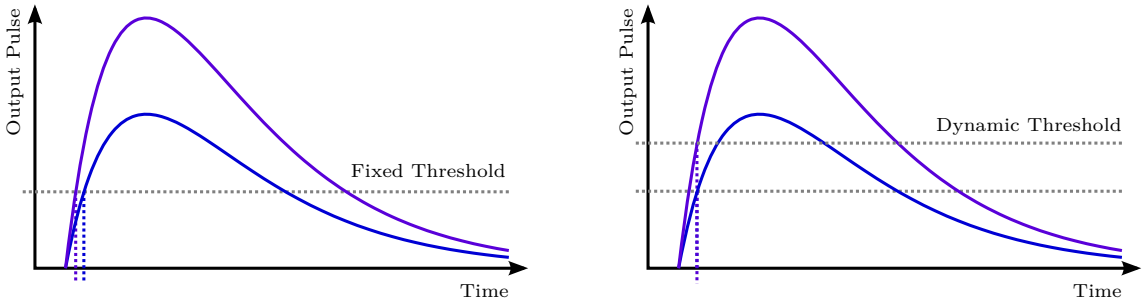
preamplifier circuits already exist for the readout of PIN diodes and avalanche photodiodes, but due to the significantly larger detector capacitance, these solutions are not suited for the readout of SiPMs, due to the low signal-to-noise ratio. Therefore, special electronic readout circuits with a low input impedance have to be developed [73–75], which provide a sufficient SNR to measure single photon spectra with even low gain sensors.

A less accurate method for the measurement of the signal charge is the Time over Threshold (ToT) measurement. In this method the charge is evaluated by measuring the time during which the signal stays over a defined threshold. This ToT method is illustrated in Figure 5.2a. The pulse width of the signal after discrimination increases with the signal charge. However, due to the pulse shape of the current signal, the response of the ToT to the signal charge is not linear. The exponential decay of the SiPM signal results in a logarithmic dependence of the pulse width to the signal charge as it is shown in Figure 5.2b for different discrimination thresholds. In applications where a high energy resolution is not mandatory, the possibility to determine the energy with a time measurement eliminates the necessity to implement both, an ADC and a TDC module in an ASIC. In this way, the complexity, size and power consumption of the readout channels can be reduced.

The design of STiC makes use of the integrated high precision Time-to-Digital Converter for time measurements, by implementing a linearized form of the ToT, which provides an improved energy resolution compared to conventional ToT methods. The pulse width of the signal is encoded by the analog signal processing together with the arrival time in a common output signal. A single TDC channel is therefore sufficient to measure both, incident time and energy of the particle, which will be described in Section 5.1.3.

5.1.2 Time Measurement Methods

The arrival time of the incident particles is measured by discriminating the current pulse of the SiPM at a defined threshold level. As already described in Section 3.2, the precision of the generated time trigger signal is limited by the time jitter of the signal, as well as the time walk effect. To reduce the influence of the time jitter, the noise performance of the analog



(a) Leading-Edge triggering. **(b)** Constant-Fraction triggering.

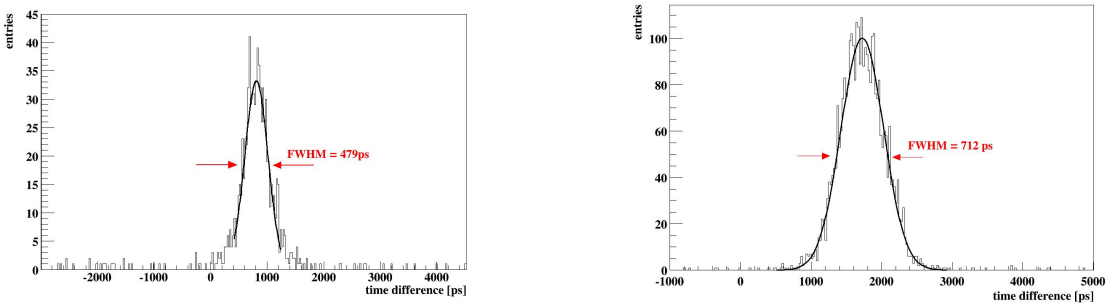
Figure 5.3: Discrimination methods used for precise time triggering.

circuits and the input impedance of the input stage have to be optimized. In contrast to the jitter originating from statistical noise sources, the time walk is systematical and can be corrected by special discrimination methods or by offline corrections using the known charge of the signal.

The two main principles used for the generation of the high precision trigger signals are graphically shown in Figure 5.3. The leading edge (LE) discrimination uses a fixed threshold level to which the input signal is compared. The point at which the input signal crosses this threshold defines the trigger point. The error of the time walk effect when using leading edge discrimination depends on the threshold level and is smaller for low thresholds and fast signal rise-times. In addition to the time walk, also the statistical distribution of arrival time of the scintillation photons at the SiPM surface affects the signal timing. By triggering on the signal generated by the first detected scintillation photons, the timing resolution is improved [25]. For an accurate measurement of the trigger time, the threshold therefore has to be chosen as low as possible.

Assuming a constant rise time of the input signal from the sensor, the time walk effect can be cancelled out by using a dynamic threshold, which discriminates the signal at a constant fraction of the amplitude. This method is shown in Figure 5.3b for a threshold level at 50 % of the signal amplitude. Constant-fraction (CF) discriminators typically use a pulse shaping of the input signal to create a bipolar output pulse for the discrimination, which crosses the electrical zero-point at a fixed time, independent of the signal amplitude.

Both methods have been implemented in the first version of the STiC ASIC and the Coincidence Time Resolution (CTR), which is important for Time-of-Flight measurements, has been evaluated [68]. The measurements show that the fluctuations in the signal rise-time due to the photon statistics of the scintillation process ultimately deteriorate the resolution of the CF discrimination method. Without a prior signal shaping to ensure a constant rise-time, the CF method therefore yields worse results than a LE signal discrimination. The measurements with the first STiC generation are shown in Figure 5.4 and yield a CTR resolution of 479 ps and 712 ps FWHM for the LE and CF methods, respectively. In the later STiC versions, the constant fraction method has been dropped in favour of the leading edge



(a) CTR with leading edge discrimination.

(b) CTR with constant fraction discrimination.

Figure 5.4: CTR measured with STiC1 for the different discrimination methods [68].

discrimination. In the LE measurements, the time walk effect is then corrected by the known charge information of the signal.

5.1.3 Time and Charge Measurements with STiC

The STiC ASIC uses two separate discrimination paths with individual thresholds to extract the time and charge information from the SiPM current pulse. Both thresholds can be tuned in a certain range to achieve the best timing and charge resolution. The generated trigger signals from the two discrimination paths are in this thesis also referenced to as T-Trigger and E-Trigger.

A low threshold leading edge discriminator has been chosen to generate the high precision T-Trigger signals marking the arrival time of the incident particles. The threshold of this discrimination stage has been designed to be configurable in a range below a single pixel signal to multi-pixel signals.

The charge is determined in the second discrimination path using the previously explained Time over Threshold method. Due to the non-linearity of this method, the ToT measurement with the time trigger path would yield a poor resolution for larger signals, and a higher threshold is required to generate the E-Trigger signal. As will be explained later, the STiC ASIC implements a linearized Time over Threshold method, which significantly improves the resolution of the charge measurement. By requesting a valid E-Trigger signal for each recorded event, only events with sufficient energy will be recorded for the later data analysis. This condition is used to filter out unwanted events, such as dark-noise pulses from the SiPM.

5.2 STiC3 Architecture

The architecture of STiC3 is presented as a block diagram in Figure 5.5. The current signal of the SiPM is processed by the analog input stage to generate the required time and energy trigger signals. To measure both discrimination signals in a single TDC channel, the information is encoded into a single trigger output by the Hit Logic unit. The input stage also allows to

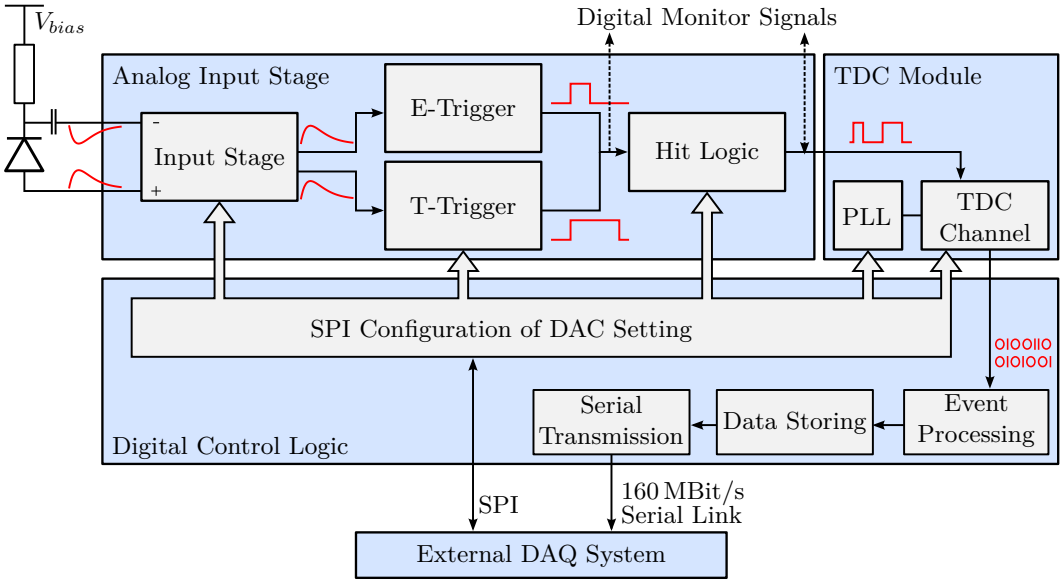


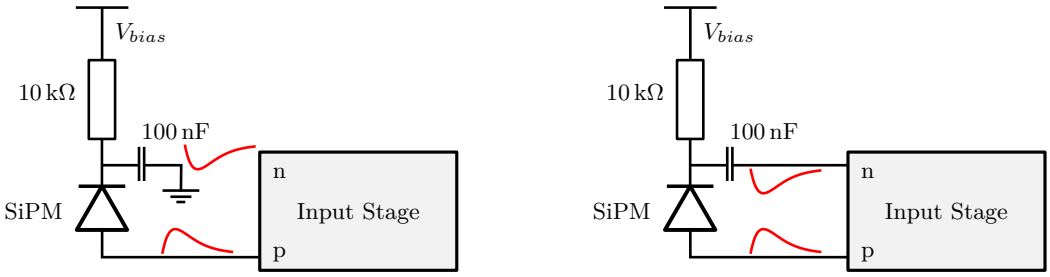
Figure 5.5: Overview of the dataflow for a single readout channel of STiC3

control the sensor bias voltage by tuning the potential at the input terminals. The generated output trigger signal is measured by a high precision TDC module with a time binning of 50 ps. For each event, two timestamps are recorded which together contain the arrival time and charge information of the SiPM signal. In the digital control logic, the two timestamps are grouped into events which are then processed and stored in an internal First In - First Out (FIFO) buffers. The interfaces of the ASIC have been designed in accordance with the specifications of the EndoTOFPET-US DAQ system. Every 6.4 μs, the recorded events are read from the FIFO and packed in data frames using 8b/10b bit encoding which are transferred over a 160 MBit/s serial link to the DAQ system. The functionality of the chip, including the settings of the analog input stage and the TDC module, is configured using a Serial Peripheral Interface.

With each generation, the analog readout structure of STiC has been optimized to ultimately provide a Coincidence Time Resolution of 200 ps FWHM required by the EndoTOFPET-US project. The electronic circuits have been developed by Wei Shen and are described for the first STiC versions in [49, 68, 69]. The signal processing chain implemented in the last version of STiC will be described in this section.

5.2.1 Analog Signal Processing

The analog input stage has to process the current pulses generated by the SiPM sensor to extract the time of arrival and the charge information as individual trigger signals, using the previously described methods. To achieve the required precision of the time measurement, the signal processing makes use of a fully differential design to reject common mode noise from external sources, as well as the integrated TDC and digital circuits.



(a) Single-ended SiPM connection. **(b)** Differential SiPM connection.

Figure 5.6: Different SiPM readout schemes possible with the STiC ASIC.

Input Stage

The differential design offers two possible connection schemes for the readout of a Silicon Photomultiplier, which are shown in Figure 5.6. In the single-ended mode, the positive terminal of the channel is connected to the anode of the sensor while the negative terminal is left floating. The cathode of the sensor is in this case connected over 100 nF to ground. In the differential readout scheme, the sensor signal at the cathode is AC coupled over the capacitor to the negative input terminal. Although the additional capacitance at the input terminal due to the differential connection increases the statistical noise in the readout chain, the benefits of the common mode noise rejection from the differential signal connection ultimately improve the timing performance of the circuit.

In the ASIC, the input terminals are connected to a symmetrical readout structure with identical circuits for the negative and positive signal path. One half of the circuit is shown as a schematic diagram in Figure 5.7. The analog input stage uses a common gate amplifier stage to provide a high bandwidth and low input impedance for the readout of the charge pulse from the SiPM. The input transistor M1 in this circuit is biased by a constant current source generating the current I_{bias}, which can be controlled by a DAC parameter from the digital control logic. As has been calculated in section 3.2, the impedance of the readout electronics has to be as low as possible to increase the slope of the current pulse and thereby reduce the error from the time jitter effect. The input impedance R_{in} of the common gate amplifier stage is determined by the transconductance of the input transistor

$$\mathrm{R}_{in} = \frac{1}{g_{m,1}}\,, \tag{5.1}$$

with

$$g_m = \frac{2I_d}{V_{gs} - V_{th}} \tag{5.2}$$

if M1 is in the saturation region and the body effect of the transistor is neglected. V_{gs} denotes the voltage difference between the gate and source terminals of the transistor and V_{th} the threshold voltage of the transistor. Since $g_{m,1}$ increases with the current through the transistor, the input impedance can be reduced by increasing I_{bias}. In this way, an input impedance of

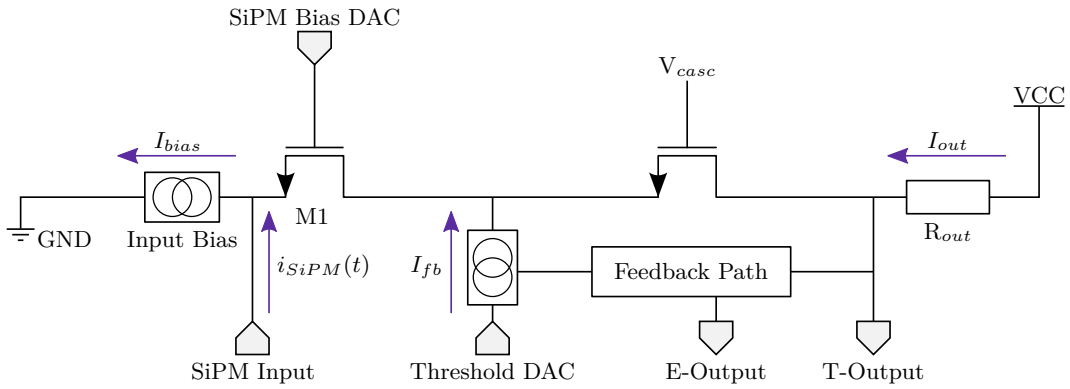


Figure 5.7: Schematic diagram of one half of the differential input stage.

less than 50 Ω can be achieved.

The gate voltage of the input transistor is also controlled by a DAC parameter of the chip configuration to provide the required bias tuning of the SiPM sensor. In the saturation region, the current I_{M1} through the input transistor is proportional to

$$I_{M1} \propto (V_{gs} - V_{th})^2 \ . \tag{5.3}$$

For a fixed bias current I_{bias} the voltage difference between the gate and source terminal of the input transistor is therefore defined and has to be constant. The voltage at the source terminal has to follow the change in the gate voltage to keep V_{gs} constant. In this way, the DAC voltage setting at the gate of M1 can tune the input terminal voltage in a range of more than 0.5 V.

The DC voltage at the output terminal is given by the current I_{out} through the load resistor R_{load} with

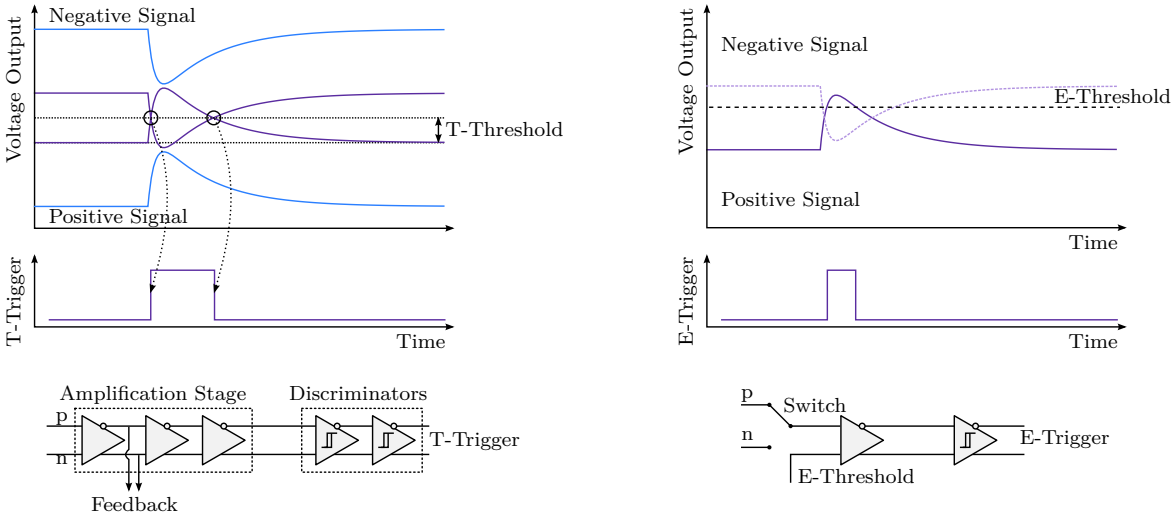
$$V_{out} = \mathrm{VCC} - I_{out} \cdot R_{load} = \mathrm{VCC} - (I_{bias} - I_{fb}) \cdot \mathrm{R}_{out} \tag{5.4}$$

The DC voltage at the output is stabilized by a low frequency feedback from the timing output path, which introduces an additional current I_{fb} at the drain of the input transistor M1. The feedback current I_{fb} is in addition controlled by a DAC setting, which is used to tune the DC level at the output terminal and thereby the trigger threshold for the time discriminator circuit, as will be explained later.

The additional current signal from the SiPM $i_{SiPM}(t)$ is mirrored in the current I_{out} through the load resistor. The signal at the output terminal is then given by

$$v_{out}(t) = \mathrm{VCC} - (I_{bias} - I_{fb} - i_{SiPM}(t)) \cdot \mathrm{R}_{out} \tag{5.5}$$

and has the same polarity as the current signal at the input. To provide a sufficiently high output impedance, a cascode transistor is introduced to boost the output impedance of input stage. An illustration of the signal output for the positive and negative signal paths during



(a) T-Trigger generation.

(b) E-Trigger generation.

Figure 5.8: Analog signals in the discrimination paths of the STiC3 ASIC.

a SiPM signal is shown in Figure 5.8a. The second signal copy for the charge evaluation is generated in the feedback path. The tuning of the feedback current to define the T-Trigger threshold will consequently affect also the behaviour of the E-Trigger path.

Time Trigger

For generation of the precise time trigger signal, the difference in the output signals of the analog input stage is first amplified by three subsequent high bandwidth differential amplification stages. The output of the first amplification stage is also used for the feedback path to the input stage. The comparator circuit generating the trigger signal is designed as a positive feedback loop, which provides an intrinsic hysteresis for the discrimination process. The hysteresis is important to suppress multiple triggering on noise especially during the slow decay of the SiPM signal.

If the DC voltage points of the output signals are closer to the common-mode voltage, the amplitude of the SiPM signal require to create a trigger signal is smaller, as it is shown in the Figure 5.8a. By tuning the feedback current in the input stage with the Threshold DAC setting, the voltage difference between the positive and negative output signal of the input stage can be controlled, which corresponds to a change in the trigger threshold.

Energy Trigger

In contrast to the T-Trigger generation, the energy discriminator uses only the positive or negative part of the differential output signal from the input stage. Which part of the signal is used for the discrimination can be chosen by the setting of a switch. The comparator circuit generating the energy trigger is shown in Figure 5.8b. The input signal is compared

to a threshold voltage, which can be tuned by a DAC setting. Both, the switch selecting the positive or negative signal path and the threshold voltage are configured by the digital control logic. Since the threshold setting of the time trigger influences the DC values of the input signal paths, it also affects the relative discrimination threshold of the E-Trigger. For a higher T-threshold, the effective threshold for the energy discrimination is also increased. As a consequence, the E-Trigger has to be adjusted for each setting of the T-Trigger threshold.

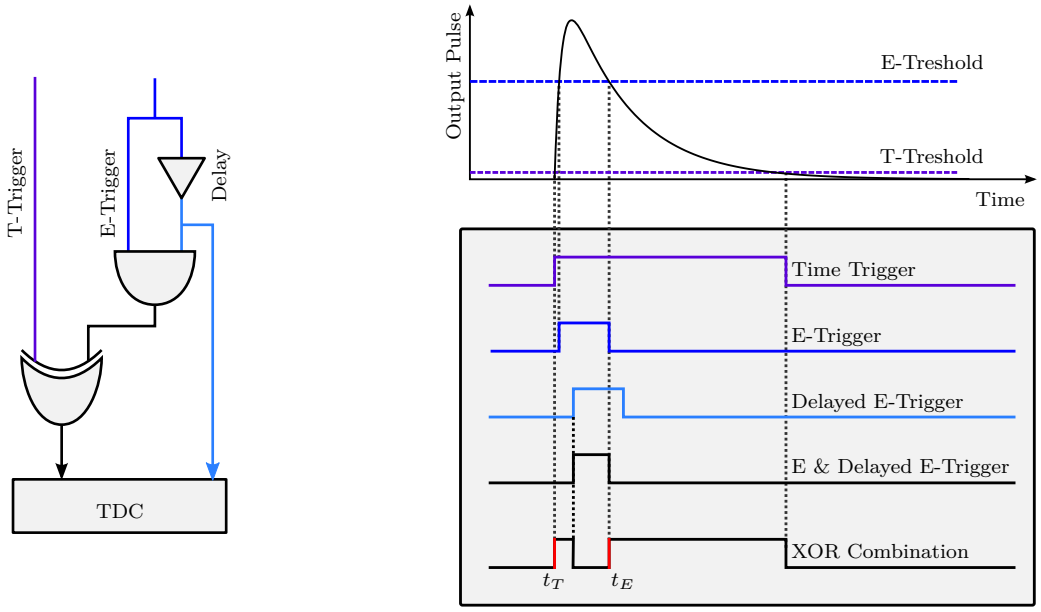
As was already mentioned, the STiC3 ASIC implements a linearized Time-over-Threshold method for the charge measurement. This linearization is achieved by integrating the current of large SiPM signals on the detector capacitance itself. For signals with sufficient charge, the bias current I_{bias} in the positive signal path of the analog input stage is completely supplied by the SiPM, and no current flows through the input transistor. While the charge collected on the detector capacitance is discharged, the input stage is turned off and the voltage at the positive output terminal equals to VCC. As a results, the E-Trigger will stay active during this time and the measured Time over Threshold is the time it takes to discharge the SiPM detector capacitance with the constant current I_{bias}.

Hit-Logic

In order to measure the time and energy information in a common TDC channel, the two distinct trigger signals have to be merged into a single output signal, which contains the processed timing and charge information of the SiPM current pulse. Due to the differential structure of the discriminator circuits, the output trigger signals intrinsically meet the differential Current Mode Logic (CML) standard, which is also used in the design of the TDC module. Digital CML logic gates are therefore used to implement the required logic for the signal processing. A simplified schematic of the logic circuit and the signals in the corresponding processing stages are shown in Figure 5.9.

Because of the fast rise time of the SiPM signal, the Time over Threshold of the current pulse can also be evaluated by the time difference between the rising edge of the T-Trigger and the falling edge of the E-Trigger output without significantly affecting the accuracy of the measurement. Since the TDC channel only records to the rising edges of the trigger signal, the time and pulse width of the event have to be combined into a trigger signal with two separate rising edges. This can be achieved by an XOR combination of the two trigger signals. The result of this logic operation are two successive pulses starting at the rising edge of the T-Trigger and the falling edge of the E-Trigger, respectively. However, to ensure a minimal width of the first pulse, the rising edge of the E-Trigger has to be delayed before it can be combined with the T-Trigger signal. For this purpose, a delayed copy of the E-Trigger is combined with the original signal by a logic AND gate, delaying the rising edge, but maintaining the timing of the falling edge of the signal.

The edges of the final trigger output pulse which are digitized by the TDC module are highlighted in Figure 5.9b. The state of the delayed energy signal is stored together with the timestamp to distinguish between the digitized edges originating from time and energy



(a) Trigger merging in the Hit-Logic.

(b) Signal waveforms during the trigger merging.

Figure 5.9: Signal readout methodology implemented in STiC.

discriminations. For the timestamps corresponding to the falling edge of the E-Trigger, this recorded signal will always be high.

Analog Channel Debug Monitors

For the functionality and performance characterization of the chip, each analog readout channel can be configured to connect relevant signals to dedicated pads of the chip for monitoring. These debug monitors comprise two differential digital outputs and one analog signal output. With the analog monitor output it is possible to observe the analog signal after the input stage and at the amplification stages in the time and energy discrimination paths.

The digital monitor pads provide access to the T- and E-Trigger signals after the discrimination process, and the corresponding output signals after the XOR combination by the Hit Logic unit. With these signals, it is possible to measure the performance of the analog processing without the influence of the digitization process. In addition to monitoring the trigger signals, the digital monitor pads can also be used to directly access the input terminals of the TDC channel. This allows to inject an external trigger signal for measurements with the TDC and characterize its functionality and performance individually.

5.2.2 Time-to-Digital Converter

Many different TDC architectures exist, which can provide the required picosecond time resolution to digitize the trigger signals generated by the analog input stage. A review of the most commonly used methods has been published in [76].

In order to measure the absolute timing of a single event, the TDC architectures rely on a combination of a coarse and fine counters to achieve the picosecond resolution in a large measurement range. The coarse counter subdivides the time range in bins of typically several nano-seconds by a low frequency clock. The slow frequency allows to implement this stage as a simple counter module covering a long measurement range. The fine counter is used to interpolate the arrival time of the event within a coarse counter bin with a high precision in the order of picoseconds.

The different fine counter implementations can be roughly classified as analog and digital time interpolation methods. Analog time interpolations use the charging and discharging of a capacitor or similar slow analog processes with a subsequent digitization step to achieve the high timing resolution, whereas digital methods rely on the propagation time of a digital signal through logic gates. In order to evaluate the different implementations, several key characteristics of a TDC have to be considered, such as the time resolution, the dead time and possible readout speed, the power consumption, and the ease of use.

The design of analog fine counters can achieve high time resolutions with a low power consumption. Their implementation in integrated circuits is however more susceptible to the ambient temperature, variations in the fabrication process, and other external influences, which requires complex calibrations to achieve the desired resolution. In addition, the conversion time of a measurement required by the analog interpolation methods is longer compared to digital fine counters, which results in a longer dead time of the TDC.

The integrated Time-to-Digital Converter in the STiC3 chip has been developed at the ZITI[1] Heidelberg and uses a digital interpolation method based on a Phase Locked Loop (PLL). The module is functionally separated in the Timebase and TDC channels, which have been designed using the differential Current Mode Logic standard. In the global Timebase unit, the coarse and fine counter time values are generated and distributed as a timestamp to several TDC channels. Each TDC channel contains fast latches to store the current timestamp value upon a signal at its trigger input terminal. The principle of operation of these two units is presented below to understand the time information and the subsequent processing thereof by the STiC3 ASIC. A detailed description and analysis of this TDC module is presented in [77].

Timebase Unit

A block diagram of the Timebase unit is shown in Figure 5.10. The core of the unit is a Voltage Controlled Oscillator (VCO) consisting of 16 delay elements. The propagation delay τ_d of the delay cells can be tuned by a reference voltage, which is controlled by the PLL circuit. The logic signal propagating through the cells is inverted after $16 \cdot \tau_d$ in the last element and fed back to the first delay cell. In this way, the VCO creates a coarse counter clock with a period of $2 \cdot 16\tau_d$, and the state of the delay cells provides the fine-time interpolation by subdividing the VCO clock in the 32 possible states of the oscillator.

The period of the VCO clock has to be locked to a stable reference clock to prevent

[1] Zentrales Institut für Technische Informatik

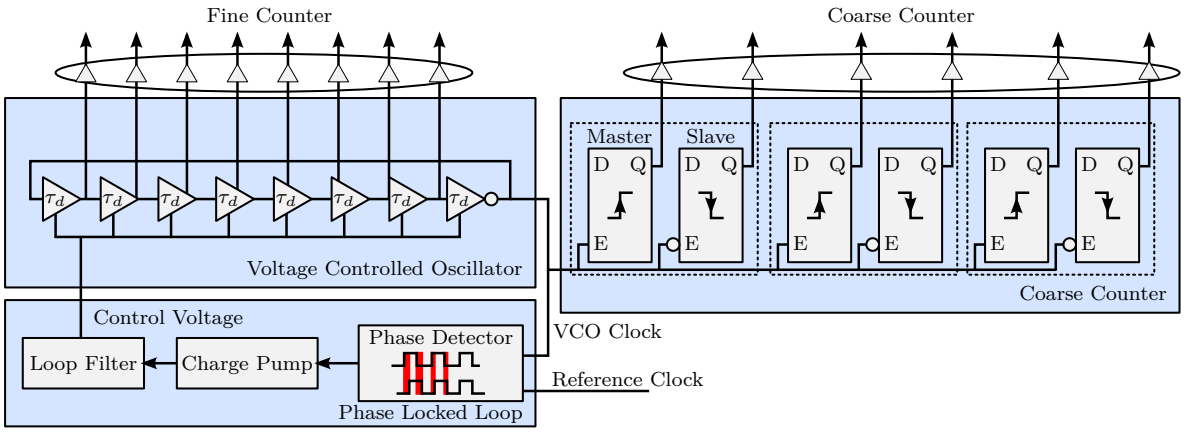


Figure 5.10: Block diagram of the Timebase unit. The VCO and coarse counter latches are shortened in the illustration.

variations in the clock frequency due to power, voltage or temperature variations. This also allows to synchronize multiple PLLs to an external reference clock, providing a common time reference for different ASICs. To match the VCO frequency to the reference clock, a phase detector unit evaluates the phase difference of the two clocks and creates a control signal which determines whether the delay of the VCO elements has to be increased or decreased. This control signal is interpreted by a charge pump to charge or discharge a capacitor unit in the loop filter, effectively changing the control voltage and thereby the speed of the delay elements in the desired direction. The whole chain of VCO, phase detector, charge pump and loop filter is referenced to as the Phase Locked Loop. After an initial locking period, the frequency of the VCO equals that of the reference clock and the PLL is locked. As long as the reference signal is stable, deviations of the VCO frequency from the reference will be automatically corrected by the feedback loop. In order to monitor the VCO clock, the Timebase unit contains a separate VCO output which is connected to an analog IO pad of the chip. The monitor can be enabled by a bit in the chip configuration and allows to measure the oscillation frequency and jitter of the VCO.

The PLL has been designed to lock on a frequency in the range of $f_{ref} = 625\,\mathrm{MHz}$. The average delay of the VCO cells in the locked state is then

$$\langle \tau_d \rangle = \frac{1}{32 \cdot 625\,\mathrm{MHz}} = 50\,\mathrm{ps}\,. \tag{5.6}$$

In the ideal case of a uniform cell delay, the resulting resolution with this time binning is

$$\frac{50\,\mathrm{ps}}{\sqrt{12}} = 14.43\,\mathrm{ps}\,. \tag{5.7}$$

Although the average delay is fixed by the Phase Locked Loop, the individual delays of the cells vary due to differences in the physical layout, the interconnection of the cells and fluctuations in the fabrication process. In addition, the cell delay can be different for the propagation of

rising ($0 \rightarrow 1$) and falling($1 \rightarrow 0$) logic transitions. The errors in the fine-time measurements that arise from the variations in the cell delays are characterized by the differential and integral non-linearity of the fine counter. The differential non-linearity (DNL) of a fine counter bin is defined as the relative deviation of the cell delay τ_i from the average delay:

$$DNL_i = \frac{\tau_i - \langle \tau_d \rangle}{\langle \tau_d \rangle} \tag{5.8}$$

The integral non-linearity (INL) value of a cell is its total deviation from the correct fine time value and can be obtained by the summation of the DNL values of all cells prior to the investigated cell.

$$INL_i = \sum_{j=1}^{i} DNL_i \tag{5.9}$$

The DNL and INL are typically expressed in least significant bits (LSBs), which is the smallest quantization step of the digitization process. As with the analog input stage, the bias currents of the PLL can be controlled by Digital-to-Analog converters, which allows to achieve DNL values of $< 1\,\text{LSB}$. By measuring the true delay values of the fine counter elements the remaining non-linearities can be corrected offline to further improve the timing resolution of the TDC module.

The coarse counter of the Timebase unit is driven by the VCO clock output. It is implemented as a 15-bit linear feedback shift register (LFSR). The LFSR runs through a repetitive sequence of $2^{15} - 1$ binary states. To get a successive numbering of the counter states, each state is mapped to its sequence number in a later data processing stage. In the short time interval during which the next counter value is stored in the registers, the output values of the corresponding register stage are unstable. The Timebase therefore uses two stages to always provide a stable counter value. These registers are called *Master* and *Slave* registers and are incremented at the rising and falling edge of the VCO clock signal, respectively. By recording both, the Master and Slave registers for each trigger signal, it is guaranteed that at least one of the two stages contains a stable counter value. The selection of the Master or Slave coarse counter for the event is performed later in the digital signal processing based on the fine counter value of the timestamp. The coarse counter values are reset to an initial value by a reset signal from the digital core logic. This reset signal is used to synchronize multiple TDCs to a common reference time point.

The full timestamp generated by the PLL and distributed to the TDC channels consists of 16 bits describing the stage of the VCO, and 30 bits of the coarse counter Master and Slave registers.

TDC Channel

The TDC channel units store the states of the fine and coarse counters of the Timebase upon a hit signal from the analog input stage in fast latches. The block diagram of this unit is shown in Figure 5.11. As already described in the previous section, the energy flag output

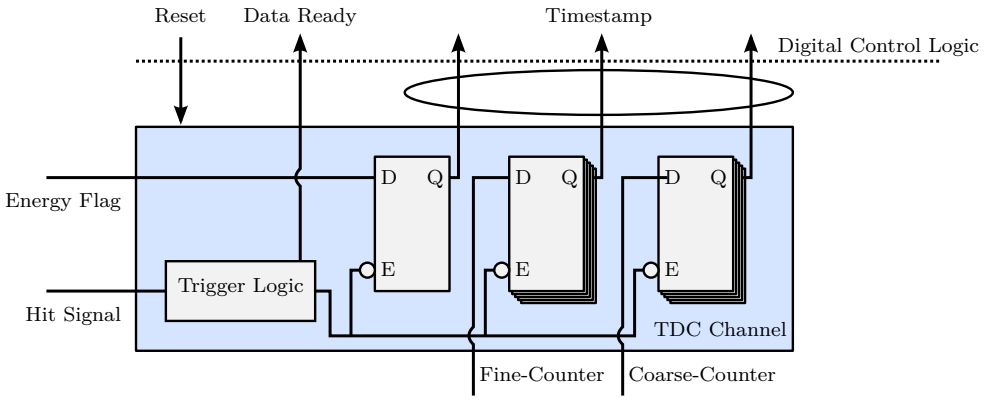


Figure 5.11: Block diagram of the TDC channel unit.

signal is also recorded with the timestamp to distinguish between the T-Trigger and E-Trigger signals. The TDC architecture is designed using the differential CML logic. The output values of the latches therefore have to be converted to standard CMOS levels to interface with the standard cell logic. The trigger logic of the channel generates for each new recorded timestamp a *Data Ready* signal. The digital control monitors this signal and records the data of each timestamp before issuing a reset of the channel data. Upon receiving the reset signal, the Data Ready signal and the latches are cleared and after a short recovery time of around $\sim 30\,\text{ns}$, the channel is ready to record the next trigger signal. Because of the additional energy flag, the width of the recorded timestamp data is increased to 47 bits.

5.2.3 Digital Control Logic

The digital control logic is responsible for the processing of the generated TDC data, the storing and transmission of event data to the data acquisition system, as well as providing a communication interface for the chip configuration. A diagram of the individual blocks and their interconnection is shown in Figure 5.12. The most important steps of the event data processing in the individual modules will be described in the next sections.

TDC Hit Receivers

The digital core logic arranges the 64 readout channels in four groups. The recorded timestamps of each TDC channel are handled by a dedicated Hit Receiver module. In this module, the timestamps belonging to a physical event are grouped together to form the event data. The signal processing of the TDC data during the recording of an event is illustrated in Figure 5.13. The time and energy information belonging to a physical event are provided by the TDC channel as two subsequent timestamps t_T and t_E which are stored in two register stages R1 and R2 by the Hit Receiver module. With each Ready signal from the TDC channel, the timestamps are shifted through R1 and R2 such that the registers always contain the current and previous timestamp. During the data transfers from the first register stage, the state of the VCO elements, which is at this point still provided in its original thermometric code, is

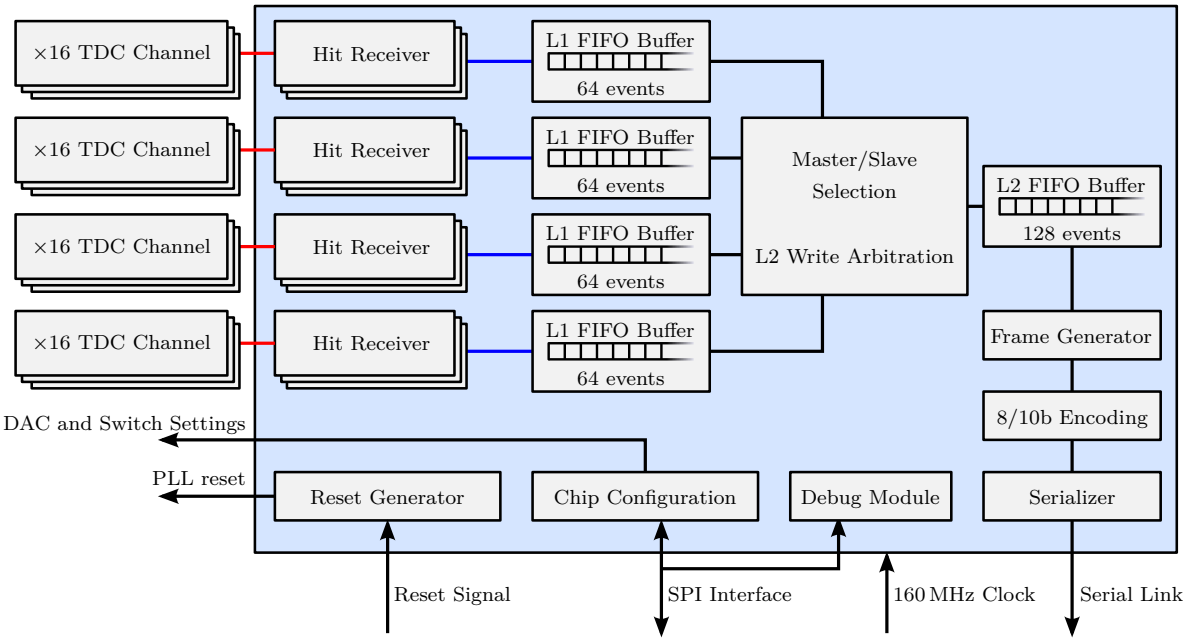


Figure 5.12: Block diagram of the digital control logic.

converted to the corresponding 5 bit binary number. If the recorded thermometric code is invalid, i.e. it contains more than one consecutive sequence of 0 or 1, the conversion is flagged by an additional bit which is referred to as BadHit. To ensure the correct transfer of the timestamp data from the TDC to the registers in the digital control the asynchronous Data Ready signal of the TDC is synchronized to the digital clock by an additional Flip-Flop, before it is evaluated by the digital logic. The reset signal of the readout channel is also controlled by the Hit Receiver module and is generated simultaneously with the sampling of the timestamps. It stays active until the sampled Ready signal of the TDC is again low.

If the recorded energy flag of the current timestamp is high, the Hit Receiver will assign the timestamps stored in R1 and R2 to an event, which is copied to the Event Data registers. The new data is indicated to the later signal processing stages by the Event Ready signal. The requirement that the event has to pass the energy threshold to be recorded rejects a large amount of noise events, reducing the rate of generated events by the channel. The data is kept in the output registers until it has been transferred to the FIFO buffer by the next digital unit. The separate output data registers allow the Hit Receiver to continue recording timestamps from the TDC, which prevents the loss of TDC data while the current event data is written to the FIFO.

The Energy Flag signal can be overridden by the chip configuration, causing the Hit Receiver to generate an event for each recorded timestamp. This mode is used to measure the timing of signals that do not pass the energy threshold, such as single pixel signals, allowing to measure the single photon timing resolution or the dark count rate of the SiPM.

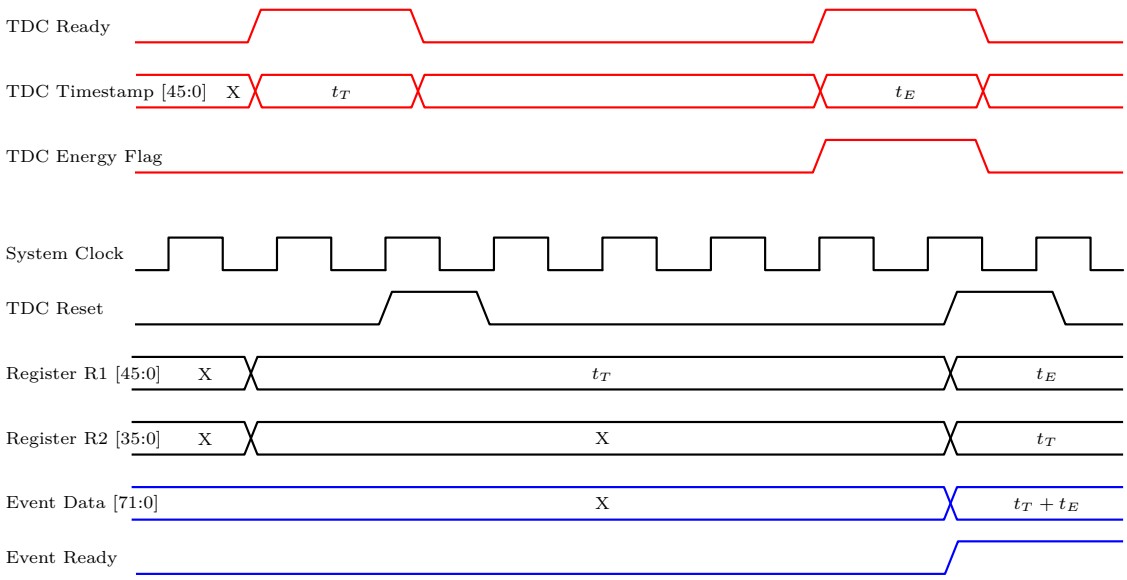


Figure 5.13: Signal waveforms during the event generation in the hit receiver modules.

Event Processing and Data Storing

The event data from the Hit Receiver modules is stored in 4 Level 1 (L1) FIFO buffers, which can store up to 64 events. Each L1 buffer is assigned to a group of 16 readout channels. The 4 bit channel number within a group is appended to the event data before it is written to the buffer. For the low event rates of 10 kHz per channel expected in the PET detector system, a simple priority arbitration based on the channel number is sufficient to control the write access of the channels to the L1 buffer. To prevent noisy channels from blocking the write access to the L1 buffer, the individual channels can be excluded from the data taking by the chip configuration.

In the next stage, the events stored in the four L1 buffers are transferred to the Level 2 (L2) FIFO memory, which stores up to 128 events simultaneously. Again, the group number is appended to the event data such that the resulting channel number contains 6 bits ranging from 0 to 63. Since each L1 group concentrates the data rates of 16 channels, the write access to the L2 buffer is arbitrated using a fair round robin algorithm to prevent a group from blocking the write access due to a high event rate.

Before the event data is written to the second FIFO buffer stage, the fine counter values of the T-Trigger and E-Trigger timestamps are used to select the correct coarse counter value. The selection criterion is programmable by a parameter of the chip configuration, which specifies the fine counter ranges in which the Master or Slave counter values are selected. For debugging purposes, a test mode has been implemented in which the same event is written twice to the FIFO, once with the Master and once with the Slave coarse counter value. The removal of the redundant data reduces the size of the events to 48 bits. The final data format of the events which are stored in the Level 2 FIFO buffer and transmitted to the DAQ system is shown in Table 5.1.

Serial Data Transmission

The data transmission of the events stored in the L2 buffer to the DAQ uses a 160 MHz serial data link, as specified by the EndoTOFPET-US system. The data link is encoded using 8b/10b encoding [78], which maps the byte symbols to 10 bit symbols. The mapping is chosen such that the symbols provide enough state changes to allow clock recovery from the data stream and achieve DC balance of the signal. In addition to the 256 mapped 8 bit signals, the encoding defines 12 control symbols, which can be used to control the data transmission. An important subset of these symbols are the comma symbols, which are used to reconstruct the bit alignment within the serial data stream. The encoding also provides a way to detect errors in the data transmission by the DAQ system, since invalid 10 bit symbols can be recognized, indicating a bad data link.

Every 1024 clock cycles, corresponding to 6.4 μs at 160 MHz, the transmission of the events currently stored in the L2 buffer is initiated. The event data is packed in frames which are mapped on the fly to the 8b/10b encoding. Every data frame consists of

- the frame header control symbol, which indicates the start of a new frame,
- followed by an 8-bit sequential frame number,
- the data of the events, transmitted least-significant byte first,
- the frame trailer control symbol, indicating the end of the event data,
- and the number of events transmitted in this data frame.

Between the individual frames, a comma-symbol is transmitted to allow the DAQ to recover the data transmission clock and to align the sampled bytes in the data stream.

Chip Configuration

For the configuration of the digital and analog modules the widely used Serial Peripheral Interface is implemented. The interface uses a simple shift register of Flip-Flops, as it is shown in Figure 5.14, to transfer the configuration data between the DAQ and the ASIC. A Chip-Select (CS) signal enables the data transfer to the chip and is low for the full duration of the data transmission. The output of the SPI interface is connected to the last element in the shift register. During the transmission, the previous data stored in the elements can be read back by sampling the SPI Data Out signal with each clock cycle. To prevent an invalid configuration to propagate to the analog modules during the data transfer, the SPI data is latched to the active chip configuration vector with the Chip-Select signal. The full

Bit	[0 : 4]	[5 : 19]	[20]	[21 : 25]	[26 : 40]	[41]	[42 : 47]
Value	E-Fine	E-Coarse	E BadHit	T-Fine	T-Coarse	T BadHit	Channel

Table 5.1: Event data format after digital signal processing.

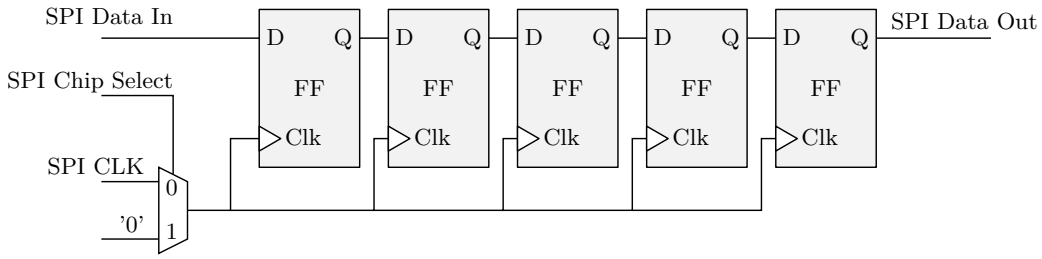


Figure 5.14: Serial Peripheral Interface implemented in STiC.

configuration pattern of the chip contains 4657 bits and includes parameters for the DAC settings of the analog signal processing and the TDC module, as well as parameters controlling the behaviour of the digital signal processing.

Chip Reset

The EndoTOFPET-US DAQ system specifies two reset modes, which are defined by the duration of the reset signal from the DAQ. A reset signal which is active for a single system clock cycle specifies a synchronization pulse to reset the coarse counter values of the TDC. Longer reset pulses are used to reset also the finite-state machines of the sequential digital circuits. The reset generator module interprets the lengths of the reset signal from the DAQ and issues the corresponding PLL and system reset signals.

Debugging Module

In order to monitor the operation of the digital logic, a debug module is implemented which shares the SPI signal lines but has a separate Chip-Select signal. A finite state machine evaluates a command field in the received data from the SPI interface to perform different debugging actions. Two digital output pads on the chip are controlled in this way, which allows to monitor the state of several important logic signals in the digital part, such as the status signal of the FIFO buffers. The debug module also allows to write event data to the L1 buffers, which can be used to test the data processing chain and verify the serial data transmission. In addition, the state of event data signals in the individual processing steps of the data path can be probed with the debug interface. By stepping the system clock of the digital core logic, this allows to reconstruct the digital data flow in the chip during the event processing.

5.3 Back-End Design Implementation

The physical implementation in the UMC 0.18 μm technology of the STiC3 ASIC contains 64 of the described high resolution readout channels together with the digital signal processing on a die of $5 \times 5\text{mm}^2$. For the implementation of the chip the design flow described in Chapter 4 has been used. The abstract views of the implemented custom analog blocks have been

generated from the physical layout of the modules and are provided in the Library Exchange Format format to the back-end tools. The layout uses a symmetric floorplan with the separate channels distributed along the left-hand and right-hand side, and the digital core placed in the center of the chip. The final layout of STiC3 is shown in Figure 5.15 and several design specifications are presented in this chapter.

5.3.1 Analog Readout Channels

Each readout channel has a width of 110 μm and a total length of 1448 μm, including both, the analog input stage and the TDC channel. Both sides of the symmetric floorplan contain 32 readout channels and are again subdivided in a top and bottom half. The readout channels are vertically abutted to automatically provide the required vertical power and signal connections. The Timebase units of the TDC on each side are located in between the sets of 16 TDC channels, distributing the global timestamp from the middle to the top and bottom of the chip. The reference clock for the PLL is supplied by differential pads from the top pad row of the ASIC. These high speed clock signals is routed differentially by manually specifying the metal traces of the interconnection.

The differential connection of the SiPMs to the analog input stages requires two analog signal pads per readout channel. To accommodate the 64 differential connections on both sides of the ASIC, the analog IO cells are staggered in two rows. The inner and outer rows correspond to the n- and p-input terminals of the channels, respectively. In order to connect the signals to the analog input stages, the metal traces have been manually specified to create the desired differential routing. For the shorter connections of the analog trigger output to the input terminals of the TDC channels, the mixed-signal router of Encounter provides good routing results and has been constrained to automatically create the differential interconnections. The signal monitor outputs of the analog input stage are connected to IO cells in the top pad row of the ASIC.

The power distribution network is separated in the sensitive power supply for the analog input stages and a common network for the TDC and digital core power. The two power networks are isolated from each other on the chip to reduce the pollution of the analog power by digital noise sources on the chip. Additional capacitors are added in the free spaces at the top and bottom, as well as the center of the chip to filter noise from the analog power lines.

5.3.2 Digital Core Logic

The digital logic is located in the center of the chip die, between the readout channels on the left and right-hand side. For the synthesis of the digital logic, the Faraday standard cell library [79] has been used. In the floorplan of the chip, the placement of the Hit Receiver modules is constraint to the areas in front of the corresponding TDC channel. The placement of the critical interface between the analog and digital signal processing of the chip has been manually arranged by defining Structured Data Paths (SDPs) in the Encounter software. This method defines structured columns and rows of Flip-Flops and has been used to achieve a

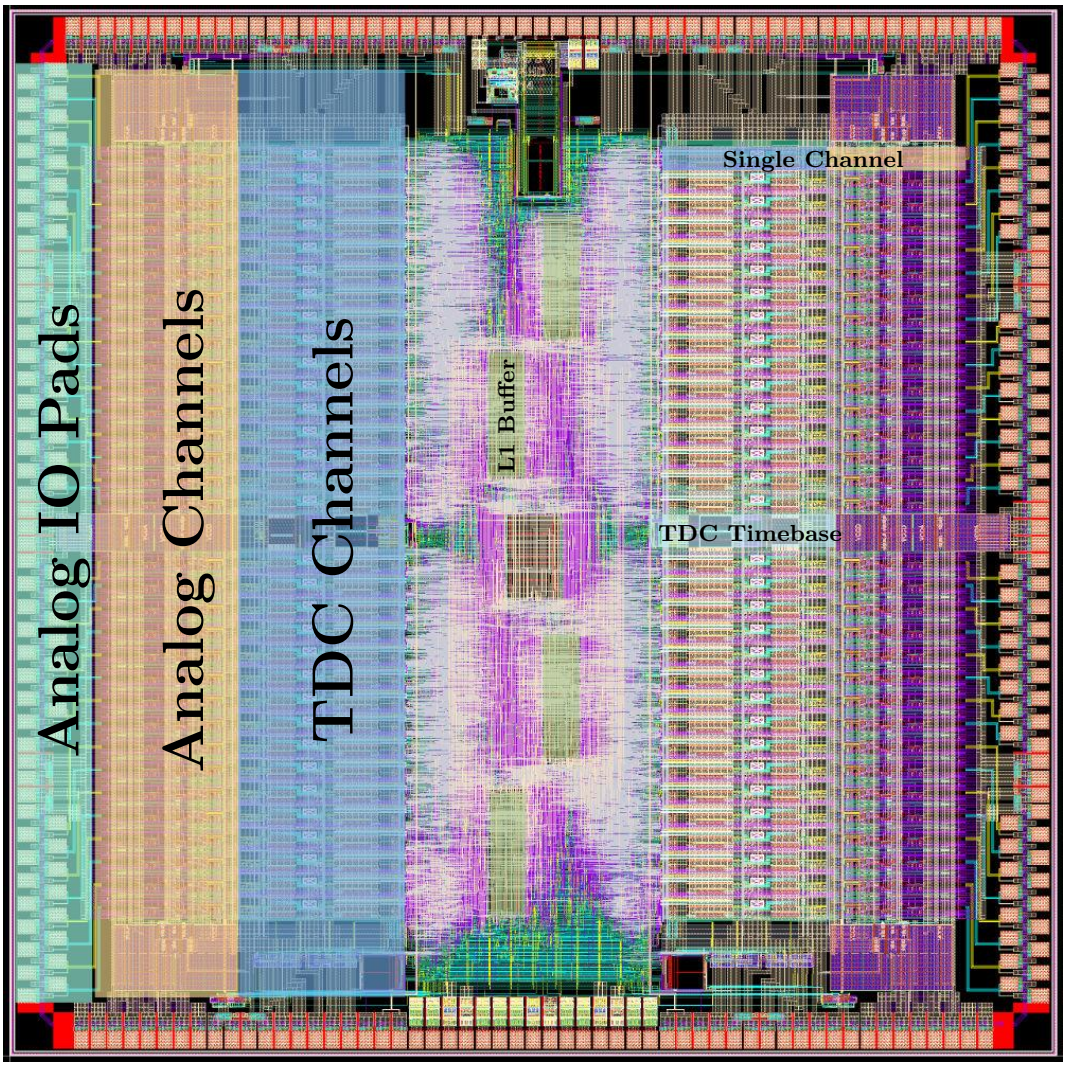


Figure 5.15: Layout of the STiC3 ASIC.

more uniform placement and routing of the standard cells in the Hit Receiver modules. The Tcl scripts and the results of the SDP definition are shown in Appendix A.1.

The placement of the Level 1 FIFO buffers close to the associated group of 16 Hit Receiver modules is also highlighted in the layout view of the chip. The Level 2 event buffer is situated in the center of the digital part. The digital IO cells are distributed to the top and bottom of the ASIC. At the top, the differential LVDS receiver and transmitter cells are placed, which receive the 160 MHz system clock signal and transfer the serialized data stream from the frame generator. The single ended Serial Peripheral Interface and the debug module connections are placed at the bottom of the chip. Power pads for the digital core logic are placed in both digital IO cell rows.

5.3.3 Timing Constraints

The timing of the clocks for the SPI and the system clock as well as the digital IO signals are specified in the timing constraints of the Back-End design and can be found as a reference in Appendix A.2. The Encounter software and the verification tools use these specifications as described in Chapter 4 to optimize and test the design for timing violations. The system clock has been slightly over-constrained with a period of 5.8 ns corresponding to 172 MHz. For the SPI clock signal, a period of 20 ns has be specified. The constraints also specify the data signals from the TDC channels to the digital core logic as asynchronous timing paths to exclude these signals from the evaluation of setup timing violations.

5.3.4 Design Verification

The chip has been extensively simulated before the design submission and has passed all physical and timing verification procedures described in Section 4.5.5.

The correct timing of the generated mixed-signal interface between the TDC and the digital logic has been verified by a mixed-signal simulation. In addition, the extracted transistor level SPICE netlist from the Hit Receiver module has been introduced to an analog simulation of the combined TDC channel and Hit Receiver. Both simulations showed no errors during the recording of events from the TDC channel by the digital module.

Apart from the static timing analysis of the digital part, a detailed backannotated simulation of the digital signal processing with randomly generated TDC events has been performed. The data reconstructed from the simulated serial interface has been compared to the generated random events to verify the correct behaviour of the digital core logic. During the simulations, no errors were found even in long simulations covering several seconds of system operation.

Chapter 6

Single Chip Performance

In order to validate the functionality and the performance of the designed ASIC, several characterization measurements have been conducted, which will be presented in this chapter. These include characterizations of the digital data processing, the TDC module, the analog input stage, as well as the full readout chain of STiC. The performance of the chip in terms of time and energy resolution for a PET detector system has been evaluated in coincidence measurements, using detector modules of the EndoTOFPET-US outer plate.

6.1 Characterization Setup

In all characterization measurements, the chip has been operated with a common setup, which includes the power supply of the chip, the reference clock signals for the PLLs of the TDC module, as well as the data acquisition system. In this way, the environment for the test measurements is defined and provides reproducible results.

The chip is wire bonded to a printed circuit board (PCB) module and enclosed in glob top epoxy to protect the fragile bond wires from mechanical stress. The glob top also provides a thermal contact which is used to cool the chip with an additional heat sink during operation. A picture of the test setup is shown in Figure 6.1. The PCB has been specifically designed to facilitate the characterization measurements and provides pins to access all required debug IO pads of the chip. The connections to the input terminals of the analog readout channels are routed over a flexible circuit to connector boards. Several different connectors are provided on these boards to perform the required electrical tests and connect the SiPM sensors to the chip. To simplify the bonding structure for the PCB, only 28 of the 64 readout channels have been bonded on the test board. Each connector board has a separate high-voltage connection to adjust the bias voltage of the SiPM sensors. This allows to individually tune the operating voltage of the SiPMs on the opposite sides in a large range. A ceramic oscillator[1] provides a reference clock of 622.08 MHz with a stability of 50 ppm for the PLLs.

The PCB module is connected to a mainboard which contains the power regulator circuits to supply the chip with the required 1.8 V and 3.3 V operating voltages. The digital interfaces are connected over the mainboard to the DAQ system for the configuration and event readout of the chip. The DAQ is based on a Xilinx Spartan-6 [81] field-programmable gate array (FPGA) board. The FPGA board was designed at the Kirchhoff-Institute, and was also used in [82].

[1] FOX ELECTRONICS FXO-LC535R-622.08 LVDS oscillator [80]

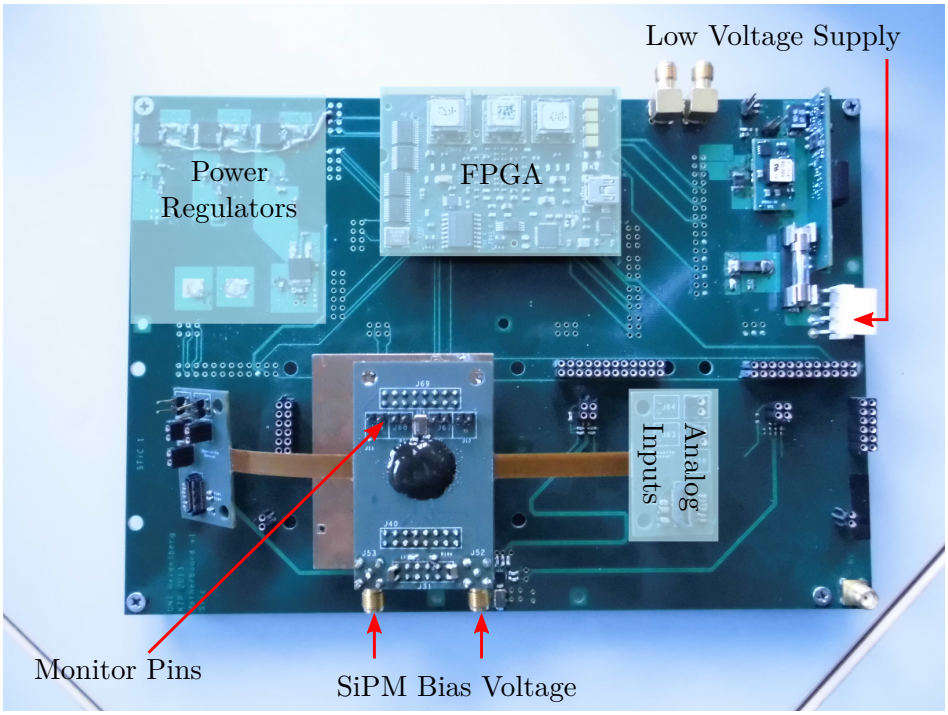


Figure 6.1: Test setup used for the characterization of the STiC3 ASIC.

The FPGA provides the necessary differential and single-ended IO ports to interface with the STiC ASIC. A USB interface is used to transfer data between the DAQ PC and the FPGA. As part of this thesis, the required firmware and software for the communication with the STiC chip have been developed and will be explained in this section.

6.1.1 DAQ FPGA Firmware

FPGAs are programmable integrated circuits (ICs), which provide a large number of configurable logic resources and RAM blocks to implement complex digital designs [83]. As in the design flow of a mixed signal ASIC, the digital circuits are described in a hardware description language and synthesized to a logic netlist. Instead of a standard-cell library, the netlist is then mapped to the available logic resources of the FPGA and programmed to the device to implement the described circuit.

In Figure 6.2, the block diagram of the FPGA firmware is shown, which has been designed for the configuration and event readout of the STiC ASIC. The data transfers between the submodules of the firmware is controlled by a finite state machine (FSM). The USB connection to the PC is established by a Cypress FX2 USB2.0 microcontroller [84] on the FPGA board. If the full bandwidth of the USB link is utilized, the event data can be transmitted at 480 MBit/s to the DAQ PC. The read and write processes between the FPGA and the Cypress microcontroller are handled by a dedicated USB FIFO interface module in the FPGA firmare.

The SPI for the configuration of the chip uses a master/slave communication model to

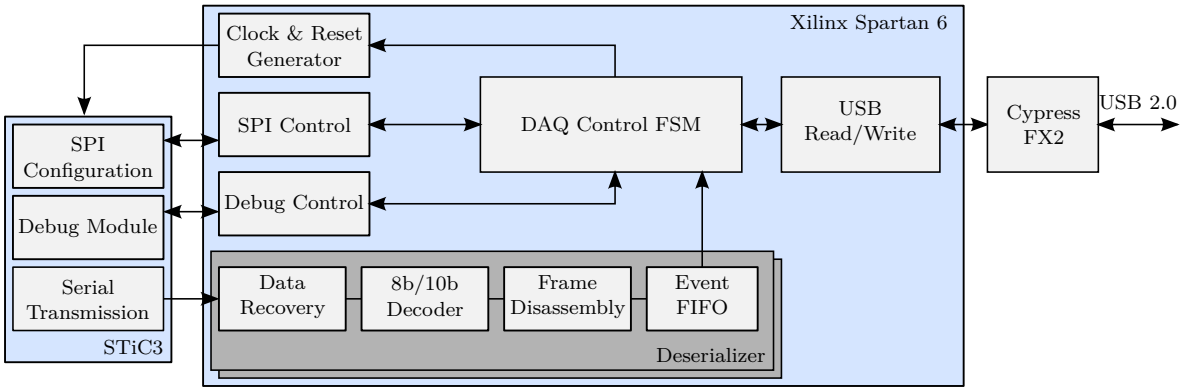


Figure 6.2: Block diagram of the DAQ firmware implemented in the FPGA.

transfer the data between the individual devices. The module implemented in the FPGA acts as the SPI master, controlling the transmission of the configuration provided by the DAQ software to the chip. After transmission, the previously stored chip configuration is sent back to the DAQ software. By writing the same configuration twice, the written and returned bit patterns are compared for validation of the data transmission process. The debug control module of the FPGA uses the same SPI module, although with a shorter bit pattern of 80 bit, containing the debug command and parameters. The debug procedure is controlled by the DAQ software on the PC, which composes the commands and parameter values and evaluates the response from the chip.

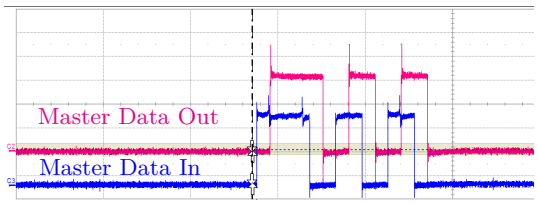
The event data transmitted by the STiC ASIC is processed in a deserializer module, which recovers the data bits in the serial data stream based on a technique described in an application note from Xilinx [85]. From the embedded comma symbols, the correct alignment of the 10 bit symbols in the sampled bit stream is determined. In the subsequent steps, the 8b10b symbols are decoded into control and data bytes, which are then used to disassemble the data frame. The extracted event data is written to a FIFO buffer, which can store up to 8192 events before they are transmitted by USB interface to the PC.

6.1.2 DAQ Software

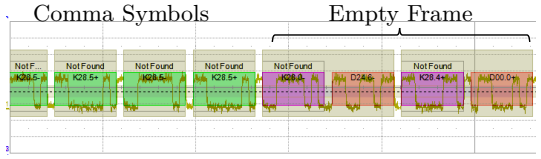
The DAQ software has been developed for the Linux operating system and provides programs for the configuration, event readout and debugging of the STiC chip. A variety of tools are provided to facilitate the debugging and monitoring of the chip operation, as well as recording automated measurement runs.

The event data is received in the format given in Table 5.1 and has to be processed by the DAQ software into time and energy values. In the first step, the values of the LFSR are converted to their 15 bit binary sequence number. For the event timing, the 5 bit of the T-Fine counter are appended to the corresponding coarse counter value:

$$\text{Time} = \text{T}_{\text{Coarse}} \cdot 32 + \text{T}_{\text{Fine}} \,. \tag{6.1}$$



(a) Transmission of an SPI configuration to the chip. The configuration has been written twice and the data output matches the input bit pattern.



(b) Serial data stream from STiC showing the transmission of an empty data frame.

Figure 6.3: Verification of the digital communication interfaces of STiC.

The Time over Threshold is calculated by the difference between the E-Trigger and T-Trigger coarse counter values:

$$\text{Energy} = \text{E}_{\text{Coarse}} - \text{T}_{\text{Coarse}} \,. \tag{6.2}$$

The resulting time and energy values are stored together with the original data in ROOT [86] files for data analysis. The software also provides an online monitor, which can display histograms of the energy, time, period or TDC raw data of recorded events. With these monitors, the effects of different chip parameters on a measurement can be immediately observed and the data quality verified before recording long measurement runs.

The chip configuration is specified in a graphical user interface (GUI), which provides a user friendly way for editing the large amount of configuration parameters of the chip. The configuration can be directly sent to the chip or saved in text files. The text representation is also used during automated measurement runs to modify parameters in the file in a specified range and configure the ASIC with the updated configuration. For the characterization measurements performed in this chapter, the corresponding chip configurations are listed in Appendix B for reference.

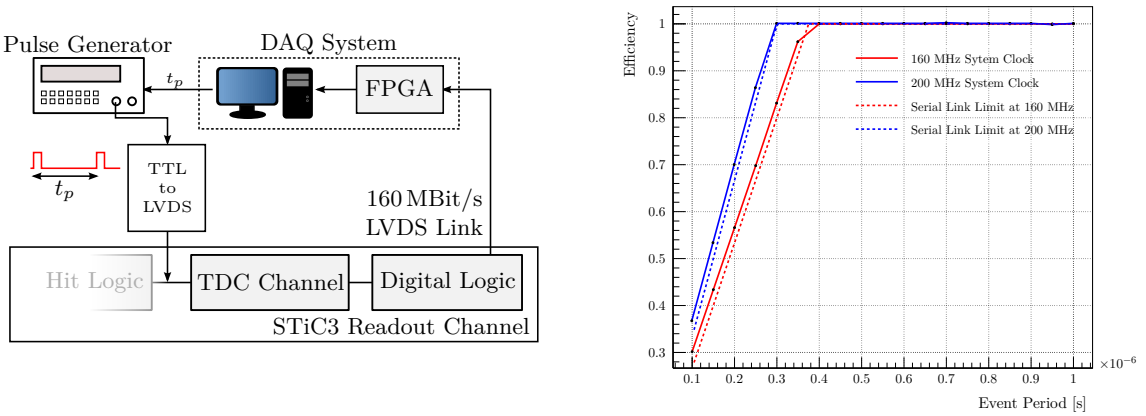
6.2 Digital Logic Verification

The correct behaviour of the digital chip interfaces has been verified with a serial data analyzer (SDA)[2]. The waveforms of the SPI and 8b10b encoded serial data link recorded with the oscilloscope are shown in Figure 6.3.

While the correct transmission of the configuration data is verified by matching the bit patterns at the data input and output of the interface, the serial data link has to be first decoded by the SDA. The transmission of an empty frame from the chip is shown in Figure 6.3b. The encoded 8b10b symbols are highlighted by the SDA showing the comma symbols, which define the alignment of the 10 bit characters in the serial bit stream, and the control and data symbols of the transmitted data frame structure from the chip.

As described in Section 5.2.3, the debug module implemented in the digital core logic allows to write event data to the L1 buffers of the chip. This functionality has been used to

[2]LeCroy SDA 813Zi



(a) Measurement setup for injecting trigger signals to the TDC Channel.

(b) Event processing efficiency compared to the limit of the serial data link.

Figure 6.4: Measurement of the maximal possible event rate at system clock frequencies of 160 MHz and 200 MHz.

verify the digital signal processing by writing events with known timestamp values to the buffers and recording them in the DAQ system. The recorded timestamps of the events are then compared to the values expected from the injected data. During these tests, no errors in the digital data processing or the subsequent event data transmission from the chip to the DAQ were found.

An important parameter of the chip is the maximum event rate R_{max} that can be processed and transmitted without loosing events. Due to the small dead time of the TDC channels and the parallel processing of the event data in the digital core logic, the "bottleneck" for the maximum event rate is the limited bandwidth of the serial data link to the DAQ system. At a speed of 160 Mbit/s and 48 bit per event, the maximum event rate is given by

$$R_{max} = 160\,\text{Mbit/s} \cdot \frac{8}{10} \cdot \frac{1}{48\,\text{bit}} = 2.67\,\text{MHz}\,. \tag{6.3}$$

The factor of 0.8 is given by the efficiency of the 8b10b encoding. The overhead of the data frame structure is with 16 bit per frame negligible and therefore not included in the calculation.

The maximum event rate the chip can sustain has been measured by injecting a defined number of trigger signals with a specified frequency and measuring the fraction of events transmitted by the chip to the DAQ system. The setup which has been used for this measurement is shown in Figure 6.4a. The trigger signals generated by a pulse generator are directly connected to the TDC channel using the debug pads of the analog signal processing. In the designed DAQ system, the speed of the USB 2.0 interface is not fully used and the bandwidth of the data transmission from the FPGA to the PC is smaller than the 160 Mbit/s of the chip. In order to still measure the bandwidth limitation of the chip, the trigger events have been generated in bursts of 5000 events. This amount of generated events can be completely

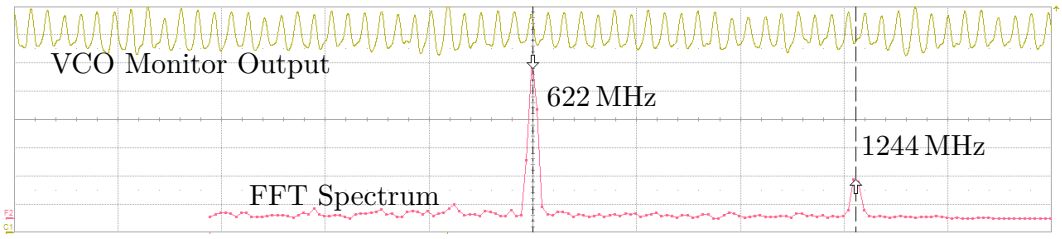


Figure 6.5: Measurement of the VCO frequency using the corresponding monitor output signal for a PLL in the locked state.

stored inside the memory of the FPGA, but exceeds the buffer capacity of 192 events of the STiC ASIC. In this way, the maximum event rate is only limited by the speed of the serial link between the chip and the FPGA.

In Figure 6.4b, the fraction of events transmitted to the DAQ is plotted against the period of the generated trigger pulses for the nominal system clock frequency of 160 MHz and at a higher speed of 200 MHz at which the chip is still functional. As can be seen from this measurement, up to an event period of 100 ns corresponding to an event rate of 10 MHz, the measured efficiency follows the theoretical limit of the serial link. Because the events are generated in bursts, the measured maximum event rate slightly exceeds the calculated limit due to the event buffers in the chip. If all channels are active, the digital bandwidth of the link is shared by the 64 channels. Consequently, the maximum event rate per channel is 41 kHz, which is sufficient for the expected event rate of 10 kHz per channel in the EndoTOFPET-US system. For high rate experiments like the Mu3e project, the speed of the serial link and thereby the maximum event rate will be increased in future STiC versions.

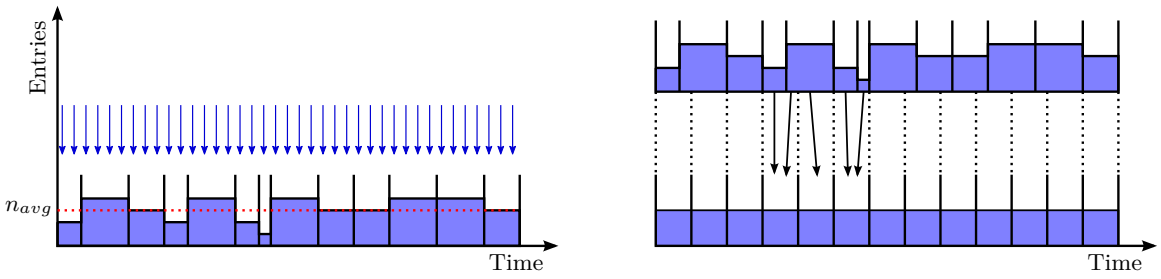
6.3 TDC Characterization

The setup shown in Figure 6.4a has also been used to characterize the TDC module, which encompasses measurements of the PLL locking behaviour, the non-linearities of the fine counter distribution in the individual TDC channels, as well as the timing resolution for the measurement of different pulse periods. An in depth characterization of the TDC module has been performed at ZITI Heidelberg using the TC_UM16 chip and is presented in [77].

6.3.1 PLL Locking

As explained in Section 5.2.2, the VCO of the Timebase unit has to be locked to an external reference clock to provide a stable and precise time reference to the TDC channels. To achieve this locked state, the bias voltages of the phase detection circuit, the charge pump and the delay elements in the ring oscillator have to be tuned.

To assess the state of the PLL in the different configurations, the oscillation of the VCO can be measured on the dedicated monitor output pad of the chip, which is shown in Figure 6.5.



(a) Measured fine counter distribution with uniformly generated events in a code density test.

(b) Pseudorandom bin dithering to correct the non-linearities of the fine counter [87].

Figure 6.6: Determination and correction of the fine counter non-linearities.

The Fast Fourier Transform of the signal shows the expected peak at 622 MHz and the first harmonic at 1244 MHz, verifying that the PLL is locked to the external reference frequency.

In setups where the VCO monitor is not accessible, the state of the PLL can also be determined by using the debug pads of the analog channel to inject trigger signals with a defined period, as presented in Figure 6.4a. From the measured time difference in TDC bins and the known period of the injected trigger signals, the average bin size of the VCO elements can be calculated. In the locked state, this value will be $1/622.08\,\text{MHz}/32 = 50.2\,\text{ps}$. Typically, the locking procedure requires only a small adjustment of the bias voltage for the VCO delay elements, while the settings of the phase detection and charge pump can remain at a default value. This has been exploited to automatically find the correct bias settings for the PLL during the characterization of the produced EndoTOFPET-US modules, which will be explained in Chapter 7.

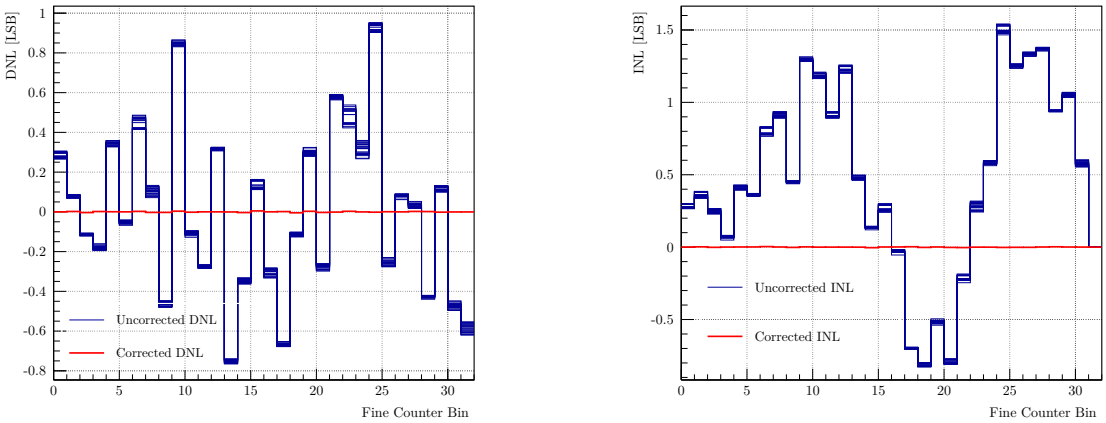
6.3.2 Fine Counter Non-Linearities

In order to evaluate the differential and integral non-linearities of the VCO elements, the delays of the individual fine counter bins have to be measured by a so-called code density test (CDT), which is graphically illustrated in Figure 6.6a. In this test, a defined number of trigger events are generated with a uniform distribution over the coarse counter period. The number of events recorded in a single fine counter bin is proportional to its propagation delay [88]. The expected average number of events n_{avg} per fine counter bin is given by the ratio between the number of available bins and the total number of generated events. With this, the differential non-linearity of time bin i can be calculated from the CDT by

$$DNL_i = \frac{n_i}{n_{avg}} - 1\,, \tag{6.4}$$

where n_i is the number of recorded events in this time bin. With the known DNL values of the bins, the corresponding INL is given by Equation 5.9.

Several approaches exist to correct the non-linearities of a TDC, such as the use of lookup tables for the correction of the INL or remapping of the non-uniform time bins to a uniform



(a) Differential non-linearity.

(b) Integral non-linearity.

Figure 6.7: Measured non-linearities of the TDC using a code density test before and after DNL correction. The measurement was repeated in regular time intervals to validate the stability of the distribution.

distribution [87]. The latter approach is used in this thesis. From the known bin sizes of the VCO elements, a statistical mapping is defined between the fine counter bins and an uniform distribution of the bins, as shown in Figure 6.6b. The probability values of the mapping are calculated from the overlap of the time intervals covered by the real fine bins and the ideal case.

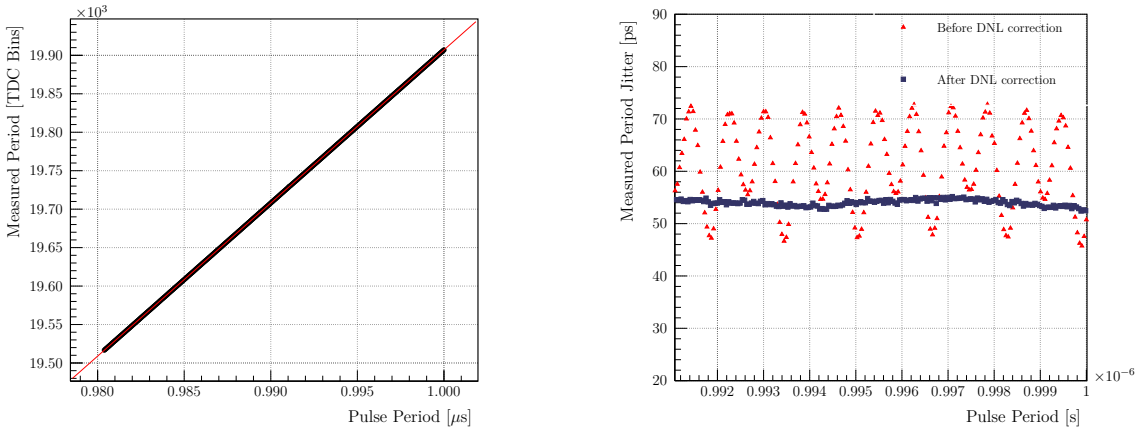
When mapping the fine counter to a uniform distribution with the same number of bins, the more accurate time information provided by cells with a short propagation delay is lost. This case is demonstrated in Figure 6.6b for the two small fine counter bins which are mapped to the same bin in the uniform distribution. In order to retain this information and improve the resolution of the measurement, the fine counter can be mapped to a uniform distribution with smaller bin sizes.

Figure 6.7 shows the measured differential and integral non-linearities of a TDC channel using the code density test before and after calibration. The measurement was repeated in regular time intervals for the same channel to evaluate the stability to the VCO delays. As expected from the time interpolation by the PLL, the differential non-linearities are less than 1 LSB and are stable over time. The values measured with the STiC ASIC are consistent with the characterization of the TDC module integrated in the TC_UM16 chip presented in [77].

6.3.3 TDC Resolution

The resolution of the TDC has been evaluated by measuring the period of a precise trigger signal. For this characterization, the same setup presented in Figure 6.4a has been used. The trigger signal for the TDC is provided by a precise pulse generator[3]. The period of the trigger

[3]The used trigger signal is generated by the digital controller unit EIG 20000X of the PiLas Laser system [89].



(a) Measured difference in TDC bins for different periods.

(b) Resolution of the measurement for different signal periods before and after DNL correction.

Figure 6.8: Period measurement with the TDC for different pulse periods.

signal has been varied in small steps to cover all possible fine counter difference values.

Figure 6.8a shows the measured period in TDC bins plotted with respect to the configured period of the pulse generator. A linear fit to this curve is used to determine the average bin size of the TDC bins and thereby the frequency of the VCO clock, which yields a value of $(622.097 \pm 0.001)\,\mathrm{MHz}$. This is consistent with the frequency stability of 50 ppm of the reference clock from the external oscillator and also shows that the PLL is locked. The measured resolution of the TDC is shown in Figure 6.8b for the different trigger periods. Without DNL corrections, the time distributions are distorted and the measured jitter varies in a range of approximately 25 ps, depending on the period of the input trigger signal. After the DNL corrections are applied to the recorded timestamps, the measured jitter is stable within 3 ps at a resolution of $\sigma_{period} \approx 55\,\mathrm{ps}$. The remaining fluctuation visible in the resolution is caused by a period dependent jitter of the generated trigger signals[4] This shows that the TDC module delivers the required performance for the precise time measurements. In all remaining measurements using the TDC module, the non-linearities have been corrected with the described method.

6.4 Full Readout Chain Measurements

The performance of the time and charge measurement of the STiC ASIC with the full readout chain has been evaluated using a charge injection setup, which is illustrated in Figure 6.9. In this setup a capacitor C_{inj} and an arbitrary waveform generator[5] are used to emulate the signal of a SiPM at the positive input terminal of the analog readout chain, while the negative

[4]The period dependent jitter has been confirmed by measurements with an oscilloscope.
[5]Tektronix AWG 7102

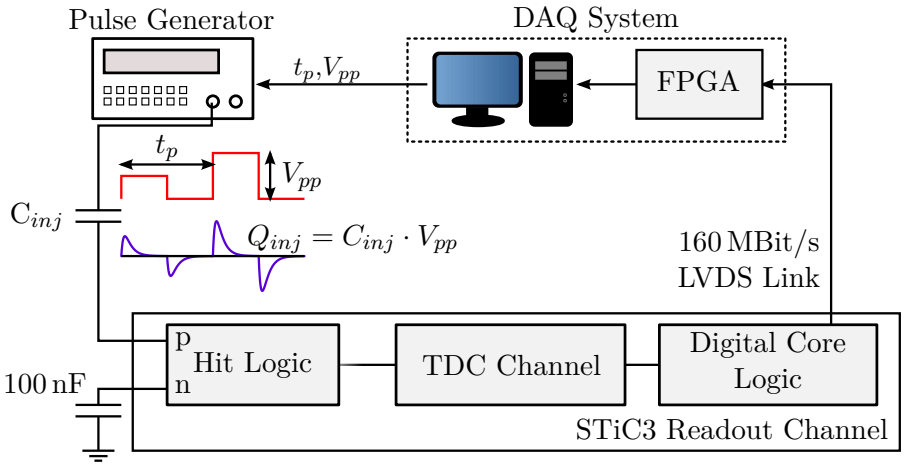


Figure 6.9: Charge injection setup for the characterization of the complete readout chain.

terminal is AC coupled with 100 nF to ground. With the known pulse amplitude and the value of C_{inj}, the charge of the injected signal is

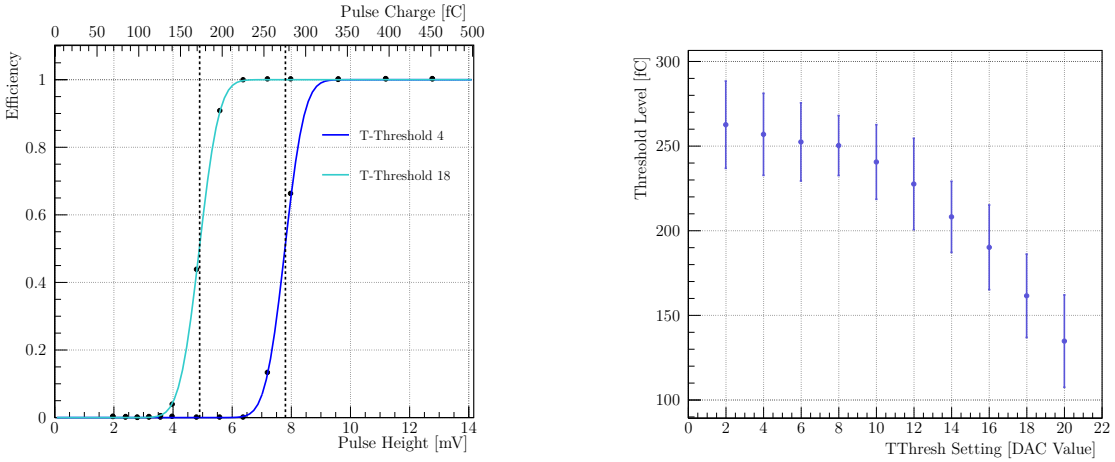
$$Q_{inj} = C_{inj} \cdot V_{pp} \,. \tag{6.5}$$

The period t_p and pulse amplitude V_{pp} of the generated trigger signals are remotely controlled by the DAQ PC, which is used to measure the response of the discriminators for different pulse amplitudes and chip configurations in automated measurement runs.

During the characterization of the analog input stage, a problem in the current feedback circuit was found, which limits the possible configurations for the input stage bias current to low values. Because of this, all measurements were performed with the same Input Bias DAC parameter of 4, corresponding to a current of approximately 25 μA. The problem has already been corrected in the latest submission of STiC version 3.1.

6.4.1 T-Trigger Response

For the timing path, the behaviour of the T-Trigger at small signal charges corresponding to a signal of a few fired pixels of a SiPM is of particular interest. At a gain of 10^6 the current pulse generated by a single SiPM pixel contains a charge of 160 fC. Therefore an injection capacitor of 33 pF and pulse amplitudes of 1 mV to 30 mV are used, corresponding to signal pulses from 33 fC to 990 fC. Since small signals in this range do not pass the threshold of the energy discriminator, the chip is configured to record all timestamps generated by the TDC as individual events, as described in Section 5.2.3. With this setup, the threshold levels of the discriminator circuit, as well as the jitter of the T-Trigger has been measured, using the full signal processing chain of the chip.



(a) Measured trigger efficiency at two different threshold levels for different injected signal charges.

(b) Measured thresholds levels and noise for different T-Threshold DAC configurations.

Figure 6.10: Measurement of the T-Threshold trigger levels using a single ended charge injection.

T-Threshold Scan

The threshold level of the discriminator is determined by measuring the trigger efficiency for increasing signal charges. When the charge of the injected signal crosses the threshold level, the efficiency will rise from 0 % to 100 % as it is shown in Figure 6.10a for two different T-Threshold DAC settings. The slope of the transition is determined by the noise on the threshold level and the input signal. From the fit of a Gauss error function, the discrimination level and noise can be extracted.

To confirm that the threshold can be set at the low single pixel levels required for the high timing resolution, the efficiency curves have been measured for the different possible T-Threshold settings of the channel. The corresponding DAC parameter can be configured in a range from 0 to 63, with a higher DAC value causing a lower threshold level. The efficiency curves have been measured at each DAC setting and the threshold level and noise are extracted from the data with a fitted Gauss error function. The result of this scan is shown in Figure 6.10b. At DAC settings larger than 20, the discrimination threshold reached the noise level of the used charge injection setup and the subsequent measurement points have been excluded from the plot.

The scan confirms, that the trigger threshold can be tuned below the level of 150 pC of a single pixel SiPM signal. In the differential readout scheme used for the SiPM, the signal charge will also be mirrored on the negative input terminal of the channel, which will improve the rejection of common mode noise on the signal. Since the T-Trigger is generated by the difference between the positive and negative output of the input stage, as explained in Section 5.2.1, the trigger threshold in this readout mode will be effectively scaled by a factor of 1/2.

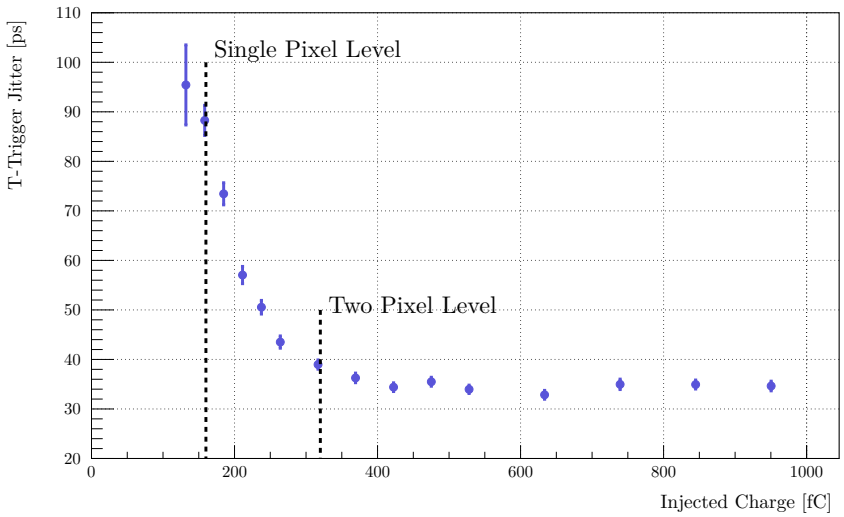


Figure 6.11: Dependence of the period jitter on the injected signal charge for the T-Threshold DAC setting of 20.

T-Trigger Jitter

The pulses generated by the arbitrary waveform generator have been used to measure the jitter of the T-Trigger for different injected signal amplitudes and different threshold DAC settings. With a total jitter of less than 20 ps and transition times of 45 ps [90], the timing of the generated trigger signals is precise enough to measure the jitter of the T-Trigger in the picosecond range.

Similar to the characterization of the TDC resolution, the jitter has been determined from the resolution σ_{period} of the period measurement as $\sigma_T = \sigma_{period}/\sqrt{2}$. Figure 6.11 shows the measured trigger jitter for the lowest possible threshold level of the T-Threshold scan plotted against the charge of the injected signal. At the charge level corresponding to single pixels, the jitter value is smaller than 90 ps. With increasing injected charges, the jitter improves until it reaches a minimal value of $\sigma_t \approx 35$ ps and is at the 2 pixel level already below 40 ps. For the signals generated by the detection of 511 keV photons containing a signal charge of more than 200 pC, a good timing resolution can be expected.

6.4.2 Linearized Time over Threshold Response

As explained in Section 5.2.1, the STiC chip features a linearized ToT method, which integrates the charge of the input signal on the detector capacitance itself. To verify this method, larger signal charges have to be injected and the injection capacitance has been consequently increased to $C_{inj} = 330$ pF. The signal amplitude of the pulse generator has been varied in a range from 40 mV to 1.6 V, corresponding to signal charges of 13.2 pC to 528 pC.

The mean value of the ToT response to the injected signal charges has been evaluated for different E-Threshold settings and is plotted in Figure 6.12. For larger threshold DAC

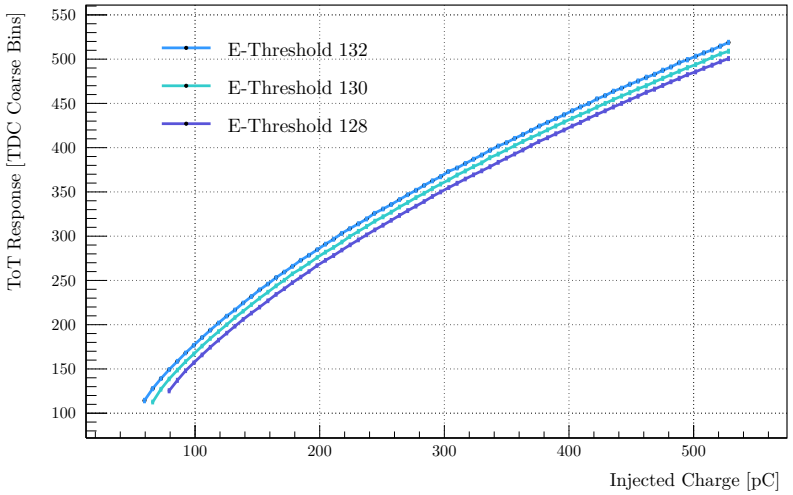


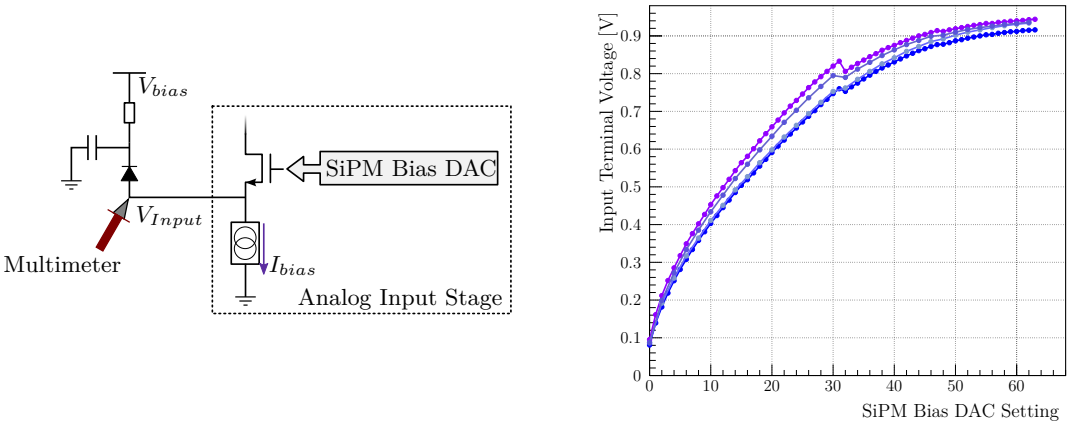
Figure 6.12: Measured Time over Threshold response to the injected signal charge for different E-Threshold settings.

settings, which again translates to a lower discrimination level, the measured ToT increases and starts triggering at lower thresholds, as expected. The measurement clearly shows the linearization of the ToT response to the signal charge, which promises a significantly improved energy resolution compared to conventional ToT methods.

6.4.3 SiPM Bias Tuning

In order to stabilize the operation of the SiPM and compensate for variations in the breakdown voltage of the sensors or changes in the temperature, the STiC ASIC provides the possibility to control the voltage at the input terminal as it is shown in Figure 6.13a. The terminal voltage is determined by the gate voltage of the input transistor and the corresponding bias current. Both parameters can be tuned by a DAC setting in the chip configuration.

Figure 6.13b shows the measured voltage at the input terminal of four different channels plotted against the SiPM Bias DAC configuration. A tuning range of more than 700 mV is achieved for all channels with a channel to channel deviation of less than 10 %. Between the DAC values 31 and 32, the transistors with the largest influence on the DAC output voltage are switched. Because of fluctuations in the fabrication, mismatches between the individual transistors can cause a non-monotonicity, which can be observed in the measurements between these DAC values. During the switching of the lower DAC bits, this effect is less pronounced and not visible in this plot. Assuming a temperature dependence of 0.058 V/K for the sensor [40], a fluctuation of up to 12 °C can be compensated.



(a) Setup for the measurement of the SiPM bias tuning.

(b) Measured voltage at the input terminals of four different channels at different SiPM Bias DAC settings.

Figure 6.13: Characterization of the SiPM bias tuning with STiC.

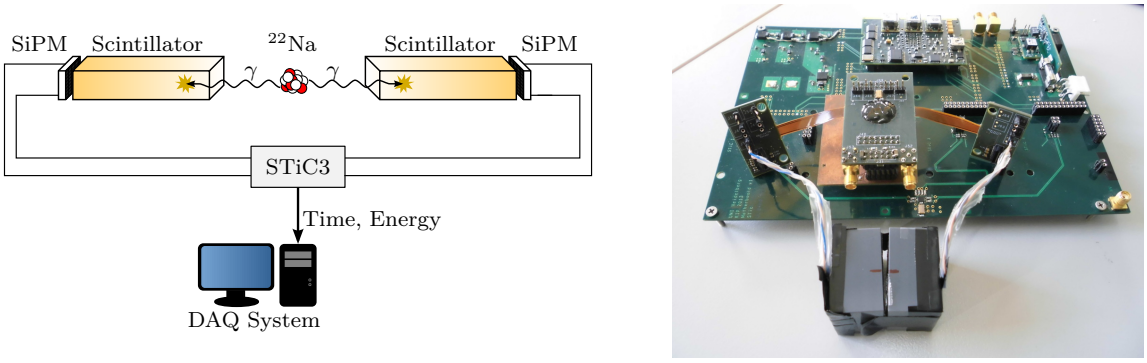
6.4.4 Power Consumption

The current used by the STiC ASIC during operation has been measured to determine the power consumption of the analog input stage and the combined consumption of the TDC and digital core logic. With all channels configured to their working configurations, the current consumed by the analog channels is 0.45 A at 1.8 V, corresponding to 0.81 W for all configured 64 channels. The TDC module and the digital core logic require a current of 0.9 A, which corresponds to 1.62 W. The power consumptions of the full chip sums up to 2.43 W or 38 mW per readout channel. To protect the chip from damage by the generated heat during long measurement runs, the die is cooled with a heat sink and an air fan.

6.5 Coincidence Measurements

The design goal of the STiC ASIC is to provide a very high timing resolution for the readout of SiPMs in coincidence measurements. To characterize the performance of the chip in this regard, coincident photons from positron annihilations have been measured to determine the energy resolution and the Coincidence Time Resolution of the system. The setup for this measurement is illustrated in Figure 6.14a. A radioactive ^{22}Na source with an activity of approximately 15 kBq is used as a β^+ emitter. The 511 keV photons generated by the positron annihilation are detected by two opposing $3.1 \times 3.1 \times 15\,\mathrm{mm}^3$ LYSO:CE crystals, which are wrapped in Teflon foil to enhance the light collection efficiency of the generated scintillation photons. Each crystal is glued to a single channel of a 4×4 SiPM array from Hamamatsu[6] with a sensitive surface of $3 \times 3\,\mathrm{mm}^2$. The same SiPM matrices are also used in the outer

[6] Hamamatsu MPPC S12643-050CN(X))



(a) Diagram of the coincidence setup.

(b) Picture of the detector modules connected to the STiC testboard.

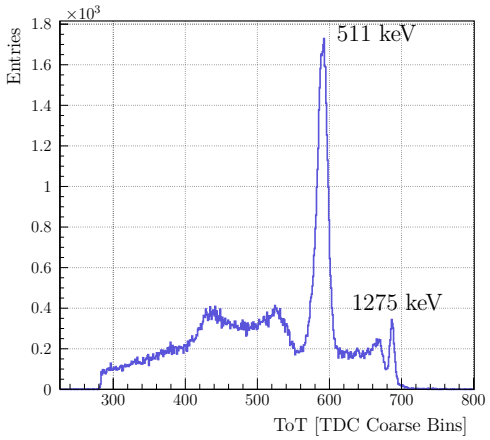
Figure 6.14: Detector setup for the measurement of coincident 511 keV photons from positron annihilations.

plate of the EndoTOFPET-US system [91]. The bias voltages for the SiPMs are provided by an external power supply [7] with two separate high voltage outputs, allowing to tune the SiPM bias voltage in a large range for both sensors individually. The SiPMs are connected to channels 20 and 33 of the STiC3, which are located on the left and right side of the chip, respectively. The measurements therefore also include the synchronization between different TDC modules. A picture of the two detector modules connected to the STiC testboard is shown in Figure 6.14b. The full setup can be operated inside an temperature chamber, which has been used in the final coincidence measurements to control and stabilize the ambient temperature of the setup. From the recorded data, the time and energy resolution of the STiC chip for the coincidence measurement of the photons is determined.

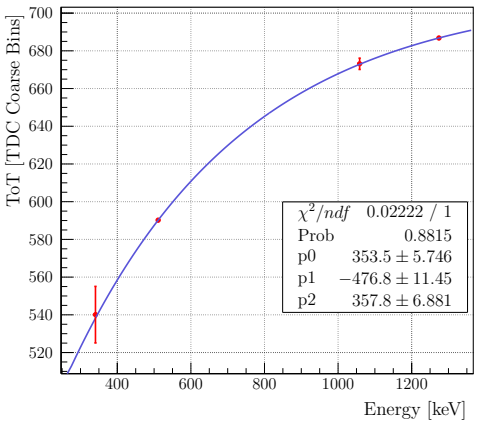
6.5.1 Energy Resolution

Figure 6.15a shows a ToT spectrum of the recorded events. The ^{22}Na decays predominantly to the 1.275 MeV level of ^{22}Ne, which instantaneously decays to its ground state [92]. Due to the linearized ToT method of STiC, the two photopeaks resulting from the positron annihilation and the decay of the exited state of neon can be observed simultaneously with a good resolution. However, the measured ToT response is not fully linear, which is mainly caused by the limited dynamic range of the SiPM. In order to calibrate the ToT to energy units, the known energies of the two photopeaks and the corresponding Compton edges are used as calibration points. While the position of the photopeaks can be determined by the fit of a Gauss function, the Compton edges have been manually read from the spectrum and estimated error for these points is consequently large. The calibration points extracted from the ToT spectrum are listed in Table 6.1.

[7] Agilent B2962A Low Noise Power Source



(a) Recorded Time-over-Threshold spectrum of the decay.



(b) Fit of the saturation curve to the chosen calibration points.

Figure 6.15: Measurement of the ^{22}Na decay spectrum. For the energy calibration, the Compton edges and the photopeaks of the 511 keV and 1.275 MeV photons have been used.

A parametrized form of the SiPM saturation function [42]

$$E_{ToT}(E_\gamma) = p_0(1 - \exp(\frac{E_\gamma}{p_1})) + p_2\,, \tag{6.6}$$

with three free parameters p_0 to p_2 has been used to describe the non-linear response. The fit of this function to the calibration points is shown in Figure 6.15b. With this calibration function, the width of the 511 keV photopeak in units of ToT is converted to keV. The fit of a Gauss function to the photopeak in the ToT spectrum yields a standard deviation of $\sigma_{ToT} = (8.3 \pm 0.03)$, which corresponds to $\sigma_E = (32.7 \pm 2.4)$ keV. The errors of the individual fit parameters have been propagated to the calculated width in energy units. For the measured 511 keV peak, the resulting energy resolution is

$$\frac{\sigma_E \cdot 2.35}{511\,\text{keV}} = (15 \pm 1.1)\%\,. \tag{6.7}$$

This result is consistent with the characterization of the scintillating crystals performed in

Energy [keV]	**Energy [ToT]**
340.7	540 ± 15
511	590.2 ± 0.1
1061.18	673 ± 3
1275	686.8 ± 0.1

Table 6.1: Calibration points for the conversion of ToT to energy. The error of the photopeak positions in the ToT spectrum is the error of the mean parameter from the corresponding Gaussian fit.

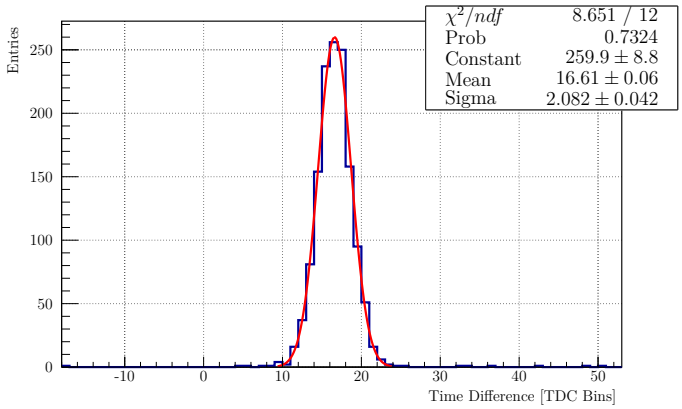


Figure 6.16: Measurement of the CTR between the two channels.

the framework of the EndoTOFPET-US project [93], and significantly exceeds the required resolution of 20 %. This also verifies the good energy resolution possible with the linearized ToT method.

6.5.2 Coincidence Time Resolution

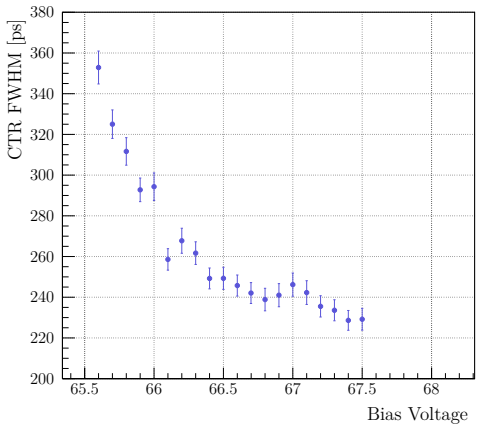
The selection of coincident events detected in the separate detector modules is based on the timing and the energy of the detected photons. As explained in Section 5.2.3, the data frames are generated every 6.4 μs and contain all events recorded since the last frame transmission. By considering only events within the same data frame for the measurement, a coarse coincidence time window is defined corresponding to the 6.4 μs data frame period.

The position of the 511 keV peak is determined by a Gaussian fit from the full data sample for each measurement. To select only photons which have been fully absorbed in the scintillator and reject Compton scattered events, the energy of the coincident photons has to be within $\pm 1.5\,\sigma$ of the 511 keV photopeak to be included in the analysis.

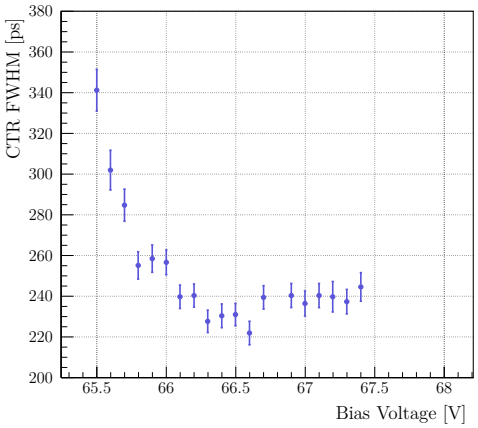
The initial chip configuration and the SiPM bias voltages have been tuned manually using the online event monitoring to record energy spectra with a clear 511 keV photopeak, and to optimize the rate of recorded coincidence events.

The Coincidence Time Resolution (CTR) is evaluated by measuring the distribution of the time differences between the selected coincidence events. A time spectrum measured with STiC using the described coincidence setup is shown in Figure 6.16. The data is fitted with a Gaussian function to evaluate the CTR, which shows a good resolution of (246 ± 5) ps FWHM.

As shown in Equation 3.23, the slope of the current pulses generated by the sensor increases with the overvoltage V_{ov}. A higher bias voltage of the sensors will therefore also improve the time resolution. Since the DCR also increases with the overvoltage, an optimal operation point for the sensors has to be found. In order to find this bias point, the high voltages for the SiPMs have been tuned for both detector modules individually. The optimization has been performed in two steps. In the first run, the bias voltage of channel 33 has been fixed



(a) High voltage scan of channel 20. Bias of channel 33 fixed to 66.3 V



(b) High voltage scan of channel 33. Bias of channel 20 fixed to 67.3 V

Figure 6.17: Measured CTR for different sensor bias settings. The measurements have been conducted without temperature stabilization.

to a voltage of 66.3 V, and only the high voltage of channel 20 is varied in a range of 1.9 V. For each measurement, the CTR is evaluated, as it is shown in Figure 6.17a. The sensor bias providing the best time resolution in this measurement has been fixed for channel 20 during the second run, in which the voltage of channel 33 is tuned. The CTR values measured in this second optimization step are shown in Figure 6.17b. The measurements show that a good coincidence time resolution of less than 250 ps FWHM can be achieved without difficulties by the STiC chip without temperature stabilization and in a large range of bias voltages

The measurements have been repeated at a stabilized ambient temperature of 18 °C, using a temperature chamber[8], to provide reproducible results at a defined temperature. The final detector system will be operated in an air conditioned operation room and the cooling system of the outer PET plate will operate at 18 °C, which is why this temperature has been chosen. Due to the lower dark count rate, a better time resolution is expected. Since the breakdown voltage of the SiPMs is reduced at the cooler temperature, the best bias point for the sensors was determined again. In the next step, the T-Trigger threshold has been tuned to find the best CTR value.

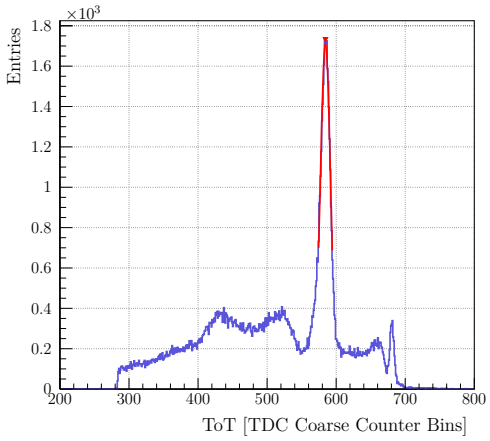
The best time resolution achieved after the tuning of the high voltage and T-Threshold settings, is shown in Figure 6.18. The measured resolution of

$$(213 \pm 3)\,\text{ps FWHM}$$

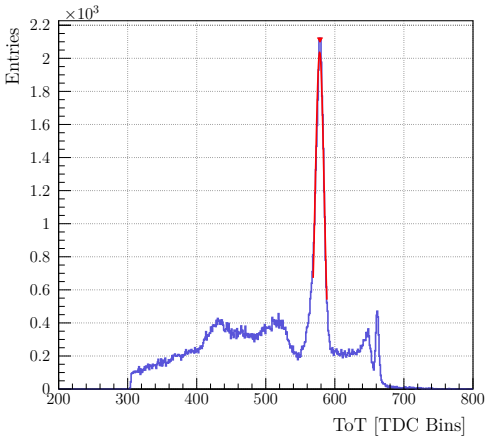
is very close to the envisioned 200 ps FWHM of the EndoTOFPET-US project. To the knowledge of the author this result is among the best coincidence time resolutions achieved in a mixed signal system for the readout of LYSO crystals coupled to SiPM sensors to date.

[8] TS Binder MK 53

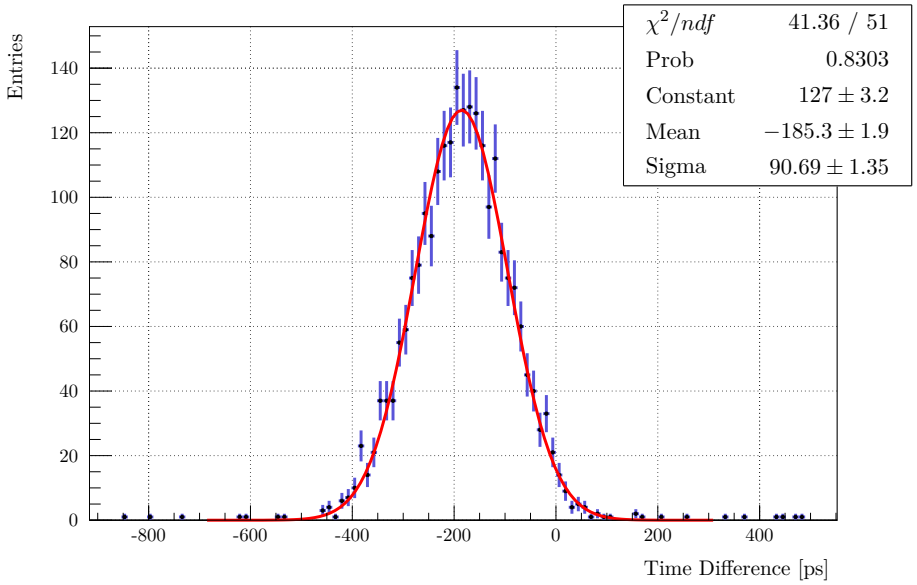
During the performed measurements, the bias current of the analog input stage was limited due to a problem in the current feedback circuits. In the new version 3.1 of STiC, this has been fixed and the tuning of the input bias will allow to reduce the input impedance of the readout channels further, which promises an even better time resolution. In addition, the STiC ASIC implements a tail cancellation circuit, which has not yet been used in the timing measurements. As is shown in [44], the tail cancellation can significantly reduce the influence of pileup effects, thereby improving the time resolution. Therefore, the full potential of the chip has not yet been uncovered. An exhaustive and systematic scan with the full parameter range of the chip is expected to yield even better results for the CTR measurements.



(a) Energy spectrum for channel 20.



(b) Energy spectrum for channel 33.



(c) Measured CTR of 213 ps FWHM at 18 °C after T-Threshold optimization.

Figure 6.18: Measurement of the coincidence time resolution between channels 20 and 33 [94].

Chapter 7

EndoTOFPET-US System Integration

In the last part of this thesis, one hundred STiC3 ASICs have been produced to fully equip the outer plate of the EndoTOFPET-US detector system. The production run has also been used to correct the problem found in the feedback path of the analog input stage. The manufactured chips have been integrated in readout modules, which were characterized in an automated test stand to verify their functionality. During these measurements, the bias parameters of the readout channels were automatically adjusted to find a working chip configuration. The outer plate has been fully equipped with 64 of the characterized STiC ASICs and is at the time of writing used for first pre-clinical tests at CERIMED[1] in Marseille.

7.1 PCB Design

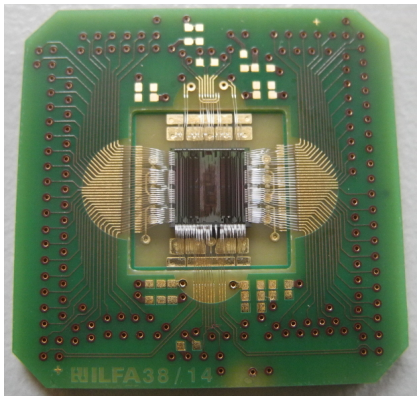
In parallel to STiC, the TOFPET ASIC [95] has been developed at LIP[2] in Lisbon as an alternative readout solution for the outer plate detector. To avoid the development of two distinct DAQ systems for the two ASICs, a common readout topology for both designs has been chosen. In this topology, two chips are mounted together on a single front end readout board (FEB/A) to provide 128 readout channels. The geometry of the modules has to be smaller then the surface of $30 \times 60\,\mathrm{mm}^2$ covered by the eight connected detector modules of the outer plate. A high speed connector with a compatible pinout for both developed ASICs is used to interface the chips with the DAQ system, which has also been developed at LIP [96, 97].

In order to accommodate the two STiC chips and the necessary passive components for the differential readout of the SiPMs in the available area, an approach using two separate boards has been pursued, which is presented below.

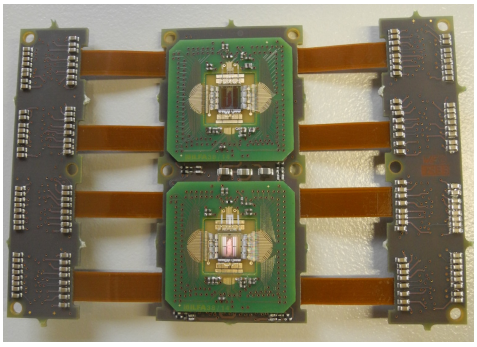
7.1.1 STiC3 MCM Board

The STiC3 ASIC itself is bonded on a small daughter board of $25 \times 25\,\mathrm{mm}^2$, which has been termed MCM[3] and is shown in Figure 7.1a. A ball grid array (BGA) on the bottom side of the board allows to solder the MCMs to the FEB/A modules. Due to the high density of bonding wires on both sides of the chip, which is required for the differential connection to

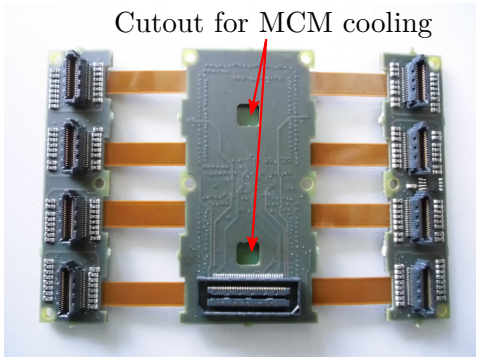
[1] Centre Européen de Recherche en Imagerie Médicale
[2] Laboratory of Instrumentation and Experimental Particle Physics
[3] Research group internal abbreviation for *magnificent chip module*



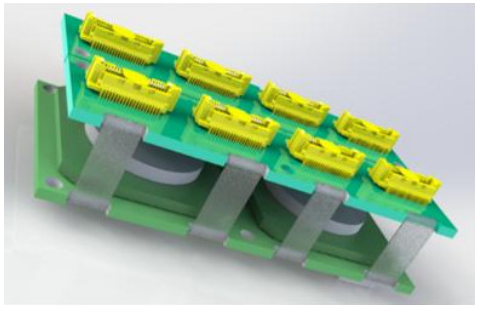
(a) STiC3 bonded to a cavity MCM module.



(b) FEB/A board with two mounted MCM modules.



(c) Backside of the FEB/A module.



(d) Illustration of the folded FEB/A board in the detector system [94].

Figure 7.1: STiC3 readout modules for the integration in the outer PET plate.

the sensors, the MCM has been designed using a PCB cavity process. This process allows to bond the pads of the chip directly to two different signal layers of the PCB. In this way, the complexity of the bonding structure can be significantly reduced. To prevent the chips from overheating, the die is thermally contacted by PCB vias to a metal pad on the bottom side of the board. This pad can be contacted by a cooling system to cool the chips during operation.

7.1.2 FEB/A Board

The FEB/A board is shown in Figure 7.1b and Figure 7.1c. It has been designed as a flexible circuit board to provide sufficient space for the required components. The eight connector sockets and passive components for the biasing and differential readout of the SiPM sensors are placed on the separate boards on either side of the module. In addition to the connectors and passive components for the SiPMs, a temperature sensor is included on one of the connector boards to monitor the temperature of the sensors during operation. In the central part of the FEB/A PCB, two MCMs are soldered to provide the required 128 readout channels, which can be seen in Figure 7.1b. A cutout on the backside of the board allows to contact the thermal

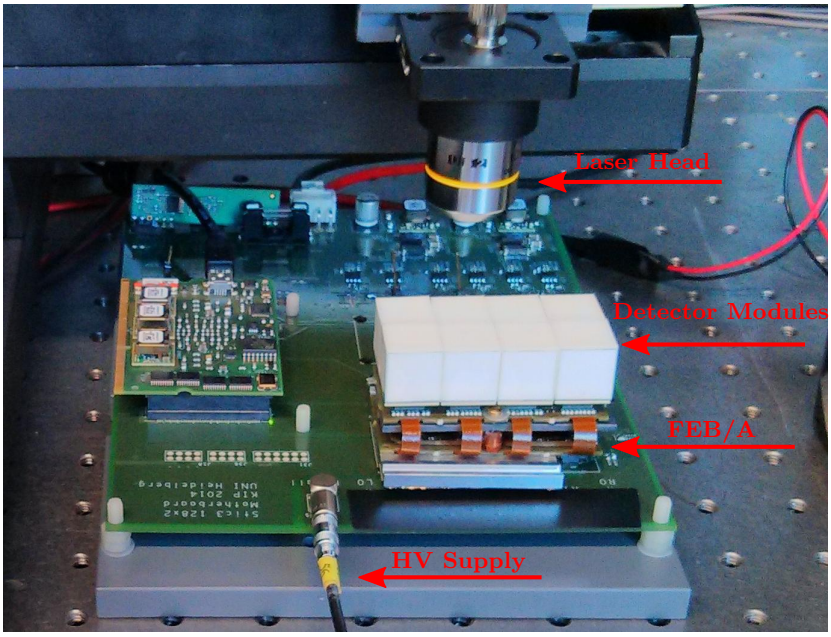


Figure 7.2: Measurement setup for the automatic FEB/A characterization.

pads of the MCMs in order to cool the mounted chips, as its shown in Figure 7.1c. In the detector system, the flexible parts are folded over the central FEB/A board to create two PCB layers, as it is shown in Figure 7.1d.

To equip the full outer plate with 32 FEB/A modules and provide additional boards for replacement, 40 readout modules have been produced and tested. Each board is identified by a serial number, which is used to reference the results of the automatic characterization and the generated configuration files to the chips mounted on the board.

7.2 Automated Functionality Tests

Before the readout modules have been sent for commissioning in the EndoTOFPET system, they had been tested and characterized in order to verify the functionality and find an initial set of working configuration parameters for the two ASICs on the board. In this section, the characterization setup, the measurement procedure and the result of the characterization tests of the produced boards are presented.

7.2.1 Characterization Setup

The readout of the FEB/A modules uses a dedicated mainboard, which connects the readout modules to the DAQ system presented in Section 6.1. The used test stand is shown in Figure 7.2. In order to confirm the functionality of the boards with the final detector system, the readout boards have been fully populated with detector modules from the outer PET plate. Since the characterization of the modules with a radioactive source would take too long,

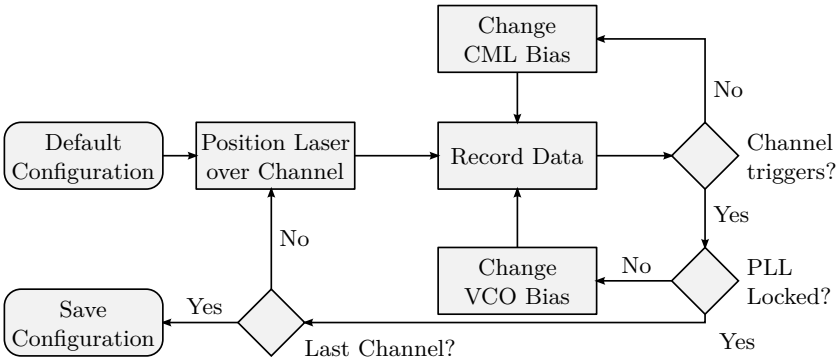


Figure 7.3: Flow chart of the automatic FEB/A test procedure.

the detector modules have been illuminated with a pulsed laser system[4]. The laser head is mounted on a remotely controlled positioning stage, which is used to automatically move the laser over a specific readout channel for characterization. During the measurement, the laser pulses recorded by the channel are analyzed in order to evaluate whether the channel is functional as well as adjusting the bias settings. A channel is considered to be working if it records a large fraction of the generated laser pulses and if the period of the recorded events matches the pulse period of the laser.

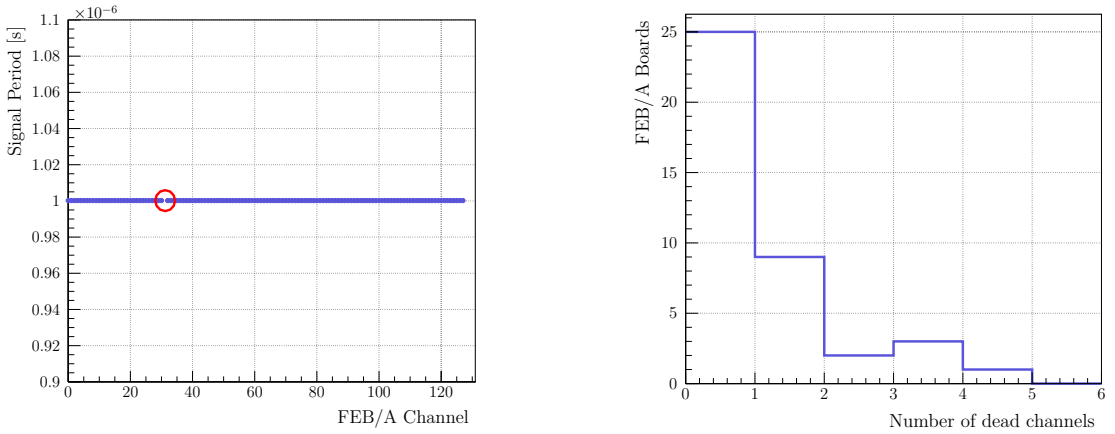
7.2.2 Measurement Procedure

Figure 7.3 shows a diagram of the used test procedure to find the correct bias settings. From the experience gained during the characterization measurements of the chip, a default configuration file is provided, which defines initial parameter values for the analog channels and the TDC modules. For most channels, only a single parameter of the analog readout channel and the TDC module has to be tuned to achieve a working configuration.

In the first step, the number of recorded events by the readout channel is evaluated. If the channel does not respond to the laser pulses, the bias setting of the CML logic cells in the Hit Logic unit of the analog channel is adjusted. In the case that no working bias configuration is found for the channel, it is marked as broken in the resulting configuration file.

Once the channel records events, the signal period is measured to determine whether the corresponding PLL circuit is locked to the external reference frequency. If the measured period does not match the period of the laser pulses, the PLL is not locked and the bias voltage of the VCO elements has to be adjusted. The test program automatically determines from the measured period if the VCO frequency has to be increased or decreased and adjusts the bias setting accordingly. Because the Timebase unit of the TDC is shared by 32 channels, the locking procedure is only performed once for each group of channels sharing a PLL in the ASIC. For the subsequent channels, the period measurement is only analyzed to confirm the correct functionality of the channel. After the PLL is locked the laser is moved to the position of the next readout channel and the procedure is repeated. In this way, the default

[4]ALS PiLas Laser System



(a) Measured signal periods by the FEB/A channels.

(b) Dead channels per board found by the automatic characterization.

Figure 7.4: Test results of the FEB/A production.

configuration file is iteratively changed to receive working bias settings for the full chip.

After the characterization has finished for both mounted ASICs, a report of all failing channels on the board is created. The ROOT files containing the recorded events at each laser position are saved in a database, together with the report, final configuration files and the serial number of the tested board.

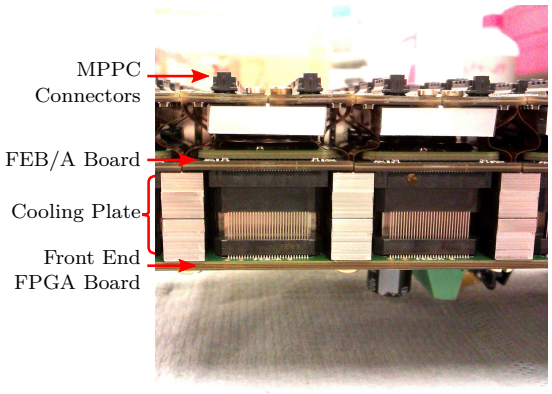
7.2.3 Test Results

Figure 7.4a shows the periods measured by the individual channels of a single FEB/A module during the characterization. Only channel 31 could not be configured automatically and is presumed broken. In all other channels, the correct laser pulse period of 1 μs has been recorded showing that all four PLLs on the board are locked and the channels are functional. Based on this evaluation, the number of dead channels per FEB/A board has been determined and is plotted in Figure 7.4b. In total, only 26 out of 5120 tested channels distributed on 15 different FEB/A boards were found to be broken. The produced boards and the corresponding configuration files have been transferred to DESY[5] Hamburg for the integration in the outer plate.

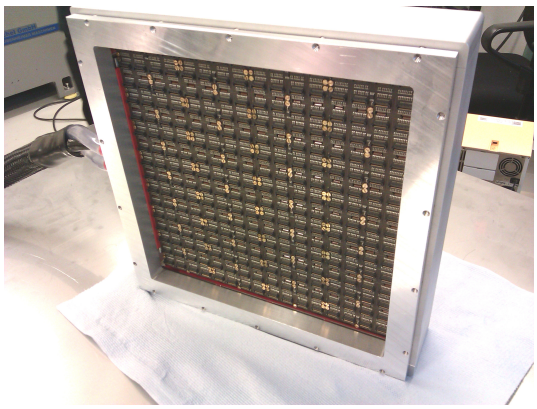
7.3 Detector Assembly and Commissioning

The commission of the outer plate encompasses the mechanical assembly of all 32 readout modules in the detector system, as well as the adaptation of the DAQ system developed at LIP to interface with the STiC ASIC. The mechanical assembly of the system took place at

[5]Deutsches Elektron Synchrotron



(a) Side view showing the layers of the detector system.



(b) Fully assembled outer plate with 32 FEB/A boards before the mounting of the detector modules.

Figure 7.5: Mechanical assembly of the external plate.

DESY Hamburg and the system was shipped afterwards to CERN for the final commissioning together with the endoscopic probe.

7.3.1 Mechanical Assembly

Figure 7.5a shows the mechanical integration of the STiC3 ASICs in the outer PET plate. The flexible parts of the FEB/A PCBs are folded and fixed to a mechanical holder to create the two PCB layers, with the uppermost layer containing the connectors for the detector modules. The folded modules are mounted on an aluminium cooling plate, which contacts the thermal pads of the MCM modules through the cutout of the FEB/A boards. The plate uses a water cooling system to transfer the heat generated by the chips and DAQ boards to an external chiller unit, which cools the water to 18 °C. In the last PCB layer, the FPGA boards of the DAQ system are mounted, which are used to communicate with the ASICs and to transfer data between the DAQ PC and the chips. The fully assembled outer plate, before the mounting of the detector modules, can be seen in Figure 7.5b. After the detector modules are assembled, the front and backside of the plate are closed to create a fully sealed detector system for the use in a medical operation room.

7.3.2 DAQ System

The FPGA front end boards (FEB/D) have been developed at LIP and provide the necessary infrastructure for the operation of eight FEB/A boards. Four of these boards are combined in the outer plate to control the 32 readout modules of the detector system. The board provides the necessary 1.8 V and 3.3 V power supply for the chips and a high voltage DAC modules to generate the bias voltage for the SiPM matrices. The system uses a low jitter clock multiplier to synchronize the reference clock of the TDC units between all FEB/A boards and the

readout electronics in the endoscopic probe. Instead of a reference frequency of 622.08 MHz, which was used during the characterization measurements, a frequency of 640 MHz is provided by the FEB/D boards to allow a synchronization between the endoscopic detector head and the outer PET plate. The configuration and data readout of the 16 connected STiC ASICs is handled by a Kintex 7 FPGA. The existing digital modules, which have been developed during this thesis to perform this task and to communicated with the temperature sensor, have been provided to LIP for the implementation in the firmware of the FEB/D FPGA.

Based on the experience gained during the automatic characterization of the FEB/A modules, several additional software tools have been provided to the DAQ system to facilitate the operation of the STiC ASICs with the FEB/D. These include software for the configuration of the chips, tests of the state of the TDC PLLs and the automatic adjustments of configuration parameters such as the E-Trigger thresholds of the channels to achieve a more uniform ToT response from the detector system in the energy measurements.

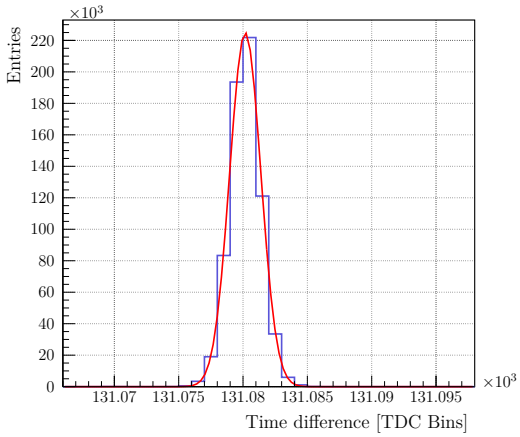
7.3.3 Preliminary Functionality Tests

During the first commissioning of the system, several issues in the readout system have been found and solved. First tests of the system have been conducted to check if the produced boards are operational in the outer plate. During these very early tests, only one FEB/D module was fully operational and has been used for the measurements.

As has been described earlier, the state of the PLL can be determined by triggering the TDC channel over the debug ports with a fixed period. Figure 7.6a shows the measurement of a trigger signal with a period of 6.4 μs. The fit of a Gauss function to the distribution allows to calculate the VCO frequency and yields 640.04 MHz, which shows that the PLL can lock to the reference frequency of the FEB/D board.

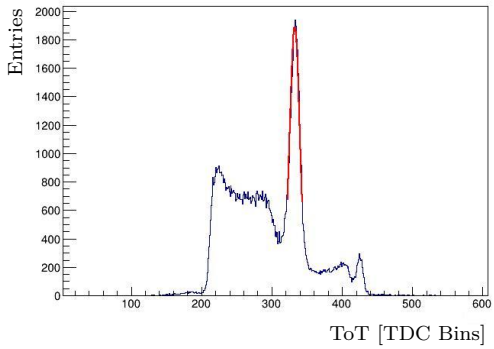
To test the full detector chain, a radioactive ^{22}Na point source has been placed in four different positions in front of the detector modules, as it is shown in Figure 7.6b. With the outer plate, the energy spectra and the number of recorded events per channel have been measured. An example of a measured spectrum can be seen in Figure 7.6c. As in the characterization measurements, the 511 keV and the 1.275 MeV photopeaks of the ^{22}Na decay are clearly visible. The four positions, where the source has been placed, can be clearly distinguished by the number of recorded events. Since the detector head of the endoscopic probe was not yet functional, no coincidence measurements could be performed at this early commissioning stage to evaluate the timing performace of the chip in the final system.

The measurements show that the produced FEB/A boards are functional in the outer plate detector system. After the commissioning at CERN, the full system including the endoscopic probe, was shipped to Marseille in January 2015 to be used in the first preclinical tests. During these measurements, the performance of the full detector system will be evaluated.

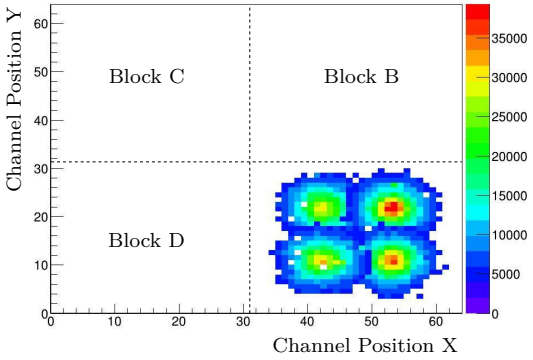


(a) Measured signal period for injected trigger signals with a period of 6.4 μs.

(b) Fully closed outer plate with a ^{22}Na source.



(c) Example of a measured energy spectrum.



(d) Number of recorded events in block A.

Figure 7.6: Preliminary test of the functionality of the detector system performed by EndoTOFPET members during the commissioning effort at CERN.

Chapter 8

Conclusion and Outlook

Since their development, Silicon Photomultiplier have become a popular choice for the detection of scintillation light in particle detectors. However, their full potential in terms of timing resolution has not yet been exploited in the detector systems, due to a lack of suitable highly integrated readout electronics. The STiC ASIC has been developed in the framework of the EndoTOFPET-US project to rectify this situation and provide a mixed-mode readout solution for high precision timing measurements with SiPMs.

To achieve this goal, the analog input stage of the chip has been optimized in the course of three chip generations to generate a low jitter trigger signal for the timing measurement of the SiPM current pulse. The charge information of the signal is evaluated using a linearized Time over Threshold method, allowing to measure both, time and energy with a single TDC. The developed analog readout channel has been integrated together with a high precision TDC module and digital core logic in a mixed-mode ASIC. The communication interfaces for the transmission of the digitized event information and the configuration of the chip has been devised according to the specifications of the EndoTOFPET-US DAQ system. In the course of this thesis, the digital core logic and the mixed-signal back-end design of two STiC generations have been designed and characterized. With STiC2, a 16 channel prototype was developed to verify the performance and functionality of the chosen readout structure. In the third generation of the chip, which has been presented in this thesis, 64 of the readout channels have been integrated on a $5 \times 5\,\mathrm{mm}^2$ die using the UMC $0.18\,\mu\mathrm{m}$ CMOS technology.

During all performed measurements, the chips have been operated by a dedicated DAQ system, which has been developed as part of this thesis. The results of the electrical characterization of the chip are consistent with circuit simulations and the performance of the TDC module is in accordance with measurements conducted at ZITI Heidelberg. The performance of the chip for timing measurements with SiPMs has been evaluated in coincidence measurements using $3.1 \times 3.1 \times 15\,\mathrm{mm}^3$ LYSO scintillator crystals glued to 4×4 SiPM arrays from Hamamatsu. The good energy resolution of the implemented linearized ToT method could be verified by the measurement of the ^{22}Na decay spectra, showing an energy resolution of 15 % for the 511 keV photopeak. This exceeds the specifications of the PET detector system, which requires an energy resolution of 20 %. The achieved CTR of less than 215 ps FWMH at 18 °C ambient temperature is among the best values achieved for the time resolution to date in coincidence measurements using SiPM sensors coupled to LYSO crystals.

The conducted characterization measurements in this thesis have been focused on establishing a well defined readout system and verifying the performance of the chip. Therefore the

full parameter range of the ASIC and several of its implemented features have not yet been investigated. Further improvements in the time resolution can be expected when performing exhaustive and systematic scans of the chip configurations. The developed system also serves as a basis to investigate many interesting aspects of timing measurements with SiPMs, such as the single pixel time resolution of the sensors, the impact of a tail cancellation on the time resolution and the improvement of a differential readout scheme with respect to a single-ended sensor readout.

For the commissioning of the EndoTOFPET-US detector system, the STiC ASIC has been integrated in specially designed readout modules, providing 128 SiPM readout channels. Before the assembly in the outer plate, the functionality of each produced module has been verified in an automated test stand. The detector system has been fully equipped with 32 readout modules, providing the required 4096 readout channels. Preliminary tests during the commissioning of the system show that the modules are functional after the assembly in the outer plate. The performance of the full PET system is currently being evaluated in first preclinical tests at CERIMED in Marseille.

Although the STiC ASIC has been developed for the use in Time-of-Flight PET systems, the high timing resolution it provides is a common requirement for many particle detectors. Consequently, the chip is currently being evaluated for the application in several different projects. STiC has also been chosen as the baseline design of the Mu3e experiment for the readout of the scintillating fibre tracker and the tile detector. In this context, a new version of the STiC ASIC is being developed, which aims to provide a fast serial link with a bandwidth of more than 1 GBit/s for the transmission of the event data. In this way, the maximum event rate of the chip will be increased to handle even rates of up to 1 MHz per channel.

With the continuous addition of features in each generation, STiC becomes a viable readout solution for an even broader range of detector systems. Therefore, the chip has the potential to become the first choice for particle detectors requiring high precision timing measurements with SiPMs.

Appendix A

Mixed Signal Design

A.1 Hit Receiver module

The first stage of the data processing is the recording of TDC data and the assignment of subsequent T-Trigger and E-Trigger timestamps to a common event. This functionality is implemented in the hit receiver entities. Figure A.1 shows a simplified block level diagram of this module. The timestamps recorded for each trigger signal of the analog channel by the TDC module is stored in two subsequent register stages R1 and R2. With each new trigger signal, the previous timestamp is moved to the register stage R2 and the new data is stored in the first Flip-Flop stage. During the data transfer from R1 to the subsequent registers, the fine counter value, which is at this point still represented by its thermometric code, is converted to the corresponding 5 bit binary number.

The register stages have been arranged in Flip-Flop columns using Structured Data Paths (SDP) available in the back-end tools. The definition of a single Flip-Flop column is shown below:

```
1  VERSION 1
2  datapath ch_hit_recv {
3      row register_l1 {
4          justifyBy SW
5          column  data_reg1_0_mux {
6              justifyBy SW
7              inst data_reg1_reg_0__U4
8              inst data_reg1_reg_1__U4
9              inst data_reg1_reg_2__U4
10             inst data_reg1_reg_3__U4
11             inst data_reg1_reg_4__U4
12             inst data_reg1_reg_5__U4
13             inst data_reg1_reg_6__U4
14             inst data_reg1_reg_7__U4
15             inst data_reg1_reg_8__U4
16             inst data_reg1_reg_9__U4
17             inst data_reg1_reg_10__U4
18             inst data_reg1_reg_11__U4
19             inst data_reg1_reg_12__U4
20             inst data_reg1_reg_13__U4
21             inst data_reg1_reg_14__U4
```

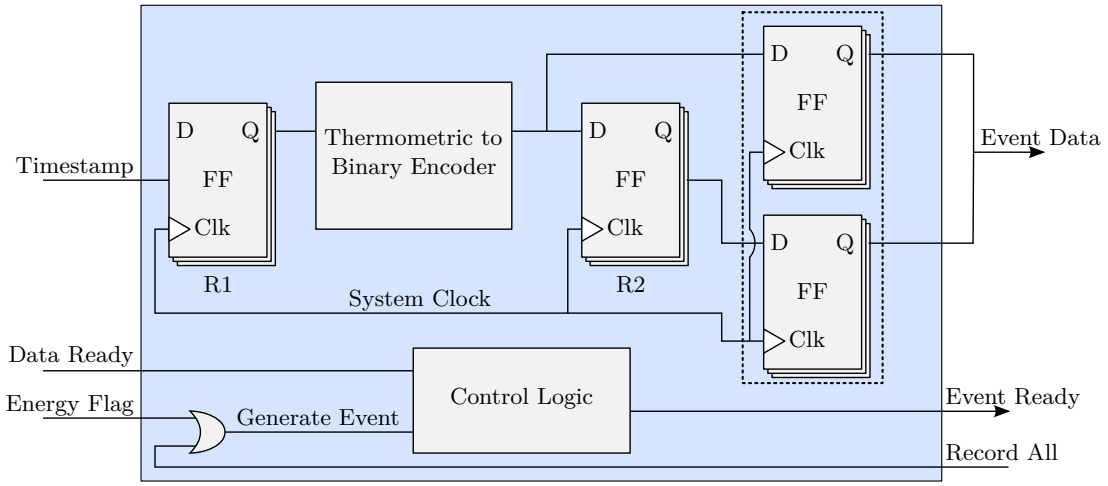


Figure A.1: Block level diagram of the hit receiver module.

```
22              inst data_reg1_reg_15__U4
23          }
24          column  data_reg1_0 {
25              justifyBy SW
26              inst data_reg1_reg_0_
27              inst data_reg1_reg_1_
28              inst data_reg1_reg_2_
29              inst data_reg1_reg_3_
30              inst data_reg1_reg_4_
31              inst data_reg1_reg_5_
32              inst data_reg1_reg_6_
33              inst data_reg1_reg_7_
34              inst data_reg1_reg_8_
35              inst data_reg1_reg_9_
36              inst data_reg1_reg_10_
37              inst data_reg1_reg_11_
38              inst data_reg1_reg_12_
39              inst data_reg1_reg_13_
40              inst data_reg1_reg_14_
41              inst data_reg1_reg_15_
42          }
43
44      }
45
46  }
```

In the back-end design, this definition is used to arrange the Flip-Flops in the desired columns, as it is shown in figure A.2. With the organized structure, the routing of the clock signal and the interconnection between the register stages becomes more uniform than for an automatic placement of the cells.

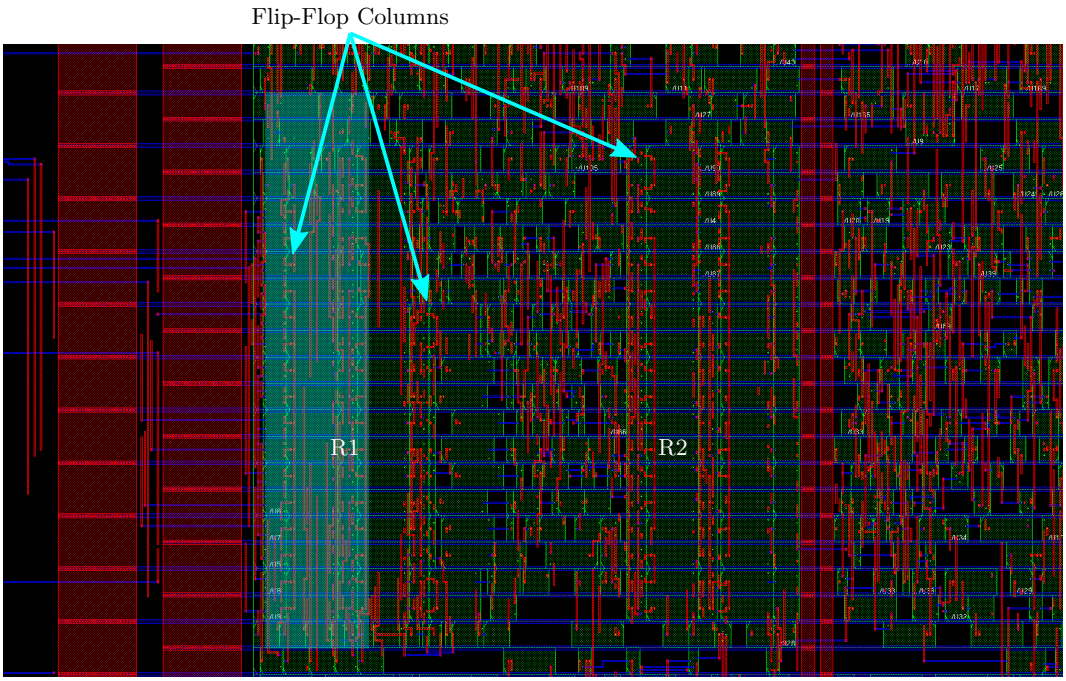


Figure A.2: Resulting placement of the register stages using Structured Data paths

A.2 STiC Timing Constraints

The clock and signal timing is defined in Synopsis Design Contraint files. The constraint definitions for the clock signals, digital input and output ports and timing exceptions are provided below.

A.2.1 Clock Signal Definitions

```
##############################################################################
#
# spi CLK (50 MHz)
# root port : sclk
# name      : spi_clk
# sources   : clock for spi
#
# system CLK (160 MHz)
# root port : sclk
# name      : sys_clk
# sources   : clock for system

#FOR THE DIFFERENTIAL INPUT CLOCK TAKE THE PORT AFTER THE LVDS RECEIVER
create_clock -name "sys_clk" -period 5.8 [get_pin {u_lvds_clk/OP}]
#FOR THE SPI CLOCK TAKE THE PORT AT THE INPUT OF THE PAD
create_clock -name "spi_clk" -period 20 [get_pin {pad_sclk/O}]
```

```
set_clock_latency 1.0 [get_clocks {sys_clk}]
set_clock_uncertainty -setup 0.4 [get_clocks {sys_clk}]
set_clock_uncertainty -hold 0.25 [get_clocks {sys_clk}]
set_clock_transition  0.4  [get_clocks {sys_clk}]
set_clock_latency -min  1.0 [get_clocks {sys_clk}]
set_clock_latency -max  1.8     [get_clocks {sys_clk}]

set_clock_transition  0.4  [get_clocks {spi_clk}]
set_clock_uncertainty  0.4  [get_clocks {spi_clk}]
set_clock_latency -max  1.8  [get_clocks {spi_clk}]
set_clock_latency -min  1.4  [get_clocks {spi_clk}]

#==CREATE THE GENERATED CLOCKS
create_generated_clock -source [get_pin {u_lvds_clk/OP}] -name "div_clk"
-divide_by 10 [get_pin {u_digital_all/unit_frame_gen/cdiv/q_reg/Q}]

create_generated_clock -divide_by 10 -source [get_pin {u_lvds_clk/OP}]
-name "div_clk_delay" [get_pin {u_digital_all/unit_frame_gen/cdiv/q_delay_reg/Q}]

set_clock_transition  0.4  [get_clocks {div_clk}]
set_clock_transition  0.4  [get_clocks {div_clk_delay}]
```

A.2.2 Timing Constraints for the Digital Ports

```
##############################################################################
# Define default IO Load

set_load 10 [all_outputs]
set_load 25 [all_inputs]



##############################################################################
#Define the input to clock delays of the TDC ouputs and the SPI


##The digital input signal will become valid after min 8 and max 12 ns
# after the rising edge of the clock signal

set_input_delay -min 10 -clock spi_clk [get_port {di_sdi}]
set_input_delay -max 12 -clock spi_clk [get_port {di_sdi}]

set_input_delay -min 10 -clock spi_clk [get_port {di_cs}]
```

```
set_input_delay -max 12 -clock spi_clk [get_port {di_cs}]

set_input_delay -min 10 -clock spi_clk [get_port {di_debug_cs}]
set_input_delay -max 12 -clock spi_clk [get_port {di_debug_cs}]

set_input_delay -min 1.0 -clock sys_clk [get_port {di_rst}]
set_input_delay -max 3.0 -clock sys_clk [get_port {di_rst}]
```

A.2.3 Definition of Asynchronous Clock Domains

```
##############################################################################
# Set asynchronous false paths

#==SEPERATE THE CLOCK NETS
set_false_path -from [get_clocks {sys_clk}]
               -to [get_clocks {spi_clk}]

set_false_path -from [get_clocks {spi_clk}]
               -to [get_clocks {sys_clk}]

#==SET FALSE PATHS FROM THE SPI CLOCK TO THE DIVIDED CLOCKS
set_false_path -from [get_clocks {spi_clk}]
               -to [get_clocks {div_clk}]

set_false_path -from [get_clocks {spi_clk}]
               -to [get_clocks {div_clk_delay}]

#==SET THE ASYNC FALSE PATHS
set_false_path -from [get_pins {u_digital_all/i_tdc_data*}]
               -to [get_clocks {sys_clk}]
set_false_path -from [get_pins {u_digital_all/i_tdc_strobe*}]
               -to [get_clocks {sys_clk}]

set_false_path -from [get_pins {u_digital_all/i_tdc_energy_flag*}]
               -to [get_clocks {sys_clk}]


set_false_path -from [get_clocks {spi_clk}] -to [get_pins {u_analog_channel_*/*}]


##SET A FALSE PATH TO THE MONITORING OUTPUTS
set_false_path -to [get_ports {do_debug_mon*}]


####################################
```

```
### set dont touch networks to prevent buffering of the nets

set_dont_touch_network [get_pins u_SUSDAC_*/VN*]

set_dont_touch_network [get_pins u_pll1_left/RefP]
set_dont_touch_network [get_pins u_pll1_left/RefN]

set_dont_touch_network [get_pins u_pll1_left/VCOMonitor]
set_dont_touch_network [get_pins u_pll1_left/PLLFilter*]

set_dont_touch_network [get_pins u_pll1_left/CC*]
set_dont_touch_network [get_pins u_pll1_left/T*]

set_dont_touch_network [get_pins u_pll2_right/RefP]
set_dont_touch_network [get_pins u_pll2_right/RefN]

set_dont_touch_network [get_pins u_pll2_right/VCOMonitor]
set_dont_touch_network [get_pins u_pll2_right/PLLFilter*]

set_dont_touch_network [get_pins u_pll2_right/CC*]
set_dont_touch_network [get_pins u_pll2_right/T*]

set_dont_touch_network [get_pins u_analog_channel_*/Q]
set_dont_touch_network [get_pins u_analog_channel_*/QN]
set_dont_touch_network [get_pins u_analog_channel_*/flagN]
set_dont_touch_network [get_pins u_analog_channel_*/flag]

set_dont_touch_network [get_pins u_lvds_transmitter_DC1v2/DCcommon]

set_dont_touch_network [get_pins u_dig_mon*/pbias]
set_dont_touch_network [get_pins u_dig_mon*/nbias]

set_dont_touch_network [get_pins u_ana_mon*/monitor_*]
```

Appendix B

STiC Configuration Files

Because of the large parameter space, the files for the different measurements are shortened to show only the relevant settings for the corresponding measurement.

B.1 Maximum Event Rate and TDC Characterization Measurement

Parameter Name	Hex Value	Parameter Name	Hex Value
O_GEN_IDLE_SIGNAL	1	MS_LIMITS_LEFT_TDC	0
MS_LIMITS_RIGHT_TDC	0	MS_SWITCH_SEL	0
MS_DEBUG	0	MS_RECV_REC_ALL	1
PLL1_SETCOARSE	0	PLL2_SETCOARSE	0
PLL1_ENVCOMONITOR	0	PLL2_ENVCOMONITOR	0
DISABLE_COARSE	0	DAC_CHANNEL_MASK_CH0	0
ANODE_FLAG_CH0	0	CATHODE_FLAG_CH0	0
S_SWITCH_CH0	0	SORD_CH0	0
SORD_NOT_CH0	0	EDGE_CH0	0
EDGE_CML_CH0	0	DAC_CMLSCALE_CH0	1
DMON_ENA_CH0	0	DMON_SW_CH0	0
TDCTEST_CH0	0	AMON_CTRL_CH0	0
COMP_SPI_CH0	0	DAC_SIPM_SC_CH0	0
DAC_SIPM_CH0	0	DAC_TTHRESH_SC_CH0	0
DAC_TTHRESH_CH0	0	DAC_AMPCOM_SC_CH0	0
DAC_AMPCOM_CH0	0	DAC_INPUTBIAS_SC_CH0	0
DAC_INPUTBIAS_CH0	0	DAC_ETHRESH_CH0	ff
DAC_POLE_SC_CH0	0	DAC_POLE_CH0	0
DAC_CML_CH0	0	DAC_DELAY_CH0	0
DAC_DELAY_BIT1_CH0	0	DAC_TDC_LEFT_VND2C_SCALE	0
DAC_TDC_LEFT_VND2C_OFFSET	3	DAC_TDC_LEFT_VND2C	1f
DAC_TDC_LEFT_VNCntBuffer_SCALE	0	DAC_TDC_LEFT_VNCntBuffer_OFFSET	3
DAC_TDC_LEFT_VNCntBuffer	7	DAC_TDC_LEFT_VNCnt_SCALE	0
DAC_TDC_LEFT_VNCnt_OFFSET	3	DAC_TDC_LEFT_VNCnt	1e
DAC_TDC_LEFT_VNPCP_SCALE	0	DAC_TDC_LEFT_VNPCP_OFFSET	3
DAC_TDC_LEFT_VNPCP	18	DAC_TDC_LEFT_VNVCODELAY_SCALE	0
DAC_TDC_LEFT_VNVCODELAY_OFFSET	3	DAC_TDC_LEFT_VNVCODELAY	c
DAC_TDC_LEFT_VNVCOBUFFER_SCALE	0	DAC_TDC_LEFT_VNVCOBUFFER_OFFSET	0
DAC_TDC_LEFT_VNVCOBUFFER	0	DAC_TDC_LEFT_VNHITLOGIC_SCALE	0
DAC_TDC_LEFT_VNHITLOGIC_OFFSET	3	DAC_TDC_LEFT_VNHITLOGIC	1b
DAC_TDC_LEFT_VNPFC_SCALE	0	DAC_TDC_LEFT_VNPFC_OFFSET	3
DAC_TDC_LEFT_VNPFC	8	DAC_TDC_LATCHBIAS_LEFT	708
DIG_MON1_EN_LEFT	0	DIG_MON1_DAC_LEFT	0
DIG_MON2_EN_LEFT	0	DIG_MON2_DAC_LEFT	0

Table B.1: Configuration parameters for the injection of trigger signals to TDC channel 0. The configuration has been used during the data rate and TDC characterizations.

B.2 T-Threshold and T-Trigger Jitter Scan

Parameter Name	Hex Value	Parameter Name	Hex Value
O_GEN_IDLE_SIGNAL	1	MS_LIMITS_LEFT_TDC	0
MS_LIMITS_RIGHT_TDC	0	MS_SWITCH_SEL	0
MS_DEBUG	0	MS_RECV_REC_ALL	1
PLL1_SETCOARSE	0	PLL2_SETCOARSE	0
PLL1_ENVCOMONITOR	0	PLL2_ENVCOMONITOR	0
DAC_CHANNEL_MASK_CH22	0	ANODE_FLAG_CH22	1
CATHODE_FLAG_CH22	1	S_SWITCH_CH22	1
SORD_CH22	1	SORD_NOT_CH22	0
EDGE_CH22	1	EDGE_CML_CH22	0
DAC_CMLSCALE_CH22	0	DMON_ENA_CH22	0
DMON_SW_CH22	0	TDCTEST_CH22	1
AMON_CTRL_CH22	0	COMP_SPI_CH22	0
DAC_SIPM_SC_CH22	0	DAC_SIPM_CH22	16
DAC_TTHRESH_SC_CH22	0	DAC_TTHRESH_CH22	a
DAC_AMPCOM_SC_CH22	2	DAC_AMPCOM_CH22	0
DAC_INPUTBIAS_SC_CH22	0	DAC_INPUTBIAS_CH22	3
DAC_ETHRESH_CH22	0	DAC_POLE_SC_CH22	0
DAC_POLE_CH22	3f	DAC_CML_CH22	3
DAC_DELAY_CH22	0	DAC_DELAY_BIT1_CH22	0
DISABLE_COARSE	0	DAC_TDC_LEFT_VND2C_SCALE	0
DAC_TDC_LEFT_VND2C_OFFSET	3	DAC_TDC_LEFT_VND2C	1f
DAC_TDC_LEFT_VNCntBuffer_SCALE	0	DAC_TDC_LEFT_VNCntBuffer_OFFSET	3
DAC_TDC_LEFT_VNCntBuffer	d	DAC_TDC_LEFT_VNCnt_SCALE	0
DAC_TDC_LEFT_VNCnt_OFFSET	1	DAC_TDC_LEFT_VNCnt	14
DAC_TDC_LEFT_VNPCP_SCALE	0	DAC_TDC_LEFT_VNPCP_OFFSET	2
DAC_TDC_LEFT_VNPCP	1b	DAC_TDC_LEFT_VNVCODELAY_SCALE	0
DAC_TDC_LEFT_VNVCODELAY_OFFSET	3	DAC_TDC_LEFT_VNVCODELAY	24
DAC_TDC_LEFT_VNVCOBUFFER_SCALE	1	DAC_TDC_LEFT_VNVCOBUFFER_OFFSET	2
DAC_TDC_LEFT_VNVCOBUFFER	f	DAC_TDC_LEFT_VNHITLOGIC_SCALE	0
DAC_TDC_LEFT_VNHITLOGIC_OFFSET	3	DAC_TDC_LEFT_VNHITLOGIC	10
DAC_TDC_LEFT_VNPFC_SCALE	0	DAC_TDC_LEFT_VNPFC_OFFSET	2
DAC_TDC_LEFT_VNPFC	d	DAC_TDC_RIGHT_VND2C_SCALE	0
DAC_TDC_RIGHT_VND2C_OFFSET	3	DAC_TDC_RIGHT_VND2C	3f
DAC_TDC_RIGHT_VNCntBuffer_SCALE	0	DAC_TDC_RIGHT_VNCntBuffer_OFFSET	3
DAC_TDC_RIGHT_VNCntBuffer	3f	DAC_TDC_RIGHT_VNCnt_SCALE	0
DAC_TDC_RIGHT_VNCnt_OFFSET	3	DAC_TDC_RIGHT_VNCnt	3f
DAC_TDC_RIGHT_VNPCP_SCALE	0	DAC_TDC_RIGHT_VNPCP_OFFSET	3
DAC_TDC_RIGHT_VNPCP	3f	DAC_TDC_RIGHT_VNVCODELAY_SCALE	0
DAC_TDC_RIGHT_VNVCODELAY_OFFSET	3	DAC_TDC_RIGHT_VNVCODELAY	3f
DAC_TDC_RIGHT_VNVCOBUFFER_SCALE	0	DAC_TDC_RIGHT_VNVCOBUFFER_OFFSET	3
DAC_TDC_RIGHT_VNVCOBUFFER	3f	DAC_TDC_RIGHT_VNHITLOGIC_SCALE	0
DAC_TDC_RIGHT_VNHITLOGIC_OFFSET	3	DAC_TDC_RIGHT_VNHITLOGIC	3f
DAC_TDC_RIGHT_VNPFC_SCALE	0	DAC_TDC_RIGHT_VNPFC_OFFSET	3
DAC_TDC_RIGHT_VNPFC	3f	DAC_TDC_LATCHBIAS_LEFT	708
DAC_TDC_LATCHBIAS_RIGHT	0	AMON_LEFT_EN	0
AMON_LEFT_DAC	0	AMON_RIGHT_EN	0
AMON_RIGHT_DAC	0	DIG_MON1_EN_LEFT	1
DIG_MON1_DAC_LEFT	e6	DIG_MON1_EN_RIGHT	0
DIG_MON1_DAC_RIGHT	0	DIG_MON2_EN_LEFT	0
DIG_MON2_DAC_LEFT	0	DIG_MON2_EN_RIGHT	0
DIG_MON2_DAC_RIGHT	0		

Table B.2: Configuration parameters during the charge injection measurements for the characterization of the T-Trigger threshold and jitter. The DAC_TTHRESH parameter has been varied during the measurement.

B.3 Characterization of the E-Trigger Response

Parameter Name	Hex Value	Parameter Name	Hex Value
O_GEN_IDLE_SIGNAL	1	MS_LIMITS_LEFT_TDC	0
MS_SWITCH_SEL	0	MS_DEBUG	0
MS_RECV_REC_ALL	0	PLL1_SETCOARSE	0
PLL1_ENVCOMONITOR	0	DISABLE_COARSE	0
DAC_CHANNEL_MASK_CH25	1	ANODE_FLAG_CH25	1
CATHODE_FLAG_CH25	1	S_SWITCH_CH25	1
SORD_CH25	1	SORD_NOT_CH25	0
EDGE_CH25	1	EDGE_CML_CH25	0
DAC_CMLSCALE_CH25	1	DMON_ENA_CH25	1
DMON_SW_CH25	0	TDCTEST_CH25	1
AMON_CTRL_CH25	0	COMP_SPI_CH25	3

Parameter Name	Hex Value	Parameter Name	Hex Value
DAC_SIPM_SC_CH25	0	DAC_SIPM_CH25	17
DAC_TTHRESH_SC_CH25	0	DAC_TTHRESH_CH25	a
DAC_AMPCOM_SC_CH25	2	DAC_AMPCOM_CH25	0
DAC_INPUTBIAS_SC_CH25	0	DAC_INPUTBIAS_CH25	3
DAC_ETHRESH_CH25	88	DAC_POLE_SC_CH25	0
DAC_POLE_CH25	3f	DAC_CML_CH25	1
DAC_DELAY_CH25	1	DAC_DELAY_BIT1_CH25	0
DAC_TDC_LEFT_VND2C_SCALE	0	DAC_TDC_LEFT_VND2C_OFFSET	3
DAC_TDC_LEFT_VND2C	1d	DAC_TDC_LEFT_VNCntBuffer_SCALE	0
DAC_TDC_LEFT_VNCntBuffer_OFFSET	3	DAC_TDC_LEFT_VNCntBuffer	8
DAC_TDC_LEFT_VNCnt_SCALE	0	DAC_TDC_LEFT_VNCnt_OFFSET	3
DAC_TDC_LEFT_VNCnt	1f	DAC_TDC_LEFT_VNPCP_SCALE	0
DAC_TDC_LEFT_VNPCP_OFFSET	2	DAC_TDC_LEFT_VNPCP	1b
DAC_TDC_LEFT_VNVCODELAY_SCALE	0	DAC_TDC_LEFT_VNVCODELAY_OFFSET	3
DAC_TDC_LEFT_VNVCODELAY	21	DAC_TDC_LEFT_VNVCOBUFFER_SCALE	1
DAC_TDC_LEFT_VNVCOBUFFER_OFFSET	2	DAC_TDC_LEFT_VNVCOBUFFER	f
DAC_TDC_LEFT_VNHITLOGIC_SCALE	0	DAC_TDC_LEFT_VNHITLOGIC_OFFSET	3
DAC_TDC_LEFT_VNHITLOGIC	10	DAC_TDC_LEFT_VNPFC_SCALE	0
DAC_TDC_LEFT_VNPFC_OFFSET	2	DAC_TDC_LEFT_VNPFC	d
DAC_TDC_LATCHBIAS_LEFT	708		

Table B.3: Configuration parameters during the charge injection measurements for the characterization of the E-Trigger response. The DAC_ETHRESH parameter has been varied during the measurement.

B.4 SiPM Bias DAC Scan

Parameter Name	Hex Value	Parameter Name	Hex Value
DAC_CHANNEL_MASK_CH16	0	ANODE_FLAG_CH16	1
CATHODE_FLAG_CH16	1	S_SWITCH_CH16	1
SORD_CH16	1	SORD_NOT_CH16	0
EDGE_CH16	1	EDGE_CML_CH16	0
DAC_CMLSCALE_CH16	0	DMON_ENA_CH16	0
DMON_SW_CH16	0	TDCTEST_CH16	1
AMON_CTRL_CH16	0	COMP_SPI_CH16	0
DAC_SIPM_SC_CH16	0	DAC_SIPM_CH16	0
DAC_TTHRESH_SC_CH16	0	DAC_TTHRESH_CH16	20
DAC_AMPCOM_SC_CH16	2	DAC_AMPCOM_CH16	0
DAC_INPUTBIAS_SC_CH16	0	DAC_INPUTBIAS_CH16	0
DAC_ETHRESH_CH16	ff	DAC_POLE_SC_CH16	0
DAC_POLE_CH16	0	DAC_CML_CH16	0
DAC_DELAY_CH16	0	DAC_DELAY_BIT1_CH16	0

Table B.4: Configuration parameters for the SiPM Bias DAC scan.

B.5 Coincidence Measurements

Parameter Name	Hex Value	Parameter Name	Hex Value
O_GEN_IDLE_SIGNAL	1	MS_LIMITS_LEFT_TDC	0
MS_LIMITS_RIGHT_TDC	0	MS_SWITCH_SEL	0
MS_DEBUG	0	MS_RECV_REC_ALL	0
PLL1_SETCOARSE	0	PLL2_SETCOARSE	0
PLL1_ENVCOMONITOR	0	PLL2_ENVCOMONITOR	0
DISABLE_COARSE	0	ANODE_FLAG_CH33	1
CATHODE_FLAG_CH33	1	S_SWITCH_CH33	1
SORD_CH33	1	SORD_NOT_CH33	0
EDGE_CH33	1	EDGE_CML_CH33	0
DAC_CMLSCALE_CH33	0	DMON_ENA_CH33	0
DMON_SW_CH33	0	TDCTEST_CH33	1
AMON_CTRL_CH33	0	COMP_SPI_CH33	3
DAC_SIPM_SC_CH33	0	DAC_SIPM_CH33	11
DAC_TTHRESH_SC_CH33	0	DAC_TTHRESH_CH33	f
DAC_AMPCOM_SC_CH33	2	DAC_AMPCOM_CH33	9
DAC_INPUTBIAS_SC_CH33	0	DAC_INPUTBIAS_CH33	3

Parameter Name	Hex Value	Parameter Name	Hex Value
DAC_ETHRESH_CH33	69	DAC_POLE_SC_CH33	0
DAC_POLE_CH33	3f	DAC_CML_CH33	7
DAC_DELAY_CH33	1	DAC_DELAY_BIT1_CH33	0
DAC_CHANNEL_MASK_CH33	1	ANODE_FLAG_CH20	1
CATHODE_FLAG_CH20	1	S_SWITCH_CH20	1
SORD_CH20	1	SORD_NOT_CH20	0
EDGE_CH20	1	EDGE_CML_CH20	0
DAC_CMLSCALE_CH20	0	DMON_ENA_CH20	0
DMON_SW_CH20	0	TDCTEST_CH20	1
AMON_CTRL_CH20	0	COMP_SPI_CH20	3
DAC_SIPM_SC_CH20	0	DAC_SIPM_CH20	11
DAC_TTHRESH_SC_CH20	4	DAC_TTHRESH_CH20	1e
DAC_AMPCOM_SC_CH20	2	DAC_AMPCOM_CH20	9
DAC_INPUTBIAS_SC_CH20	0	DAC_INPUTBIAS_CH20	3
DAC_ETHRESH_CH20	7f	DAC_POLE_SC_CH20	0
DAC_POLE_CH20	3f	DAC_CML_CH20	7
DAC_DELAY_CH20	1	DAC_DELAY_BIT1_CH20	0
DAC_CHANNEL_MASK_CH20	1	DAC_TDC_LEFT_VND2C_SCALE	0
DAC_TDC_LEFT_VND2C_OFFSET	3	DAC_TDC_LEFT_VND2C	12
DAC_TDC_LEFT_VNCntBuffer_SCALE	0	DAC_TDC_LEFT_VNCntBuffer_OFFSET	3
DAC_TDC_LEFT_VNCntBuffer	8	DAC_TDC_LEFT_VNCnt_SCALE	0
DAC_TDC_LEFT_VNCnt_OFFSET	2	DAC_TDC_LEFT_VNCnt	14
DAC_TDC_LEFT_VNPCP_SCALE	0	DAC_TDC_LEFT_VNPCP_OFFSET	2
DAC_TDC_LEFT_VNPCP	1b	DAC_TDC_LEFT_VNVCODELAY_SCALE	0
DAC_TDC_LEFT_VNVCODELAY_OFFSET	3	DAC_TDC_LEFT_VNVCODELAY	a
DAC_TDC_LEFT_VNVCOBUFFER_SCALE	0	DAC_TDC_LEFT_VNVCOBUFFER_OFFSET	3
DAC_TDC_LEFT_VNVCOBUFFER	0	DAC_TDC_LEFT_VNHITLOGIC_SCALE	0
DAC_TDC_LEFT_VNHITLOGIC_OFFSET	3	DAC_TDC_LEFT_VNHITLOGIC	0
DAC_TDC_LEFT_VNPFC_SCALE	0	DAC_TDC_LEFT_VNPFC_OFFSET	2
DAC_TDC_LEFT_VNPFC	d	DAC_TDC_RIGHT_VND2C_SCALE	0
DAC_TDC_RIGHT_VND2C_OFFSET	3	DAC_TDC_RIGHT_VND2C	12
DAC_TDC_RIGHT_VNCntBuffer_SCALE	0	DAC_TDC_RIGHT_VNCntBuffer_OFFSET	3
DAC_TDC_RIGHT_VNCntBuffer	8	DAC_TDC_RIGHT_VNCnt_SCALE	0
DAC_TDC_RIGHT_VNCnt_OFFSET	2	DAC_TDC_RIGHT_VNCnt	14
DAC_TDC_RIGHT_VNPCP_SCALE	0	DAC_TDC_RIGHT_VNPCP_OFFSET	2
DAC_TDC_RIGHT_VNPCP	1b	DAC_TDC_RIGHT_VNVCODELAY_SCALE	0
DAC_TDC_RIGHT_VNVCODELAY_OFFSET	3	DAC_TDC_RIGHT_VNVCODELAY	a
DAC_TDC_RIGHT_VNVCOBUFFER_SCALE	0	DAC_TDC_RIGHT_VNVCOBUFFER_OFFSET	3
DAC_TDC_RIGHT_VNVCOBUFFER	0	DAC_TDC_RIGHT_VNHITLOGIC_SCALE	0
DAC_TDC_RIGHT_VNHITLOGIC_OFFSET	3	DAC_TDC_RIGHT_VNHITLOGIC	0
DAC_TDC_RIGHT_VNPFC_SCALE	0	DAC_TDC_RIGHT_VNPFC_OFFSET	2
DAC_TDC_RIGHT_VNPFC	d	DAC_TDC_LATCHBIAS_LEFT	708
DAC_TDC_LATCHBIAS_RIGHT	708		

Table B.5: Configuration parameters for the coincidence measurements during the SiPM bias scan at room temperature.

Parameter Name	Hex Value	Parameter Name	Hex Value
O_GEN_IDLE_SIGNAL	1	MS_LIMITS_LEFT_TDC	0
MS_LIMITS_RIGHT_TDC	0	MS_SWITCH_SEL	0
MS_DEBUG	0	MS_RECV_REC_ALL	0
PLL1_SETCOARSE	0	PLL2_SETCOARSE	0
PLL1_ENVCOMONITOR	0	PLL2_ENVCOMONITOR	0
DISABLE_COARSE	0	ANODE_FLAG_CH33	1
CATHODE_FLAG_CH33	1	S_SWITCH_CH33	1
SORD_CH33	1	SORD_NOT_CH33	0
EDGE_CH33	1	EDGE_CML_CH33	0
DAC_CMLSCALE_CH33	0	DMON_ENA_CH33	0
DMON_SW_CH33	0	TDCTEST_CH33	1
AMON_CTRL_CH33	0	COMP_SPI_CH33	3
DAC_SIPM_SC_CH33	0	DAC_SIPM_CH33	11
DAC_TTHRESH_SC_CH33	0	DAC_TTHRESH_CH33	f
DAC_AMPCOM_SC_CH33	2	DAC_AMPCOM_CH33	9
DAC_INPUTBIAS_SC_CH33	0	DAC_INPUTBIAS_CH33	3
DAC_ETHRESH_CH33	69	DAC_POLE_SC_CH33	0
DAC_POLE_CH33	3f	DAC_CML_CH33	7
DAC_DELAY_CH33	1	DAC_DELAY_BIT1_CH33	0
DAC_CHANNEL_MASK_CH33	1	ANODE_FLAG_CH20	1
CATHODE_FLAG_CH20	1	S_SWITCH_CH20	1
SORD_CH20	1	SORD_NOT_CH20	0
EDGE_CH20	1	EDGE_CML_CH20	0
DAC_CMLSCALE_CH20	0	DMON_ENA_CH20	0
DMON_SW_CH20	0	TDCTEST_CH20	1
AMON_CTRL_CH20	0	COMP_SPI_CH20	3

Parameter Name	Hex Value	Parameter Name	Hex Value
DAC_SIPM_SC_CH20	0	DAC_SIPM_CH20	11
DAC_TTHRESH_SC_CH20	4	DAC_TTHRESH_CH20	1e
DAC_AMPCOM_SC_CH20	2	DAC_AMPCOM_CH20	9
DAC_INPUTBIAS_SC_CH20	0	DAC_INPUTBIAS_CH20	3
DAC_ETHRESH_CH20	7f	DAC_POLE_SC_CH20	0
DAC_POLE_CH20	3f	DAC_CML_CH20	7
DAC_DELAY_CH20	1	DAC_DELAY_BIT1_CH20	0
DAC_CHANNEL_MASK_CH20	1	DAC_TDC_LEFT_VND2C_SCALE	0
DAC_TDC_LEFT_VND2C_OFFSET	3	DAC_TDC_LEFT_VND2C	12
DAC_TDC_LEFT_VNCntBuffer_SCALE	0	DAC_TDC_LEFT_VNCntBuffer_OFFSET	3
DAC_TDC_LEFT_VNCntBuffer	8	DAC_TDC_LEFT_VNCnt_SCALE	0
DAC_TDC_LEFT_VNCnt_OFFSET	2	DAC_TDC_LEFT_VNCnt	14
DAC_TDC_LEFT_VNPCP_SCALE	0	DAC_TDC_LEFT_VNPCP_OFFSET	2
DAC_TDC_LEFT_VNPCP	1b	DAC_TDC_LEFT_VNVCODELAY_SCALE	0
DAC_TDC_LEFT_VNVCODELAY_OFFSET	3	DAC_TDC_LEFT_VNVCODELAY	a
DAC_TDC_LEFT_VNVCOBUFFER_SCALE	0	DAC_TDC_LEFT_VNVCOBUFFER_OFFSET	3
DAC_TDC_LEFT_VNVCOBUFFER	0	DAC_TDC_LEFT_VNHITLOGIC_SCALE	0
DAC_TDC_LEFT_VNHITLOGIC_OFFSET	3	DAC_TDC_LEFT_VNHITLOGIC	0
DAC_TDC_LEFT_VNPFC_SCALE	0	DAC_TDC_LEFT_VNPFC_OFFSET	2
DAC_TDC_LEFT_VNPFC	d	DAC_TDC_RIGHT_VND2C_SCALE	0
DAC_TDC_RIGHT_VND2C_OFFSET	3	DAC_TDC_RIGHT_VND2C	12
DAC_TDC_RIGHT_VNCntBuffer_SCALE	0	DAC_TDC_RIGHT_VNCntBuffer_OFFSET	3
DAC_TDC_RIGHT_VNCntBuffer	8	DAC_TDC_RIGHT_VNCnt_SCALE	0
DAC_TDC_RIGHT_VNCnt_OFFSET	2	DAC_TDC_RIGHT_VNCnt	14
DAC_TDC_RIGHT_VNPCP_SCALE	0	DAC_TDC_RIGHT_VNPCP_OFFSET	2
DAC_TDC_RIGHT_VNPCP	1b	DAC_TDC_RIGHT_VNVCODELAY_SCALE	0
DAC_TDC_RIGHT_VNVCODELAY_OFFSET	3	DAC_TDC_RIGHT_VNVCODELAY	a
DAC_TDC_RIGHT_VNVCOBUFFER_SCALE	0	DAC_TDC_RIGHT_VNVCOBUFFER_OFFSET	3
DAC_TDC_RIGHT_VNVCOBUFFER	0	DAC_TDC_RIGHT_VNHITLOGIC_SCALE	0
DAC_TDC_RIGHT_VNHITLOGIC_OFFSET	3	DAC_TDC_RIGHT_VNHITLOGIC	0
DAC_TDC_RIGHT_VNPFC_SCALE	0	DAC_TDC_RIGHT_VNPFC_OFFSET	2
DAC_TDC_RIGHT_VNPFC	d	DAC_TDC_LATCHBIAS_LEFT	708
DAC_TDC_LATCHBIAS_RIGHT	708		

Table B.6: Configuration parameters after optimization of the coincidence measurements at 18 °C.

Appendix C

Supplementary Material

C.1 T-Threshold Scan for CTR Measurement

In Chapter 6, the parameters of the chip have been optimized to achieve the best possible time resolution with the chip. After finding the optimal point for the high voltage, the T-Threshold has been tuned to find the minimum of the measured CTR values. The result of this scan is shown in Figure C.1. The time resolution below 215 ps FWHM has been achieved for two of the configured T-Threshold settings.

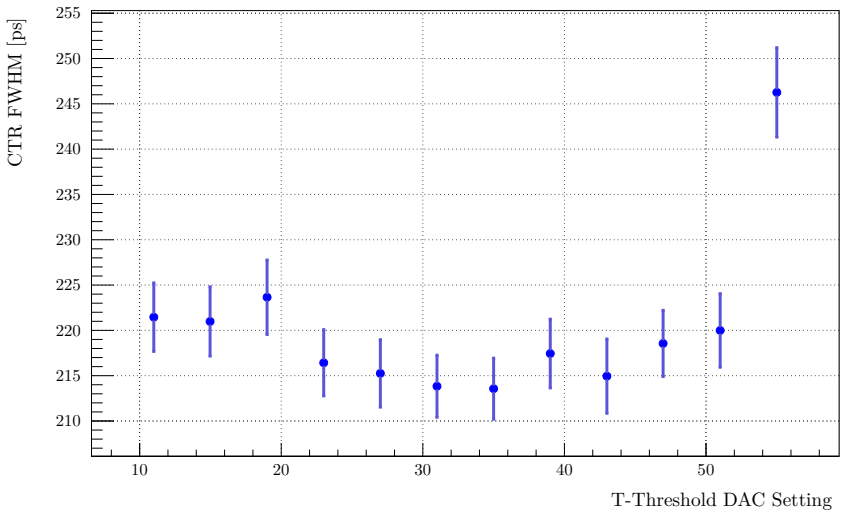


Figure C.1: Measured CTR values during the T-Threshold scan to find the optimal time resolution.

List of Figures

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