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XNAP: A NOVEL TWO-DIMENSIONAL X-RAY DETECTOR FOR TIME RESOLVED SYNCHROTRON APPLICATIONS

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Christophe Jan Thil: *XNAP: A Novel Two-Dimensional X-Ray Detector for Time Resolved Synchrotron Applications*

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ABSTRACT

XNAP: A Novel Two-Dimensional X-Ray Detector for Time Resolved Synchrotron Applications

The XNAP project develops a demonstration system for a spatially resolving detector with timing capabilities in the nanosecond range. A dense array of avalanche photodiodes is combined with multiple readout ASICs to build the detector hybrid. On an area of nearly $1\,\mathrm{cm}^2$, single photons can be counted within each of the 1k pixels.

After 20 years of continuous improvements during operation, the ESRF Synchrotron is going to be upgraded substantially by the replacement of major parts of the source and the beamlines. For experimental techniques that will benefit from the increased brilliance, research into X-ray detectors is required.

The requirements for the novel detector are composed of the distinguished properties of multiple state-of-the-art detector systems, shifted towards technical limits. The specification is transferred into the design of the sensor, ASIC, interposing structure and the readout system. A smaller prototype detector is built to resolve implementation challenges ahead of its large-scale accomplishment. Emphasis is put on the ASIC, and parallel approaches for the interconnecting technology and the readout system are carried out. The usability of the smaller prototype system is demonstrated with measurements of microfocus X-ray and Synchrotron light. Parts of the final detector are characterized at the laboratory prior to its commissioning.

ZUSAMMENFASSUNG

XNAP: Ein neuartiger Flächendetektor zum zeitaufgelösten Nachweis von Synchrotronstrahlung

Im Rahmen des XNAP-Projekts wird das Demonstrationssystem eines neuartigen Flächendetektors mit einer Zeitauflösung im Nanosekunden-Bereich erstellt. Einzelne Photonen können in jedem der 1k Pixel, die eine Fläche von 1 cm² bedecken, gezählt werden. Eine segmentierte Lawinenphotodiode (APD) sowie mehrere Auslesechips, montiert auf beide Seiten einer Trägerstruktur, bilden den Kopf des Detektors.

20 Jahre nach Inbetriebnahme des ESRF-Synchrotrons werden erstmalig große Teile komplett ausgetauscht. Durch die Modernisierung der Quelle und diverser Strahlrohre soll die Brillanz des Synchrotronlichts wesentlich erhöht werden. Um davon vollständig in den Experimenten zu profitieren ist jedoch die Entwicklung neuartiger Detektoren notwendig.

Die Anforderungen an den neuen Detektor ergeben sich aus der Kombination der herausragenden Eigenschaften mehrerer aktueller Detektoren, die an die Grenze des technisch realisierbaren angepasst werden. Diese Spezifikation wird in das Konzept für Sensor, Trägerstruktur und Chip sowie für die weitere Ausleseelektronik überführt. Anhand eines kleineren Prototyps werden die technischen Herausforderungen der Konstruktion vor der Implementierung des finalen Detektors untersucht und gelöst. Im Fokus dieser Arbeit steht der Chip, jedoch auch alternative Umsetzungen der Trägerstruktur und der Ausleseelektronik. Durch Messungen mit einer Mikrofokus-Röntgenquelle sowie am Synchrotron wird die Funktionstüchtigkeit des Prototyps bestätigt. Vor dem Zusammenbau des finalen Systems erfolgt die Charakterisierung einzelner Detektorbestandteile im Labor.

ACKNOWLEDGMENTS

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To all members of the XNAP collaboration, I am truly thankful for their continued effort. By their vision of a novel detector for Synchrotron applications, they sparked a strong interest, not solely for photon detector research and development, but for a much broader field of Synchrotron physics.

Many thanks to Christian Kreidl for his advice and hands-on assistance on interconnection technology.

For the warm welcome and kind guidance during different testbeams at the ESRF Synchrotron, I want to thank the members of the Instrumentation Services and Development Division (ESRF ISDD).

Last but not least, many thanks to my family and friends for their unconditional confidence and substantial encouragement.

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ACRONYMS

ADC analog to digital converter

APA avalanche photodiode array

APD avalanche photodiode

APS active pixel sensor

ASIC application specific integrated circuit

CCD charge coupled device

CMOS complementary metal oxide semiconductor

CSA charge sensitive amplifier

CXDI coherent X-ray diffraction imaging

DAC digital to analog converter

DAQ data acquisition

DCL differential current-mode logic

DCM digital clock manager

DDR double data rate

DePFET depleted p-channel field effect transistor

DESY Deutsches Elektronen-Synchrotron

DLS dynamic light scattering

DRAM dynamic random access memory

EDA electronic design automation

ERL energy recovery linear accelerator

ESRF European Synchrotron Radiation Facility

eV electron volt

FEL free electron Laser

FIFO first-in first-out

FPGA field-programmable gate array

FSM finite state machine

FWHM full width at half maximum

GPIB general purpose interface bus

HDI high density interconnect

IC integrated circuit

ILL Institut Laue-Langevin

IP Internet protocol

LED light emitting diode

LDI Laser direct imaging

LINAC linear accelerator

LSB least significant bit

LTCC low temperature cofired ceramic

LVDS low voltage differential signaling

MCP micro-channel plate

MOS metal oxide semiconductor

MSB most significant bit

NRS nuclear resonant scattering

NFS nuclear forward scattering

NIS nuclear inelastic scattering

NMOS n-channel metal oxide semiconductor

PCB printed circuit board

PCELL parameterized macro cell

PID proportional integral derivative

PMOS p-channel metal oxide semiconductor

PMT photomultiplier tube

RF radio frequency

ROC readout controller

SASE self-amplified stimulated emission

SDR single data rate

SEM scanning electron microscopy

SiPM silicon photomultiplier

SMU source measurement unit

SRAM static random access memory

TCP transmission control protocol

TDC time to digital converter

TIA transimpedance amplifier

ToF-PET time of flight positron emission tomography

USB Universal Serial Bus

UV ultraviolet

VHDL VHSIC hardware description language

XNAP X-ray nanosecond array of pixels

XPCS X-ray photon correlation spectroscopy

Part I

SYNCHROTRON PHYSICS AND ITS APPLICATIONS

The XNAP project and its members as the framework for the detector development are presented. By a short historical review, Synchrotron light is introduced. The fundamental properties of the radiation are then deduced from the underlying physical effects. Different generations of light sources where these effects are used to produce X-rays are presented, including details on the ESRF machine. The interaction effects of photons with matter are shown, leading to different detector concepts for X-ray detection. Three selected experimental techniques are presented as use cases for a novel detector.

1 INTRODUCTION

Over the past few years, research at the nanoscale level has vastly influenced our life. Even simple things used as everyday commodities, like toothpaste, contain materials developed by means of progressive technology.

For the research at the inner composition of matter and where the analyzed structures get smaller than electromagnetic radiation of visible range, X-ray and Synchrotron light sources are important tools.

Generators for Synchrotron radiation are stadium sized machines built of high technology parts, requiring considerable expenses for the construction and operation. Dedicated facilities funded by the government, but also an increasing number of commercial institutions, provide access to shared light sources. As a comprehensive service, the users are supported by infrastructure and instrumentation essential for their experiments.

For several decades, solid state photon detectors have been used for the instrumentation of Synchrotron radiation experiments. Sensors built of avalanche photodiodes (APDs) provide sensitivity to electromagnetic radiation at the single photon level, which is, depending on the setup of the experiment, even necessary if illuminating the sample with a very high flux. Further, these devices are characterized by an excellent time resolution, very short dead time and thus allow for photon counting at very high dynamic range. Unfortunately, the research on APDs is limited, as special manufacturing steps are required to build the devices. In the same time, the rise of Silicon microelectronics lead to advanced manufacturing and interconnection techniques. This allowed classic PIN diode detectors to evolve from single element devices, where the development of APDs has stalled, to detectors covering large areas with several thousand to million of position sensitive picture elements named *pixel*.

The performance gap between detector systems built of unstructured APDs and those built of pixelated devices becomes more and more important with the development of novel experimentation techniques, taking advance of the increased photon flux and shorter pulse duration provided by optimized light sources. Therefore, upgrades are not only necessary for the radiation sources, but also for the variety of photon detection systems.

The X-ray nanosecond array of pixels (XNAP) project is initiated by the European Synchrotron Radiation Facility (ESRF) as a proof of concept for an area detector with segmented APD array. The target for the final demonstration system is a kilopixel detector with time res-

olution in the nanosecond range and a per pixel photon count rate of several 10^7 1/s. Emphasis is placed on demonstrating the detector capabilities, therefore application specific optimization should be avoided.

As the development of such a detector consists of many different and complex tasks, research, development and implementation, it is distributed among the members of the project: ESRF, Deutsches Elektronen-Synchrotron (DESY), Excelitas Corp., SPring-8 and Heidelberg University.

This work was started with a special focus on the development of the readout application specific integrated circuit (ASIC). Within time, it gradually extended to a much broader spectrum including the development of interconnection technology between different Silicon devices, the implementation of complex firm- and software code for field-programmable gate array (FPGA) devices and testing of the whole detector system.

The thesis is split into five parts: In the first part, this introduction is followed by a presentation of Synchrotron light, methods of its detection and how they are implemented in the context of experimental techniques. The second part initiates the detector development with an abstract definition of the requirements and summarizes the design and implementation of the detector. Within the third part, selected measurement results, obtained at different phases of the project, are shown. The fourth part concludes on the project with a summary of the current status and an outlook to further development. As the fifth part, additional information is presented in an appendix.

2 SYNCHROTRON LIGHT

2.1 HISTORY OF SYNCHROTRON LIGHT

The traditional research with light has lead to a large number of discoveries and therefore vastly influenced our view of the world. With the first observation of the X-rays by Wilhelm Röntgen at the end of the 19th century, a huge step in science from the analysis of the surface area towards the internal structure of matter was made possible. Compared to visible light, the X-ray photons are characterized by their higher energy or shorter wavelength, leading to the ability to easily traverse matter. Since then, X-ray experiments using different techniques have become standard tools in scientific and technical applications. For a long time, traditional gas discharge and cathode ray tubes were used as the only sources of ultraviolet (UV) and X-ray radiation.

Three years after the discovery of the X-rays, the French physicist Alfred-Marie Liénard formed the equation for the electromagnetic effect of a fast moving electric point charge on a trajectory, which theoretically predicts the presence of radiation in particle accelerators emitted by the circular moving charges.

The first experimental recognition of this radiation took place many years later: In 1947, visible light emission was seen while operating an electron accelerator (Figure 2.1).

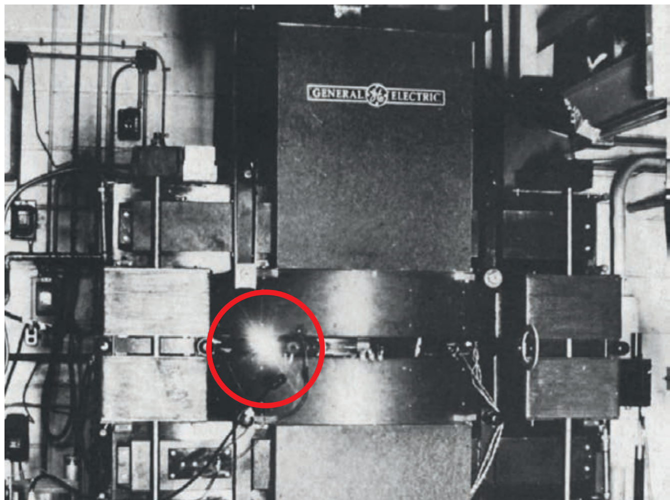


Figure 2.1: First observation of visible Synchrotron radiation at the General Electric laboratory in 1947.

This electron accelerator was of Synchrotron type: The electrons were forced to move on a fixed circular trajectory by bending magnets, whose magnetic strength is constantly adapted to the kinetic energy of the beam. The light-weight electrons are ultra-relativistic, they travel at a speed which is very close to the speed of light and the duration per turn is almost independent of their energy if the loop perimeter is kept constant. After the name of this machine, the observed radiation was called Synchrotron radiation.

Massive relativistic particle: Particles with a kinetic energy equal to or greater than their rest mass.

First considered only as an inherent drawback of that accelerator technology, as the energy loss through the emittance of Synchrotron radiation needs to be continuously compensated, the radiation properties were later studied in detail by many physicists.

Nevertheless, Synchrotron radiation and the analytic possibilities of its usage did not attract broad interest in the following decade. There were no dedicated facilities for Synchrotron radiation applications nor were modifications made to existing accelerators to allow for easier access to the emitted radiation.

2.2 PROPERTIES OF SYNCHROTRON LIGHT

The following derivation of the fundamental physical properties is based on [30]. Also within this work, the focus is set to explain the principle of Synchrotron radiation in an accessible way. Therefore some results are simplified with emphasis on understanding, not ultimate completeness. An in-depth study can be found in [45].

2.2.1 *Frequency shift by Doppler effect and special relativity*

The fundamental phenomena related to the emission of Synchrotron light from accelerated charges are the well-known Doppler effect and the special relativity. Combining both together, it is possible to get a very high frequency photon beam.

In order to simplify, consider a moving source in a two-dimensional plane, defined by the axis x and y (Figure 2.2). The source moves along the x axis at the speed of v. For the analysis, two reference systems are used: F_S, the source frame, moving with the source, and F_L, the laboratory frame, moving along the x axis at the speed of $-v$ when seen from F_S. The x axis is therefore collinear between the frames whereas the y axis are parallel.

Between both reference frames, the position coordinate and the time can be converted using the Lorentz transformation

$$x_L = \gamma(x_S + vt_S) \tag{2.1}$$

$$y_L = y_S \tag{2.2}$$

$$t_L = \gamma\left(t_S + \frac{vx_S}{c^2}\right) \tag{2.3}$$

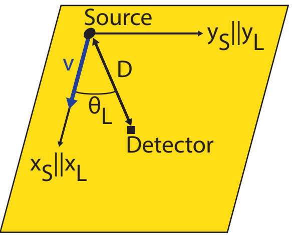


Figure 2.2: Source and detector with coordinate systems in the source (x_S and y_S) and laboratory (x_L and y_L) reference frames. The detector spans the angle θ_L to x_L.

with the Lorentz factor γ

$$\gamma = \frac{1}{\sqrt{1-\beta^2}} \tag{2.4}$$

$$\beta = \frac{v}{c} \tag{2.5}$$

Using the Lorentz transformation for the momentum and energy yields to

$$p_{L,x} = \gamma(p_{S,x} + m_0 v) = \gamma\left(p_{S,x} + \frac{E_S}{c^2}v\right) \tag{2.6}$$

$$p_{L,y} = p_{S,y} \tag{2.7}$$

$$E_L = \gamma(E_S + v p_{S,x}) \tag{2.8}$$

The source now emits a photon of angular frequency ω_S along the x axis with

$$E_S = \hbar\omega_S \tag{2.9}$$

$$p_{S,x} = \frac{\hbar\omega_S}{c} \tag{2.10}$$

$$p_{S,y} = 0 \tag{2.11}$$

In the laboratory frame, Equation 2.9 corresponds to

$$E_L = \hbar\omega_L \tag{2.12}$$

Now injecting Equation 2.9 and Equation 2.10 with Equation 2.12 into Equation 2.8

$$\hbar\omega_L = \gamma\left(\hbar\omega_S + v\frac{\hbar\omega_S}{c}\right) = \gamma\hbar\omega_S\left(1+\frac{v}{c}\right) = \gamma\hbar\omega_S(1+\beta) \tag{2.13}$$

$$\omega_L = \omega_S\gamma(1+\beta) \tag{2.14}$$

As $\beta < 1$, this is equivalent to the known Doppler effect formula

$$\omega_L = \omega_S\sqrt{\frac{1+\beta}{1-\beta}} \tag{2.15}$$

If the source moves with velocity $v \to c$, like the relativistic charge in a Synchrotron, $\beta \to 1$, this yields to

$$\gamma(1+\beta) \approx 2\gamma \tag{2.16}$$

Therefore, with Equation 2.14 and Equation 2.16, the observed photon frequency can be approximated

The frequency of the emitted Synchrotron radiation is about 2γ the incident frequency.

$$\omega_L \approx 2\gamma\omega_S \tag{2.17}$$

If the detector is not in the direction of the velocity, the fraction of the effect can be projected with the following geometric consideration. Assume the angle θ_L between the direction of velocity, the x axis, and the detector D.

$$p_{L,x} = \frac{\hbar\omega_L}{c}\cos\theta_L \tag{2.18}$$

Now take the inverse Lorentz transformation of Equation 2.8, negating the relative speed v and interchanging the reference frames

$$E_S = \gamma(E_L - v p_{L,x}) \tag{2.19}$$

By injecting Equation 2.18 into Equation 2.19, this leads to

$$\hbar\omega_S = \gamma\left(\hbar\omega_L - v\frac{\hbar\omega_L}{c}\cos\theta_L\right) = \gamma\hbar\omega_L(1-\beta\cos\theta_L) \tag{2.20}$$

$$\omega_S = \gamma\omega_L(1-\beta\cos\theta_L) \tag{2.21}$$

$$\omega_L = \frac{\omega_S}{\gamma(1-\beta\cos\theta_L)} \tag{2.22}$$

For $\theta_L = 0$, this is equivalent to the calculation without angular dependence (Equation 2.15). For $\theta_L = \pi/2$, when the source is at the point of closest approach of the detector, this leads to the transverse Doppler effect with

$$\omega_L = \frac{\omega_S}{\gamma} \tag{2.23}$$

2.2.2 *Angular collimation for moving wave sources*

Apart from the frequency shift, the emission of waves by a *moving* source also affects how the emitted radiation is received at the detector. This phenomenon is true for non-relativistic speeds; going up to the relativistic range, the impact is increased.

Let the moving source emit waves, collimated at an angle θ_S (Figure 2.3). Using the velocity components $u_{S,x}$ and $u_{S,y}$ of the emitted wave, the angle equals to

$$\theta_S = \arctan\frac{u_{S,y}}{u_{S,x}} \tag{2.24}$$

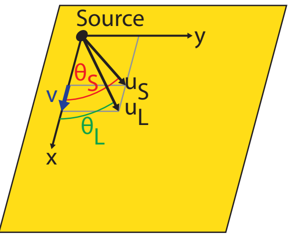


Figure 2.3: Source emitting collimated waves with coordinate systems in the source (x_S and y_S) and laboratory (x_L and y_L) reference frames.

These components can also be expressed with the wave magnitude u_S and θ_S

$$u_{S,x} = u_S \cos\theta_S \tag{2.25}$$

$$u_{S,y} = u_S \sin\theta_S \tag{2.26}$$

In the laboratory frame, the wave is detected at the angle θ_L, which can expressed with the velocity components $u_{L,x}$ and $u_{L,y}$ as

$$\theta_L = \arctan \frac{u_{L,y}}{u_{L,x}} \tag{2.27}$$

Now, transforming the velocity of the wave from the source to the laboratory frame

$$u_{L,x} = u_{S,x} + v = u_S \cos\theta_S + v \tag{2.28}$$

$$u_{L,y} = u_{S,y} = u_S \sin\theta_S \tag{2.29}$$

Injecting this into Equation 2.27, the detected emission angle θ_L can be written as

$$\theta_L = \arctan \frac{u_S \sin\theta_S}{u_S \cos\theta_S + v} = \arctan \frac{\sin\theta_S}{\cos\theta_S + \frac{v}{u_S}} \tag{2.30}$$

Therefore, the angle θ_L is smaller than the initial angle θ_S, decreasing with increasing v/u_S, therefore increasing speed v of the source.

The same considerations can be made for a moving photon source at relativistic speed. Keeping the same environment as for the frequency shift calculations, previous results can be reused. With Equation 2.6 and Equation 2.7

$$\theta_L = \arctan \frac{p_{L,y}}{p_{L,x}} = \arctan \frac{p_{S,y}}{\gamma \left(p_{S,x} + \frac{E_S}{c^2} v \right)} \tag{2.31}$$

With the same geometric considerations than within Equation 2.25 and Equation 2.26 and with $p_S = \hbar\omega_S/c$

$$\theta_L = \arctan \frac{\frac{\hbar\omega_S}{c} \sin\theta_S}{\gamma \left(\frac{\hbar\omega_S}{c} \cos\theta_S + \frac{\hbar\omega_S}{c^2} v \right)} = \arctan \frac{\sin\theta_S}{\gamma(\cos\theta_S + \beta)} \tag{2.32}$$

The angular collimation is proportional to $1/\gamma$ for Synchrotron radiation.

As the velocity of the source $v \to c$ for relativistic charges in a Synchrotron, therefore $\beta \to 1$, this leads to

$$\theta_L = \arctan \frac{\sin\theta_S}{\gamma(\cos\theta_S + 1)} \propto \frac{1}{\gamma} \tag{2.33}$$

2.3 LIGHT SOURCES

Insertion devices: Dedicated magnets in the beam path to emit Synchrotron radiation.

Ultrarelativistic charged particles, electrons or positrons, due to their small rest mass, which move with a speed close to the speed of light, are accelerated radially by the magnetic field of bending magnets or insertion devices and emit an electromagnetic radiation called Synchrotron radiation. Depending on the properties of the magnetic field used to interfere the particle trajectory, the properties of the emitted electromagnetic waves are determined.

1 electron volt (eV) is the amount of energy gained or lost by one electron moving across the potential difference of 1 V.

Synchrotron light sources can be categorized into different generations. Common for almost all generations of light sources is their general accelerator layout: A bunch composed of charged particles is generated, for negative charged particles for example by using a classical triode electron gun. The charge then gets further accelerated from a few 100 keV to few 100 MeV of kinetic energy by the electric field of a linear accelerator. The next stage, the booster Synchrotron then accelerates the charge to the final energy in the GeV range. Finally, the charge is transferred to the storage ring, where solely the energy loss through Synchrotron radiation is compensated but no further acceleration takes place.

As protons are much heavier than electrons and therefore require much higher energy to produce the same radiation as an electron beam, Synchrotron light sources typically use electrons as their primary charged particles. Also, the particle acceleration for electrons in the Synchrotron is easier than for protons as their speed is close to the speed of light and therefore almost constant, only the particle energy increases, requiring an increasing magnetic field in order to bend the beam, but no change in the accelerator period.

2.3.1 *First generation light sources*

The *parasitic* usage of electron or positron Synchrotrons designed for high energy or nuclear physics mark the beginning of science with this light type. There were no optimizations made for Synchrotron radiation usage in terms of the beam properties like its energy or the orbital stability. The single sources of radiation were the bending magnets with their uniform magnetic field used to keep the charges on track. Due to this and the relative low particle energy below 1 GeV, the emitted photons were only in the UV and soft X-ray part of the electromagnetic spectrum.

The photon beam by the bending magnets can be pictured as a sweeping search light across the bent trajectory, hence of very large spread. The emitted photon spectrum is exceptionally broad, as the single pulse duration is fairly short. As this is a parasitic effect, the photon beam is not optimized in terms of spot size, beam divergence or flux. The emitted photon energy spectrum can be calculated from the energy E of the incident particle and the magnetic field T by the bending magnets used to force the charges on a circular trajectory. The so called *critical energy* $\hbar\omega_c$ is the one which divides the total emitted power from a bending magnet in two halves. Expressed in commonly used units, it can be written as [45]

$$\hbar\omega_c\,[\text{keV}] = 0.655E^2\,[\text{GeV}]B\,[\text{T}] \tag{2.34}$$

Through the construction of the DESY in Hamburg, Germany, which went into operation in the mid-1960s, with a beam energy of 6 GeV, the emitted photons with about 125 keV reached the hard X-ray region of the electromagnetic spectrum.

2.3.2 *Second generation light sources*

In the following years, existing storage rings were modified for the production of Synchrotron radiation, and also new facilities were built due to the increasing demand by the developing scientific user community. Many parameters of these sources were optimized, for example the emittance was reduced by a factor of five and the coherence length of the Synchrotron light was extended.

Interference between waves always occurs, but in order to observe constructive or destructive interference the waves must show a sufficient coherence length. Spatial or transverse coherence is a metric for the correlation between waves at different points in space. The coherence length ξ_t denotes the maximum size of a transverse coherent beam which can be achieved for a given source. Temporal or longitudinal coherence is a metric for the correlation at different moments in time. The coherence length ξ_l is the distance along the propagation direction of the beam over which phase correlation is lost. A perfect monochromatic source of point-like shape or placed infinitely away emits fully coherent waves, which, passing through a slit, interfere to a sharp diffraction pattern. But with a spatially extended or imperfect monochromatic source, the diffraction patterns overlay and therefore blur or are entirely invisible.

No one has ever been able to define the difference between interference and diffraction satisfactorily. It is just a question of usage, and there is no specific, important physical difference between them.

—R. Feynman [13]

The beam emittances (ϵ_x in the horizontal and ϵ_y in the vertical plane) are parameters to describe the ability to focus the beam in the accelerator, as they describe the occupied surfaces in the two-dimensional phase spaces. The desired small emittance can be obtained by segmenting the bending magnets, therefore reducing the deflection per magnet, and inserting focusing magnets in between them. The

coupling of the horizontal to the vertical emittance is described by the coupling coefficient k, with $\epsilon_y = k\epsilon_x$.

2.3.3 *Third generation light sources*

Further improvements in the beam characteristics were requested by the increasing number of experiments. A smaller beam spot with less divergence and an even higher photon flux enabled new experimentation techniques but also reduced the sampling time on existing ones.

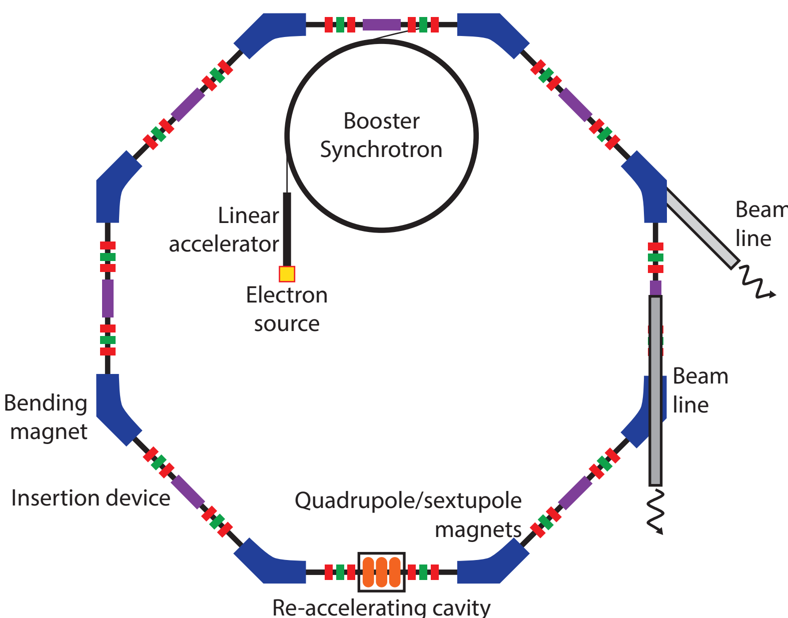


Figure 2.4: Schematic arrangement of a third generation light source. Free electrons from the source are accelerated to an intermediate energy in the LINAC, then transferred to the booster Synchrotron where they are accelerated to their final energy. Then, they are transferred to the storage ring where they keep circulating. Due to the magnetic deflection in the Synchrotron and storage ring, the electrons radiate energy and therefore need to be re-accelerated. The beam is kept on track by bending magnets (blue) and focused by quadrupole magnets (red). Sextupole magnets (green) correct chromatic aberrations. X-rays are fed out via beam lines, either from bending magnets or insertion devices (purple). Details of the booster Synchrotron are omitted for simplicity.

In addition to the bending magnets which still serve as an X-ray source, dedicated devices for the generation of the Synchrotron radiation were developed (Figure 2.4). The basic operation principle for these insertion devices is still the same as with bending magnets, the moving charge is deflected from its original trajectory, but the electro-

magnetic field organization and strength inside these wigglers and undulators is different (Figure 2.5).

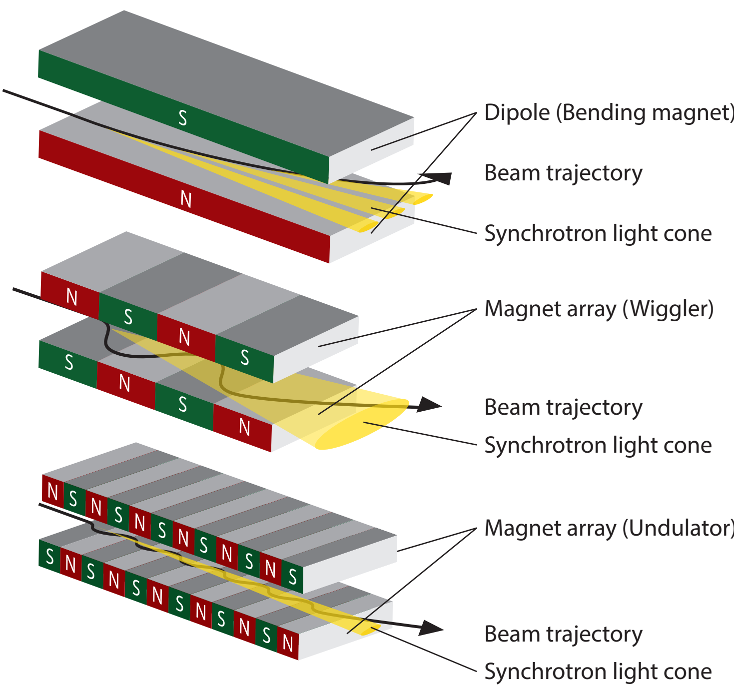


Figure 2.5: Magnet types used in the Synchrotron storage ring for the emission of radiation: Bending magnets (low flux, broad continuous spectrum), wigglers (high flux, broad continuous spectrum) and undulators (very high flux, narrow line spectrum, low divergence).

Wigglers and undulators are built as an array of magnets of alternating polarity. By the Lorentz force of the magnetic field, the charged particles are deflected and travel on a sinusoidal trajectory. Depending on the characteristic of the magnetic field, the emitted Synchrotron radiation has either a continuous or line spectrum and is highly polarized in the plane of the deflection force. The magnets itself can be permanent or electromagnetic, either regular or super conducting, or a combination of both fundamental types, depending on the required strength of the magnetic field.

In order to differentiate between the two insertion devices by using a metric for the deflection of the charge, the undulator parameter K is used

$$K = \frac{eB_u\lambda_u}{2\pi m_0 c} \tag{2.35}$$

where

$$B_u : \text{magnetic field,}$$
$$\lambda_u : \text{undulator period,}$$
$$m_0 : \text{particle rest mass,}$$

Wigglers are insertion devices with $K > 1$. There, the oscillation amplitude is high, due to the strong magnetic field of large magnetic poles. The emitted Synchrotron radiation does not interfere and the intensity sums up independently. Wigglers can be seen as a series of traditional bending magnets, turning the beam alternately to the left and to the right. Therefore, like from a bending magnet, the emitted photons are in a wide spectrum (Figure 2.6). Typical characteristics are a magnetic field of more than 2 T in a 10 mm gap with less than 10 magnetic periods.

Undulators have a smaller oscillation amplitude, therefore $K \leqslant 1$. The emitted radiation interferes constructively on the selected charge trajectory and therefore the intensity is proportional to the square number of undulator periods. In addition, the positive interference leads to a line spectrum with higher brilliance, but as the oscillation amplitude is smaller, also to lower photon energy (Figure 2.6). The number of magnetic periods is in the order of 100 with a magnetic field of 1 T in the 6 mm gap, for a 2 m long device.

Brilliance: Figure of merit for the photon flux density. See Equation 2.38 for the exact definition.

The energy of the first harmonics of the Synchrotron radiation emitted by an undulator can be approximated

$$\hbar\omega_L \approx \frac{\hbar 4\pi c\gamma^2}{\lambda_u} \frac{1}{1 + \frac{1}{2}K^2 + \theta_L^2\gamma^2} \tag{2.36}$$

where

$$\lambda_u : \text{undulator period,}$$
$$K : \text{undulator deflection parameter,}$$
$$\theta : \text{emission angle } \tan\theta = {}^1/_{\beta\gamma}.$$

In this formula, the effects of relativistic length contraction γ/λ_u and relativistic Doppler shift 2γ can be recognized.

The photon flux an undulator generates is a proportional function

$$\phi \propto I n_u Q_n(K) \tag{2.37}$$

where

$$I : \text{beam current}$$
$$n_u : \text{number of undulator periods}$$
$$Q_n(K) : \text{a function of the deflection parameter } K.$$

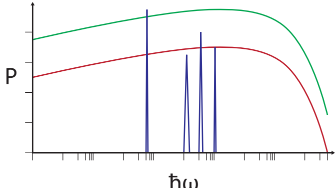


Figure 2.6: Schematic emission spectrum for bending magnets (red), wigglers (green) and undulators (blue). The energy axis is log scaled, whereas the power is linear.

The brilliance is an important metric which combines the properties of the particle accelerator and individual insertion devices. It is defined as the emitted number of photons per second, per photon energy bandwidth, per solid angle and per unit size

$$B = \frac{\phi}{(2\pi)^2 \epsilon_x \epsilon_y} = \frac{\phi}{(2\pi)^2 k \epsilon_x^2} \tag{2.38}$$

where

ϕ : is the photon flux,
ϵ_x : horizontal emittance,
ϵ_y : vertical emittance,
k : coupling coefficient.

For the users of Synchrotron radiation, it is the important figure of merit as it describes how efficiently a photon flux with small spot size and small divergence can be obtained. It scales proportionally with the beam current in the Synchrotron ring and inversely proportional with the horizontal and vertical emittances.

All current major light sources are built of these three radiation emitters and of storage rings of multiple GeV energy.

In-depth information on the third and next generation light sources are presented in [5].

2.3.4 *Fourth generation light sources*

The elevated requirements by upcoming experimentation techniques can only be accomplished in part by the well-known storage ring based sources. Other machine approaches in order to increase brightness and coherence and to decrease the bunch length are free electron Lasers (FELs), based on linear accelerators instead of Synchrotron accelerators and storage rings, and energy recovery linear accelerators (ERLs), which combine linear accelerators with a return arc to recover the energy from the returning particles into the accelerating structure (but not re-accelerating them) [6]. These light sources

consist of a high-quality electron accelerator with a very low beam emittance and very long undulators. Like with third generation light sources, these undulators force the electron beam on a sinusoidal trajectory, therefore emitting Synchrotron radiation in the same plane as the electron beam. The special design of the very long FEL undulators leads to an interaction between the photons and the electrons, resulting in a microstructure of the electrons called bunching, equal to the wave length of the emitted radiation. These electron bunches then radiate in phase in the undulator. The photon pulses emitted during this self-amplified stimulated emission (SASE) process are very short and of very high brilliance.

2.4 THE EUROPEAN SYNCHROTRON RADIATION FACILITY

The ESRF is a light source dedicated to fundamental and applied scientific research with Synchrotron light for the research of matter at the molecular and atomic level. It is located in Grenoble, France, and funded as a multi-national research facility with the mission not only to provide the Synchrotron light, but also the necessary infrastructure, like optic and electronic equipment, in order to allow visiting scientists to run their experiments without the need to bring their own gear.

Figure 2.7: Aerial view of the ESRF. The linear accelerator and booster Synchrotron are located in the right inner area of the white roofed storage ring and beam line area [8].

The light source is of third-generation electron storage ring architecture. Its construction was started in 1988 and it is currently upgraded in multiple phases in order to increase the scientific utility even further.

At current, the machine consists of three major parts (Figure 2.7):

- Thermal electron source and linear accelerator up to 200 MeV energy
- Booster Synchrotron up to the final 6 GeV energy
- Storage ring with magnets, Synchrotron light extracting beam lines and re-accelerating and focusing devices

A filament is heated in an evacuated tube and an electron beam of 200 mA is ejected in short pulses. It is then accelerated by an external electric field to several 100 keV energy. The charges then are compressed even further into a bunch of either 1 us or 2 ns length by a standing wave buncher. The electron bunch then is accelerated to an intermediate energy of 200 MeV by a LINAC.

Bunchers compress charge clouds by the interaction of the primary electrons with an additional electromagnetic RF field in resonant cavities.

From the LINAC, the electron bunch is passed to the Synchrotron accelerator using a transfer line, equipped with magnets to focus and steer the beam.

The booster Synchrotron increases the energy up to the final 6 GeV by feeding in pulsed RF energy through high voltage cavities. Depending on the desired filling mode, the full or only a part of the 300 m ring circumference are occupied by the charge bunches. Different magnets, dipoles, focusing and defocusing quadrupoles and sextupoles are installed to shape the beam.

Focusing quadrupoles are called the horizontally focusing and vertically defocusing magnets. Defocusing are horizontal defocusing and vertically focusing. Combining both at the right distance, the overall effect is focusing.

The connection between the Synchrotron and the storage ring is the second transfer line. Like the first one, it is equipped with beam optics to keep the beam in shape and to kick it on the right trajectory.

Figure 2.8: Electron beam pipe and Synchrotron radiation beam lines at the ESRF storage ring. A dipole magnet (blue) with associated beam line and a quadrupole magnet (red) can be seen.

The storage ring is the final section of the accelerator (Figure 2.8). Contrary to its name, it is built of 32 straight sections, each of 6 m

length, where the insertion devices, wigglers and undulators, can be installed. In between, 64 bending magnets force the beam on the circular trajectory and about 300 quadrupoles keep the beam well focussed down to a horizontal emittance of 4 nm and a vertical emittance of 4 pm, while about 200 sextupoles correct chromatic aberration. Some insertion device slots are used for beam injection and RF powered re-acceleration in order to compensate for the radiated energy per turn per electron of about 5 MeV, mostly from the bending magnets. A single electron bunch or multiple bunches, up to 992 depending on the filling pattern, travel with a revolution frequency of 355 kHz through the beam pipe, which has a circumference of 844 m. Synchrotron radiation is extracted from the storage ring in 52 beam lines of different arrangement and therefore length. The maximum magnetic field in the undulators and wigglers is in the range of 0.2 T to 3 T with magnetic periods between 17 mm and 375 mm and gaps between 5 mm and 24 mm. The radiated X-rays are in the energy range of 0.3 keV to 750 keV. Depending on the radiating device, the coherence length is in the order of $\xi_{t,\text{horizontal}} = 10\,\text{um}$, $\xi_{t,\text{vertical}} = 100\,\text{um}$ and $\xi_{l} = 10\,\text{um}$.

All parts where the electrons travel are evacuated and kept with a very low pressure in the order of 10^{-9} mbar to avoid collisions between the moving charges and residual gas.

3 PHOTON DETECTION

3.1 INTERACTION OF PHOTONS WITH MATTER

Photons are the massless and electrically neutral elementary particles quantifying all forms of electromagnetic radiation, including visible light, and the electromagnetic force carrier. Their lifetime is endless, but photons can be absorbed and also created by many natural processes. In the empty space, photons always travel at the speed of light c. The photon energy $E = \hbar\omega = h\nu$ and momentum solely depend on the (angular) frequency $\omega = 2\pi\nu$, as their rest mass is zero.

Depending on their origin, photons can be classified, but this does not influence their mode of interaction. For example, *gamma rays* are originating from nuclear transitions, *Bremsstrahlung* (also called *continuous X-rays*) is emitted by accelerated charged particles whereas *characteristic X-rays* are emitted from the transition of bound electrons in the atomic shells.

In contrast to charged particles continuously losing their energy, photon interaction occurs at once: Either a photon is entirely removed from the incident beam in one single interaction or it traverses matter without interaction at all, which leads to a truly exponential reduction of the photon number.

The intensity of an incident photon beam I_0 is reduced after travelling a given mass thickness with an area density of ρd to the remaining amount I, which is given by the absorption law of Lambert-Beer

$$I = I_0 \exp\left(-\frac{\mu}{\rho}\rho d\right) \tag{3.1}$$

where

$$\begin{aligned} \frac{\mu}{\rho} &: \text{mass attenuation coefficient} \\ \mu &: \text{absorption coefficient, depending on } E, Z \\ \rho &: \text{density of traversed matter} \\ d &: \text{travelled distance.} \end{aligned}$$

The mass attenuation coefficient μ/ρ for various elements and mixtures is tabulated in [16].

By the kind of which electromagnetic radiation interacts with and the effect of the interaction, the processes can be categorized:

Kinds of interaction	Effects of interaction
(1) Interaction with atomic electrons	(a) Complete absorption
(2) Interaction with the nucleus	(b) Elastic scattering
(3) Interaction with the electric field surrounding the nuclei or electrons	(c) Inelastic scattering
(4) Interaction with the meson field surrounding nucleons	

Following the systematic, 12 ways of combining kinds and effects thus 12 methods of interaction are possible. In practice, when observing photons with an energy up to several 100 MeV, three dominating effects can be distinguished (Figure 3.1):

1. Photoelectric effect (1a)
2. Compton scattering (1c)
3. Pair production (3a)

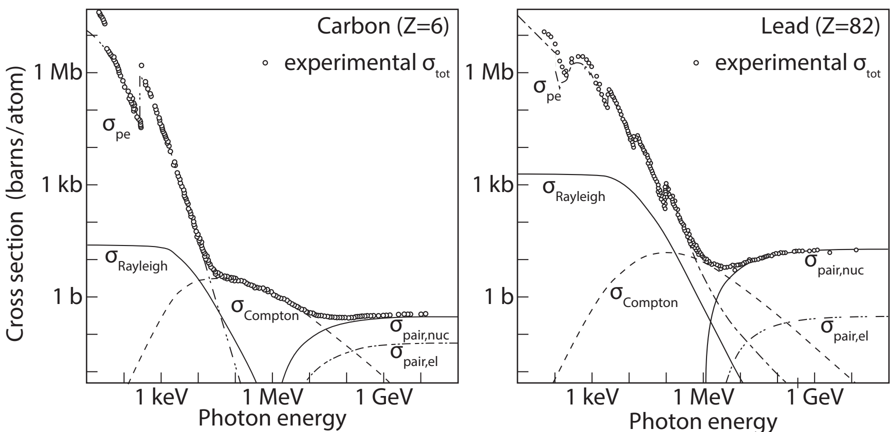


Figure 3.1: Energy dependent photon cross section in light (carbon, left) and heavy (lead, right) matter, with selected contributing processes and experimental data [17].

PHOTOELECTRIC EFFECT In the low energy region, the photoelectric effect is dominant. If the energy absorbed by an electron from a photon is higher than its binding energy, the photon disappears and the electron is ejected from the atom, carrying away the absorbed energy from the photon, reduced by the binding energy of the electron

to the atom. The photon irradiation intensity does not affect this process, only the individual photon energy. The photoelectric effect cross section is characterized by sawtooth shaped absorption edges, as the electrons are arranged in different shells each requiring a different energy level for its photoionization: The cross section steeply increases if the photon energy is high enough to ionize the next electron shell, but with further increasing energy, the cross section decreases.

The order of magnitude of the photoelectric cross section σ_{pe} is given by

$$\sigma_{pe} \propto \frac{Z^4}{E^{7/2}} \text{ for } E < mc^2 \tag{3.2}$$

$$\sigma_{pe} \propto \frac{Z^5}{E} \text{ for } E > mc^2 \tag{3.3}$$

where

Z : atomic number.

COMPTON EFFECT For medium energy photons, the Compton effect is dominant. The energy where the dominant effect transitions from photoelectric to Compton depends on the atomic number of the interacting element, typically in the MeV range. The compton cross section decreases with increasing photon energy. The process of compton scattering describes an energy transfer from a photon to a scattering electron. A new photon with reduced energy is emitted from the recoiling electron at at different angle. The energy of the scattered photon can be written as

$$E = \frac{E_0}{1 + \frac{E_0}{m_e c^2}(1 - \cos\theta)} \tag{3.4}$$

where

E_0 : Energy of incident photon
θ : Scattering angle

The amount of transferred energy reaches its maximum if the direction between incident and emitted photon is reversed at $\theta = 180°$. This maximum can be recognized as a sharp line when drawing the (transferred) energy, called the Compton edge.

The cross section for Compton scattering is given by the Klein-Nishina formula. The order of magnitude of the Compton cross section $\sigma_{Compton}$ is given by

$$\sigma_{Compton} \propto Z \tag{3.5}$$

PAIR PRODUCTION For even higher energy, pair production, either by interacting with the field surrounding the nucleus or the electrons, dominates. The interaction of a high-energy photon in the electric field of the nucleus or electron creates a pair of an electron and its antiparticle, a positron. The energy of the incident photon must be at least equivalent to the sum of rest masses of the produced particles, therefore above 1.022 MeV, while the momentum is absorbed by the nucleus.

The order of magnitude of the pair production cross section σ_{pair} is given by

$$\sigma_{\text{pair}} \propto Z^2 \tag{3.6}$$

3.2 PHOTON DETECTORS

Only a small section of the electromagnetic spectrum can be seen by the human eye as direct visible light, covering the energy range of about 1.6 eV to 3.3 eV. For other photon energies, especially for X-rays, a suitable detector is needed to capture and convert the photons.

Apart from photographic plates, which are included for historic completeness, the first process to detect the electrically neutral photon is to convert it by the photoelectric effect into a photoelectron or a free electron-hole pair. The fraction of generated electrons per incident photon is called *quantum efficiency* and is a strong function of the photon energy. For some combination of detector material and the incident energy, it can be larger than one. The term of *collection efficiency* describes the fraction of collected photoelectrons per generated photoelectron. Some detectors use an internal *gain* mechanism to multiply the number of collected electrons, which is typically very small, to a larger number either with a proportional or binary multiplication factor in order to ease their detection. The product of quantum efficiency, collection efficiency and gain can be used to calculate the mean overall photon detection abilities for a given detector, and also to analyze its statistical fluctuations.

Detectors can also be distinguished by their ability to provide *spatial information*. Devices intrinsically not resolving any spatial characteristics are referenced by the name of point or zero-dimensional detectors. The size of the photon sensitive area varies from um^2 to cm^2. They are typically used for special purposes or if the arrangement of the experiment uses scanning techniques with the detector and therefore does not require spatial data from the detector itself. With line or one-dimensional detectors, incident photons can be distinguished in one spatial dimension. This can be achieved by splitting the sensor volume into a linear arrangement of discrete pixels along the detector axis or by using a continuous signal splitting, for example with a position controlled voltage divider. Area or two-dimensional detectors provide spatial information for two, typically orthogonal, axes. These

detectors can be built of two line detectors with rotated detector axes, or by a two-dimensional array or matrix arrangement of pixels. Timing properties and therefore how a detector handles multiple photons is another distinguishing factor. Detectors where the collection and processing time is short compared to the interval between incident photons operate in photon *counting mode*. The charges liberated by single photons are collected and processed, therefore these detectors have single photon sensitivity, either only for counting the number of pulses, therefore incident photons, or also for energy by digitizing the signal amplitude corresponding to the photon energy. These detectors require a fast charge collection time in the sensing volume itself and also fast readout electronics to interface the sensor. If the interval between photons is small compared to the readout time of the detector, these systems are typically operated in *integrating mode*. This might be necessary due to very high photon rates or due to large charge collection or long readout time. Single photons cannot processed with these systems, but as they collect charges over a given period, the integral number of photons can be calculated from the charge, which is the sum of all signal charges.

3.2.1 *Photographic plates*

The discovery of X-rays happened with photographic plates, and also for a long time, they served as a method to trace invisible electromagnetic radiation, as it blackens the light-tight sealed plates or film sheets.

As the direct detection ability of the photographic emulsion is comparatively low, scintillating mixtures, converting the X-rays into light with different wavelength or even into the visible range, which then is captured by the plates were used. Still, this type of photon detector is used for medical radiography, but due to many drawbacks, especially in the handling processes, it was abandoned in other scientific areas as soon as electronic detection techniques were available.

3.2.2 *Vacuum photon detectors*

Vacuum photon detectors were among the first detectors where photon generated electrons were detected in direct. Roughly sketched, the incident photon ejects an electron from a photocathode, coated with a material whose work function is adapted to the energy region of interest, for example alkali metals like Caesium Iodide or Rubidium Caesium Antimony. The electron then is accelerated in an evacuated volume towards multiplication elements and finally collected and fed to the readout electronics.

For the detection of high energy photons, scintillating materials are typically used to shift the photon energy down to the regime where the photocathode materials exhibit higher quantum efficiency.

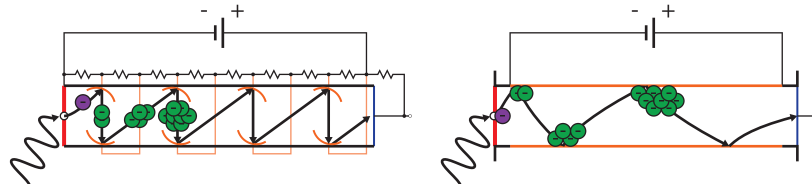


Figure 3.2: Schematic cross section of PMT (left) and MCP (right) devices. The electron (purple) is ejected from the photocathode by the photon (white). The dynodes (orange) in the PMT devices are biased, for example with a resistive network, in a way that there is an electron accelerating potential between the adjacent electrodes. For the MCP device, the resistive coating (orange) inside the channel defines the potential difference itself. Secondary electrons (green) are ejected when the primary electron hits the material, and this cascade continues down to the collection anode (blue).

PHOTOMULTIPLIER TUBES The general layout of PMTs can be figured as reversed cathode ray tube (Figure 3.2). The photon entry window can be made of special glass to minimize losses due to photon absorption as it acts as a parasitic wavelength filter. Incident photons can either eject photoelectrons from the photocathode in the same direction of travel (transmission type), or the photocathode can bounce the electron back from a metal base (reflection type). An electric field is applied between the cathode and the following electrodes, called dynodes, so that the electron is accelerated towards them. Between the dynodes, a resistive network or active components generate the appropriate voltages for the electrons to travel. The dynodes exhibit secondary emission when hit by a primary electron, therefore ejecting a multiple of the primary charge. This amplification mechanism happens multiple times leading to a large number of electrons collected at the anode, where the current is fed out of the tube.

Despite the bulky and delicate glass housing of PMTs and the need for a high voltage supply in the kV range, they remain widely used for high sensitive, low noise photon counting applications.

MICROCHANNEL PLATES As an effort in miniaturization, MCPs can be thought of a flattened PMT (Figure 3.2): Instead of accelerating the photoelectron towards the first and following dynodes, the electron enters a volume of highly resistive material through a hole connecting the front and back side, also connected to a high voltage source, forming a resistive voltage divider. Inside the hole, the electron hits the sidewall and ejects secondary electrons. As this happens

through the entire length of the hole, high amplifications are possible through the high field strength by a high voltage.

As the bulk material for the channels can be made as thin as some mm, PMTs combine huge amplification with reduced space requirements, but do not entirely replace PMTs as the gain variation is significant larger.

HYBRID PHOTON DETECTORS Combining the beneficial properties of PMTs and solid state sensors, this leads to hybrid photon detectors. The photoelectron is accelerated by an electric field and then captured by a solid state diode, where the kinetic energy from the accelerated electron creates a large number of electron-hole pairs. Space-resolving devices can easily be created as the amplification takes place in one single step, further exposing only small variation in gain. Almost all properties of regular diode detectors are preserved.

3.2.3 *Gaseous photon detectors*

The fundamental operation principle of PMTs and MCPs can be transferred to gas electron multipliers, well known as tracking devices in high energy physics, for example named multiwire proportional chamber. In contrast to the previously described devices, the electron, which is ejected by a photon hitting the cathode and then accelerated using high voltage, is amplified by an avalanche ionization process of the gas molecules in the amplification volume. The gas mixture severely influences many parameters of the device, not only the timing and amplification properties. The secondary electrons then are collected at one single anode or location resolving anode strips.

The impact ionization process provides huge gains, allowing for single photon detection sensitivity, but also introduces unwanted effects like the generation of secondary ions and photons which must be taken into account.

3.2.4 *Solid state photon detectors*

Emerging from the rapidly developing solid state microelectronics, photon detectors based on semiconducting devices have influenced many areas, not only limited to the scientific usage. In general, they are more compact and cheaper to build than other detection techniques. Many different sub-device types allow to match the detector to the application, therefore there are plenty of special designs, particular small or rugged, tolerant to different environments, ...

The process initiated by the photon differs from vacuum or gaseous detectors: Instead of ejecting a photoelectron from a sensitive cathode material, an unbound electron-hole pair is liberated if the absorbed energy is larger than the bandgap for the particular semiconductor.

For silicon, on average 3.67 eV of photon energy is needed to liberate one electron-hole pair, while diamond as a wide bandgap semiconductor requires on average 13 eV. These amounts of energy are above the pure bandgap energy of 1.12 eV respective 5.5 eV as some energy excites the crystal lattice into vibration.

One optimization goal for all types of semiconducting photon sensors is to develop materials where the bandgap energy is high enough to allow operation at room temperature without excessive thermal-induced noise, with high density in order to collect a large number of photons in a small volume and where the charge carrier mobility but also their life time is high to allow fast collection of a large number of signal charges.

For doped extrinsic semiconductors, p type denotes a larger hole concentration whereas n type denotes a larger electron density. For strong doping, a + sign is added afterwards, whereas - denotes low dopant concentration.

The typical detector configuration is a p-n junction which is depleted of mobile charges and therefore an electric field is induced. Any electron-hole pair liberated by the photoelectric effect is separated and the charges are carried out at the electrodes, where an electric current can be measured.

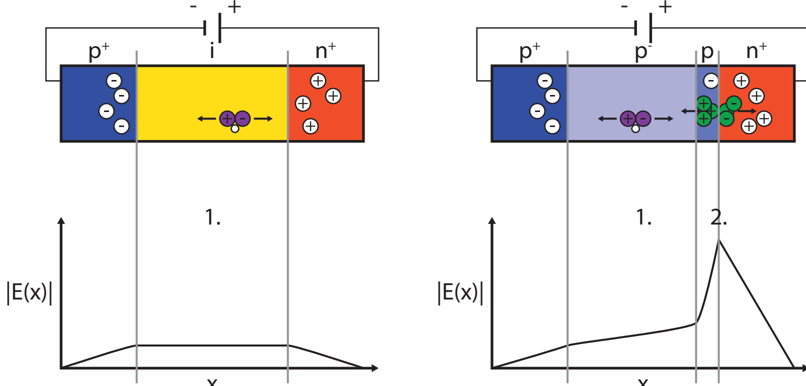


Figure 3.3: Schematic cross section of PIN (left) and APD (right) structure with doping concentration and depleted region after diffusion. The purple electron-hole pair is the one liberated by the photon (white) in the collection zone (1.), while the green electron-hole pairs are secondaries generated by impact ionization in the multiplication zone (2.). On the bottom half, the magnitude of the electric field strength across the devices is shown.

PHOTODIODES Plain photodiodes consist of a p-n junction made of doped semiconducting material. Further optimizations are an asymmetric doping profile to define a preferred area where the depletion extends or an additional layer of slightly or undoped silicon, an intrinsic layer (PIN diode) with high resistivity, to increase the size of the photon collecting depleted zone (Figure 3.3). Also, an external voltage to reverse bias the diode can be applied, as this increases the size of the depletion zone, thus allowing a larger sensitive volume,

and decreases the drift time, therefore increasing the responsiveness of the device.

AVALANCHE PHOTODIODES Regular photodiodes only collect the liberated signal charges, however the sensor does not multiply them. Therefore, detecting low energy photon fluxes or small flux to single photon sensitivity requires a low noise, high sensitive readout of the signal charges. These requirements can be relaxed if the initial electron-hole pair is already amplified close to its liberation. The specially crafted doping profile in the semiconducting material [10] and a very high externally applied reverse bias of several 100 V up to kV accelerate the charges, leading to the liberation of secondary charges by impact ionization in the very high field multiplication region (Figure 3.3). Also, the high field keeps the secondary charges from recombining and instead accelerate them, leading to further ionization with an exponential growth rate and therefore an avalanche breakdown of the junction. Apart from thermal runaway, the breakdown is reversible and does not destroy the diode structure.

Depending on the field intensity, which can be adjusted through variation of the externally applied reverse bias voltage, two distinct operation modes are possible:

LINEAR MODE is an amplification method where the gain is finite, allowing therefore to measure the amplified signal current and calculate the linear proportional incident flux. Typical amplification factors are in the range of some 100×. The charges are extracted faster from the device than they are generated, therefore the current fades away without further circuitry.

GEIGER MODE is a binary amplification method with infinite gain. The avalanche amplification of charges occurs faster than they can be carried out of the detector, therefore the device saturates and a current flows independent of the incident flux. To interrupt the current and return the device into photon sensitive state, the circuit must be externally quenched, either passively with a resistor, dissipating a large amount of the bias voltage if the avalanche current flows, therefore reducing the gain and quenching the avalanche, or actively with a transistor shutting off the biasing circuit.

Very fast response times in the ps timescale and large signal currents compared to conventional photodiodes highlight APDs for single photon timing and counting purposes (Figure 3.4). On the downside, the devices must be temperature compensated by cooling or high voltage regulation, as their dark current and breakdown voltage is highly dependent on the operating temperature. Also, the design of the devices relies upon special implantation profiles, not only complicating the integration into or of other components, but also the

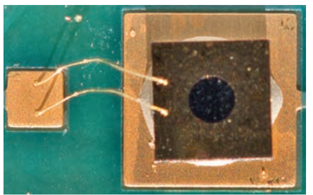


Figure 3.4: Single pixel APD device with an active diameter of 3 mm. General purpose design from Excelitas, but without typical metal can housing as used for characterization of X-ray photon induced current pulses. Operating in linear mode, this device provides 100× amplification at 420 V.

design of position sensing devices like linear segmented sensors or those with pixels in an array arrangement. The operation point of linear mode APDs must be precisely chosen, as statistical variations in the amplification process increase the total noise and might cancel out the positive effect by the internal signal amplification.

SILICON PHOTOMULTIPLIERS Combining the operation principle of Geiger mode APDs with the ability to generate an approximately photon flux dependent output signal, silicon photomultipliers (SiPMs) were created. These devices consist of a large number of tiny APD cells operating in binary Geiger mode, each with its own dedicated biasing circuit (Figure 3.5). Compared to regular APDs, the individual gain per cell is lower, thus requiring only several 10 V to bias the circuit, but as all signal outputs are connected in parallel, the total signal current is proportional to the number of firing cells and therefore approximately proportional to the incident photon flux if the photons do not hit one single cell but are spread over a large number of them.

DEPLETED P-CHANNEL FIELD EFFECT TRANSISTORS Common with the APD or SiPM sensors, the depleted p-channel field effect transistor (DePFET) provides internal signal amplification, but through an entirely different principle than the prior devices (Figure 3.6): Each pixel combines a depleted diode and a first amplification stage in a specially crafted metal oxide semiconductor (MOS) transistor which can absorb and accumulate photon liberated electrons in a region of the transistor where they modulate its current flow [21, 22].

Incident photons are absorbed in the bulk volume below the transistor, which is depleted by the application of an external reverse bias in the order of several 10 V. Above this collection zone, PMOS transistor is build, either with the classical or with annular shaped gate separating the source from the drain electrode. Below the gate, a specially

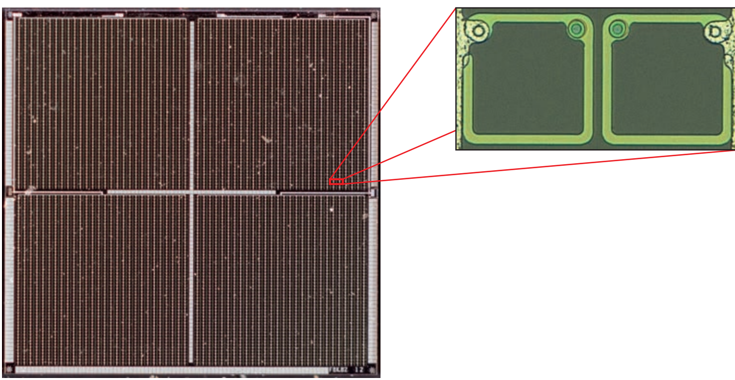


Figure 3.5: Quad pixel SiPM device with an overall size of 4×4 mm, a special design built by FBK-SRS for ToF-PET applications. Each pixel consists of about 3000 cells, arranged in two-fold symmetric blocks, as shown on the right.

designed doping profile creates an electric field which attracts and accumulates the electrons from the photon-liberated electron-hole pairs. If the transistor is switched on by applying a voltage to the gate contact, a current can flow through the transistor if a voltage is applied between the source and drain contacts. The signal charges collected below the gate modulate this current, allowing to measure a difference by measuring the current flow without and with collected signal charges. As any readout is non-destructive, an additional contact is necessary to remove the signal charge from below the gate of the transistor.

Depending on the design parameters of the transistor, the conversion gain measured in current per charge is fixed, but also nonlinear conversion functions, for example to cover very high dynamic ranges by compressing large signals, can be implemented.

Arrays of DePFETs can be used as highly sensitive position-resolving detectors, but are expensive, due to their non-standard implant design and a huge number of required voltages and steering signals.

CHARGE COUPLED DEVICES One of the oldest, but still widely used techniques for the buildup of large pixel arrays for position-resolving detectors is the charge coupled device (CCD). The photons liberate electron-hole pairs in a regular depleted diode structure. But instead of feeding out the charge by dedicated wires for each pixel, an analog shift register is used: By special implants in the sensor bulk potential wells acting as a trap for the signal charges are created, and the electric field generated through an overlaid grid of wires raises or

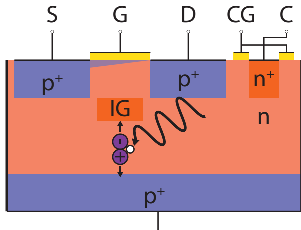


Figure 3.6: DePFET sensor cross section. The left part of the upper half is nearly identical to a classic PMOS transistor with its source (S), drain (D) and gate (G) contact. The n-implant below the gate forming the internal gate (IG) captures electrons from liberated electron-hole pairs and therefore modulates the p-channel if the transistor is turned on via its gate. On the upper right, the clear (C) and cleargate (CG) contacts are shown, which are used to remove collected charges from the internal gate. Like with regular diodes, the backside contact is used to deplete the sensing volume.

lowers the potential barrier in between two selected adjacent buckets, allowing the signal charge to flow from one well to another.

CCDs are used to build large arrays as the readout requires only one single analog to digital signal conversion, by shifting all signal charges to one edge of the array and then perpendicular to the signal output in one of the corners. Therefore, CCDs requiring one signal digitalization and only a few steering signals are very cheap, but on the other hand slow due to their serializing architecture while they do not provide any charge amplification.

ACTIVE PIXEL SENSORS With advancing miniaturization in complementary metal oxide semiconductor (CMOS) technology, a sensing device where each individual pixel is built of the collecting diode and further processing elements, like amplification or digitization, could be built, as a sufficient ratio between the photon sensitive absorption area and insensitive circuit areas could be achieved.

Named active pixel sensors (APSs) or, by their fabrication technology, CMOS sensors, an entire spectrum of sensors exist with an extensive range of included circuitry. With some designs, the photon sensitive diode area is placed next to the insensitive area where regular CMOS circuit elements reside, while with other designs, the entirely depleted bulk volume is used to liberate and collect charges which are further amplified and processed by the electronics placed at the surface layer [35].

4 EXPERIMENTAL TECHNIQUES

The experiments carried out with Synchrotron radiation can be categorized into four sets by the property of a sample they analyze:

IMAGING By exploiting the highly intense, focussed and short wavelength radiation and sometimes also its coherence, classic imaging techniques are used to analyze the *position* properties of a sample. Compared to electron microscopes, the penetration depth is larger and therefore allows to study internal properties. As the energy can be tuned, it can be matched to the absorption properties of the sample and therefore provide the best contrast. The experiments can be carried out by capturing full-field images or by exploiting the narrow beam size by using scanning techniques.

SPECTROSCOPY With an incident beam of monochromatic photons and by analyzing the *energy* of the emitted or absorbed photons, the electron motion and arrangement and also chemical bonding properties can be analyzed. Compared to other technologies, the ability to generate a steady monochromatic beam with tunable energy and small spot size is unique.

SCATTERING By analyzing the patterns produced by deflection of the incident photons their transferred *momentum* can be measured and therefore the atomic lattice of crystals or the molecule structure can be analyzed. Unique properties of Synchrotron radiation are their wavelength tunable to the range of atomic distances, high monochromatic flux, excellent collimation and a good angular resolution.

DYNAMICS Strictly speaking not a category of its own, the *time* variant dynamic properties of a sample can be analyzed using variants of the preceding experiment types. As the photons can be emitted by the Synchrotron in precise timed, very short pulses which can be combined with time resolving detectors, the progression in time is recorded.

In order to understand the various requirements deduced in the next chapter the XNAP detector should fulfill, some of the experimentation techniques routinely carried out at the ESRF are presented for reference.

4.1 COHERENT X-RAY DIFFRACTION IMAGING

In the domain of classical imaging techniques, switching from visible light to electrons lead to an increased magnification by orders of magnitude, allowing to analyze objects of sub-nanometer scale. Many different techniques are now commonly used for a detailed analysis of the surface, for example scanning electron microscopy (SEM) imaging, but as the penetration depth is very small, structural analysis is only possible by destructive slicing of the sample.

As a recent development, imaging with coherent X-rays is a complement to electron microscopy for the analysis of samples with several 10 nm resolution, without being limited to surface analysis or periodic crystal structures [29]. Recently, extrinsic effects like strain on external surfaces or interfaces between components of the sample were analyzed [36].

Due to the lensless nature, the general setup for coherent X-ray diffraction imaging (CXDI) is fairly simple, but has challenging demands to the source and the detector system: First, the source must provide a beam with high flux and coherence in the longitudinal and transverse domain for coherent scattering in the sample volume. Insufficient coherence leads to incoherent scattering and therefore only to an averaged projection of the scatterers in the sample. Second, to reconstruct the real image, the detector must be able to oversample the diffraction pattern to fulfill the Nyquist–Shannon sampling theorem. Combining both requirements, one can conclude that sampling an object of size x requires a beam coherence length in the order of x and an effective detector resolution of $x/2$. In order to reconstruct the real space image from the diffraction pattern, phase reconstruction algorithms are necessary as the pattern holds the magnitude information. Current algorithms require a lot of redundant pattern data of high contrast, whereas to cover a large solid angle, large detectors with small pixels in the vicinity of the sample are desirable. At current, CXDI experiments are carried out with classic CCD cameras. Radiation damage to the sample, as recording times in the order of several to tens of hours are common, is a major issue, especially for biological samples. With the development of short-pulsed FEL radiation sources, this could be avoided, but detectors with smaller pixels and faster readout are still favored.

4.2 NUCLEAR RESONANT SCATTERING

The family of experiments under the name of nuclear resonant scattering (NRS) is related to the recoilless emission and absorption of electromagnetic radiation by bound nuclei in a solid, known as the Mößbauer effect.

A specially selected Mößbauer isotope like ^{57}Fe in an excited state, for example by using the products of the radioactive decay of its parent isotope ^{57}Co, decays by the emission of gamma rays in a narrow spectrum to a lower energy level. For a free nucleus, a fraction of the transition energy goes into the recoil of the nucleus, therefore the energy of the gamma ray is reduced. However, if the nucleus is bound in the matrix of a solid, the effective mass receiving the recoil is the mass of the entire system. For modest decay energies therefore, virtually all energy is taken with the gamma photon, emitted solely with negligible recoil. Another nucleus of the same material but in the ground state can now absorb the photon if it is part of a solid matrix. This phenomenon of fluorescence is limited to a very sharp and well defined energy within the natural line width of the nuclear transition. If the source is accelerated and decelerated, therefore shifting the energy of the emitted photon by the Doppler effect, an absorption spectrum as a function of the velocity change can be measured, for an identical source and absorber with maximum absorption where the source is at rest and therefore the emitted photon energy matches exactly the energy needed for excitation of the absorber.

This type of measurement, called Mößbauer spectroscopy, is commonly used to probe energy levels in absorbing nuclei which are affected by the electronic and magnetic environment and chemical bonds.

Instead of using the limited number of parent isotopes decaying into suitable excited Mößbauer isotopes for the emission of gamma photons, the emission by a Synchrotron accelerator can be used to excite a sample [40]. This is more convenient as the energy range can be tuned and a specific beam of photons can be extracted using monochromators. A major difference between Mößbauer spectroscopy and NRS is the domain used to analyze emission or absorption: Classic Mößbauer spectroscopy is based on the Doppler shift induced frequency modulation, therefore the analysis takes place in the frequency domain as no time coincidence between the photon emission from the source and the absorption or re-emission cannot be made. For NRS, measurements in the time domain are used, as a correlation between the Synchrotron bunch clock and therefore between the exciting photons of constant energy and absorbed or re-emitted photons can be recorded.

Detectors used for the instrumentation of NRS experiments must either be sensitive to the delayed X-rays emitted from the excited nuclei if a nuclear forward scattering (NFS) type setup is used, or for the range of inelastic scattered photons centered at the previously mentioned elastic case, if the setup not of forward scattering type, for example with nuclear inelastic scattering (NIS) [38]. One common used energy is 14.413 keV for the resonance of the Mößbauer isotope ^{57}Fe. Further, the detector must provide the necessary time resolution in

the ns regime, as the excitation half-life time is, depending on the isotope, in the order of a few ns to a few 100 ns. Essential for forward scattering type experiments is the discrimination between the exciting, prompt and the fluorescent, delayed photons, which is done in the timing domain. Therefore, a mechanism to suppress the prompt photons by gating the detector, controlled by the timing system of the X-ray source itself, is necessary, but also a fast removal of collected prompt charges from the sensor itself in order to detect a typically lower number of delayed photons.

Earlier experimental setups have used Germanium detectors and scintillators coupled to PMTs. In the early 1990s, APDs were used the first time in the experiments. Since then, detectors based on APDs have become the standard instrumentation, but without significant changes in the detectors, development has slowed down [2].

4.3 X-RAY PHOTON CORRELATING SPECTROSCOPY

X-ray photon correlation spectroscopy (XPCS) as an experimentation technique is a recent development although the basic idea was already realized with dynamic light scattering (DLS) many years ago. The scattering in the sample volume of coherent light, emitted by lasers in DLS experiments or from Synchrotrons when referred as XPCS, creates speckle patterns with areas of constructive and destructive interference. As the scatterers in the sample vary over time, the speckle pattern also does and by recording time series and calculating their correlation, it is possible to deduce slow dynamics in the sample, at molecular scales. In addition to changes in the speckle pattern, a frequency change can be observed at the scattered photons which is related to the Doppler effect by the moving scatterers in the sample volume.

As the operating principle for DLS and XPCS is the same, the main challenge in the step from visible light to X-rays is related to the need for coherent light. Coherence lengths of several 100 m can be achieved with lasers, but in order to get coherence lengths of only 10 um in the X-ray regime, many improvements to the accelerator and the insertion devices were needed. Even today, XPCS is limited to some high flux, high coherence radiation facilities as most of the photons need to be masked out from the full beam in order to get the required transverse coherence.

For the instrumentation of XPCS experiments, a highly sensitive detector is necessary, as the typical count rate is very low. APDs are used for their single photon sensitivity, but in order reduce the area over which photons are integrated to a single signal, leading to a loss of contrast during the reconstruction, a pinhole is used that further reduces the number of collected photons. Also, APDs exhibit excep-

tional timing behavior allowing to analyze sample dynamics in the sub ns time scale.

Two-dimensional detectors like CCDs are also used today, allowing to record a large number of speckles in parallel, therefore reducing the time habitually needed for scanning with a point detector through the speckle pattern. The major disadvantage of standard CCD cameras, the longish readout time in the order of 1 s and therefore their poor frame rate, has been addressed with the development of dedicated photon counting detectors [28], decreasing the readout time by a factor of about 50. Still, the reconstruction by correlating the pixels in the time domain, is carried out independently for each pixel.

Part II

SPECIFICATION AND DESIGN OF THE DETECTOR SYSTEM

Driven by the requirements of novel experimental techniques, a specification for the detector is provided as the guideline for the following development process. A detailed view of the design and the subsequent implementation phases of various prototypes is given. The building blocks for the final detector system are illustrated, including alternative implementations for the bring-up and test phase prior to the final assembly and the current state of the detector implementation.

5 DETECTOR REQUIREMENTS AND CONSTRAINTS

The applications where the advantages of a fast pixelated detector system like XNAP can be demonstrated are currently using detectors based on CCDs or single element APDs [3]. Many of the requirements for the new system are therefore derived from the combination of the two current detectors and shifted towards technical limits, but others are entirely new to allow for new experimental setups.

5.1 PHOTON DETECTION ABILITIES

5.1.1 *Photonic properties*

The X-ray energy bandwidth where the detector must be effective is in the order of 5 keV to 20 keV, including the 14.413 keV frequently used for NRS experiments. Direct detection of these low energy X-rays must be possible without the need for a scintillating converter with sufficient efficiency.

The detector must provide single photon sensitivity with an internal signal amplification mechanism, but also a short recovery time after being hit by a photon to tolerate a large number of possibly unwanted primary photons up to 10^7 1/s at pixel and 10^9 1/s at detector level, and to capture a very small but interesting number of short spaced secondary photons. The recovery time must be smaller as the Synchrotron bunch separation time of 2.84 ns to resolve photons from individual bunches. The internal amplification should provide enough gain for easy processing of the electronic signal, but must keep a fixed relation to the photon energy to allow for later discrimination.

The pixel geometry should be optimized for amplification homogeneity with little photon loss at the radiation entry side. The gain variation between pixels and areas with entire photon loss should be as small as possible. For experiments requiring smaller pixels than the array provides, a method to reduce the effective pixel size to some 10 um by a pinhole mask should be foreseen.

The device thickness should provide a good tradeoff between detection efficiency, requiring large absorbing volumes, and charge drift time in the order of 1 ns, requiring devices with small drift volumes.

5.1.2 *Electronic properties*

The electronic signal from the sensor is fed into the ASIC which is connected to the readout controller, serving as the interface to the host computer. Electronic aspects therefore affect the ASIC, but also further parts in the readout chain.

By direct connection, the signal current is fed into a low impedance receiver circuit in order to not deteriorate the timing and hit rate properties of the sensor. The additional electronic noise floor should be kept below the equivalent of 5 keV X-rays. A per channel discrimination between noise background and the signal current with a global on-chip reference should also allow for a basic energy selectivity.

To be compatible with different sensor types, the receiver circuit should handle signal currents of both electrical polarities and its amplification should be switchable. There must be an independent threshold trim mechanism for each pixel to compensate variations both at sensor but also ASIC level. Defective or noisy sensor pixels and receivers must be individually masked out.

After signal amplitude discrimination and amplification to the electrical levels used by the digital circuit, some simple hit processing should take place: An electronic shutter common for all pixels must be implemented, with emphasis on short latency and low inter-pixel skew and jitter $\leqslant 500\,\text{ps}$, called *GATE*. The same timing constraints apply to the *VETO* functionality, globally switching between the operating modes, and to a digital hit injection mechanism called *INJ*, to characterize and tune the timing properties bypassing the analog part of the channel.

As required by the experiments, the detector should implement two readout modes:

LIST MODE For experiments with low occupancy, the position of every photon hitting the sensor is saved at the ASIC and signalled to the readout controller for timestamping, with high resolution in the order of 2 ns and low inter-pixel skew $\leqslant 500\,\text{ps}$. Until being read out and rearmed by the readout controller, hit signals by further photons must be discarded by the ASIC to guarantee data integrity.

COUNTING MODE For high occupancy experiments, the number of photons hitting the sensor are individually saved for each pixel at the ASIC. The maximum count rate should ideally be limited by the carrier drift time in the sensor, not by the speed of the ASIC electronics.

For counting mode, some flexibility should be implemented with multiple high dynamic range accumulators which should be able to be switched and read out at variable lengths without any deadtime.

An indication of photon overload, independent of the previously mentioned readout mechanisms, should be included for easy setup and monitoring of the experiment.

The fast electronic interfacing between the ASIC and the readout controller should use differential lines with common electrical levels matched for Xilinx FPGAs.

5.2 AMBIANCE CONSTRAINTS AND USABILITY

5.2.1 *Mechanical aspects*

The detector is built as a hybrid system, consisting of several individual pieces made of different materials adapted to the individual purpose. The Silicon sensor and the ASIC should be assembled on both sides of a support structure called *interposer* using interconnection techniques adapted to handling and assembly restrictions by the individual pieces. The interposer material should be chosen to match the thermal expansion of Silicon but also to maximize the X-ray shielding of the ASIC. The entire detector head should be as small as possible, with the sensor active area pushed to the edge of two adjacent borders.

The possibility of mounting the detector in the vacuum flight tube should be considered.

5.2.2 *Power and thermal aspects*

As the dark current, avalanche gain and breakdown of Silicon photodiode devices is dependent on the bulk temperature, it must be kept constant by the system itself. The thermal power dissipated by the ASIC should be minimized to a few 1 W, but as natural convection is limited by the compact detector, forced cooling is necessary. As both sensor and ASIC are coupled through the interposer, a single thermal control is sufficient.

Stabilization of the temperature should be done with a closed loop cooling system either with Peltier elements and appropriate sized heat sinks when operating in free air, or a closed water circuit and chiller.

The bias voltages required to operate the sensor should be regulated by the system according to the temperature.

5.2.2.1 *Connectivity*

With the focus on easy setup and operation, the detector system should be as much self-contained as possible. One power and one data connection should be the only required external cabling. All

supply voltages including the high voltage for sensor biasing should be generated and monitored by the detector itself.

Data connectivity should be implemented using common Ethernet technology using 1 Gbit/s transfer rate, with foreseen expansion of the data rate to 10 Gbit/s.

5.2.3 *User interaction*

Interaction with the detector should be done either by a standalone communication software running on a usual computer system without further dependencies, sufficient for simple tests. For advanced measurement set-ups, the detector should be integrated into the ESRF SPEC beamline control system [39], which then also handles persistent data storage.

6 DESIGN OF THE XNAP DETECTOR

6.1 OVERALL SYSTEM ARCHITECTURE

The target for the XNAP detector is to be an entirely self-contained detector system. As this involves many and in some extents divergent techniques, and also a demanding complexity, the detector is split into sub-components which are developed, manufactured and tested on their own before being integrated.

INTERPOSER ASSEMBLY The sensor converting incident electromagnetic radiation, the X-ray photons, and the very first piece of active electronics circuitry, the readout ASIC, are both made of Silicon. But the processing of the bulk Silicon to form a highly sensitive photon detector is different from what is necessary for high-speed low-power electronics circuitry. Therefore both devices are made with separate processes and then mated on a substrate, providing mechanical support and electrical connection between the components, to form the interposer assembly (Figure 6.1, Figure 6.2). Using a hybrid sensor/readout configuration also introduces the flexibility to use different sensor structures and sizes with the same ASIC.

FRONTEND BOARD The main purpose of the frontend board, a typical printed circuit board with some active components, is to supply power to the ASICs on the interposer assembly and to recondition its output signals (Figure 6.1, Figure 6.2). It also contains components to monitor the environment temperature and the operating current flows.

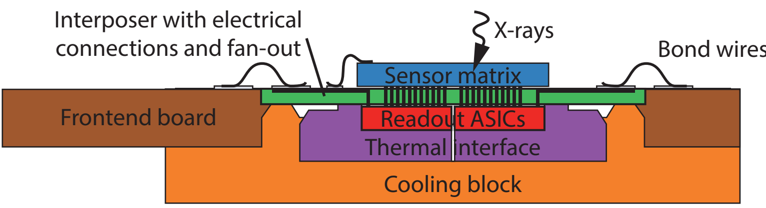


Figure 6.1: Schematic cross section of the XNAP 1k detector head.

READOUT BOARD The readout ASIC needs to be steered with precisely timed control signals, and also needs an endpoint capable of timing the hit signals and reading out the serial data stream. The

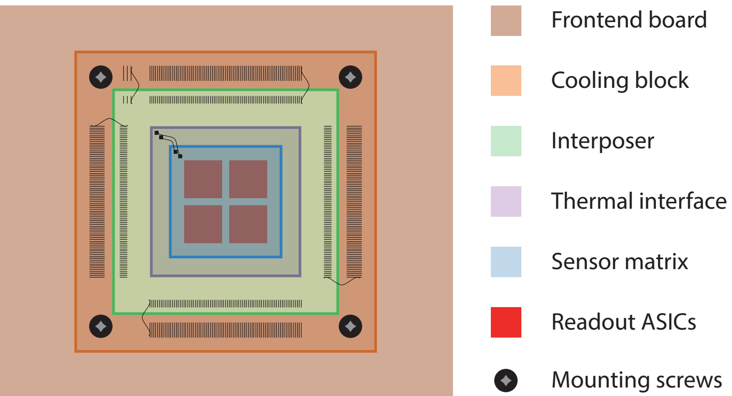


Figure 6.2: Schematic top view of the XNAP 1k detector head.

readout board therefore contains dedicated reconfigurable FPGA hardware and software components to acquire and process the raw data from the ASICs.

Once connected to a power source, the readout board takes care to provide the sensor and ASIC with correct supply and bias voltages, configure the ASIC with a predefined setting stored in its nonvolatile memory and then listens for commands on the network interface, the only data connection used for communication with the user.

COOLING AND HOUSING Several sensor properties like the number of dark counts and the leakage current are dependent on the Silicon bulk temperature. Also, the bias voltage to achieve constant amplification must be adjusted to the temperature. Even designed as a low power device, the readout ASIC dissipates significant amount of heat through the interposer. To remove the heat and stabilize the sensor at a given temperature, an active temperature control system is implemented, thermally connected to the backside of the ASICs (Figure 6.1, Figure 6.2).

To allow for easy installation and removal, the various pieces of the detector system are mounted into a rigid housing. No electrical or mechanical work should be needed by the user, apart from connecting power and data cables.

COMMUNICATION SOFTWARE All communication with the detector is done through a generic Ethernet network connection to the embedded processor on the readout board. As most of the data abstraction takes place in the readout board, the set of Python classes to interface with the readout board is fairly simple.

The detector can be used in standalone mode where data acquisition is controlled with a command line tool. For larger measurement

setups, a device server to integrate the detector into the beamline control system, which, apart from the beamline itself can also control other devices like position stages, is developed.

6.2 THE AVALANCHE PHOTODIODE SENSOR MATRIX

The sensor matrix within the detector uses a doped semiconductor structure called avalanche photodiode (APD) as the device sensitive to electromagnetic radiation in kind of X-ray photons. The two main variants of the APD structure were proposed in the mid-1960s and since then improved due to enhancements in semiconductor manufacturing lead by the microelectronics industry. A third structure was created some decades later as an optimized sensor for special detection tasks.

6.2.1 *Overview of APD device structures*

6.2.1.1 *Beveled edge structure*

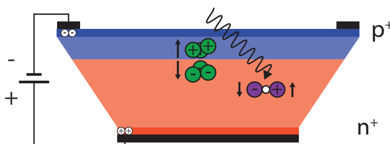


Figure 6.3: Schematic cross section of beveled edge type APD structure.

With a highly resistive substrate of n-type as the base material, an electron acceptor is diffused at a large depth to build an uniform junction up to the boundary of the device with low built-in electric field (Figure 6.3). To reduce the field along the edge of the device, the side walls are beveled, hence the name of the device. This APD type provides a very large and uniform amplification at low dark current and with a low excess noise factor, but requires high bias voltages above 1 kV. Under bias, the depletion extends away from the junction towards the back of the device, proportional to the square root of the applied voltage [37]. The structure is illuminated through the junction, therefore some charge carriers are lost if they are liberated in the undepleted area between the surface next to the light entry side and the junction.

The excess noise factor > 1 denotes how much the (electrical) shot noise is increased due to the stochastic avalanche multiplication process. It is a function of the ratio of impact ionization rates for holes and electrons.

This structure is suited to the detection of low energy photons, yielding to a low number of primary charge carriers liberated next to the junction and then amplified with high gain. Large devices can be produced.

6.2.1.2 *Reach through structure*

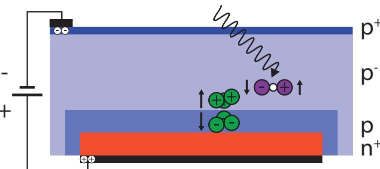


Figure 6.4: Schematic cross section of reachthrough type APD structure.

Starting with a highly resistive substrate of p-type, an electron acceptor is implanted (Figure 6.4). Then, the junction is built by implanting a shallow layer of electron donators in the previously built p-well. The shape of the wells and therefore the extent of the electric field can be very well defined, allowing for a field gradient towards the boundary of the device without any risk of spark discharges.

Photons enter the device from the side opposed to the junction. When biased, the depletion extends from the junction towards the light entry side up to full depletion (almost) without any area where liberated charge carriers are lost. Also, the field strength in the collecting volume, the drift area, can be kept constant reducing sensitivity differences due to different absorption depths as the amplification region is very narrow.

This structure provides less avalanche gain at higher dark current and a bigger excess noise factor than the beveled edge structure, but also typically operates at lower bias voltages of 500 V to fully deplete the device and provide decent amplification. It is suited for the detection of photons with higher energy, liberating more primary charge carriers but requiring thicker depleted devices due to the increased absorption length.

6.2.1.3 *Reverse structure*

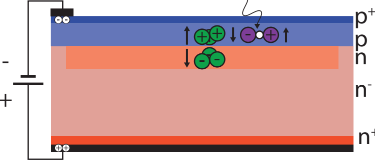


Figure 6.5: Schematic cross section of reverse type APD structure.

The overall structure for the reverse type APD is similar to the reach through device, but with the junction buried just below the front of

the device where the photons enter the device (Figure 6.5). This structure was developed for efficient detection of visible blue to near UV photons, as the absorption depth for these energies is very little, typically within the first 1 um of the detector.

The structure takes advantage for photons liberating charges near the junction. The dark current is only slightly amplified as most of the unwanted charges undergo little amplification due to the small hole ionization coefficient.

6.2.2 *APD optimization*

The dark current is a device characteristic governed by the geometrical properties and the doping profile, especially the ionization ratio $k = \beta/\alpha$, where α and β are the ionization coefficients for electrons and holes. One well-known optimization technique to lower the dark current and improve the signal timing is to use the primary electrons with their faster mobility to induce the avalanche gain by attracting signal electrons in the direction of the multiplication region with an appropriate electric field and heavily shifting the ionization rate towards the electrons. Other electrons in the bulk volume, away from the multiplication region, which drift due to the dark current, are collected without multiplication. The corresponding holes which are attracted to the multiplication region gain only little amplification due to a low hole ionization coefficient.

Typical electron mobility in Silicon at room temperature $m_e = 1400\,\mathrm{cm^2/Vs}$, *hole mobility* $m_h = 450\,\mathrm{cm^2/Vs}$.

The excess noise factor F is governed by the ionization ratio k, but also a function of the avalanche gain M and therefore dependent of the applied reverse bias [31]

$$F = k_{\mathrm{eff}}M + (1 - k_{\mathrm{eff}})\left(2 - \frac{1}{M}\right) \approx k_{\mathrm{eff}}M + 2 \qquad (6.1)$$

To optimize the devices for a fast overall response time, signal charges must be liberated in the fully depleted zones only where they drift up to the maximum drift velocity. The diffusion process outside the depleted areas is slow compared to drift, and has to be reduced as much as possible not to deteriorate the signal timing.

Also, by applying reverse bias to the device, the capacitance of the junction decreases by the widening depletion layer. The necessary reverse bias for depletion depends on the device thickness d and can be estimated for a known substrate doping N_D by [37]

$$V_{\mathrm{depletion}} = \frac{eN_D d^2}{2\epsilon_0 \epsilon_{Si}} \qquad (6.2)$$

The overall thickness of the device must match the photon energy, as an unnecessary thick device leads to a loss of responsiveness as the charge carriers transit through the detector volume. The speed

of this process is limited by the mobility for electron and hole charge carriers. Typically, the faster electrons govern the time resolution by the leading edge of the electronic signal, whereas the slower holes define the sensor deadtime by the current tail.

6.2.3 *APD structure choice for the XNAP detector*

As the XNAP detector does not involve a scintillator, it is required for the sensor to convert incident the X-rays an electric charge. The expected X-ray energy range of 5 keV to 20 keV corresponds to an attenuation length in Silicon between 18 um and $\approx$ 1 mm. Shallow sensing types like the reverse structure are not adequate for efficient detection, nor could the beveled edge structure be manufactured by the supplier, therefore the reach through type is chosen. The typical Silicon substrate thickness is far below 1 mm nor would such a large volume allow for good timing response, as the drift time for electrons through such a substrate would be more than 14 ns, even at 500 V bias voltage. A thinner sensor of 300 um reduces the transition time to the order of 1 ns, but also the detection efficiency to about 1/4 for 20 keV X-rays.

6.2.4 *Structures for pixelated APDs*

The principal goal when segmenting a zero-dimensional device into a one or two dimensional array is to be able to resolve the position of the incident photon from the processed electronic signal. For an ideal detector built of many entirely independent pixels, this would lead to an unique and pure representation of the position by the incident photon. Spatial and electrical constraints do not allow to build such a sensor for efficient detection, therefore a tradeoff has to be chosen.

For many sensor designs of pixelated type, it is sufficient to separate one of the two electrodes where the signal charges are carried out. The sensor arrays built of diodes therefore get their name from the electrode, anode or cathode, which is exclusively connected to one independent readout channel.

The reach through APD principally allows for four segmentation types: Either to be segmented on the electrode next to the p-n junction or next to the ohmic contact in the bulk volume. These two types can further be translated into physical structures where the high voltage bias has to be connected next to the segmented side or on the opposite light entry side. When connecting the high voltage bias at the segmented side the bias must be blocked from the readout ASIC, as its operating voltage is decades lower than the bias voltage. This can be done by capacitive coupling between the sensor and the input stage, but requires either a special high voltage withstanding ASIC technology if the coupling capacitor is built into the ASIC or a cou-

pling capacitor built into the sensor. Sometimes an external coupling capacitor is used, but this is impossible for sensors with dense contacts due to high channel numbers. Direct coupling without the need for a capacitor implies to bias the sensor at the electrode opposite to the readout, which is then shared across all pixels.

6.2.4.1 *Divided cathode sensor with junction side readout*

The APD structure where the cathode is segmented corresponds to a conservative approach (Figure 6.6). In order to not have the high voltage bias next to the pulse output pads facing the readout ASIC, the detector is biased at the light entry side with a negative voltage. The depletion induced by the bias extends from the junction at the bottom to the lightly doped volume at the top.

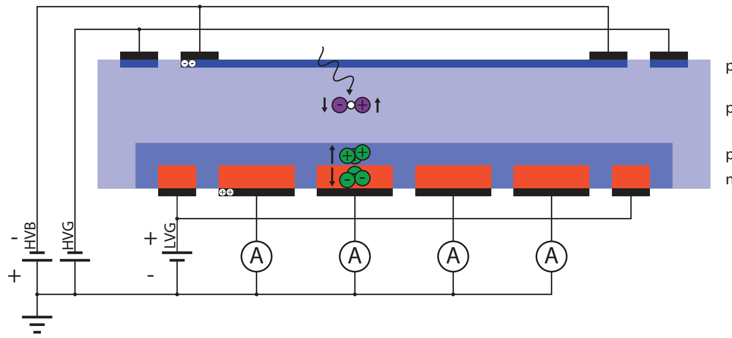


Figure 6.6: Schematic cross section of divided cathode type APD structure. HVB and HVG denote the connections to the high voltage bias respective guard power supply. LVG is the low voltage guard connection.

Incident photons traverse the thin and highly conductive layer at the top and liberate electron-hole pairs in the large depleted volume. Electrons are attracted to the p-n junction at the bottom due to the drift and liberate secondary electron-hole pairs. Holes are swept out of the detector at the top contact of the device.

The p-n junction itself is segmented by isolating discontinuities in the n^+ layer. A structural advantage is perfect isolation between the electrodes as the n^+-p-n^+ diode between pixel pads is always in reverse direction. Charge sharing at the border between the pixels is limited to the unamplified signal. The major disadvantage is the large dead area between individual junctions where the electric field must be reduced by adding extensive spacing between the p^+ implants and an additional channel stop implant.

Guard ring structures can be added at the light entry and pixel output side. At the light entry side, it is connected to the same negative

potential than the bias pad. Separating the two allows to measure the bulk leakage and the surface and boundary leakage by monitoring the two current flows. The guard structure at the output side, connected to the same potential as the output pads, provides the same environment to the pixels at the boundary than is present next to the inner pixels and also removes stray charges in the periphery. The top guard ring does not improve the signal at the output, but the bottom guard ring does, by sweeping out unwanted charge carriers due to leakage.

6.2.4.2 *Divided anode sensor with ohmic side readout*

The divided anode APD structure is a rather aggressive approach (Figure 6.7). The sensor is biased at the light entry side with positive voltage. Depletion extends from the junction at the top of the device towards the segmented output pads at the bottom.

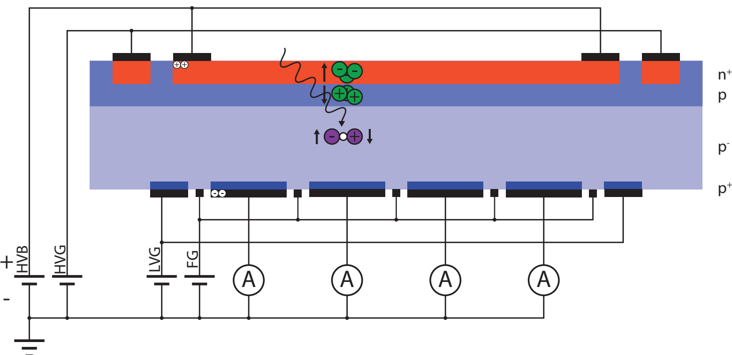


Figure 6.7: Schematic cross section of divided anode type APD structure. HVB and HVG denote the connections to the high voltage bias respective guard power supply. LVG is the low voltage guard connection. FG denotes the field grid connection.

The photons traverse the n^+-p junction at the light entry side of the device. Special care is taken for the implant to reduce the thickness of the n^+ layer as well as the overall longitudinal dimension to the absolute minimum to minimize losses at the entry side. In the depleted bulk volume located below the junction, photons liberate electron-hole pairs. Holes are swept out to the pixel pads at the bottom of the device. The electrons are accelerated to the junction and liberate secondary electron-hole pairs.

The amplification area, the p-n junction, is one continuous layer. Primary as well as secondary holes from the avalanche process drift across the silicon volume to the p^+ pads at the bottom of the device.

The major advantage in this structure is the homogeneity in the amplification area. There is no low-field gap, all primary electrons

liberate (almost) independent of their location a large number of secondary charges. As the p^{+}-p-p^{+} interface between the output pads does not contain a diode junction, the resistivity between the contacts depends on the number of free charge carriers in the p section. Without depletion, the inter-electrode resistivity is low, roughly 1 kOhm. When the silicon volume depletes by the applied bias voltage, the resistance between the electrodes increases as free charge carriers are swept out of the area. Therefore, the sensor can only operate with applied bias, otherwise all output pads would be shorted.

As an improvement, very thin grid lines are applied on the Silicon surface next to the output pads. Connecting a positive voltage to this field grid pushes charge carriers out of the gap between the electrode and therefore increases significantly the resistance.

The same guard structures as for the divided cathode sensor type are built on top of the light entry and pixel output surface. Although their implants differ, the functionality is the same: Separate measurement of surface/edge and bulk leakage current, and electric shielding of the output signal.

6.2.5 *Electronic modeling of the sensor for simulation purpose*

In order to develop and optimize the signal current receiver circuit in the ASIC, the electronic characteristics of the sensor must be modeled to be able to simulate the combination of sensor and readout electronics.

Recently, complex modeling of APD devices is accomplished [20], but the usage of these models requires an in-depth knowledge of physical parameters. Different parameter sets are evaluated by the sensor manufacturer to optimize its performance, but their values are not available due to licensing restrictions.

Instead, a simplified model for the output signal is derived, focusing on the signal output (Figure 6.8).

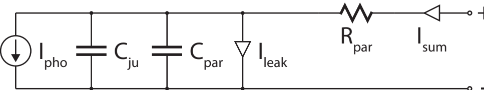


Figure 6.8: Simplified electronic model for the APD device.

In the simplified electronic model, the primary photocurrent as well as the current due to the amplifying avalanche is combined to a single current source I_{pho}. It is assumed that the current pulse is of triangular shape with an equal rise and fall time of 1 ns. The bias voltage dependent junction capacitance C_{ju} as well as all other parasitic capacitances combined in C_{par} are connected in parallel to the

current source. The sensor dark current as well as all leakage currents are summed in I_{leak} connected in parallel to the photocurrent source. Finally, resistive parasitic elements are collected in R_{par}, which feeds the total sensor current I_{sum} to the terminal.

For the intended X-ray energies of 5 keV to 20 keV, about 3.6 eV are required to liberate one electron-hole pair in the Silicon volume. Therefore a primary charge in the range of about 1300 e-h pairs to 5500 e-h pairs is liberated, which corresponds to a current of about 100 nA to 450 nA for the expected pulse shape. The internal avalanche gain depends on the applied reverse bias with typical values in the order of $10\times$ to $100\times$. Hence, the signal amplitude for the amplified current is assumed to be in the range of 1 uA to 50 uA.

A value of 100 fF is assumed as the per pixel sensor capacitance at full depletion of the Silicon volume.

For the total dark current which is dominated by the bulk leakage partially multiplied by the avalanche gain, a per pixel current two orders of magnitude less than the signal current is assumed, therefore in the order of a few 10 nA per pixel input.

6.3 SENSOR MATRIX READOUT ASIC

The avalanche photodiode array (APA) readout ASIC evolved from a four-channel circuit test design (revision 1.x) over a a 4×4 matrix readout (2.x) to a 16×16 two-side abuttable chip. The latest 3.x generation contains 256 pixels which are identical for their analog front-end, but individual in the digital readout chain. Previous versions of the APA ASIC included only part of the circuitry and/or less channels, therefore they are not described here in detail. A table of all built ASICs with some details on the functionality is presented in Appendix B.

Common for all versions of the ASIC is the physical design and implementation. For the design process, the Cadence Virtuoso electronic design automation (EDA) tools are used. The Silicon devices are implemented in the UMC 180 nm mixed mode process using one polysilicon and six metal layers and fabricated on multiproject wafer runs via the Europractice prototyping service [9]. The latter limits the Silicon die size to $5\,mm \times 5\,mm$.

The ASIC integrates multiple tasks which, with the current hardware present at the ESRF beamlines, are distributed over multiple devices: First, the signal from the APD pixel is received and amplified. Then, it is compared to a threshold setting and then routed either to the hit storage or a counter. Both memory structures are subsequently read out by a fully digital backend and transferred to the host computer.

6.3.1 *Circuit description*

The ASIC circuit can be partitioned depending on the logical operation method into an analog and digital part, while the digital part contains distinct blocks for the list mode and the counting mode. In Figure 6.9, blocks which logically operate in the analog domain are marked green, while digitally operating blocks are blue, red and yellow. The yellow ones are specific for the readout in list mode while the red ones for readout in counting mode. Blocks required for configuration and biasing are omitted in the signal flow schematic.

6.3.1.1 *Input selection and fast current pulse amplification*

The electronic signal from the APD hit by a photon is a current pulse, overlaid to the inevitable dark current from the sensor. The rising edge of the current signal solely depends on the physical properties of the APD, the Silicon thickness and the charge carrier velocity, but the trailing edge not only depends on the sensor, but also on the impedance of the interconnection and the receiving circuit. To read out the current pulse from the APD, a transimpedance amplifier (TIA) is chosen as the input stage. This type of amplifier converts the current fed into its input to a proportional voltage at its output with a given proportionality factor, the transimpedance gain $Z_t = v_{out}/i_{in}$. Ideally, the input impedance is low to allow for fast current flow while the output impedance is significantly higher, isolating the output node from the input. Compared to other amplifier types, for example charge sensitive amplifiers (CSAs), TIAs typically have a faster impulse response and do not require an additional reset mechanism, making them well suited for the reception of repeated short pulses.

Prior to the amplifier, an analog input switch built of n-channel metal oxide semiconductor (NMOS) pass gates allows to route the current from the pixel input to the amplifier or to connect a chip-wide testbus, either direct or via a resistor for current injection (Figure 6.10). Also, the pixel input and thus the sensor pixel, can be connected to the testbus.

The active part of the TIA is built of an NMOS transistor common source amplifier with a PMOS transistor current mirror as active load (Figure 6.10). The primary branch of the current mirror is shared across all pixels and connected to a current mode digital to analog converter (DAC) with global programming named *DACTIA*. As the amplifier is optimized for high bandwidth, the open loop gain is rather low, in the order of -20. With a typical bias of $100\,\text{uA}$, the DC operating point is at $470\,\text{mV}$.

A purely resistive feedback is added from the output of the inverting amplifier to the current input to complete the TIA structure (Figure 6.10). The feedback network is built of a chain of one, two or four series-connected interleaved unit resistors of $2\,\text{kOhm}$, which

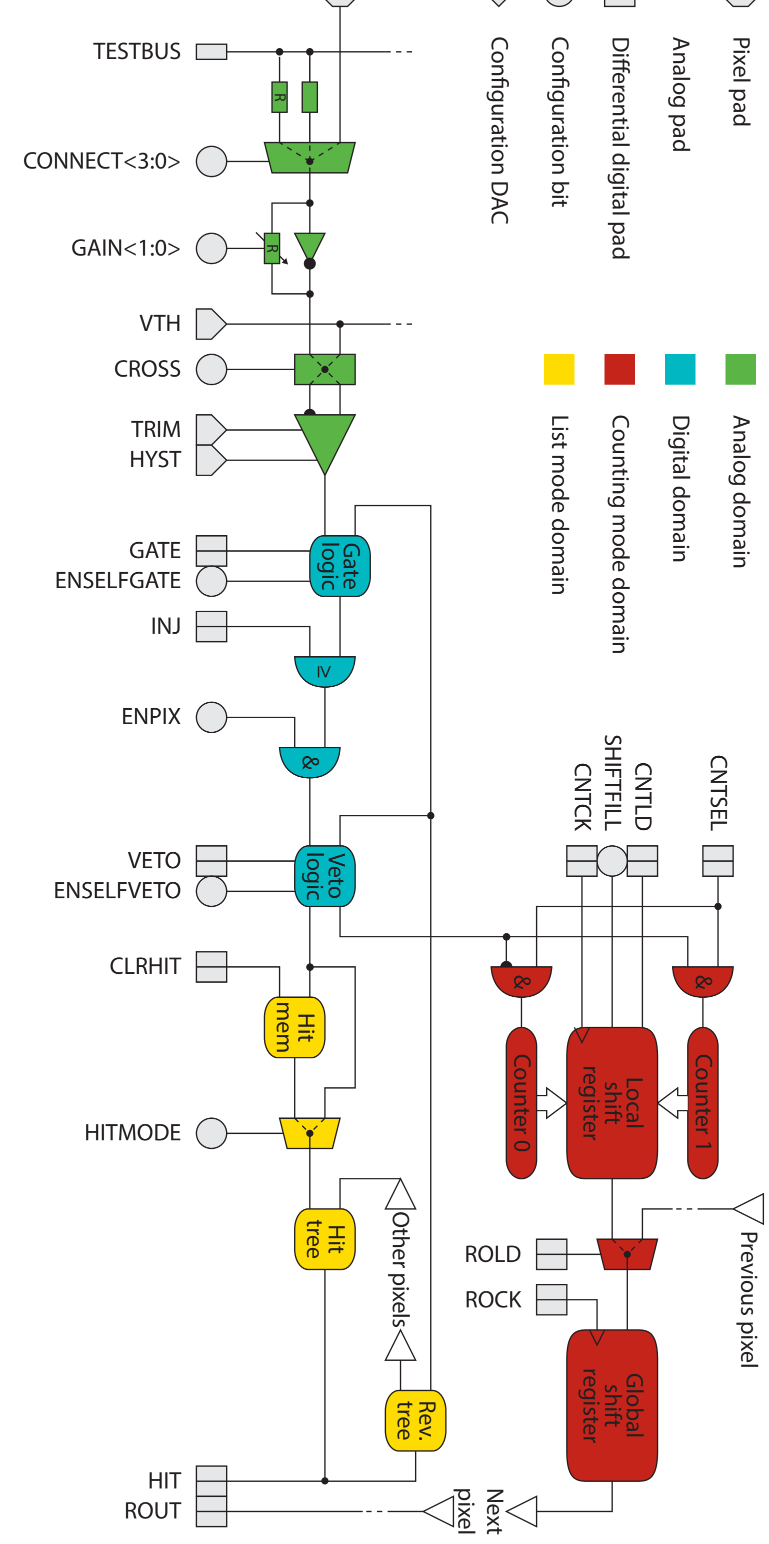


Figure 6.9: Schematic signal flow and partitioning of the APA 3 ASIC family.

can be shorted using two pass-gates to select a feedback resistance R_f from the discrete set of 2 kOhm, 6 kOhm, 10 kOhm or 14 kOhm. The unit resistors are implemented using salicide-blocked p^+ polysilicon structures, as they provide the least voltage and temperature variance for the given fabrication technology, which is still ±25 % related to the absolute value. When shorted, the residual switch resistance is in the order of 130 Ohm per gate.

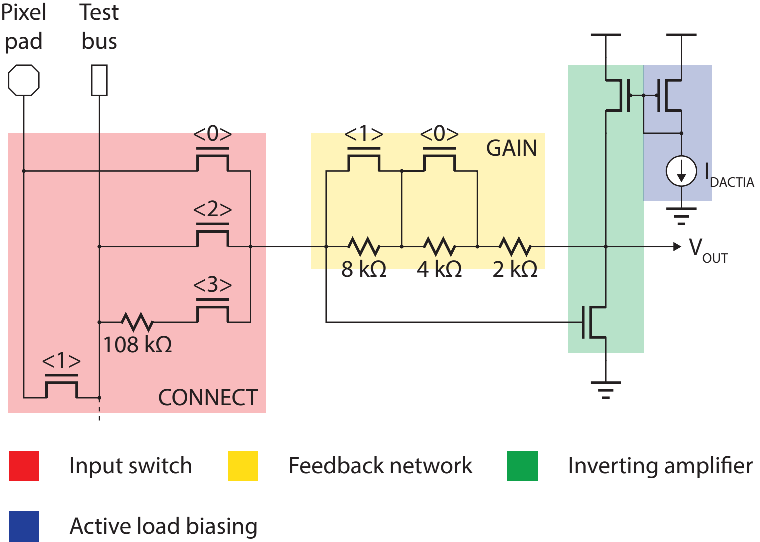


Figure 6.10: Schematic of the input stage circuit. The signal input switch is marked red. The TIA consists of the common source amplifier in green and the feedback network in yellow. The shared active load biasing is marked blue. The number in angle brackets indicates the bit position in the control signal word.

Simulations of the noise behavior carried out that in low gain mode, the major noise source is the thermal noise of the feedback resistor, whereas in high gain mode, the r_{ds} thermal noise of the amplifying transistor dominates. The total input referred noise current $i_{n,rms}$ is estimated to about 233 nA in the low gain and 490 nA in the high gain mode in the DC to 2 GHz band.

In an iterative process, the physical layout of the input stage is optimized using the parasitic enhanced model to reduce unwanted stray capacitance and the risk for pixel to pixel mismatch. Common centroid layout as well as additional dummy structures and antenna diodes are connected to improve matching. Additional feedback capacitance for stability of the TIA is not necessary and is abandoned in order to not reduce the amplifier bandwidth.

The four CMOS local control signals *CONNECT* for the input switch are buffered in every pixel, as well as the two local control signals

GAIN for the feedback network, which are only inverted for intuitive value encoding.

6.3.1.2 *Signal to noise discrimination*

The voltage pulse at the output of the TIA is the sum of the converted photo- and the dark current, overlaid with noise from the sensor itself, but also from the input amplifier. To be able to detect the photon events only, the signal therefore needs to be compared to an adjustable threshold.

The threshold voltage is generated from an on-chip reference circuit and can be adjusted by programming the global *DACTH* setting in a certain range. Prior to the comparison of the TIA output and the reference voltage, their polarity can be swapped, to be compatible with both divided anode and divided cathode APDs, as their current pulses are of different polarity and therefore also the voltage pulses at the TIA output. This is implemented with an NMOS only cross switch, controlled by the local *CROSS* control signal which is buffered in every pixel.

The pulse comparison is implemented with a fully differential pure NMOS discriminator, consisting of three building blocks (Figure 6.11): First, the reference voltage VTH and the signal voltage VIN are connected to a fully differential amplifier. The branch where the voltages are fed into the amplifier depends on the *CROSS* setting:

The polarity of the CROSS *setting is modified a number of times between the ASIC as the default value of 0 should correlate to the default sensor.*

- *CROSS* is 0: VTH is connected to the positive, VIN to the negative branch. The logical result is therefore VTH-VIN.
- *CROSS* is 1: VIN is connected to the positive, VTH to the negative branch. The logical result is therefore VIN-VTH.

The tail current I_{TAIL}, which is the sum of the branch currents I_{LEFT} and I_{RIGHT}, can be adjusted by programming the global *DACDISC* value, typically to 100 uA. Next, to compensate per pixel level variation at the sensor and also the ASIC, each discriminator can be adjusted by subtracting a trim current I_{TRIMP} and I_{TRIMN} from the left and the right branch of the differential amplifier via the corresponding current mirror. The trim range is set with the global *DACTRIM* parameter while for each pixel, the *DACTRIML* setting defines the per pixel bipolar correction current. The third building block adds a programmable hysteresis to the output of the discriminator by a positive feedback loop. An additional tail current $I_{HYSTTAIL}$ flows through the load diodes, which can be set globally with the *DACHYST* setting. The width of the hysteresis window can be adjusted to an equivalent input current between several 100 nA to several 10 uA, depending on the *GAIN* setting of the TIA.

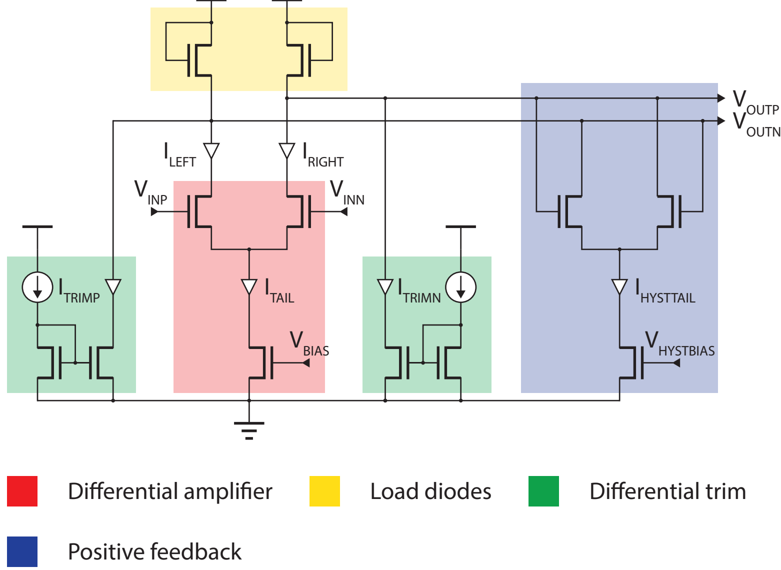


Figure 6.11: Schematic of the differential discriminator circuit. The differential amplifier with its current source is marked red. Both current mirrors for threshold trimming are marked green, and the positive feedback hysteresis circuit is marked blue. The load diodes, one per output, are marked yellow.

6.3.1.3 *Amplification and level shifting*

The discriminator itself applies some amplification to the differential voltage present between the input and reference input. For further improvement of the signal, it is amplified in a chain of four fully differential amplifiers, which are simplified versions of the comparator, lacking the trim mirrors (green marked parts in Figure 6.11) and the differential pair used for the hysteresis (marked blue in Figure 6.11). As the differential pair with its current source and the load diodes are exact replicas of the discriminator, the bias voltage to define I_{TAIL} is shared with the discriminator.

Including the discriminator gain, the total differential voltage amplification is up to the order of $30\,\times$.

When biased with a current of 100 uA, the common mode voltage of the output signal is about 900 mV, which must be reduced in order to fit the following circuit stages, operating at a lower supply and therefore lower common mode voltage. An NMOS source follower with NMOS load is chained at each of the two differential amplifier outputs, shifting the common mode voltage down by about 300 mV without major reduction on the differential gain (Figure 6.12).

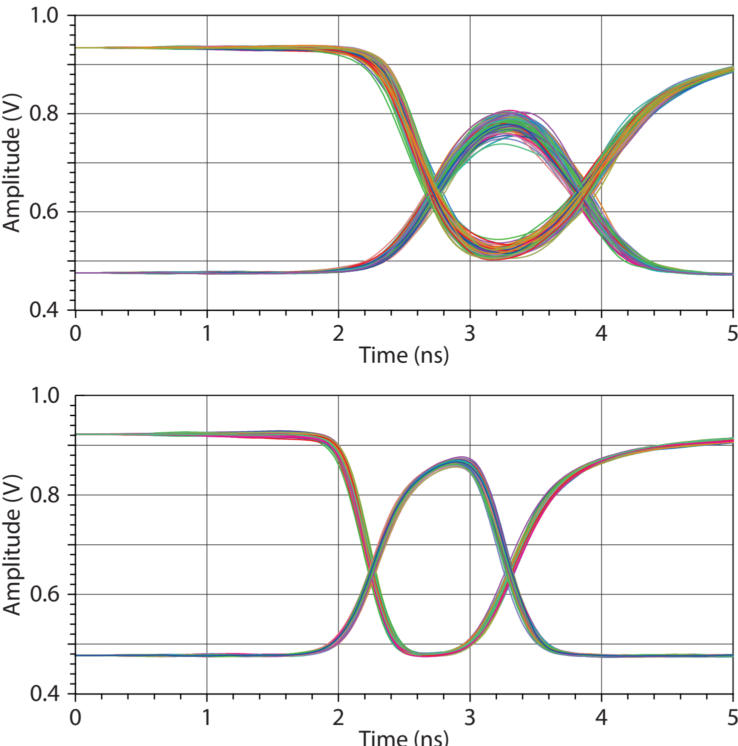


Figure 6.12: Simulation of the differential output signal as the frontend response to a triangular current pulse of 2 uA in high gain (top) and of 20 uA in low gain mode (bottom), with 1 ns rise and fall times, centered at $t = 2$ ns. The threshold is set to half of the signal amplitude. Overlaid results from 100 simulation runs including electronics noise.

6.3.1.4 *Digital processing*

The raw hit signal, which is approximately a square pulse of very short duration, as it is not stretched in the analog domain, is processed further in the digital domain. To profit from the differential architecture of the ASIC in the previous signal path, the digital processing is implemented in a differential logic named differential current-mode logic (DCL). At the cost of doubling all metal wiring and slightly larger cells, interference into the sensitive analog part is reduced. Also, some gates are internally simplified to take advantage of easy inversion of the input signal by swapping the two wires: For example, an inverter is a simple buffer with mutual exchange of the two input wires. For details on the DCL, see Appendix A.

The hit processing implements four major tasks (Figure 6.13):

ELECTRONIC SHUTTER The low latency, low jitter electronic shutter is implemented as the conjunction of the raw hit pulse and a gate

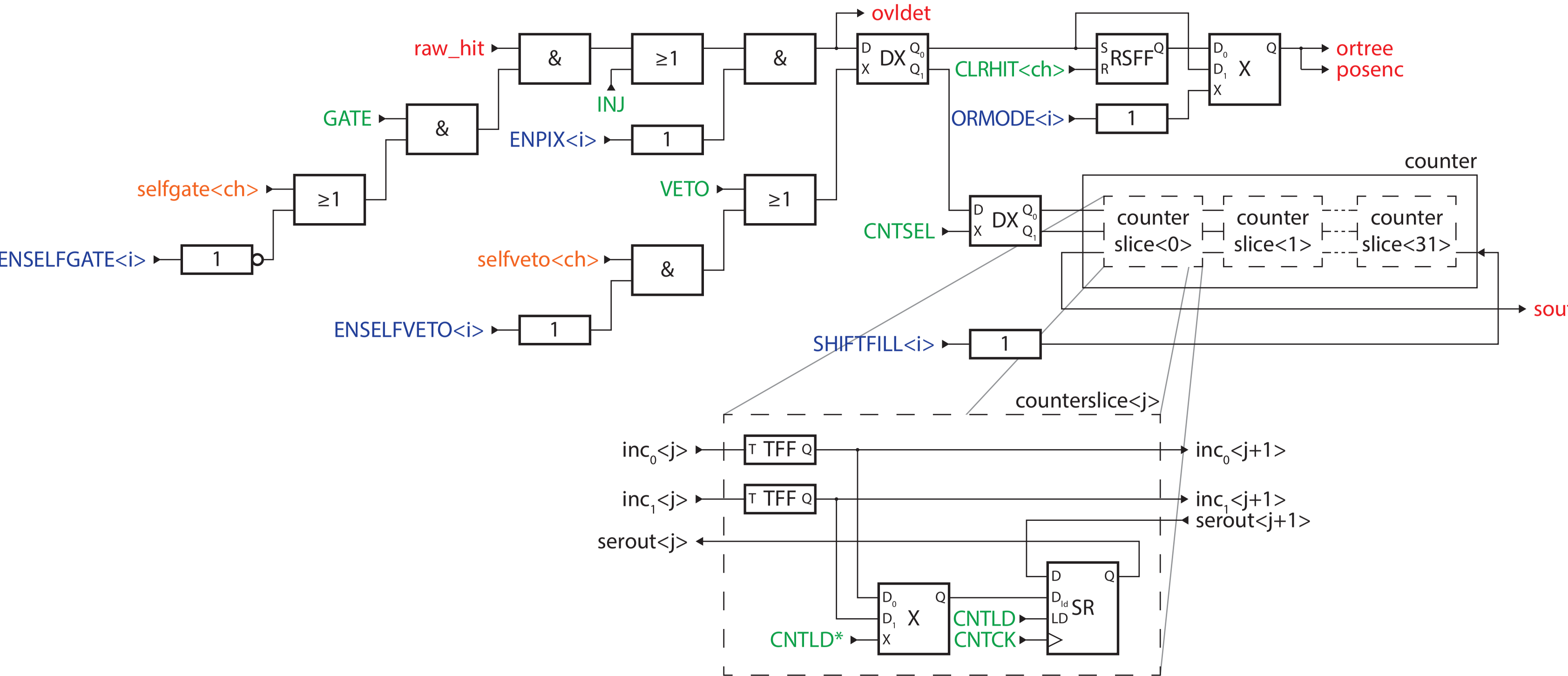


Figure 6.13: Digital hit processing in the APA 3 ASIC. Main input and output signals are in red, static configuration bits are marked blue, external differential signals green and internal feedback signals orange. From the discriminator, the hit pulse *raw_hit* enters at the left. An intermediate signal *ovldet* leaves towards the integrating overload detector, while the outputs to the OR tree *ortree*, the position encoder *posenc* and the readout shift register *sout* are at the right.

signal. The latter is generated internally from the chip input *GATE* and the selfgating mechanism. If both components are *high*, the shutter is open and hits can propagate further. The selfgating, which feeds back the hit signal of the corresponding readout channel to disable further hits if a stored hit is not yet readout, therefore reducing the risk of false hits, but can be disabled with the *ENSELFGATE* pixel configuration bit. The bit is internally inverted and shifted to DCL level, therefore if the bit is 0, only the global gating is relevant, while if the bit is 1, global and selfgating are active.

DIGITAL TEST INJECTION For testing of the digital processing and the readout channels without involving the analog front-end, a global input *INJ* is added by disjunction. During normal operation, this input must be fixed *low*.

PIXEL-BY-PIXEL MASK The digital output of each pixel can digitally be disabled by writing the bit *ENPIX*. The bit is converted to DCL level and then conjunctively combined. Disabling a pixel does not affect the preceding (analog) part, therefore does not influence the total power consumption.

At this point in the signal path, an intermediate tap is provided for the in-pixel overload detector.

MODE SWITCH With the same timing properties as the electronic shutter, the mode switch is implemented by demultiplexing the hit signal either to the list mode or to the counting mode path. The veto signal, which acts as the control of the demultiplexer, is generated internally from the chip input *VETO* in disjunction with the selfvetoing. The latter is the result from the readout channel wise feedback from the hit memory in conjunction with a level-converted control bit *ENSELFVETO*. If the bit is 1, further hit pulses are routed to the counting mode domain until the hit memory is cleared.

6.3.1.5 *Hit combining and position encoding*

Feeding out individual hit signals for all pixels is neither reasonable nor technically possible due to the limited number of connections at the ASIC boundary. Therefore, a reduction to a signal carrying the timing property and an encoded storage of the origin is implemented.

The reduction function itself influences the timing behavior of the output signal by the number of logic gates in the signal path, but also by the length of the metal traces and necessary signal buffers to drive them within given constraints for the slew rate.

Beginning with the 3.1 generation of the APA ASIC, the reduction is implemented as an upside-down perfect binary tree of OR gates without synchronous logic cells or memory elements. The outstanding benefit is a position-independent propagation time from the in-

put, a leaf node, to the output, the root node of the reduction tree, as the number of involved gates in a perfect binary tree with n inputs is constant with $\lceil \log_2 n \rceil$.

The pixel cells in the APA 3.x ASICs are organized in eight columns and eight rows named *A* to *H*. Each element in this matrix contains a block of four pixels: 0 or red in the upper left, 1 or green in the upper right, 2 or blue in the lower left and 3 or yellow in the lower right. The number indicates to which readout chain the particular pixel belongs. At the cost of increased wiring, the pixels are evenly spread across the ASIC to reduce the risk of event pileup in a particular readout channel.

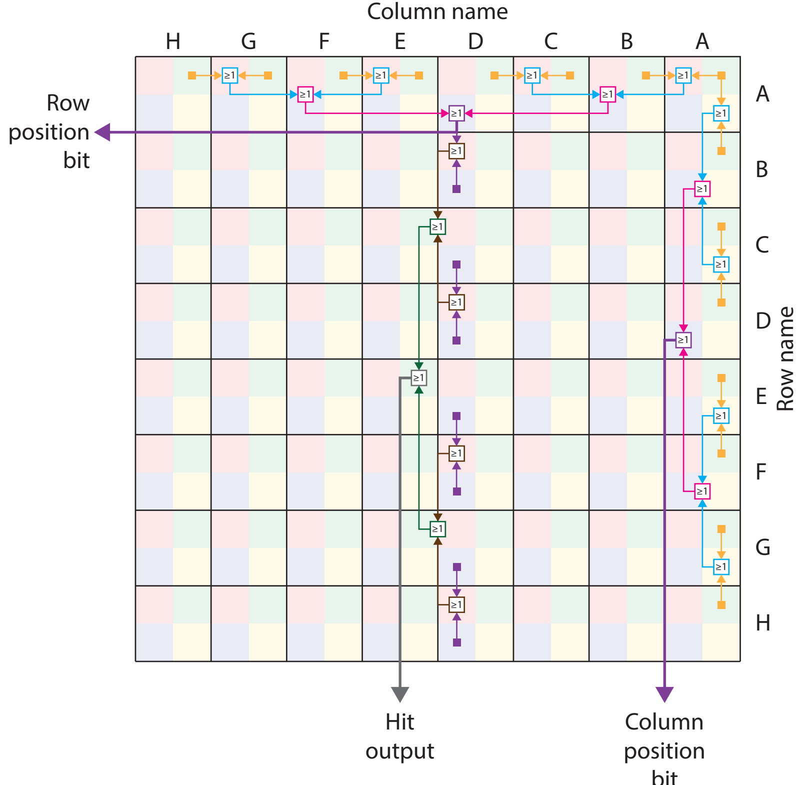


Figure 6.14: Simplified schematic of the OR tree. For one of the four pixels in each block, the reduction tree in column *A* and in row *A* is shown.

The OR tree and auxiliary structures are replicated four times, for each readout channel consisting of 64 pixels in the 8×8 sub-matrix. The tree itself is made of three items (Figure 6.14):

- A single column tree reducing eight pixel inputs (in yellow) in a column to one output (in purple) using a three-stage subtree
- A single row tree reducing eight pixel inputs (in yellow) in a row to one output (in purple) using a three-stage subtree

- A single row combiner tree reducing eight row tree outputs (in purple) to one output (in grey) using a three-stage subtree

Each OR tree has three outputs: The row position is fed out to the readout register as an intermediate output before being further combined with all other columns to add up as the hit signal, which is routed to an output buffer at the chip boundary. The column position is also connected to the readout register.

6.3.1.6 *Pulse counting*

With the design target of low power consumption while keeping the ability to count pulses with multiple 100 MHz, a simple yet powerful approach is taken. The process of counting incoming pulses itself is done with toggle flipflops: A logic gate structure which toggles the output value between low and high with every incoming pulse cycle, effectively reducing the pulse rate at the output to half of the input rate.

To allow for deadtime free counting and read out, two independent counters are present in each pixel and an external signal *CNTSEL* is used to switch between them. For accurate timing, the select signal is implemented as a perfect binary tree which guarantees by design equal signal propagation time between all pixels.

The counter itself is made of slices containing two sets of toggle flipflops and a common multiplexer and shift register cell (Figure 6.13). Each pixel contains 32 slices: The five least significant bits (LSBs) are built of toggle flipflops with *HP* logic cells allowing for fast operation. Taking advantage that each slice halves the toggle signal which has to be fed into the next stage and at which the slice has to operate, the sixth, only toggling at 1/32 of the primary rate, and all following slices are built of *LP* logic cells saving a vast amount of operating power. For simplification, the toggle flipflops miss a reset mechanism. Their initial state, random at power-up, must therefore be read out once ahead of the first counting cycle and then subtracted from the pulse count result.

The readout of the counter slices takes place by transfer of the toggle bits to a 32 bit parallel in, serial out shift register. The multiplexer selecting which of the two toggle flipflop chains is loaded to the shift register is implemented in an optimized, non-standard way of reusing the load and clock lines of the shift register.

The LSB output of the shift register holding the LSB of the toggle flipflops is routed in each pixel to the readout register. As the process of latching the values from the toggle flipflops and shifting them towards the output are controlled using two independent signals, *CNTLD* to load the values and *CNTCK* to shift them by one bit, it is possible to read out any number of bits from the pixel counters. Therefore, it is possible to optimize the readout time for the application case: Either to read out a large word from the counter requiring

more readout time or to read out only a few bits, requiring significant less readout time.

For testing purposes, the last input in the pixel shift register is connected to a logic signal *SHIFTFILL*, which can be set individually in each pixel using the configuration interface.

6.3.1.7 *Fast data input/output interface*

The acquisition is transferred out of the ASIC into the readout controller (ROC) via two interfaces:

The hit output *HIT* carries a single bit information that a photon hit is recorded in the appropriate channel, but also its time of arrival as the analog delay. The hit pulse is not synchronized to any timebase, the timing of its leading edge is purely determined by the arrival of the signal pulse. The ROC must acknowledge the hit by pulsing the *CLRHIT* signal which clears the hit flipflop, and, if the selfgate or selfveto mechanism is enabled, therefore re-enables the detector. The two signals *HIT* and *CLRHIT* are dedicated to each readout channel, therefore four pairs exist in the APA 3.x ASIC.

All other information is transferred as a serial data stream out of the *ROUT* port. The ASIC serializes the data using a parallel in, serial out shift register built of fast *HP* DCL logic and special line driver cells allowing for multiple 100 MHz operation speed (Figure 6.15). The shift register is steered externally with two signals, *ROLD* to load the data from its source into the shift register and *ROCK* to shift the serial word by one bit position towards the output. At the beginning of the register, a constant header with the binary values *0* and *1* is prefixed to the stream to allow the receiver to synchronize its deserializer to the data bits. After the header, the register contains eight row position bits and eight column position bits out of the respective OR tree. Therefore, to get the time and position of an event, it is sufficient to capture the leading edge of the *HIT* signal and to shift out 18 bits out of the readout register.

In order to read out the pixel counter data, more cycles are needed: The LSB of each pixel counter shift register is connected to the input of the readout shift register, which is routed in a snake shape across the matrix of 64 pixels. To transfer only the counter LSB, which can be captured to the pixel shift register using the *CNTLD* port, 18 plus 64 cycles are necessary. Using the *CNTCK* signal, all pixel shift registers are shifted by one bit, so the next *ROLD* pulse loads the second to *LSB* bit to the readout shift register, which can then be shifted out by clocking the *ROCK* port. As all four load and clock lines are operated by the ROC, the number of transferred pixel counter bits can be adjusted to the needs during each readout cycle.

For testing and adjustment purposes, both the readout shift register and the pixel counter shift register have their last input connected to a configurable fill bit.

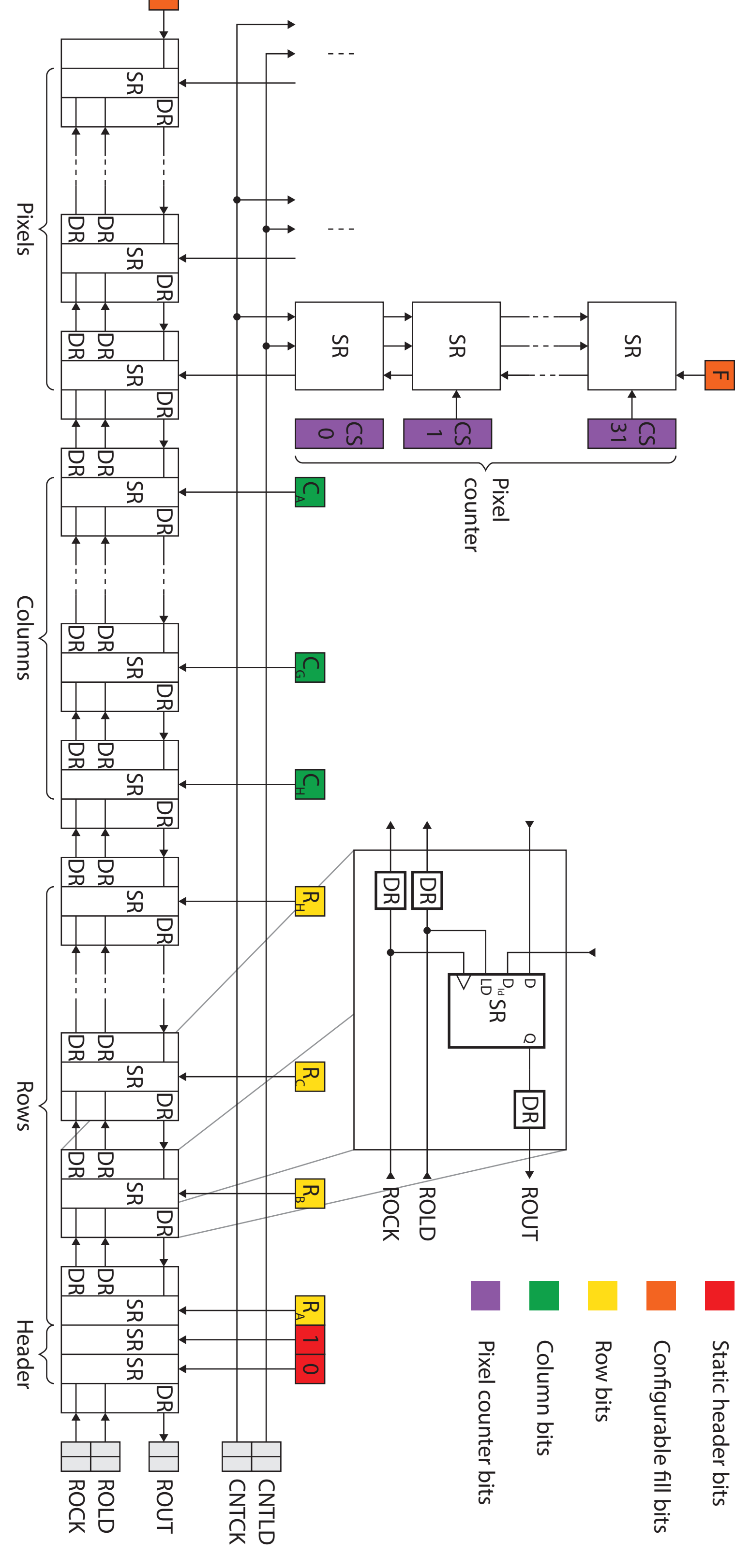


Figure 6.15: Schematic of the fast readout register of the APA 3 ASIC family. SR denotes a shift register bit while DR a line driver.

6.3.1.8 *Pulse overload detection*

Apart from the two outputs to transfer the acquired hit information, a third output *OVLOUT* is aimed as an alarm signal if the detector is irradiated with too much photons. Targeted with very little power consumption, this part of the ASIC uses standard CMOS gates and very small transistors, as there is no time critical information.

In each pixel, the hit output is routed towards the overload detector in parallel to the demultiplexer switching between list and counting mode readout, therefore the circuit operates independent from that mode switch. The differential hit signal is converted by subtraction to a single ground referenced voltage, which is then smoothed by a RC low pass filter with a time constant in the order of 60 ns.

A global threshold can be set using the configuration interface, which is distributed as a voltage to each pixel. The smoothed voltage is compared to this threshold voltage with a differential amplifier with built-in hysteresis, and then amplified to logic level by an inverter. A simple OR chain combines all of these signals and is then fed to the ASIC boundary.

6.3.1.9 *Circuit biasing and slow configuration interface*

For proper operation, many cells in the ASIC need a bias current or voltage. This is not only limited to the *analog* part of the design, but also applies to the *digital* part using DCL gates, as they require, in contradiction to simple CMOS gates, two biases. A design choice might be to fully trust the Silicon foundry supplied simulation models and fix the bias values using unalterable resistors, which is from the implementation point of view the simplest solution. Another more flexible approach is to integrate programmable current or voltage sources to generate the biasing so that it can be altered in a given range at operating time.

The APA ASICs use the latter approach, as a 12 bit current mode DAC cell was previously designed as parameterized macro cell (PCELL) and successfully used within other ASICs. The cell operates as a matrix of unit current sources, which can be connected to the output, summing the current in a switchable way. The LSB current of 62.5 nA is derived in the DAC cell itself by dividing an external reference current of 16 uA by the factor 256. At the output of the switched matrix of current sources, an NMOS mirror serves to scale the current to the desired range. If necessary, a second current mirror of PMOS type can be connected, transferring the DAC characteristic from current source to current sink.

The DAC itself must be supplied with a reference current I_{REF} or the corresponding voltage V_{REF} to bias the unit current sources. In previous designs, this is done by dumping the current through an external resistor to ground at printed circuit board (PCB) level. For the

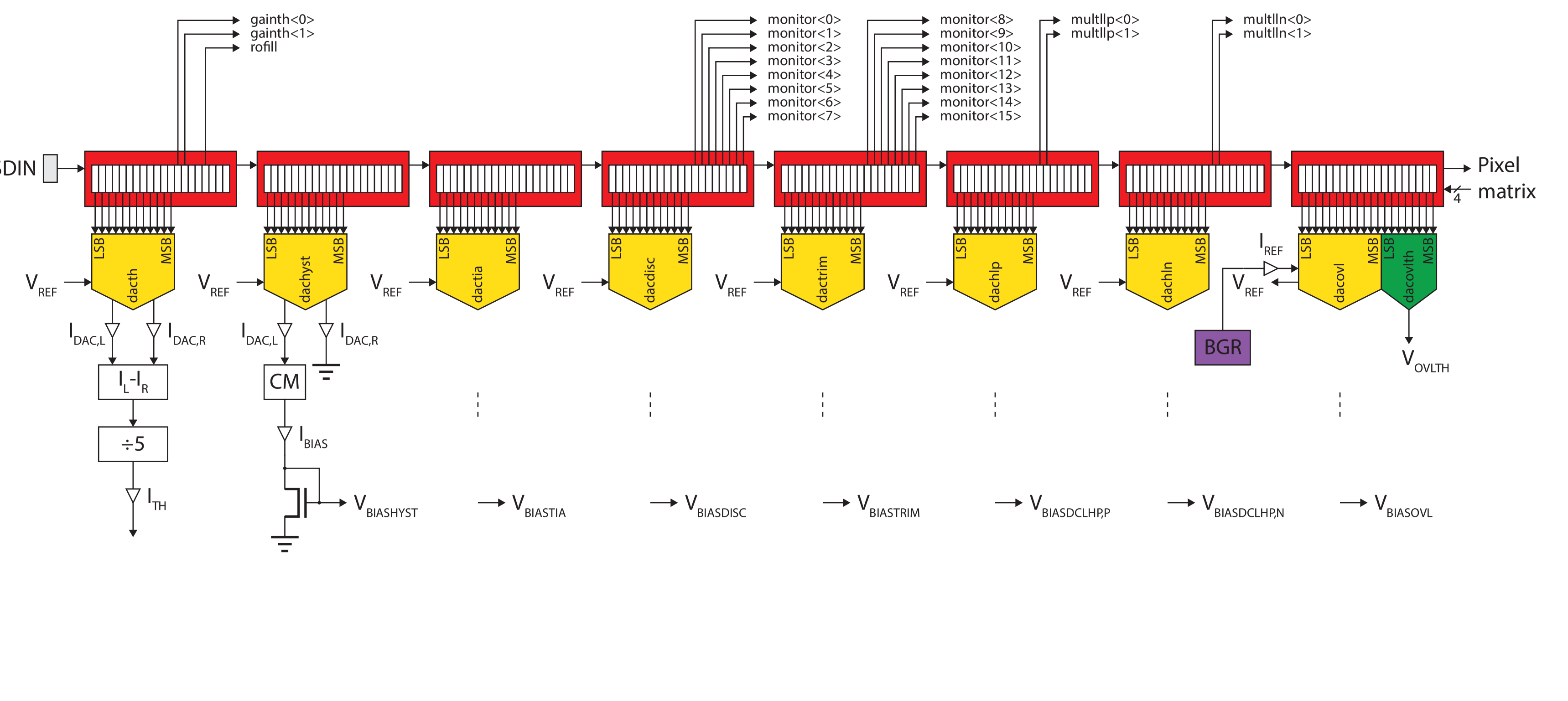


Figure 6.16: Schematic diagram of the global biasing for the APA 3.x ASIC family. The serial configuration data enters the chain of shift registers (red) from the left at the *SDIN* port. Each register holds 20 bits, while some are unconnected. Current DACs are in yellow, voltage DACs in green. The bandgap reference (purple) is connected to one DAC, where its reference current is transformed to a then further distributed reference voltage. Labelled arrows at the top of the register denote binary configuration switches. At the right of the register chain, the serial data leaves to the pixel matrix. Clock and control signals leaving the pixel matrix enter at the right.

APA 2.x and 3.x ASICs, a temperature-independent current reference is used, eliminating the need for a precise dump resistor but also any effects of a changing operating temperature. The current from the bandgap reference I_{REF} is connected to a single DAC block where it is converted to the corresponding voltage V_{REF}, which is then further distributed to all other DACs.

Each current DAC has two outputs, $I_{DAC,L}$ and $I_{DAC,R}$, defined by the following formula for the decimal setting val:

$$I_{DAC,L} = I_{LSB} \times \text{val} \tag{6.3}$$

$$I_{DAC,R} = I_{LSB} \times (4095 - \text{val}) \tag{6.4}$$

Obviously, the sum of the two currents is constant per DAC. Except for the first DAC, which is not implemented using the mentioned PCELL, the current $I_{DAC,R}$ is not used and therefore dumped to GND. Instead, the first DAC for the global threshold subtracts $I_{DAC,R}$ from $I_{DAC,L}$ and scales the resulting current to 1/5. This approach allows to switch between current source and sink mode at operating time.

A simple but safe two phase shift register is used as the slow control interface, where the binary value for the DAC is shifted in at the *SDIN* port using *SCK1* and *SCK2* as the clock signals for the ϕ_1 and ϕ_2 latches and then loaded to the DAC decoder by the *SLD* signal. For validation purposes, the value at the decoder can be loaded back to the shift register using the *SRB* signal. The decoder itself takes care to connect a multiple of the unit current sources to the output if a given bit is set in the binary code.

A two phase clocking scheme requires twice the number of clock wires, but eliminates the risk of setup and hold timing violations by using two independent controlled non-overlapping clock pulses.

Although 12 bit control words are sufficient to configure each DAC, 20 bit wide words are used to keep the size of all registers equal. Some of the additional bits are used for control purposes, others are unused (Figure 6.16).

The voltage DAC used to define V_{OVLTH} is built of a resistor string between VDD_{CMOS} and GND and is therefore independent from any reference signal. Different from all other DACs, it uses one-hot encoding.

Apart from the global biasing block, the slow control chain extends in a snake-shaped path across the pixel matrix. Each pixel also contains one 20 bit register, where 7 bits are used for a smaller current mode DAC defining the per pixel threshold trim current, the remaining bits for configuration purposes (Figure 6.17).

The various DACs are listed in Table 6.1, the binary switches in Table 6.2.

Name	Logical range Description	Electrical range
DACTH	$0_{10} - 4095_{10}$ Threshold current where the global threshold voltage is generated from.	−49.2 uA – 49.9 uA

DACHYST	$0_{10} - 4095_{10}$	0 uA – 105.2 uA
	Additional tail current for hysteresis at the discriminator.	
DACTIA	$0_{10} - 4095_{10}$	0 uA – 339.7 uA
	Bias for the input and reference TIAs.	
DACDISC	$0_{10} - 4095_{10}$	0 uA – 220.1 uA
	Bias for the discriminators and gain stages.	
DACTRIM	$0_{10} - 4095_{10}$	0 uA – 10.2 uA
	Unit current for the per pixel threshold trim.	
DACHLP	$0_{10} - 4095_{10}$	0 uA – 63.8 uA
	Bias for the *HP* DCL logic cells, PMOS load side.	
DACHLN	$0_{10} - 4095_{10}$	0 uA – 60.6 uA
	Bias for the *HP* DCL logic cells, NMOS current source side.	
DACOVL	$0_{10} - 4095_{10}$	0 uA – 100 uA
	Bias for the overload detectors.	
DACOVLTH	$10000000_2 - 00000001_2$	0.2 V – 1.6 V
	Threshold voltage for the overload detectors.	
DACTRIML	$0_{10} - 127_{10}$	$-63\times - +64\times$
	Trim current for the per pixel threshold adjustment.	

Table 6.1: DAC names, descriptions and ranges for the slow control configuration interface.

Name	Binary representation and corresponding value Description
GAINTH	00: 2 kOhm, 10: 6 kOhm, 01: 10 kOhm, 11: 14 kOhm Feedback resistance for the threshold TIA.
ROFILL	0, 1 Trailer fill value for all readout channels.
MLLP	00: 0.5 ×, 10: 1 ×, 01: 1.5 ×, 11: 2 × Multiplier for the *LP* DCL logic cell bias, PMOS load side.
MLLN	11: 0.5 ×, 01: 1 ×, 10: 1.5 ×, 00: 2 × Multiplier for the *LP* DCL logic cell bias, NMOS current source side.
ENSELFGATE	0, 1 Disable or enable pixel gating by reverse hit tree.

ENSELFVETO	0, 1 Disable or enable pixel veto (operating mode selection) by reverse hit tree.
SHIFTFILL	0, 1 Trailer fill value for the per pixel counter readout shift register.
ORMODE	0, 1 Disable or enable the bypass hit flipflop path for direct hit pulse output.
ENPIX	0, 1 Disable or enable of the digital hit processing on a per pixel level.
CROSS	0, 1 Polarity selection for the discriminator input of VIN and VTH.
GAIN	00: 2 kOhm, 10: 6 kOhm, 01: 10 kOhm, 11: 14 kOhm Feedback resistance for the pulse input TIA.
CONNECT	0000: No connection, 1000: Bump ↔ TIA, 0100: Bump ↔ Testbus, 0010: Testbus ↔ Amplifier, 0001: Testbus ↔ Resistor ↔ Amplifier Connections made by the input switch to route bump and testbus connection to the input amplifier.

Table 6.2: Switch names, descriptions and ranges for the slow control configuration interface.

6.4 Sensor-interposer-asic assembly

Solid state hybrid detectors usually deliver the best detection performance as they can be made of different base materials and manufacturing processes specially suited for sensing and regular electronics applications. Some detectors interface the sensor without an interposing layer to the ASIC, therefore one of the two parts serves in addition as the mechanical support and also as the interconnection point to the next level in the readout chain. This assembly technique is typically used when the material budget, leading to unwanted losses, aims to be minimal, for example in the inner shells of a multi-layer particle detector.

For a single-layer low energy photon detector, the more robust approach involving an additional interposer layer as mounting support and to route the electronic signals is chosen.

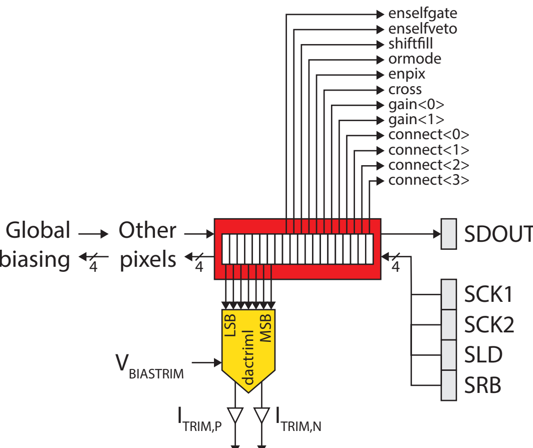


Figure 6.17: Schematic diagram of the digital pixel control for the APA 3.x ASIC.

But for the XNAP detector, the interposer is not only necessary to simplify mounting. The major drawback from using a moderate cost multiproject wafer production process for the ASIC is the limited die size, being only 1/4 of the targeted sensor area of about $1\,\mathrm{cm}^2$. It is clear that a double-side abuttable design is necessary and that a single piece sensor connects to four readout ASICs.

Out of a single wafer, various designs are cut out by dicing the silicon. Even if precision diamond blades or wires are used, this is a rather rude technique which causes mechanical stress up to visible damage. Sealing structures are required by the ASIC foundry at the periphery of the die to protect the sensitive core by enclosing it with a defined structure and an additional unused area between this ring and the actual scribe line is added.

Microscope inspection of previously built dies shows that outside of the designed region, the dimensions of the protective area varies a lot. Further, the mounting process used to attach four tiles to one single interposer requires some space in between the ASIC edges, with at least 150 um for the available equipment.

Considering the largest die boundary (Figure 6.18), the additional space for mounting and the pixel pitch of 280 um, it is clear that a fanout adapter is necessary for the arrangement of the ASIC tiles.

6.4.1 *Ceramic interposer*

For many years, interposers built of ceramic base materials are widely used. In its simplest form, ceramic substrates are used as carriers to built modules out of multiple parts, for example Silicon devices or

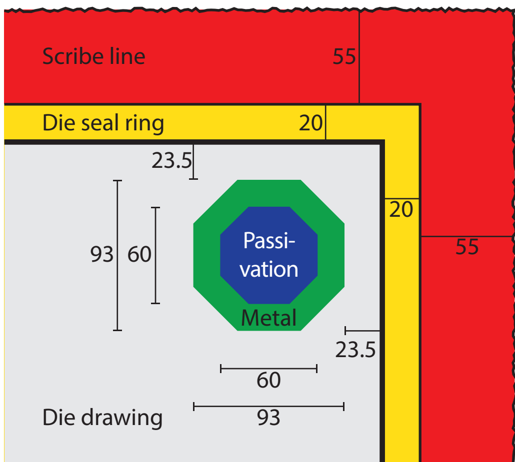


Figure 6.18: Schematic of the APA 3.x ASIC die corner with worst case border dimensions (in um). Other dies are abutted at the top and right side. The active part of the die is colored grey, with its I/O pad at the upper right position in green and blue. Foundry-added protective structures are colored yellow and red.

passive components. Another common use is to bridge the geometric gap between Silicon devices with interconnect structure sizes less than 100 um to the scale of regular PCBs, being a multitude of that. Classic thick film manufacturing techniques allow only for a single ceramic core, which is machined for the via holes and afterwards printed on both sides with conductive material. Novel fabrication techniques not only allow a multitude of stacked layers, but also to integrate passive components, resistors, capacitors and inductors, or even tiny channels for liquid coolant.

Compared to PCBs, the thermal expansion of the ceramic interposer match well to these of the Silicon sensor and ASICs, which is crucial for the mechanical and electrical stability of the interconnection. With minimum trace widths of 100 um and via diameters of 80 um, structure sizes are not as small as high-end PCB techniques provide, but can be compensated by spreading wires over a large number of layers, connected by staggered blind vias. Further, the very smooth and mechanically resistant surface is suited for connecting the interposer with various wirebond and bump bonding techniques. Even if no protective silkscreen is available with the given manufacturing technology, any risk for short-circuit is reduced by immediately routing all interconnection traces to the inner layers, therefore only the bare contact pads are exposed on both outer sides.

Shielding the ASIC from photons traversing the sensor is purely possible by the ceramic substrate. Layout restrictions prohibit an additional metal fill at the inner layers to improve absorption.

6.4.2 *HDI-PCB interposer*

Traditional PCB technology crossed the structure size limit of 100 um to very fine and precise traces with the ability of Laser direct imaging (LDI) technology, where the photolaminates are structured in direct by Laser light without an additional mask set. Trace widths and spacings of 25 um are routinely achieved. Laser drilling enables via holes of 50 um diameter and less, at the cost of thin base materials due to a limited aspect ratio between the hole diameter and the depth of the drilled hole.

Compared to the ceramic interposer, the high density interconnect (HDI)-PCB offers much finer structures while not even fully exploiting the technical abilities. As the electrical routing is much more relaxed high layer counts as for the low temperature cofired ceramic (LTCC) are not necessary. On the downside, the increased resistance by very thin traces must be taken into account. The surface quality does not differ from the ceramic in terms of planarity and solder and bond ability. The base material however, which is still an Epoxy laminate, is typically thinner and therefore more flexible, especially under heat.

6.5 FRONTEND BOARD

The frontend board, developed and manufactured by the DESY group, is a classical PCB with active electronic components but also provides the mechanical support to mount and connect the interposer assembly. It serves as the interface between the APA ASICs and the following FPGA used to communicate with the readout chips.

The interposer assembly is mounted in a hole of the frontend board. Wire bonds connect the traces on the PCB to the corresponding pads at the four sides of the interposer.

The power supply for the four ASICs is done by linear regulators, reducing one single supply voltage to the multitude of necessary supplies while also monitoring the current flow. Digital input signals to the ASICs are forwarded from the readout board without amplification. Differential lines leading to the ASICs are terminated next to the wirebond pads by discrete resistors. The digital output signals from the ASIC are fed into differential line buffers. These buffers receive the differential signal from the APA ASICs and convert the common mode level and differential swing to the low voltage differential signaling (LVDS) standards.

To monitor the thermal conditions of the board, various temperature sensors are distributed next to the interposer and the supply regulator integrated circuits (ICs), with a digital I^2C interface connected to the readout board.

The all-digital interface between the frontend and readout board uses, apart from the I^2C for monitoring purposes, differential sig-

nalling, which is routed between the board via four Z-Pack connectors at a total of 140 differential line pairs.

6.6 READOUT BOARD AND HOST COMMUNICATION

The readout board is the last part in the electronics chain before the connection to a general purpose computer is made. It consists of two main devices, a programmable logic device and an embedded processor (Figure 6.19). Not only the design of the hardware is done by the ESRF group, but also the firmware which runs the FPGA and the processor.

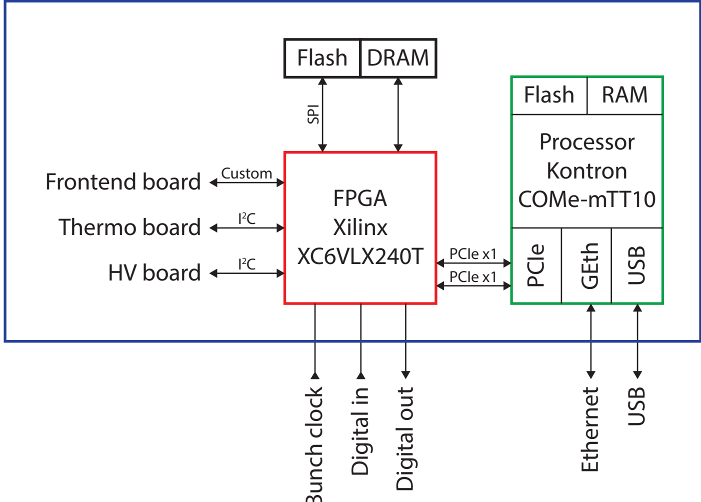


Figure 6.19: Schematic of the XNAP 1k readout board. The components and connections within the blue box are not accessible by the end user.

When a photon is recorded by the ASIC, either the hit output goes high to signal that a readout cycle is needed, or simply a particular hit counter increments, waiting to be read out at a later time. The actual readout cycle from the hit memory or the pixel counters is controlled by the readout board, which must generate the appropriate electronic signals. Being a time-critical item, this is implemented in the programmable logic at the FPGA: Triggered by a changing *HIT* line, a time to digital converter (TDC), which is previously enabled either manually or by the bunch clock input, is stopped. Then, the position information is transferred out of the ASIC by pulsing *ROLD* and *ROCK* lines. Finally, a *CLRHIT* pulse resets the hit flipflop and re-enables acquisition. The hit counter readout is manually initiated but then runs autonomous.

The serialized data from the ASIC is transferred and deserialized within the FPGA. Helper structures to synchronize to the data stream are present for each readout channel and are engaged at the system initialization.

The transferred data is temporarily stored in dynamic random access memory (DRAM) cells connected to the FPGA.

The frontend board is plugged into the readout board and electrically connects through large Z-Pack connectors, mating the differential lines used for data transfer towards and from the ASIC.

Further connections at the readout board are dedicated I^2C buses for a temperature controller board and the high voltage source.

General purpose inputs and outputs are added for later usage.

In the FPGA firmware, endpoints for the serial PCI express bus are instantiated. Two single lane buses connect the embedded processor with the FPGA.

The embedded processor is a single board computer module, including all the necessary components to run the Linux operating system, like non-volatile storage, memory, USB and networking interface. Through the gigabit network interface, all control and data transfer takes place, so that this is, together with a Universal Serial Bus (USB) port in order to upgrade the firmware code, the only accessible port by the user. A dedicated process is running on the processor, responsible for the data transfer and control communication with the FPGA. On the network side, a regular Internet protocol (IP) socket is opened at the transmission control protocol (TCP) port 5001 to which the user can connect with the command and control software through a common network to the detector.

The command protocol encapsulated in TCP/IP packets, providing reliable, ordered and error checked transport of the data, is a flat text-based command and response protocol, where the control software sends a command at a time and, if any, results are sent back to the client.

6.7 COMMAND AND CONTROL SOFTWARE

From a typical computer with Ethernet connection to the detector, it can be controlled either by a stand-alone command line based software or integrated as a pseudocounter device in the ESRF Spec beamline control.

The software is written as a set of Python classes communicating over a regular socket interface with the detector. Most of the software task is integrated to the embedded processor firmware, therefore the set of Python code mostly passes the commands and decodes the returned values for display.

6.8 MECHANICS AND COOLING

Even if the XNAP detector is a low power device and the typical power dissipated by the sensor and ASICs is only a few 1 W, the heat up must be controlled. The dark current by the APD cells in the sensor typically doubles every 10 °C, therefore excessive heat could lead to very small signal to noise ratio.

A water cooling system has been considered, but then has been rejected in favor of a portable, smaller housing including an air cooling system, built by the DESY group (Figure 6.20).

Prior to mounting the interposer assembly, a solid copper block is glued to the backside of the ASICs to build a good thermal connection. A set of metal clamps then connects a Peltier element to the cooling block which acts as a heat pump towards a large, forced air flow cooled heat sink.

The current which flows through the Peltier element and therefore the amount of transferred heat is controlled by a microcontroller-driven proportional integral derivative (PID) controller on the thermo board. The temperature used as input for the controller is measured by a dedicated sensor mounted to the outside of the cooling block. If necessary, the temperature sensors on the frontend board can be used by connecting the I²C bus of both boards.

All electronic and supporting mechanical and thermal components are mounted on a base plate slightly smaller than the area covered by an A4 sized sheet of paper and enclosed by a protective cover.

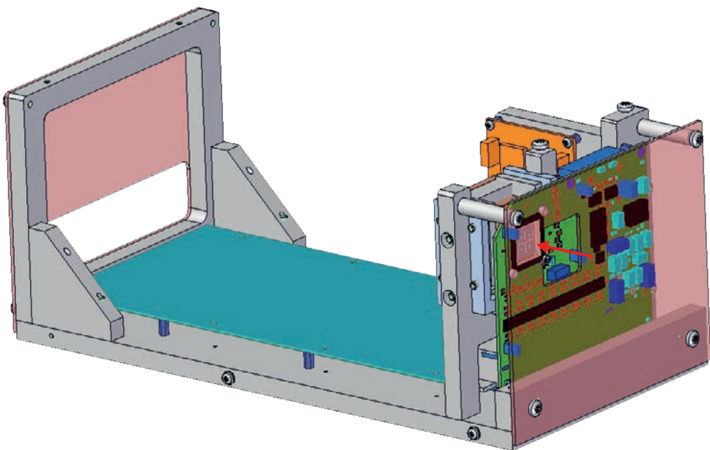


Figure 6.20: Sketch of the mounting and housing of the detector. The aluminium base and mounting structure is colored grey. The sensor is mounted in the photon beam (marked by the red arrow) passing through a window in the front plate. The sensor and ASICs, glued on a copper block, are fixed to the frontend board (green), which is plugged into the readout board (teal). The thermo board (orange) is mounted vertically, keeping the area behind the copper block for the Peltier element and its heatsink and fan (not shown). Original drawing by DESY with modified colors.

7 PROTOTYPING AND SYSTEM IMPLEMENTATION

7.1 ASIC STUDIES PRIOR TO THE PROTOTYPE

The development of the APD array and the readout electronics are parallel processes, regardless of the fact that the electronics development depends on some key parameters set by the sensor. Therefore, it is decided to use present devices, both for the sensor and the preamplifier, and to derive assumptions from the measured data. Where possible, the electronics should be designed to match multiple sensor implementations and readout schemes.

7.1.1 *APD sensor*

To start with the evaluation of APDs as X-ray detectors, Excelitas provided some samples of the C30817 [11] general purpose Silicon APD. Although the diode design is almost 25 years old, the device is still built without modification and used for photon detection within the 400 nm to 1100 nm wavelength range.

The active part of the reach through device is of circular shape with an area of 0.5 mm² and a thickness of about 110 um. The detector capacitance, including packaging and leads, is given as large as 2 pF to 4 pF. Each part is calibrated by selecting the operating voltage to a gain of 120 × for visible light.

Even with the internal avalanche amplification, the electronic signal from the APD needs to be further amplified ahead of being displayed with an oscilloscope. As an alternative approach to amplifier boards [4] based on the MAR-6+ [33] RF amplifier, the ADN2880 [1] high bandwidth TIA is used to convert the signal current to a corresponding voltage with a moderate transimpedance gain of 4400 V/A (Figure 7.1).

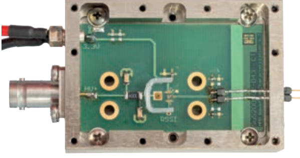


Figure 7.1: Test board with a commercial TIA and an unpackaged APD die.

The measurements with a 5.9 keV ^{55}Fe source show that a signal current of 13.6 uA can be expected by the detection of those low energy X-ray photons by the APD, as well as typical pulse widths of a few 1 ns, limited by the charge transport time inside the device itself, if the APD is connected to such a fast current receiver.

7.1.2 *Single channel test structure*

A simple structure is designed and submitted by Peter Fischer together with some other test designs on a 1.5 mm × 1.5 mm MiniASIC. The circuit includes a single resistive feedback TIA, a chain of four differential amplifiers and a simple discriminator with CMOS output. The reference voltage for the discriminator as well as all biasing currents must be generated outside of the chip, as no DAC is present. Apart from some internal nodes, almost all inputs and outputs are routed to pads at the chip boundary.

Despite for its simple design, the test structure suffers from major stability problems: As soon as the hit output changes its level, the circuit starts to oscillate and can only be reset to stability by powercycling the entire chip. Many efforts to locate a stable operating point by adjusting the biasing, the operating voltage and by adding additional capacitance at the power supply nodes were unsuccessful, therefore a redesign is decided.

7.1.3 *Four channel test structure*

As a consequence to the oscillation problems within the test structure, the circuit is analyzed regarding sensitive nodes and sources for fast transients. Potential sources of crosstalk are attributed to the CMOS type internal buffers and output drivers, coupling back to the input amplifier. As by design, the input stage must provide a small time constant in the order of 1 ns, additional capacitance can not be placed in the feedback loop to reduce the bandwidth of the amplifier.

The digital part of the test structure then is replaced with differential current mode logic, known to be an alternative to CMOS logic emitting less switching noise while being able to operate at high speed if properly biased. Within another project, such logic cells are already used for basic digital logic. The cell library is extended with a 16 bit ripple counter while keeping the basic frame and the layout arrangement intact.

The APA 1.1 test structure contains four analog channels, each built of the TIA and a chain of differential amplifiers. A tiny logic block allows to disable the analog input and inject a digital test signal. The result is connected to a demultiplexer either routing the signal to a disjunction with the other channel outputs going to the chip boundary or to another conjunction whose output is connected to the tog-

gle input of the ripple counter. The most significant bit (MSB) of the counter is routed to the chip boundary.

For reading out the counter states, it is necessary to use the digital inputs of the particular channel to inject and count the number of pulses while watching the MSB output to toggle. The number of injected pulses corresponds to the maximum counter value of $2^{16} - 1$ reduced by the number of captured hits. This simple readout mechanism is chosen to reduce the logic inside the ASIC and the number of necessary I/O pads.

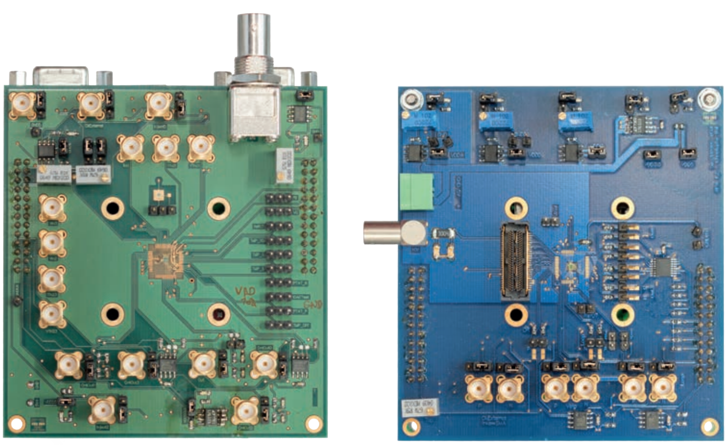


Figure 7.2: APA 1.1 (left) and APA 1.2 (right) test boards, stacked on top of the Uxibo.

The APA 1.2 test structure evolves from the previous design by substituting the first differential amplifier in the chain by a more advanced differential discriminator, containing a pair of current mirrors to inject an additional trim current in each branch of the differential pair. Also, a two-way switch in front of the TIA is added, allowing to inject a test pulse through an on-chip resistor. Further, the differential output buffers are replaced to provide larger drive strength and faster transition times.

For testing the structures, the ASIC dies are glued to a PCB and wire bonded to the board, without further packaging (Figure 7.2). While the PCB for the APA 1.1 is mostly passive, the one for the APA 1.2 contains differential transmitters and receivers as the driving FPGA board provides only single ended connections. Further, components for power supply and a connector for the analog inputs are added.

To test different APDs in conjunction with the ASICs, the connector left of the ASIC die on the APA 1.2 board (Figure 7.2, right), allows to stack different boards on top, which carry the diodes. All four analog channels as well as the supply for the APDs are routed through the connector.

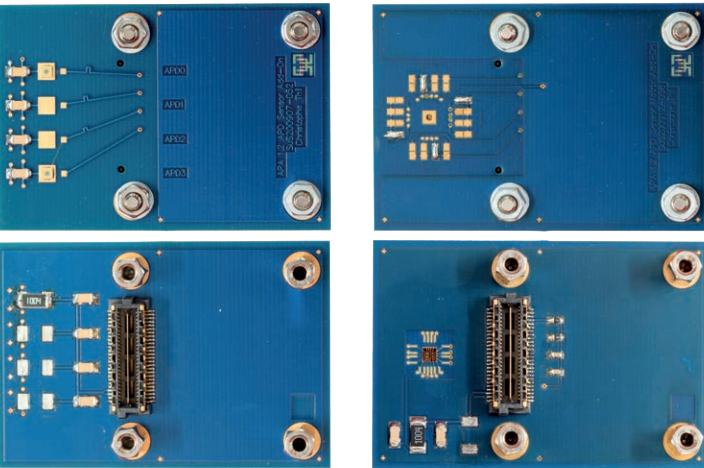


Figure 7.3: APD carriers with different diodes for the APA 1.2 and APA 2 test boards, which can be stacked on top. Enlarged to 150 % relative size for better vision.

Two different APD carriers are manufactured (Figure 7.3): One containing four discrete diodes of the same type used on the previous boards, the C30817, and another with a prototype 4×4 APD array of divided cathode type suited for wirebonding, where four of the 16 channels are connected.

7.2 PROTOTYPE SYSTEM WITH 16 PIXELS

The overall layout of the 16 pixel prototype (XNAP 4x4) is a reduced form of the final detector. As opposed to the previous APA 1.x chips, the pixels are arranged in a 4×4 array with a bump pad in the corner of each cell as the electrical connection. The power and data connections are also designed as bump pads in the section below the pixel area.

7.2.1 *16 pixel APD array*

Three types of APD arrays suited for the prototype geometry and therefore for bump bonding are developed by Excelitas, evolving from the first array concept.

The standard design for reach-through APDs is ported to a diode array, implementing a conservative and safe divided cathode configuration. Even if the exact details on the Silicon implants are not known, a relative small active area is anticipated as the charge multiplying p-n junction is entirely separated between the pixels, requiring significant area to bring the electrical field down. A batch of Silicon devices

is fabricated and then optically characterized. As the dead space between the pixels is found to be in the order of 150 um, therefore only 22 % of the pixel area being active, the design is discarded for its low sensitive area.

The second design is a dead-space optimized variant of the divided cathode arrangement, where the isolating interruptions within the p-n junction are modified. A single guard ring is placed at the bottom side, surrounding the pixel pads. Silicon devices are light scanned by Excelitas and show a smaller dead area between the pixels of 60 um, therefore 62 % of the pixels are considered active. Different variations of this design are built, where the best parameters for dead space, guard ring arrangement but also the shape of the electric field by the implants are determined by Excelitas. Wafers of 120 um and 200 um thickness are processed and kept for later usage.

The third design is an entirely different approach by segmenting the anode while keeping the multiplying p-n junction as a continuous area. There is only one guard ring at the light entry side which must be tied to the bias voltage, therefore the pixel pads are not protected from leakage currents. This divided anode arrangement is considered as an experiment for further reduction of the dead area, as by design, this sensor does not suffer from such. There is little to no experience in building such a device and it is not known if the ASIC is able to cope with the reduced inter-pixel resistivity. For this device, no special techniques to increase the inter-pixel resistivity are implemented.

7.2.2 *16 pixel readout ASIC*

The 16 pixel readout ASIC is the first chip implementing most of the design aspects of the final system, although the number of pixels and communication channels is reduced for simplicity, the analog overload detection and autonomous double-hit suppression left out.

The Silicon die, which is a 2×1 MiniASIC of $3\,\mathrm{mm} \times 1.5\,\mathrm{mm}$ size, consists of three major parts (Figure 7.4, left): The pixel matrix (purple), the biasing and DAC block (orange) and the I/O area with pads and buffer cells (green). The pixel unit cell is shown on the right: About $1/9$ of the area is blocked by the bump pad in the top right corner, which prohibits this area from any usage for active components and half of the metal stack below the contact surface for routing. Left of the pad, the amplification chain consisting of TIA, discriminator and differential amplifiers are placed. Left of that, about $1/3$ of the area is occupied by the digital logic, most by the counters and the associated shift register. The electrical routing for common signals is implemented as a mesh network without buffering of the signals. Therefore, the external device generating the control signals, the readout controller, has to drive the full internal wireload for the signal

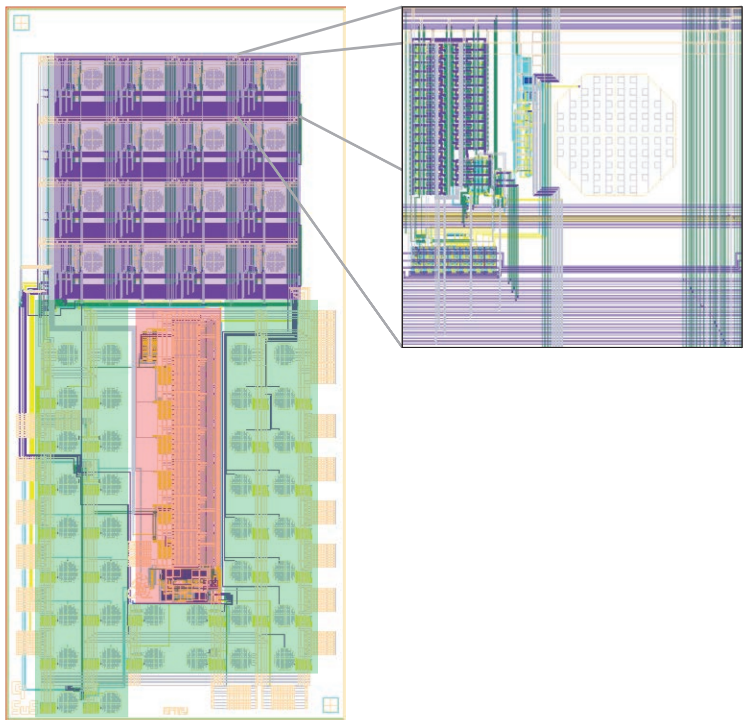


Figure 7.4: Layout overview (left) and pixel detail (right) of the APA 2.1 metal and polysilicon layers.

inputs. The output signals however are buffered with differential drivers next to the pads.

The digital logic block of the generation 2 APA ASICs is built of entirely redesigned differential gates, both at schematic and layout level. The supply voltage and the operating current is lowered as well as the transistor geometries adapted for decreased power consumption. Also, the split of high and low speed logic is implemented, effectively doubling the number of cells. At the downside, the number of biasing nets doubled, as the two cell variants require different biasing voltages.

Even for the small chip, the routing of the electronic signals and the power supplies occupy a large amount of area (Figure 7.4, right). Global routing is done on the upper four metal layers, orange, grey, purple and green, whereas the power routing is implemented on the top metal, providing the lowest sheet resistance due to a thick metallization. Local routing at pixel level is done on the lower two layers, yellow and light blue, in the digital block also on metal 3.

Two revisions of the ASIC are submitted and manufactured by Europractice. For the second version, in addition to fixing errors, a monitor bus is added to sense supply and bias voltages at different places of the die, allowing for a later voltage drop analysis.

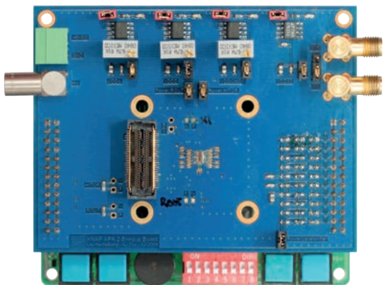


Figure 7.5: APA 2.1 ASIC, glued and wirebonded to a test board, stacked on top of the Uxibo.

Although the chip is designed to be bump bonded, first tests are performed without involving the interposer necessary for the bump bonding attachment. Instead, the ASICs, glued to a carrier PCB, are connected by traditional wirebonding (Figure 7.5).

Specific details on the operating procedures can be found in [41].

Measurements and results are published in [43].

7.2.3 *Interposer*

To exercise the double sided assembly on an interposer, necessary by the concept to tile four ASICs to one sensor, an interposer is also designed and manufactured, both by Excelitas, for the small 16 pixel prototype.

7.2.3.1 *Thick film ceramic*

As a first trial, a conventional thick film technology ceramic is fabricated (Figure 7.6, top). The base material is a single 400 um thick, 4.5 mm × 6 mm sized layer of Al_2O_3, which is machined for the via holes. The conductors are screen printed on the bottom side facing the ASIC, whereas vias in the pixel area pass the connections for the sensor and its biasing to the top side. Both traces and via filling are made of a liquid Gold conductor dye. The assembly is fired, drying the traces and building a rigid ceramic structure. No passivation layer is added on both sides, leaving the conducting traces exposed at the surface.

The interposer is a pure passive device, bridging the signal as well as bias connections of the pixel matrix between both sides of the ceramic. The signal and power pads for the ASIC are routed to the two opposed edges for easy wirebonding.

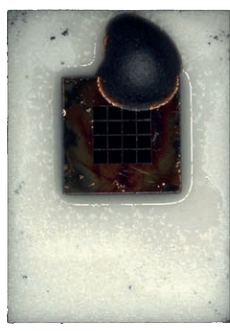
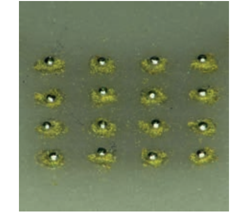
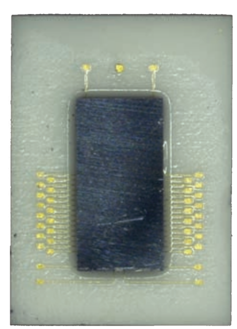
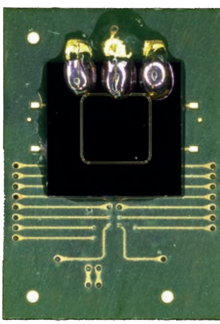
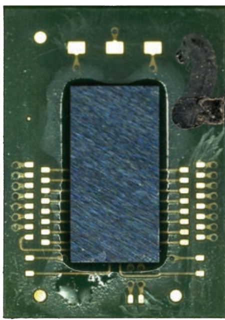






Figure 7.6: 16 pixel assemblies on both interposer types: Ceramic (top) and PCB (bottom). The top side of each assembly with mounted sensor is shown in the right column. The bump pads connecting the sensor to the ASIC are shown in the middle: Gold filled vias with applied solder bumps.

7.2.3.2 *Glass-reinforced Epoxy laminate interposer*

An alternative to the ceramic interposer is made in HDI-PCB technology (Figure 7.6, bottom). It shares the mechanical dimensions and the pad layout with the ceramic, but due to fabrication restrictions, the traces are placed both on the top and bottom sides. An additional passivation protects the traces on both sides from short circuits, only leaving the bump and wirebond pads exposed.

7.2.4 *Interposer stack assembly and test*

The initial attempt to electrically and mechanically assemble the complete stack, consisting of ASIC, interposer and sensor, was to use conductive Epoxy glue for all electric connections, and then mechanically reinforce both sensor and ASIC connections with an Epoxy underfill with capillary flow.

The envisaged conductive Epoxy glue is a two component mixture where the electrical conductance is achieved by dispersion of very small silver or Gold particles. After the curing procedure, an elec-

tric connection and mechanical attachment is made, without applying any force necessary for traditional stud bumping or excessive heat, required for reflow soldering with conventional melting metal. Therefore, Epoxy glueing is suited for the attachment of delicate parts sensitive to mechanical and thermal stress.

Solely glueing turned out not to be possible, both for ASIC and sensor attachment: On the top metallization of the ASIC pads made of Aluminium, an oxide layer builds up which is not steeped by the Epoxy. So even if the mechanical attachment is solid, any electric connection fails. The sensor however, metallized with Gold, does not suffer from isolating oxide build-up, but a mechanical spacer is necessary to avoid short circuits as the Epoxy is smeared between the connections.

Different attempts to solve the interconnection problems finally lead to an entirely different approach of mounting the assembly involving reflow soldering and to reject the ceramic interposer in favor of the HDI-PCB, as the via filling did not withstand the reflow process (Figure 7.7).

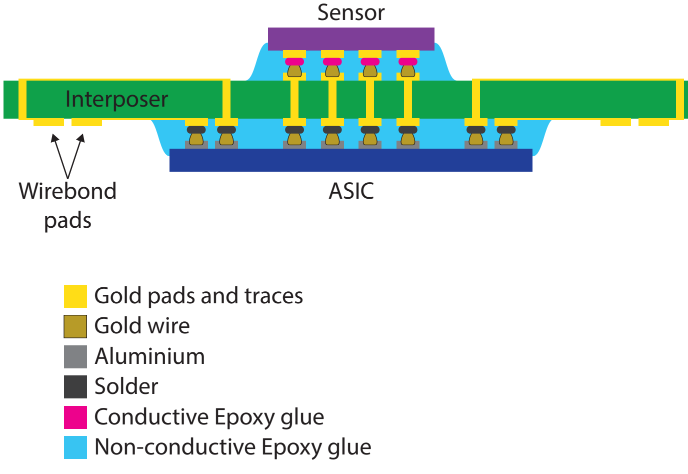


Figure 7.7: Final 16 pixel assembly cross section and procedure.

Finally, successful mounting is achieved in a combined process involving mounting techniques done in parts on our own, all steps up to the sensor mounting, and other parts by Excelitas.

1. The surfaces of the HDI-PCB interposer and the ASIC are cleaned in an ultrasonic bath and activated by plasma cleaning.

2. On the top side sensor connections, Gold studs are placed with a Gold wire bonding machine. If their height varies significantly, they are coined to a common level.

3. The ASIC die is also populated with Gold studs for all bumping pads. If necessary, they are also coined to a common height.

4. At the bottom side of the interposer, solder balls are applied by jetting the liquified SAC 305 solder to the Gold pads.

5. The interposer is mounted with the bottom side facing the head in the flipchip machine without applying mechanical force to the Gold studs on the other side.

6. The ASIC is flipped to the interposer and reflowed at 220 °C.

7. A capillary underfill is dispensed around the ASIC, fixing the die to the interposer.

8. On the sensor die, dots of conductive Epoxy are dispensed.

9. The sensor is flipped to the Gold studs on the interposer and then cured.

10. A capillary underfill is also dispensed next to the sensor.

During the development of the assembly process, mechanical and electronic tests of the samples are necessary, allowing to tune the parameters like the amount of solder applied to the interposer or the force and temperature for the flipping procedure. Electronic testing prior to full integration of the assembly to a readout board, which involves glueing and wirebonding it to the PCB, is possible using a probe station: The electric connection is made by touching the bond pads with probe needles, which can be positioned using micrometer screws.

The usage of individual probes is possible if the number of connections is only a few, but for multiple tens of connections a custom needle ring is necessary (Figure 7.9, right). The needle ring is manufactured by htt GmbH based to the specification of the needle tip positions. The ring itself is a standardized PCB with a diameter of about 6 cm, with metal pins to be inserted in the probe card. The needles are fixed by glueing into a smaller Epoxy ring with the lever extending to the inner. Bent tips of 38 um thickness made of a Beryllium Copper alloy finally establish the electric connection to the bond pads on the interposer.

The probe card PCB, mounted via a metal frame to the probe station, not only serves as mechanical support for the needle ring, but also contains the full frontend board with various power supply and signal amplification ICs (Figure 7.9, left). Digital signals from and towards the readout board, mounted outside the probe station, are passed by cable.

Even if theoretically possible, tests involving the sensor were not made within the probe station. This would either have involved a

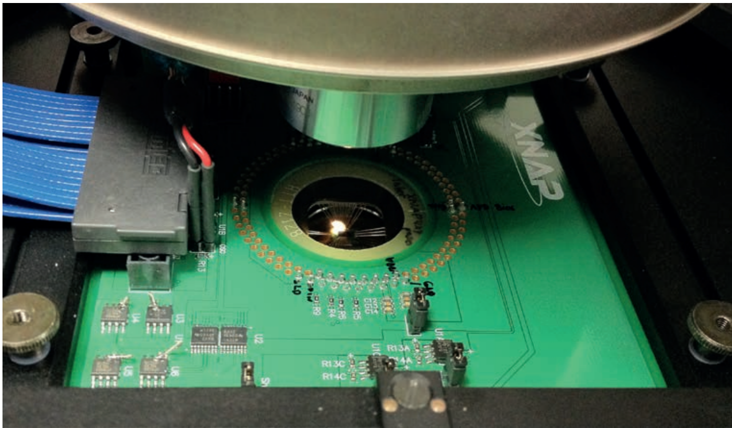


Figure 7.8: Detail view of the probe station test. A microscope (top) illuminates the sample and allows to position the needles with micrometer precision, which are mounted to the probe card. The sample (illuminated dot) is fixed on a vacuum table which can be electrically moved on three axis.

special support to place a photon source between the vacuum table and the sensor as it faces down or a high energy X-ray source, emitting through the whole stack (Figure 7.8).

An automated test routine is run to check the slow control interface with the DACs and configuration switches, pixel and readout shift register, hit signalling and position encoding as well as all fast control signals, *VETO*, *GATE* and *INJ*: A single pixel is enabled at a time and the digital injection pulsed. If the detector is disabled by the *GATE* signal, no hit must be recorded, neither by the hit memory for list mode readout nor by the respective counter for counting mode. If

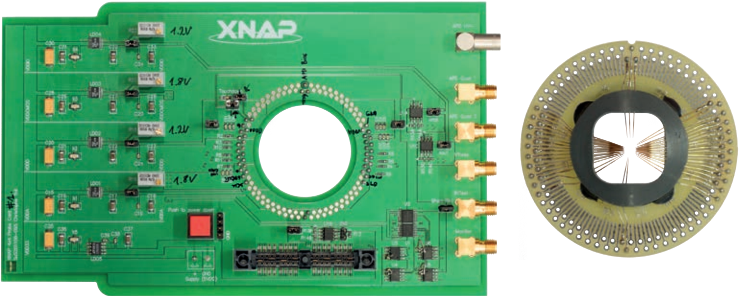


Figure 7.9: Probe card to test the APA 2.1 interposer assembly prior to sensor mounting.

the hit path is enabled, it is verified that by the *VETO* signal, each hit is either routed to the hit memory or the counter. If the correct pixel position is found in the hit memory and the respective counter did increase by the number of injected pulses, the pixel is considered operational. During these tests, it is verified that disabled pixels do not trigger, for example by cross talk, as all hit memory positions and all counters are read out during every test cycle and checked for their unchanged state. For such a single erroneous trigger, the respective pixel is marked as defective and masked out.

Parallel to these systematic tests of all assemblies, some failing the electronic test are analyzed by microfocus X-ray inspection not only to determine that they fail, but also why.

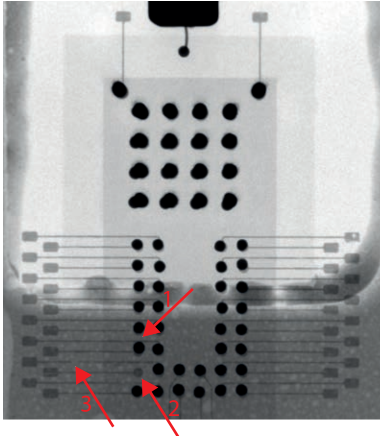


Figure 7.10: Transmission X-ray image of fully assembled interposer glued to a frontend board. The arrows highlight three defects: Shorted connection by displaced bump (1), missing bump ball (2) and broken trace (3).

The radiographies, carried out by an external company, revealed that for some of the early assemblies traces on the interposer are broken or Gold studs missing, leading to open connections (Figure 7.10). Also, bad trace quality or displaced bumps lead to shorted connections.

7.2.5 *Frontend and readout boards and associated control software*

In addition to the frontend and readout boards designated for the general usage during beam time designed by DESY and ESRF, a second set of these two PCBs are produced focusing on commissioning and electronic testing of the ASIC.

7.2.5.1 *Test system for bringup*

The readout system serves as bridge between the ASIC and a host computer running the control software which takes the user input and returns captured data from the chip. As a modular system, it is designed to be replaced or extended in parts, while being able to reuse components readily available.

As such, the frontend board is designed as an add-on PCB to a general purpose FPGA board named Uxibo, which was developed at the chair, but independent from this project by another student and already used for other tasks (Figure 7.11). The firmware which implements the specific functionality in the general purpose hardware is in contrary part of this project, likewise the software running on the host computer.

On the frontend board, four adjustable linear regulators provide the necessary supplies to the analog, digital and CMOS domain of the ASIC as well as the supply for the on-chip fast differential output buffers. As the current is comparatively small, linear regulators are chosen in favor of switching regulators, as the risk for oscillation and noise due to switching ripple of the supply is avoided. As with the present FPGA board, no differential ports are provided, two separate outputs are used for one differential ASIC input, scaled and shifted from 1.8 V CMOS levels to the absolute voltage range of the differential signal by a passive resistor network. The output however is received by a differential line buffer and converted to a conventional single-ended CMOS signal routed to an input of the FPGA.

The ASIC is mounted to the PCB by glueing the die to the Gold surface of the board and wirebonding in direct the bump pads to the PCB.

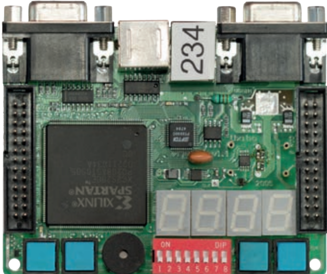


Figure 7.11: Uxibo general purpose FPGA board developed at the chair.

The FPGA board serving as readout controller mainly consists of a Xilinx Spartan 3E FPGA with its 48 MHz clock generator and an external USB controller IC, connected by a bidirectional interface.

Implemented in Verilog, the firmware transfers all the data out of the USB chip to the FPGA, where it is buffered and decoded. Logic blocks implement the controllers for the serial slow control interface, as well as for position and counter readout.

As the FPGA hardware itself is running at clock frequencies as low as 48 MHz and the resources provided by the somewhat outdated FPGA are simple, the readout runs at a much lower clock frequency than designed, but sufficient for the bring-up. Also, the generation of differential signals by two output pins which are sourcing opposite voltage levels, controlled by the firmware, does not allow accurate timing.

Given these limitations, a new general purpose FPGA board, the Susibo, with up-to-date components is developed at the chair and implemented by a student outside this project (Figure 7.12).

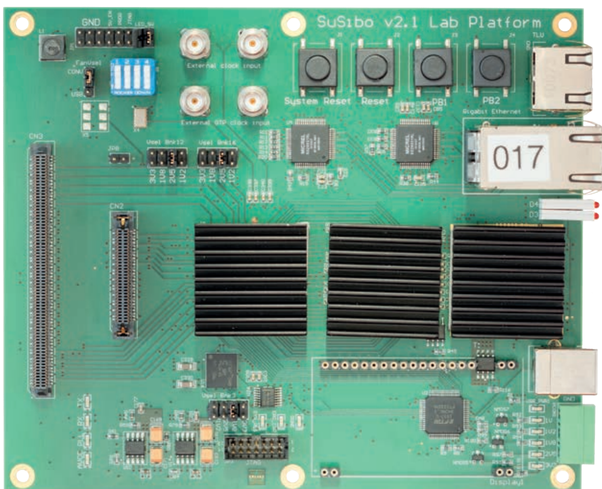


Figure 7.12: Susibo general purpose FPGA board, developed at the chair to replace the outdated Uxibo. The three heat sinks in black cover the FPGA, external SRAM and voltage regulators. The large and small extension connectors are on the left.

Upon the availability of the Susibo hardware, the firmware code is ported to the new programmable logic hardware and an adapter board is built to interface the existing frontend boards. To take full advantage of the newer hardware, the firmware had to be rewritten, which is abandoned in favor of using the readout board designed and built in the meantime by ESRF.

The frontend board designated for probe station tests, the probe card, does not connect to neither of the two boards, but to the readout board developed at ESRF. It is therefore not limited by the hardware and logic resources of the Uxibo.

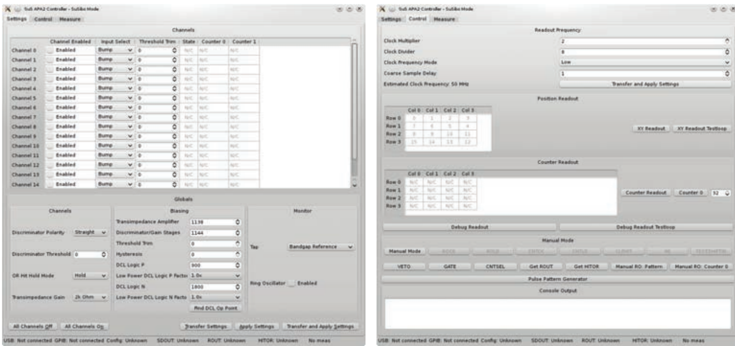


Figure 7.13: Software running on the host computer connected to the Uxibo/Susibo to control the APA 2 ASIC. On the left, the settings screen to configure the ASIC is shown, while the screen on the right shows different readout mode selections and results.

Running on the host computer which is connected to the readout board loaded with the respective firmware, the ASIC is controlled by a graphical application (Figure 7.13). The C++ application uses the libftdi library [19] to communicate over the USB bus with the controller, which is polled for new data in a loop. Events generated within the graphical interface, but also received data packets are dispatched by an event processor using Qt signals and slots. Apart from steering the readout board, laboratory instruments like multimeters and source-measure-meters can be controlled by the application through connection via a general purpose interface bus (GPIB) adapter, which allows automated measurements, for example threshold scans, where the injected current is generated by sweeping a supply.

For some test scenarios, the event driven control software is not suited, as the program flow is independent from the operating state of the FPGA firmware and therefore no way of waiting for completion of a requested action is possible. A scriptable, sequential control software running in text mode is considered, but the implementation postponed, as the control software for the ESRF readout could be used for these tests.

During the development and test of the 16 pixel prototype, different combinations of frontend and readout boards and also control software were used, depending on the availability in time and the implemented functions. These combinations and pictures of the components are listed in Table 7.1.

7.2.5.2 *Readout system for beam measurements*

The frontend board which is used for beam measurements is developed with the focus on running the photon detector as a system, and

Frontend board	Readout board	Software
Bringup FEB	Uxibo	APA2GUI
Figure 7.5	Figure 7.11	Figure 7.13
DESY FEB	Susibo	APA2GUI
Figure 7.14	Figure 7.12	Figure 7.13
DESY FEB	ESRF NIMA	NIMA CLI
Figure 7.14	Figure 7.15	
APA Probecard	ESRF NIMA	NIMA CLI
Figure 7.9	Figure 7.15	

Table 7.1: Different implementations of the readout system for the 16 pixel prototype.

not like the bringup board, to test the ASIC and find good parameter sets (Figure 7.14). Further, it respects safety rules for the sensor high voltage supply bias, like trace distance and component dimensions. The board, developed and manufactured by DESY, connects via an all-differential electric interface by a shielded ribbon cable to the NIMA readout board, designed and built by ESRF, but also by a bridge PCB to the Susibo readout board.

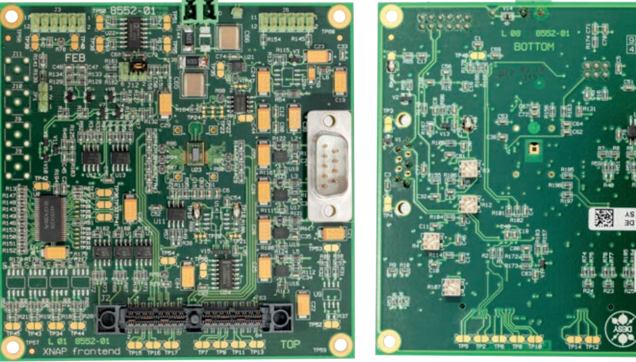


Figure 7.14: Frontend boards made by DESY. Left, the top side where the interposer is glued to. On the right, the bottom side is shown with the sensor in its mounting hole.

Like the bringup frontend board, it includes linear regulators for the various power supplies, which allows to be powered by a single main adapter. Differential signals from the FPGA, which are connected to regular single-ended CMOS inputs at the ASIC are converted, which also applies to the reverse direction. Differential inputs at the ASIC are driven by the FPGA without amplification. Contrary, differential out-

puts from the ASIC, like *HIT* or *ROUT*, are terminated at the readout board and buffered to the common LVDS standard before being sent to the readout board. A temperature sensor on the frontend board is connected by an I^2C bus also routed to the readout board. Unique to this board, it is equipped with a DAC to generate the guard ring voltage for the APD matrix.

The board is stacked up of eight conducting layers with an outer Gold metallization. In the center area, the interposer is mounted by glueing it to the board, with the sensor facing through a hole to the bottom side. Electrically, the interposer is connected by regular wirebonds, also for the high voltage bias to the sensor.

The power supply is connected to the board via a D-SUB connector. The data connection to the readout board is done with a Samtec differential connector. As a big advantage, not only PCB-mounted pieces of this connector are available, but also flexible cables built of shielded differential conductors with matched length. These cables are used in lengths of about 50 cm to interconnect the boards.

Implemented by ESRF, the readout board for the 16 pixel system reuses an existing hardware built for another photon detector (Figure 7.15). Therefore, some of the connectors are unused and masked by tape.

Figure 7.15: NIMA readout board, built by ESRF. The chassis holds the PCB with processor and FPGA, and also a main transformer.

On the PCB, a Xilinx Virtex 5 FPGA is used in conjunction with a Ka-Ro Triton embedded processor module. Apart from the ARM

processor, the module contains its proper RAM, nonvolatile memory and an Ethernet network interface.

Timing critical signal patterns are generated by state machines in the FPGA, also the hit timestamping with a TDC [15] and readout data reordering. The firmware, written in VHSIC hardware description language (VHDL), is provided by the ESRF. From the FPGA, the data is transferred via a 32 bit parallel bus to the processor. It runs the Linux operating system with a custom built kernel module taking care of the FPGA data transfer, but also the transfer process of the firmware image to the FPGA.

All other signal patterns are generated by a software program running on the processor, which also transfers the data by the kernel module to the user layer. The software opens within the Linux IP stack a TCP port, which is the interface to the host computer by a plaintext based control protocol.

On the host computer, the user can interact with the detector either by a dedicated control program written in Python which presents a keyword based shell to the user, or by integration of the detector to the ESRF beamline control software.

The Python control program consists of several classes providing easy access to the hardware. It is also used for the scoreboard based automated testing of interposer assemblies with the probe card.

7.3 SYSTEM WITH 1024 PIXEL

The kilopixel system (XNAP 1k) comprises the experience of the building process for the 16 pixel prototype and also various results from laboratory and beamline tests. All components, the sensor, interposer, ASIC, PCBs and the whole data acquisition system are rebuilt to fit a detector with 64 times the amount of pixels than the previous one.

7.3.1 *256 and 1024 pixel APD array*

The third sensor type built for the small prototype detector, the divided anode arrangement, is implemented for the final detector. Previously seen as an aggressive sensor design and thus considered mainly as an experiment, this concept outperformed both other designs during the tests.

The sensor is made in two sizes which are electrically identical. The smaller one, designated for mounting with a single ASIC of 256 pixels, is intended for optimizing the assembly process where many assemblies need to be built, and therefore to have more of them from a single sensor wafer.

Although no exact details are given by Excelitas, the active sensor implants are thought to be the same as for the prototype sensor. The main differences concern the placement of guard rings and the met-

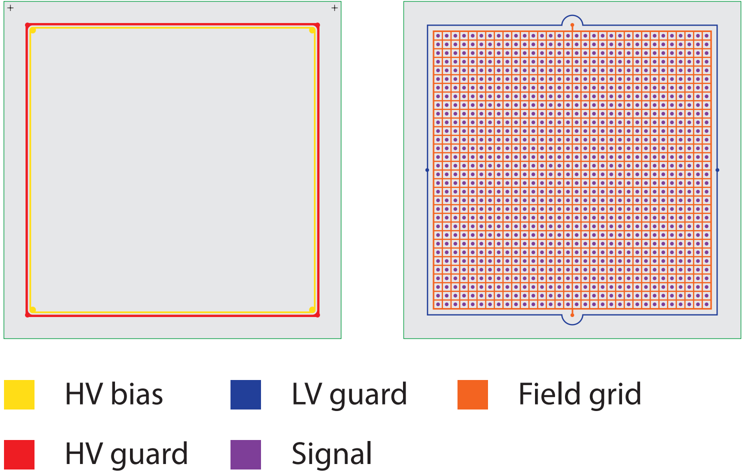


Figure 7.16: XNAP 1k sensor metallization. Photon entry/top side (left) and readout/bottom side (right).

allization (Figure 7.16): The mistake of placing a single guard ring at the top side is solved by including a second one at the bottom side. Both guard rings are routed to different pads allowing for different bias. The second change is the addition of a metal grid at the bottom side, visually dividing the area into small pixel rectangles. The metallization has no electrical connection to the substrate, it is applied to the surface only. By connecting a positive voltage, an electrostatic field builds up which deflects positive charges to the centers of the pixel, where they are collected by the electrode.

At the top side where the photons enter the device, two Gold rings are present (Figure 7.16). The inner (yellow) is used to bias the sensor with positive high voltage, the outer (red) is connected to the same potential. Independent monitoring of the bulk and surface leakage current is possible by connecting the two rings via separate amperemeters to the high voltage source. On the bottom side, the outer ring (blue) is also a guard ring, but this time for protecting the signal pads (violet) from surface leakage. It is connected to the same potential as the pixel. The field grid (orange) has no ohmic connection to the sensor bulk. It is connected to positive voltage, whereas the exact potential needs to be evaluated. Last, the violet bump pads carry the signal current which is fed into the TIA preamplifiers of the ASIC.

7.3.2 *256 pixel readout ASIC*

The third major revision of the APA readout ASIC implements the pixel arrangement planned for the kilopixel detector. Each APA 3 ASIC contains four readout channels in an interleaved arrangement, therefore

four times all wiring and interconnection structures required to read-out out four times 64 pixels.

Like the previous chips, the ASIC is fabricated by Europractice, but as a much larger 5 mm × 5 mm Silicon die. Up to today, three revisions of the device are manufactured in four runs: For the first one, called APA 3, the hit combining structure is simplified by removing the binary tree found in previous devices to relax the complex routing.

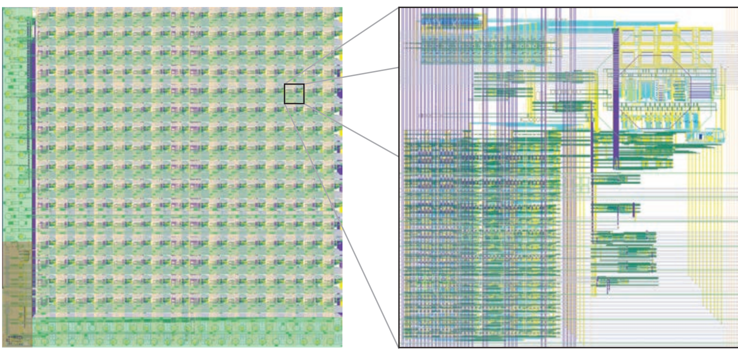


Figure 7.17: Layout overview (left) and pixel detail (right) of the APA 3.2 metal and polysilicon layers.

Beginning with the APA 3.1 revision, the ASIC foundry offered to apply solder bumps at their factory, which introduced two important changes: First, a ninth metal layer is added on top of the regular eight layer metal stack. This extra layer, providing only coarse design abilities, is mainly designated to re-route wirebond pads from the periphery to the pads spread all over the Silicon area. As this is already the case with the prior design, it is used to intensify the power grid by adding parallel bus bars. The second and more important change is related to the bumps itself. Previously, they have been added as Gold studs, involving mechanical stress for the ASIC by the applied force. As the solder bumps are applied to the clean, oxidation free surface without mechanical stress, the large dead area below the pixel bump pads is usable again at the lower metal layers and also for active parts, liberating large channels now usable for the electrical routing (Figure 7.17, right).

By these two major changes, the schematics and the layout are reworked and the binary tree for hit combining is reintroduced. Also, the pure passive distribution of fast signals is modified in a buffered tree for equal propagation delays and buffered chains running in reverse direction for the shift registers.

The L-shaped area highlighted in green contains the pads for data I/O and power supply (Figure 7.17, left). The DAC block, even larger

by one unit, now occupies a negligible area compared to the relations found at the APA 2.x ASICs.

The overall pixel layout resembles the one implemented in the APA 2.x ASICs: The pixel input pad is in the top-right corner, which is also occupied by the analog frontend. The left half of the pixel is filled with the differential logic cells, thus holds the counters and hit memory. The lower right corner contains the logic cells and line drivers for the OR tree and the reverse hit distribution tree. Depending of the position, the amount of cells and wires is different between the pixels.

At the transistor level, the APA 3.2 ASIC is made of about 413000 PMOS and 844000 NMOS gates in a highly hierarchical design. Although some space is left in the pixel area, almost all metal layers are entirely filled with wires for the interconnect.

Details on the operating procedure, like signal names and timing, are documented in [42].

7.3.3 *Interposer*

For the kilopixel detector, the interposer is an essential part to solve the geometric discrepancy between homogeneous layout of the sensor and the larger pixel gaps between the edges of the four readout chips. Like for the prototype, a multitude of interposer manufacturing techniques are studied and suppliers inquired, while Excelitas, in charge for the development and manufacturing of the pieces, decided in favor of the HDI-PCB technique, but for a different supplier they used for the prototype.

7.3.3.1 *Low temperature cofired ceramic (LTCC)*

As an alternative to the HDI-PCB interposer designed by Excelitas, an electrically compatible ceramic interposer is developed, which is manufactured by KOA Europe GmbH in an LTCC process (Figure 7.18, left) [25].

The design consists of nine layers, which are flexible sheets of a mixture of Al_2O_3, SiO_2 and a binding agent. Each sheet is mechanically punched with its proper via pattern and then the metallization, Ag covered with Ni and Au, also filling the via holes, is printed. The stacked sheets then are fired together to form a rigid substrate with a final thickness of 1.125 mm.

A simplified layout is shown in Figure 7.19, consisting of the top metallization facing the sensor as red outlines and the bottom metallization facing the ASICs as blue outlines. The outer dimensions for the interposer, the sensor and the four ASICs are outlined in black. Each ASIC, from A to C, has its proper 16×16 matrix of interconnect pads to the sensor and the associated wirebond pads for I/O and the three supply voltages as well as GND at the periphery.

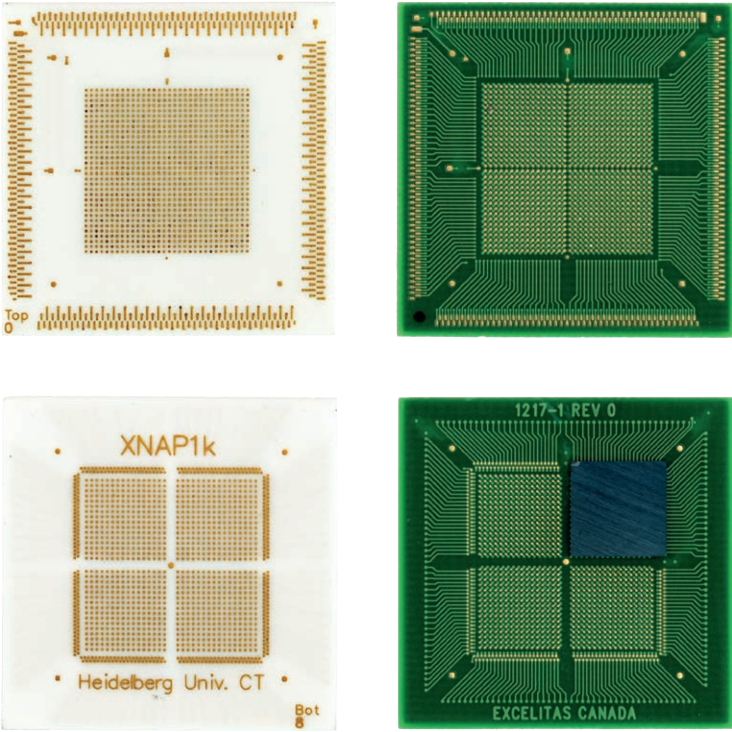


Figure 7.18: XNAP 1k interposers: LTCC (left) and HDI-PCB variant. The top/sensor sides are in the upper, the bottom/ASIC sides in the lower row.

By shifting the four ASICs slightly off towards the outer edges of the interposer, the gaps between the ASICs are added to allow for mounting. As the connection pattern on the sensor side shows an equal spacing between all connection pads, the shifting of the pads at the ASIC side is done with the stacked vias inside the ceramic core, seven times by 30 um, resulting in a horizontal and vertical gap of 420 um.

7.3.3.2 *Glass-reinforced Epoxy laminate interposer*

The design by Excelitas consists of only four layers, taking benefit from the advanced manufacturing techniques for HDI-PCBs (Figure 7.18, right). The general layout of the wirebond pads at the periphery and the sensor and ASIC connection pattern is equal with the ceramic, whereas the gaps between the ASICs are larger with a horizontal and vertical shift of 560 um each.

As a downside of the manufacturing technique, it requires thinner substrate material, giving a total thickness of only 560 um for the PCB interposer. To compensate the lighter shielding by the thinner bulk

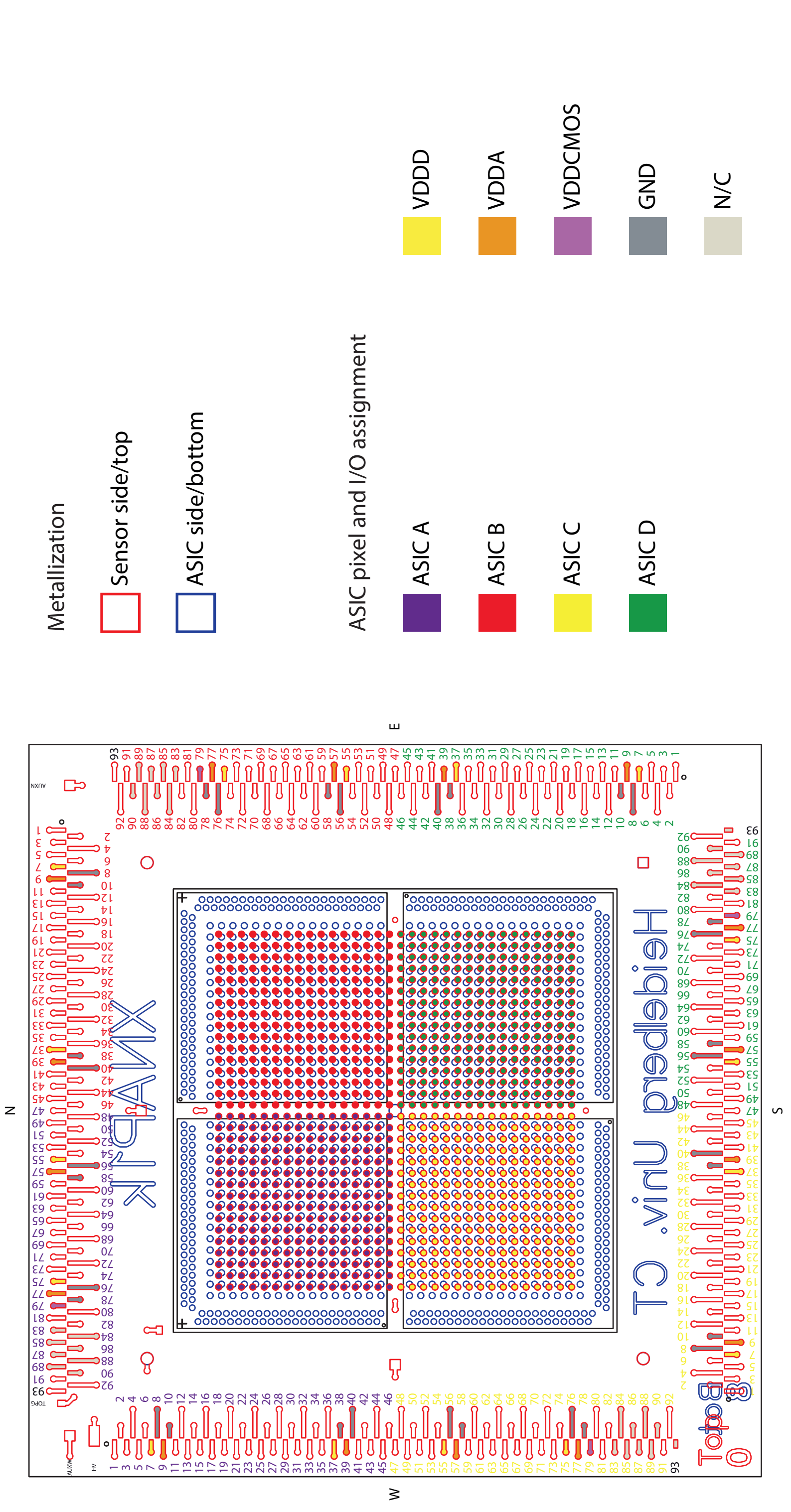


Figure 7.19: Annotated layout of the LTCC interposer. The internal vias and metal traces are hidden, the top metal is outlined red and the bottom metal blue.

material, the two internal panels are drawn as solid metal planes only exempt by the via areas.

7.3.4 *Interposer stack assembly and test*

The assembly procedure for bumpless ASICs on both types of interposers is equal to the mounting of the smaller prototypes.

For the APA 3.1 and later ASICs however, the assembly has to be modified: The application of Gold studs and solder bump jetting is not necessary anymore, as the dies are supplied pre-bumped. The alloy is of the same lead-free SAC 305 type as previously applied on our own, consisting of 96.5 % Tin, 3 % Silver and 0.5 % Copper, suitable for soldering to Gold surfaces. Compared to the self-jetted balls, the solder volume is significantly smaller, but as the passivation opening diameter is adjusted from 100 um to 60 um, additional solder or even Gold studs, serving as spacers, are not necessary (Figure 7.20).

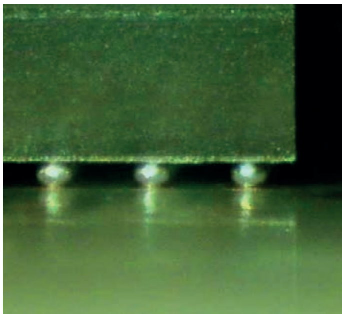
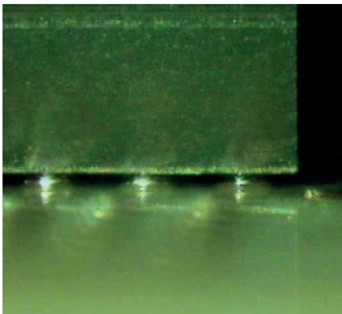



Figure 7.20: APA 3.2 ASIC with factory solder bumps placed on the HDI-PCB interposer, prior to (left) and after (right) the reflow. The ASIC die is in the upper half of the picture, the interposer is at the bottom, as seen from the side.

The XNAP 1k assembly process is as following, with the last five steps for mounting the sensor done by Excelitas:

1. The surfaces of the interposer and the ASIC are cleaned in an ultrasonic bath and activated by plasma cleaning.
2. On the top side sensor connections, Gold studs are placed with a Gold wire bonding machine. If their height varies significantly, they are coined to a common level.
3. The interposer is mounted with the bottom side facing the head in the flipchip machine without applying mechanical force to the Gold studs on the other side.

4. One or multiple ASICs are placed on the interposer and reflowed in a single cycle at 220 °C.

5. A capillary underfill is dispensed around the ASICs, fixing the dies to the interposer.

6. On the sensor die, dots of conductive Epoxy are dispensed.

7. The sensor is flipped to the Gold studs on the interposer and then cured.

8. A capillary underfill is also dispensed next to the sensor.

9. Bias and guard structures on the sensor topside are wirebonded to the interposer.

10. The bias bonds are sealed with Epoxy glue.

Extensive connectivity tests like those with the smaller prototype using a probe card are not considered. Instead, a much simpler but time consuming approach to validate the basic electrical connection between the interposer and the ASIC is done with a few flying probes in the probe station (Figure 7.21).

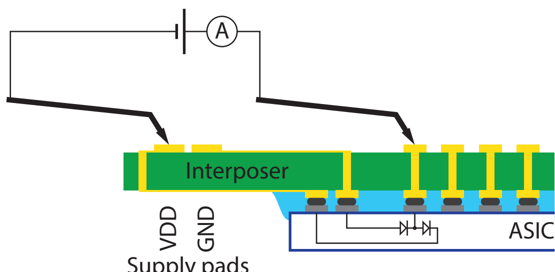


Figure 7.21: Probing the APA 3.2 for connectivity after being soldered to the interposer. A current flows through the forward biased protection diodes (schematically drawn inside the blue ASIC rectangle) to the corresponding supply pad. Both pads are connected by flying probe needles (thick black).

First, the resistance is measured between each of the power supply pads for the same net. As there is only one pad for for VDD_{CMOS}, this step is omitted there.

Then, the presence of a current flow from a signal pad through the protection diode in forward direction to the power supply is checked by carefully applying an external voltage, limited to a current of a few 1 uA. As each of the 322 signal pads is protected by these diodes, to ground and the corresponding positive supply, the solder connection can be verified.

7.3.5 *Frontend and readout boards and associated control software*

The same strategy of creating two independent readout systems like for the small prototype is chosen. The test system which can be tuned by many parameters targets at the bringup and basic operation for an experienced user, while the beam measurement system can easily be used by a broader audience.

Even if the development is fully redundant in the end, the test system is important to speed up the whole bringup process.

Up to today, the second readout system is only available in parts and still under development.

7.3.5.1 *Test system for bringup*

The test system for bringup is built of four modules stacked together via a number of connectors, extending the module concept from the small prototype even further (Figure 7.22).

As the base, the Susibo general purpose FPGA board is used. It provides two connectors for expansion: A large one at the edge of the board, serving as the primary plug-in point for extension boards. It has 150 pins of which 80 are designated to be used in pairs for differential transmission, with equal wire lengths and adjacent connection at the FPGA. The smaller connector holds the 12 pins which did not match the limited number of contacts at the large one. It is designated for slower, non-differential signals, as no care has been taken at the routing and placement.

FRONTEND BOARD The frontend board is a custom PCB connected to the Susibo via the large extension connector. A single power supply input of at least 4 V is regulated to the four ASIC supplies by linear regulators. The LT3022 regulator provides a current up to 1 A and a voltage which can be adjusted using per supply potentiometers between 0.9 V and the input voltage. Two auxiliary regulators for 2.5 V and 3.3 V supply other components on the PCB. All regulators are shut down until enabled by the FPGA, allowing also to powercycle the entire add-on board. The differential outputs from the ASIC are buffered to the common LVDS levels by a number of nine SN65LVDS100 receivers, chosen by their 220 ps rise/fall time and low jitter and skew. Differential input signals to the ASIC are passed without being repeated. A couple of voltage analog to digital converter (ADC) and DAC with bridgeable series resistor can be used to measure and apply a voltage or current to a net, selected by a jumper wire.

CARRIER BOARD On the top of the frontend board, another extension connector forms the counterpart where the carrier board is

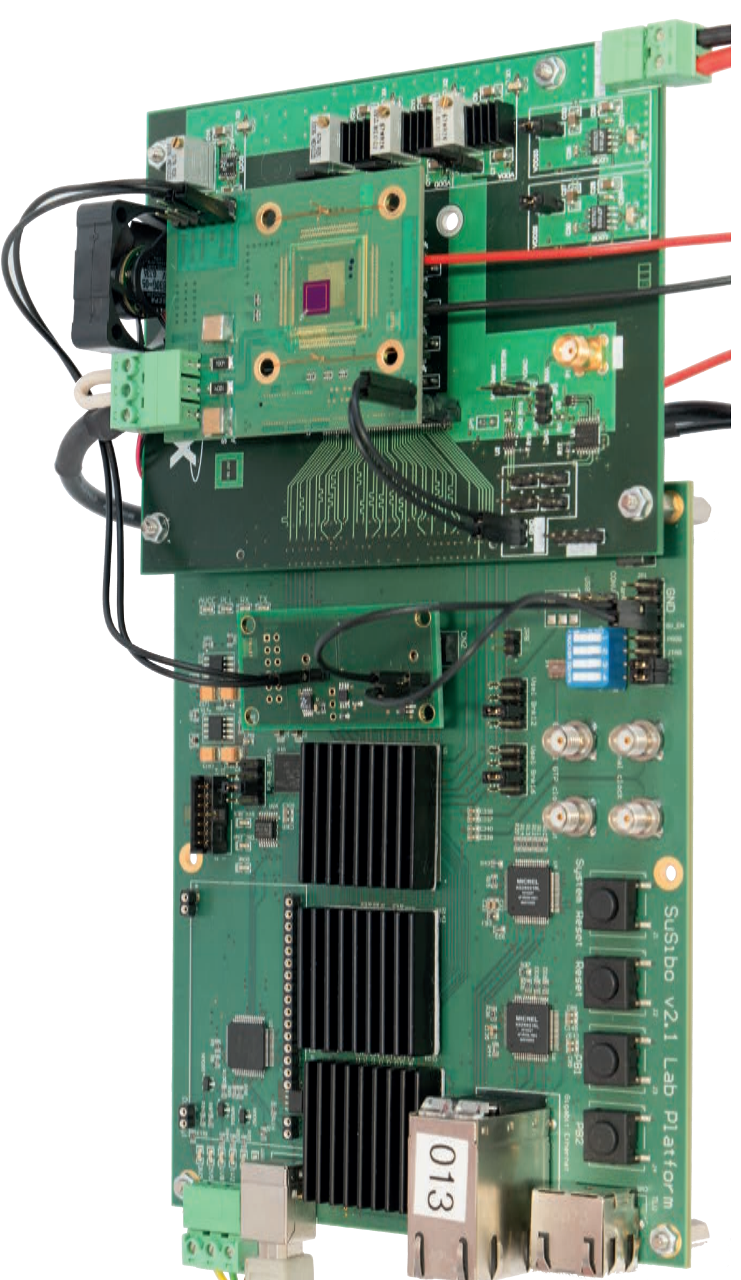
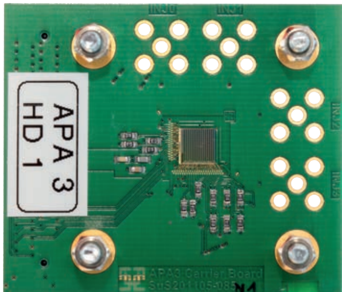


Figure 7.22: Photograph of the stacked boards for the APA 3 test readout. The Susibo is shown on the left, with the temperature readout PCB mounted on the small extension connector. The frontend board (lower board on the right) mates via the large extension connector. A carrier with HDI-PCB interposer is stacked on the frontend board, with the Peltier-cooled ASIC on the bottom side and 256 pixel sensor at the top. Some additional connections require jumper wires between the boards (temperature readout etc.)

plugged into. Through this connector, the supplies and all signals are passed to the ASIC, which is mounted to the carrier.



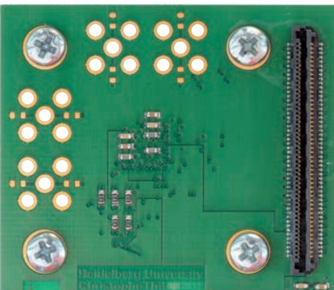


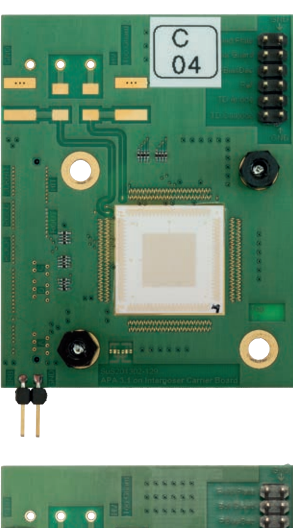
Figure 7.23: APA 3 carrier board with wirebonded ASIC on the top side (left) and connector to the frontend board on the bottom side (right).

Different carriers are built: For the APA 3 dies without factory-applied solder balls on the bump pads, a carrier where the ASIC is connected by wirebonds (Figure 7.23). For the APA 3.1 and later dies, a carrier where an interposer can be mounted is used, as the pre-balled bump pads cannot be used for wirebonding any more (Figure 7.24). The interposer is glued to the Gold frame around the center hole and then wirebonded to the pads at the carrier PCB. As the carrier is an entirely passive part, many of them can be built and therefore various ASICs and assemblies tested.

FIRMWARE Going from a small and simple FPGA board built for teaching purposes to a much more powerful and recent board developed for the control and readout of ASICs, the need for a firmware rewrite is obvious. Most of the firmware code is written in plain Verilog 2001, which can be synthesized to hardware resources independent of the used FPGA. But some elements for low-level interfacing to input/output and clocking resources and memory structures instantiate primitives of the Xilinx Virtex 5 FPGA [46] in direct as there is no generic way to describe the functionality in Verilog.

The main design goal from the previous FPGA based readout system is maintained: To push as much intelligence from the host computer to the readout system while maintaining the flexibility needed for efficient bringup and debugging of the chip. Therefore, many of the automated readout procedures which run independently of the host computer can be overridden by a manual mode, where each signal can be set, cleared and read out under full software control.

One big change from the old readout system is the availability of differential I/O structures, which can be accessed as such via the extension connector. At the boundary of the FPGA, incoming differential signals are received by *IBUFDS* structures, or *IBUFGDS* for clock sig-



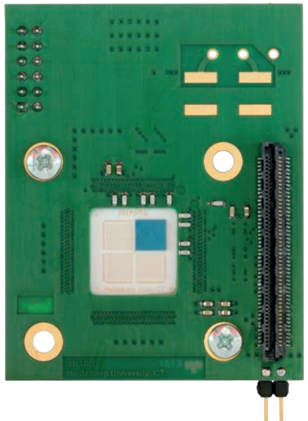
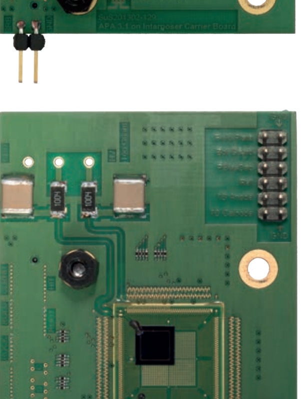
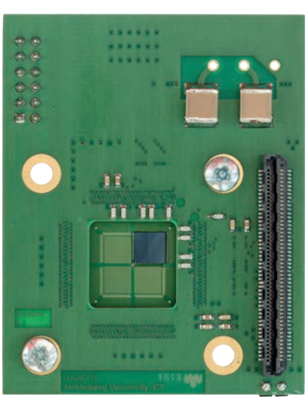




Figure 7.24: Carrier boards for APA 3.x ASICs. The ASIC on the interposer bottom faces towards the readout board, which mates with the black connector to the bottom of the carrier (right). The HDI-PCB interposer (bottom) is already equipped with a single quadrant 256 pixel sensor and the carrier prepared with components necessary for biasing it.

nals, which translate them to the internal signalling scheme. Similarly, outgoing differential signals are converted from the internal scheme to electrically differential signals by *OBUFTDS* cells, which can also isolate the line drivers from the output pins.

The second big advance from the previous Spartan 3E system is related to the operating frequency of the general purpose logic. Previously limited to about 50 MHz, switching rates of 200 MHz are possible, while datasheet values suggest up to 500 MHz, for example as the register-to-register performance of a 32 bit adder [47]. However, preceding tests have shown that at a useful level of combinational logic, a clock frequency of 200 MHz is a good tradeoff between the effort for the logic design and the time necessary for synthesis and

implementation, as the latter increases significantly at higher switching rates.

To reach the goal of switching the fast serial data lines at up to 400 MHz, serializers for the clock and load signals, *ROCK* and *ROLD*, as well as deserializers for the *ROUT* data lines are required. These blocks are provided by all the SelectIO capable pads for the Virtex 5 FPGA.

Apart from the FTDI master block, previously authored by another chair member [24], all code is specially written for this project (Figure 7.25).

Generated by a discrete oscillator, a 200 MHz clock is fed to the CLK manager block. There, it serves as the reference for two digital clock manager (DCM) primitives: The first one is statically configured to two output clocks of 200 MHz and 20 MHz, the system and system slow clock. The second one is also running at 200 MHz by default, but can be reprogrammed dynamically with a divisor and multiplier pair between 2 and 32 for the multiplier and 1 and 32 for the divisor. The synthesized clock and another one at 1/4 of it are used as the serial and parallel readout clock. The reprogramming and mandatory reset sequence is handled by the FPGA itself by a finite state machine (FSM). All four clocks are fed to the global clock tree which allows for fast equal propagation times, therefore low skew and jitter.

Communication between the FPGA board and a host computer is done via the USB interface. A dedicated discrete IC serves as an USB slave device, implementing the electrical layer and also the whole logical protocol stack. Towards the FPGA, it presents a bidirectional synchronous first-in first-out (FIFO) interface and a clock source, which drives another DCM primitive, used as the clock source for the whole communication between FTDI IC and the FPGA. A state machine inside the FTDI control master generates the control signals necessary to transfer all the data out of the FTDI chip to an 8 bit wide FIFO on the FPGA side, and also in the inverse direction, from a second FIFO to the FTDI chip. Both FIFOs have two independent clock sources to allow for safe clock domain crossing but also to buffer and therefore decouple the data stream between the host computer and the downstream logic, processing or generating the data words.

At the logical level, the communication between the readout board and the host computer is implemented as a packet-based multiplexing scheme with variable payload length. The packets are processed by the host communication block which decodes the packet header, therefore differentiates between a read request where the payload is transferred from the FPGA to the host or a write request where the data payload traverses in the opposite direction. A three bit subsystem ID multiplexes the 16 bit addresses to multiple memory blocks, allowing to split the address space into independent partitions. The payload data length is given by a 16 bit number at a granularity of

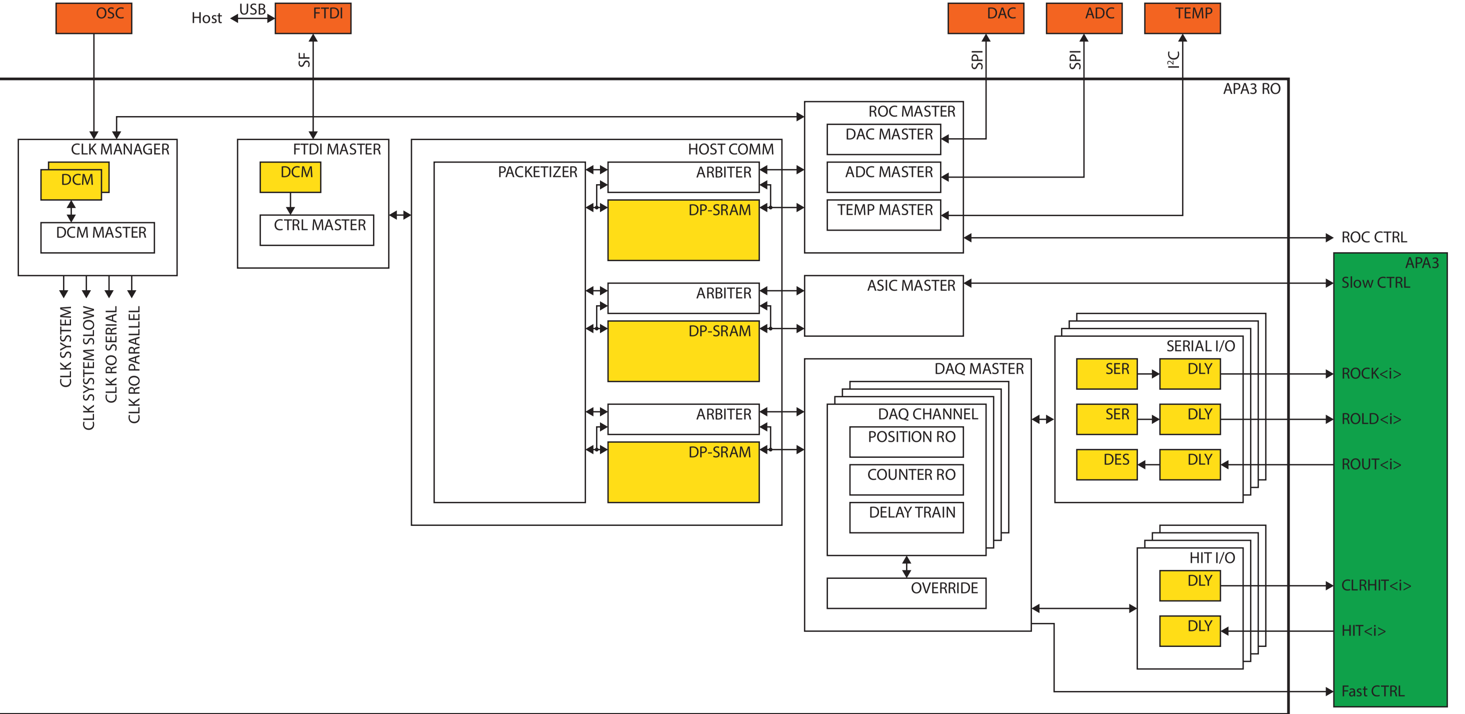


Figure 7.25: Structure of the APA 3 readout firmware for the Susibo FPGA board in conjunction with the APA 3 frontend and temperature sensor add-on boards. Mainly generic Verilog blocks are colored white and Xilinx Virtex 5 primitives yellow. Discrete components on the PCB are in orange while the ASIC is marked green.

32 bit words. For multiple memory word payloads, the memory address is automatically incremented upon reset to zero at the end of the address space.

Each subsystem provides a dual ported RAM with two independent clock inputs as the interface between the host communication block and the following logic, to separate clock domains while ensuring data validity. An address-level arbiter denies concurrent reading or writing to the same memory line by a request-grant scheme. Deadlock conditions are avoided by restricting the maximum lock time after which a previously given grant is recalled and the requester penalized in a wait state.

The three connected subsystems constantly monitor their memory for changes on certain trigger addresses. If an action is triggered, the corresponding bit in the memory word is cleared and written back without releasing the memory lock, protecting the memory from corruption, as an atomic read-modify-write operation.

The ROC master subsystem controls all functionality external to the ASIC, provided by components on the frontend PCB and the readout board itself. The power regulators for the frontend board can be shut down remotely. A voltage DAC as well as an ADC can be set and read out via two serial interfaces, allowing for some quick measurements without laboratory equipment. A temperature readout IC is mounted on an additional PCB which plugs into the small extension connector of the Susibo. The component is parametrized and read out via an I^2C bus and provides two remote measurement connections, one connected to the thermal diode pins of the ASIC, and also an integrated sensing in the IC itself.

The ASIC master subsystem implements the master controller for the slow control interface of the ASIC. The raw configuration words in the RAM are rearranged to the ASIC order and then sent over the serial interface by the *SDIN* line. Hence, the master not only emits the data stream, but also the necessary clocks, *SCK1* and *SCK2*, and the load signal *SLD*. By using the *SRB* readback wire, the latched configuration is read back and compared to the original datastream. Upon success, a flag bit is set within the memory.

By far, the most complex subsystem is the DAQ master. For each of the four serial readout ports, it implements an autonomous wire delay training using the readout register header and trailer bits, which shifts the deserialized datastream by coarse steps, equal to parallel clock cycles, fine steps, equal to clock cycles of the faster serial clock, and sub-clock cycle units using adjustable delay elements. Further, for all channels in parallel, FSM controlled blocks to read out the hit position and the per pixel counter values are present. These blocks not only generate the required *ROCK* and *ROLD* pulses to shift out the data, but also reorder the received raw bitstream from its pixel-wise interleaved format to an abstract representation of common bi-

nary LSB 0 format for the position and counter data using a multitude of helper structures and allow for safe crossing of the clock domain by synchronizing FIFOs. As some of the fast control signals are shared across all readout channels, the DAQ master also implements an arbiter for these lines, allowing either for synchronous operation on all channels or sequential transfer on selected ones. Given the complexity of these state machines and the necessary knowledge of the timing requirements, all signals can be slowly controlled in an entirely software controlled mode by the host computer if the data acquisition is set to *override mode*.

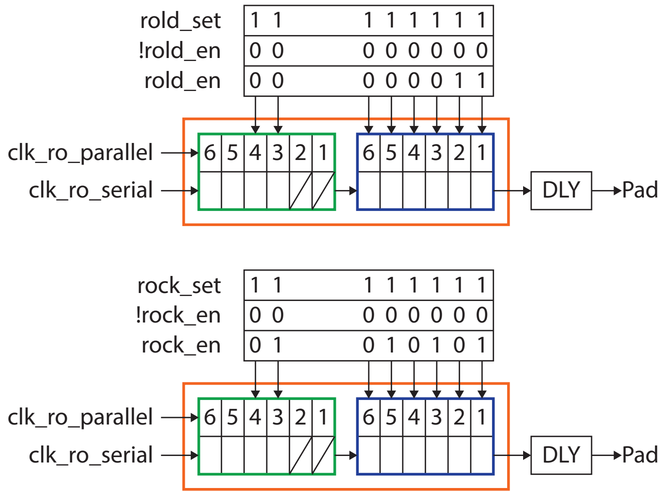


Figure 7.26: Generation of the *ROLD* (top) and *ROCK* (bottom) signals by serialization of a fixed pattern with a DDR serializer. The serializer (orange) is built of two six bit blocks chained as master *OSERDES* (blue) and slave *OSERDES* (green), where the first two bits of the slave must be left unconnected and the last two bits are unused. One of the three patterns above each serializer is selected depending on the requested output. Both serializers use the same pair of clocks, but the *ROCK* signal is delayed at the output to allow the *ROLD* signal to overlap both edges of the first *ROCK* high pulse.

Each serial I/O channel consists of two serializers, one for the *ROCK* clock line and another for the *ROLD* load line, and a deserializer for the *ROUT* signal. To get the most precise timing, DDR cells are used for the clock and load output signals, as they are physically located in the output pad, thus with least interconnection latency and jitter, and can be employed to generate arbitrary defined logic values at two precisely defined clock edges. As the Virtex 5 is limited to 6:1 serialization, but an 8:1 serialization is necessary to implement the 4:1 serialization at both clock edges, two *OSERDES* primitives must be chained (Figure 7.26). For the clock serializer, a static 1-0

pattern repeating four times is connected at the inputs when clocking is enabled. For the load serializer, the static pattern is two times a 1 with the following six times 0. The deserializer for the input signal runs at single data rate (SDR), therefore one *ISERDES* is sufficient for the 1:4 deserialization. Delay elements after the serializers shift the load pulse to the center of the corresponding clock pulse by a static amount, as these cells can only be adjusted while building the firmware. The input delay of the *ROUT* deserializer however can be set to an optimum sample time during runtime by the DAQ master.

Python modules can be structured into directories. With a magic __init__.py file, this directory is considered as a module, which can be imported at once. Modules can be nested, allowing hierarchical structures.

SOFTWARE The software to control the readout system consists of a Python package with several modules and an initialization file, which the Python interpreter runs before it drops to interactive mode. Access to the FTDI hardware via the USB is provided by the *ftdi1* package [19], abstracted from the actual hardware by the UsbComm class. A generic blocking send/receive interface is implemented, which also splits and reassembles data packets as necessary by the limited hardware buffer space. On top of this, the Packetizer class provides a software implementation of the various FSMs located in the host communication block of the FPGA. Read and write calls on an object of this class generate necessary headers, assemble and send the packet. Returned data from the readout is interpreted and disassembled upon arrival. Sub-packages contain classes for the three subsystems as defined by the FPGA firmware, ROC, ASIC and DAQ. By the instantiation of these, object trees are created which represent, by their getter and setter methods, various parameters without the user needing to know of the physical representation of the data. Any data is solely stored in the subsystem memory on the FPGA. As some software objects share a single memory word with others, it is read ahead of modification and then written back in a single call, preventing data corruption by concurrent access. As all of the multi-bit data is already reordered to common binary representation by the FPGA firmware, the data processing is limited to unmasking respective values from the memory words and to check for its validity ahead of a write cycle.

The provided initialization file creates an initial set of objects to access the ASIC and the various functions provided by the frontend and temperature readout board. Then it drops to the regular Python interpreter, where any regular command can be used which allows easy interactive and also scripted usage of the system. A set of commonly used methods is written to fully automate test procedures.

Persistent storage of raw measurement data is implemented by the PANDAS [32] library. For graphical representation of the data, different plotting methods by matplotlib [18] are used.

Compared to a graphical interface, easy sequential scripting with the Python language and the availability of (self-written) packages to

access measurement equipment leverages the IPython [34] interpreter to a powerful and extensible measurement control system.

7.3.5.2 *Readout system for beam measurements*

At the time of writing, the frontend board, designed and manufactured by DESY, has completed its first production batch. Together with the readout board, it is electronically tested and the necessary firmware and software is built at the ESRF.

Part III

MEASUREMENTS WITH THE XNAP DETECTORS

The prototype system with reduced pixel count is tested in detail at the laboratory. Instead of X-ray illumination from a Synchrotron source, visible light photons and those generated by the radioactive decay of sealed sources are used for measurements. At the ESRF, the prototype detector is studied in-depth using a special X-ray generator, while selected properties are analyzed during a short beam time test at the Synchrotron itself. A subset of the measurement results with the prototype is presented together with recent results of laboratory measurements obtained using parts of the final large-scale detector.

8

16 PIXEL PROTOTYPE TESTS AT THE ESRF

Apart from pure electronic tests of the ASIC in the laboratory and experiments also involving the sensor, where radioactive check sources are used as X-ray emitters, the 16 pixel prototype was tested at the ESRF. Due to limited availability of the expensive beam time at the Synchrotron, a special X-ray source was used, developed and commercialized by the Institut Laue-Langevin (ILL), located at the same scientific campus as the ESRF. Aside from timing measurements, this source can be used to characterize the full detector stack, including sensor, ASIC, various PCBs and the readout system, as a focused spot with high flux can be directed at the detector. Timing measurements at the Synchrotron are carried out as an addition, but only during a much shorter period. A subset of the results is published in [44].

8.1 PREPARATION

8.1.1 *Assembly of detector heads*

For the beam test, six complete detector heads are built, as this is the most convenient exchangeable unit for testing multiple ASICs and sensors.

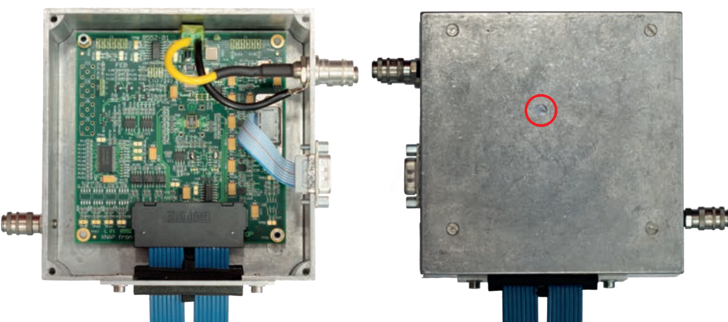


Figure 8.1: 16 pixel detector head, mounted in the shielding box for X-ray tests. The box is closed on its rear side, giving access to the upside down mounted PCB exposing the ASIC (left). On the front side, the X-ray entrance window, marked by the red circle, is a drilled hole covered with visible light tight foil (right).

The detector head consists of a machined Aluminium enclosure with holes at the front and the back side in the axis of the sensor

(Figure 8.1). These holes are covered by a metallized Mylar film to shield the detector from visible light while transmitting almost all of the X-ray photons. Power supply connections for the frontend board and also the high voltage sensor bias are extended to a D-Sub respective SHV socket mounted in the enclosure. The data connection to the readout board is done by a shielded ribbon cable, routed inside the box through a slit, which is sealed by black foam and metallized tape.

No direct cooling is provided to the ASIC, therefore it radiates energy together with the components on the frontend board, heating the air volume inside the box. To avoid thermal runaway, two ports to connect hoses for pressurized air are mounted at opposite directions in the sidewalls, forcing an air flow inside the box to remove the heat.

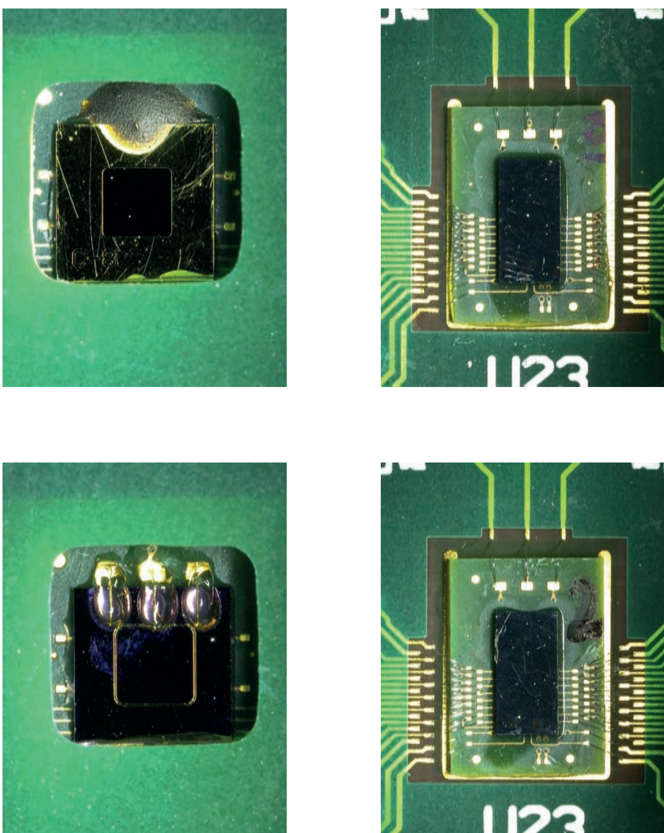


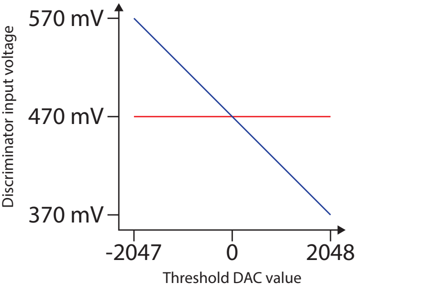
Figure 8.2: Sensor (seen through X-ray hole) and ASIC (from the back) on 16 pixel detector head 1 (top row) and 9 (bottom row).

Two detector heads are selected for in-depth analysis: System 1 is built of a second generation frontend PCB, where an APA 2.1 ASIC is mounted to a second generation HDI-PCB interposer together with a

divided cathode sensor (Figure 8.2, top). System 9 uses a modified second generation frontend PCB with the same ASIC-interposer configuration, but with a divided anode sensor (Figure 8.2, bottom). These modifications are necessary as several components on the PCB are conceived for the divided cathode sensor. To operate the divided anode sensor, polarized capacitors and protective diodes must be reversed to fit the inverted polarity of the sensor bias. In addition, the guard ring DAC must be removed and its connection bridged to the high voltage supply.

8.1.2 *Electronic and basic optical tests*

The electronic test routine, as described on Page 87, can not only be run with the probe card, but also with a wirebonded interposer assembly on the frontend board, as the electrical and mechanical interface to the readout system is equal. After each ASIC passing these tests, scans with the embedded threshold DAC are used to check for connectivity between the ASIC and the sensor and to probe for the basic photodiode behavior.



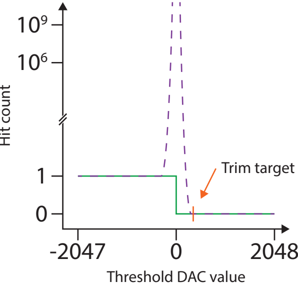


Figure 8.3: Effects of different threshold DAC settings: On the left, voltage at the discriminator inputs, at the threshold (blue) and a signal port with no current flow (red). On the right, the resulting number of hits when scanning the threshold is shown, with its theoretical (green) and actual (dashed purple) values.

The hit counter in each pixel has a well defined behavior to static signals (Figure 8.3). Assuming no signal input current, the voltage at the TIA output as seen by the discriminator only fluctuates due to the system noise (red graph, left plot). The threshold voltage however decreases when scanning the threshold DAC in positive direction, by the nature of the inverting amplifier (blue graph). For the given example, the polarity of the discriminator is set to straight, its output is therefore logical high if the threshold voltage is positive compared to the signal voltage, and low if the signal voltage is positive compared to the threshold.

For each threshold DAC step, the input signal is fed to the hit counter for an constant interval, after which it is suppressed and the counter read out. The counter therefore increments by exactly one hit if the discriminator output is high, or keeps the previous value if the discriminator output is low (green graph, right plot).

For a small range of threshold DAC settings, where signal and threshold voltage are almost equal, the counter increments at a very high rate, as noise sources in the signal and the threshold path trigger false hits (dashed purple graph). Both width and position (in DAC counts) of the noise peak are used to characterize each full detector channel, including the sensor itself.

The electrical connection with the bias circuit and the ASIC as well as basic photon sensitivity of the sensor is verified by applying a moderate reverse bias in the order of 100 V to deplete the Silicon, but low enough not to initiate avalanche multiplication. Then, the threshold DAC is scanned while recording the center and width of the noise peak, once at dark, once under illumination (Figure 8.4). Channels where the peak center does not move due to the photocurrent are considered dysfunctional and masked from further operation. Some defective pixels leak current to neighbor pixel, which is detected by reversed current polarity. A cross-check is made by correlating the total photocurrent via the shared electrode to the amount of DAC units the peak moves with varying light intensity.

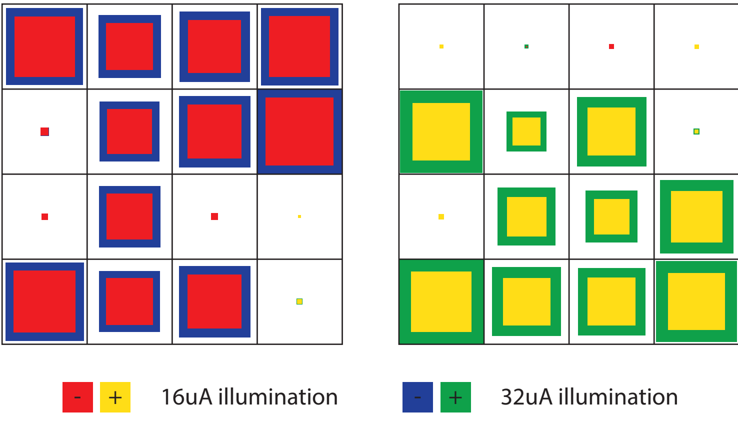


Figure 8.4: Relative shift of fitted noise peak for detector heads 1 (left) and 9 (right) by LED illumination. The color indicates the polarity whereas the area of each box corresponds to the normalized current. Pixel 0 is in the upper-left edge.

In a first attempt, the variations at ASIC and sensor level leading to a dispersion of the noise peak position are also corrected by trimming the edge after which no dark hits are detected at all (Figure 8.5): First, the local trim range for a given global *DACTRIM* setting is mea-

sured by a threshold scan, then optimal settings are calculated for each pixel. This simple but powerful method allows for dispersion reduction from about 300 DACU to seven DACU for detector 1 and from about 200 DACU to 15 DACU for detector 9.

Although impossible to measure in direct the value of one DACU, it is calculated to about 25 nA.

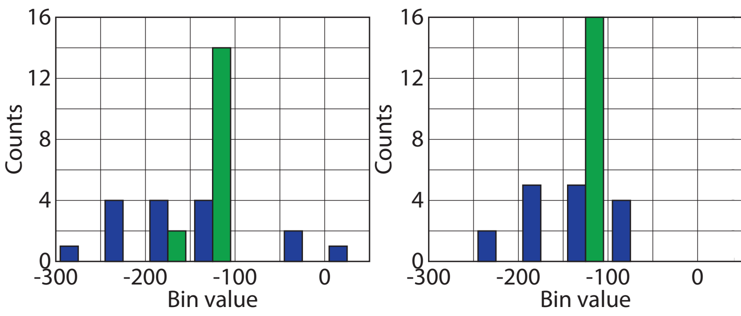


Figure 8.5: Dispersion of noise peak, measured by threshold scans for detector 1 (left) and 9 (right), prior (blue) and after (green) trimming. Each bin is 50 DACU.

8.1.3 *Sensor tests with radioactive sources*

The dynamic behavior of the detector head is studied with radioactive test sources: A small amount of the ^{55}Fe isotope, enclosed in an acrylic glass disk, emits X-ray photons at discrete energies, about 25 photons per 100 disintegrations at 5.9 keV and 3.4 photons at 6.5 keV. As the disintegration rate is low and the emission is isotropic, the source must be located as close to the detector as possible to cover most of the irradiated sphere with the detector, in order to maximize the count rate.

Both detector heads are used in counting mode with the source, integrating the number of hits over 10 s. From the source parameters and geometric properties, an ideal per pixel photon count rate of 100 $^1/_s$ is estimated.

As no direct cooling of the ASIC or the sensor is implemented at this time, the dark current of the APD is many times higher than the designated value for its operation. The divided cathode sensor in detector head 1 operates at −560 V at about 0.5 uA dark current. Detector head 9 with the divided anode sensor is much more sensitive to temperature: Biased at 420 V, the initial dark current at room temperature is about 2 uA, rising to 3 uA after one hour of operation. As a simple countermeasure, the whole setup is placed in a climatic chamber cooling down the environment to about 20 °C, allowing for about one hour measurement time before the dark current rises high and the signal to noise ratio gets too low.

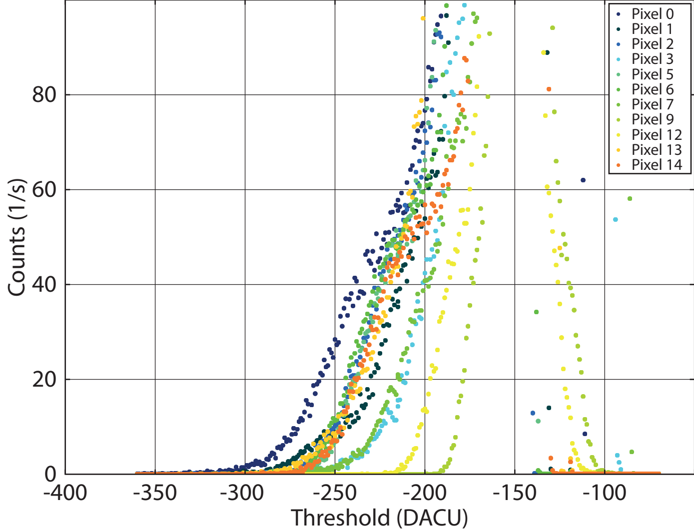


Figure 8.6: Threshold scan for detector 1 using the 5.9 keV ^{55}Fe source. The noise peak with 50 DACU width is right of the X-ray events.

With detector 1, X-ray photons can be detected left of the noise peak, although the threshold band is very narrow with about 50 DACU (Figure 8.6). Even after successful trim, the threshold edges vary between the pixels. The count rate has no clear plateau at which it is almost independent from the threshold setting, which is the desired area to set the discrimination threshold.

With detector 9, the counted X-ray photons are right of the noise peak, as the discriminator polarity is reversed, but so is the signal polarity, as the sensor is read out from the opposite electrode side (Figure 8.7). Apart from one pixel, a clear plateau with significant width can be seen where the photon count is almost independent from the threshold setting and also from the pixel. The plateau itself has a width of 100 DACU and extends with decreasing count rate by another 100 DACU.

Compared to the estimated per pixel hit rate of 100 1/s, about 20% are detected and counted by the system.

8.2 MICROFOCUS X-RAY TUBE TESTS

8.2.1 *Setup overview*

The X-ray source consists of two parts: The generator itself, where a Copper target is used as the anode for the electron beam. The characteristic K_α emission by the Copper target defines the photon energy of 8 keV. The raw beam traverses the evacuated X-ray optics, where

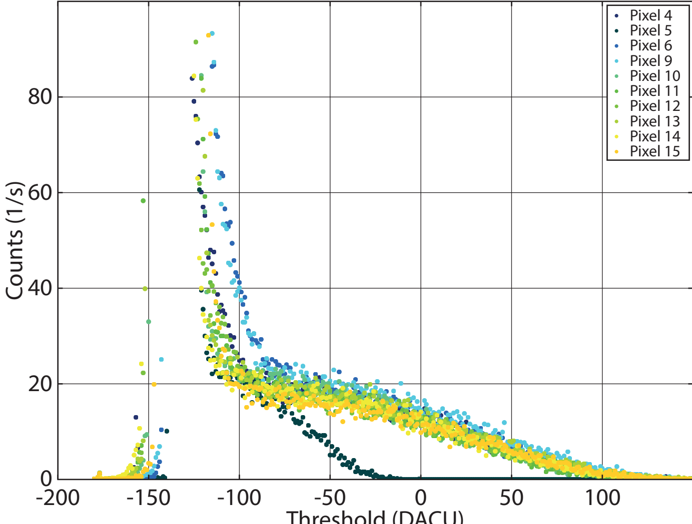


Figure 8.7: Threshold scan for detector 9 using the 5.9 keV ^{55}Fe source. The noise peak with 50 DACU width is left of the X-ray events, which are visible as the threshold-independent plateau between a setting of -100 and 0 and further extending to +100.

it is focused to a semi-circle shape with a full width at half maximum (FWHM) size of 100 um. At the exit window, a monochromatic and low divergent photon flux of 10^8 1/s is achieved, with the focal pane about 20 cm in front of the window.

To reduce the X-ray photon flux, the generator current can be lowered, but as this has a negative impact on the beam quality, a set of absorbers is placed in the beam (Figure 8.8). The absorbers are made of thin, high uniform Aluminium and Copper sheets mounted in handling frames.

The detector head is mounted on a motorized stage which can be shifted with micrometer precision along all three axis (Figure 8.8). For the initial adjustments, a sheet of X-ray fluorescent film is placed over the X-ray entrance window. By the spot of visible light transmitted out of the shielding room by a video camera, the sensor is positioned in the center of the beam.

To estimate the photon flux ratio at the detector when using different absorbers (Table 8.1), a reference APD with associated electronics is used (Figure 8.8). The single element APD has an active area of 10 mm × 10 mm and a thickness of 200 um. In order not to lose low energy X-ray photons in the thick junction, it is illuminated through the anode side.

Material	Thickness	Transmission factor for 8 keV X-rays
Aluminium	100 um	0.27578
Aluminium	100 um	0.27578
Copper	50 um	0.10217
Copper	100 um	0.01044
Copper	105 um	0.00831
Polyimide	4×75 um	0.77525

Table 8.1: Filter materials, thicknesses and transmission factors used for 8 keV X-ray tests.

8.2.2 *Energy selectivity*

Threshold scans, as previously described with the ^{55}Fe source, are also carried out with the 8 keV X-ray photons. The beam is positioned at the center of an individual pixel. With the high intense beam, short integration times for counting in the order of 1 s are possible while the flux is still orders of magnitude higher than with the radioactive source.

With the X-ray generator, the plateau with almost constant count rate is more pronounced than with the radioactive source, whereas the slope of the count rate decrease with increasing threshold is the same (Figure 8.9).

Even if the focused beam spot is positioned at the center of the pixel, charge sharing effects in the adjacent pixels can be seen: The pixel counters of direct neighboring cells of the illuminated pixel increase by about two orders of magnitude less than the main pixel, but still with significant rate.

For spectral analysis of the threshold scan, the counter data, representing the integral pulse height distribution, is fitted to a modified s-curve, to model the charge sharing effects by the drifting charge carrier cloud in the sensor as proposed by [26]. The XNAP detector is not designed to provide direct information on the incident photon energy, but as any threshold scan and the fitted s-curve contains the integrated energy information, it can be retrieved from that by differentiation. If the detector is illuminated with monochromatic photons, the width of the spectral response peak indicates the overall noise from the sensor and the readout electronics, as it widens the incident spectral line.

For detector 9, two classes of spectral responses are obtained for the responsive pixels (Figure 8.10): The majority shows an equal FWHM width of about 135 DACU centered at a threshold DAC value of 125. These pixels exhibit the typical s-curve shape with a significant

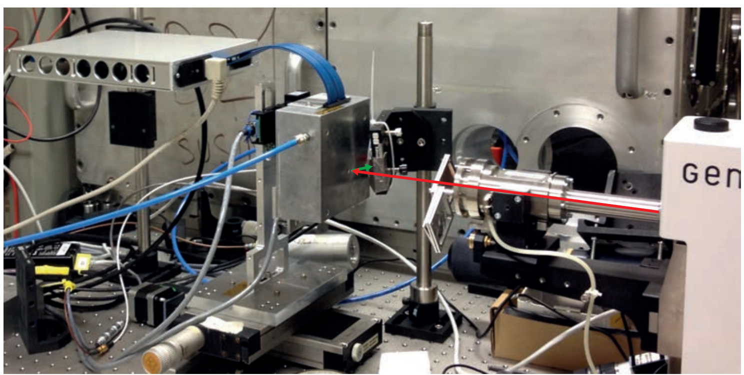


Figure 8.8: Overview of the microfocus X-ray tube setup. The white box at the right holds the X-ray source, where the optics for focusing and the filter sheets are also mounted on. The primary path of the beam through different absorbers is shown by the red arrow. The detector head is at the center with a number of cables and pipes, connected to the readout in the upper-left edge. The path of scattered photons towards the reference detector is shown by the green arrow.

plateau. The second set in pixel 1, 5 and 7 is characterized by a narrow spectral peak close to the noise edge, indicating a lower margin between the noise floor and the upper threshold limit for detection.

From the threshold scans, the exact source for these variations cannot be concluded, as the sensor itself may have non-homogenous collection efficiency or variation in amplification, or the electronics chain may influence the signal current.

To estimate the noise margin for detection of low energy X-rays, the s-curves and derived spectra are compared to those resulting from irradiation with monochromatic 5.9 keV photons from the ^{55}Fe source. For better statistics, these measurements are redone at the ESRF with a higher activity source, although still emitting photons by one order of magnitude less than the X-ray generator. For pixels of the second group within the X-ray tube test, only pixel 5 counts the lower energy photons and exhibits a threshold curve with distinctive shape, although the mean value of the fitted s-curve is with -49 DACU significant less than those of the first group, at about 45 DACU. Thus, from the relative shift of 80 DACU between the 5.9 keV and 8 keV spectra and an assumed linearity between the threshold DAC setting and the system response to the incident photon energy, the value of 38 DACU per keV photon energy is concluded.

As a second metric, the FWHM energy resolution is calculated as the ratio of the FWHM of the fitted s-curve and the shift of the s-curve mean value from the mean of a Gauss distribution fitted to the noise

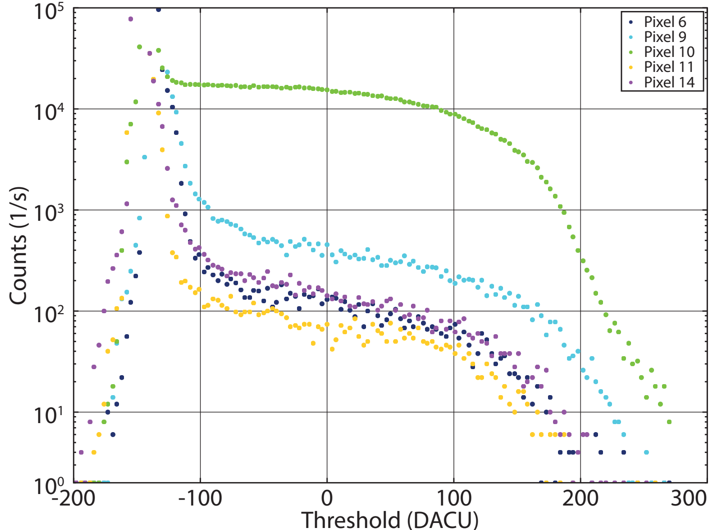


Figure 8.9: Threshold scan for detector 9 using the 8 keV microfocus X-ray source, directed at pixel 10. The adjacent pixels also collect charges, while other pixels exhibit no significant counter increments.

peak. The average value is in the order of 50% for the 8 keV and 59% for the 5.9 keV photons

The applied high voltage bias to the sensor has important effects on the energy resolution: By increasing bias, the gain of the APD increases also, delivering a larger signal current to the electronics. On the other hand, the surface and bulk leakage currents also increase, and, for the bulk leakage, are also multiplied by the increasing avalanche gain. Further, the excess noise factor, modeling the statistical avalanche gain fluctuations, is also a function of the gain, increasing linear proportional at large bias.

The sensor in detector 9 is operated at a reverse bias between 400 V and 435 V, below breakdown of the junction (Figure 8.11). At 420 V, which is the bias used for all other measurements, the dark current is in the order of 200 nA.

With reduction of the sensor bias, the energy resolution increases, giving 45% FWHM at 400 V for the 8 keV beam. By increasing the bias voltage, the increasing noise degrades the energy resolution to 50% FWHM at 430 V.

8.2.3 *Spatial response*

The spatial response of the detector is also analyzed with the microfocus X-ray source. For the mapping procedure, each detector is

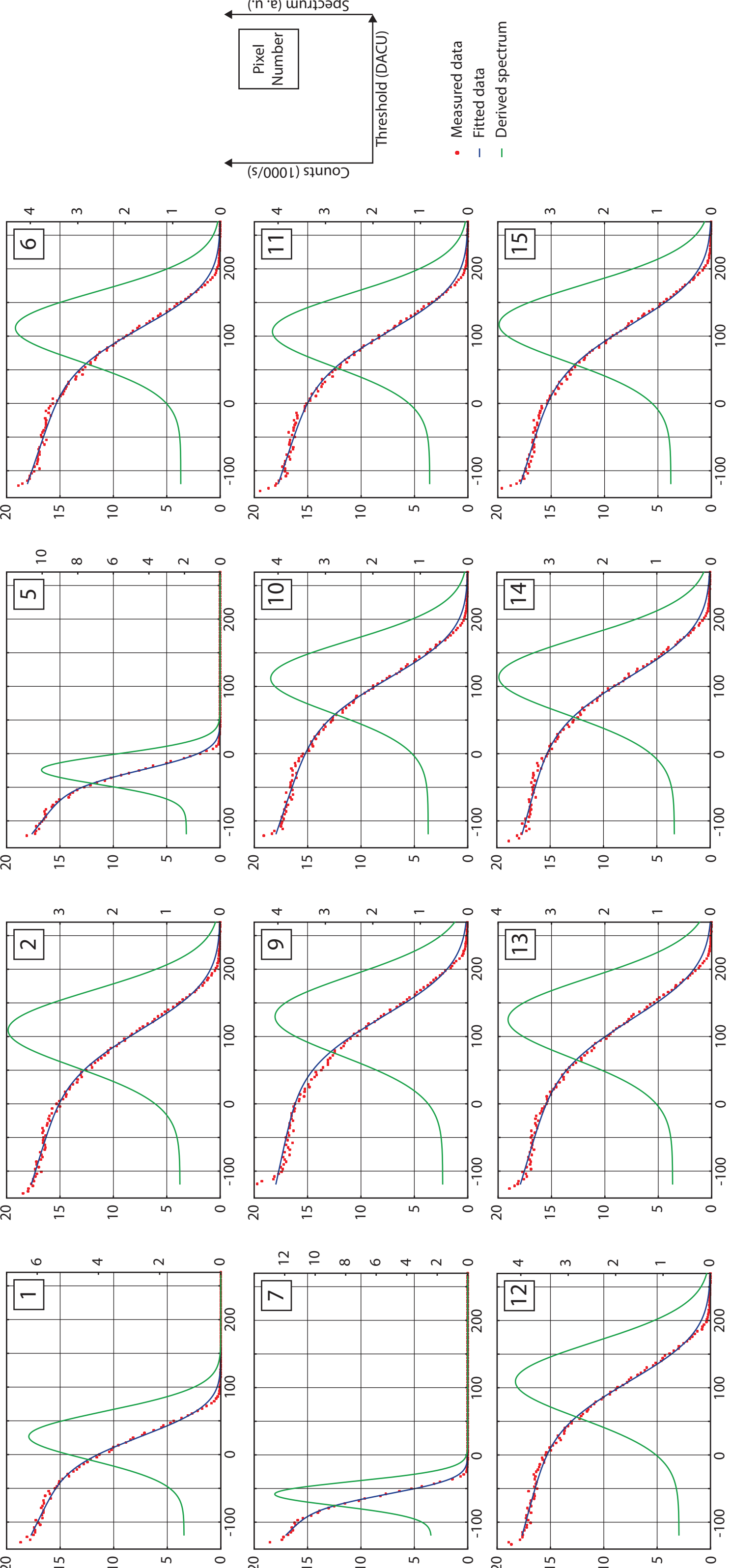


Figure 8.10: Pixelwise threshold scans for detector 9 with the X-ray source, fitted s-curve model and derived spectral response. Defective pixels are omitted.

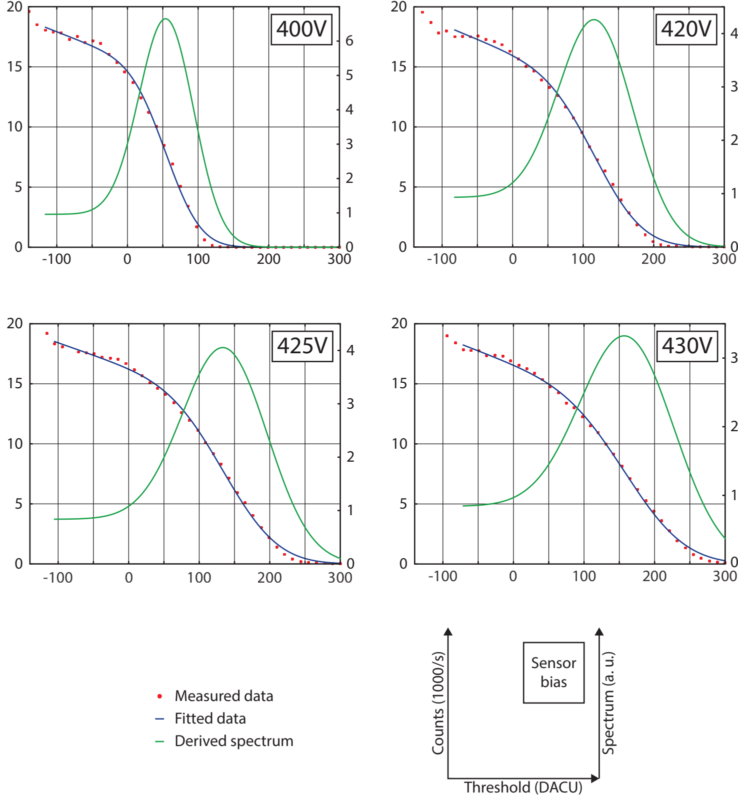


Figure 8.11: Threshold scan for detector 9 using the 8 keV microfocus X-ray source, directed at pixel 12, with different high voltage bias applied to the sensor.

trimmed for a common threshold level as previously determined by the threshold scans, where the incident photons can be detected with (virtually) no background. The beam is focused at the center of the first pixel by scanning the distance to the source along the beam axis.

The focused beam is scanned through the pixel centers, once along the horizontal, then along the vertical axis while keeping the other coordinate fixed to the respective center of the pixel. During each step, the photon counts are read out for each pixel counter. After the completion of the eight scans, the raw counter values are processed and combined into an intensity map, where for each of the 16 pixels the area is shown where incident photons lead to an incrementing photon counter.

For the perfect detector, the darkest spot on each individual map should correspond to the position in the overall map, therefore the counter only increments when the photon beam illuminates the selected pixel, and does not increment when illuminating other positions outside the pixel itself. For example, the map in the upper left

cell of Figure 8.12 should show a dark spot also in the upper left edge, where all other positions should be empty.

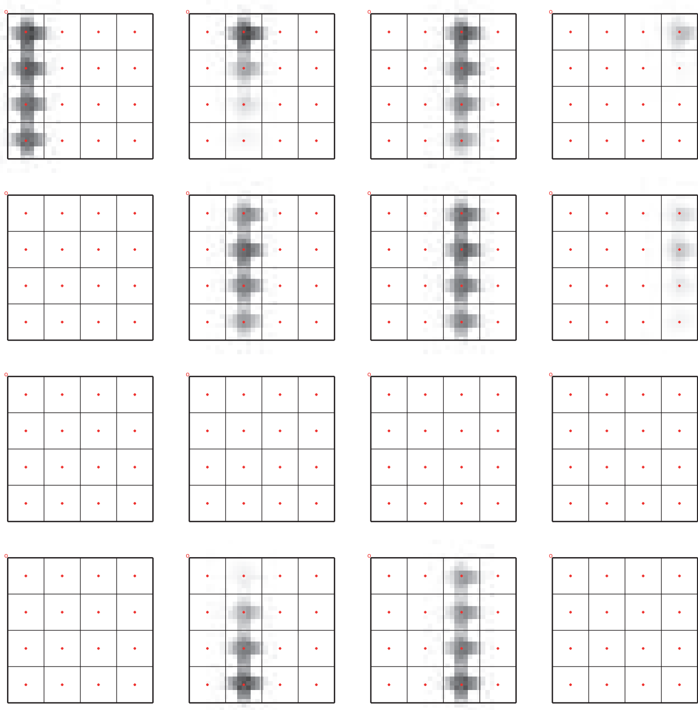


Figure 8.12: Photon collection map for detector 1. Pixel 0 is in the upper left edge of the overall and the individual pixel maps. The pixel centers are marked by red crosses. The number of collected photons is encoded in the intensity, where dark shading corresponds to more photons than light.

The spatial response to X-rays of detector 1 can be divided into three categories (Figure 8.12): First, a large number of pixels do not respond at all to the incident photons. Second, at pixel positions 3 and 7, very little response to photons is seen, whereas the third group exhibits significant response to photons.

Even if for some pixels photon collection and conversion into an electronic signal works fine, there is a major problem regarding position sensitivity, as all pixel counters also increase at a high rate if their proper pixel is not illuminated, but also increment when illuminating neighboring cells.

The crosstalk is predominant along the vertical axis, as the counters increase if the pixel above or below is illuminated, but almost keep their value if the horizontal neighbors are so. Even if the pixels are vertically shorted, the area of the APD structure with little or no avalanche multiplication can be seen as the count rate decreases

when the beam is in between two pixels, independent of variations of the threshold setting.

Within this detector, no pixel can be pointed out as the reference as there is no pixel solely responding to X-ray illumination on its proper position.

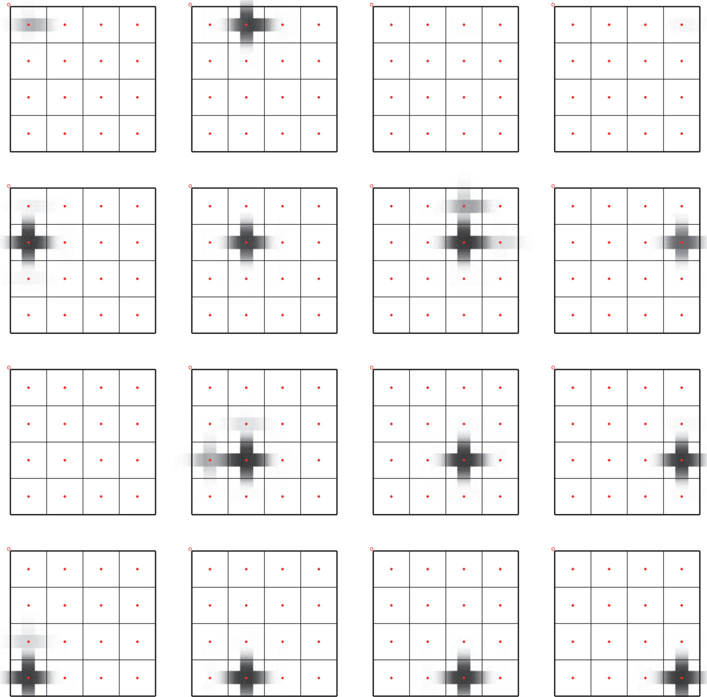


Figure 8.13: Photon collection map for detector 9. Pixel 0 is in the upper left edge of the overall and the individual pixel maps. The pixel centers are marked by red crosses. The number of collected photons is encoded in the intensity, where dark shading corresponds to more photons than light.

The detector head 9 is scanned with the same procedure, although the step size is reduced from 35 um to about 9 um (Figure 8.13). Like the other detector head, three pixels do not react at all to X-ray illumination, while pixel 0 increments, but only with little sensitivity. Most of the pixels however are highly sensitive to incident photons.

Crosstalk effects are less pronounced than with detector 1 and do not show a directional preference: Pixel 6 also increments when illuminating the one above, pixel 9 when illuminating the pixel left of it, but both at a lower rate than the proper pixel itself.

The four pixels in the lower row exhibit the stipulated position response. Hence, they are chosen to analyze the threshold dependent double count behavior at the interface between the pixels.

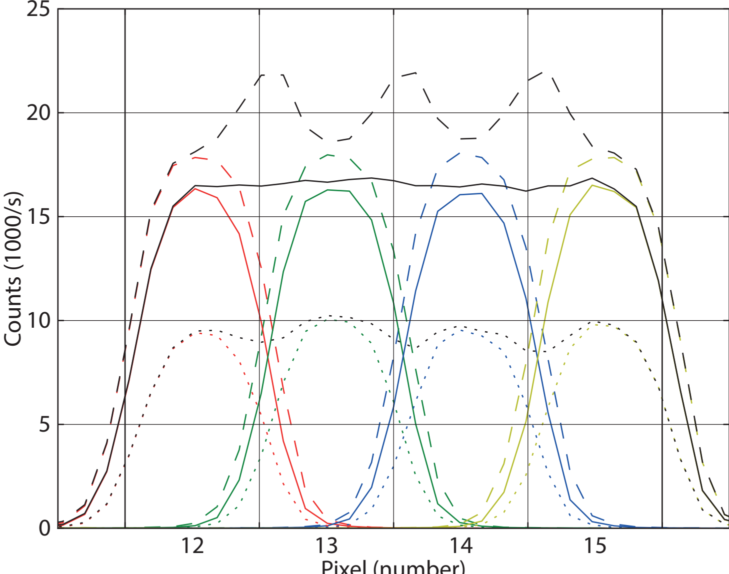


Figure 8.14: Photon count rates depending on X-ray beam position, scanned horizontally through pixel 12 to 15, and the sum of photons for these four pixels (black plots). Three threshold settings are shown: The dashed threshold is set too low, while the dotted is too high. The continuous lines are at optimum threshold. The theoretical APD array boundaries are indicated by the thicker vertical lines, but due to misalignment, slightly shifted to the right.

An optimal threshold setting is particularly important for the divided anode APD structure, as there is no physical isolation between the multiplication zone of each pixel. Therefore, a charge cloud can split between multiple anode pads, leading to double counts if the threshold is set too low. The count rates for four adjacent pixels are recorded for an X-ray beam sweeping across the pixels (Figure 8.14). The black plots, showing the count sum of the four pixels, depicts the threshold dependence: In between the pixels, the count rate increases exceeding the number of photons if the threshold is set too low, counting the split charge clouds as multiple independent photons (dashed plot). If the threshold is set too high, the photon count decreases also within the pixel centers. When set even higher, split charge clouds in between the pixels do not trigger the counter, leading to losses (dotted plot). An optimum threshold results in a flat count rate sum (continuous plot) across adjacent pixels.

8.2.4 *Maximum count rate evaluation*

The maximum rate at which the whole detector can count independent photons is evaluated by comparison of the photon flux and the number of counted events. The photon flux is controlled by inserting different combinations of attenuating sheets (Table 8.2). As there is no reference detector available which can be safely mounted into the direct beam and being fast enough to count every photon, an indirect approach is used: The reference APD head is placed next to the XNAP detector, but outside the primary beam path facing towards the X-ray entrance window. The backside of the reference detector is covered with shielding material to minimize background noise, resulting from any scatter in the primary beam path. The X-ray entrance window on the XNAP detector is covered with a Polyimide film, which transmits about 78% of the incident photons towards the detector, but also scatters back a fixed fraction of photons, of which a certain part is counted by the reference detector. As the number of events in the reference detector is below its counting limit, therefore operating at its maximum detection efficiency, it can be seen as linearly proportional to the flux of primary photons and therefore to the number of photons hitting the XNAP detector.

With the attenuating sheets, eight different absorption factors are combined, while recording both the count rate at the XNAP and the reference detector.

During a 30 s integration period, both detectors are irradiated with different photon fluxes. In Table 8.2, transmission factors and the normalized counts per second for both detectors and the respective reference counts are given. The reference counts slightly vary between the two measurement series as the arrangement is changed.

On the low flux end of the measurements, the backscatter ratio fluctuates a lot, as a single background photon captured by the reference detector already has big impact. Neglecting the first and the last photon flux items, the backscatter ratio, the number of scattered photons into the reference detector per photon captured by the XNAP detector is almost constant. This indicates that at the given count range, neither detector is saturated by excessive incident photons. With the unattenuated beam, saturation effects are visible for the XNAP detector as the count rate drops by $^1/_3$.

The detector dead time and the resulting maximum count rate is commonly modelled by one of the following two ideal models [23], depending on the system behavior on excessive event flux. Each detector has an intrinsic dead time during which further events cannot be processed and therefore are lost. The *nonparalyzable* model assumes that additional events during that deadtime have no prolonging effect to it, whereas the *paralyzable* model does so, while still not being counted as additional hits.

Material and thickness	Trans-mission	Detector 1 Detector 9	Reference Reference	BS ratio
No attenuator	100 %	80180700	18607	4309
		82417900	18826	4377
Al 100 um	27.578 %	32708000	5151.3	6349
		34826100	5244.7	6640
Cu 50 um	10.217 %	14248800	2036	6998
		15378200	2075.2	7410
2x Al 100 um	7.605 %	9763590	1415.4	6898
		10726500	1454.7	7374
Al 100 um	2.818 %	4118570	574	7175
+ Cu 50 um		4435710	577.1	7686
Cu105 um	0.831 %	1603020	224.9	6546
		1730540	225	7691
2x Al 100 um	0.777 %	1150410	166.2	6922
+ Cu 50 um		1216090	168.6	7213
Cu 50 um	0.085 %	176151	27	6524
+ Cu 105 um		192560	29.2	6595
Cu 100 um	0.009 %	9224	3.3	2795
+ Cu 105 um		9803.8	3.1	3162

Table 8.2: Forward and backscatter X-ray photon count with different filters, resulting in different primary photon fluxes. Detector 1 and 9 photon counts are normalized to one second. The backscatter ratio gives the number of counted transmitted photons per counted backscattered photon.

For the nonparalyzable model, the number of lost events is solely dependent on the system dead time τ and the count rate, with a count rate asymptotically converging to $1/\tau$. The paralyzable model however peaks at a maximum rate, after which the count rate decreases again by pile-up of dead time slices. The true rate n and the observed rate m are given by

$$m = n \exp -n\tau \tag{8.1}$$

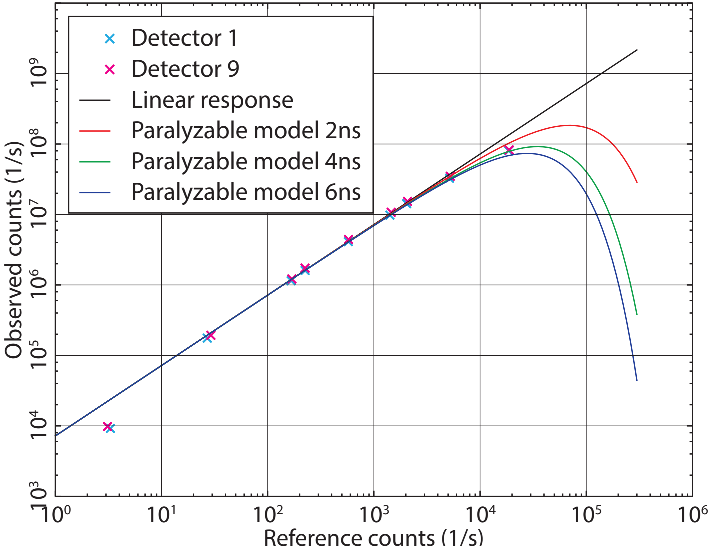


Figure 8.15: Photon count rates as seen by the reference and the XNAP detector, with modelled values for paralyzable detectors with various dead time values.

The observed count rate for the XNAP detector is compared to the reference detector rate (Figure 8.15). A linear ratio between both is given by the black line, whereas three curves for the paralyzable model with dead times of 2 ns, 4 ns and 6 ns are shown in red, green and blue.

The observed count rates for detector 1 and 9 follow the linear response up to the mid-10^7 $1/s$ region. Surpassing that rate, the observed rate falls within the estimation for the paralyzable model with a 4 ns dead time.

8.3 SYNCHROTRON BEAMLINE TESTS

X-ray beam tests at the Synchrotron are made as a refinement to the microfocus source tests, as the beam is much more intense and focused, structured in time, and depending on its source can be tuned

in energy. As the downside, due to its restricted availability, the number of tests are limited. At the beamlines ID 18 and BM 5, measurements by the beamline scientists are carried out under the direction of Pablo Fajardo [12].

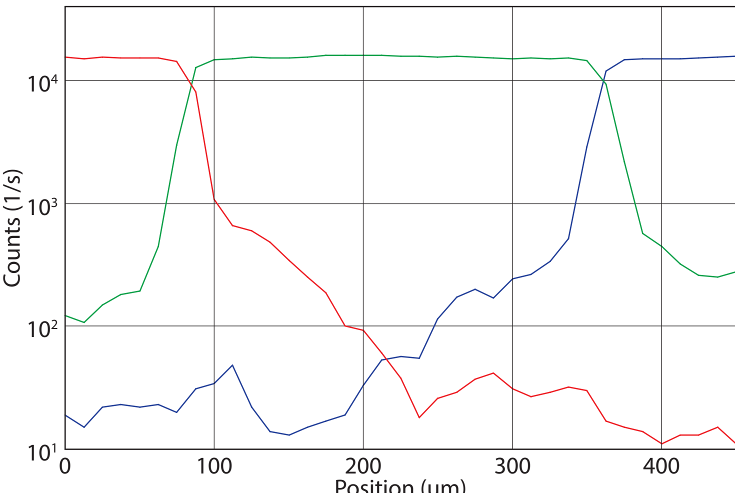


Figure 8.16: Photon count rates depending on X-ray beam position, scanned through the pixel centers. The ID 18 beamline with its focused X-ray spot at 14.4 keV is used. The 280 um pixel width is clearly visible by the count rate plateau (green).

The X-ray focal spot at the ID 18 beamline with a size of 6 um × 13 um is about two orders of magnitude smaller than the area than the microfocus spot size. The charge sharing at the pixel edges of the APD array is therefore analyzed again (Figure 8.16). Compared to the measurement with the microfocus source (Figure 8.14), the pixels are much better separated as the count rate drop off i stronger, due to the smaller beam size.

Contrary to the microfocus X-ray source, the photon beam from the Synchrotron is not continuous in the time domain. Depending on the filling mode, the electron beam circulating in the accelerator is structured in bunches of different intensity and separated by empty intervals, leading to a pulsed X-ray flux.

The time dependent count rates for a 14.4 keV X-ray beam are captured at the end of the long bunch train in *7/8 + 1 filling mode* [7]: The electron bunches are spaced 2.82 ns apart, whereas the first (not shown) and last bunch in the long train is of about 4.4 × the current of the bunches in between. The separate high intensity bunch in the remaining 1/8 timeslice is not shown. Individual bunches can easily be distinguished in the recorded count rates, whereas the more intense flux for the last bunch is also visible (Figure 8.17).

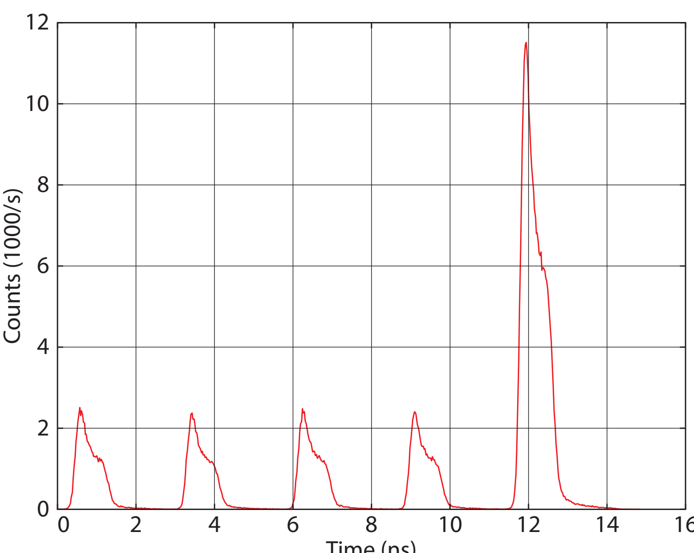


Figure 8.17: Time structure at the end of a bunch train, resolved as the count rates with detector 9: The last four low current bunches and the following bunch of higher current in the long train.

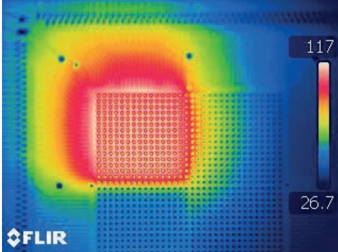
9 FINAL DETECTOR TESTS

Due to limited availability of the final frontend board and the associated readout system, the presented measurements are made with the test system which is designed for electronic characterization without the operation of the sensor. No measures to shield the setup from light or to cool the detector assembly were planned, but had to be subsequently added.

9.1 ASSEMBLY OF THE DETECTOR HEAD

All APA 3.2 ASIC dies are equipped with solder bump balls at the factory, rendering it impossible to connect them with traditional wirebonds. Even for pure electronic tests, the chip must be mounted to an interposer by a reflow process and then wirebonded to the appropriate carrier PCB. The carrier is stacked on top of the frontend board whereas the ASIC faces down, with a heatsink mounted on its back between the two PCBs. As the mounting hole where the heatsink must fit into is about 1 cm × 1 cm, the size of the heatsink is limited.

As a consequence of the small heatsink, even when operating the whole assembly in an air conditioned cabinet, the heat is only partially dissipated from the ASIC.



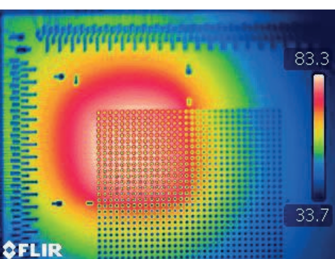


Figure 9.1: Infrared images of one single APA 3.2 ASIC mounted to the HDI-PCB (left) and LTCC (right) interposers, as seen from the sensor side of the interposer.

The surface temperature at the top side of the interposer settles at about 80 °C with the LTCC, whereas using the HDI-PCB, it increases even more, due to less dissipation via the interposer, to about 120 °C (Figure 9.1). While restricted operation of the ASIC is feasible by adjusting the supply and bias voltages, any usage of the sensor is impossible.

In a second attempt, the heat transfer from the ASIC to a much larger heatsink is improved by interposing a small Peltier element between the two, which efficiently extracts the heat out of the chip to the heatsink, placed in the cold air flow of the air conditioned cabinet (Figure 9.2). The thermoelectrical element is connected to a constant current source of 2 A, resulting in an ASIC temperature settling at 20 °C, measured with the integrated diode sensor.

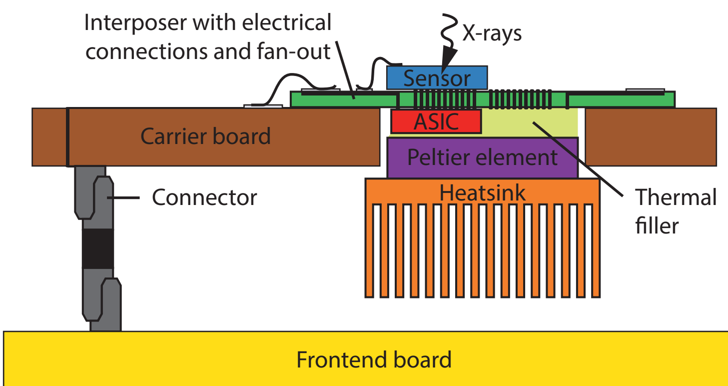


Figure 9.2: Schematic side view of the APA 3.2 carrier PCB, modified for operation with Peltier element and large heatsink. A single quadrant of the interposer is populated with a 256 pixel APD array and one readout ASIC.

The air conditioned cabinet serves not only as the second stage to transfer the heat away from the sensor and ASIC, but also shields the APD from visible light. Hence, the cable feedthrough ports and the window are sealed with light-proof material.

Two different sensor sizes are manufactured: The full 1024 pixel APD array, designed to be connected to four ASICs, and a downscaled 256 pixel array which fits to one single ASIC with all other parameters equal to the large one.

Multiple attempts to mount the sensor to the pre-populated interposer were made by Excelitas. The last trial yielded to assembly 14, built of one HDI-PCB interposer with one APA 3.2 ASIC and a 256 pixel APD array and assembly 15, built of one HDI-PCB interposer with four APA 3.2 ASICs and a 1024 pixel APD array, the very first of the ultimate design. By the limitations of the test setup, only one quadrant of the four can be connected and therefore tested.

9.2 ELECTRONIC TESTS OF THE ASIC

The fast readout register is first operated in slow software controlled mode to verify a working state. Then, the data path latency is cali-

brated by filling the whole register with the header bit set to 1 followed by a single load cycle, which puts a 10 transition in the datapath, and measuring the time to read the 101 pattern back. After successful calibration, the readout is switched to firmware controlled mode with an initial readout clock of 200 MHz.

An automated test routine is designed, similar to the implementation for the APA 2.x ASICs described on page 87, to verify that the interconnection between the readout system and the ASIC works properly and the digital domain of the ASIC is fully operational.

9.2.1 *DACTH transfer function*

The threshold voltage used by the hit signal discriminator is accessible outside of the ASIC. Hence, it allows to measure the combined transfer function of the integrated current DAC chained with the reference TIA, used to convert the reference current to voltage with the same structure that is used for the signal currents.

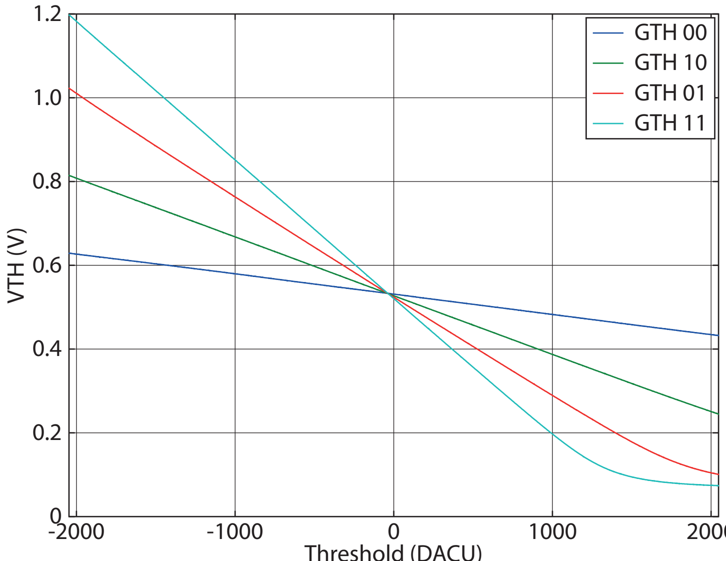


Figure 9.3: Measurement of the DACTH transfer function of assembly 14, with the four *GTH* transimpedance settings.

The transfer function is measured with the ADC on the frontend board, which digitizes the 1.8 V range into 12 bit. With all four transimpedance settings, the transfer function shows good linearity with a slight offset error of -37 DACU (Figure 9.3). With the two high transimpedance settings, the useful DAC range is limited by the minimum V_{DS} voltage required for saturation at the TIA input stage, which is

reached with about 1350 DACU for the second-to-highest, and about 1000 DACU for the highest transimpedance gain.

As there is no possibility of isolated threshold DAC transfer function measurement, the absolute transimpedance gain can only be cross-checked by assuming a unit current of 25 nA per DACU, which gives 1.9 kOhm, 5.6 kOhm, 9.6 kOhm and 13.2 kOhm, hence between 3.5% and 6.8% less than the expected value.

9.2.2 *Analog properties of the pixels*

9.2.2.1 *Potential at pixel inputs*

The input node of each pixel TIA can be routed to the analog test bus by individual programming of the *CONNECT* bits (Figure 6.10). This serves not only to inject test pulses, but also to measure the DC potential for each pixel, giving an indication of ground lift and voltage drop due to the parasitic resistance of the power grid, and also due to variation by the bias current sources.

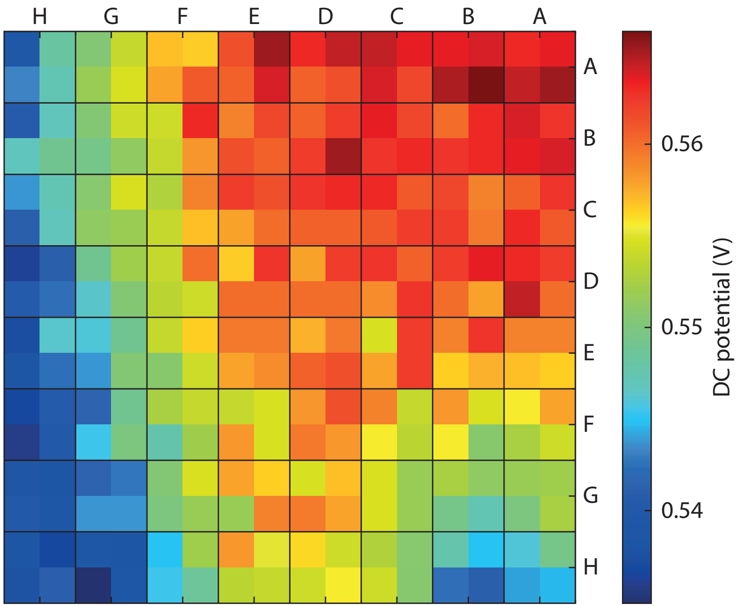


Figure 9.4: Per pixel measurement of the potential at the TIA input nodes of assembly 14 via the test bus.

The potential at the TIA input nodes is measured, for a *DACTIA* bias setting of 1688 DACU, corresponding to 100 uA (Figure 9.4). The pixel block in the upper right edge, where the power supply and bias grid have to bridge the largest distance, exhibits an increased potential by 25 mV. Although the power supplies are located both at the

bottom and the left edge, the potential increase is more pronounced at the bottom than at the left.

9.2.2.2 *Discriminator threshold dispersion and trim*

Like with the smaller prototype system, due to variations in the readout ASIC but also within the sensor, a common threshold without dark hits must be found by adjusting the trim DAC in each pixel. The overall procedure by locating the falling edge of the noise peak and then shifting them to a common level is the same as presented on Page 117, but instead of using the hit counter, the position memory is used. By using a binary search for the coarse location of the switching point and then only scanning through a few DACTH values, this method saves time for the increased number of pixels to process.

The procedure of calculating the *DACTRIML* values for each pixel is done outside the readout system by a dedicated Python script: Based on three threshold scans with −32, 0 and +32 as trim DAC setting for each pixel, the effective shift per DAC bit is calculated and then extrapolated to compensate the offset between the individual threshold and the average threshold for all pixels. As this simple approach does not take any linearity errors of the trim DAC into account, further optimization by hand is necessary.

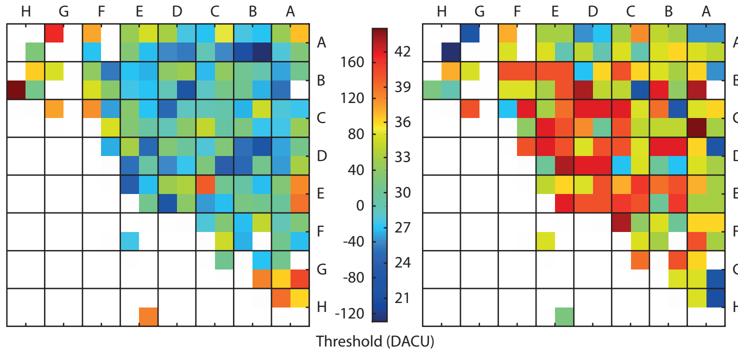


Figure 9.5: Threshold map of the noise edge for the untrimmed (left, in the -120 to 160 DACU range) and trimmed (right, 21 to 42 DACU range) APA 3.2 ASIC. Both scans were recorded with connected and biased APD array and a *DACTRIM* value of 150 using assembly 14. Defective and noisy pixels are hidden.

Threshold trimming is done first to compensate the pure electronic variations of the ASIC with the sensor disconnected, and after its successful application also with connected sensor, to take the pixel to pixel variation of the APD dark current into account (Figure 9.5).

By the first trim attempt, the distribution of threshold settings at the noise edge is reduced from 280 DACU to about 21 DACU (Fig-

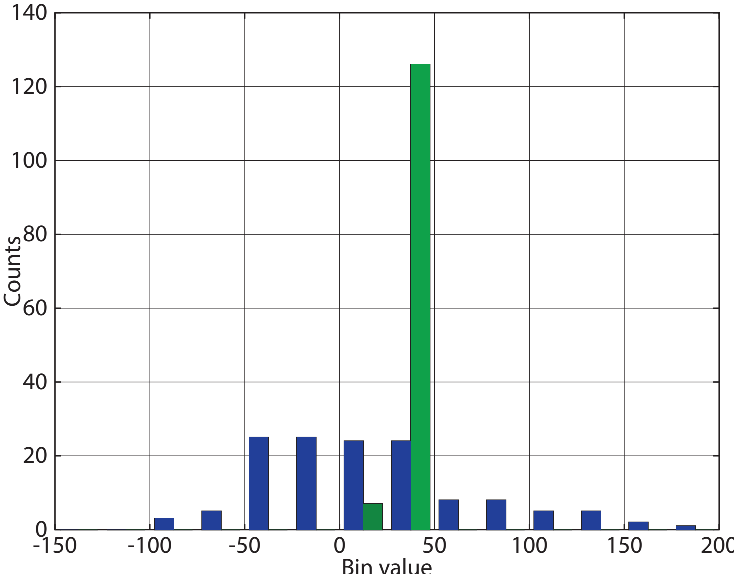


Figure 9.6: Distribution of the noise edge for the untrimmed (blue) and trimmed (green) APA 3.2 ASIC. Both scans were recorded with connected APD array and a *DACTRIM* value of 150 using assembly 14. Defective and noisy pixels are hidden.

ure 9.6). By further reducing the global unit current per trim DAC bit and careful tuning of every pixel, this can be lowered even further, as demonstrated for the APA 2 ASIC.

9.2.2.3 *Threshold scan at the noise peak*

For each pixel, the threshold is scanned around the noise peak to characterize the noise properties. The number of hits due to noise in the frontend and discriminator is recorded by integrating the hits in a time window by the in-pixel counters. For the analysis, the counter values are fitted with a Gaussian distribution. The typical FWHM for the noise peaks (see Figure 8.3) without connected sensor is in the order of 3 DACU at default bias conditions and a TIA gain setting of 11_2.

9.3 ELECTRONIC TESTS OF THE SENSOR

9.3.1 *Biasing the sensor*

The divided anode sensor is biased with positive high voltage, which is generated by an external supply and connected to the sensor via a bond wire at the light entry side. The top guard ring, which must be set to the same voltage as the bias, is connected by a second bond

wire but in parallel to the same source. Hence, the measured leakage current is the sum of the surface leakage current flowing through the guard wire and the bulk leakage.

The bottom guard ring is set to the voltage at which no current flow is measured between the ring and the pixels at the periphery while the bias connection is left floating.

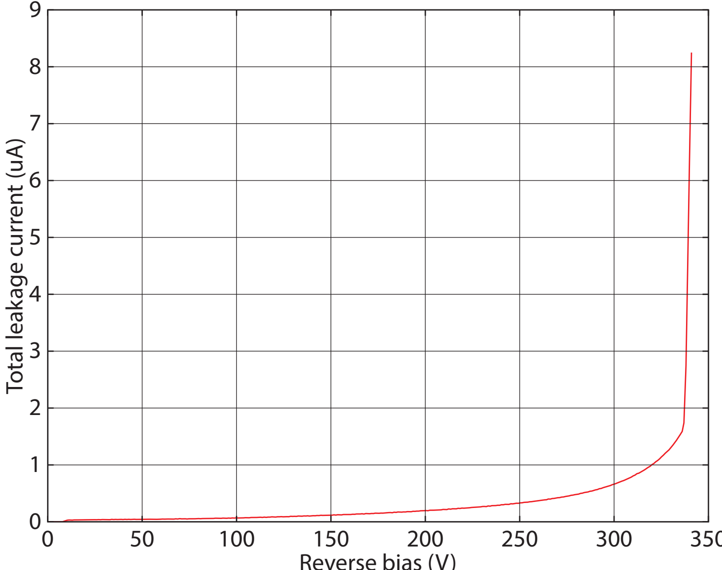


Figure 9.7: Reverse bias dependent total leakage current for the 256 pixel sensor mounted on assembly 14.

The leakage current as well as the breakdown voltage are a function of the Silicon temperature. For assembly 14, the total leakage current is about 1.3 uA at 330 V reverse bias and 20 °C ASIC temperature (Figure 9.7). Above 340 V, the APD junction breaks down with a steep current increase, limited by the power supply at 10 uA.

Biasing the large array of assembly 15 does not result in a stable state: The reverse current oscillates with an amplitude of multiple 1 uA and frequently reaches the current limit of the supply, thus tripping the voltage to ramp down.

9.3.2 *Sensor to ASIC connectivity and inter-pixel resistance*

By measuring the resistance between the sensor electrodes, not only is the connectivity between the ASIC and the sensor validated, but also the sensor structure itself is checked, as the resistance varies depending on the applied reverse bias and field grid voltage: Without applied bias, the p^+-p-p^+ structure shorts all pixels together by the undepleted bulk volume. Under reverse bias, the depletion, extending

from the junction towards the lower doped region where the read-out electrodes are located, isolates the pads by sweeping out charge carriers, leading to a significant increase of the inter-pixel resistance.

The resistance can be further increased by application of a positive potential at the field grid, concentrating charge carriers through the electrostatic field at the center of the electrode pads.

The sensor is mounted last at the interposer, therefore a method to measure the resistance with mounted ASIC is developed: All sensor pixels except the pixel under test are connected to the respective TIA input with a *CONNECT* setting of 1000_2, which applies by the TIAs a constant potential at the sensor. The pixel under test is connected to the test bus and thus accessible at the respective ASIC pad by writing the *CONNECT* setting 0100_2 to the respective pixel configuration register. An external source measurement unit (SMU) instrument forces the potential at the pixel several ± 100 mV around the DC potential while measuring the current flow, which is in the range of a few 10 uA. This measurement is repeated for all pixels, with only one pixel connected to the test bus at a time.

A SMU instrument combines both a remotely programmable voltage or current source with precise current or voltage measurement.

From the recorded data, the differential resistance $R = {}^{\Delta U}/_{\Delta I}$ is calculated, which corresponds to the averaged resistance between the pixel under test and its surrounding pixels.

To improve the robustness of the calculation, instead of taking the numerical difference which is particular sensitive to measurement errors, the voltage and current curves are fitted to a linear model and the resistance calculated from the respective fit parameters.

For some pixels, there is no relation between the current flow and the forced voltage or no current flow at all. These positions are marked white in the map and correspond to open connections between the ASIC and the sensor.

At the periphery of the sensor array, the measured resistance differs slightly from the inner pixels, as the pixel under test is not surrounded by a homogenous structure as at the inner positions of the array.

With assembly 14, a number of 144 pixels show the expected ohmic behavior. The resistances span a range of 1.5 kOhm to 2.6 kOhm in the unbiased state (Figure 9.8). Under reverse bias of 330 V, the range shifts towards higher resistance between 2.2 kOhm and 3.9 kOhm.

For quadrant A of assembly 15, the number of pixels with the expected ohmic behavior is 172. In the unbiased state, the resistance range is from 1.6 kOhm to 2.3 kOhm (Figure 9.9). Under bias, increased values in the range of 2.2 kOhm to 3.2 kOhm are measured. To bias the sensor, a value of 300 V is preset at the power supply. As the APD device is unstable with large oscillation in the dark current (Page 141), the applied voltage heavily fluctuates up to entire breakdown, which makes the measurement data very noisy.

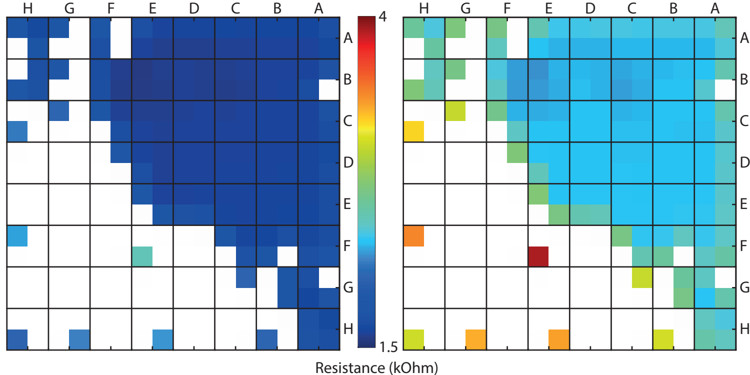


Figure 9.8: Inter-pixel resistance map for the 256 pixel sensor assembly 14. The left is the unbiased state, the right map shows the biased state at 330 V. Both maps share the linear scale between 1.5 kOhm and 4 kOhm.

9.3.3 *Inter-pixel resistance improvement by the field grid*

The improvement of electrical isolation by the electrostatic field of a metal grid surrounding the electrode area is not commonly employed by the sensor manufacturer. Hence, no indication is given for the required potential. With the previously used method of resistance measurement, the field grid effect is determined by sweeping the applied DC voltage from 0 V to 6 V.

With the available interposer assemblies, only for assembly 3, consisting of one APA 3.1 ASIC and one 256 pixel APD array and assembled using a different mounting technique, an effect to the inter-electrode isolation is measured (Figure 9.10). By a different cooling setup, the applied reverse voltage determined by some 10 V below breakdown, is significant higher.

For all others, the field grid connection is either floating in an open state with no effect regardless of any positive or negative voltage applied, or shorted to a number of pixel inputs, which can be measured by a current flow into the particular TIA node by connecting it to the pixel bump pad.

9.3.4 *Threshold scan at the noise peak*

With connected and biased APD array, threshold scans are recorded as previously without the sensor. Due to increased capacitance at the input node by the interconnect and the sensor itself, the width of the fitted noise peaks increases.

The effect of switching the TIA input to the bump pad can be quantified in three sets (Figure 9.11): Pixels with missing connection show

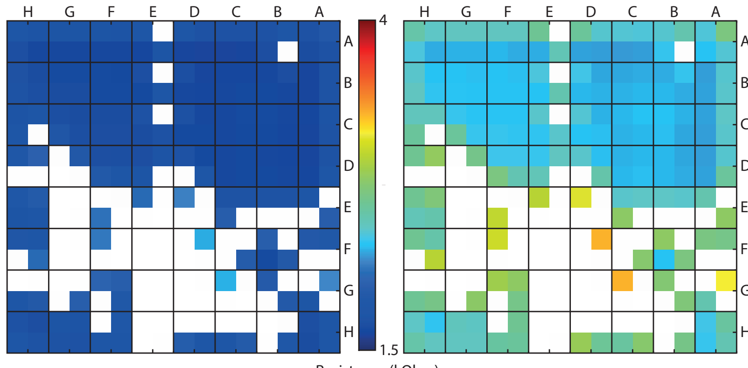


Figure 9.9: Inter-pixel resistance map for quadrant A of the 1k pixel sensor assembly 15. The left is the unbiased state, the right map shows the biased state. Due to oscillation and random breakdown, a fixed bias voltage could not be determined. Both maps share the linear scale between 1.5 kOhm and 4 kOhm.

only little increase in the noise peak width compared to the unconnected state, with a typical FWHM width of 5 DACU or less. Those pixels correlate with the cells failing the inter-pixel resistance measurement (Figure 9.8). The second set consists of those with a FWHM width between 10 DACU and 15 DACU. The third set contains the pixels at the sensor array boundary in the vicinity of the guard ring, which increases, especially marked in the four corners, the width of the noise peak to more than twice the value of inner pixels. The additional noise for these pixels is accounted to the increased capacity by the guard ring structure, but also to fluctuations of the applied guard ring voltage, leading to an additional noise injection.

9.4 DETECTOR TESTS WITH RADIOACTIVE SOURCES

The sensitivity to low energy X-rays is measured by threshold scans with a ^{55}Fe photon source, similar to the procedure done with the 16 pixel detector (Page 119). With the sensor of assembly 14 biased at 330 V and the transimpedance gain set to the highest value, thresholds are adjusted to a common level by using a *DACTRIM* value of 150. The field grid is left floating, as it had no effect on previous measurements to the inter-pixel resistance. The capsule with disintegrating material is placed within 1 cm above the sensor plane, thus a per pixel photon rate in the order of 9000 $1/s$ is expected.

The threshold is scanned, starting left of the noise peak with incrementing *DACTH* setting, while the signal path is enabled for 1 s. In comparison to the number of hits recorded without the source, a minor increase is visible next to the noise peak (Figure 9.12). However, a

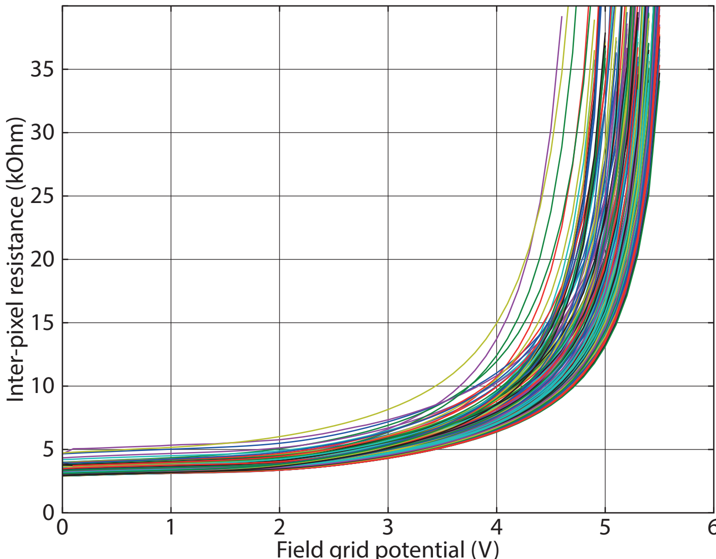


Figure 9.10: Inter-pixel resistance as a function of the field grid potential. Measured with the first-generation assembly 3, biased at 400 V. Defective or unconnected pixels are hidden.

distinct plateau several 100 DACU wide, as observed with the 16 pixel prototype (Figure 8.7), is not detected for different gain settings of the TIA.

Even if the shift of the noise edge is small, a correlation between the *DACTH* offset and the inter-pixel resistance of the respective pixel can be noticed. For pixels of higher resistance, for example BE0, it is more pronounced than for pixels of smaller resistance, for example EB0.

By circuit simulation of two TIA input stages with resistive coupling in the order of 2.5 kOhm (Figure 9.8), it is confirmed that the signal to noise ratio at the discriminator is not sufficient to reliably trigger the counter.

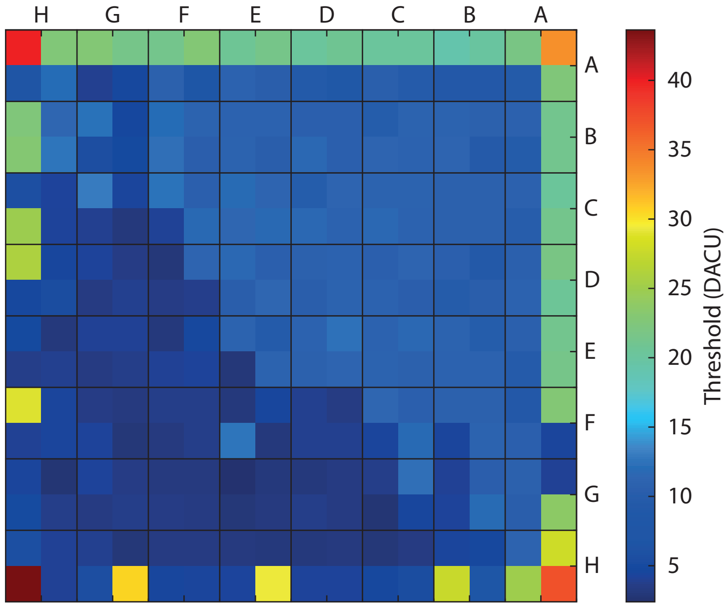


Figure 9.11: Noise peak FWHM for the 256 pixel sensor assembly 14. The sensor is biased at 330 V with all pixel inputs connected to the bump pads.

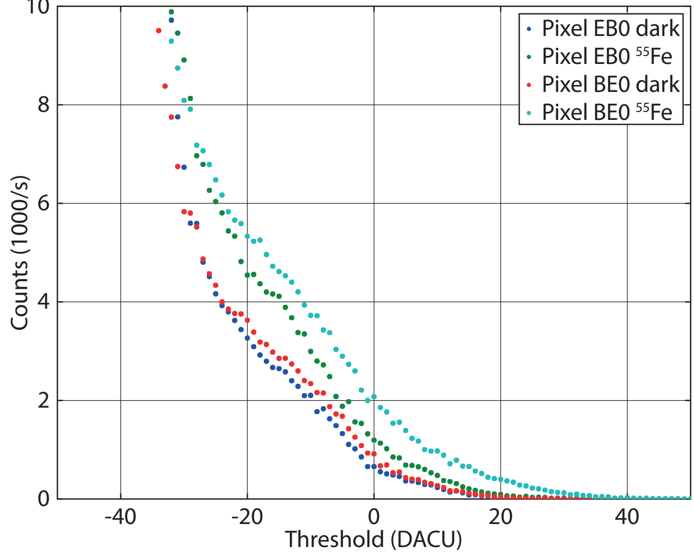


Figure 9.12: Threshold scan for assembly 14 using the 5.9 keV ^{55}Fe source. The noise peak is at the left.

Part IV

CONCLUSION AND OUTLOOK

As a retrospective of the presented work, a summary of the objectives is provided together with an overview of the implementation and measurement results. Further steps towards the commissioning of the detector are given as an outlook together with closing thoughts for subsequent research projects.

10 CONCLUSION

The design and implementation of a multi-channel readout ASIC that is suited for bump-bonding to an APD array is achieved by the second and third generation of APA ASICs. The family of APA 2 ASICs consists of smaller prototypes with 16 readout channels arranged in a 4×4 array, whereas with the APA 3 generation, the number of readout channels is expanded to 256 in a 16×16 array. Most of the frontend characteristics are preserved between the two generations while the readout structure is adapted to handle larger amounts of data.

In order to verify the electronic properties of the different chips, two proper implementations of the FPGA based readout system were developed. While the functionality of the first was limited by the resources of the FPGA board, major effort was put into the second with the availability of recent programmable logic, which allowed to take advantage of the fast digital interface between the ASIC and the following ROC.

The use of an interposer between the sensor and the ASIC, intended to simplify the mounting process, emerged as one of the main challenges, as it requires several hundreds successful bump bondings on both sides of the substrate without damaging neither the ASIC die nor the delicate sensor.

As the quality of the first interposer did not prove satisfactory, an alternative was designed and built as an effort to escape the stalled assembly. Huge benefit from work on interconnection technology by a chair member [27] helped for the development of a reliable assembly process covering the entire ASIC attachment and preparation work for the sensor mounting.

The successful operation of the 16 channel detector was proved at the ESRF: Extensive tests with a special X-ray generator were done to analyze fundamental photon detection properties, while the small beam size allowed to demonstrate the novel position resolving of APD arrays. By the high flux source, photon count rates even exceeding the target of 10^7 $^1/_s$ were demonstrated. Additional measurements at the Synchrotron revealed that the previously determined position sensitivity was deteriorated by the spatially extended beam size, as with the finer spot size the pixel boundaries could be resolved even sharper. The ability to resolve the arrival time of incident photons was demonstrated by successful recording the pulsed structure of the multi-bunch beam.

Numerous sensors for the final detector were consumed through the development of the sensor bumping process, as the supplied

dummy pieces were not applicable due to decomposition of the incompatible metallization. Even with recent attempts, only a few weeks old, the number of attached sensors is low whereas the connection yield is still limited below the expectation by the manufacturer.

Measurements of the inter-pixel resistance for the latest APD arrays proved the effect of depletion to the pixel isolation, while the absolute increase is below the expected value. Using the experimental field grid isolation seemed beneficial, but is limited by interconnection problems to a single assembly, initially rejected for its low number of connected pixels.

The detection of low energy X-rays with the final detector is under study. Very recent measurements have not shown significant count rates for the 5.9 keV photons emitted by a ^{55}Fe source, although electronic testing, adjustment to the biased sensor and detection of visible light photons was successful for a subset of the 256 channels. Little inter-pixel isolation of the employed sensor assembly and therefore a reduced signal to noise ratio is considered the cause.

First tests of the kilopixel sensor resulted in oscillation and random breakdown of the applied reverse bias.

These measurements were performed without final readout electronics and cooling system necessary for a more robust analysis.

11 OUTLOOK

As the remaining parts for the final detector, the frontend and readout boards, the cooling block with its controller PCB and the support chassis, will be completed within the next few months as well as firm- and software code will be written, a more robust setup suited for serious measurements seems to be in the offing.

Still, the quality of the interconnect between the ASIC and the sensor is an open issue, and the ultimate cause for bad connections needs to be solved. As of today, the method of connecting the sensor by conductive glue is challenged for its reliability and might be replaced. Indium bump bonding is considered as an alternative, as it allows to build the electrical connection either at room temperature, at the cost of reduced stability, which must be compensated by an adapted underfill procedure, or using a reflow process but at much lower temperatures than common SAC solder. As carried out with the 16 pixel prototype, the interposer assemblies should be verified by X-ray screening prior to the mounting of heat sink components, as this renders the analysis impossible.

The need for the interposer is questioned a number of times, as it increases the complexity of the assembly process. Direct bump bonding of the sensor array to the ASIC might be possible, at least for small pixel arrays where no adaption of the electrical pitch is necessary. Adequate high voltage isolation and radiation hardness of the ASIC must be considered.

Current research projects demonstrate that the integration of APD arrays together with the entire readout electronics on the same substrate is possible. This could not only ease the detector assembly, but also might be a method for much smaller pixels arranged in dense arrays.

The present APD arrays require further analysis to fully understand the properties of such novel structures. To analyze random breakdown effects, infrared imaging technique is considered beneficial to locate failures in the pixel area and periphery of the device.

Part V

APPENDIX

A DIFFERENTIAL CURRENT MODE LOGIC

A.1 OPERATION PRINCIPLES

Today, most general purpose digital circuits are implemented using the CMOS logic family, where a complementary tuple of PMOS and NMOS transistors is used to pull the output nodes up to the positive supply for the high level and down to ground for the low level. For each input, two transistors are needed, but only one is conducting at a time, so no static current flows through a CMOS gate. While switching, large transient currents proportional to the switching frequency occur. This is the major drawback of the CMOS logic, as it injects noise to sensitive circuits or even causes catastrophic instability. Sometimes, common countermeasures like guard structures and separate supplies for the analog and digital domain are not sufficient and therefore CMOS logic blocks cannot be used.

Differential or symmetric signalling is characterized by using two inputs and two outputs for each logic signal, one P or + branch and one N or - branch, and defining the two logic levels as the relation of the two branches: A logic level *high* is represented by a positive difference between the voltages or currents of the P and N branch, whereas a logic level *low* is represented by a negative difference between the P and N branch. Although the absolute electrical level is irrelevant for the logic representation, it must be kept with certain bounds as the gates only operate in a limited common mode voltage range.

This signalling technique is commonly used in digital systems, for example within the electrical layer of USB and Ethernet, but also found at some special analog applications, like professional audio systems.

The differential logic used within the APA ASIC is based on the differential signalling technique, combined with complementary switching trees. A differential pair is the basic building block of the DCL gate cell, together with a current source shared between both branches and two independent load circuits in each branch (Figure A.1). The differential switch pair steers the current from the NMOS current source either to the P or the N branch, resulting in a voltage drop at one of the two load circuits. The two potentials at the loads are used to control the switching tree at the next gate.

The basic operation principle for this logic family was developed earlier [14], but specially adapted for implementation in this ASIC. The programmable current source at the bottom of each gate as well as the complementary switch trees are built of NMOS gates. The two loads at the top are made each of a PMOS programmable current

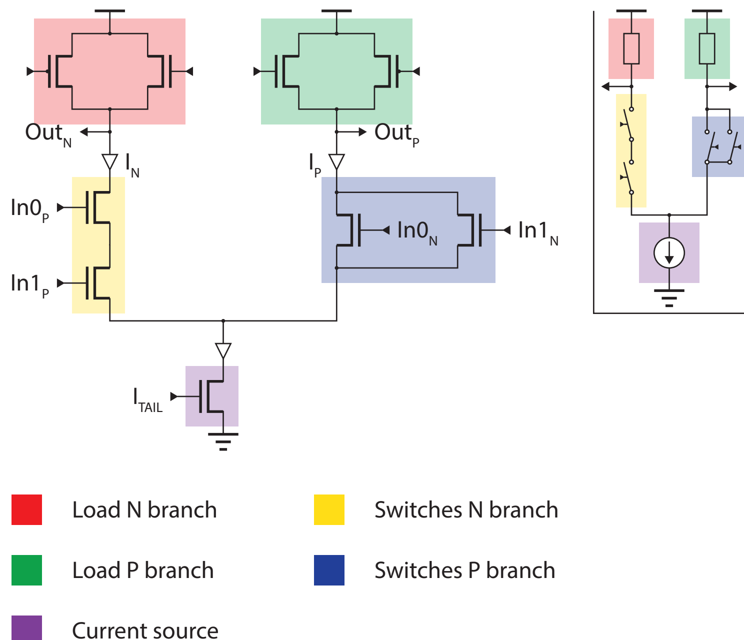


Figure A.1: Schematic circuit of a simple two-input AND gate using DCL technology. A simplified representation is shown in the insert, while the main image shows the transistor-level implementation.

source and a NMOS diode. Operating at a low supply voltage of only 1 V, the switch network can be built of up to three stacked switches, implementing a complex logic function.

The main advantages compared to CMOS logic are constant power consumption, low signal swing, little emission of switching noise, and easy adaption to switching speed requirements. Independent of the logical state and the switching frequency of the gate, the current flow is constant as it is defined by the current source at the bottom and only steered by the switching tree to one of the two branches. External crosstalk overlaid to the output signal cancels out due to the differential signalling technique, therefore the swing can be reduced to the bare minimum by adjusting the current sources and diodes by their respective bias voltages in a wide range or even by reducing the size of the transistors if smaller currents are sufficient.

A.2 CELL LIBRARY

The foundation of the DCL cell library are three basic building blocks, included in each gate (Table A.2, Table A.3): Current source, single switch element and single load, designed in two flavors: The *HP* variant with larger transistors requiring a larger operating current,

which is optimized for transition times in the 1 ns range, and the *LP* variant with smaller transistors requiring less bias current, operating with 10 ns switching times. The latter ones are used where slower operating speed is sufficient and save large amounts of electrical and thermal power.

A.2.1 *DCL current source*

The current source is a single NMOS transistor with its gate connected to the global bias network. The bias network itself distributes the bias voltage across the whole chip, which is derived from a diode connected NMOS transistor, and therefore mirroring the current from a DAC into each DCL gate. The transistor is kept in saturation mode, reducing the influence of the voltage at the switches to the tail current.

A.2.2 *DCL active load*

The load circuit is a combination of a PMOS transistor with its gate connected to the global bias network acting as a current source and a NMOS transistor also connected to the bias network. The voltage at the NMOS is fixed to a value slightly lower than the positive supply voltage, therefore the NMOS is basically operating as a diode. Its very steep voltage-current characteristic precisely limits the low level and contributes to fast transients at the falling edge. The PMOS current source defines the high level and contributes to fast transients at the rising edge. Even when the two components are balanced, the waveform of the rising edge has a larger tail because the PMOS current source leaves saturation and the final pull-up works in linear mode where the current flow is smaller.

A.2.3 *Key electrical and timing properties*

The key electrical parameters for both *HP* and *LP* DCL cells are summarized in Table A.1. Signal levels and switching times are given for the stated nominal bias, although it can be changed by modification of the currents. The switching time is taken from a single buffer cell driving four buffers of the same type connected in parallel at the output.

Property	*HP* variant	*LP* variant
Minimum supply voltage	1 V	1 V
NMOS current source bias	20 uA	2 uA
PMOS current source bias	10 uA	1 uA

NMOS diode bias	VDD – 150 mV	VDD - 300 mV
Common mode voltage	735 mv	735 mV
Differential swing	±265 mV	±265 mV
Switching time (10%-90%, FO4)	770 ps	2.8 ns

Table A.1: Key electrical and timing parameters for the DCL gates.

A.2.4 *Virtuoso Cell library*

Name	Contents	Description
DCL_HP_Frame	Layout	Basic structure of logic gate: Source, two loads, substrate/well contacts, metal wiring
DCL_HP_Load	Schematic	PMOS current source and NMOS diode load
DCL_HP_Source	Schematic	NMOS current source
DCL_HP_Switch	Schematic Layout	Single switch element
DCL_HP_Switch_Double	Layout	Space-optimized series connected double switch
DCL_HP_And2	Schematic 4 Layouts	Two input conjunction
DCL_HP_Buffer	Schematic 2 Layouts	Buffer
DCL_HP_Demux2	Schematic 3 Layouts	One input, two outputs demultiplexer
DCL_HP_Flipflop_SR	Schematic 3 Layouts	Single bit memory element with set and reset input
DCL_HP_Flipflop_T	Schematic 2 Layouts	Single bit memory element with toggle input
DCL_HP_Latch	Schematic Layout	Single bit memory element with load input
DCL_HP_Mux2	Schematic 2 Layouts	Two inputs, one output multiplexer
DCL_HP_Mux2_Latch	Schematic Layout	Single bit memory element with load and two selectable data inputs
DCL_HP_Or2	Schematic 6 Layouts	Two input disjunction

DCL_HP_Shiftreg	Schematic 3 Layouts	Dual stage single bit memory element with two selectable data inputs
Or_Line_Driver	Schematic 2 Layouts	Buffer with 10x drive strength

Table A.2: Building blocks and gates in the *HP* variant differential cell library.

Name	Contents	Description
DCL_LP_Frame	Layout	Basic structure of logic gate: Source, two loads, substrate/well contacts, metal wiring
DCL_LP_Load	Schematic	PMOS current source and NMOS diode load
DCL_LP_Source	Schematic	NMOS current source
DCL_LP_Switch	Schematic Layout	Single switch element
DCL_LP_Switch_Double	Layout	Space-optimized series connected double switch
DCL_LP_And2	Schematic Layout	Two input conjunction
DCL_LP_Buffer	Schematic 3 Layouts	Buffer
DCL_LP_Flipflop_SR	Schematic Layout	Single bit memory element with set and reset input
DCL_LP_Flipflop_T	Schematic 3 Layouts	Single bit memory element with toggle input
DCL_LP_Latch	Schematic Layout	Single bit memory element with load input
DCL_LP_Mux2	Schematic Layout	Two inputs, one output multiplexer
DCL_LP_Mux2_Latch	Schematic Layout	Single bit memory element with load and two selectable data inputs
DCL_LP_Mux2_Shiftreg	Schematic 3 Layouts	Dual stage single bit memory element with two selectable data inputs

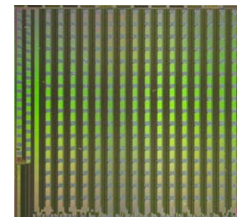
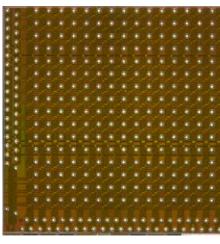
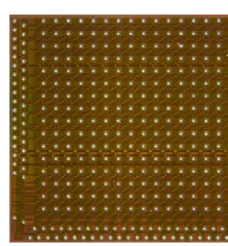
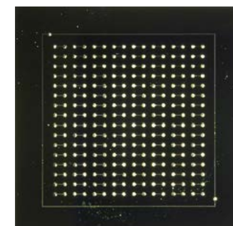
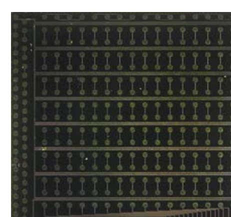
DCL_LP_Or2	Schematic Layout	Two input disjunction

Table A.3: Building blocks and gates in the *LP* variant differential cell library.

B

TABLE OF DESIGNED SILICON DEVICES

Name	Die photograph	Description and major improvements over previous chips
APA 1.1		Four channel TIA test structure with a die size of 1.5 mm × 1.5 mm.
APA 1.2		Four channel test structure with simple DCL based digital hit processing and threshold DAC.
APA 2		16 channel prototype with full digital hit processing, serial readout and revised threshold DAC. Pads compatible with wire and bump bonding. The die size is 1.5 mm × 3 mm.
APA 2.1		16 channel prototype with modified power routing, monitor bus and digital output pads.

APA 3		256 channel chip with linear hit combination. The die size is 5 mm × 5 mm.
APA 3.1		256 channel chip with entire reworked layout for factory bumping. Tree distribution and combination of time critical signals. Addition of self-gate and self-veto mechanisms. Pads compatible with bump bonding only.
APA 3.2		256 channel chip with modified power routing and small changes in the digital hit processing.
APD dummy		Silicon dummy of the APD array with snake structures for bumping tests. Manufactured by Excelitas.
APA 3 dummy		Silicon dummy for the ASIC with snake structures for bumping tests and heating resistor. Manufactured by Excelitas.

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