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Systems-on-Chip (SoC) for applications in High-Energy Physics

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Zusammenfassung

Systems on Chip (SoC) für Hochenergiephysik-Anwendungen

In Hinblick auf die Time Projection Chamber (TPC) für den geplanten Linear Collider (LCTPC) wurde ein neuer, anwendungsspezifischer integrierter Schaltkreis für das Front-End entwickelt: der 16-Kanal Super-Altro Prototyp. Aufgrund der geringen verfügbaren Fläche von $1\times4\text{mm}^2$ pro Kanal wurde der Chip als kompaktes integriertes System realisiert, welches der Vorverstärkung der analogen Eingangssignale, der Impulsformung, der 10-bit Analog-Digital-Wandlung, sowie der digitalen Signalverarbeitung dient. Geeignete Designtechniken wurden verwendet, um die Kopplung zwischen Analog- und Digitalteilen des Systems zu verringern. Der Schaltkreis ist für das Bunch-Train-Regime des Linear Colliders optimiert; die Stromaufnahme ist durch die Verwendung von Power-Pulsing stark reduziert worden.
Die durchgeführten Tests zeigen ein Rauschen von lediglich 316 Elektronen, sowie die Funktionalität der Power-Pulsing Technik. Der Super-Altro kann sowohl für das Auslesen von Gasdetektoren mit Drahtkammern, als auch mit GEMs oder MicroMegas, eingesetzt werden.

Diese Dissertation behandelt unter anderem auch Analog-Digital-Wandler (ADC), geeignet für Front-End Systeme in der Hochenergiephysik. Simulationen zeigen die Realisierbarkeit von 12-bit 100MHz Pipeline ADCs, in einer 130nm CMOS Technologie.

Abstract

Systems on Chip (SoC) for applications in High-Energy Physics

In view of the Time Projection Chamber for the future Linear Collider (LCTPC), a new front-end Application-Specific Integrated Circuit has been developed: the 16 channels Super-Altro Demonstrator. Given the small pad area of $1\times4\text{mm}^2$, the chip is a compact integrated system, including signal preamplification/shaping, 10-bit analog-to-digital conversion and digital signal processing. Adequate design techniques were used to reduce noise coupling between analog and digital parts of the system. The bunch train structure of the linear collider is exploited by the introduction of power pulsing features in the design, which result in a significant reduction of the power consumption. The tests carried out show noise as low as 316 electrons and effectiveness of the power pulsing approach. Super-Altro can be used for studies of gaseous detector readout with classical wire chambers as well as modern GEMs and MicroMegas.

This thesis also studies Analog-to-Digital Converters (ADC) suitable for integration in High-Energy Physics front-end systems. Simulations show the feasibility of a 12-bit 100MHz pipeline ADC in a 130nm CMOS technology.

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Chapter 1

Introduction

1.1 The present: CERN, the LHC, and ALICE

The European Organization for Nuclear Research (CERN) [Ce] operates the world's most powerful particle accelerator, the Large Hadron Collider (LHC) [LHC]. This facility accelerates and collides alternatively protons, currently at an energy of 3.5TeV (design energy 7TeV), or lead ions, currently at 2.76TeV per nucleon (design energy 5.5TeV/nucleon); the bunch crossing is synchronized with the global clock, at a frequency of 40MHz.

A Large Ion Collider Experiment (ALICE) [AL1] is located at one of the collision points along the LHC, and targets primarily Pb-Pb collisions. The main tracking and particle identification sub-detector of ALICE is the Time-Projection Chamber (TPC). The TPC has the shape of a cylinder, whose axis is on the trajectory of the LHC beam. In the middle of the cylinder, perpendicular to the beam, a central electrode is kept at a high positive voltage; particles resulting from collisions ionize the gas in the TPC along their trajectory, which is bent by a magnetic field; the ionization produces electrons, which drift towards one of the end caps of the TPC, under the action of a uniform electric field generated by the high voltage electrode. Detecting the arrival area of these electrons on the endplate gives information on the trajectory of the ionizing particle; thus, the momentum of the particle can be inferred. At the same time, the amount of charge collected gives a measure of the energy loss per unit length (called dE/dx). A combination of momentum and dE/dx measurements is used to identify the initial particle originating from the collision.

1.1.1 Wire chambers, GEMs, MicroMegas

The charge generated through ionization by the initial particle is small and must be amplified and detected. Three main architectures are used for this scope: Multi-Wire Proportional Chamber (MWPC), Gas Electron Multiplier (GEM), Micro-MEsh GAs detector (MicroMega).
The readout of the ALICE TPC is based on MWPC.

Using MWPC, electrons drift towards the end cap, where they find anode wires [Ro, 3]. The electrical field in the proximity of the anodes increases, and avalanches occurs; therefore, the initial electrons produce many more electron-ion pairs. The TPC end cap is populated by metal pads where these charges induce an electrical signal. Electrons reach immediately the anode wires, while ions are much slower; a gating grid is added between the drift volume and the anode wires to prevent the backflow of ions towards the central electrode. The positive signal induced on the pads has a fast rise and a slow fall (tenths of microseconds), due to the slower ions (ion tail). Each pad is connected with a dedicated Front-End Electronics module (FEE), for the amplification, filtering and measurement of the signal; in ALICE, the connection is done with kapton cables, and the FEE is composed of Pre-Amplifier Shaping Amplifier (PASA) and ALICE TPC ReadOut chip (ALTRO). The minimum pad size of the ALICE TPC is 7mm×4.5mm.

The Gas Electron Multiplier [Sa] is a thin polymer foil, coated on both sides with metal. Holes with diameter of the order of 70μm are regularly distributed across the foil. A voltage difference, applied between the two metal coatings, creates an intense electric field in the hole regions. Electrons arriving from the drift region are multiplied by the avalanche, which occurs due to the high electric field. Afterwards, the resulting electrons continue their trip towards the pads on the end cap of the detector.
Signals produced by GEMs are only due to electrons; therefore they are negative, fast and do not present any ion tail; the duration of signals is in the order of a few tenths nanoseconds.

MicroMegas [CD] replace the anode wires of a MWPC with a metallic mesh, which is held by insulating pillars at a very short distance (in the order of 100μm) from the pad plane. A high voltage applied to the mesh creates an amplification region between the pad plane and the mesh itself; electrons resulting from the avalanche travel towards the pads, while the corresponding ions are collected by the mesh.
Signals produced with MicroMegas have a fast rise due to electrons and a tail due to ions. The important point is that, given the short distances, the collection of ions is much quicker than in MWPC, in the order of 100ns.

1.2 Front-end architectures for detectors

There exist three main categories of chips for the read-out of signals produced by detectors:

Binary chips: each analog signal is converted in a digital line by a discriminator. This architecture has low power consumption and produces a simple digital output.

Analog memories: the analog signal is sampled on capacitors, and later sent off-chip to an external ADC.

Digital Signal Processing (DSP) chips: the analog signal is sampled, and each sample is converted in a digital word. This allows further processing of the signal in the digital domain. Zero suppression reduces the amount of data and discards non relevant data.

Some examples of existing chips, using the three different architectures, are given in the next paragraphs.

1.2.1 Binary chips

In a binary chip like VFAT2 [A1], an analog front-end amplifies and shapes the signals coming from a detector. The resulting pulse is fed to a discriminator, which performs the comparison with an analog threshold and generates a digital output. A "fast OR" of the outputs of all 128 channels generates a trigger output. Moreover, VFAT2 offers a tracking function, where it tells which channels have been hit after a given trigger.

Another interesting binary chip is the TimePix [Ll]. The architecture of the front-end is based on a preamplifier followed by a discriminator; the digital output of the discriminator can be used in various operating modes. In particular, in Time-Over-Threshold (TOT) mode, a clocked counter measures the time duration of the signal being above threshold; this is proportional to the amplitude of the analog pulse, and, therefore, to the detected charge.

1.2.2 Analog memories

The PACE3 assembly [A2] is an example of analog memory. Pre-amplifier and shaper are followed by a Switched-Capacitor (SC) circuit with a set of 192 capacitors, which constitute an analog memory. At each clock period, a sample of the analog signal is stored on a different capacitor. After receipt of an external trigger, three capacitors are protected from overwriting; in this

way, the analog memory saves the three consecutive samples which follow the trigger and contain the pulse. Later, the saved samples are buffered off-chip, where they are digitized by an external converter. The three samples allow some processing, e.g. baseline subtraction.

Another example of analog memory is N-XYTER [BB]: after a pre-amplifier, the signal is delivered to a fast shaper and to a slow shaper in parallel. Following the fast shaper, a discriminator generates a trigger, which provides digital information on the arrival time of the pulse. The slow shaper is followed by a peak detector, instead; the peak detector holds the maximum amplitude of the pulse, which is then stored across a capacitor in an analog memory.
With this architecture, N-XYTER is capable of self-triggering, and provides as outputs the sampled analog voltage together with the corresponding digital time stamp; an off-chip Analog-to-Digital Converter (ADC) is needed to digitize the analog sample.

1.2.3 DSP chips

The ALTRO chip [Bl], is an example of DSP-based architecture, and it was initially developed for the Alice TPC. Each channel contains a 10bit pipelined ADC and a data processor, while another chip is needed to perform pre-amplification and shaping of the signal coming from the detector. A clock up to 20MHz triggers the sampling in the ADC; the samples are passed in a pipelined fashion to the data processor. The DSP part of the chip is similar to that of the Super-Altro, described in section 4.5; it allows correction of non-idealities or perturbations in the signal, e.g., systematic offsets or patterns, distortions of the pulse shape, temperature drifts, supply voltage variations. The large amount of data produced is reduced with a digital threshold for zero suppression: only the pulses exceeding the threshold are saved in the memories, and later read-out.

1.2.4 Comparison between the three front-end architectures

Binary chips have small size and power consumption per channel. They are particularly appealing when the detector is quiet and perturbations are small. They are not capable of filtering fluctuations of the baseline. With a negative fluctuation, the discriminator may not detect signals smaller than the fluctuation; with a positive fluctuation, the discriminator may be triggered even when no real signal is present. A solution is to increase the threshold;

the discriminator would not detect fake events, but it would also miss many more real events.
If the system noise is considerable, it will also trigger the discriminator; a solution is, again, to increase the threshold, which leads to the loss of many small signals which do not exceed the threshold.
A purely binary readout provides only hit information, and no information on the signal amplitude, which is required in TPC applications. Therefore, it is not used in TPCs.

Analog memories allow some digital signal processing (PACE3) and self-triggering (N-XYTER). Their disadvantages are the maximum time they can hold the information and the difficulty in implementing zero suppression before storing the information in the memories.

The advantage of DSP-based chips is that they can filter fluctuations of the baseline; therefore, the threshold for the zero suppression can be kept at a minimum, allowing the detection of the smallest signals. Moreover, DSP chips can correct distortions of the signals due, for example, to long ion tails; this results in better measurements when pile-up of pulses occurs.
The drawback of DSP chips is that large power is needed for the ADCs and for the data processor.

1.3 The future: FAIR, ILC/CLIC

In the close future, a new accelerator facility will enter operation at the GSI Helmholtzzentrum für Schwerionenforschung GmbH (GSI) [GSI]. The Facility for Antiproton and Ion Research in Europe GmbH (FAIR) [Fa] will host the Compressed Baryonic Matter experiment (CBM) [CBM].

At the same time, new accelerators are under investigation for the post-LHC era. The International Linear Collider (ILC) [IL] and the Compact LInear Collider (CLIC) [CL] are two proposals of linear electron-positron colliders. In both cases, bunches of particles are grouped together in trains; in ILC, each train is about 900μs long, and trains are repeated every 200ms (5Hz); in CLIC, the train duration is 156ns, and the train repetition rate is 50Hz (20ms). Therefore, front-end electronics do not need to be continuously powered, as in the LHC; a duty cycle can be applied to turn on the electronics only during collisions, thus dramatically reducing the power consumption.
For ILC/CLIC there are two detector proposals: International Large Detector (ILD) [ILD] and Silicon Detector (SiD) [SiD]. The ILD includes a TPC, which is being developed in a collaboration named Time Projection Chamber for a future Linear Collider (LCTPC) [LT]; the pad size in the LCTPC is 1mm$\times$4mm.

1.3.1 Motivation for this work

The trend in microelectronics goes towards the implementation of Systems on Chip (SoC), where different analog and digital components are integrated on the same silicon die. SoC are compact solutions, which usually need less space and less power than multi-chip systems; they also reduce assembly costs, while improving reliability. Technology scaling decreases the area of digital circuitry; therefore, modern designs tend to increase the intelligence in a chip in terms of digital functionalities. The main drawback with SoC is signal integrity: coupling mechanisms between signals of different nature endanger the quality of analog signals.

In view of the experiments planned for the next years, a new SoC is under conceptual development. The signal coming from the detector is pre-amplified, and sent to two shapers in parallel, with different shaping times; gain, polarity and shaping times are programmable by the user. The fast shaper feeds a discriminator, which provides trigger and timing information. This front-end is replicated for many channels (32, 64 or 128). Upon reception of a trigger, the output of the corresponding slow shaper is routed to a peak detector, and the voltage held by the peak detector is converted to digital by an ADC.
Depending on the expected occupancy of the detector, an average number of channels will receive events in the same time interval, while the other channels will not register any relevant data. Therefore, a small set of peak detectors is sufficient; when an event is detected by the discriminator of a channel, the output of the slow shaper of that channel is routed to the next available peak detector. The same argument is applied to ADCs, which are a much smaller number than the channels.
The result is a self-triggering SoC, which outputs digital information on pulse heights with the corresponding time stamps. Some control logic implements the routing of analog signals from many channels to smaller sets of peak detectors and ADCs. The minimum numbers of channels, peak detectors and ADCs depend on the specific application, as well as the requirements of each functional block. The ADC, for example, can be designed with a high resolution, and can be maskable, so that the application selects the appropriate number of bits. Also the design sampling frequency can be high; in case a lower frequency is required, either the ADCs are clocked with the appropriate frequency, or some of them are masked, so that they do not consume power, while the operating ADCs provide the necessary speed.
For this thesis, the chosen ADC specifications are 12 bits of resolution and a maximum sampling frequency of 100MHz. These are demanding values, which push the design to the limits of the technology in use.

In view of the future Linear Collider (ILC/CLIC), the development of a new DSP-type front-end chip has started. The basis is the ALTRO chip, evolving into a complete SoC: the Super-Altro. Given the small 1mm×4mm pads of the LCTPC, the ALTRO chipset, which includes the pre-amplifier in a separate chip, occupies too much area; a compact solution is required, where pre-amplifiers are integrated with ADCs and digital processor; this also implies that the technology used must be modern, in order to benefit from the small transistor size. Additionally, new designs have to take advantage of the bunch timing of the Linear Collider, including power pulsing features which decrease dramatically the power consumption of the system. Ongoing testing activities on GEMs and MicroMegas are also potential applications of the new SoC; in this case, a required additional feature is versatility, so that the chip can be used in a variety of configurations according to the specific needs.
The 16 channels Super-Altro Demonstrator (S-Altro) addresses all these requirements. The pre-amplifier and shaper is programmable in terms of gain, polarity and shaping time. The detected charge spans from a Minimum Ionizing Particle (MIP) of 4.8fC (30000 electrons) to a maximum of 30MIP (900k electrons); a good Signal-to-Noise Ratio (SNR) is achieved with noise lower than 1000 electrons, which sets a requirement for the pre-amplifier. An ADC with a resolution of 10 bits ($2^{10} = 1024$) fits best the dynamic range between the acceptable noise and the maximum charge. The minimum shaping time of 30ns sets a condition on the maximum sampling frequency of the ADC: in order to collect at least one sample during the rising edge of the pulse, the ADC must operate up to 40MHz. Another important aspect of the design is that the communication protocol of the S-Altro must be compatible with the ALTRO protocol, so that existing systems developed for ALTRO can be easily updated to the new front-end.

1.3.2 Summary of the thesis

The work presented in this thesis is based on a modern 130nm CMOS technology. An understanding of the devices and effects present when designing with such technology is necessary. **Chapter 2** reviews the theory of operation of transistors in modern technologies.

A feasibility study of the ADC introduced in the previous paragraph has been done, and is described in **chapter 3**:

- Specifications are resolution of 12 bits and maximum sampling frequency of 100MHz.

- Low power consumption is essential, to allow integration of many channels.
- General models for the design of pipelined ADCs are studied.
- Good design of the main amplifier is the bottleneck of this ADC. The amplifier has been designed in schematic, using the small-signal models reported in **appendix A**, and simulation results are shown.

The work on ADCs was carried out at the Physikalisches Institut in Heidelberg and was preparatory for the work on the Super-Altro, which was carried out at CERN in Geneva.

The design of the Super-Altro 16 channels Demonstrator is reported in **chapter 4**. Main challenges and innovations in the Super-Altro include:

- System integration decreases the area.
- Having analog together with so much digital functionalities on the same silicon die, with acceptable performance degradation is a major challenge.
- Measuring the noise is one of the main goals, which should tell whether it is possible to continue in this path of system integration for future High-Energy Physics (HEP) experiments.
- With the bunch train schemes of future linear colliders, power pulsing features are now vitally important. This project must include such features, and provide estimations of attainable reductions of the power consumption.

The Pre-Amplifier and Shaping Amplifier (PASA) are based on the PCA16 prototype, developed as a follow-up to PhD Thesis [Tr], while the ADC is based on the prototype presented in [FS]. The DSP is similar to ALTRO, with some modifications explained in [GB]. The main points of the work carried out are:

- The PCA16 was designed with different technology options, not suitable for Super-Altro. Therefore the design has been modified and fully re-simulated before integration in the Super-Altro; more robust ESD protections have been included.
- The biasing of the ADC was conceived for power pulsing (external biasing resistor). The ADC prototype was completed with the error correction logic.

- A clock tree for the whole chip has been designed, and testability features have been added to the chip. The much simplified idea behind the clock tree is depicted in **appendix C**.
- The full system has been assembled, with careful choice of the chip floorplan.
- Special attention was paid to techniques to reduce noise coupling and crosstalk in the system.
- A Verilog-AMS model of the full chain has been written, allowing simulations to validate the integration of all blocks. This type of simulations may assume primary importance in the future, due to the complexity of advanced analog and digital functionalities in SoC. It is also useful for performance evaluations of complex systems, including detectors and any external component. The models are included in **appendix B**.

After submission of the Super-Altro, a test plan has been prepared. A test board has been designed, capable of handling all the possible operations of the chip. The details of the test board are reported in **chapter 5**, together with the results of the tests which have been carried out on the chip.

Chapter 6 draws the conclusions of this thesis, and gives a glimpse into the future of SoC for HEP applications.

Chapter 2

Technological overview

This chapter summarizes the knowledge about semiconductor devices needed in order to understand the topics discussed in this thesis. This theory can be found in several textbooks; in general the discussion in this chapter follows references [Ba] and [MK].

2.1 The MOS transistor

Semiconductor foundries implement complicated processes, based on lithography, to manufacture chips. In the technology available for this thesis, the minimum component size which can be drawn is 130nm. The semiconductive material (silicon) becomes n-doped with the addition of donor atoms, or p-doped with the addition of acceptor atoms. In most chip manufacturing technologies, the substrate is a p-type material; for technological reasons, it follows that the structure of n-channel transistors is simpler than in the p-channel case. Therefore, the discussion refers to the NMOS transistor; nevertheless, these considerations and equations are valid in an analogous way also for the PMOS transistor, leading to symmetrical results.

The Metal-Oxide-Semiconductor system (MOS) is the basic structure to build up the transistors in our technology. A silicon oxide layer is grown on the substrate and some conductive material is deposited on the oxide; in the past, this material was aluminum, which has been later replaced by polisilicon. The thickness of the oxide is of the order of a few tens of Angstrom. This basic system can be seen as a capacitor, whose plates are the metal and the substrate; the oxide is considered in most cases as an ideal insulator, although some small leakage may exist, as explained in paragraph 2.3.2.

A voltage applied to the metal induces some variations in the substrate, namely a positive voltage attracts electrons on the surface; when the voltage

applied to the metal is high enough (higher than the substrate voltage plus the threshold voltage, discussed later), a channel is formed by the electrons in the substrate in the surface region close to the interface between substrate and oxide. This condition is called inversion, because the holes which populate the p-type substrate are replaced by electrons.

In the case of PMOS devices, an N-well is created in the p-type substrate; therefore, if the voltage applied to the metal is low enough, a holes inversion layer is formed on the surface, and the system can be described as in the NMOS case.

The region of the substrate which lies under the metal is called channel and at its both sides a heavily-doped n+ diffusion is present. This diffusion allows the creation of contacts with the metal layer that can be deposited on its top. At this point, the system with three metal terminals is a NMOS transistor and the metal above the channel is the gate; of the remaining two contacts, the one held at the lower voltage is called source and the other one drain. The system is depicted in figure 2.1.

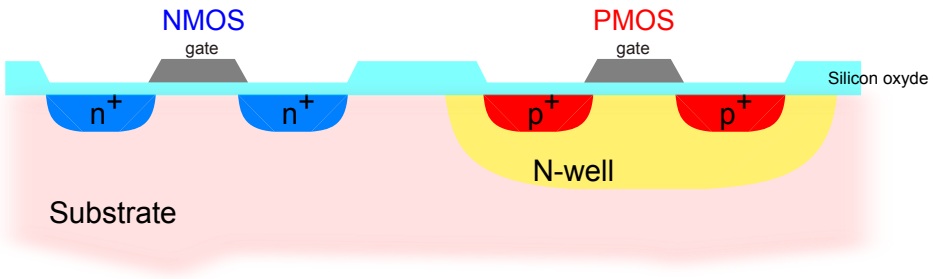

Figure 2.1: Section of an NMOS on the left. The PMOS on the right is the complement of the NMOS, built inside an N-well.

Two design parameters, namely the voltage of the body and the voltage of the source of the transistor, affect the threshold voltage. With the available technology, PMOS transistors have an n-well which can be biased independently; usually this well is tied to the source, such that the source-body voltage difference is zero. On the other hand, NMOS transistors are built on the substrate, which means that their bodies are tied to the substrate, which is held at ground potential; in this case, the source-body voltage V_{SB} can be greater than 0V. Electrons in the inversion layer are attracted towards the source, which is at a higher potential than the body; therefore, they depopulate the channel, and a voltage higher than the nominal threshold voltage is needed at the gate in order to keep the channel inverted. This phenomenon is known as body effect.

Characteristic curves of transistors in different operating regions are plotted in figure 2.2.
With the help of the threshold voltage, we can define three regions of operation for a MOS transistors according to its gate-to-source and drain-to-source voltages V_{GS} and V_{DS}.

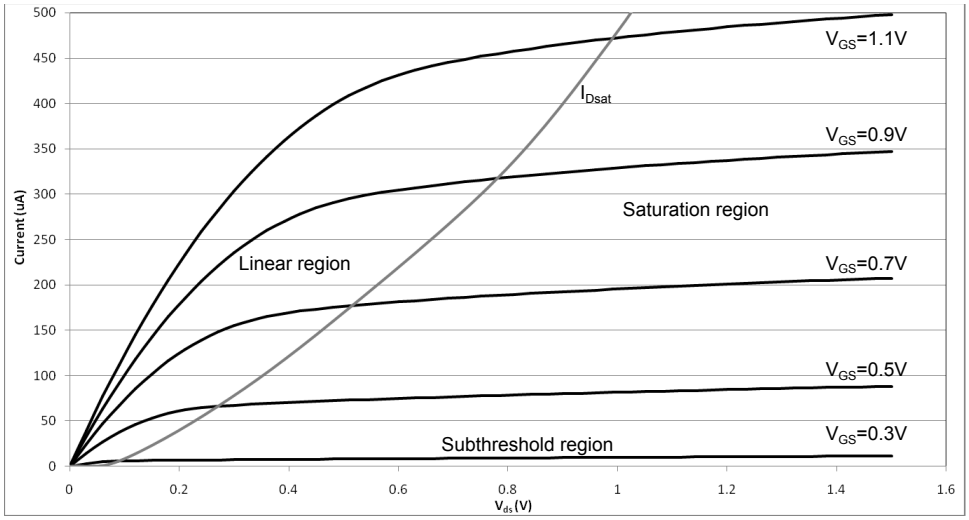

Figure 2.2: Channel currents of an NMOS, as a function of the drain-source voltage V_{DS}, simulated for different values of V_{GS} [Ba, 6.3.2].

Linear region: V_{GS} is greater than the threshold voltage V_{th}; the channel is in inversion, therefore the system behaves like a resistor and the current is proportional to V_{DS}.

Saturation region: V_{GS} is greater than the threshold voltage, and V_{DS} is greater than the overdrive voltage $V_{OV} = V_{GS} - V_{th}$; under this condition, the high voltage at the drain attracts many electrons from the inversion layer, and the channel is said to be pinched off. The current flowing along the channel is almost constant and independent of the drain voltage.

Subthreshold region: V_{GS} is smaller than V_{th}, the channel is not inverted and nominally no current flow takes place. Still, the short-channel effect of subthreshold current may happen, as explained in 2.3.2.

In digital circuits, the allowed voltage levels are 0V and the supply voltage V_{DD}. Therefore, in the standard case of the digital inverter, each transistor is

either in the OFF state (gate voltage $V_G = 0$) or in the ON state ($V_G = V_{DD}$, $V_{DS} = 0$).

In analog circuits, transistors are usually biased in the saturation region, which provides high gain (in figure 2.2, the curves in this region are closest to horizontal). In the case of transistors used as switches, the gate voltage V_G is either 0V (open switch) or V_{DD} with V_{DS} close to 0V (closed switch).

Before proceeding with the equations which describe the behaviour of MOS transistors in the different operating conditions, some parameters have to be defined.

When an electric field is applied across the channel of the transistor, the carriers reach a certain velocity. The ratio between velocity and electric field is defined as mobility [Ba, 5]:

$$\mu_{n,p} = \frac{Average\,velocity\,(cm/s)}{Electric\,field\,(V/cm)} \tag{2.1}$$

The mobility of electrons μ_n is about three times larger than the mobility of holes μ_p.

Indicating the oxide capacitance per unit area as C'_{ox}, the transconductance parameter $KP_{n,p}$ can be defined as [Ba, 6.3.1]:

$$KP_{n,p} = \mu_{n,p} \cdot C'_{ox} \tag{2.2}$$

The β parameter, which includes not only technological constants, but also design parameters, is defined by:

$$\beta = KP \cdot \frac{W}{L}$$

where W and L are the width and length of the MOS transistor.

With these definitions, the characteristic equations of MOS transistors can be written [Ba, 6]. The NMOS case is considered here; for PMOS transistors, the equations are complementary (V_{GS} and V_{DS} have opposite sign).

In the linear region, the current flowing through the inverted channel of the transistor is [Ba, 6.3.1]:

$$I_D = KP \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_{th})\, V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.3}$$

In the saturation region, the current through the transistor is given by [Ba, 6.3.2]:

$$I_D = \frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 \tag{2.4}$$

An improvement can be applied to this equation by taking into account an effect called channel length modulation. Equation 2.4 can be rewritten in the form:

$$I_D = \frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2 \left[1 + \lambda \left(V_{DS} - V_{DSsat}\right)\right] \tag{2.5}$$

where V_{DSsat} is the V_{DS} at the border between linear and saturation region for a given V_{GS}, and is equal to the overdrive voltage V_{OV}. The current when $V_{DS} = V_{DSsat}$ is symbolized as I_{Dsat}. The channel length modulation parameter λ originates from the fact that part of the geometrical length of the channel is occupied by the width of the depletion layer (this effect is called channel length modulation).

From these equations, called square-law equations, the channel resistance and the transconductance of the transistor in the saturation region can be derived. By definition, the transconductance g_m is the derivative of the current with respect to the gate-to-source voltage; from equation 2.4, it follows that [Ba, 9.1.2]:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = KP \cdot \frac{W}{L} \cdot (V_{GS} - V_{th}) = \frac{2I_D}{V_{OV}} \tag{2.6}$$

If we derive the same equation with respect to the drain-to-source voltage V_{DS}, we obtain the resistance of the channel r_0:

$$r_0 = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\lambda I_{Dsat}} \tag{2.7}$$

The symbol of an NMOS transistor is depicted in figure 2.3, together with the associated junction capacitances.

Reference [Ba, 6.1] reports the equations to calculate these capacitances in the saturation region:

- The drain-to-bulk C_{db} and source-to-bulk C_{sb} capacitances are constants (they depend on the technology).
- The gate-to-bulk C_{gb} capacitance is proportional to the channel length L.
- The gate-to-drain C_{gd} capacitance is proportional to the channel width W.
- The gate-to-source C_{gs} capacitance is proportional to the channel area WL.

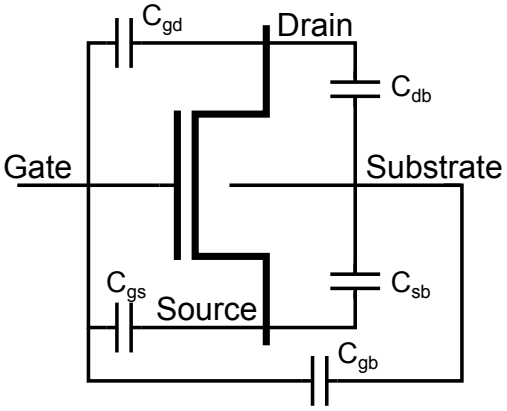

Figure 2.3: The parasitic capacitances in an NMOS [Ba, 6.1].

Therefore, designers have control over the parasitic capacitances through the design parameters W and L.

In a comparison between an NMOS and a PMOS transistor with the same drain current and overdrive (giving the same transconductance), the NMOS transistor is smaller, because of the larger mobility μ_n (equations 2.2-2.5); as a consequence, the parasitic capacitances C_{gd} and C_{gs} of the NMOS are roughly three times smaller than in the PMOS case.

Other necessary components available in semiconductor technologies are resistors and capacitors. Resistors can be built in several different ways, for example as strip of polichristalline silicon on the oxide, or as narrow metal paths. The designer chooses the width and length of these structures according to the desired resistance.
Capacitors are created, for example, as two horizontal metal plates separated by an insulating dielectric (MIM=Metal-Insulator-Metal structures) and the capacitance depends on the area of the plates. In MIM capacitors, the bottom plate forms also a parasitic capacitor with the substrate, and therefore sees a slightly bigger capacitance than the top plate.

Every technology provides also a stack of electrically isolated metal layers, that designers use to interconnect the devices.

2.2 Noise

Resistors and MOS transistors are affected by noise; equations exist for the spectral density of white thermal noise and flicker 1/f noise. In the next equations, f is the frequency, k is the Boltzmann's constant and T is the

absolute temperature.

In MOS transistors, noise can be represented as concentrated on a single voltage source, placed at the gate of the transistor. When the transistor is in the saturation region, the power spectral density of this source has a thermal white component and a flicker one given, respectively, by [JM, 4.3]:

$$v_{ts}^2(f) = \frac{8kT}{3g_m} \qquad (V^2/Hz) \tag{2.8}$$

$$v_{fs}^2(f) = \frac{K_F}{C'_{ox}WL \cdot f} \qquad (V^2/Hz) \tag{2.9}$$

where K_F is a constant depending on the technology and on the device, while C'_{ox} is the gate capacitance per unit area.

Thermal noise in a resistor is represented by a voltage source in series with it or equivalently, by a current source in parallel; their power spectral densities are, respectively [JM, 4.3]:

$$v_n^2(f) = 4kTR \qquad (V^2/Hz) \tag{2.10}$$

$$i_n^2(f) = \frac{4kT}{R} \qquad (A^2/Hz) \tag{2.11}$$

where R is the value of the resistance.

2.3 Short-channel

In modern technologies, transistors can be fabricated smaller and smaller. As a consequence, some effects, named short-channel effects arise; these are described in the literature, for example in [MK, 9, 10] and [Ba, 6, 9].

2.3.1 Effects and model

Source-drain charge sharing, drain-induced barrier lowering and punchthrough are short-channel effects that decrease the threshold voltage of the transistor; here they are briefly addressed, based on [MK, 9.2] and [Ba, 6.5.2].

Source-drain charge sharing refers to the fact that the width of the depletion region surrounding the drain and source is not negligible any more, in comparison with the short length of the channel.

Drain-Induced Barrier Lowering (DIBL) is a decrease of the threshold voltage, due to the electrons which are attracted in the channel by the positive voltage of the drain. As a consequence, the output (channel) resistance of

short-channel transistors decreases, and this leads to the unwanted effect of a lower gain of the amplifiers.

Punchthrough is a short between the drain and source depletion regions, which can happen in the bulk of the transistor (far from the oxide-silicon interface).

Mobility degradation originates from the fact that, as the transistor sizes are reduced, also the oxide thickness is reduced. Therefore, the electrical field across the oxide, between gate and channel, increases; this results in a decrease of the mobility of electrons in the channel.

When the electric field across the channel, between source and drain, is large, the velocity of carriers does not increase any more as expected from equation 2.1, and a saturation velocity v_{sat} is reached.

Equation 2.4 is rewritten for short-channel transistors [MK, 9.2]:

$$I_{Dsat} = WC'_{ox} \cdot (V_{GS} - V_{th} - V_{DSsat}) \cdot v_{sat} \tag{2.12}$$

where V_{DSsat} is not equal any more to the overdrive voltage, as it was in the long-channel case. Equation 2.6 becomes [Ba, 9.2.1]:

$$g_m = v_{sat} \cdot C'_{ox} \cdot W \tag{2.13}$$

2.3.2 Leakage currents

Leakage currents are present in every transistor, but they become more relevant as the dimensions decrease. A brief overview follows, based on [MK, 10.2, 10.3] and [Ba, 6.5.2].

Electrons with a sufficiently high kinetic energy (hot electrons) can hit the atoms and ionize them (impact ionization); this results in new free electron-hole pairs. The resulting electron feels the positive voltage of the drain. The resulting hole, instead, travels in the substrate and, by doing this, contributes to the leakage current I_{sub}.

The gate is not actually a perfect insulator, and some current can flow through it. The gate leakage current is generated by channel hot electrons (they gain an energy higher than the potential barrier between silicon and gate), drain-avalanche hot carriers (carriers generated by impact ionization events) and cold electrons (which pass through the oxide by means of the tunnel effect).

If the field across the oxide becomes too large, the oxide breaks down; therefore, the voltage difference between gate and channel must be kept below very few Volts in modern technologies.

When the gate-to-source voltage of a transistor is less than its threshold voltage, the device is in subthreshold region [Ba, 6.4.2]. Still, some current

flows through it, with an exponential dependency on $V_{GS} - V_{th}$. In short-channel technologies the threshold voltage is, generally speaking, lower, and therefore the unwanted subthreshold current is higher.

Chapter 3

Analog-to-digital converter

3.1 Specifications

In any analog-to-digital converter, a sample of an analog signal is converted in a digital code; the numerical value of the digital code is proportional to the amplitude of the analog sample. The input signal will be differential in order to reject common-mode noise; each half-signal will vary between a maximum V_{ref+} and a minimum V_{ref-}. Therefore, the differential signal will assume positive or negative values, between a maximum $+V_{ref}$ and a minimum $-V_{ref}$, defined as $V_{ref} = V_{ref+} - V_{ref-}$; the differential voltage span V_{pp} (peak-to-peak voltage) is equal to $2V_{ref}$.

The number of bits N, which makes up the digital word, determines the resolution of the converter.

The minimum signal which can be discerned is called Least Significant Bit (LSB), and is expressed by:

$$LSB = \frac{V_{pp}}{2^N} \tag{3.1}$$

In the next paragraphs, this simplified model will be expanded, including several parameters which are helpful in expressing the performance of ADCs. The literature offers several sources of information about ADC parameters; in general here the discussion follows references [JM, 11] and [Ba, 28].

3.1.1 Quantization error

ADCs convert an analog signal, which is by definition continuous, in a digital representation, which is discrete. The higher the number of bits, the more precise this conversion is. Anyhow, an infinite number of bits is not realistic, and therefore there will always be a loss of resolution when a digitization takes

place. The difference between an analog signal and its digital approximation can be calculated statistically, and its root mean square is the quantization error (quantization noise).

It has been shown [Ba, 28.5] that the dependency of the quantization error Q_{error} on the LSB, and therefore (equation 3.1) on the number of bits is:

$$Q_{error} = \frac{LSB}{\sqrt{12}} = \frac{V_{pp}}{2^N} \cdot \frac{1}{\sqrt{12}} \tag{3.2}$$

3.1.2 Transfer curve of an ADC and non-linearity

ADC transfer curves can be plotted. They typically look like figure 3.1.

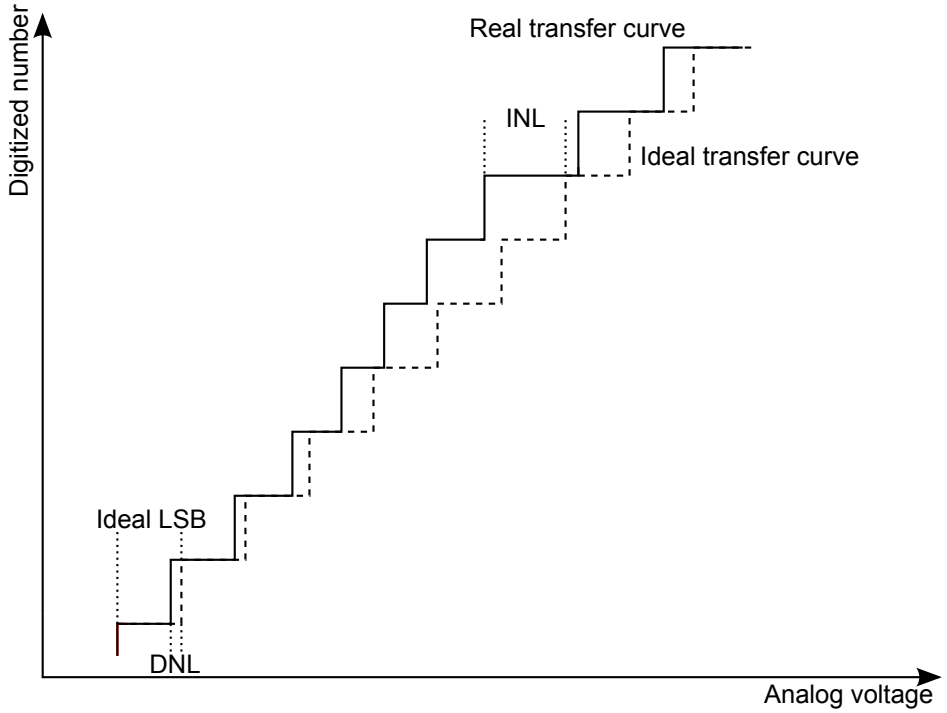

Figure 3.1: Example of transfer function of an ADC, with graphical explanation of DNL and INL.

The figure shows an ideal transfer curve (dotted), where all steps are equal. The continuous line represents the transfer curve for a real ADC, affected by non-linearities.

An horizontal step represents the range of analog voltage which is discretized in the same digital code. Ideally, this analog range would be given

by the LSB; the difference between the ideal value and the real one, expressed in LSBs, is called Differential Non-Linearity (DNL). The DNL for a converter can be plotted as a function of the analog input, or also given as a number; in this last case, only the maximum value of the DNL is given, as a worst-case.

One important property of ADCs is the monotonicity of their transfer curve. In order to ensure it, designers typically try to keep the DNL smaller than 1LSB, because if this condition is satisfied, then the ADC is monotonic [JM, 11.5].

Figure 3.1 also shows that, due to the accumulation of the DNL of many digital steps, the real transfer curve may, at, some point, be significantly far from the ideal one. The maximum displacement between each real vertical steps and its corresponding ideal vertical step is defined as Integral Non-Linearity (INL).

The discussion so far voluntarily neglected the fact that the transfer curve may not start from the origin and may have a slope different from the ideal $2^N/V_{pp}$. The first effect is an offset, while the second one is called gain error. They are subtracted from the transfer curve before calculating DNL and INL.

3.1.3 Signal-to-noise ratio

The concept of quantization error (or noise) has been introduced. Even in the case of an ideal ADC, without additional noise sources, this noise is present and limits the maximum Signal-to-Noise Ratio that the converter can achieve.

The maximum analog input signal is V_{pp}; a sinusoidal signal with this amplitude carries a power of $V_{pp}^2/8$. Therefore, with the presence of the quantization noise, using equation 3.2, the maximum Signal-to-Noise Ratio (SNR) achievable is given by:

$$SNR_{max} = \frac{V_{pp}^2}{8} \cdot \left(\frac{\sqrt{12} \cdot 2^N}{V_{pp}} \right)^2 = 1.5 \cdot 2^{2N}$$

Usually, the SNR is expressed in dB, and the espression for the ideal SNR becomes [Ba, 28.5]:

$$SNR_{max} = 6.02 \cdot N + 1.76 \ (dB) \tag{3.3}$$

In real ADCs, also other random noise sources are present; they add quadratically to the quantization error. Therefore, they degrade the SNR, which becomes lower than SNR_{max}. Equation 3.3 can be used also to express

the resolution in terms of a measured SNR; this is the Effective Number Of Bits (ENOB):

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{3.4}$$

Sometimes, also the SIgnal-to-Noise and Distortion ratio (SINAD) is used instead of the SNR, to include the effect of the harmonic distortion of the ADC, and give a more accurate value of the ENOB.

3.2 ADC architectures

A number of architectures have been developed for ADCs to meet a broad range of application requirements. In this section an overview will be given, following [JM, 13, 14] and [Ba, 29.2], focusing on the architectures which suit best our needs. The last paragraph motivates the choice of the pipeline architecture for the ADC object of this thesis.

Among the most popular ADC architectures, the focus is on flash, pipeline, delta-sigma. Additionally, successive approximation ADCs, which will be mentioned in section 6.2, are briefly introduced.

3.2.1 Successive Approximation Register

In Successive Approximation Register (SAR) converters [JM, 13.2], a threshold is set at the middle of the maximum voltage range, and the input signal is compared to this threshold; after this first comparison, the voltage range which contains the input signal is divided into two more equal sub-ranges by a second threshold. The input signal is then compared to this second threshold to determine in which sub-range it lies. After that, a third sub-range is determined by a third threshold, a new comparison has place and so on for a number of cycles N equal to the number of bits of resolution required.

3.2.2 Flash

As explained in [JM, 13.4], the flash architecture generates at the same time all the $2^N - 1$ fixed thresholds corresponding to the number of digital steps. These thresholds are created by a resistive divider from a given reference voltage. Per each threshold, a comparator determines whether the signal is larger or smaller than the threshold.

It is clear that, as the number of bits N increases, the number of comparators increases exponentially. Apart from the complexity, this is bad also because many comparators add up to a large capacitance seen by the input

signal. As a consequence, for high resolution, flash converters become slow or require more power.

Most of all, the accuracy of each comparator and of the voltage divider must be good (offset lower than 0.5LSB) in order to avoid errors in the output code. Some digital correction techniques are available to relax the requirement on the comparator offset and on the resistor mismatch, to 4LSB.

3.2.3 Pipeline

Pipeline is an evolution of two-step ADCs. Two-step ADCs, described in [JM, 13.5] and [Ba, 29.2.2], are used to compensate the drawbacks of flash ADCs: they have less capacitive load and they need fewer comparators with relaxed resolution and offset requirements.

The main idea of two-step ADCs is to split a big flash converter into two smaller blocks, each one being itself a flash ADC. The first block resolves the most significant N_1 bits and passes the residue (difference between the analog signal and the voltage equivalent to the N_1-bit code digitized so far) through a DAC to an amplifier with a gain of 2^{N_1} and then to the second block, which resolves the remaining $N_2 = N - N_1$ least significant bits.

This principle can be extended to more than two blocks, each one resolving a lower number of bits, the so-called pipeline architecture [JM, 13.8] [Ba, 29.2.3]. In the extreme case, N stages can be implemented, with 1-bit of resolution each.

Pipeline requires a much lower number of comparators than flash ADCs, especially for higher resolutions. Moreover, the offset requirements of comparators is much more relaxed. On the other side, the implementation of the gain stages to generate the residue is a challenge. Pipeline also has a long latency, because N clock cycles after the signal sampling are needed before the digital output is ready.

3.2.4 Delta-Sigma (Oversampling)

Delta-Sigma converters, explained in [JM, 14] and [Ba, 29.2.6], are different from the other converter architectures covered so far. In fact, SAR, flash and pipeline ADCs belong to the category of Nyquist rate converters because, according to the Nyquist sampling theorem, their sampling frequency S_R must be higher than the Nyquist frequency, defined as twice the maximum frequency component of the signal that they have to digitize.

In Delta-Sigma converters, the signal is converted at low resolution and at a much higher frequency than its bandwidth. The ratio between conversion frequency and Nyquist frequency, called OverSampling Ratio (OSR),

can be in the order of hundreds (typically powers of 2 are implemented for convenience).
The advantage of oversampling is that the power spectrum of the quantization noise is spread over a frequency range up to the conversion frequency, while the power spectrum of the input signal is limited to its bandwidth. Therefore, a digital low-pass filter can keep the signal power at low frequencies, and filter out much of the quantization noise at high frequencies.

Often the core of a Delta-Sigma converter is a 1-bit ADC (one single comparator). The comparator converts the same sampled signal many times (at the high conversion frequency) and produces a series of bits. A digital decimation filter reduces the number of 1-bit samples and yields a higher resolution digital output, updated at the (low) sampling frequency.

The main drawback is the low speed: typically, the sampling frequency is of the same order as the maximum signal frequency, while the clock (conversion) frequency is a few hundred times (OSR) the sampling frequency. This means that, even with a clock frequency in the GHz region, the sampling frequency will be in the MHz region.

3.2.5 Architecture choice

The requirements for the ADC object of this thesis are up to 100MHz clock frequency and resolution up to 12 bits.

Delta-Sigma ADCs are used when high resolution, for example 16 bits, is required. The price to pay for this resolution is their low speed.

Flash architecture requires $2^N - 1$ comparators: 4095 for a 12-bit converter. In the present case, their offset should be as low as $200\mu V$ (without digital correction), which is a very harsh requirement. Flash converters are fast and have no latency, but they are typically found with a resolution of 8 bits.

Pipeline ADCs require only $2N$ comparators in the case of 1.5 bits of resolution per pipeline stage. The offset of the comparator is not critical because some digital correction techniques can compensate any error as long as the offset is lower than $200mV$ in the present application (section 3.3). The main disadvantage is that the signal has to travel through all the stages. This travel, controlled by the clock, introduces a latency between the sampling instant of the analog signal and the instant when the corresponding digital code is available at the output. Anyhow, for applications in High-Energy Physics (HEP), latency is usually not an issue, because the digitized data will be further processed, thus delayed.

In the trade-off between speed and resolution, pipeline ADCs are the solution which suits best the needs of the present application, as shown in

[AB] and [FS].

In the next sections, a deeper description of the pipelined architecture will be given in order to understand better its theory of operation and its implementation.

3.3 The pipeline architecture

Pipeline ADCs are widely described in the literature, for example in [Su].

The operating principle of a 1bit/stage pipeline ADC is shown in figure 3.2. The input signal to be digitized is compared with a fixed threshold.

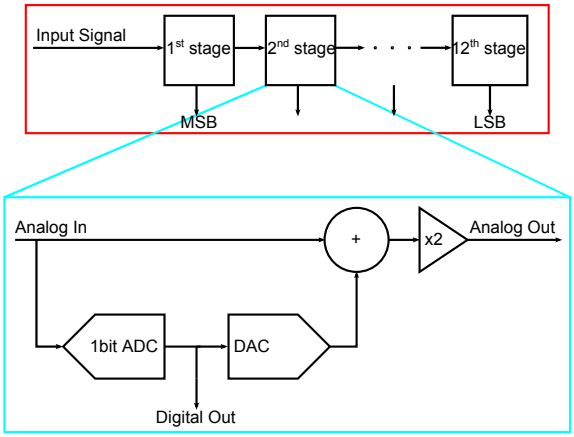

Figure 3.2: Diagram of a pipelined ADC with a resolution of 1bit per stage.

According to the result of the comparison, the residue is calculated as the voltage difference between the signal and the threshold. The residue is then multiplied by two and passed over to the next stage. The algorithm adds one bit of resolution at each stage, in order to figure out which of the 2^N bins contains the signal. From the diagram, one can see the reason why each stage is named Multiplying Digital-to-Analog Converter (MDAC).

With this straightforward implementation, the offset of the comparators must be very small (less than half LSB, or 390μV), otherwise an error in the comparison in the first stages leads to a wrong digital output. This is practically not implementable.

A more robust implementation exists, which uses some redundancy in order to correct for offsets or possible errors of the comparators. In this architecture, each MDAC has 1.5bit of resolution. In each pipeline stage, two comparators compare the input voltage with two thresholds $\pm V_{ref}/4$.

The ideal transfer function of this MDAC, plotted in figure 3.3, is:

$$V_{out} = 2 \cdot V_{in} + D \cdot V_{ref} \tag{3.5}$$

where D corresponds to the decision of the comparators, and can assume values 0, 1, -1.

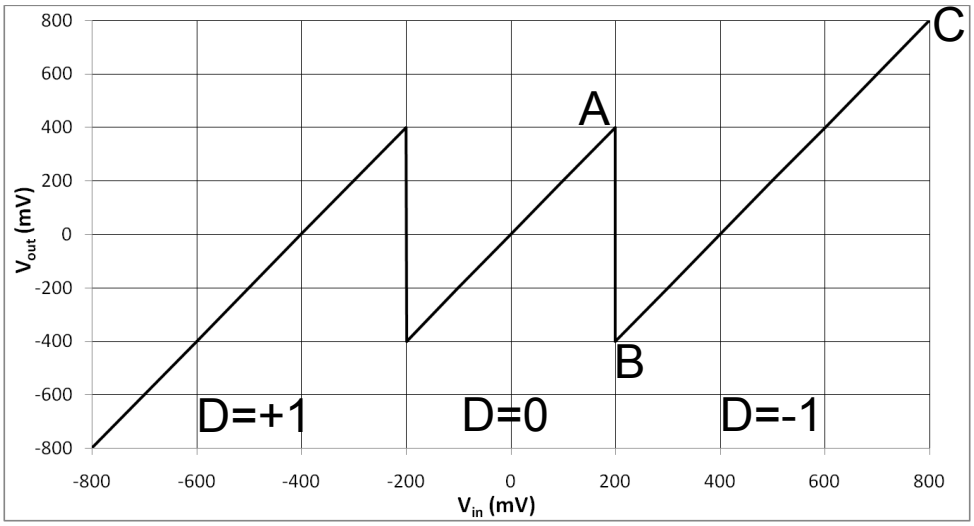

Figure 3.3: Plot of the ideal transfer function of a 1.5bit MDAC. When $V_{in} < -200mV$, $D = +1$; when $-200mV < V_{in} < +200mV$, $D = 0$; when $V_{in} > 200mV$, $D = -1$.

In this implementation, the important requirement is that a signal in the upper range ($\geq +V_{ref}/4$) must not be classified in the lower range ($\leq -V_{ref}/4$) and vice versa. Any other error can be corrected, as will be detailed in section 4.4, where the digital error correction is explained. Therefore, the requirement for the comparator offset is relaxed to $< V_{ref}/4$ (200mV).

Figure 3.4 is a diagram of the pipeline ADC, including the digital error correction. It shows also that the first stage acts as a Sample-and-Hold (S/H), as well. The spectrum of the input signal is known, and lays in the baseband of the ADC; therefore, the skew between the comparison instant and the sampling instant is not crucial, and there is no need of a dedicated, noisy and power-hungry S/H.

The commonly-used figure of merit fom for this type of ADC is the energy required for the effective conversion of an analog signal in one bit:

$$fom = \frac{energy}{conversion} = \frac{power}{2^{ENOB} \times S_R} \tag{3.6}$$

where S_R is the sampling rate of the ADC.

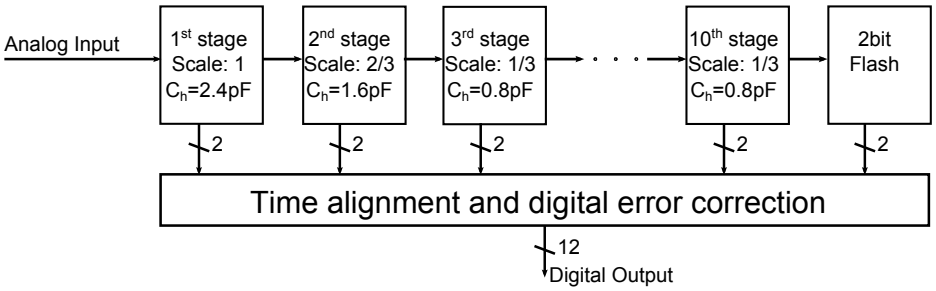

Figure 3.4: Diagram of a 1.5bit/stage pipeline ADC, including stage scaling and digital error correction, which will be explained in section 4.4 [AB].

3.3.1 Multiplying Digital-to-Analog Converter

Figure 3.5 shows how a 1.5bit MDAC is implemented. The implementation must be differential for noise reasons. Two comparators decide in which range the input voltage lays, by comparing it with the two thresholds $\pm V_{ref}/4$; two reference voltages, V_{ref+} and V_{ref-}, define $V_{ref} = V_{ref+} - V_{ref-}$.
The digital outputs of the comparators are latched and then passed to the decoding logic, which controls the switches in order to provide the correct voltage output to be subtracted to the input signal by the amplifier.
The amplifier uses Switched Capacitors (SC) to implement the multiplication by a factor of 2. The input signal is first sampled on capacitors C_s and C_f; bottom-plate sampling must be used to reduce the charge injection dependency on the input signal [Ba, 25.2.1]. In the next phase, C_f is flipped and becomes the feedback capacitor of the amplifier. The clock ϕ_{1d} is a delayed copy of ϕ_1; clocks ϕ_1/ϕ_{1d} and ϕ_2 are non-overlapping.

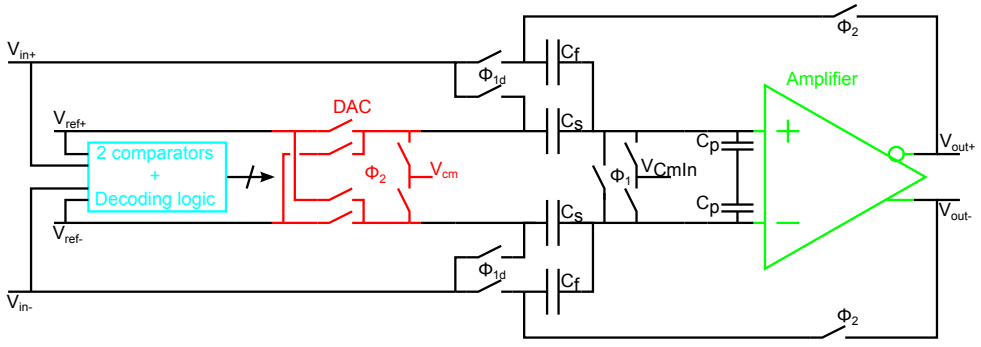

Figure 3.5: Scheme of one pipeline stage, with reference voltages V_{ref+} and V_{ref-} and V_{cm}, and clocks ϕ_1, ϕ_{1d} and ϕ_2 [AB].

Figure 3.5 suggests that equation 3.5 represents an ideal transfer function; a more realistic transfer function is given by 3.7 (derived from [AB]):

$$v_o(t) = \frac{\beta A_o}{1+\beta A_o} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \cdot \left[\left(1 + \frac{C_s}{C_f}\right) \cdot V_{in} + D \cdot \frac{C_s}{C_f} \cdot V_{ref}\right] \qquad (3.7)$$

The first term gives the effect of the finite open-loop gain, which depends on the feedback factor β and on the open-loop DC gain of the amplifier A_o. The exponential term corresponds to the finite bandwidth of the amplifier, with time constant τ. The term with capacitances C_s and C_f quantifies the influence of the mismatch between capacitors.

In the next pages, these aspects will be analysed and applied to the design of the main amplifier for the MDAC.
The issue of capacitor mismatch, which determines the size of C_s and C_f, will be addressed in 3.3.2.
An helpful technique used in pipeline ADCs is stage scaling, which is included in figure 3.4 and will be explained in 3.3.3.
Noise issues are dealt with in 3.3.4; in this design, they mainly affect the sizing of the compensation capacitors in the main amplifier.
Finally, gain and bandwidth requirements of the amplifier are calculated in 3.3.5.

Currently, a state-of-the-art 12bit pipeline ADC is described in [AB], which is taken as a reference in this chapter.

Comparator, decoder and switching block

Since the thresholds are $\pm V_{ref}/4$, the main requirement for each comparator is an offset lower than $V_{ref}/4$; moreover, the power consumption should be kept as low as possible. The speed should be such that the delay introduced by comparators, logic and switches fits in the time budget; for a sampling frequency $S_R = 100MHz$, these delays should be shorter than $1ns$ [AB].
When it comes to the decision on the topology for comparators, the aim at a low power consumption makes dynamic comparators the most suitable solution to the power issue. Dynamic comparators do not dissipate DC power; when the comparison takes place, parasitic capacitances have to be loaded or discharged by some transient currents, which represent the only source of power consumption in dynamic comparators.

Some different topologies for dynamic comparators can be found in [Su, 4.1].

3.3.2 Sample and multiply capacitors

The operation of the SC amplifier is shown in its three phases in figure 3.6; the total sampling capacitance can be defined as $C_h = C_f + C_s$. The input voltage V_{in} charges C_h; at the instant of the bottom-plate sampling, the charge Q_{in} corresponding to V_{in} is stored at the amplifier input node. When C_f is connected in feedback and $D = 0$, C_s is discharged, because both its terminals are at ground (virtual), and Q_{in} is completely transferred to C_f; if $C_f = C_s$, this implements a multiplication by two.
If $D \neq 0$, it is straightforward to see that the MDAC performs a multiplication by one of $D \cdot V_{ref}$.

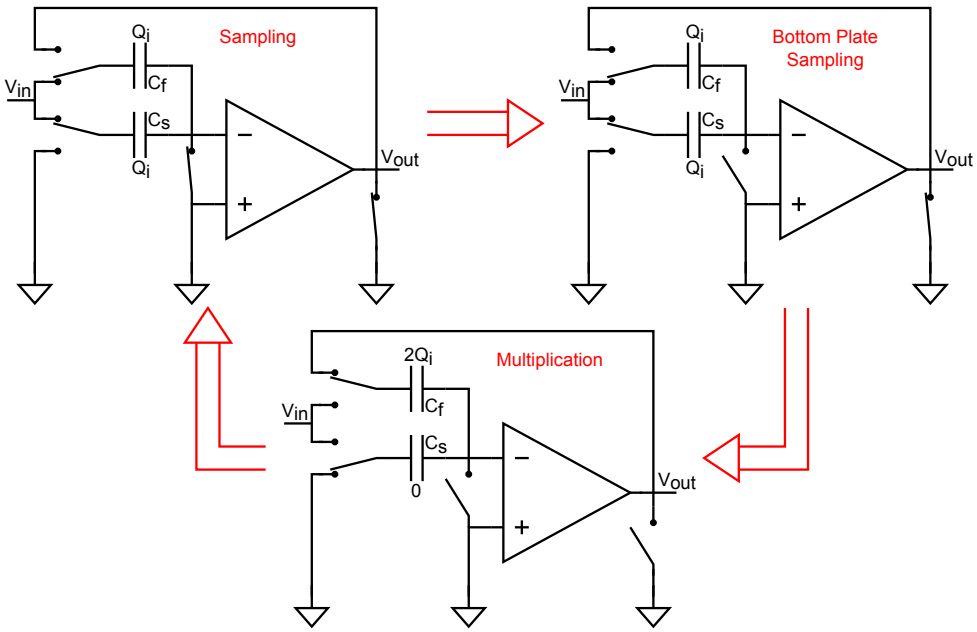

Figure 3.6: MDAC multiplies by 2 the input voltage and by 1 the reference voltage. Single-ended version shown [Ch, App 2].

From equation 3.7, including a mismatch $\Delta C_{f,s}$ between C_f and C_s, the gain of the stage can be written as:

$$\left(2 + \frac{\Delta C_{f,s}}{C_{f,s}}\right) \cdot V_{in} + D \cdot \left(1 + \frac{\Delta C_{f,s}}{C_{f,s}}\right) \cdot V_{ref} \tag{3.8}$$

As explained in [Ma], the capacitor mismatch can be expressed by equation:

$$\frac{\Delta C}{C} = \frac{6 \cdot 10^{-4}}{\sqrt{C_h(pF)}} \tag{3.9}$$

where the capacitance is expressed in pF, and the mismatch is intended as 3σ variation; the conventional mismatch coefficient (numerator in the equation) actually depends on the technology. Now, the mismatch requirement for 1/4 LSB of linearity error in an N-bit resolution, 1.5bit/stage pipeline ADC, is:

$$\frac{\Delta C_h}{C_h} < \frac{1}{2^N} \tag{3.10}$$

From the last two equations, it follows that [Ma]:

$$C_h(pF) \geq 3.6 \cdot 10^{-7} \cdot 2^{2N} \tag{3.11}$$

Therefore, for 12bit and 1/4 LSB error, C_h=6pF; for 12bit and 1/2 LSB error, C_h=1.5pF. Since large capacitors need large currents (paragraph 3.4.2), the choice of the value of the capacitors is a trade-off between good matching and low power. The design choice is C_h=2.4pF (C_f=C_s=1.2pF); this value also gives good sampling noise, as explained later in 3.3.4.

3.3.3 Stage downscaling

In a system made up of several stages, the equivalent input noise of stage i is its noise $N_t(i)$ divided by the gain of the previous stages; therefore the total input referred noise N_{tot} for this pipeline ADC with stage gain of 2 is:

$$N_{tot}^2 = N_t(1)^2 + \frac{N_t(2)^2}{2^2} + \frac{N_t(3)^2}{4^2} + \frac{N_t(4)^2}{8^2} \ldots \tag{3.12}$$

A noise increase of a factor of two (RMS) from one stage to the next one leads to the same noise per stage. As a consequence, the requirements of the later stages can be relaxed. In the present ADC, this translates into a scaling of the stage capacitors along the pipeline, with the clear advantage of a significant decrease in the area and power consumption.

The literature offers some studies of the optimum scaling factor, as in [CG]: the two opposite cases are a scaling factor of 1 (equal stages or no scaling) and a scaling factor of 4. If the factor is 1, only the first stage contributes noise, while the noise of the other stages is negligible; all stages have the same power consumption. If the factor is 4, all stages introduce an equal amount of noise, and the power consumption is concentrated on the first stage; the problem is that the power of the first stage must be significantly increased, in order to compensate for the noise contributions from the later stages. Therefore, an optimum exists, when the capacitors are scaled by the stage gain, in this case 2.
In many implementations, the chosen scaling factor is a bit smaller than 2,

and a good choice is 1.5 for the second stage and 3 (twice the second stage) for the following stages [AB], as shown in figure 3.4.

Table 3.2 will show that, with this scaling scheme, only the noise of the first stages is relevant.

3.3.4 Noise

The main noise sources considered in this thesis are quantization noise, sampling noise, and amplifier noise.

The quantization noise was already given by equation 3.2, reported here:

$$Q_{error} = \frac{LSB}{\sqrt{12}} = \frac{V_{pp}}{2^N} \cdot \frac{1}{\sqrt{12}} = \frac{2V_{ref}}{2^N \cdot \sqrt{12}} \tag{3.13}$$

Sampling noise and amplifier noise are calculated next.

Sampling noise

The sampling noise is the thermal noise of resistors (the switches used in the Switched Capacitor circuit), sampled by the capacitors; it is often named kT/C noise. The general equation for the sampling noise $N_{sampling}$ on a capacitor $C_{sampling}$ is:

$$N^2_{sampling} = \frac{kT}{C_{sampling}}$$

where k is the Boltzmann's constant, and T is the temperature expressed in °K. In the specific case of this MDAC, the sampling noise V_{nsi} of a pipeline stage can be calculated as suggested in [Ch, pag 136-138].
Figure 3.6 shows that, during the sampling phase, the kT/C noise on the sampling capacitors (single-ended) is:

$$V^2_{nsi} = \frac{kT}{C_s + C_f + C_p}$$

where C_p is the parasitic input capacitance of the amplifier.
The corresponding charge Q_{nsi} accumulated across the capacitors is:

$$Q^2_{nsi} = kT \cdot (C_s + C_f + C_p)$$

When C_f is flipped in the multiply phase, the output voltage V_{nso} due to Q_{nsi} is:

$$V^2_{nso} = \frac{Q^2_{nsi}}{C^2_f} = kT \cdot \frac{C_s + C_f + C_p}{C^2_f} = \frac{kT}{C_f} \cdot \frac{1}{\beta}$$

where the feedback factor β is defined in equation 3.20. The last equation, divided by the stage gain, gives the input referred sampling noise N_s of the MDAC (single-ended):

$$N_s^2 = \frac{V_{nso}^2}{G^2} = \frac{kT}{C_f} \cdot \frac{1}{\beta} \cdot \left(\frac{C_f}{C_s + C_f} \right)^2 = \frac{kT \cdot (C_s + C_f + C_p)}{(C_s + C_f)^2} \tag{3.14}$$

If the input capacitance of the amplifier is small enough, it is possible to approximate:

$$N_s^2 = \frac{kT \cdot (C_s + C_f + C_p)}{(C_s + C_f)^2} \approx \frac{kT}{C_s + C_f}$$

Since the noise of the two single-ended inputs adds in an uncorrelated way to the differential noise, the differential input-referred sampling noise N_{sd} is twice as big, and can be approximated by:

$$N_{sd}^2 = 2 \cdot N_s^2 = 2 \frac{kT}{C_s + C_f} \cdot \frac{C_s + C_f + C_p}{C_s + C_f} \approx 2 \frac{kT}{C_s + C_f} = \frac{kT}{C_s} \tag{3.15}$$

Amplifier noise

In section 3.4.1, it will be explained that the chosen architecture for the MDAC amplifier is a two stage with telescopic cascode input. The noise of the output stage is negligible, because it is divided by the high gain of the first stage, when referred to the input. In the telescopic stage, the cascode transistors do not change the currents in the two branches; therefore, also their noise contribution is negligible. As a consequence, the noise in this amplifier can be calculated as explained in [Ra, 7.5, 9.10], using the simplified model of a differential pair, shown in figure 3.7.

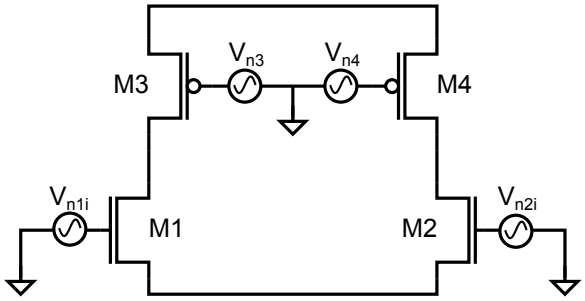

Figure 3.7: Model of the amplifier for noise calculations. Due to symmetry, the noise power of the input transistor M1 is equal to that of M2; also the load transistors M3 and M4 have the same noise power; V_{n1i}, V_{n2i}, V_{n3} and V_{n3} represent the noise sources. All other noise sources in the amplifier are negligible, as explained in the text.

The amplifier will have a large GBW, which will make thermal noise the dominant noise source; flicker noise is therefore neglected in the following calculations.

The noise spectral density of the two input transistors is $V_{n1i}(f) = V_{n2i}(f) = v_{ts}^2(f)$, as in equation 2.8. Also the noise of one current source transistor M_3 (or M_4) is given by its $v_{ts}^2(f)$; since the gain from the gate of M_3 (or M_4) to the output is $g_{m3}(r_{o1}\|r_{o3})$, the output noise spectral density $V_{n3o}(f)$ due to a current source transistor is:

$$V_{n3o}(f) = v_{ts3}^2(f) \cdot g_{m3}^2(r_{o1}\|r_{o3})^2$$

The equivalent input noise spectral density due to T_3 is calculated dividing this last expression by the gain of the amplifier:

$$V_{n3i}(f) = \frac{V_{n3o}(f)}{g_{m1}^2(r_{o1}\|r_{o3})^2}$$

The noise of the current sink transistor M_{11} has no influence on the total noise, because it is a common-mode noise, while the output is differential.
The total equivalent input noise spectral density due to M_1, M_2, M_3, M_4 is:

$$V_{ni}^2(f) = V_{n1i}(f) + V_{n2i}(f) + V_{n3i}(f) + V_{n4i}(f)$$

Substituting expression 2.8, the input-referred noise spectral density $V_{ni}(f)$ becomes:

$$V_{ni}^2(f) = \frac{16kT}{3g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right) \tag{3.16}$$

The factor $(1 + g_{m3}/g_{m1})$ is named excess noise factor of this amplifier topology.
The amplifier in closed-loop is approximated as a single pole system; therefore, the closed-loop pole is located at a frequency $f_{cl} = \beta \cdot GBW$, where GBW is the gain-bandwidth product of the amplifier (equation 3.29), and β is the feedback factor (equation 3.20). The equivalent noise bandwidth B_n is then determined by f_{cl} [JM, 4]:

$$B_n = \frac{\pi}{2} \cdot f_{cl} = \frac{\pi}{2} \cdot \frac{g_{m1}}{2\pi C_c} \cdot \beta = \frac{g_{m1}}{4C_c} \cdot \beta$$

The input-referred noise spectral density is amplified at the output by a factor $1/\beta^2$ [Kh, 5.3.1]. Moreover the input-referred noise spectral density is filtered by the bandwidth of the amplifier; the integral is easily calculated by using the equivalent noise bandwidth. Therefore, the integrated noise at the output of the amplifier N_{ao} is:

$$N_{ao}^2 = V_{ni}^2(f) \cdot B_n \cdot \frac{1}{\beta^2} = \frac{4kT}{3C_c}\frac{1}{\beta}\left(1 + \frac{g_{m3}}{g_{m1}}\right) \tag{3.17}$$

Noise type	Symbol	Value	Contribution
Quantization	Q_{error}	113μV	46.7%
Sampling	N_{sd}^2	82μV	24.5%
Amplifier	N_{ai}^2	88μV	28.8%
Total	N_{tot}^2	165μV	

Table 3.1: Contribution of the different types of noise to the total noise.

Since the pipeline stage has a gain of 2, the amplifier noise referred to the input of the MDAC N_{ai} is:

$$N_{ai}^2 = \frac{N_{ao}^2}{4} \tag{3.18}$$

Total noise

Now that the three main noise contributions are defined, the total noise can be calculated, keeping in mind the stage scaling described in 3.3.3.
The values used in the calculations are $C_s = C_f = 1.2pF$, and $C_c = 3pF$. As for C_s and C_f, also the choice of the value of C_c is a compromise, between low noise (large C_c) and low power (small C_c).
The amplifier noise of the i-th stage, calculated using equation 3.18, is denoted $N_{ai}^2(i)$.
Similarly, the sampling noise of stage i, defined in equation 3.15, is denoted $N_{sd}^2(i)$.
With the help of equation 3.12, the total input-referred noise of the pipeline ADC N_{tot} is calculated as:

$$N_{tot}^2 = Q_{error} + \sum_{i=1}^{10} \frac{N_{ai}^2(i)}{2^{2(i-1)}} + \sum_{i=1}^{10} \frac{N_{sd}^2(i)}{2^{2(i-1)}} \tag{3.19}$$

The values calculated in tables 3.1 and 3.2 are based on $T = 50°$, while other parameters ($\beta = 0.45$, excess noise factor 1.47, $V_{pp} = 1.6V$) are extracted from the simulations of paragraph 3.4.4.
A sinusoidal input waveform of 1.6V peak-to-peak and a noise of 165μV give a SNR=71dB; according to equation 3.4, this corresponds to $ENOB$=11.45.

Table 3.1 shows that the choices of C_s, C_f, and C_c are good: they add as much noise (quadratic sum of sampling and amplifier noise) as the quantization noise. This means that quantization error remains a relevant limitation to the ADC resolution, and, at the same time, the power is not wasted for unnecessarily low sampling and amplifier noise.

Stage	Scaling	Noise contribution
1	1	32.8%
2	2/3	12.3%
3	1/3	6.1%
4	1/3	1.5%
5	1/3	0.4%
6	1/3	0.1%
7-10	1/3	0.0%

Table 3.2: Stage scaling factors and noise contributions along the pipeline (only sampling and amplifier noise).

These noise calculations are based on the largest noise contributions of quantization, sampling and amplifier noise. There are several smaller noise sources which add to the total noise: clock jitter, noise on the reference voltages, noise from the bias circuitry, noise on V_{ref} from the DAC switches, distortion of the switches (the $SINAD$ should be used, instead of SNR), distortion from the amplifier (limited step response). Therefore, the $ENOB$ measured in a prototype will be worse than the calculated 11.45 bits.

3.3.5 Amplifier requirements

In SC circuits, the output voltage of an amplifier at the time when the following stage is sampling must be stable and close to the ideal value, within the limits of the required accuracy. Based on this, the requirements for the amplifier are calculated [Ah, 3.4].

The amplifier is used during the amplifying phase (ϕ_2 in figure 3.5), with C_f as feedback capacitor. The response of the amplifier to a step input signal is similar to a low-pass step response. The feedback factor β is the feedback capacitance divided by the total capacitance at the input node of the amplifier; this includes the parasitic input capacitance of the amplifier C_p. The feedback factor is given by:

$$\beta = \frac{C_f}{C_s + C_f + C_p} \approx 0.45 \tag{3.20}$$

The theory of feedback says that, at low frequencies, the closed-loop low-frequency gain A_c is related to the open-loop low-frequency gain A_o of the amplifier through the feedback factor β by the equation:

$$A_c = \frac{A_o}{1 + A_o\beta} = \frac{1}{\beta + \frac{1}{A_o}} \tag{3.21}$$

The error on the closed-loop gain must be smaller than the required accuracy N_r, expressed in bits:

$$\frac{1}{A_0} \leq \frac{\beta}{2^{N_r}} \Rightarrow A_0 \geq \frac{2^{N_r}}{\beta} \tag{3.22}$$

Once the requirement for the open-loop gain at low frequencies has been calculated, one has to calculate the gain-bandwidth product of the amplifier GBW. The amplifier in closed-loop configuration is modeled as a first-order system with the pole at a frequency $f_{cl} = \beta \cdot GBW$; the transient response $v_o(t)$ to a positive voltage step is:

$$v_o(t) = V_{out} \cdot (1 - e^{-\frac{t}{\tau}}) \tag{3.23}$$

where $\tau = \frac{1}{2\pi f_{cl}}$ is the time constant associated to the pole, t is time and V_{out} is the ideal final value of $v_o(t)$. The maximum time interval allowed to the amplifier for settling is one semi-period of the clock T_s; at this time, the output of the amplifier must be close to V_{out}, within the accuracy N_r:

$$v_o\left(\frac{T_s}{2}\right) \geq V_{out}\left(1 - \frac{1}{2^{N_r}}\right) \tag{3.24}$$

Solving this inequality for f_{cl} gives:

$$f_{cl} \geq \frac{N_r \cdot \ln 2 \cdot S_R}{\pi} \tag{3.25}$$

where S_R, the sampling rate of the ADC, is equal to $1/T_s$. The corresponding gain-bandwidth product GBW must be:

$$GBW \geq \frac{N_r \cdot \ln 2 \cdot S_R}{\pi \cdot \beta} \tag{3.26}$$

The minimum requirements calculated from 3.22 and 3.26 are listed in table 3.3. In practice, the requirements on GBW will be increased, as explained in paragraph 3.4.4; the reason is that, in the time budget, some time (a few hundred picoseconds) has to be allowed to the decoding logic, the switches, and the non-overlapping period of the clocks.

The settling time is defined as the time that the amplifier takes to settle its output to the final value, within the required accuracy. This depends not only on the GBW, but also on the Phase Margin (PM). Condition 3.26 is necessary but not sufficient. In SC circuits, an overshoot in the step response increases the settling time; therefore, the phase margin at the closed-loop frequency f_{cl} needs to be high ($\sim$65°-76°), as explained in [LS, Appendix 6-1].

Stage	N_r	A_0	GBW	f_{CL}	LSB@output
1	13	85dB	633MHz	287MHz	781μV
2	12	79dB	585MHz	265MHz	1.56mV
3	11	73dB	536MHz	243MHz	3.12mV
4	10	67dB	487MHz	221MHz	6.25mV

Table 3.3: Requirements of the first four stage amplifiers and output voltage of each stage corresponding to one LSB.

3.4 Amplifier

In this section the amplifier, designed according to the calculated requirements, is described.
The first paragraph introduces the architecture necessary to fulfill the requirements, while keeping the power consumption as low as possible.
The second paragraph deals with frequency compensation schemes. Three approaches are considered, and their small-signal models are developed (see appendix A). The small-signal models include all the transistors of the amplifier, and give an insight into the different frequency behaviours of the three compensation schemes; furthermore, the model confirms that indirect compensation is effective against the detrimental RHP zero z_1 of standard Miller compensation, and can make the amplifier quicker by increasing the first non-dominant pole p_2.
The third paragraph explains the gain-boosting technique, with the associated condition for stability.
Then, the fourth paragraph shows the simulation results obtained with the amplifier, designed according to the conclusions of the three previous paragraphs.

3.4.1 Architecture choice

The requirements of paragraph 3.3.5 dictate the choice of the amplifier topology, with considerations similar to [AB].

First of all, the output swing must be large, in order to obtain a good SNR; at the same time, the gain must be high. Therefore, a two-stage architecture is used, where the first stage accomplishes a high gain, and a differential pair output stage provides a wide output voltage range.
In order to obtain a high gain, the input stage is cascoded. Since this is not sufficient, also the gain-boosting technique is used. Cascoding and gain-boosting are explained in paragraph 3.4.3. In the small-signal model of para-

graph 3.4.2, the added gain-boosting amplifiers are omitted, because their effect on the locations of poles and zeros is not crucial; the frequency behaviour of these added amplifiers is also explained in 3.4.3.

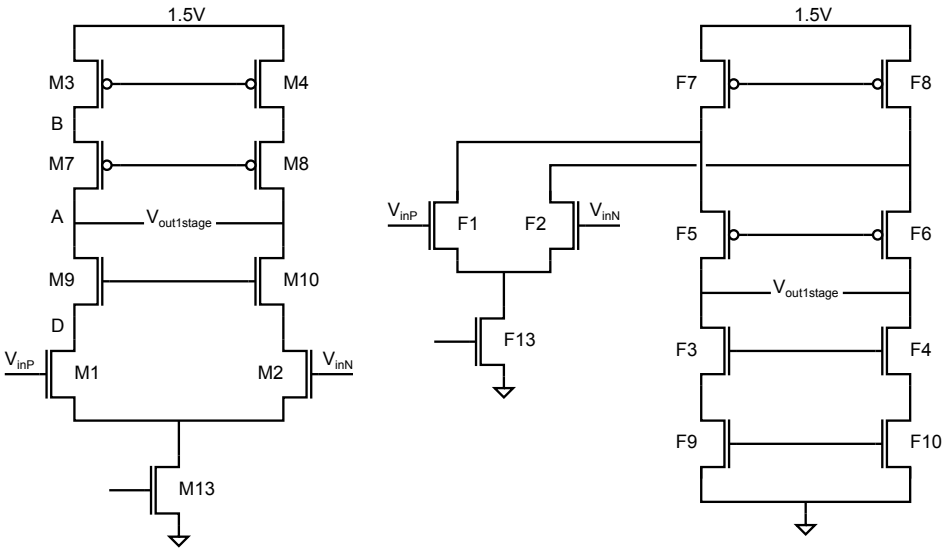

Figure 3.8: Schematic of a telescopic (left) and a folded (right) cascode input stage.

There are two types of cascoded stages: telescopic cascode and folded cascode, both shown in figure 3.8.
The telescopic cascode has two current branches, and a stack of five transistors which decrease the output swing, because of their V_{DSsat} (section 2.1). The excess noise factor is $(1 + g_{m3}/g_{m1})$, as given by equation 3.16.
The folded cascode "folds" the current of the input transistors to a stack of four other transistors; therefore, it has four current branches, and the output swing is one V_{DSsat} larger than in the telescopic topology. The excess noise factor is $(1 + g_{m7}/g_{m1} + g_{m9}/g_{m1})$, as in [Ra, 9.10].
The telescopic cascode is the most suitable topology for the first stage of this amplifier, because only two current branches contribute to the power consumption, and only two transistors contribute to the noise. The smaller output swing is not an issue, because the output stage of the amplifier provides the necessary voltage swing; in this design, the output peak-to-peak swing V_{pp} is 1600mV, leading to a V_{ref} of 800mV.

The requirement for high speed drives the choice of the compensation scheme towards indirect compensation on the cascode, as shown in [HL]. Moreover, NMOS input stages are preferred, so that the signal travels only

through NMOS transistors: PMOS transistors have larger parasitic capacitance (paragraph 2.1) and are therefore slower.

All these topology considerations are reflected in the schematic of the amplifier, shown in figure 3.9, which includes also the compensation capacitors (section 3.4.2).

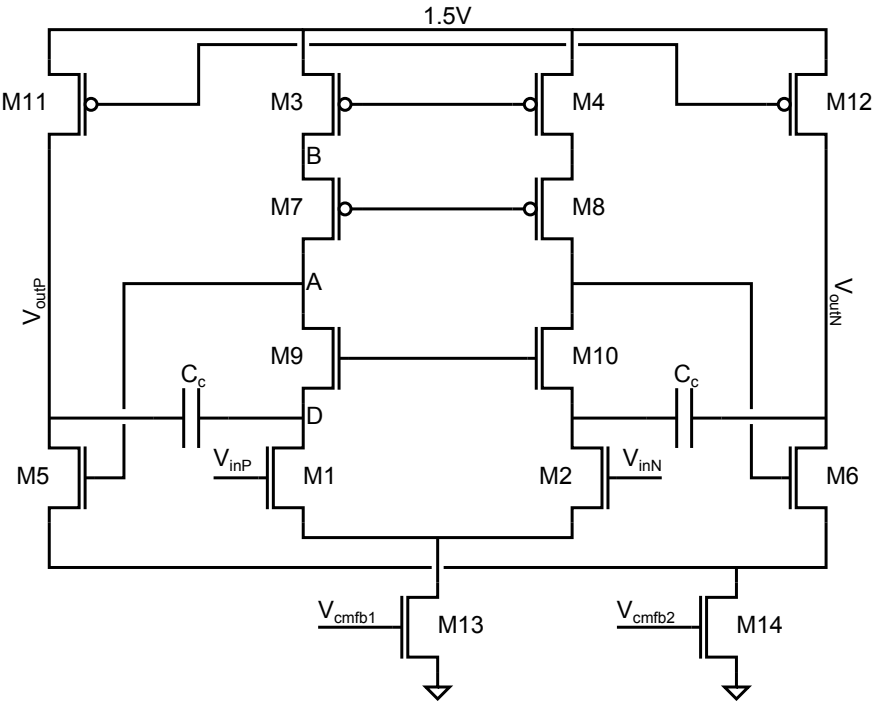

Figure 3.9: Topology of the chosen amplifier [AB]; the gain-boosting amplifiers are included later, in figure 3.14. The compensation capacitors C_c are connected between the output and the input cascode node "D".

3.4.2 Small-signal model

After the discussion of paragraph 3.4.1, a suitable compensation technique has to be chosen, in order to stabilize the amplifier in the whole relevant frequency range.
The three candidate techniques are (node names refer to figure 3.8):

1. Standard Miller compensation (compensation capacitor between the output of the second stage and node A).

2. Indirect compensation on the current load (node B).

3. Indirect compensation on the input cascode (node D), shown in figure 3.9.

The literature offers a study [HL] on a simplified version of this amplifier, where only one node is cascoded. The amplifier in this design has cascoding devices M9-M10 on the input transistors M1-M2 as well as cascoding devices M7-M8 on the load transistors M3-M4. In this thesis, it was decided to study the small-signal models, including both cascoded nodes. Appendix A reports the models and calculations for the three compensation options, developed following reference [HL] as explained next. Simplifications and assumptions were done, aiming at obtaining simple expressions for the poles and zeros, which could be immediately used in the design.

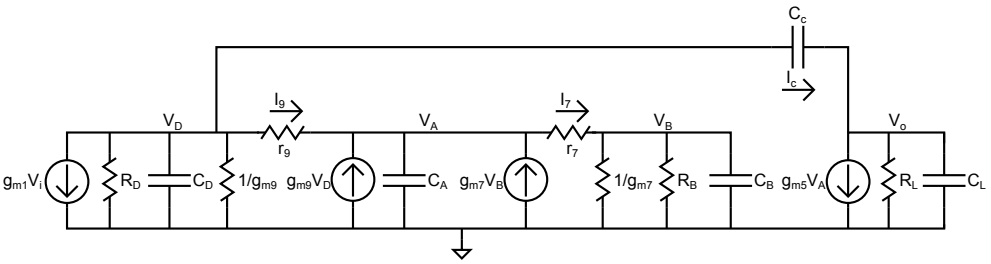

Figure 3.10: Half circuit, differential mode small-signal model of the main amplifier. The expressions for the resistances and capacitances are listed in equations 3.27.

Figure 3.10 reports here the small-signal equivalent model of the amplifier with the chosen indirect compensation on the input cascode. Since the amplifier is fully differential, only the differential mode is relevant. Moreover, a single-ended model of half circuit is sufficient, because the amplifier is balanced (symmetrical).
The cascode transistors M7-M10 are in common gate configuration: the gate voltage V_g is an AC ground, and the small-signal variations of the source and drain voltages v_s and v_d determine the behaviour of the device; figure 3.11 shows that the current generator, corresponding to the transconductance g_m of the transistor, is equivalent to a current generator and a resistor of value $1/g_m$ to ground.

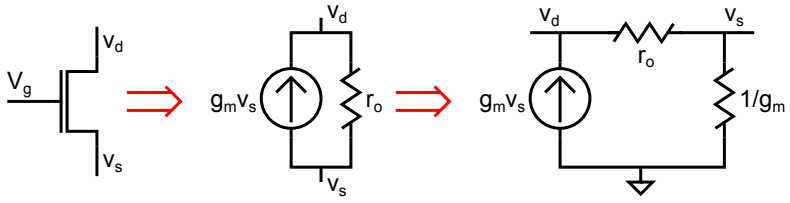

Figure 3.11: Small-signal equivalent model of a transistor in common gate configuration.

The expressions of the resistances and capacitances used in the small signal model are given in equations 3.27.

$$\begin{aligned} R_D &= r_{o1} \\ C_D &= C_{db1} + C_{gs9} + C_{sb9} \\ R_B &= r_{o3} \\ C_B &= C_{db3} + C_{gs7} + C_{sb7} \\ R_A &= r_{o1} g_{m9} r_{o9} \| r_{o3} g_{m7} r_{o7} \\ C_A &= C_{db9} + C_{db7} + C_{gs5} \\ R_L &= r_{o5} \| r_{o11} \\ C_L &= C_{db5} + C_{db11} + C_{load} \end{aligned} \tag{3.27}$$

The results of the calculations reported in the appendix are summarized in table 3.4. In all three options, the open-loop low-frequency gain A_0 and the gain-bandwidth product GBW are:

$$A_0 = g_{m1} R_A g_{m5} R_L \tag{3.28}$$

$$GBW = A_0 \cdot |p_1| = \frac{g_{m1}}{C_c} \tag{3.29}$$

The equations in table 3.4 are used in the design in order to fulfill the requirements listed in table 3.3 in paragraph 3.3.5.

It is now evident that large C_c, C_s and C_f (large C_L), although beneficial for the noise performance, require more power: the larger the capacitances, the larger the currents, which provide larger transconductances needed to send the poles and zeros to high frequencies.

Standard Miller compensation has the drawback of the zero z_1 in the right half plane (RHP). Reference [Ba, 21.2.1] explains that this issue is usually overcome with a zero-nulling resistor. The value of this resistor is process-dependent; one way of compensating the variation is implementing the resistor as a transistor in the linear region; the bias for this transistor requires one more current branch, consuming more power.

Pole / zero	Compensation type			
	Miller	Current load	Input cascode	
			C_B big	C_B small
z_1	$\frac{g_{m5}}{C_c}$	$-\frac{g_{m7}}{C_c+C_B}$	$\pm\sqrt{\frac{g_{m5}g_{m9}}{C_AC_c}}$	
z_2	$-\frac{g_{m7}}{C_B}$			
z_3			$-\frac{g_{m7}}{C_B}$	
p_1	$-\frac{1}{g_{m5}R_AR_LC_c}$	$-\frac{1}{g_{m5}R_AR_LC_c}$	$-\frac{1}{g_{m5}R_AR_LC_c}$	
p_2	$-\frac{g_{m5}}{C_L}$	$-\frac{g_{m5}C_c}{(C_c+C_L)\cdot C_A}$	$-\frac{g_{m7}}{C_B}$	$-\frac{g_{m5}C_c}{(C_c+C_L)\cdot C_A}$
p_3	$\sqrt{\frac{g_{m7}g_{m9}C_L}{2(C_c+C_L)C_BC_D}}$	$\sqrt{\frac{g_{m7}g_{m9}}{C_D[(C_C\|C_L)+C_B]}}$	$-\frac{g_{m5}C_c}{(C_c+C_L)\cdot C_A}$	$-\frac{g_{m9}}{(C_C\|C_L)+C_D}$
p_4			$-\frac{g_{m9}}{(C_C\|C_L)+C_D}$	$-\frac{g_{m7}}{C_B}$

Table 3.4: Equations for poles and zeros of the amplifier, with the three different compensation techniques. Detailed analysis and models are in appendix A.

Other techniques use additional buffer stages to avoid the feedforward path which creates the zero in the RHP; also these techniques introduce additional current branches, which increase the total power consumption of the amplifier. Indirect compensation was introduced in order to move the RHP zero to high frequencies, without dissipating more power, as explained in [SB].
In the two indirect compensation techniques of table 3.4, the first non-dominant pole p_2 is typically at a higher frequency than in the Miller compensation. The locations of the other poles and zeros in the two indirect compensation techniques do not differ much. The equations give important rules for the design of the amplifier with compensation on the cascoded input:

- Transistor M9 needs short channel length, in order to keep C_D small (from section 2.1, C_{gs9} is proportional to the channel length).
- Transistor M9 has to be made wide. For a fixed current, this decreases the overdrive voltage and maximizes the transconductance g_{m9} (equations 2.5 and 2.6).
- Transistor M7 should not be too wide. For a fixed current, the overdrive voltage decreases with the square root of the width (equation 2.5), while C_{gs7} increases linearly with the width (section 2.1); therefore, a reasonably narrow M7 produces a high g_{m7}/C_B.

3.4.3 Gain boosting

In an amplifier, the input MOS transistor converts an input voltage into a current, according to its transconductance g_m, defined in equation 2.6; this current flows through the impedance of the current branch. The open-loop low-frequency gain of the amplifier is given by the transconductance g_m of the input transistor multiplied by this impedance, as also equation 3.28 shows.
Figure 3.12 shows some techniques used to increase the output impedance of the branch:

1. In the simple case of a single transistor, its output impedance is the channel resistance r_0, defined by equation 2.7; the voltage at the drain of the transistor varies significantly with the current. The gain of this stage is $g_m r_0$.
2. A popular way to increase the output impedance is by means of a cascode transistor in common-gate configuration. This transistor, with its gain $g_m r_0$, helps keeping the voltage V_{sc} at the cascode node constant, thus keeping the input transistor in the same operating point, i.e. with

a nearly constant current. Therefore the output impedance is $g_m r_0^2$, and the gain $g_m^2 r_0^2$.

3. In order to achieve even higher gains, the gain-boosting technique can be used. An added amplifier increases the voltage gain of the cascode transistor by its amplification A_{gb}; this keeps V_{sc} even more constant. As a consequence, the output impedance is in the order of $A_{gb} g_m r_0^2$, and the gain $A_{gb} g_m^2 r_0^2$.

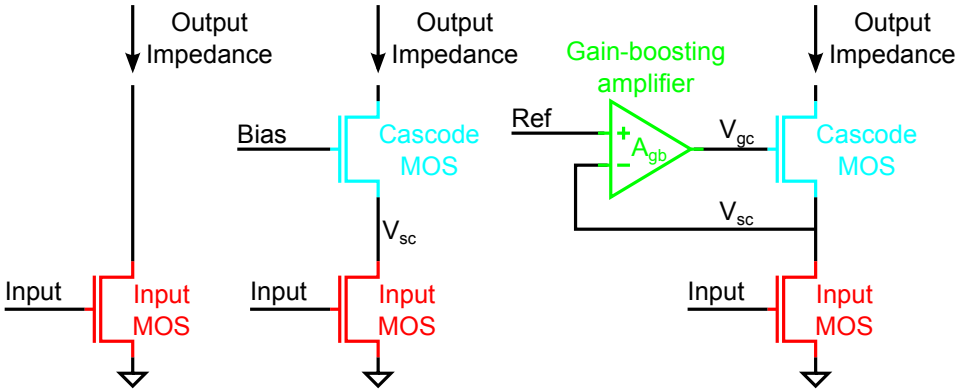

Figure 3.12: Single-transistor amplifier (left), cascoded amplifier (center), gain-boosted amplifier (right).

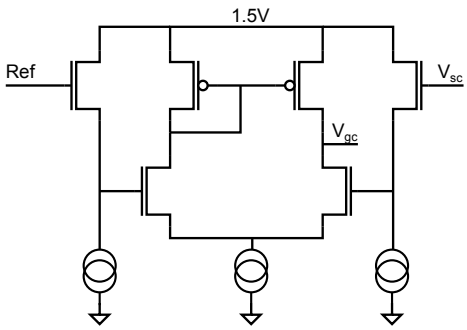

Figure 3.13: Schematic of a gain-boosting amplifier [Ba, 24.4], N type shown. A source follower buffers (level shift) the input signal for the core amplifier.

The used topology for the gain-boosting amplifiers, shown in figure 3.13, yields a gain $A_{gb} = g_m r_0$ (20/30dB); therefore, the gain of the first stage is in the order of $g_m^3 r_0^3$. The schematic of the full amplifier is in figure 3.14.

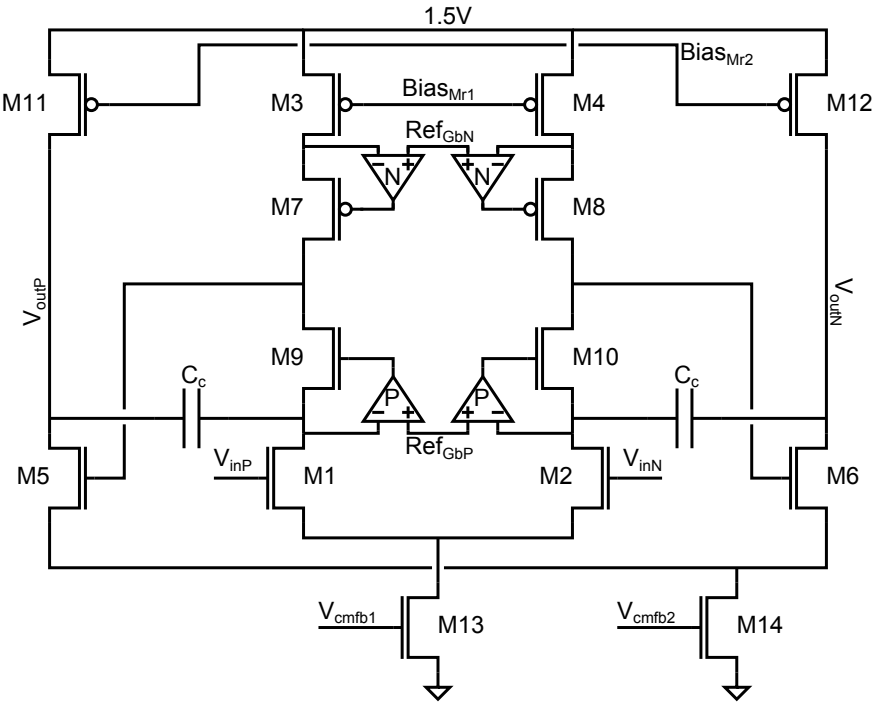

Figure 3.14: Full schematic of the designed amplifier, including the gain-boosting amplifiers at the cascode nodes of the first stage.

The gain-boosting amplifiers have a gain-bandwidth product GBW_{gb}. If GBW_{gb} is larger than the closed-loop -3dB frequency of the amplifier, the gain-boosting amplifiers do not affect the frequency response and the settling time, as in [Ba, 24.4].
Another condition for stability is that GBW_{gb} be smaller than the second pole of the main amplifier, as explained in [BG]. This requirement can be understood with the following consideration: at frequencies higher than the second pole, the output of the amplifier is in phase with the input; this effect causes instability (positive feedback), and the gain-boosters must not amplify it.
The conditions on GBW_{gb} are expressed by equation:

$$\beta \cdot GBW < GBW_{gb} < p_2$$

This condition is achievable with a reasonable current consumption of the gain-boosting amplifiers, because their load is only the C_{gs} of the cascode transistors.

3.4.4 Simulations

The main amplifier for the MDAC was designed with the chosen topology of figure 3.14.

The open-loop low-frequency gain is $A_0 = 92.4dB$. Since the compensation capacitor is $C_c = 3pF$, the transconductance of the input transistor $g_{m1} = 15.9mS$ gives a $GBW = 845MHz$ (equation 3.29).
The input capacitance is $C_p = 250fF$, leading to $\beta = 0.45$ (equation 3.20), which corresponds to a closed-loop gain of $1/\beta = 6.88dB$; the closed-loop pole f_{cl} is $\beta \cdot GBW = 380MHz$; the phase margin at f_{cl} is 73.8°.
The transconductance of the load transistors is $g_{m3} = 7.5mS$; the excess noise factor of the amplifier is $1 + g_{m3}/g_{m1} = 1.5$.
The maximum differential output swing is $V_{pp} = 1.6V$.
The current of the first stage is 3.85mA, while the second stage consumes 7.77mA. Each P-type gain-boosting amplifier consumes 580μA, and each N-type gain-booster consumes 344μA. The total power consumption of the amplifier is therefore 20.2mW, with 1.5V supply voltage. Based on this value, the forecast power consumption of the whole ADC is in the order of 165mW (linear extrapolation with the data in [AB]).
This power consumption, with $ENOB$=11.45 (paragraph 3.3.4) and S_R=100MHz gives a figure of merit (equation 3.6) of 0.59pJ/conversion.

Figure 3.15 is the bode plot of the amplifier; it shows the open-loop low-frequency gain A_0, the -20dB/decade roll-off of the gain with the frequency, and the phase margin at the closed-loop pole frequency f_{cl}.

The transient response of the amplifier when used in the MDAC was simulated using ideal switches. Figures 3.16, 3.17, and 3.18 show the results in the three cases A, B, and C, marked in figure 3.3; since the MDAC is fully differential, and differential voltages are symmetrical around the common-model level, these three cases are sufficient to prove that the amplifier behaves as required:

A: the differential input V_{in} is 200mV, and the decision D of the comparators is 0. According to equation 3.5, V_{out} is 400mV.

B: the differential input V_{in} is again 200mV, but this time the decision D of the comparators is -1. According to equation 3.5, V_{out} is -400mV.

C: V_{in} is 800mV, and D is -1; V_{out} is 800mV. This is the most delicate case for the amplifier, because the output swing is maximum.

Figures 3.16-3.18 show that the amplifier settles to the expected output voltage with the required accuracy within 3.62ns, as required by equation

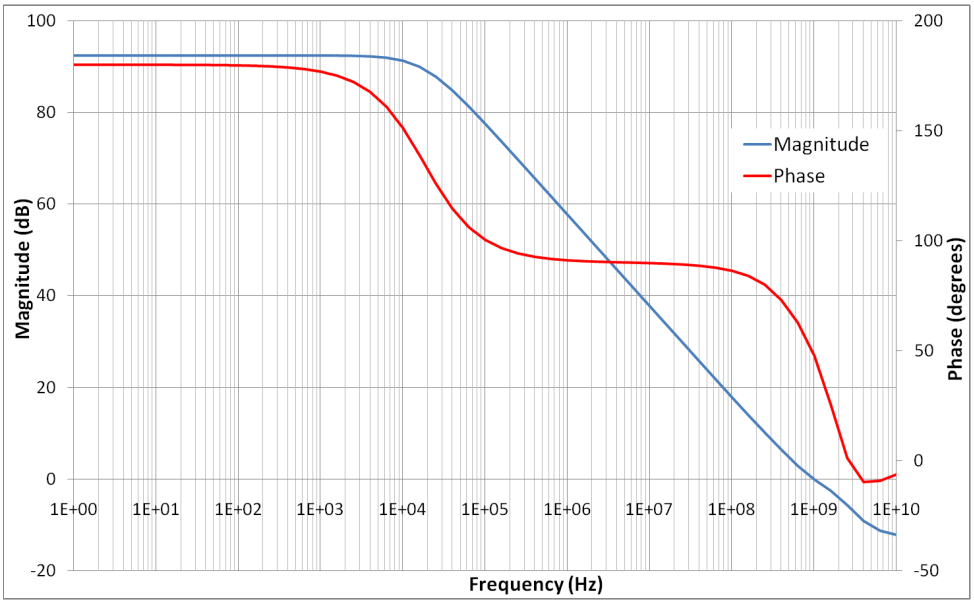

Figure 3.15: Bode diagram of the designed amplifier. At low frequencies the magnitude of the gain is 92.4dB; when the magnitude of the gain is 6.88dB ($1/\beta$), the phase is still 73.8°, which is a good margin for stability in SC circuits.

3.24. For a sampling frequency of 100MHz, $T_s/2$ is 5ns; therefore, the amplifier allows a margin of 1.38ns to the MDAC for the decoding logic, the switches and the non-overlapping period of the clocks.

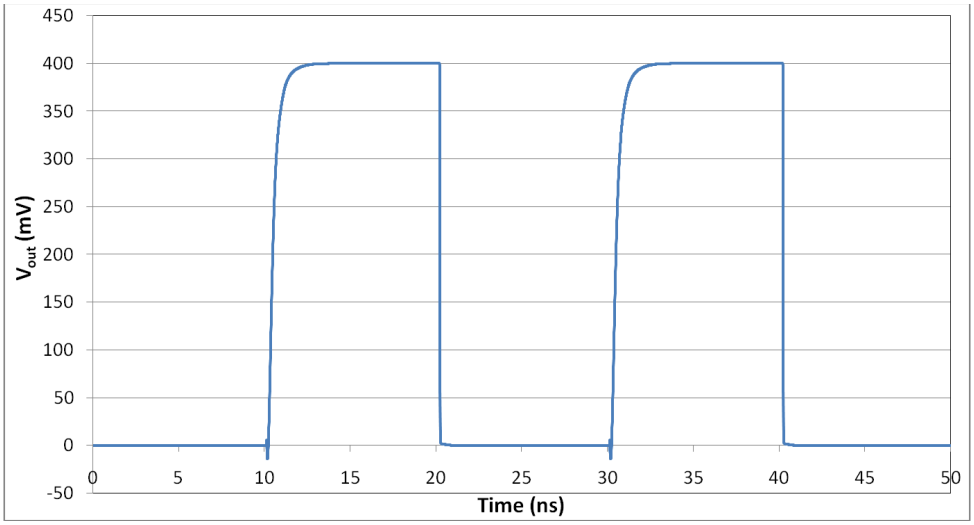

Figure 3.16: Transient response of the amplifier corresponding to case A. The simulation was run with a clock frequency of 50MHz to show the settling and the stability of the output voltage. During the sampling phase (ϕ_1 in figure 3.5), the amplifier is reset and the output is zero. During the amplification phase (ϕ_2), the output settles to the expected V_{out} of 400mV within 1/4 LSB in 3.29ns.

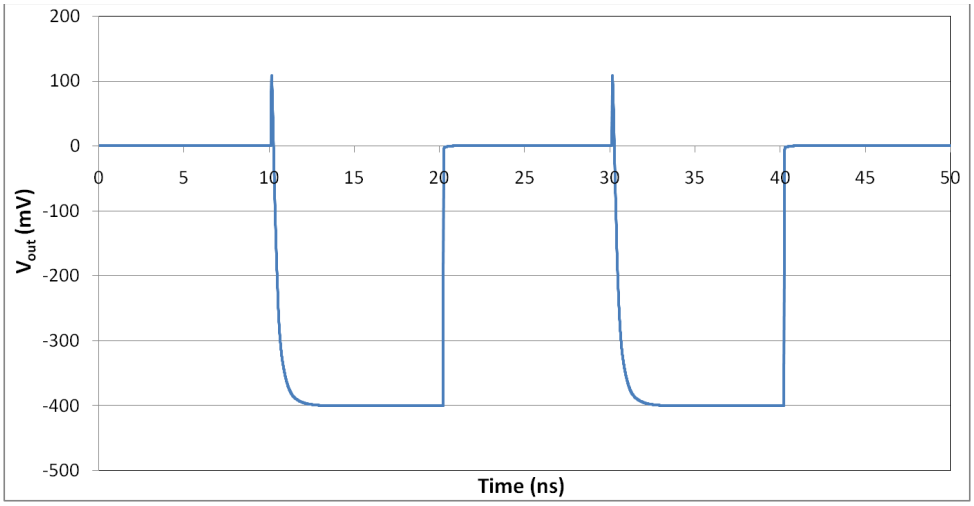

Figure 3.17: Transient response of the amplifier in case B. The output settles to -400mV within 1/4 LSB in 3.28ns.

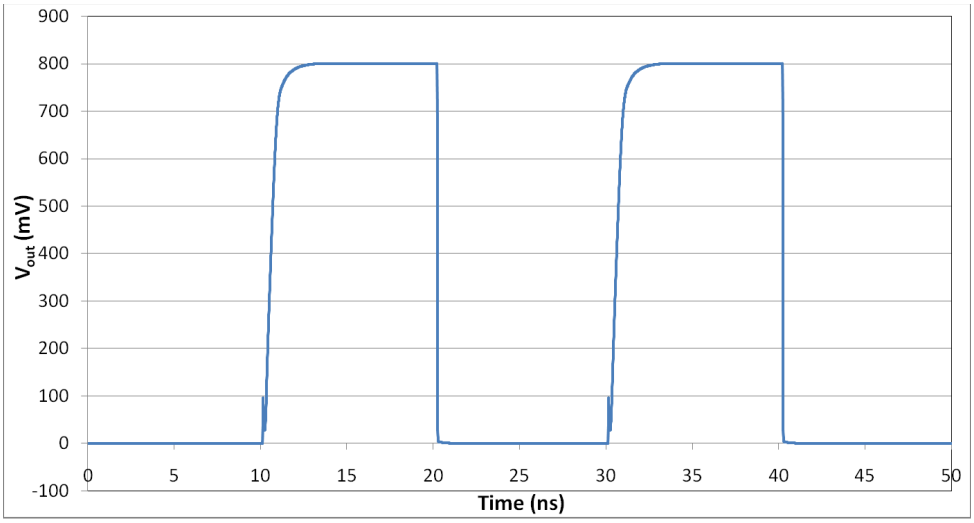

Figure 3.18: Transient response of the amplifier in case C. The output settles to 800mV within 1/4 LSB in 3.62ns.

Chapter 4

Design of the Super-Altro Demonstrator

This chapter describes the design of the Super-Altro Demonstrator (S-Altro). The first seven sections of the chapter present the different blocks and features of the chip; more attention is paid to the blocks which are object of this thesis. Section 4.8 deals with floorplanning and integration issues, while section 4.9 shows the simulation methodology for the full chip.

Since the available area per channel is less than $4mm^2$, the chip must be compact and include all analog and digital functionalities on the same substrate, as explained in paragraph 1.3.1. The logic diagram of the S-Altro is shown in figure 4.1.

4.1 Programmable pre-amplifier shaper

A single detector channel of the Time Projection Chamber is modeled as a capacitor in parallel with a current pulse generator, as will be shown in figure 4.3. The capacitor C_{det} represents the detector capacitance to ground, and in the simulations, its value is between a few and a few tens of pF. The current pulse generator emulates the charge associated with a particle ionizing the gas along its track in the TPC. For design purposes, this pulse provides a current of some tens μA during 1ns, so that the charge injected is of some tens fC. This is compatible with the ALICE TPC, where a Minimum Ionizing Particle (MIP) corresponds to 30000 electrons (4.8fC), and the maximum signal is in the order of 30MIP [Mu].

The charge pulse is amplified and filtered by the Pre-Amplifier Shaping Amplifier (PASA). The PASA used in the S-Altro is based on the PCA16 prototype, developed as a follow-up to PhD Thesis [Tr]; it has a number of

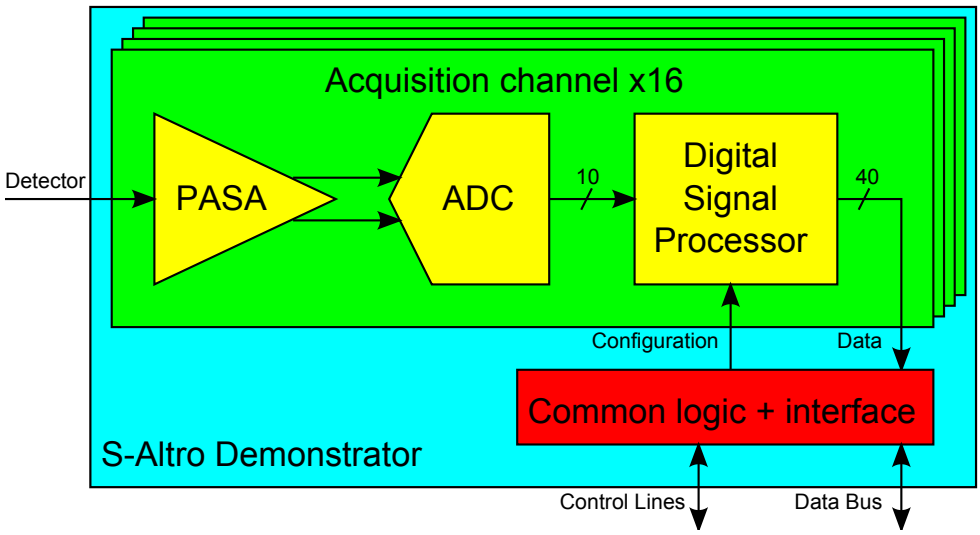

Figure 4.1: Simplified diagram of the Super-Altro Demonstrator. Each of the 16 channels has a detector input and exchanges configuration parameters and output data with the shared interface logic.

options which can be set externally by the user:

Shaping time: the time-to-peak of the output pulse can be chosen among 30-60-90-120ns.

Gain: the voltage/charge gain can be set to 12-15-19-27mV/fC.

Polarity: the PASA can handle signals of both polarities (wire chamber and GEMs have opposite polarities, as explained in paragraph 1.1.1).

BiasDecay: this external voltage controls the resistance of the feedback transistor (shown later as R_f in figure 4.5).

Preamplifier mode: use only the pre-amplifier without shaper.

Shutdown mode: the full PASA can be shut down; this will be useful for power-pulsing tests.

4.1.1 ESD protections

The input of the PASA may be exposed to ElectroStatic Discharge (ESD) events, and must be tolerant to them. Typically, ESD protection devices suit applications, where the possible discharge types are defined by models; these include the Human Body Model (HBM) and the Charged Device Model

(CDM).
A simple and commonly-used protection scheme includes two diodes, which should discharge an ESD current to ground or to the supply rail (depending on the direction of the ESD current).
In the case of high current discharges, some charge will still accumulate at the input node of the PASA, and may lead to breakdown of the oxide of the input transistor; for such currents, a more robust protection is required. This type of protection replicates twice the two diodes, and interposes a resistor of value R_{ESD} between the two pairs, as shown in figure 4.2.

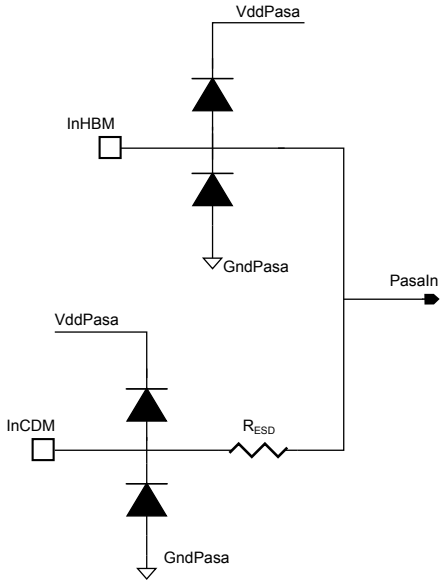

Figure 4.2: ESD protections for the inputs of the PASA. The user can choose the type of ESD protection, and connect only the corresponding pad to the detector.

If the InHBM pad is connected to the detector, an ESD event will discharge the current through one of the two diodes on the upper half of the drawing, depending on the polarity; only two diodes account for the protection of the PASA (one of the other two diodes will also drain some current, but this will not help the PASA).
If the InCDM pad is connected to the detector, an ESD event will discharge also through one of the diodes at the lower half of the drawing. More precisely, depending on the ratio between the series resistance R_{ESD} and the equivalent resistance of the diode, only a fraction of the current will flow through the resistor. Therefore, the PASA is better protected from ESD events.

In the S-Altro, each of the 16 channels has one InHBM and one InCDM input; the chosen input is connected to the detector, while the other can be left floating. This scheme was designed to increase the ESD robustness of the PASA input by a factor of 2 when using the InCDM pad. Models for ESD discharges in the detectors for High-Energy Physics (HEP) applications of the S-Altro were not available, and therefore some tests will be needed for a realistic estimation of the tolerable ESD energy. Assuming that the ESD in a gas chamber can be modeled with a charged capacitor connected to the PASA, then the series resistor would be necessary in order to limit the discharge current.
The advantage of this scheme with two inputs per channel is that also the InHBM pad is available. When using this pad, no resistance is added in series with the input signal; therefore, the noise will be lower, as explained in the next paragraph.

4.1.2 Noise in the PASA

This paragraph follows the calculations in references [Ga] [Tr] [GM, 4], in order to describe the noise introduced by the PASA. Figure 4.3 includes the main noise sources. The charge-sensitive pre-amplifier is an integrator. As

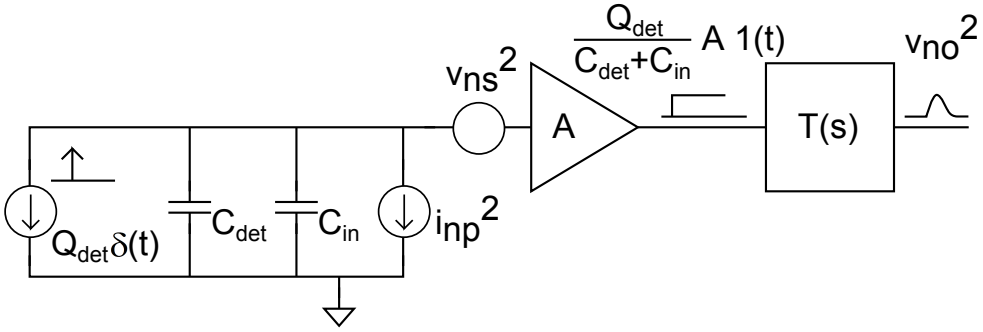

Figure 4.3: Scheme of the detector and the PASA, with pre-amplifier and shaping amplifier, including series and parallel noise sources [GM, 4] [Tr].

shown in the picture, its response to a Dirac delta current pulse from the detector is a step function ($1(t)$), which is then filtered by the shaper.

In a well-designed PASA, the noise comes mainly from the input transistor (white and flicker series noise), from the feedback resistor (white parallel noise) and from the ESD series resistor (white noise, series).
Three Parameters a, b and c are introduced; they are independent of the angular frequency ω. The average series noise voltage spectral density v_{ns}

and the average parallel noise current spectral density i_{np} are expressed as:

$$v_{ns}^2(\omega) = a + \frac{c}{|\omega|} \tag{4.1}$$

$$i_{np}^2(\omega) = b \tag{4.2}$$

Parameter c is related to the frequency-dependent flicker noise. Defining C as the total input capacitance (detector capacitance plus capacitance of the input transistor),

$$C = C_{det} + C_{in} \tag{4.3}$$

the parallel noise can be expressed as its equivalent series noise, thus obtaining the total noise spectral density at the output of the pre-amplifier with gain A:

$$N(\omega) = A^2 \cdot \left(a + \frac{b}{(\omega C)^2} + \frac{c}{|\omega|} \right) \tag{4.4}$$

With an ideal current pulse at the input, the pre-amplifier output is a step function, and the output of the shaping amplifier is the shaper step response:

$$v_o(t) = \frac{A}{C} \cdot L^{-1} \left(\frac{T(s)}{s} \right) \tag{4.5}$$

where L^{-1} is the inverse Laplace operator, s is a complex number ($s = j\omega$, where j is the imaginary unit) and $T(s)$ is the transfer function of the shaping amplifier.
The average total integrated output noise of the system is:

$$v_{no}^2 = \frac{1}{2\pi} \int_0^\infty N(\omega) \cdot |T(j\omega)|^2 \, d\omega \tag{4.6}$$

Using equations 4.6 and 4.4, the average total output noise can be expressed also as:

$$v_{no}^2 = v_{noParallel}^2 + v_{noSeriesT}^2 + v_{noSeriesF}^2 \tag{4.7}$$

where $v_{noParallel}^2$ is the output noise due to parallel noise (b),
$v_{noSeriesT}^2$ is the output noise due to series thermal noise (a),
$v_{noSeriesF}^2$ is the output noise due to series 1/f noise (c).

It is useful to imagine the amplifier as a noise-free system, with only one noise source, at the input; the noise of this source is amplified and generates an amount of output noise equivalent to v_{no}^2. This input-referred Equivalent

Noise Charge (ENC) is calculated reporting the output noise to the input, that is, dividing by the gain of the system (using equation 4.5):

$$ENC = \frac{\left\{\frac{1}{2\pi}\int_0^\infty \left[C^2 \cdot \left(a + \frac{c}{|\omega|}\right) + \frac{b}{\omega^2}\right] \cdot |T(j\omega)|^2 \, d\omega\right\}^{\frac{1}{2}}}{\max\left\{L^{-1}\left[\frac{T(s)}{s}\right]\right\}} \tag{4.8}$$

$$h(t) = L^{-1}\left[H(s)\right] = L^{-1}\left[\frac{T(s)}{s}\right] \tag{4.9}$$

To simplify, the function $h(t)$, defined above, is assumed normalized to unity, that is, $\max\left[h(t)\right] = 1$.
The integral in equation 4.8 can then be solved [Ga], and the ENC can be expressed as a sum of the contributions of the three noise sources:

$$ENC^2 = \frac{a}{\tau}C^2 A_1 + 2\pi C^2 c A_2 + b\tau A_3 \tag{4.10}$$

where τ is the time constant of the filter. In case of a 4-th order filter, τ is the shaping time divided by 4 (e.g. a shaping time of 60ns gives τ=15ns). The three parameters A_1, A_2 and A_3 are pure numbers which depend solely on the frequency shaping of the filter (a CR-RC^4 in this case).

At this point, equation 4.10 gives the ENC, and the only thing left to be evaluated are the spectral densities a, b, and c.
The series thermal noise a is given by the thermal noise of the input transistor in the strong inversion region (equation 2.8) plus the thermal noise (equation 2.10) of the ESD resistance (only in the case of InCDM pad used):

$$a = \frac{8}{3}\frac{kT}{g_m} + 4kTR_{ESD}$$

where k is the Boltzmann's constant, T is the absolute temperature g_m is the transconductance of the input transistor. The parallel thermal noise b is the noise of the feedback resistor (equation 2.11), which is actually implemented as a transistor biased in the linear region:

$$b = \frac{4kT}{R_f}$$

The feed-back resistance R_f depends on the BiasDecay voltage(introduced in 4.1): it is 300kΩ for BiasDecay=0V, and 2.3MΩ for BiasDecay=1V. For low noise performance, it is preferable to have R_f large, but in order to better tolerate pile up (increase the counting rate) of input pulses arriving at a short time distance, it is better to discharge quickly the feedback capacitor with a

small R_f.
The series flicker noise c comes from the input transistor, according to eq 2.9:

$$c = \frac{K_F}{C'_{ox} W L}$$

Figure 4.4 shows some simulations of the noise (ENC) of the PASA, as a function of the detector capacitance, with different values of BiasDecay and shaping time, with and without ESD series resistor. The interpretation of these simulations, using eq 4.10, is:

- The ENC increases with C_{det}.
- The ENC decreases with large R_f (compare red and green lines, or blue and purple lines).
- The ENC increases with the addition of R_{ESD} (compare red and purple lines, or green and blue lines).
- With shorter τ, b dominates at low C_{det}, while a dominates at large C_{det} (compare green and yellow lines).

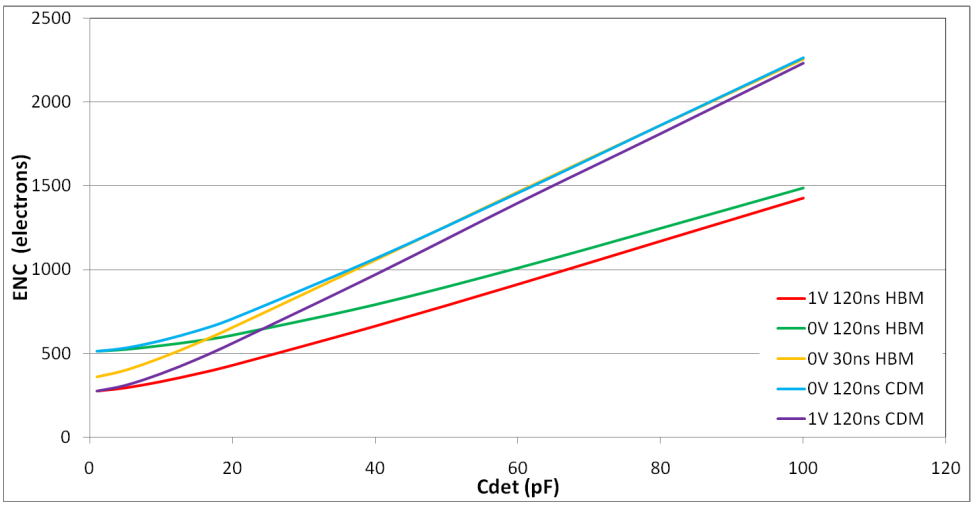

Figure 4.4: Equivalent Noise Charge of the PASA, simulated as a function of the detector capacitance. The five series refer to different values of the BiasDecay voltage (0V or 1V), of the shaping time (30ns or 120ns) and to different ESD protections (InHBM or InCDM pads).

4.1.3 Filters and power consumption

Figure 4.5 is a schematic diagram of the PASA. The pre-amplifier is a Charge Sensitive Amplifier (CSA) and is followed by the pole-zero cancellation network and by the first shaper; the first shaper has a differential output, not shown in the diagram for simplicity. A second shaper, equivalent to the first one, is also present, although not shown in the diagram. The references for this circuit are [CS, 5] and [GO].

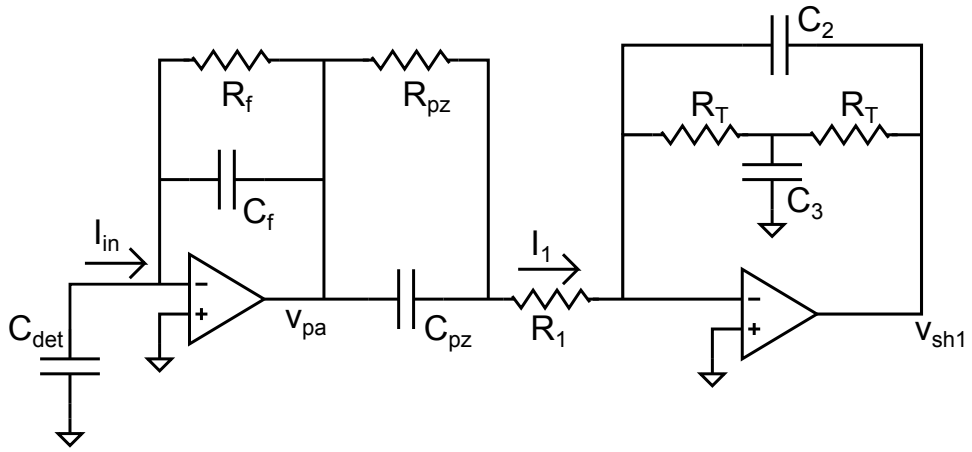

Figure 4.5: Model of the PASA: detector equivalent capacitance, pre-amplifier, pole-zero cancellation network, first T-bridge shaping amplifier; the second T-bridge shaper is not shown.

The ideal voltage/charge gain of a pre-amplifier is: $\frac{1}{C_f}$ (mV/fC); in this PASA, C_f is 790fF.

In order to drain most of the charge pulse coming from the detector (not accumulating charge on the detector capacitance), the input impedance of the PASA must be low. This means that the gain K of the amplifier in the CSA must be high, so that the Miller effect on the feedback capacitance ($C_f(1-K)$) effectively reduces the input impedance. The gain K must be high also in order to maintain the linearity of the PASA. In simulations, K is larger than 100 (40dB).

The voltage gain at the output of the CSA is:

$$-\frac{V_{pa}}{I_{in}} = \frac{R_f}{1 + j\omega R_f C_f}$$

One pole is given by the time constant of the feedback, and one comes from

the amplifier with capacitive feedback [CS, 5.3.1]:

$$p_1 = \frac{1}{2\pi R_f C_f}$$

$$p_2 = \frac{GBW \cdot C_f}{C_{det} + C_f + C_{in}}$$

The response of the CSA to a charge pulse has a rise time $t_r = 2.2\frac{C_{det}+C_f+C_{in}}{2\pi GBW \cdot C_f}$ The input of the first shaping amplifier is a virtual ground; therefore, the current through the pole-zero cancellation network into the first shaper is:

$$\frac{I_1}{V_{pa}} = \frac{1}{R_{pz} + R_1} \cdot \frac{1 + j\omega R_{pz} C_{pz}}{1 + j\omega \frac{R_1 R_{pz} C_{pz}}{R_1 + R_{pz}}}$$

This equation shows that the pole-zero network introduces one pole and one zero:

$$z_{pz} = \frac{1}{2\pi R_{pz} C_{pz}}$$

$$p_{pz} = \frac{R_1 + R_{pz}}{2\pi \cdot R_1 R_{pz} C_{pz}} \cong \frac{1}{2\pi R_1 C_{pz}}$$

The equation for the output of the first shaper (T-bridge) is:

$$\frac{V_{sh1}}{I_1} = -2R_T \frac{1 + j\omega \frac{R_T C_3}{2}}{(j\omega)^2 R_T^2 C_2 C_3 + j\omega 2 R_T C_2 + 1} = -2R_T \frac{1 + \frac{s}{\omega_z}}{\frac{s^2}{\omega_0^2} + \frac{s}{Q \cdot \omega_0} + 1}$$

The T-bridge generates one zero and two poles, with quality factor Q [GO]:

$$\omega_z = \frac{2}{R_T C_3}$$

$$\omega_0 = \frac{1}{R_T \cdot \sqrt{C_2 C_3}}$$

$$Q = \frac{1}{2}\sqrt{\frac{C_3}{C_2}}$$

The pole p_2 is at very high frequency, and therefore neglected; the pole which causes the slow decay of the output of the CSA, p_1, is cancelled by the zero of the pole-zero network z_{pz}. The pole of the pole-zero network, p_{pz}, is cancelled by the zero of the first shaper ω_z. The remaining poles and zeros are the two complex conjugate poles ω_0 from the first shaper plus the two poles and one zero from the second shaper: the whole system, with one zero and four poles, is a $CR - RC^4$ filter.

Feedback resistor R_f and pole-zero resistor R_{pz} are actually implemented as transistors operated in linear region. Their gate voltage is set by a dedicated circuit, where the externally applied voltage $BiasDecay$ plays a role; moving this voltage in the range 0V-1V, the resistance R_f varies from 300kΩ to 2.3MΩ. As explained in 4.1.2, a large value of R_f gives a better noise performance. On the other hand, a smaller R_f gives a higher p_1, which determines a faster return to baseline of the output of the CSA (V_{pa}).

The programmability of shaping time and gain of the PASA is implemented with switches, which can short some resistors and capacitors in the shapers.

Figure 4.6 shows the magnitude of the transfer function of the PASA, with 30ns and 120ns shaping time.

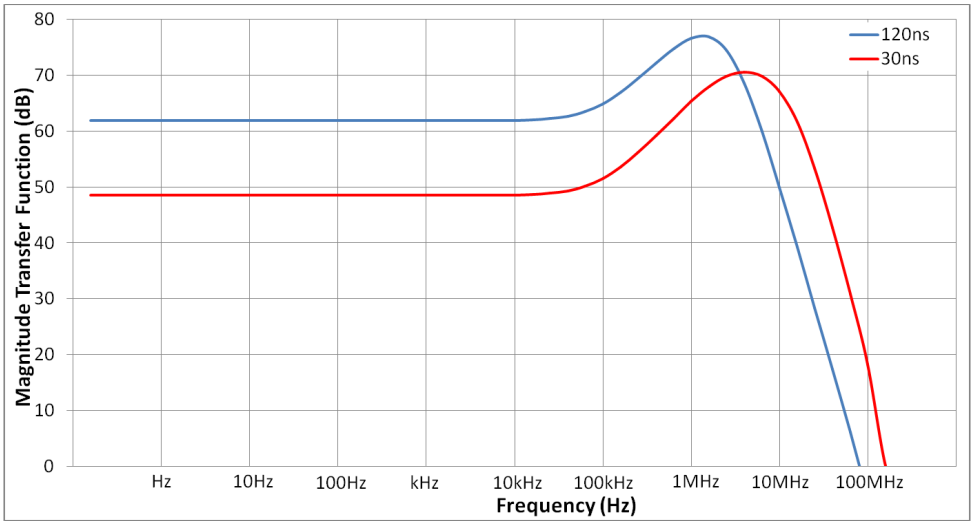

Figure 4.6: Magnitude of the transfer function of the PASA; the blue plot is for a shaping time of 120ns, while the red plot is for 30ns.

The Power Supply Rejection Ratio (PSRR) of the PASA is influenced by the ESD protections. In order to define the PSRR [LS, pag 562], the system is considered as having 3 terminals: the input, the voltage supply and the differential output; the PSRR is then given by the following equation:

$$PSRR = \frac{A_d}{A_s}$$

where A_d is the transfer function of the whole system (input voltage to differential output voltage), and A_s is the gain from the supply terminal to the differential output. Figure 4.7 plots the PSRR before and after the implementation of the ESD protections.

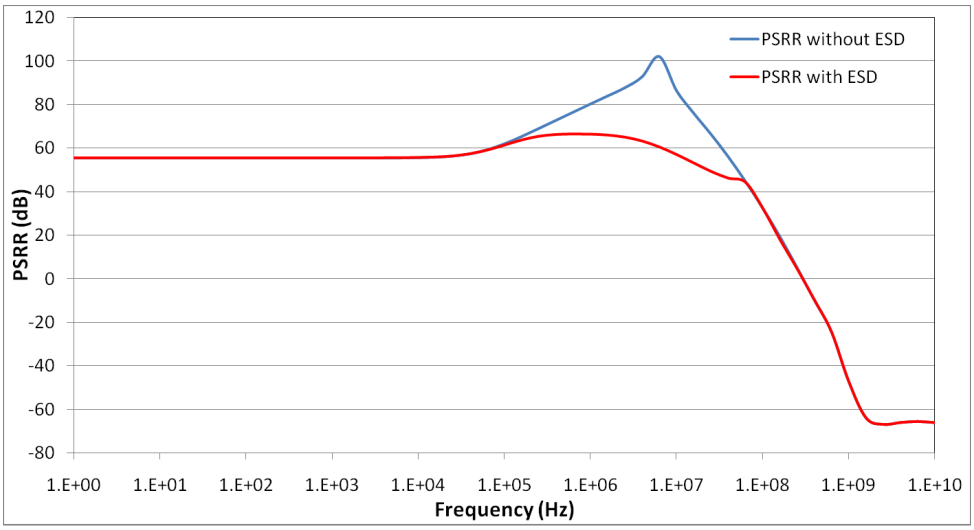

Figure 4.7: Power Supply Rejection Ratio of the PASA, simulated with (red line) and without (blue line) ESD protections.

The ESD protection diodes add some parasitic capacitance between the inputs and the supplies; a variation of the supply voltages is propagated to the input node and amplified, making the PSRR worse.

A typical profile of the power consumption of the PASA in the time transient domain is plotted in figure 4.8.

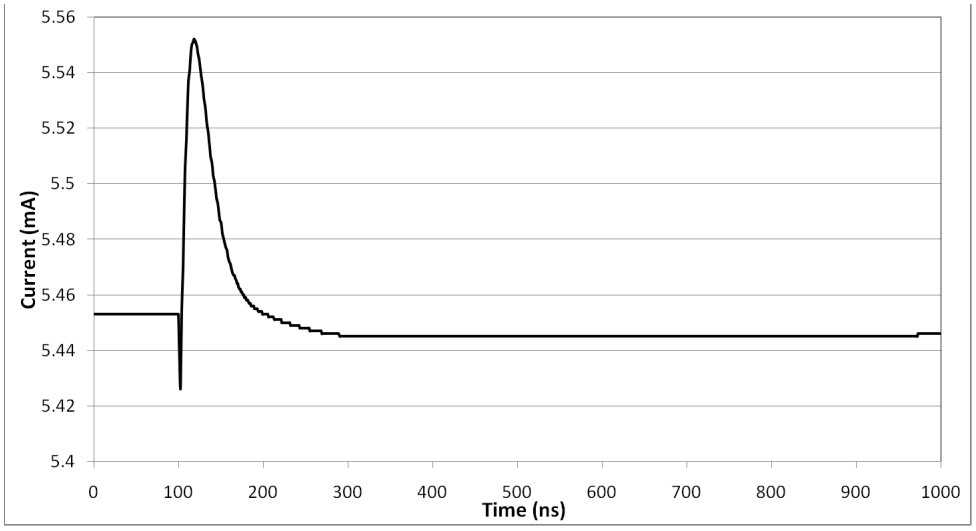

Figure 4.8: Typical time profile of the power consumption of the PASA at the arrival of a pulse.

The bias circuitry contains two switches controlled by the shutdown pin

voltage; when the shutdown feature is enabled, these two switches turn off the bias circuitry, clipping the gates of the PMOS to the supply voltage and the gates of the NMOS to ground, and, therefore, turning off the whole PASA. It takes about 100ns to turn completely off or on again the PASA; during shutdown, the leakage current is 80μA per channel.

The nominal single-ended output range of the PASA is 250mV-1.25V; thus, the maximum peak-to-peak output differential voltage is 2V. The polarity switch controls the reference voltages in the fully differential shaping amplifiers; by doing this, it is able to invert the two rails (250mV and 1.25V). Therefore, the PASA can handle signals of both polarities, keeping the outputs inside the usable range.

A Verilog-AMS model of the PASA has been written, and can be found in the Appendix (B.1). This model is necessary for the final verification of the full S-Altro assembly (4.9). The model includes the pre-amplifier, the feedback capacitance, the discharge resistance, and the pole-zero cancellation network; the DC input voltage of the pre-amplifier is taken into account. The model of the input stage is therefore electrically equivalent to the PASA. The shaper is simplified as two single-pole amplifiers. The action of the polarity switch is also modeled, in order to keep consistency with the polarity bit of the Digital Signal Processor (DSP).
Results of the simulation with this model of the PASA are plotted in picture 4.15, together with the Verilog-AMS models of the other components of the S-Altro. The simulation shows the voltage at the input node of the PASA, and the two single-ended outputs; the baselines, amplitudes and shapes of these signals look similar to the simulations of the schematic and extracted netlists.

4.2 ADC

The S-Altro integrates the ADC presented in [FS]; its features are summarized in this section. This is a pipelined 10bit ADC, which works at a maximum conversion rate of 40MS/sec. The analog input is differential and the clock is of single-ended CMOS type, as the 18 digital outputs.

Since the output of the PASA rises to its maximum in 30-120ns from the arrival of the pulse, an ADC with a sampling frequency of 40MHz (corresponding to a period of 25ns) always acquires at least one sample from the leading edge of the pulse.

The pipeline architecture is implemented with Switched Capacitor topology (SC), and it consists of eight 1.5bit stages followed by one 2bit stage. The latency of the pipeline is of 8 clock cycles.

The main amplifier of the Multiplying DAC (MDAC) is fully differential with continuous-time Common-Mode Feed-Back (CMFB), which requires the common-mode reference voltage V_{CmOut}. The MDAC uses the double sampling technique, where the capacitor structure of each stage is duplicated. In this way, while one structure is sampling, the other one is amplifying; therefore, the amplifier disposes of a double amount of time to settle (one full clock cycle). This keeps the amplifier working all the time, instead of wasting power for half clock cycle, and also allows a reduction of the bandwidth requirement of the amplifier.

The analog-to-digital conversion is based on three reference voltages (externally provided), whose nominal values are: V_{ref-}=250mV, V_{ref+}=1250mV, and V_{cm}=750mV; these voltages are centered at the half supply voltage (1.5V) and correspond to a V_{ref}=1V. The analog inputs are allowed to swing between V_{ref-} and V_{ref+}; this interval is compatible with the outputs of the PASA.

In the ideal case, the comparators do not suffer from mismatch: one comparator, with a threshold of 0V (differential), provides one bit of resolution. In the real case, comparators are affected by mismatch, and their thresholds differ from the nominal values; therefore, a pipeline ADC with one comparator per stage would offer an unacceptable non-linearity. For this reason, each pipeline stage includes a sub-ADC composed of two comparators, whose thresholds are $\pm\frac{1}{4}V_{ref}$; the 2bit output of the sub-ADC tells in which of the three ranges (defined by the two thresholds) the differential input signal was. The resolution of this type of sub-ADC is defined as 1.5bit: one bit is for the real resolution, while the other half bit is used to correct comparison errors, as will be explained in section 4.4. The comparators are dynamic (the comparison is triggered by a clock).

The quantization unit (1 Least Significant Bit, LSB) of the ADC is equal to $2V_{ref}/(2^{10}-1)$, that is, 1.955mV; the corresponding quantization noise, $LSB/\sqrt{12}$, is 0.56mV; assuming an Effective Number Of Bits (ENOB) of 9.0, the input referred noise of the ADC would be 1.12mV. These values can be reported to the input of the PASA; the results are shown in table 4.1, for the maximum and minimum value of the gain of the PASA. The last column reports the total noise of the ADC: the values are similar to the noise of the PASA for small input capacitances (see plot 4.4); this shows that the resolution of 10 bits, with ENOB$\cong$9, matches with the performance of the PASA, without degrading too much the overall system performance and, at the same time, without overdesigning the ADC (without wasting power).

The ADC incorporates a clock generator, which receives the input clock, and delivers the many clocks needed by the ADC stages for proper operation; some of these secondary clocks will be later explained in section 4.6. One

PASA Gain (mV/fC)	LSB (fC)	LSB (e^-)	Quantization noise (e^-)	Noise (if ENOB=9) (e^-)
12	0.162	1018	294	588
15	0.130	814	235	470
19	0.102	643	186	371
27	0.072	453	131	262

Table 4.1: LSB, quantization noise and total noise of the ADC expressed as equivalent charge at the input of the PASA.

important requirement of the clock generator is that the clocks must turn on and off the analog switches in a strictly controlled sequence: this is crucial in order to minimize the effects of the charge injection of the switches (bottom plate sampling technique). The clocks which control the data flow from stage to stage operate at the input clock frequency. Some clocks choose which part of the duplicated capacitor structure should be used; due to double sampling, these clocks distinguish between odd and even samples, and must operate at half the frequency of the input clock; for this reason, the clock generator uses a D flip-flop in order to produce a secondary clock, whose frequency is half the frequency of the input clock.

The circuit which sets the bias currents to the analog parts of the ADC is based on a β-multiplier, as explained in 4.3. This makes the analog power consumption adjustable depending on the clock frequency: it is 32mW at the design sampling frequency of 40MHz. At the same frequency, the power consumption of the digital parts of the ADC is 2mW.

A Verilog-AMS model of the ADC has been written (B.2).
The model of a 1.5bit stage (B.2.1) compares the differential input voltage with the references and produces the digital results; moreover, it multiplies the analog voltage by a factor of two and adds or subtracts the appropriate reference, depending on the digital results.
The model of the last 2bit flash stage (B.2.2) simply compares the analog voltage with the thresholds and provides the last 2 bits to the pipeline.
A simulation of the model of the ADC together with the digital error correction is shown in picture 4.15.

4.3 Bias circuitry for the ADCs

The amplifiers in each pipeline stage need proper biasing. The biasing current is chosen according to the bandwidth requirement of the amplifier, which

is, in turn, dictated by the sampling frequency of the whole converter. It follows that a significant amount of power would be wasted, when the ADC is operated at frequencies lower than the maximum nominal sampling frequency of 40MHz. Therefore, a biasing strategy has been chosen, which adapts the current through the amplifiers to the sampling frequency; figure 4.9 shows this biasing architecture, inspired by the β-multiplier presented in [LB].

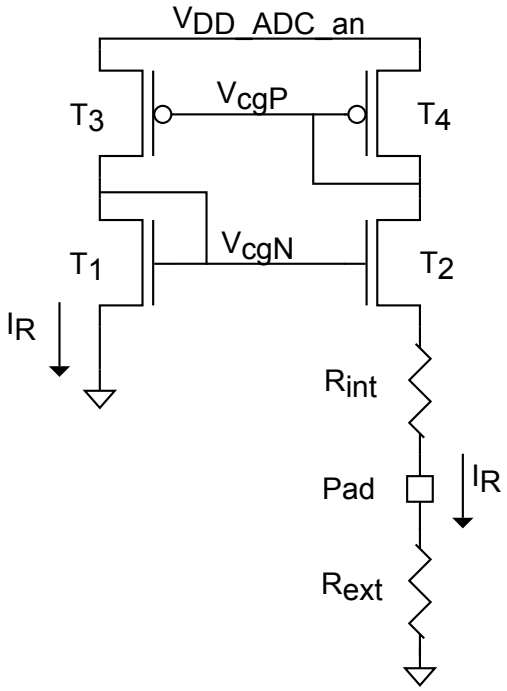

Figure 4.9: Scheme of the ADC biasing core, based on a β-multiplier [LB]. The start-up circuitry is not shown.

Transistors T_3 and T_4 are a PMOS current mirror; therefore, the same current I_R flows through the two branches of the circuit. Transistor T_2 has a W/L ratio K times that of T_1; the biasing resistance R is the sum of R_{int} and R_{ext}.
Some circuit considerations give the following equation for the current through the biasing resistor [Ba, 20]:

$$I_R = \frac{2}{R^2 K P_n \cdot \frac{W_1}{L_1}} \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

where W_1 and L_1 are the sizes of T_1, and KP_n is defined in equation 2.2. This equation suggests that this architecture offers a good PSRR, while allowing an external control on the bias current.

As the scheme shows, the loop of the four transistors creates a positive feedback. This is stable under the condition that the loop gain be less than 1. The loop gain is given by the following expression [LB]:

$$\frac{g_{m2} \cdot g_{m3}}{g_{m1} \cdot g_{m4}} \cdot \frac{1}{1 + R \cdot g_{m2}} \tag{4.11}$$

Practically, V_{cgP} will be greater than V_{cgN}, and $g_{m2} \cdot g_{m3}$ will be slightly bigger than $g_{m1} \cdot g_{m4}$. Therefore, with a small R, the loop gain would be even larger than 1. It is clear that $R \cdot g_{m2}$ is the critical factor which determines the stability of the loop. With the present design values, the resistance R must be at least 350Ω, in order to have a stable loop with gain less than 1.
A potential issue is the presence at the pad level of a parasitic capacitance, which may short high-frequency signal components to ground, decreasing the resistance at those frequencies, thus making the loop unstable [Ba, 20]. For this reason, the resistor R has been split in two components, R_{int} on-chip, and R_{ext} off-chip. The on-chip resistance has the safe value of $2.8K\Omega$; even if the external resistance is shorted to ground, this internal resistance is large enough to keep the loop stable.

The external resistance R_{ext} can assume values in the range 2-$10K\Omega$. The nominal value of $3K\Omega$ provides the appropriate current for a sampling frequency of 40MHz; in this case, the reference current I_R is $33\mu A$, and the total analog power consumption of the ADC is 32mW.

The reference voltage V_{cgP} is used to generate several biasing voltages for NMOS transistors as well as for PMOS transistors; some current mirrors, whose transistors are scaled versions of the transistors in the stage amplifiers of the ADC, generate all the needed biasing voltages. In this way, the reference current I_R is mirrored as bias current of all the analog components of the converter.

By changing the value of the external resistor R_{ext}, the user can tune the current and, as a consequence, the power consumption of the whole ADC, according to the sampling rate needed. Figure 4.10 helps finding the value of R_{ext} for a given power consumption; this dependency reflects the $1/R^2$ law of equation 4.11. Having a bias resistor off-chip can be also useful in power pulsing applications; using a switch to disconnect an external resistor, the reference current I_R can be significantly reduced, driving the ADC in a low-power state.

In the β-multiplier, the two voltages V_{cgN} and V_{cgP} in figure 4.9 could remain at ground and supply voltage, respectively; this state would be stable, without any current flowing through the two branches [Ba, 20]. In order to avoid this condition, some startup circuitry is added, which creates a low-resistance path between V_{cgN} and V_{cgP}, when these two voltages are too

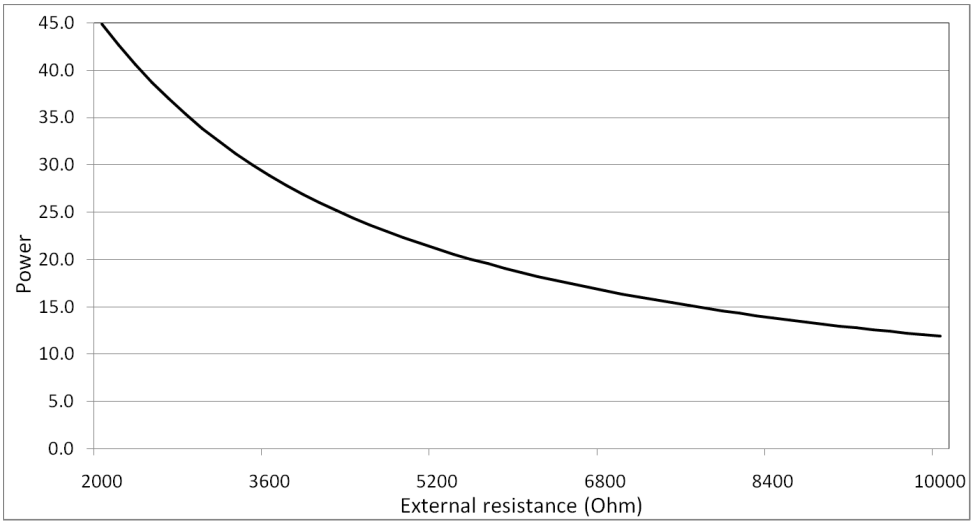

Figure 4.10: Simulation of the analog power consumption of one ADC as a function of the value of the off-chip biasing resistor.

different from each other; this is actually the case also when the off-chip bias resistor is disconnected (shutdown mode). Therefore, the simulated power consumption in shutdown mode of 1.24mW per ADC is due not only to leakage, but also to the startup circuitry for the beta multiplier.

The Super-Altro Demonstrator includes 16 ADCs. Having 16 independent biasing blocks, each one with an external resistor, would be highly impractical. Therefore, one single β-multiplier is used to provide biasing to all 16 channels; the reference V_{cgP} is routed to each individual channel, where it is used to mirror I_R into the stage amplifiers.

This poses the problem of the IR drop with one single β-multiplier. In fact, V_{cgP} is provided to 80 PMOS gates (five per channel); these gates may be leaky, and sink some current; since the V_{cgP} line travels all along the chip to reach all the 16 channels, its resistance is not negligible, and there could be a significant voltage drop, leading to a biasing current mismatch between ADC channels.
In the present design, the V_{cgP} line is 7.5mm long, and presents a resistance of 32Ω between adjacent channels, which adds up to 480Ω between the β-multiplier and the furthest current mirrors. The IR drop has been simulated, together with this value of parasitic resistance, and the results show that it does not introduce significant mismatch between ADC channels.

4.4 Digital Error Correction

In section 4.2, it has been explained that each stage along the pipeline ADC contributes with one bit to the resolution and with one bit to the redundancy of the system. The redundancy is needed in order to correct errors which take place in the comparators and are due, e.g. to noise or mismatch.

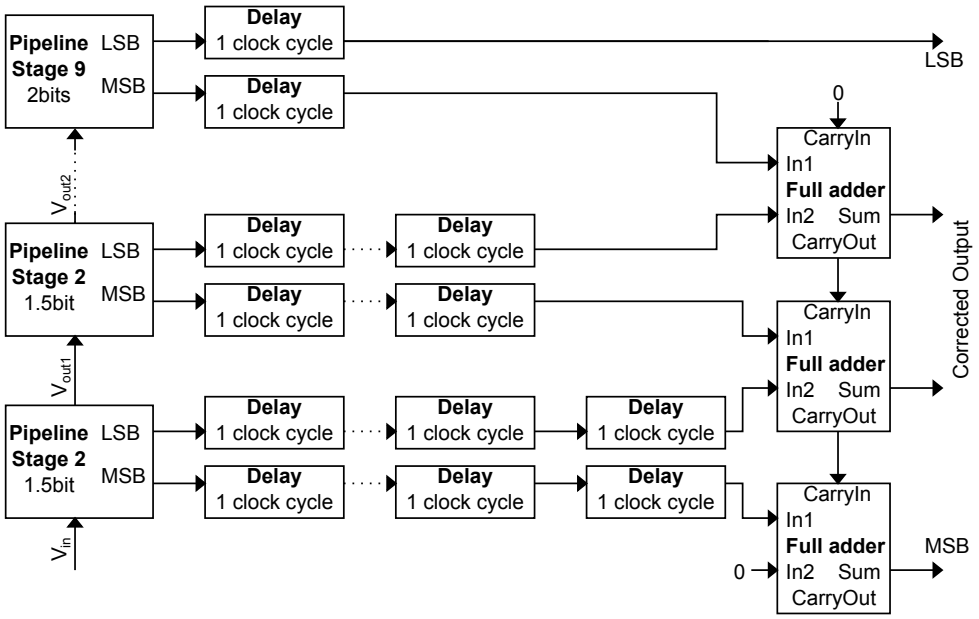

Figure 4.11: Scheme of the digital error correction logic for the ADC. The last stage is a 2bit flash ADC.

Figure 4.11 shows a simplified scheme for the implementation of the digital error correction; only the first two and the last pipelined stages are shown. This scheme takes inspiration from [CC] and [Wa].

In order to understand how this scheme works, it is worth to make two examples. We will consider the simplified case of a pipeline of three stages, as depicted in figure 4.11; the last stage is a 2-bit flash ADC, without redundancy.

Remembering the principles of the pipeline ADC discussed in section 3.3.1, we know that each pipeline stage has three possible digital output values, and the analog output will depend on the digital value according to table 4.2.

In the first example, V_{ref} is 1V and V_{in}, the analog voltage to be discretized, is 0.3V; all the pipeline stages behave correctly. In the second example, the reference and input voltages are exactly the same as in the

Input voltage V_{in}	B1	B0	V_{out}
$V_{in} < -V_{ref}/4$	0	0	$2 \cdot V_{in} + V_{ref}$
$-V_{ref}/4 < V_{in} < +V_{ref}/4$	0	1	$2 \cdot V_{in}$
$V_{in} > +V_{ref}/4$	1	0	$2 \cdot V_{in} - V_{ref}$

Table 4.2: Transfer function of each pipeline stage.

Input	First stage			Second stage			Last stage		Output
V_{in}	MSB	LSB	V_{out1}	MSB	LSB	V_{out2}	MSB	LSB	Result
0.3V	1	0	-0.4V	0	0	0.2V	1	0	1010
0.3V	0	1	0.6V	1	0	0.2V	1	0	1010

Table 4.3: Example of the error correction algorithm. In the last line, the first pipeline stage introduces an error, which is corrected by the algorithm.

first example, but this time, the first pipeline stage produces a wrong digital result. Table 4.3 shows how the correction algorithm processes the data and the final results.

In both examples, the final output result is "1010"; this algorithm can effectively use the redundancy bit of each pipeline stage, in order to correct errors.

Fig 4.12 shows the full implementation at gate level. The piece of circuitry on the upper right corner of the schematic are the buffers which distribute the clock to all the delay flip-flops (type D). These D-type flip-flops are meant to align the data coming from the different stages; as each stage operates with one clock cycle of delay from the previous stage, D flip-flops are used to ensure that all the data, which refer to the same sample of the input signal, arrive at the adders aligned in time. Each D flip-flop is clocked on the rising edge of its incoming clock signal. The buffer which receives the clock from outside is also an inverter; therefore, the whole digital correction block is clocked on the falling edge of the clock coming from the clock tree.

This design choice is compatible with the clocking scheme explained in section 4.6. It allows enough time (11.7ns) to the comparators of the first stage to take the decision. It also provides the inputs to the DSP block with a phase shift of 180° compared to the DSP sampling clock (neglecting propagation delays); therefore, this solution is very safe, because the instant when the DSP block samples the input data is well separated in time from the period when the outputs of the digital correction are switching. Most of all, this design choice lets the digital correction logic switch, and, as a con-

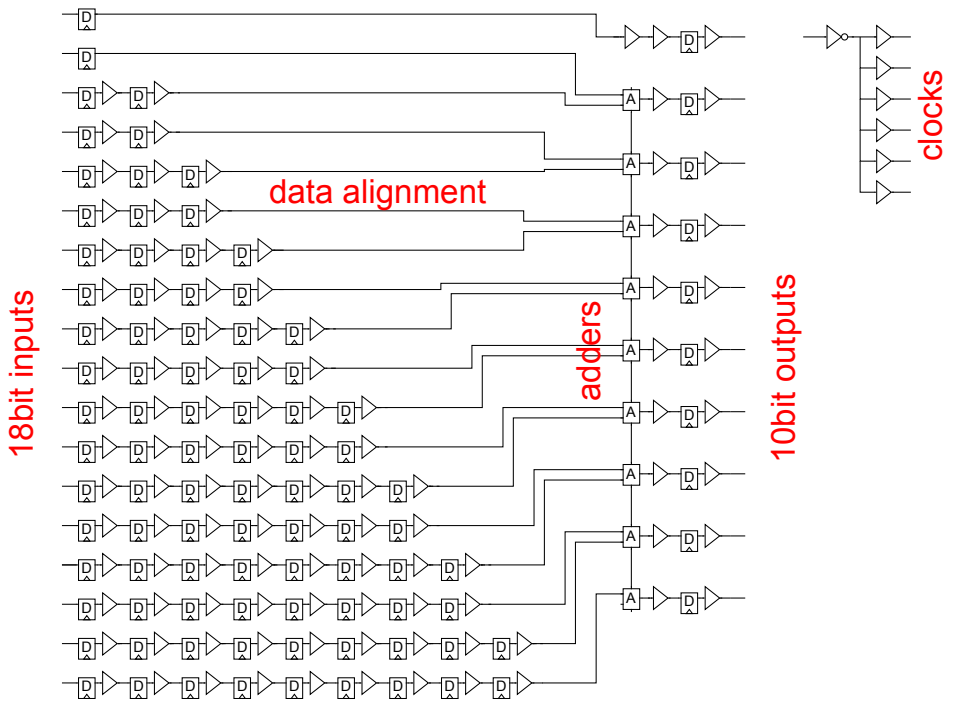

Figure 4.12: Full schematic of the digital error correction logic for the ADC. On the left-hand side, D flip-flops and buffers for the time alignment of data from different stages; on the right-hand side, the adders with D flip-flops and buffers.

sequence, produce noise, in a non-critical instant, far away from the instant when the analog inputs are sampled by the ADC stages, which is close to the rising edge of the ADC clock.

Between consecutive D flip-flops there are some buffers; their function is to delay the signal travelling from one flip-flop to the next one, in order to comply with the requirements on the setup/hold time of the receiving flip-flop. This behaviour has been simulated and verified, including parasitics, in all corner conditions and also with MonteCarlo iterations. Some D flip-flops, added to the outputs of the digital error correction, allow good alignment of the data at the output.

The digital error correction occupies an area of 130μmx145μm, located on the back-end of the ADC, close to the DSP block. As picture 4.13 shows, the clock signal has to travel all the way from the internal clock tree to the first pipeline stage; there it triggers the comparators. After that, the outputs of the comparators, buffered by the latches, travel back towards the digital error correction circuitry. Therefore, all these signals have to travel

long lines, and it is important to make sure that they have enough time to arrive at their destination before the D flip-flops of the digital error correction samples them.

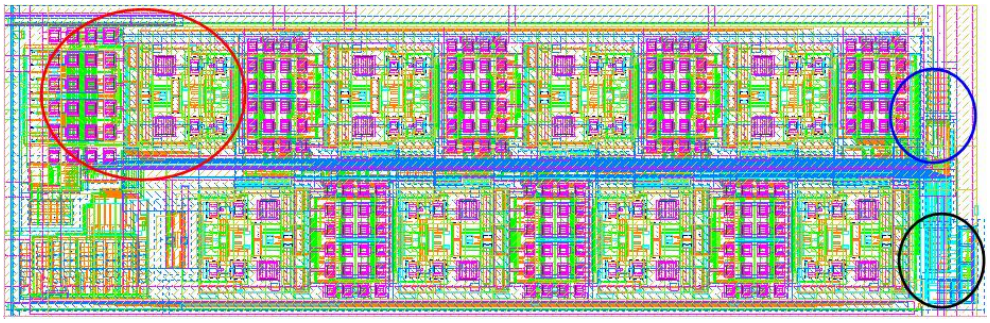

Figure 4.13: Full layout of the ADC; the horizontal size is roughly 1.5mm. The red circle marks the first pipeline stage, the blue circle marks the internal clock generator, the black circle marks the digital error correction circuitry.

The parasitics on the relevant lines have been extracted. Simulations including these parasitics give the waveforms depicted in figure 4.14. The delays of the signals along these critical lines are in the order of few hundreds picoseconds (see the red arrow in the picture); the falling edge of the clock will arrive 10.5ns later. Therefore, the choice of clocking the digital error correction on the falling edge of the clock helps, because it allows enough time for the most critical signals to travel all across the ADC.

Also for the digital error correction block, a Verilog-AMS model has been developed. Simulations, like the one shown in figure 4.15, have been run with arbitrary input pulses. The Verilog-AMS model has the same behaviour as the schematic/extracted model. Moreover, the correctness of the output data has been checked: the sampled analog signal is converted to the correct digital word after the expected latency of 9.5 clock cycles.

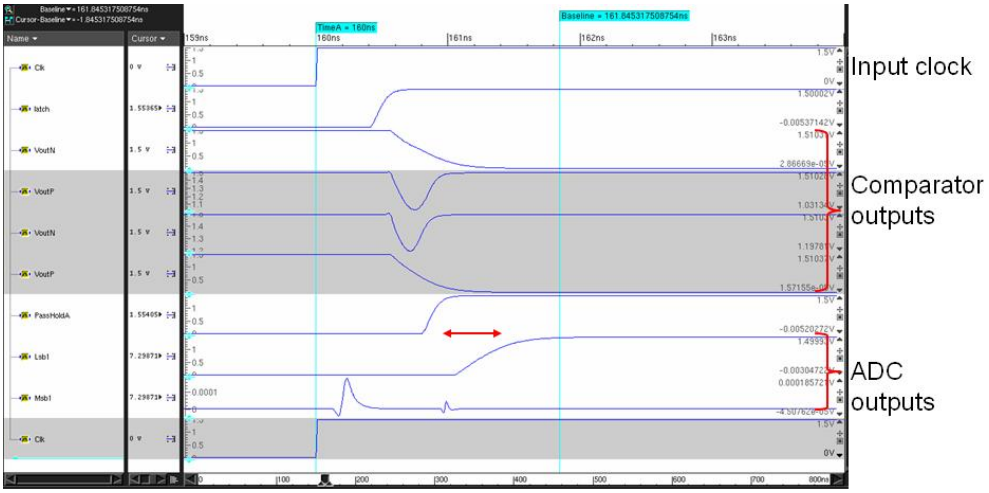

Figure 4.14: Propagation delays between the components marked in figure 4.13. The first line shows the clock arriving to the internal clock generator; the second line shows the clock arriving to the first pipeline stage; the following four lines are the outputs of the two comparators of the first pipeline stage. The lines denominated "Lsb1" and "Msb1" are the bit signals which come back from the first pipeline stage to the digital error correction.

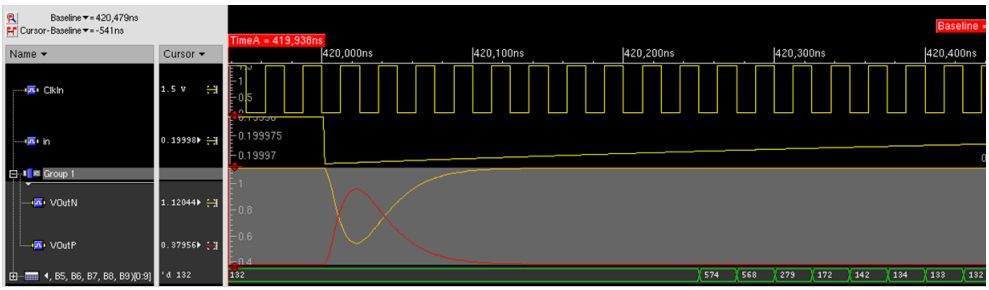

Figure 4.15: Verilog-AMS simulation of one channel, including PASA, ADC and digital error correction. The first line is the sampling clock. The second line is the input of the PASA, while the third line shows the two single-ended outputs of the PASA. The last line shows the decimal value of the digital word corresponding to the sampled output of the PASA.

4.5 Digital Signal Processing block

The Digital Signal Processing (DSP) is performed by the blocks shown in diagram 4.16. It was developed in [GG], on the basis of the DSP of the ALTRO chip [Bl]. Each block has a task which corresponds to a feature of the signal generated by the detector.

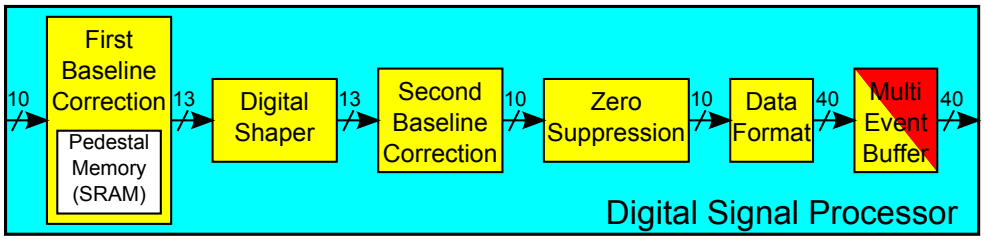

Figure 4.16: Diagram of the Digital Signal Processing block. The yellow blocks run with the sampling clock, while the red color corresponds to logic running with the readout clock [GB].

Also the logic which is shared among all 16 channels (figure 4.1) is described later on in this section (4.5.1).

First Baseline Correction BC1

The 10bit signal coming from the ADC has a baseline; the first Baseline Correction (BC1) can remove this baseline by subtracting a pedestal value. The pedestal value can be either fixed, i.e. determined by the user and saved in a register, or variable; the variable value is calculated by the BC1, using an Infinite Impulse Response (IIR) filter, whose time response can be adjusted by setting a dedicated register. The IIR filter is only active outside the acquisition window (before Level-1 trigger, see 4.5.1) and when there is no pulse (some programmable thresholds define whether a sample is to be considered baseline or a pulse), so that it does not affect the shape of a potentially interesting pulse.

This feature of the BC1 is useful for the correction of slow variations of the baseline due, e.g., to a temperature drift.

Another functionality is to remove the systematic patterns that can be introduced, for example, by the switching of the gating grid of the detector (paragraph 1.1.1). In order to do this, a Pedestal Memory (PMEM) is used to store some pre-defined values of the baseline, which are subtracted from the data stream from the ADC. The size of the PMEM is 1000 x 10bits (1.25Kbyte), which is sufficient to subtract a value from each subsequent data sample of a maximum-duration acquisition (maximum 1000 samples).

During tests, the PMEM is also used to store a known pattern, which can be processed by the rest of the DSP chain. This allows independent testing of each DSP block, without influence from the analog part of the S-Altro (without analog noise).

Tail Cancellation Filter (Digital Shaper DS)

The task of the Digital Shaper (DS) is to compensate the distortion of the signal shape due, for example, to long ion tails in the detector (in the case of MWPC).

The DS is an IIR filter derived from an analog transfer function [GB]: eight programmable filter coefficients determine the positions of up to four poles and four zeros in the transfer function; the filter is implemented as a cascade of four first order filters. With appropriate values of the filter coefficients, it is possible either to remove the tail, or the undershoot from the incoming pulses.

Second Baseline Correction BC2

The Second Baseline Correction (BC2) reduces non-systematic baseline movements, and uses a Moving Average Filter (MAF). The MAF is a Finite Impulse Response filter (FIR) filter; it computes the average of the last two, four or eight samples (decided through a programmable register). The user can set some parameters which define a higher and a lower threshold, that the MAF uses to exclude from the average the samples which correspond to a pulse.

The function of the BC2 is to correct faster (with respect to BC1) variations of the baseline occurring within the acquisition window. These variations may originate, for example, from variations of the supply voltages.

Zero Suppression, Data Formatting and Multi-Event Buffer

Once the systematic patterns, the distortions and the variations of the baseline have been removed, the Zero Suppression unit (ZS) removes the samples below a programmable threshold; this allows to save in the memories only the relevant pulses, removing all the baseline samples, thus decreasing drastically the amount of data to be sent off-chip, the required communication bandwidth, and the system dead time due to read out. The ZS includes a glitch filter, which removes the pulses shorter than a programmable number of samples (which are probably a glitch, rather than a real pulse); additionally, a programmable number of samples before and after the pulse are saved, in order to keep some useful information on the baseline.

The Data Formatting (DF) unit converts the 10bit data flow in a 40bit data format, including a header and a trailer, which carry some important information, like the time stamp of each pulse.

The Multi-Event Buffer (MEB) is a memory, where the data are stored during the acquisition. Their importance is also due to the fact, that they allow read out of the data after the end of the acquisition window; therefore, the noise-generating read out activity is postponed to a time interval, when noise is not crucial, as will be explained in 4.8.1. As the data are saved in 40bit format, while the ADC provides data in 10bit samples, the writing on the memory is performed every fourth clock cycle. The size of the memories (40Kbit=5Kbyte) allows saving four 1000-samples acquisitions or eight 500-samples acquisitions, depending on the programmable number of memory partitions (either 4 or 8).

4.5.1 Interface and system timing

Picture 4.1 shows that a part of the logic is shared among all 16 channels; this part implements the communication between the DSP block and the off-chip components. This communication is based on 40 data lines and 12 control lines; the logic family used is CMOS at 2.5V of supply voltage.

The 40bits bus is bidirectional, so that it can be used for the readout of the data in the MEBs, as well as for writing and reading the configuration registers. The control lines are used for the resets of the chip, for the determination of the direction of the communication, for the acknowledge of packets during data transfer, and for the triggers.

The structure of the acquisitions with the S-Altro is based on two trigger levels: the first level trigger (L1) starts the data acquisition, and therefore determines the start of the acquisition window, while the second level trigger (L2) validates the data from the previous L1. In case a L1 trigger is followed by another L1, without its L2 validation, a new acquisition is started and the data from the previous acquisition are lost: inside the chip, the L2 trigger moves the write pointer to the next partition of the MEB; therefore, without L2, the next L1 trigger will cause the new data to overwrite the previous data in the same memory partition.

In the Alice TPC, the maximum drift time along the 2.5m of drift region is 88μsec, and the maximum trigger rate is 200Hz for Pb-Pb collisions [AL2]. Therefore, the S-Altro can acquire the signal for 100μsec after receiving the L1 trigger (acquisition window); this corresponds to 1000 non zero-suppressed samples at 10MHz sampling frequency, which is also the size of one partition of the MEB. The L2 trigger arrives after all charges arrived to the TPC pad.

Moreover, since the total memory of the MEBs in one S-Altro is 80Kbyte,

to be read out up to 200 times per second, the readout can take a significant amount of time, which increases the dead time of the system. This is the reason why the readout clock has a maximum frequency of 80MHz, which leads to a read-out time of 0.2ms for the whole chip.

As shown in figure 4.17, during the acquisition window, the S-Altro introduces a latency between one sampling and the storage of that sample in the MEB; the latency depends on the amount of digital functionalities enabled.

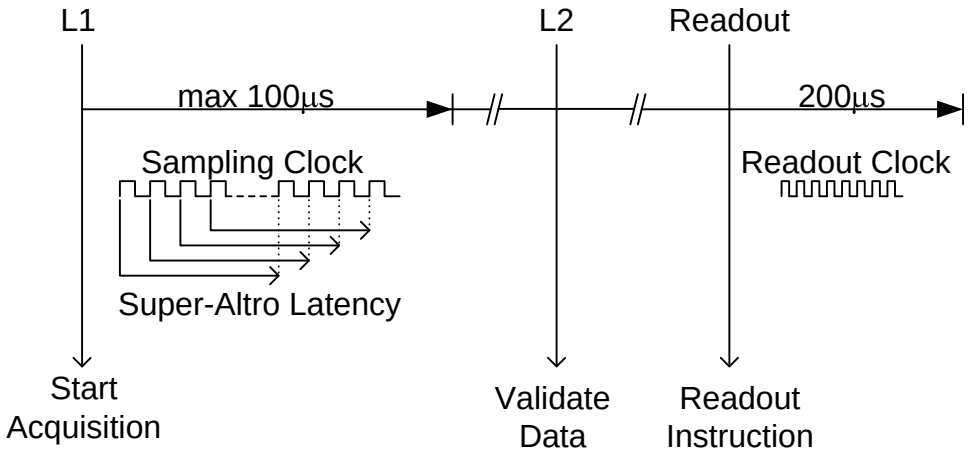

Figure 4.17: Timing diagram of the whole system, showing data processing for a maximum of 100μsec after the L1 trigger, L2 trigger, and a readout instruction sent to the S-Altro, which takes 200μsec to transfer the full contents of the memories.

4.6 Timing and clock tree

The input clock of the S-Altro is propagated by a clock tree to the stack of sixteen ADCs and to the Digital Signal Processing block. Figure 4.18 and table 4.4 help understanding the ADC internal clock and the flow of the clocked signals into the digital error correction and the DSP block; some considerations are necessary in order to understand the design of the clock tree:

1. The timing of the ADC is controlled by the internal clock generator introduced in section 4.2 (each channel ADC has its own clock generator). The analog input of the first ADC stage is not buffered by a Sample-and-Hold (S/H); therefore, the first stage has dedicated clocks,

for particular requirements. The other "regular" ADC stages are operated in double sampling mode, and have two sets of clocks which distinguish between odd and even samples. The most relevant features of the clock generator are:

(a) The bottom plate sampling of the first stage is done at each clock cycle, while for the regular stages, it is done in an interleaved fashion.

(b) The trigger for the comparators is done close to the sampling instant for the first stage, and in the middle of the sampling phase for the regular stages. In regular stages, the analog input looks like a low-pass step response; the error introduced by the comparison taking place before the end of the settling time of the previous stage is negligible.

(c) Since the comparators are reset at each clock cycle, some latches define the time window when their outputs are valid; this corresponds to the time when the outputs of the ADC core are allowed to switch.

2. The digital error correction must sample the outputs of the ADC core when they are not switching, and provide outputs which are stable when the DSP is sampling them.

3. The DSP block can be clocked with a time-shifted clock, with respect to the ADC [Bl]. Some points are important:

(a) The DSP has an internal clock tree, which introduces an additional delay between its incoming clock and the instant when the logic elements start switching.

(b) The sampling of the incoming data from the digital error correction happens when the clock arrives to these logic elements.

(c) The switching of the logic has variable duration, according to the operations required to the DSP; its noise contribution must be taken into account.

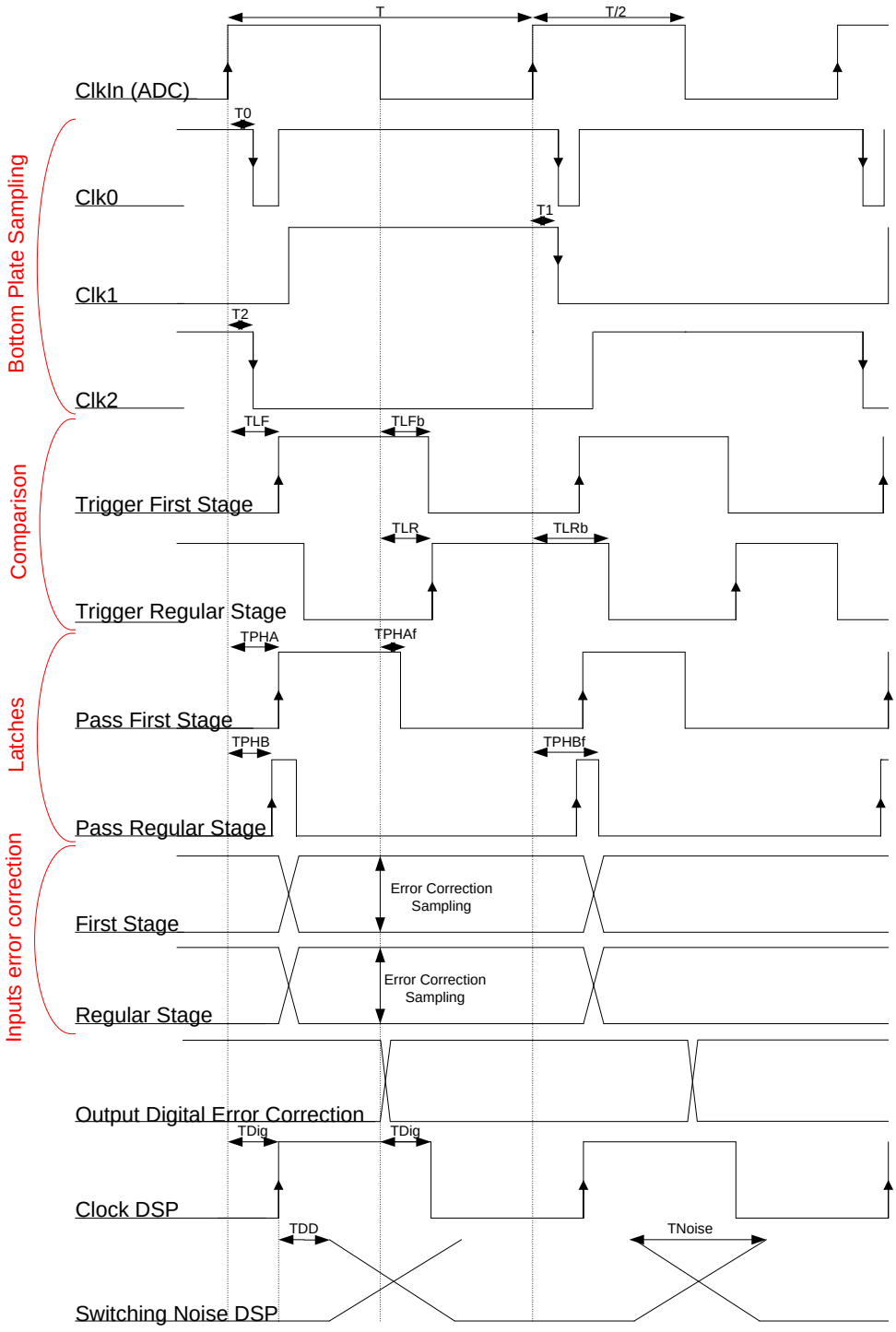

Figure 4.18: Complete timing diagram of the S-Altro; table 4.4 explains the functions of the depicted signals. The first line is the clock input of the ADC,

and is used as a reference for the timing of all the other signals. This diagram shows that the outputs of the ADC core flow with good timing through the digital error correction, and are then correctly sampled by the digital block; moreover, the noise introduced by the DSP functions is positioned after the bottom plate sampling, which is the most noise-sensitive instant in the operation of the ADC.

The switching of the logic in the DSP can last up to 12.8nsec. For noise reduction reasons, the clock must arrive to the DSP with such a timing, that this switching takes place far from the bottom plate sampling, which is the most noise-sensitive time for the ADC. With a 25ns clock period, this condition can be satisfied by clocking the DSP with a short delay after the ADC; this allows the sampling to happen at the end of a relatively quiet period, when the MDACs have some time margin to settle to the appropriate values, without noise being added from the DSP. This is shown clearly in a simplified version of the clocking scheme, depicted in the appendix C.

On the other hand, the decision has been taken, to clock the digital error correction on the falling edge of the clock. As explained in section 4.4, this solution guarantees that the data are stable when they are sampled at the interfaces ADC / error correction and error correction / DSP. Moreover, the noise produced by the switching error correction is concentrated quite far from the ADC sampling instant.

The correctness of the timing between the different blocks has been proven, as explained in section 4.9.

The task of the clock tree is to deliver the clock to the different ADC channels simultaneously, ie with reasonably low skew, and to the DSP, with a delay, as was done in the ALTRO chip [Bl]. The schematic of the designed clock tree is shown in figure 4.19, while table 4.5 reports the delays between the input clock of the S-Altro and the clock propagated to the ADCs and to the DSP; the nominal delay of the DSP clock has been chosen of 600ps.

The structure of the clock tree is fully symmetrical in schematic, as well as in layout. The S-Altro input clock is routed to the physical center of the clock tree, from where the ADC and the DSP branches start; the ADC branch is split four times, and each splitting produces two symmetrical branches. Thanks to this symmetry, the paths between the main clock and each ADC are equal in length; simulations, including the extracted parasitics, give a negligible clock skew of 2ps between different ADC channels. Figure 4.20 plots the simulated delays between the three clocks (input, ADC, and DSP).

The Verilog-AMS model of the clock tree is vital for the top-level simulations, because it contains the information on the timing between the different blocks, and determines, therefore, whether the data will flow smoothly

Signal name	Function	Delay	
ClkIn	Clock of the ADC	T	25ns
Clk0	Falling edge: bottom plate sampling of the first stage	T0	190ps
Clk1	Falling edge: bottom plate sampling, regular stages (every 50ns)	T1	190ps
Clk2	Falling edge: bottom plate sampling, regular stages (every 50ns)	T2	190ps
Trigger First Stage	Rising edge: triggers the comparators of the first stage	TLF	441ps
		TLFb	660ps
Trigger Regular Stage	Rising edge: triggers the comparators of the regular stages	TLR	750ps
		TLRb	1460ps
Pass First Stage	High: enables latches of the first stage to pass the outputs of the comparators forward	TPHA	770ps
		TPHAf	380ps
Pass Regular Stage	High: enables latches of the regular stages to pass the outputs of the comparators forward	TPHB	720ps
		TPHBf	1350ps
Clock DSP	Delay from ADC clock	TDig	590ps
Switching Noise DSP	Delay from Clock DSP	TDD	1995ns
	Duration of switching	TNoise	12.8ns

Table 4.4: Meaning of the clock signals shown in figure 4.18, with the associated delays.

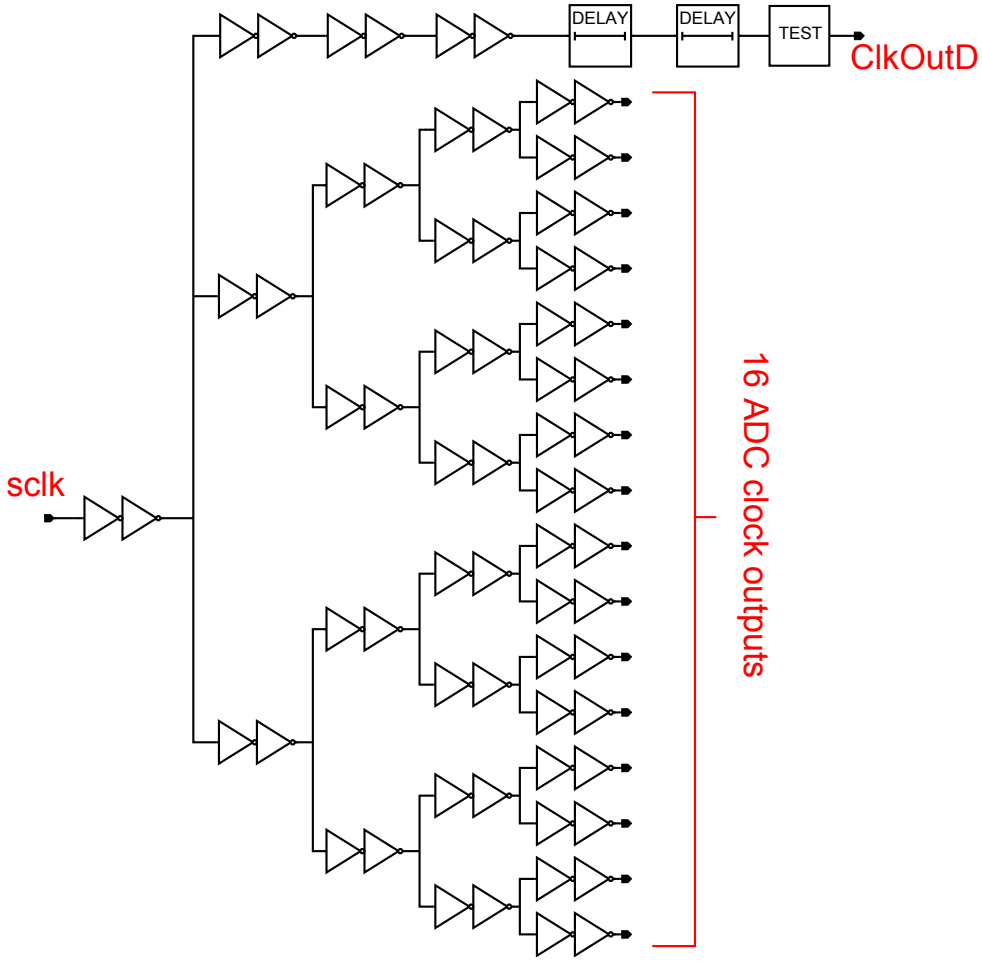

Figure 4.19: Schematic of the clock tree.

through the pipeline PASA-ADC-DSP. Analog simulations have been run, taking in consideration process, voltage and temperature corner variations; the simulated values of the delays, reported in table 4.5, have been used in the Verilog-AMS model of the clock tree. The model is a buffer, which replicates 17 times the input clock (for the 16 ADCs and for the DSP), including the appropriate set of delays, according to the corner that has to be simulated. The model is copied in the appendix B.3, and included in the simulation of figure 4.34.

Corner	Clock ADC	Clock DSP
Typical	540ps	1130ps
Fast	350ps	670ps
Slow	840ps	1830ps

Table 4.5: Delays between the S-Altro external clock and the internal clocks propagated by the clock tree; the simulations take into account process, supply voltage and temperature variations, producing fast, typical and slow values of the delays.

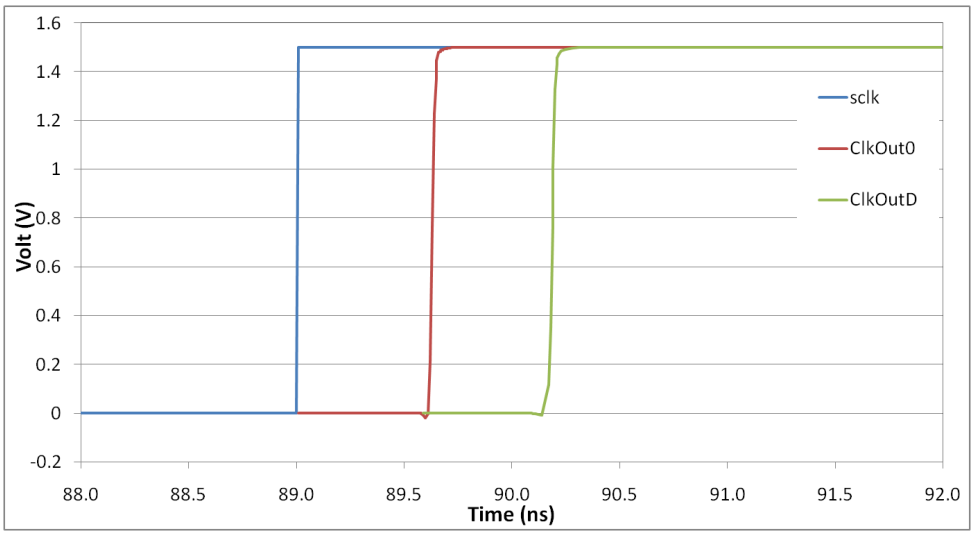

Figure 4.20: Simulation of the clock delays introduced by the clock tree: the clock for the ADC is delayed by 540ps, while the clock for the digital block is delayed by 1130ps, with respect to the incoming sampling clock. The parasitic capacitances and resistances extracted from the layout are included in the simulation netlist.

4.7 Testability

Since the S-Altro is a demonstrator chip, it is important to have testing features which allow debugging and optimizations. The main testing features of the chip are:

Test mode of channel 15: possibility of opening the signal lines between PASA and ADC, and testing the two components independently.

Clock tree: possibility of delivering two independent clocks to ADCs and DSP block; possibility of shutdown of one or both clock branches.

Auxiliary inputs: off-chip signals are used as inputs of the DSP block.

Test mode "TSM" of the DSP block: the DSP is completely disabled and the output of the selected ADCs flow directly into the 40-bit bidirectional bus.

In channel 15, some analog switches have been added at the output nodes of the PASA and the input nodes of the ADC, as shown in figure 4.21. These switches are controlled by an external signal named "TestMode"; when this signal is asserted, the switches open the connection between PASA and ADC, and send the outputs of the PASA off-chip, while the inputs of the ADC come from two other I/O pads. This structure allows independent testing of PASA and ADC; in particular, it allows testing one component at a time, even with the other component left without power supply. This can be particularly useful during tests, in order to isolate different noise sources (e.g. the noise on the PASA due to the operation of the ADC). The switches used have an ON resistance in the order of 8Ω in the relevant voltage range 250-1250mV; this introduces a reasonably small resistance, in series with the 33Ω resistance of the input switches of the ADC.

As explained in section 4.6, the clock is delivered to the DSP block with a delay of 590ps (typical), as compared to the clocks delivered to the ADCs. This delay should be optimal for the operation of the S-Altro; nevertheless, it is interesting to know how the performance of the chip varies with a different delay. For this reason, the clock tree in figure 4.19 includes the test feature depicted in figure 4.22. When the control signal "ClkSelect" is asserted, the secondary clock input "ClkAux" is delivered to the DSP block. In this way, the relative phase shift between "sclk" and "ClkAux" can be changed externally; therefore, a full scan of the phase shift can be implemented, and the performance of the chip with different delays of the DSP clock can be measured.
Moreover, this feature can be used to disable either the ADC clocks or the

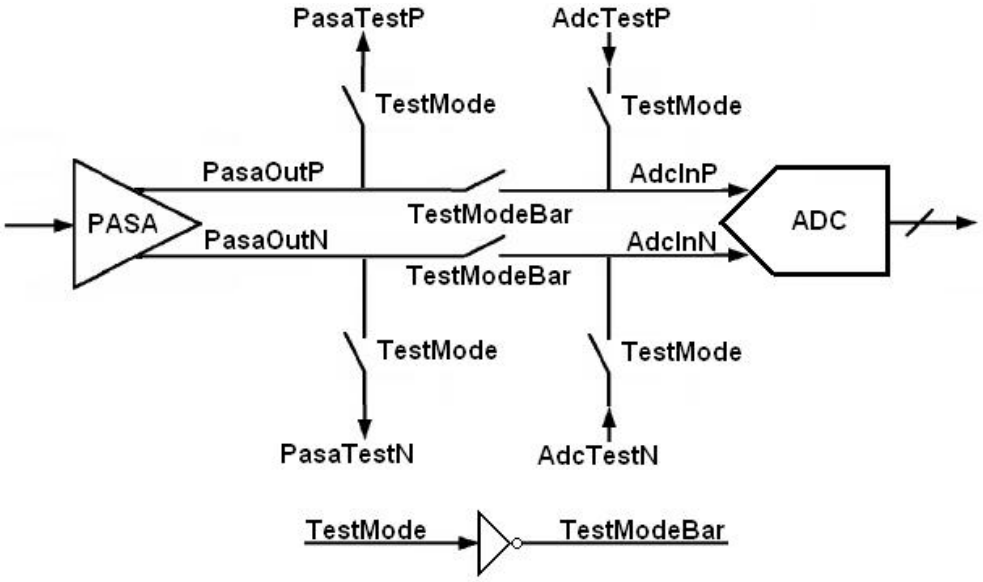

Figure 4.21: The external signal "TestMode" sets the state of the switches in channel 15. Either the PASA and ADC are normally connected, or the signal lines are open, and the outputs of the PASA and the inputs of the ADC are connected to I/O pads for testing purposes.

DSP clock. This can be useful when doing power pulsing tests, in order to avoid the dynamic power consumption of the DSP block during the shutdown phase.

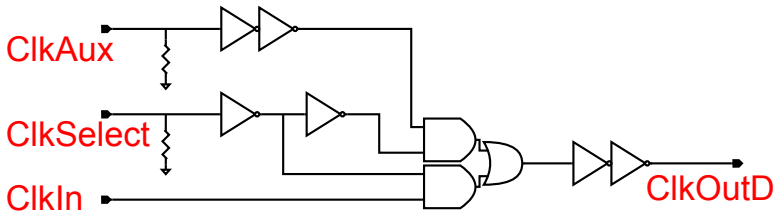

Figure 4.22: The clock tree includes the possibility of delivering an independent clock to the DSP block.

In the case that the DSP has to be tested independently, ten auxiliary digital inputs are available and selected by a control signal named "ConfigIn". When using this testing feature, the auxiliary inputs replace the ADCs as inputs of the DSP block; the same ten bits are sent to all sixteen channels in parallel.

Another useful possibility for testing is by asserting the "TSM" control signal. In this case, the DSP is disabled and the outputs of selected ADCs are buffered directly into the 40 bit bidirectional bus. Since 40 bits cannot carry all the outputs of 16 ADCs, the ADCs are masked in four groups; using two control lines, the user can select which group of ADCs are to be connected to the output buffers.

4.8 Floorplan and layout

The sizes of the PASA and the ADC are 200μmx100μm and 500μmx1500μm, respectively. Following these given sizes, several floorplanning options have been investigated; the three main ideas are shown in pictures 4.23, 4.24 and 4.25.

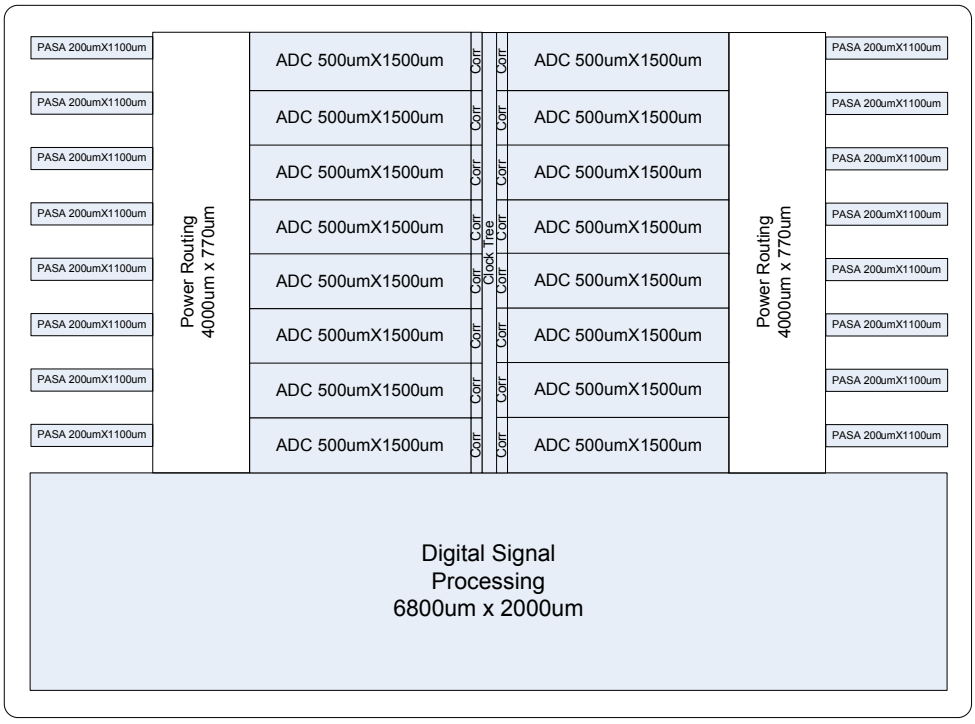

Figure 4.23: Floorplan with PASA and ADC on west and east sides, with digital part on the south side.

In figure 4.23, the PASAs are distributed on two opposite sides (left and right). The limiting factor of this floorplan is the aspect ratio of the chip: placing the digital part in between the two columns of PASAs/ADCs would

make the width too large in comparison to the height; the digital functions must therefore be implemented in the third side of the chip (bottom).

This floorplan has some drawbacks related to the asymmetry: the lower PASAs would be more influenced by the digital part than the upper ones (the coupling between analog and digital components will be explained in 4.8.1). Moreover, the propagation delays of the clocks and of the outputs of the ADCs would depend on the non-uniform distance between the channel and the digital block; this could create some timing issues and also makes the verification of the full chip more difficult.

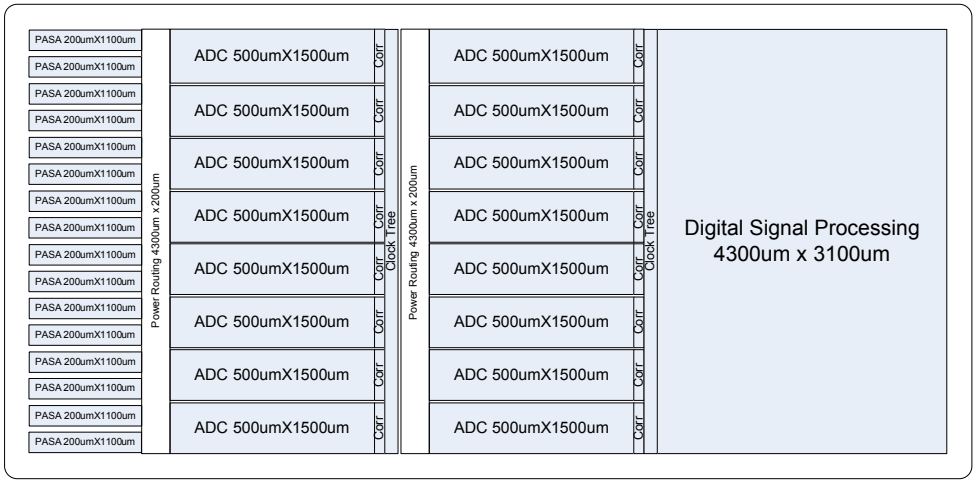

Figure 4.24: Floorplan with all PASAs on the west side, the ADCs distributed in two columns, and the DSP block on the east side.

The floorplan shown in figure 4.24 was thought in order to partially overcome the limitation of the aspect ratio. It has the advantage that little space is left between adjacent PASAs, thus saving area. The drawback is that the analog outputs of eight PASAs have to travel all along the first column of ADCs before crossing the digital outputs of those ADCs and then reaching the inputs of the second column of ADCs: this introduces big signal integrity issues, and also makes clean separation of different supply domains impossible. Following these considerations, this floorplan has been discarded.

The chosen floorplan is shown in figure 4.25. The aspect ratio of the chip is roughly 1.5, which is acceptable. Each channel is equal and the delays associated are ideally equal; only the clock tree introduces some skew between different channels, but this has proven negligible using an appropriate layout, as explained in section 4.6. The supply domains can be fully separated, thus minimizing the coupling between different grounds and supply rails.

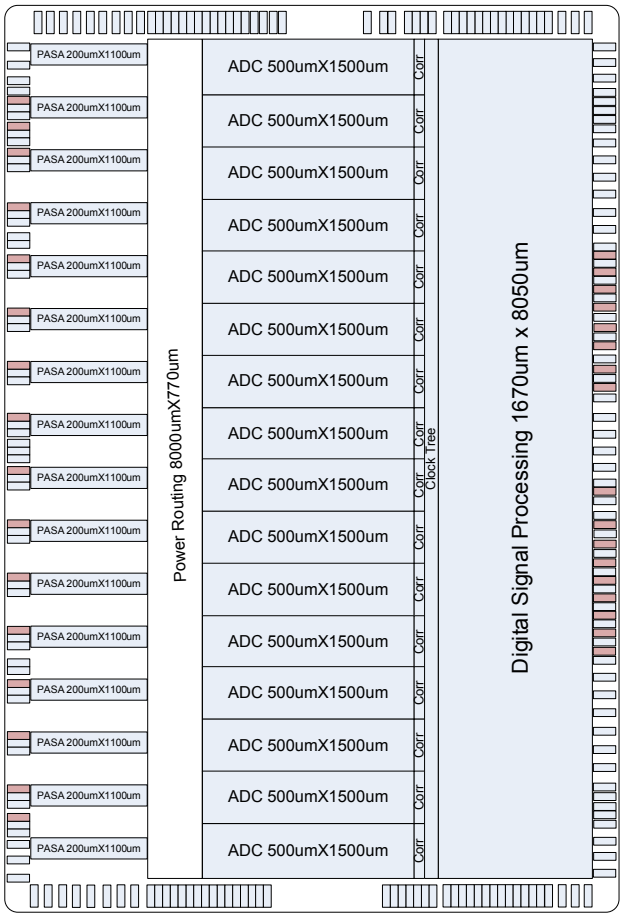

Figure 4.25: Final floorplan of the S-Altro Demonstrator. Also the pads are shown; the pads in brownish colour do not need to be bonded, when using a package with 208 pins.

The analog signals can be routed without crossing any digital signals. The drawback is that, due to the pitch of PASA and ADC, a large area is left between consecutive PASAs. Also, the ADCs in the middle of the chip are far from the edges of the chip, and therefore need wide metal connections to the ground/supply pads, in order to keep IR drop at an acceptable level, as explained later in this section.

Routing of voltage supplies and ground

The supply current for the PASA can be distributed above the PASA itself using the top metal layers.

The ADC stages are distributed in two rows. The analog power is routed over the stages, while the digital power is delivered using the horizontal space between the two rows. This makes the vertical distribution of the analog power to the 16 channels over the ADCs impossible; therefore the ADC analog power has to be routed in a dedicated space between PASA and ADC.
Since the analog power consumption is 36mW per channel, the power routing is designed with the large width of 770μm, which allows a voltage supply drop in the middle of the chip lower than 10mV. The time profile of the supply current of one ADC channel is plotted in figure 4.26.

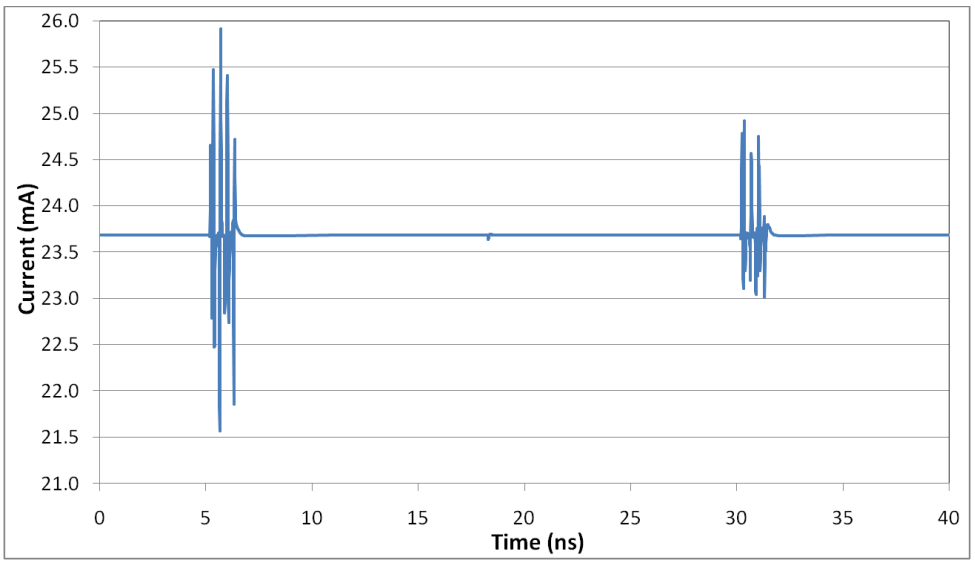

Figure 4.26: Time profile of the analog current consumption of one ADC, largely dominated by the DC component. With an external biasing resistor of 3kΩ, the power consumption will be 36mW; in shutdown mode, the power will reduce to 1.24mW.

Figure 4.27 shows the transient current consumption from the ADC digital voltage supply of one single ADC. Integrating this waveform, it is possible to calculate the power consumption: at the nominal sampling frequency of 40MHz, one ADC core consumes 0.58mW, while the error correction consumes 0.18mW.
With these values of the supply current for the digital part of the ADC, its ADC digital power routing is designed 130μm wide.

If the clock is removed, the power consumption reduces to 3.2μW for the ADC digital core and 1.2μW for the error correction. This values are interesting when operating the S-Altro with power pulsing.

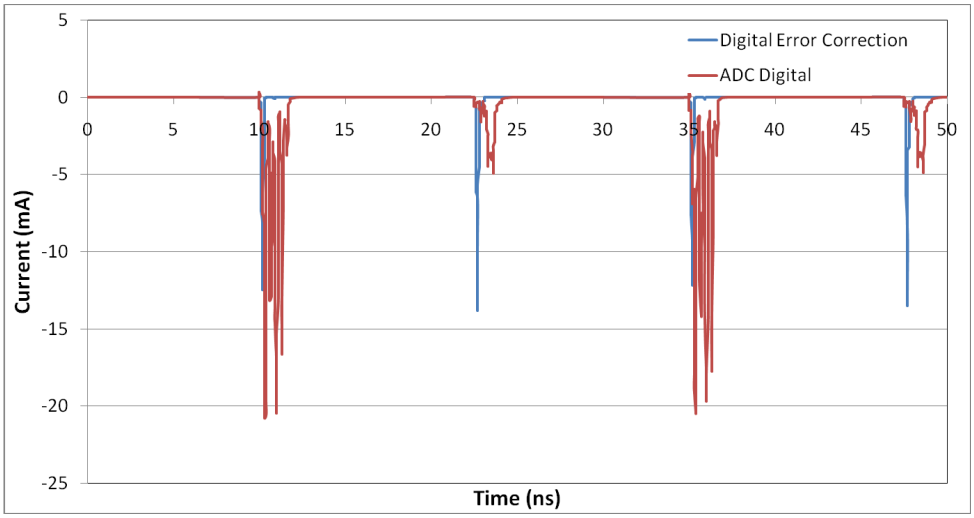

Figure 4.27: Time profile of the ADC Digital current consumption. In red is the ADC digital part, including the internal clock generation, while in blue is the digital error correction.

The area taken by the routing of the power lines is large, and this can be turned into an advantage: the top metals can be used for the power and ground rails, the intermediate metals for low-resistance routing of the ADC reference voltages (V_{ref+}, V_{ref-}, V_{cm} and V_{CmOut}), while the lower metals connect all these voltages to decoupling capacitors on the substrate. The decoupling capacitances are:

- 600pF per channel for the PASA between Supply and Ground.
- 600pF per channel for the ADC between Analog Supply and Ground.
- 40pF per channel for each reference voltage of the ADC towards the ADC Analog Ground.
- 80pF per channel for the ADC between Digital Supply and Ground.

Figure 4.28 shows the distribution of these capacitors in one Front-End (PASA+ADC) channel.

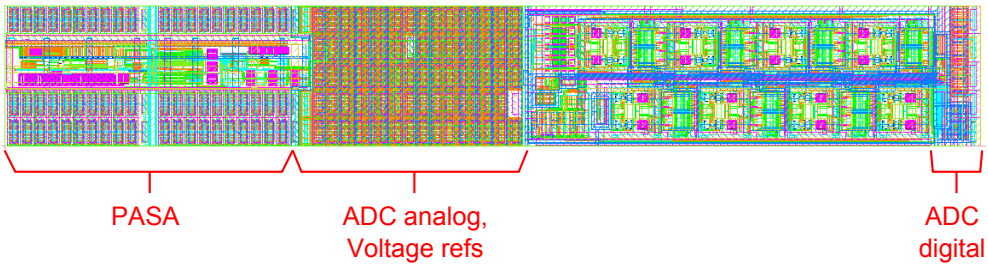

Figure 4.28: Power routing and decoupling capacitors in one Front-End channel.

4.8.1 Noise coupling, power domains and substrate isolation

A critical issue, when designing mixed-signal chips, is noise coupling between analog and digital parts.
In the S-Altro, the most sensitive analog node is the input of the PASA; a small charge injected into that node is amplified by the large gain of the whole PASA. It is possible to obtain a rough estimate of the attenuation needed from the digital transistors to the input of the PASA: digital signals have a swing of 1.5V, while on the input of the PASA, a pulse of $\approx 20\mu$V produces, on a 5pF capacitance, a charge of 0.1fC, which is of the same order of magnitude of the intrinsic noise introduced by PASA and ADC. Therefore, from 1.5V to 20μV, the attenuation needed is of 90-100dB.

Designers commonly use several techniques to tackle the generation of non-random noise and its propagation. This paragraph presents some of these techniques, used in the S-Altro. The literature offers studies of this type in [Sc] [Vi] [BK].

Analog components employ constant currents, or currents which vary lightly and smoothly with time; an example is the current consumption of the PASA during a transient event, as shown in figure 4.8. On the other hand, currents in digital components are characterized by sharp rising and falling edges, localised in discrete time windows, typically when the clock signal arrives or when one of the inputs changes state; figure 4.27 gives an example of currents in the digital domain.

The supply lines on chip present some impedance, as well as the bonding wires used to connect the chip with the external world. Therefore, digital current spikes convert into voltage spikes. If analog and digital share the same supply lines, these spikes enter into the source contacts of current sinks

and current mirrors, thus generating noise on analog signals, due to the finite Power Supply Rejection Ratio of analog circuits. It is clear that analog designs should be differential as much as possible. For example, the second shaper in the PASA and the whole ADC are differential, and this reduces their sensitivity to common-mode noise.

Anyhow, the primary isolation technique is to divide electrically the chip in power domains. The domains are defined according to the voltage supply, the type of noise that they generate (smooth analog or spiky digital) and their noise sensitivity. A separate supply is used for each domain.

The supply lines on-chip must be wide, in order to reduce voltage spikes caused by their finite resistance, as done in the S-Altro for the ADC Analog supply lines. The supplies must also be decoupled by on-chip capacitors; the charge needed by the circuitry is then provided locally by the decoupling capacitors, rather than having current spikes flowing through the whole chip and the bonding wires.

Another issue is that metal lines are affected by metal-to-metal stray capacitances. When the voltage in a metal line changes quickly, the neighbouring lines will also see a signal due to capacitive coupling. This effect is called crosstalk and it happens on supply lines as well as on signal lines; it is seen also between metal lines and the substrate, due to the interconnect capacitance.

Therefore, the domains are also a geometrical division of the chip. All supply lines corresponding to the same domain are distributed in the same region, without overlaps with the neighbouring domains. The signals belonging to the same domain are also routed together, avoiding, as much as possible, crossing of signal lines of different domains.

The metal layer on which signal and supply lines are routed is chosen carefully. The lower the metal layer used, the higher the capacitance to the substrate. Critical lines are routed on higher metal levels, and kept at some distance from other lines. For example, the outputs of the PASA are routed to the ADC using a high metal layer, so that they are not too sensitive to noise in the substrate or in the underlying metal lines; similarly, the clocks in the clock distribution have been routed in high metal levels to avoid injecting a lot of noise into the substrate.

The Super-Altro Demonstrator has been divided into five separated power domains:

PASA: analog power domain of the PASA; nominal supply voltage 1.5V.

ADC analog: power domain of the analog part of the ADC; nominal supply voltage 1.5V.

ADC digital: power domain of the digital part of the ADC and of the clock tree; nominal supply voltage 1.5V.

DSP: digital power domain of the Digital Signal Processing block; nominal supply voltage 1.5V.

Pads: power domain of the digital pads; nominal supply voltage 2.5V.

Each power domain includes, obviously, one ground and one supply rail. In addition, one more ground named "GndChipGuardRing" is needed to bias the chip guard-ring; this implant surrounds the whole chip area and is required for wafer processing reasons.

Figure 4.29 shows how these power domains are distributed at the silicon level. Also the pads are grouped together, according to their domain.
One note on the placement of digital pads [GG]: pads with high toggle rate are placed along the right-hand side, far from ADC and PASA domains; also digital power pads are kept far from the most sensitive parts, while static pads (e.g. the ones for the chip address) are closer.

So far the noise coupling through metal lines has been discussed. Once the power domains have been designed properly, substrate issues have to be considered.

Noisy lines inject noise into the substrate. A noisy ground generates currents into and out of its substrate contacts; a noisy positive voltage supply changes the biasing of the N-wells, and, as a consequence, the amount of charge at the N-well/substrate junction; every time a voltage changes in a junction (e.g. the drain of a MOS transistor), some charge is injected or extracted from the bulk.

Switching transistors, including analog switches, require bunches of charge to populate or leave the channel region; these charges are sourced or sunk by the bulk of the transistor, and can originate currents across the substrate. This issue is particularly severe in the S-Altro, because the logic family used is CMOS: since the digital voltage levels are widely spaced (supply and ground), the amount of channel charge in each transistor is maximized. Impact ionization in the transistor channel is relevant, because it also creates carriers which can travel through the substrate.

Currents in the substrate introduce noise in the analog domain also by changing the voltage in the bulk of transistors, through body effect.

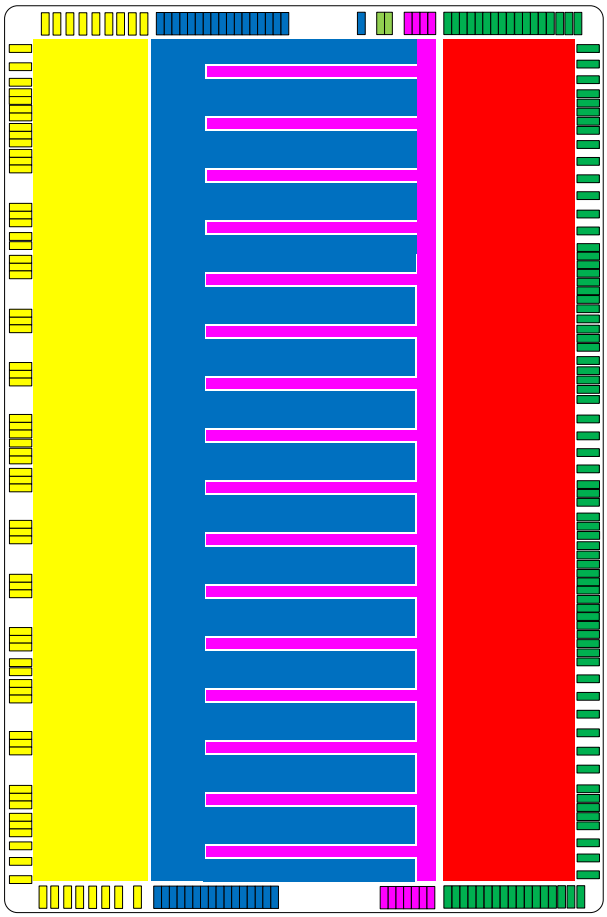

Figure 4.29: Power domains of the S-Altro Demonstrator. The PASA domain is yellow, the ADC analog domain is blue, the ADC digital domain is purple, the DSP domain is red, the pads domain is green, and the domain of the chip guard-ring is light green.

When designing a chip, the switching activities must be kept to a minimum and concentrated in non-critical time intervals. For this reason, in the S-Altro, the clock tree delays the clock to the digital block (section 4.6), and the readout of the memories is done outside the acquisition window, when noise is not a concern (interesting data arrive only within the acquisition window).

From the layout point of view, it is important to collect the currents flowing in the substrate as much as possible. Therefore, in each domain, plenty of substrate contacts are placed, and N-wells are used around noise-generating devices. Moreover, concentric N-well and P^+ guard rings surround each power domain; the N-wells, biased at the supply voltage, collect electrons, while P^+ rings keep the substrate bias stable within the domain.
The substrate used in the available technology for the S-Altro is a P^- bulk type, with a relatively low (for this type of substrate) resistance. Some studies [Sc] [SL] show that, for this type of substrates, the current flow in the substrate is quite shallow; these studies support the idea that guard rings decrease considerably the analog-digital coupling through the substrate.

The technology used for the S-Altro offers, in addition, a lightly doped high-resistivity implant, called moat. The moat implant is used between adjacent power domains, in order to further increase the resistance between them. Carriers in a given domain in the substrate will then see a large resistance to other domains, and a smaller resistance to ground and supply lines, through the N-well and P^+ contacts; therefore, most carriers will not cross the border of the next domain.
The substrate resistance depends also on the physical distance between noisy and quiet devices; therefore, in the S-Altro the most sensitive components (PASA) have been placed as far as possible from the noisiest (digital block).

A section of the substrate separation implemented in the S-Altro is shown in figure 4.30.

Figure 4.31 shows the partition of the substrate with the moat. The resistance between the internal substrate and the substrate surrounding each enclosed moat shape depends on the geometry of the moat. Isolation has been introduced also around each ADC, in order to fight crosstalk between channels. Moreover, inside the ADC, some smaller islands, not shown in the figure, have been created with the moat, in order to separate some pieces of logic from the surrounding analog components.

The small areas delimited by the moat can see a resistance of several hundred Ohms to the neighbouring areas; in the bigger areas, the resistance can decrease to a few Ohms. Nevertheless, the moat is effective also in larger areas, because the charges in a substrate partition will see, locally, some resistance to another partition, and a much smaller impedance to ground

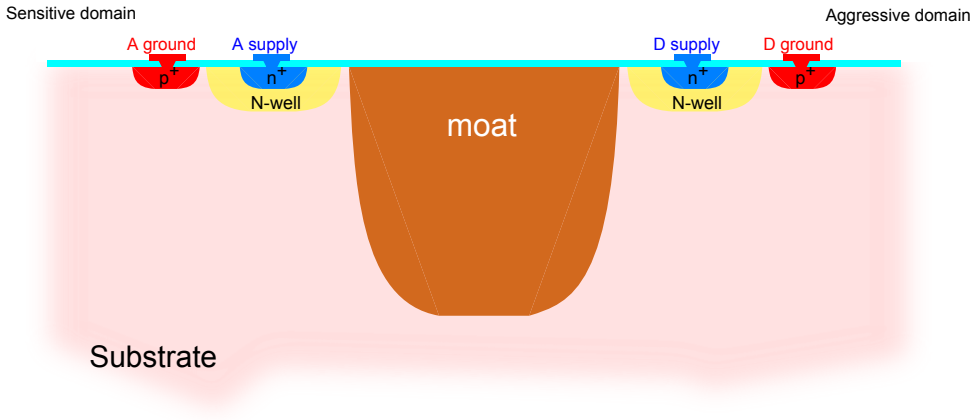

Figure 4.30: The separation of an analog and a digital power domain at the substrate level: a resistive moat, surrounded on both sides by N-wells and P^+ guard-rings.

or to the supply through the guard rings; therefore, most of the substrate current will still be picked up by the guard rings, rather than flowing into another substrate partition.
One more important point is that the series impedances of P^+ contacts to ground and of N-well contacts to the supply voltage must be minimized; therefore, a sufficient number of pads has been reserved in the S-Altro for ground and supply connections, reducing, most of all, the series inductance. Also the width of the supply lines on-chip is important, in order to keep the resistance to ground and supply low.

One note on ESD protections: after partitioning the power domains and the substrate, they should not be coupled together again, for example through ESD protection devices. A few back-to-back diodes have been connected between adjacent ground domains. These diodes provide the minimum acceptable level of ESD tolerance, but still introduce some undesired capacitive coupling between grounds. No other unnecessary protections have been implemented (for example, back-to-back diodes between each pair of grounds and supplies), in order to avoid introducing additional coupling.

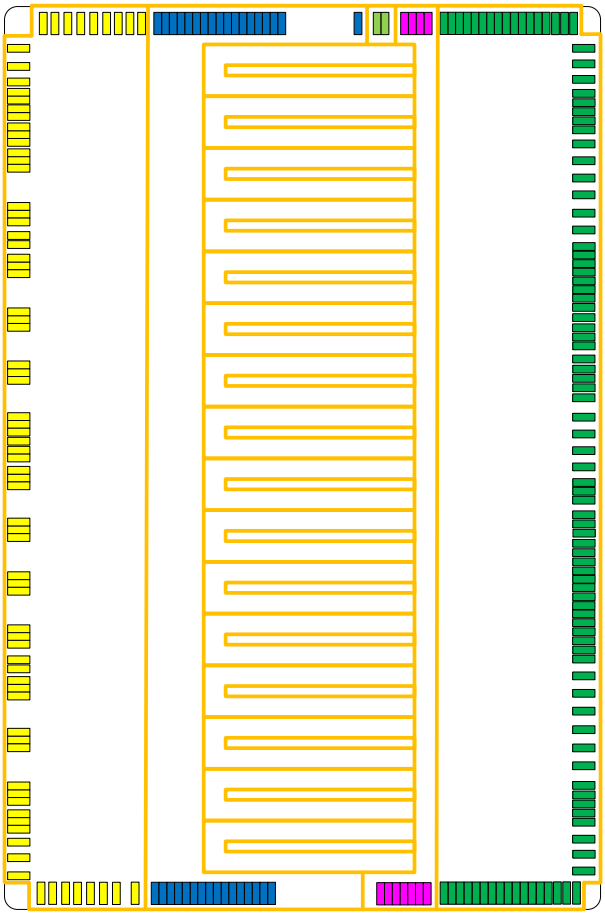

Figure 4.31: Substrate partitioning using the moat in the S-Altro Demonstrator. On each side of the moat, there are concentric rings of N-well and P^+ contacts.

4.8.2 Final layout and packaging

Picture 4.32 is a screenshot of the final layout of the Super-Altro Demonstrator.

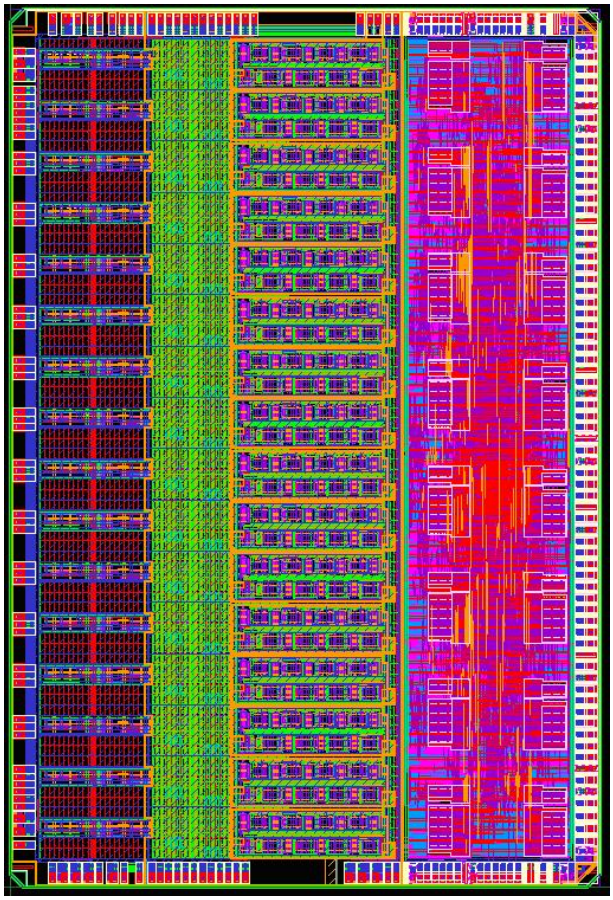

Figure 4.32: Full layout of the S-Altro Demonstrator; the sizes are $8560\mu\text{m}\times5751\mu\text{m}$ (49.2mm^2).

A few samples of the chip are packaged in a PGA package with 181 pins, for testing purposes. Once the functionality of the chip is proven, the default package for the S-Altro will be a QFP with 208 pins. In both cases, the size of the cavity is 12×12mm.

4.9 Top-level simulation

The simulation of the full chip is necessary, in order to prove that the flow of signals, clocks and data between the blocks happens smoothly. Unfortunately, this verification is not possible using analog simulation engines due to the size and complexity of the chip; moreover the duration of the simulation would need to be long (half millisecond).
On the other hand, some hardware description languages exist, like Verilog-AMS (AMS=Analog & Mixed-Signal extensions), which allow the codification of analog components, based on differential equations. The great advantage is that the model can be at a much higher level than the transistor level used by analog simulation engines; therefore, with a Verilog-AMS simulation engine, the simulation is much lighter, and also feasible.

As seen in 4.1, 4.2, 4.4 and 4.6, a Verilog-AMS model has been created for each analog component of the S-Altro. The delays have been added to the model, with values taken from analog simulations, including extracted parasitics, of the concerned block singularly. Other Verilog-AMS models have been created for the external components, e.g. the detector.
The DSP block has been implemented [GG] using a semi-automated design flow, starting from a purely digital Verilog code of the required functionalities. After the full flow has been executed, the timing information has been back-annotated.
Therefore, using the top-level testbench of figure 4.33, the full chip has been simulated, using the Verilog-AMS model of the Front-End, and the Verilog model of the DSP.

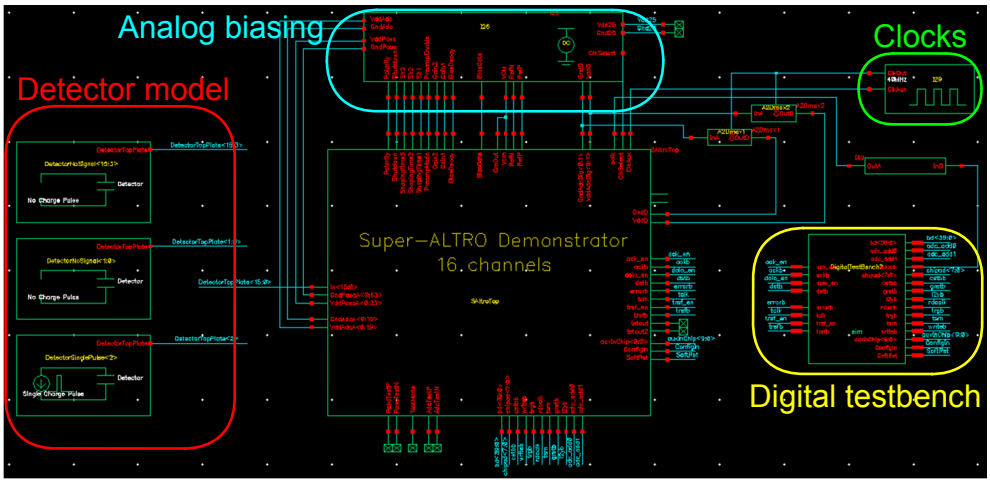

Figure 4.33: Testbench for the full S-Altro.

The testbench which proves the correct assembly of the different components of the S-Altro provides an input pulse to one channel; the PASA and ADC react as already shown in figure 4.15, and the DSP performs a subtraction of 5 ADC counts. Afterwards, a readout instruction is sent to the S-Altro.
Figure 4.34 shows the data flow, at register level, from the ADC to the DSP in the fast and slow corners: the safety margins on the setup and hold time for the DSP are wide.

Figure 4.34: Waveforms at the interface between ADC and DSP. The first line is the sampling clock, the second line is the output of the Digital Error Correction in the fast corner, the third line is the sampling register of the DSP in the fast corner, while the fourth and fifth line are again the ADC output and the DSP sampling register in the slow corner. The red circle on the left marks the ADC data valid, and the other circle on the right marks the sampling of the data by the DSP.

Figure 4.35 is the plot of the output of the DSP obtained with this simulation; the numerical values are reported in table 4.6, together with the outputs of the Front-End in the fast corner, as in figure 4.15. The table shows that the data are flowing correctly, and the DSP is subtracting 5 ADC counts, as decided; moreover, the plot shows that the timing is correct, because the sample number corresponds to the number of sampling clock cycles elapsed after the Level-1 trigger.
Therefore, this simulation proves that the assembly of the full chip is correct.

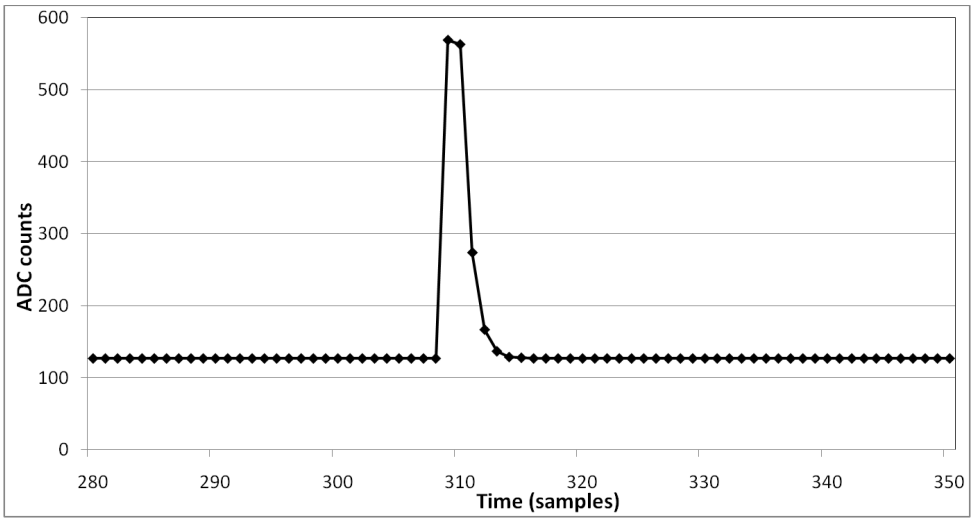

Figure 4.35: Result of the top-level simulation of the full chip.

Front-End output	DSP output
132	127
574	569
568	563
279	274
172	167
142	137
134	129
133	128
132	127

Table 4.6: The data saved by the DSP correspond to the output of the Front End (fast corner) minus 5 ADC counts.

Chapter 5

Super-Altro tests

This chapter introduces the test plan written for the characterization of the S-Altro and for the design of the test board; tests on the power pulsing possibilities of the chip are included. Section 5.2 describes the concept of the test board which has been developed, and shows its final design; this test board has been interfaced with the computer through an existing Readout Control Unit (RCU) of the type currently in use in the Alice experiment. Information on the RCU can be found in [AT]. The last section reports the results of the tests on the S-Altro, including analog measurements, digital tests, and power pulsing tests.

5.1 Test plan

A plan has been written, including all the tests that can be performed on the Super-Altro Demonstrator. Some of these tests turned out unnecessary, once the chip proved working. A complete test plan was nevertheless important to define the specifications for the test board.

The PASA can be tested independently by using the test structure in channel 15, described in section 4.7. Possible tests include:

- Checking the programmable shaping time.
- Measuring the gain in different configurations.
- Measuring the linearity.
- Evaluating the crosstalk between near channels.
- Measuring the noise with an external high-resolution ADC, varying the capacitance at the input of the PASA.

- Measuring the power consumption.

Using the same test structure in channel 15, also the ADC can be tested as a stand-alone device. In this case, a sinusoidal full-scale waveform is injected in the analog inputs and the Effective Number Of Bits (ENOB) is calculated. The power consumption is controlled and measured for different sampling frequencies, using the external bias resistor as described in 4.3.

In case of issues with the DSP block, the possibility to test the analog/mixed-signal part alone is foreseen: with the test mode "TSM" (section 4.7), outputs of the ADC are read directly.

Concerning the digital part, the programmed tests are:

- Write and read all registers, using properly chosen test patterns; this ensures that all the parameters in the chip can be correctly configured.
- Use the Multi-Event Buffers to readout events and check that there are no communication errors.
- Most of the DSP functionalities can be tested independently by using the Pedestal Memory (section 4.5); a known input pattern is written, and an output file is saved for each relevant combination of the configuration parameters. These output files are then compared with the results of the corresponding simulations.
- The power consumption of the digital block is measured for different DSP configurations.
- The digital core supply voltage, nominally 1.5V, is decreased to 0.8V and the previous tests on the functionality are repeated; this last test is meant to measure the lower limit to the power consumption of the DSP, which still maintains the functionality. The functionality at very low supply voltages may fail either because of setup/hold time violations in the logic, or because the memories lose their content.

Once the functionality of each block is proven, the full S-Altro chain can be tested:

- Check the smooth flow of signals and data through the whole chain.
- Measure the total noise, which includes the digital switching noise introduced in the analog sensitive part.
- Study the dependency of the noise on the phase delay between the sampling clock and the DSP clock (section 4.7).

- Measure the noise with different DSP configurations.
- Run some data acquisitions using the S-Altro connected to a real detector.

5.1.1 Testing the power pulsing features

Among the main goals of the Super-Altro Demonstrator, testing power pulsing capabilities is particularly interesting for potential future applications (section 1.3). Power pulsing can be implemented either by removing the supply voltages, or by using the shutdown features. In order to allow the user to test different power pulsing schemes, the test board must be capable of:

- Controlling the shutdown option of the PASA (paragraph 4.1.3) dynamically.
- Disconnecting the biasing resistor of the ADC (section 4.3) dynamically.
- Removing the sampling clock and/or the readout clocks dynamically.
- Shutting down the linear regulators which supply the PASA and the ADC analog power domains.
- Reducing the voltage supply of the DSP core, maintaining some minimum supply voltage, e.g. 1.0V.

Any combination of these features is possible. However, the option of shutting down the voltage regulators implies large switching currents to charge and discharge all supply decoupling capacitors.
From a system point of view, a much more advantageous option is the "Smart Shutdown": dedicated control lines act on the shutdown line of the PASA, on the biasing resistor of the ADC, and on the enabling of sampling and readout clock. In this way, all supply voltages remain constant, decoupling capacitors keep their charge, and the power pulsing features of the design are tested.

5.2 The Super-Altro test board

In this section the development of the test board, based on the requirements listed above, is presented. The first paragraph gives the main ideas behind the test board, and the second paragraph describes its design; the third paragraph shows the full test setup.

5.2.1 Concept of the test board

The very first decision was to reuse the existing infrastructure which is currently used in the ALICE experiment, described in [AT]; in the ALICE TPC, the front-end of this infrastructure is the RCU board, which connects with several Front-End Cards (FECs): the S-Altro test board must therefore be mechanically and electrically interchangeable with a FEC and compatible with the RCU.

After this, the main requirement for the test board is a great versatility, in order to allow testing of many features of the S-Altro. Moreover, the tests must be possible for both packaging options (PGA and QFP); therefore, the test board has a duplicated structure, where the sockets for both packages are present and each one has potentially all the electrical connections needed for the tests; eventually, using shorting or opening elements, the user chooses whether to test the PGA or QFP chip.

The diagram of the Test Board is depicted in figure 5.1. Apart from the

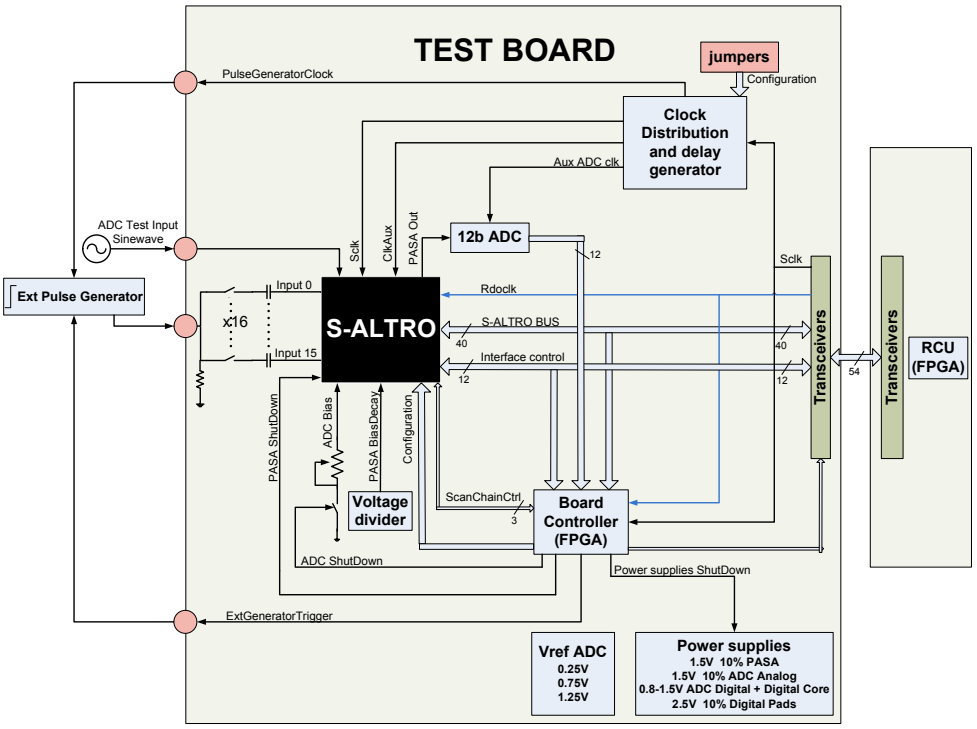

Figure 5.1: Diagram of the test board, showing also the connection to the Readout Control Unit (RCU) board.

chips under test, the core of the Test Board is the Board Controller (BC);

this is an FPGA which controls all the programmable functions on the board, and also the communication between the S-Altro and the RCU.

This communication is physically implemented by seven bidirectional transceivers. The BC sets the enable lines of the transceivers either in incoming, or outgoing direction, or in high impedance. In particular, it enables the outgoing data flow when the S-Altro asserts the DOLO_EN and TRSF_EN lines, indicating that it wants to write data into the 40bit bus. The transceivers are also used when reading or writing the configuration registers of the BC, or when sending commands to the BC itself.

The supply voltage to the various components on the board is provided by some linear Low DropOut (LDO) regulators. Some of these regulators have shutdown pins, each controlled by a signal line coming from the BC. Therefore, by writing appropriate values in some BC registers, it is possible to implement shutdown mode and power pulsing schemes.
The regulators for the power domain of the PASA, the ADC Analog and the ADC Digital can be shut down completely. The regulator for the DSP domain is configured in such a way, that its output can be reduced by the BC to a variable value as low as 0.8V; this minimum value is due to the requirement of keeping the contents of the memory, discussed in section 5.1. Regulators which supply the S-Altro have some shunt resistors, in order to measure their currents; this is used to monitor and plot the power consumption of the chips.

Two clocks arrive to the test board from the RCU board: the readout clock as single-ended and the sampling clock as a differential signal.
The readout clock is buffered by a commercial Integrated Circuit (IC) and delivered to the S-Altros and to the Board Controller; the BC has the possibility of shutting down the readout clock branches which go to the S-Altros, thus removing their clock.
The sampling clock is distributed by a more complicated IC, which delivers up to six single ended clocks, two of which can be delayed with respect to the other four. The BC controls which of these six clocks are enabled and which are off; this feature can be used in power pulsing tests. The reason why this particular IC was chosen is that the delayed clocks can be used as S-Altro ClkAux, in order to delay the clock of the DSP with respect to the ADC clock, as explained in section 4.6. The other outputs of this IC can be routed to the BC, to the S-Altro Sclk, to an on-board ADC and to an off-board instrument (after conversion to TTL logic level).
This commercial clock distribution IC provides external clock in CMOS logic at 2.5V; the sampling and auxiliary clocks of the S-Altro are in a 1.5V domain. Therefore level shifting of the clocks is necessary, and two solutions are implemented on the test board: a resistive divider, and level shifting through

a commercial IC. The performance of the commercial IC, in terms of jitter and integrity (shape) of the clock signal was to be evaluated, and therefore the resistive divider was kept as an option in case of bad results from the IC; during the tests, the chosen commercial IC proved a good solution and did not introduce any problems.

At the analog inputs of the S-Altro, an array of 0Ω resistors and capacitors allows the choice of the input signal. The input can either come from an external pulse generator (through a series capacitor which emulates the detector capacitance) or from a detector cable; in the latter case, the connector is of the same type used in the ALICE TPC, for compatibility.

The external pulse generator has to be synchronized with some internal signals, i.e. the sampling clock. Therefore, two TTL level shifters provide trigger outputs for external devices; these two outputs are driven by the BC and by the clock distribution IC. During tests, the external pulse generator is triggered by the BC, using the Level-1 trigger, which is synchronized with the sampling clock; in this way, the pulses are always sampled with a chosen phase, which allows, for example, to easily measure the maximum of the pulses; according to simulations, the jitter allowed to the trigger signal is 1.5ns when the shaping time of the PASA is 120ns, and 100ps with shaping time 30ns, for 0.5 LSB resolution.

As shown in section 4.7, channel 15 of the S-Altro has the option of sending off-chip the differential output of the PASA and of providing an external differential input to the ADC. Therefore, on the test board there are connectors for an external waveform generator, which could drive the ADC test inputs. Moreover, there is an external ADC, which can digitize the outputs of the PASA in channel 15; this external ADC was chosen with 12 bits of resolution and 65MHz of maximum sampling frequency, so that it is not the bottleneck of the measurements.

The Board Controller will save the 12bit output of the external ADC in some internal memory, when instructed to do so; the memory of the Board Controller is then readout by the RCU. The same two-step procedure applies during the test mode TSM, described in section 4.7, when the Board Controller saves the raw data from the S-Altro, and subsequently transfers these data to the RCU.

5.2.2 Design of the test board

The test board is an 8-layers Printed Circuit Board (PCB). Layers 0 (top), 7 (bottom), and 3 are used to route signals; layers 2 and 7 are ground planes, while layers 4, 5 and 6 are supply planes.

On the board, PASA and ADC analog domains have dedicated ground

planes, while all digital domains share the same ground. Grounds are well separated, without overlaps at any metal layer, as shown in figure 5.2. The three ground planes join together under the power connectors; moreover, some 0Ω resistors can be soldered to short different grounds under the S-Altro.

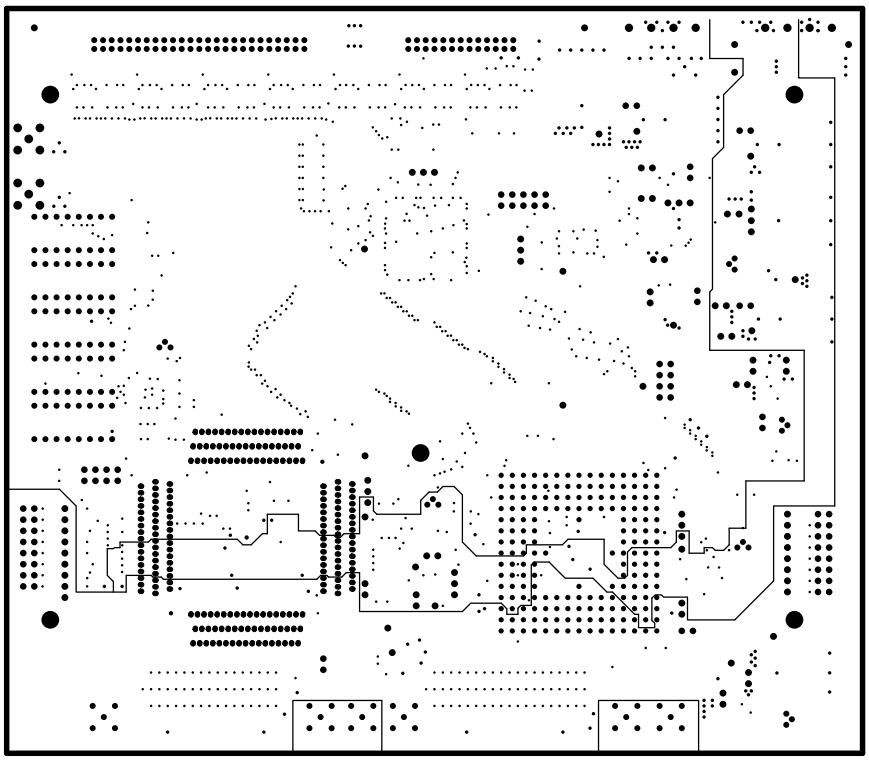

Figure 5.2: Thin continuous lines show the internal division of grounds on the test board, without any overlap between different ground domains. The largest domain is the digital ground, the domain covering the lower left corner is the PASA ground, while the domain in between is the ADC analog ground. The three domains join together at the top right corner, where power connectors are located.

Pictures 5.3 and 5.4 show the board with all mounted components, including sockets for PGA and QFP packages and one chip under test.

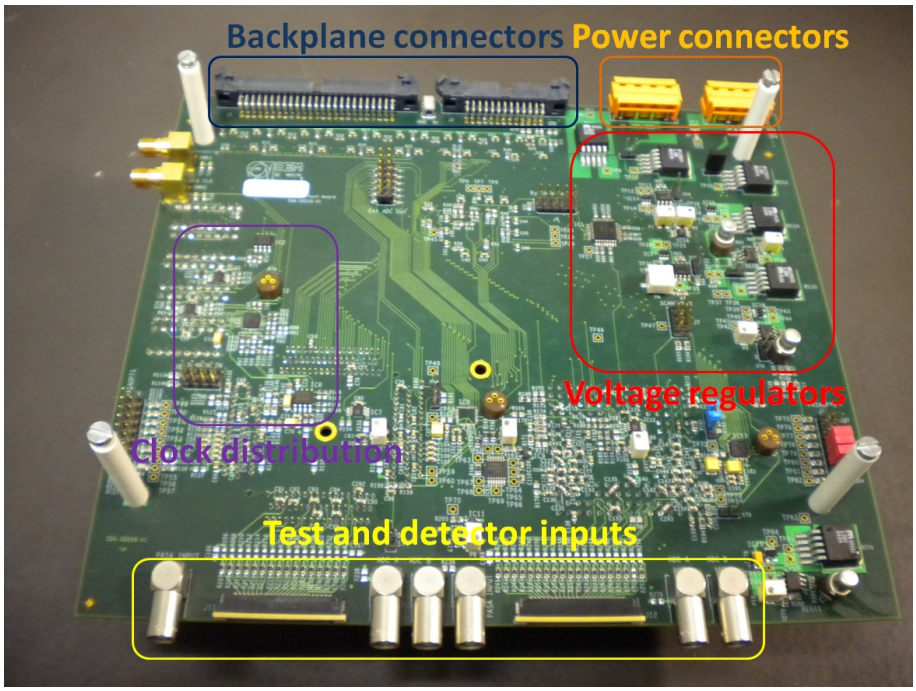

Figure 5.3: Picture of the top side of the test board.

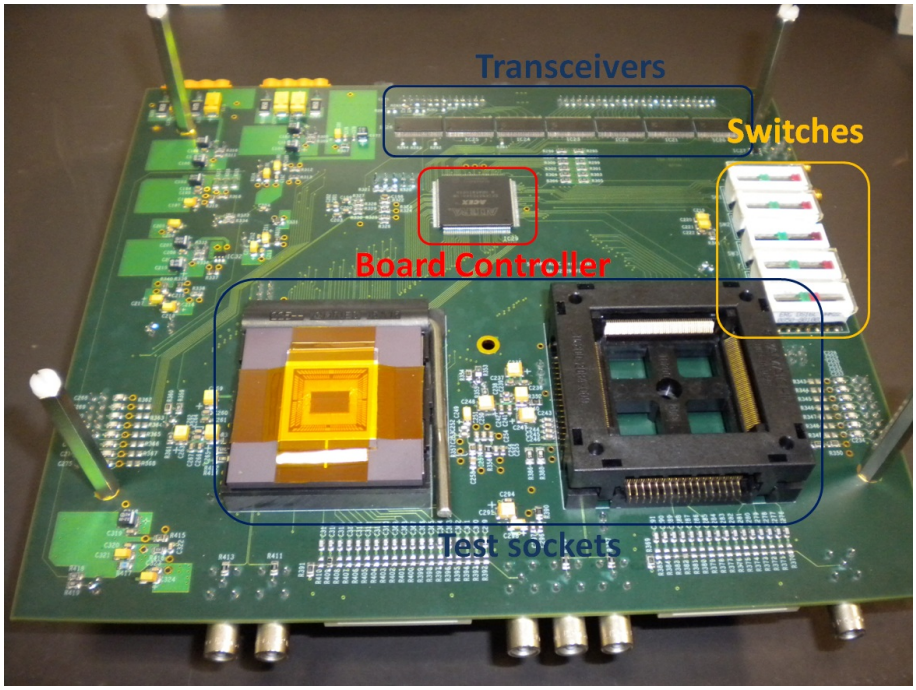

Figure 5.4: Picture of the bottom side of the test board.

5.2.3 Test setup

The test board is mounted on a backplane which connects physically with the RCU board. A backplane carries data and control lines. The full test setup is shown in picture 5.5.
The RCU FPGA is accessed by computer, using a Graphical User Interface (GUI). Using this GUI, users can set the values of the configuration registers of the RCU, of the Board Controller, and of the S-Altro chip under test; users can also run acquisitions, plot and save the readout data in files, as shown in figure 5.6. Alternatively, all these operations can be executed also from command line; this allows execution of scripts, especially useful when testing power pulsing features.

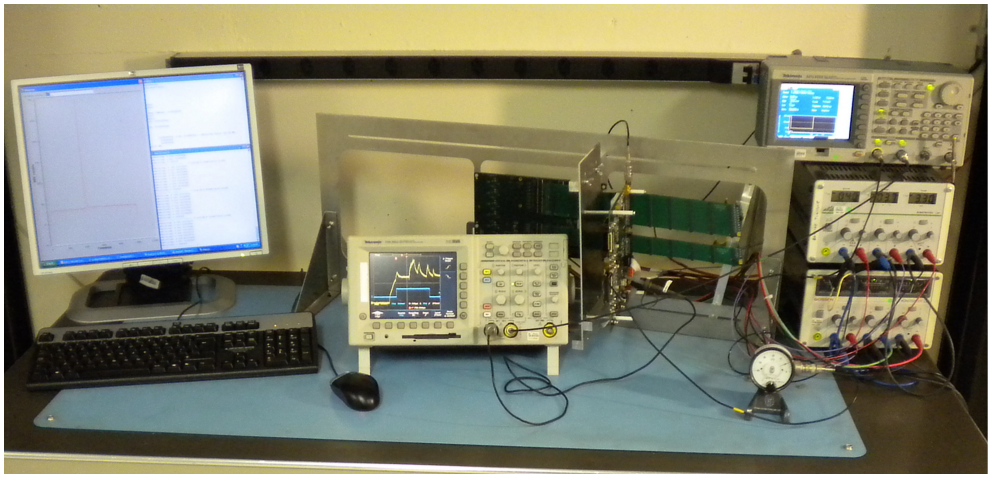

Figure 5.5: The test setup, with power supplies, pulse generator, attenuator, an oscilloscope and a computer. The test board is mounted on a backplane of the RCU.

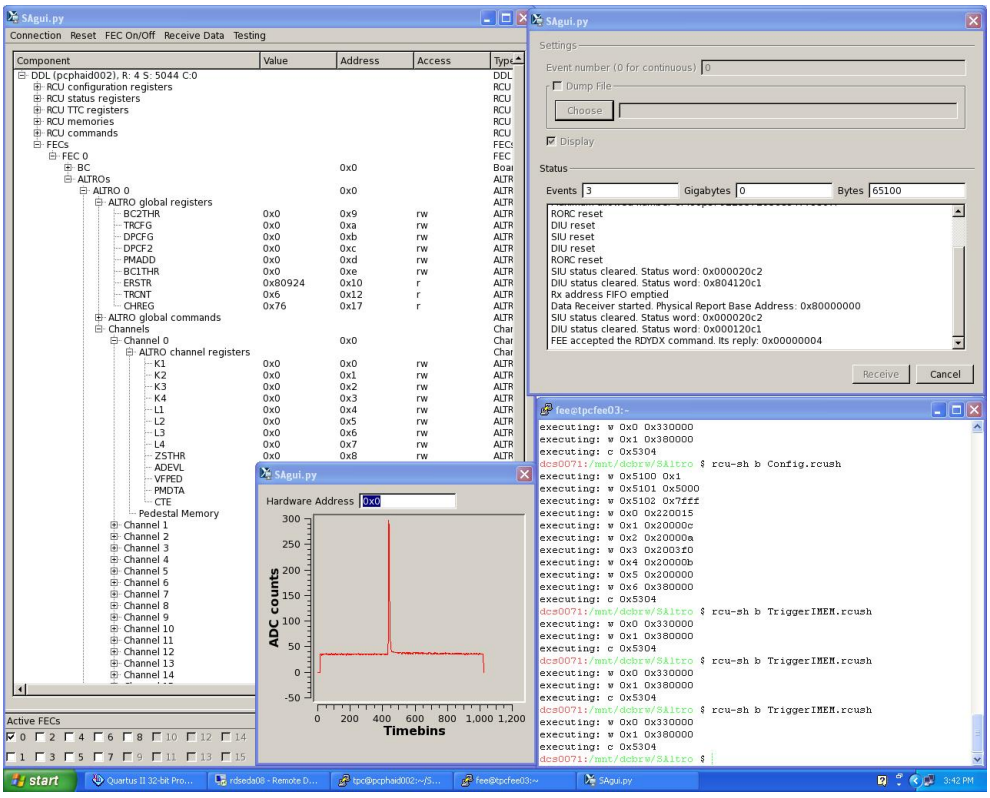

Figure 5.6: Screen shot showing the Graphical User Interface, which sets the S-Altro configuration registers and plots acquired data.

5.3 Test results

Six chips in PGA package were tested. The results reported in this section refer to chips named "PGA3" and "PGA4". PGA4 was packaged with the standard bonding diagram. In PGA3, the inputs of the PASA are left unbonded; this decouples the noise of the chip from most of the noise of the board ground plane.

5.3.1 Analog tests

Figure 5.7 shows two pulses acquired at a sampling frequency of 40MHz: a voltage step is applied to a PASA input, and the signal is filtered and processed by the PASA+ADC+DSP chain. This proves that the chip works and that data flow through the different blocks smoothly.

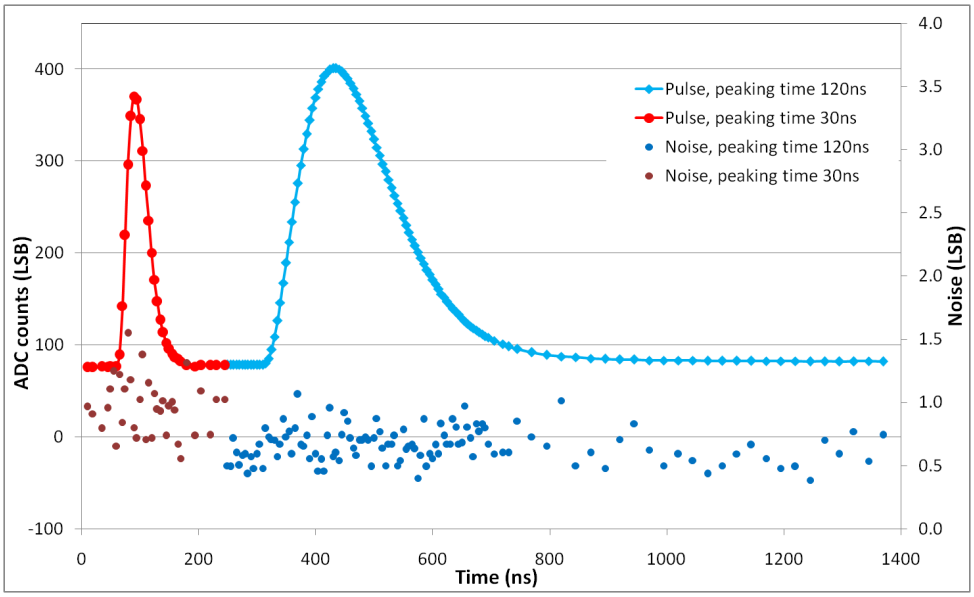

Figure 5.7: Acquisition of pulses with different peaking times of the PASA (red 30ns, blue 120ns); shapes are reconstructed with a granularity of 5ns in the time scale. The dots, corresponding to dynamic noise, refer to the secondary vertical axis.

Since the step voltage is synchronized with the Level-1 trigger and with the sampling clock, it is possible to delay it; in figure 5.7, several acquisitions of a pulse are delayed in steps of 5ns, in order to reconstruct the pulse shape with good granularity. The plot shows the semi-gaussian shape of the pulses, and also proves that the shaping times correspond to expectations. Each

sample was acquired 20 times, in order to calculate its standard deviation, which is also plotted; this constitutes a measurement of dynamic noise. It can be observed that this dynamic noise is just slightly larger during the steep rising edge of pulses, than during baseline sampling; jitter requirements (paragraph 5.2.1) are fulfilled by the system.

Many acquisitions similar to figure 5.7 have been executed; by measuring at each acquisition the peak of the semi-gaussian pulse, the gain of the system can be extracted.
Figure 5.8 is a typical plot of the gain of one PASA channel, as a function of the charge injected in the input, in the two opposite polarity configurations. The vertical error bars include random noise of the acquisitions (20 acquisitions per point) and the random uncertainty on the injected charge. The uncertainty on this type of measurements is dominated by the tolerance of the input on-board capacitors which are used to inject the pulse in the PASA; this finite tolerance introduces a systematic effect in gain measurements.

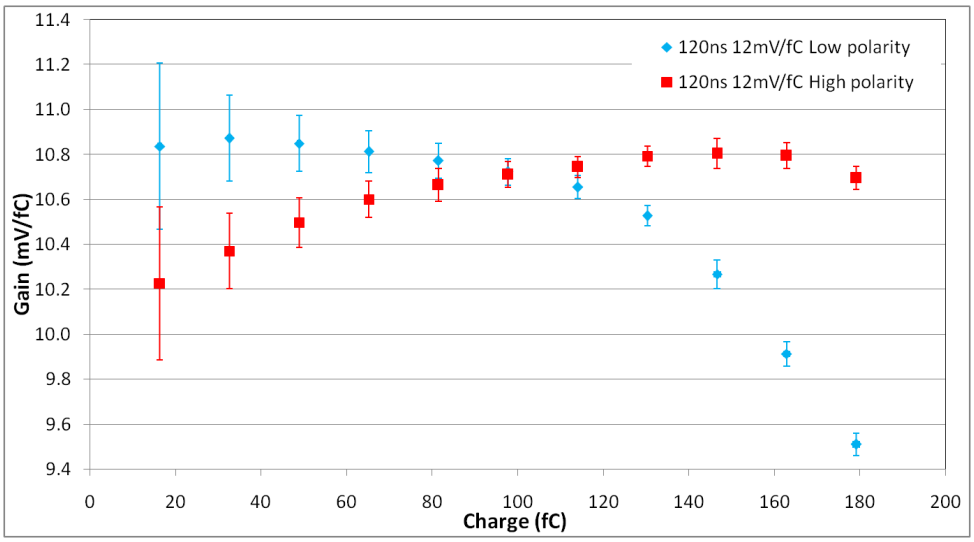

Figure 5.8: Plot of the gain of one PASA, using inputs of both polarities; the configuration is shaping time of 120ns and low gain (nominal 12mV/fC).

When no pulse is applied to the input, acquisitions allow measurements of the noise, calculated as the standard deviation of many samples of the baseline. Figure 5.9 plots baseline noise of every channel of the two chips PGA3 and PGA4.
In PGA3, PASA inputs are not bonded, and noise is about constant across all channels. In PGA4, the inputs of the PASA pick up noise from the ground plane of the test board and amplify it; therefore the noise is larger.

Moreover, channel-to-channel differences are evident. The same pattern has been observed also with other chips bonded similarly to PGA4: for example, channels 7, 14 and 15 are particularly noisy because they have both inputs (InHBM and InCDM input pads) bonded. This proves that a significant noise contribution is originated off-chip.

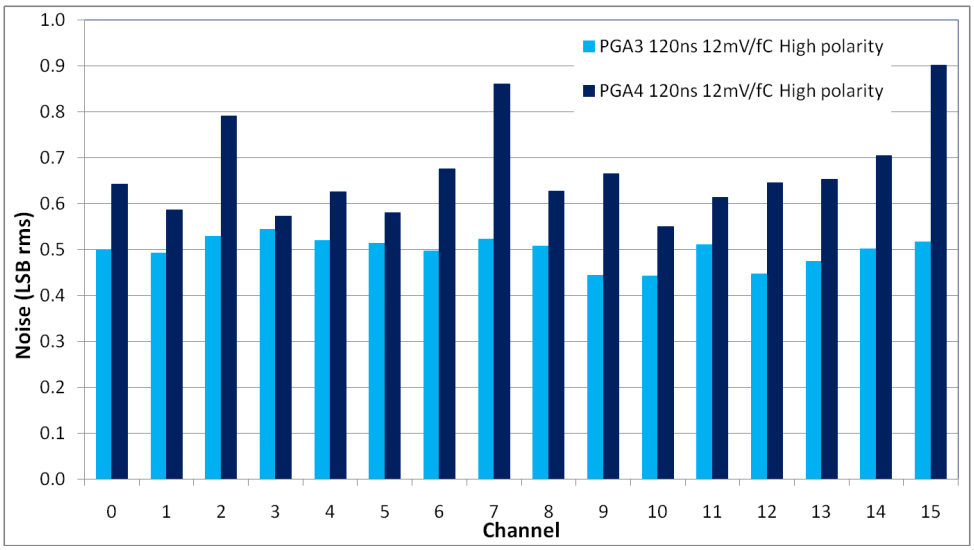

Figure 5.9: Plot of the noise in the two different packages.

Noise could be influenced by the amount of enabled DSP functionalities. Reading the Pedestal Memory (see Baseline Correction 1 in paragraph 4.5) is quite expensive in terms of power. Therefore, it is used to produce figure 5.10: in the red series, ten channels use Baseline Correction 1 in mode *din-f(t)*, that is, input data minus a pattern stored in the Pedestal Memory; at the same time, noise is measured in the other six channels. The plot shows that there is no relevant difference in noise when the Pedestal Memory is used; the amount of digital functionalities does not affect the noise performance of the system.

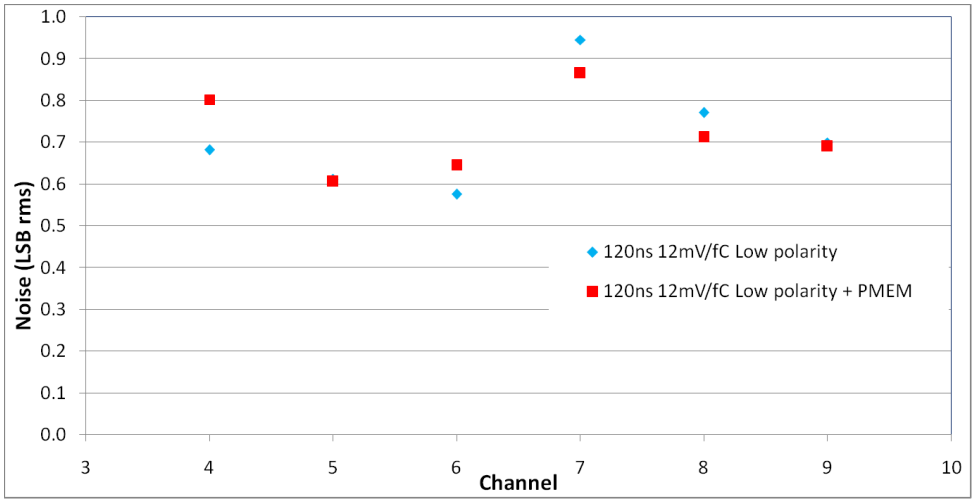

Figure 5.10: Noise of channels 4 to 9 of PGA4. In the blue series, DSP functionalities are reduced to a minimum; in the red series, channels 0-3 and 10-15 are using the Pedestal Memory (PMEM).

Table 5.1 reports noise measurements obtained with the two bonding schemes, in different configurations of the PASA; output noise, expressed in LSBs, is divided by the gain of the system (calculated as in figure 5.8) and reported to the input, expressed in fC or electrons.
PGA3 is affected by random noise of the PASA and ADC, quantization noise of the ADC, noise injected from the DSP into the analog part; measurements on PGA3 give the limit on the noise performance of the system, which could be achieved on a board with very clean ground planes. Measurements on PGA4 quantify the amount of noise that the present test board is injecting in the inputs of the PASA.

The configuration with 120ns shaping time and 12mV/fC gain is taken as reference. The values concerning PGA3 in table 5.1 give, for a Minimum Ionizing Particle of 4.8fC, a Signal to Noise Ratio of 54 and, for a maximum charge of 150fC, a dynamic range of 64.6dB; this is the upper limit of the performance achievable with the Super-Altro Demonstrator.
For PGA4, including effects of the bonding scheme and of the test board, the SNR is 37 and the dynamic range 61.3dB.

Figure 5.11 verifies the simulation of figure 4.4: some capacitors are added at the input of the PASA to measure noise as a function of the input capacitance.

	Configuration	120ns 12mV/fC	120ns 27mV/fC	30ns 12mV/fC	30ns 27mV/fC
PGA3	Noise LSB	0.480	0.655	0.526	0.683
	Noise fC	0.088	0.051	0.103	0.059
	Noise e^-	547	316	641	370
PGA4	Noise LSB	0.709	1.346	1.475	3.263
	Noise fC	0.129	0.104	0.287	0.283
	Noise e^-	809	649	1796	1768

Table 5.1: Noise summary: noise expressed in LSBs, or reported to the input (fC and electrons), in different configurations of gain and shaping time for chips PGA3 and PGA4. Values are averaged over the 16 channels.

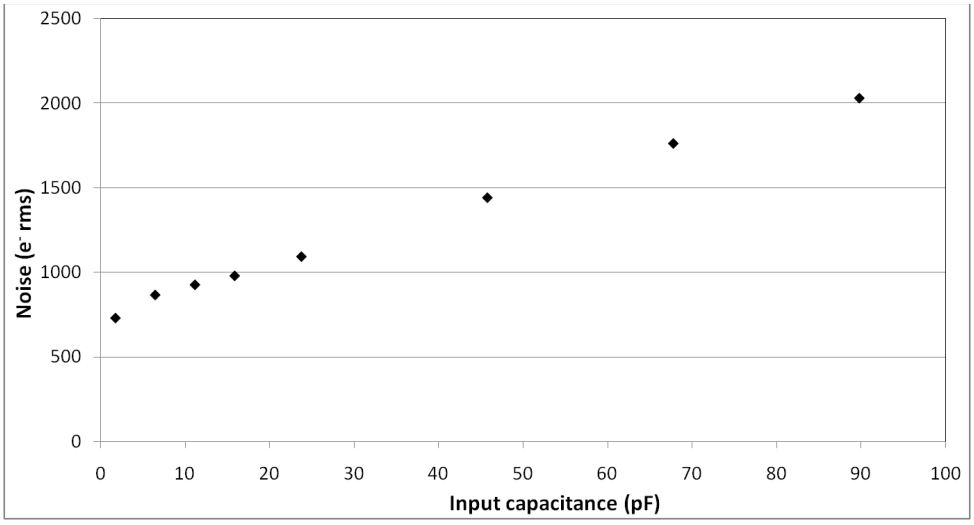

Figure 5.11: Baseline noise in channel 0 of PGA4 for different values of the detector capacitance. Configuration is 120ns shaping time, 12mV/fC gain, InCDM input pad used and 1V PASA BiasDecay voltage.

Crosstalk is evaluated by injection of a full-scale signal into one channel (aggressor); at the same time, in the next channels (victims), the induced signal is measured. This gives a crosstalk $<0.7\%$ between adjacent channels.

As explained in section 4.6, the clock tree was designed with attention to the relative phase of ADC clock and DSP clock. The test feature of the clock tree shown in section 4.7 is used to sweep this phase shift, as allowed by the on-board clock distribution IC (paragraph 5.2.1).

Figure 5.12 shows the baseline noise measured with different delays; the most sensitive region is for a delay between -2ns and 0ns, where the acquisitions are

concentrated. The absence of relevant noise increases in that region drives to the conclusion that the fully differential nature of the ADC and the isolation techniques described in paragraph 4.8.1 make the ADCs very robust against noise coming from the DSP.

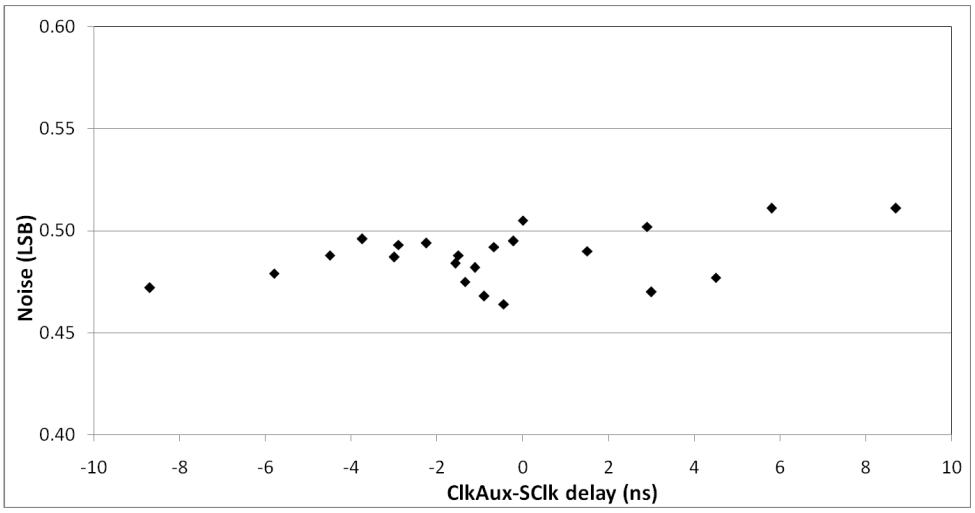

Figure 5.12: Noise in PGA3, with different delays between the auxiliary clock for the DSP and the sampling clock for the ADCs.

5.3.2 Digital tests

The digital part of the S-Altro has been tested extensively using the pedestal memory. Patterns loaded in the pedestal memory and played through the DSP were also simulated, using the same DSP parameters; the results of simulations and acquisitions were compared, to prove that the DSP behaves as designed.

Figure 5.13 exemplifies the action of the DSP on a pattern, which emulates an acquisition with a detector. The input has an offset, which drifts during the acquisition window, and the pulses exhibit an undershoot; setting a threshold for zero suppression is very challenging. When digital signal processing is used, baseline correction 1 removes the initial offset, the digital shaper corrects the undershoots, and baseline correction 2 removes the baseline drift; the produced output is much cleaner than the input, and can be easily zero-suppressed.

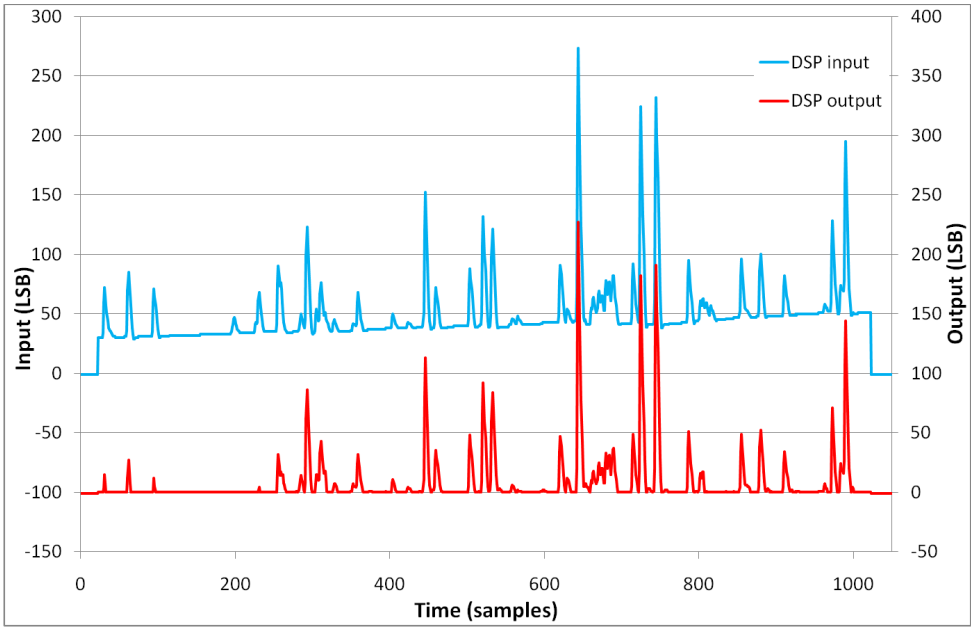

Figure 5.13: A realistic pattern is loaded in the Pedestal Memory [RB, 5]. The input pattern refers to the left vertical axis, while the output pattern refers to the right vertical axis.

The power consumption of the DSP is plotted in figure 5.14. Before a Level-1 trigger, the power consumption in standby is in the order of 65mW; during an acquisition, more logic is switching and the consumption increases; after the acquisition, the consumption returns to its baseline value in some

tenths microseconds, due to the decoupling capacitors on the supply lines.

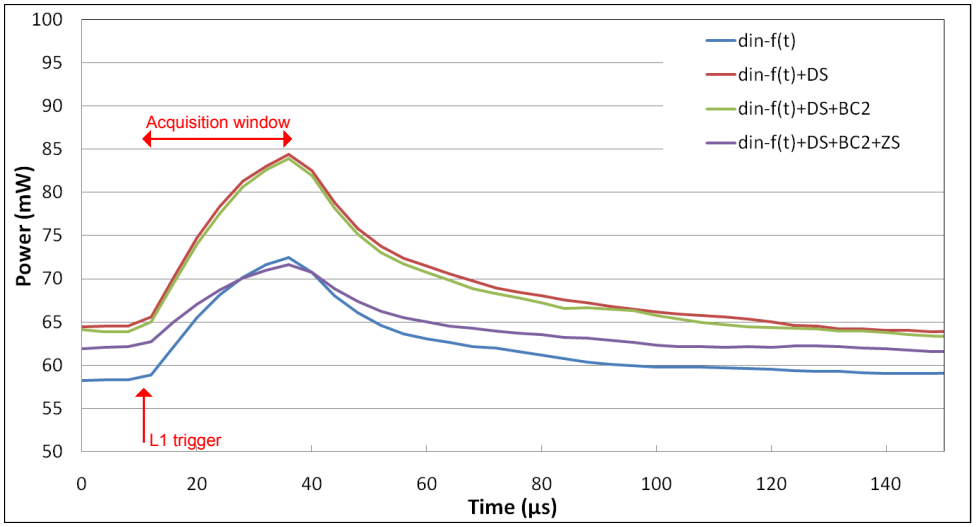

Figure 5.14: Power consumption of the DSP with different blocks enabled [RB, 5]. In the first plot, only baseline correction 1 is active, and it is operated in mode *din-f(t)*; in the following plots, also digital shaper, baseline correction 2, and zero suppression are activated.

The plot shows that the increases in power consumption with more blocks enabled are just a fraction of the standby power consumption. This explains the results of figure 5.10: the noise does not vary significantly when more functionalities are introduced, because the increases of logic switching activities are moderate.

Figures 5.13 and 5.14 can be compared with the corresponding measurements obtained with the ALTRO chip and shown in [RB, 5].

5.3.3 Power measurements and power pulsing tests

Standby power consumption of PASA, ADC and DSP are reported in table 5.2; digital pads consume negligible power because they are not switching. During acquisition and readout, DSP core and digital pads consume more power, as reflected in figure 5.16 and table 5.3.

Diagram 5.15 shows the percentage contribution of each block to the total power consumption. Clearly, the analog part, especially the ADC, consumes much more power than digital functionalities.

Power pulsing tests have been executed, using the Smart Shutdown feature introduced in paragraph 5.1.1: the biasing circuits of PASA and ADC are turned off, while sampling clock and readout clock are disabled.

Power domain	Power/channel	Total power
PASA	10.26	164
ADC analog	31.28	500
ADC digital	1.71	27
Digital Core	4.04	65
Chip total	47.3	757

Table 5.2: Standby power consumptions of the different power domains, expressed in mW.

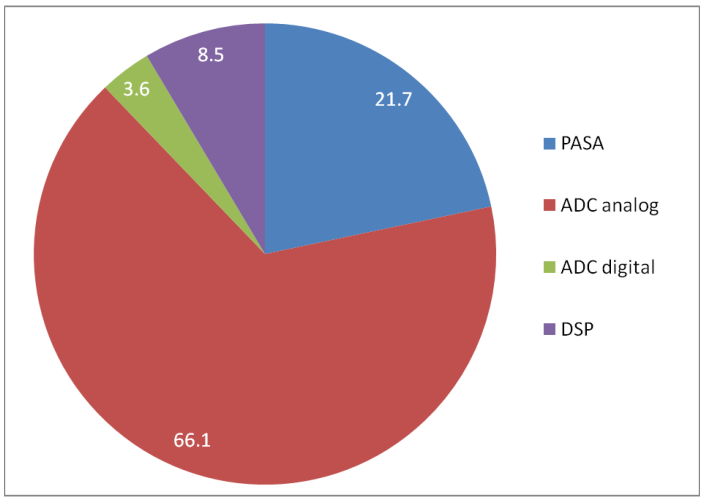

Figure 5.15: Percentage power consumption of the different blocks.

Figure 5.16 plots the power consumption of the DSP during a typical power pulsing cycle. Initially the system is in Smart Shutdown, and the power consumption is only due to leakage currents. At some point, the system is powered up: biasing circuits are activated, and clocks are enabled. After a given delay (in the plot it is 100μs), a Level-1 trigger is sent and an acquisition starts; afterwards, also a Level-2 trigger is sent, and readout is performed.

The most interesting feature of a power pulsing cycle is the minimum applicable delay between power up and L1 trigger. Any system takes some time to recover from shutdown mode into full operation, and this time sets the limit on power pulsing frequency and power consumption.
The readout procedure also takes a considerable amount of time, which should be minimized. This and other considerations concerning the test

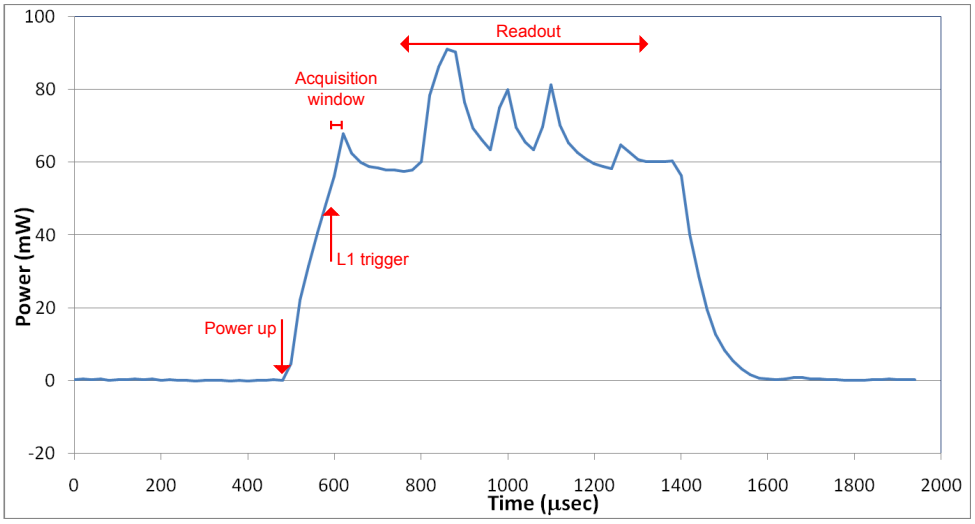

Figure 5.16: Transient power consumption of the DSP, during a power pulsing cycle.

system are detailed in the final notes below.

In order to measure the minimum delay between power up and L1 trigger, a pulse with fixed amplitude has been sent during the acquisition window, while executing power pulsing cycles. Many acquisitions have been run, with different values of the delay; the acquired pulse height is plotted in figure 5.17, as a function of the delay.

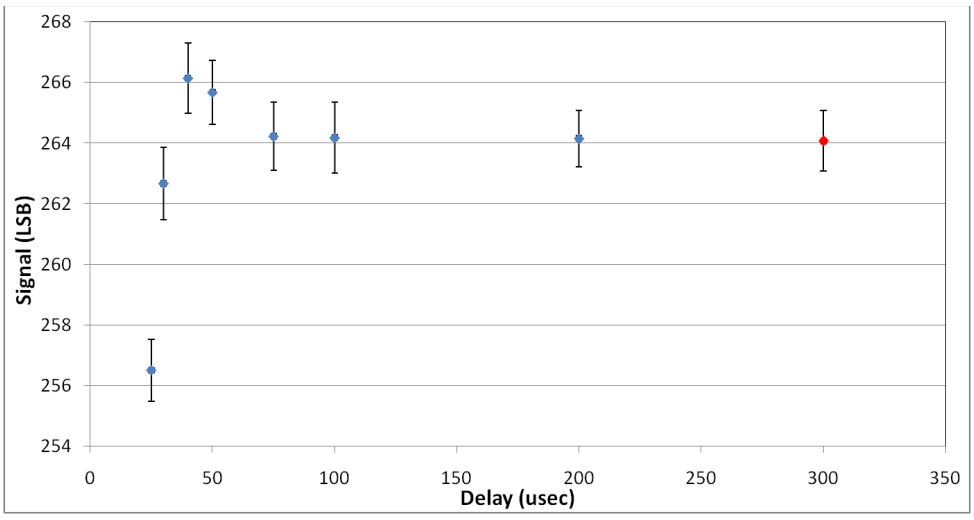

Figure 5.17: Acquired height of a test pulse, with different delays between power up and Level-1 trigger. The last (red) measure is taken in continuous

Power domain	Smart Shutdown (mW)	Power pulsing cycle (μJ)
PASA	2.12	145.2
ADC analog	6.88	421.1
ADC digital	$\approx$0	22.9
Digital Core	0.16	58.3
Digital Pads	$\approx$0	6.9
Total	9.2	654.3

Table 5.3: Power consumption of the different power domains during Smart Shutdown, and energy consumption during one power pulsing cycle.

mode, without implementing power pulsing cycles.

The figure shows that, with a delay as low as 75μs, the pulse height is acquired correctly: the power pulsed acquisition differs from a continuous acquisition by less than 1 ADC count. Therefore, a safe delay of 100μs between power up and L1 trigger is chosen for power pulsing measurements.

Power consumption plots, similar to 5.16, have been acquired for all power domains. The calculated integrals of the power during a power pulsing cycle are reported in table 5.3.

During Smart Shutdown, leakage currents produce a power consumption of 9.2mW. During a power pulsing cycle similar to that of figure 5.16, a total energy of 654.3μJ is required.
As a consequence, implementing power pulsing cycles with a frequency of 50Hz, as in the CLIC accelerator, the Super-Altro Demonstrator consumes:

$$P_{CLIC} = 9.2mW + 50Hz \cdot 654.3\mu J = 41.9mW \tag{5.1}$$

Implementing power pulsing cycles with the 5Hz pulse train frequency of the ILC accelerator, the power consumption is:

$$P_{ILC} = 9.2mW + 5Hz \cdot 654.3\mu J = 12.5mW \tag{5.2}$$

Compared with the 757mW power consumption in continuous mode (table 5.2), power pulsing using the smart shutdown mode gives power reductions of a factor 18.1 for CLIC, or 60.6 for ILC. For low pulse train frequencies (ILC), leakage currents absorb a dominant fraction of the total power.

Final notes on power pulsing

Looking at figure 5.16, one can see that the length of a power pulsing cycle is about 1ms; most of this time is spent for readout, which is controlled by the RCU (figure 5.1). During readout, PASA and ADC are unuseful but still active, and consume most of the power; therefore, the readout time needs to be minimized.
The size of one Multi-Event Buffer is 10kbit per channel, or 20kbyte for 16 channels; this can be readout in just 100μs at a readout frequency of 40MHz (the bidirectional bus has 40 bits), or in 50μs at 80MHz. Therefore, the present RCU does not fully exploit the speed capabilities of the S-Altro.
With a speed-optimized RCU firmware, the readout could theoretically be much shorter, and therefore decrease the power consumption. Moreover, with a new firmware, PASA and ADC could be turned off at the end of the acquisition window, while the DSP is still active to perform readout. The proposed scheme is represented graphically in figure 5.18; if PASA and ADC were active for just 150μs per cycle, a reduction of the energy per cycle (table 5.3) of a factor 5 is expected.

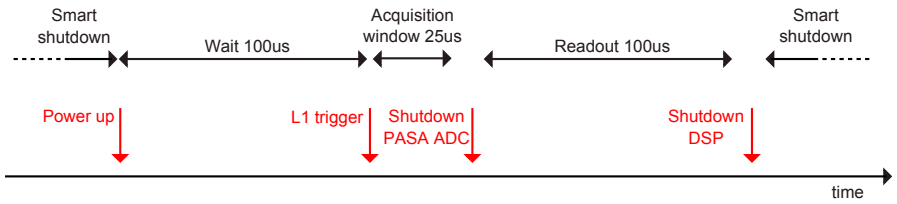

Figure 5.18: Proposal of a power pulsing scheme, with optimized timing for low power consumption.

Another important point is that the measurements have been executed without using Zero Suppression, that is, memories have been completely filled with data to be readout. Depending on the application, using ZS, the memories could store much less data; therefore the readout time and power consumption could be consistently reduced. The values given in table 5.3 are therefore based on conservative assumptions, and will be much better in real detector applications.

In some detectors, it may be necessary to keep the preamplifier always active, in order to provide a DC bias to the detector pads also during shutdown. In this case, the 164mW required by the PASA will dominate the power consumption.

Chapter 6

Conclusions and outlook

6.1 Conclusions

The potential of the pipelined ADC architecture has been studied in chapter 3. Calculations show the aspects which determine the performance and power consumption of such ADCs.
The most critical component is the main amplifier; this has been designed in schematic, aiming at an ADC with 12 bits of resolution and a maximum sampling frequency of 100MHz. The design was based on the small-signal models reported in appendix A, where three possible compensation options are considered. Simulations show the feasibility of an ADC with the given specifications, using a 130nm technology. The predicted power consumption is 165mW for the whole ADC. This value provides the basis for concept studies, in view of future chips integrating high-resolution, high-speed ADCs.

The S-Altro project developed a successful Demonstrator, which proves the feasibility of compact ADC- and DSP-based front-end chips for High-Energy Physics applications. Moreover, given the satisfactory test results, the Super-Altro Demonstrator can be already used by several experimental collaborations.

Data of table 5.1 and figure 5.11, compared with simulations of figure 4.4, show that the measured noise of the full chip is close to the simulated noise of the PASA alone. This result opens the way to integration of sensitive analog functions and noisy digital logic in the same chip and on the same substrate: using appropriate design techniques, as explained in paragraph 4.8.1, the degradation of analog performances is unimportant.

One channel of the Demonstrator occupies an area of 3.1mm^2; assuming

a 15% headroom for other components, the channel size fits in the 1x4mm pad size of the Linear Collider TPC. A few hundreds naked chips will be wire bonded to thin "stamp cards", which will be mounted directly on the pad plane of the LCTPC prototype. As opposed to the ALICE TPC, the Demonstrator chips will be sitting parallel to the pads, avoiding the need for long cables to connect to the detector; this decreases the detector capacitance and, as a consequence, the system noise.

A wide range of programmable features make the Demonstrator suitable for tests of different detector types. The minimum PASA shaping time (30ns), and the correspondingly high maximum sampling frequency of the ADC (40MHz) allow detailed measurements, for example, of the signals produced by GEMs.

Power pulsing measurements have been carried out, as detailed in paragraph 5.3.3. The used approach is effective in cutting power, while preserving the performance: power reductions of a factor 18.1 are measured using CLIC accelerator parameters, or a factor 60.6 with ILC parameters.
The board which has been developed for the tests is versatile and ready for further power pulsing tests. For example, the power consumption and distribution could be tested in a system with several boards connected to the same backplane.

6.2 Outlook

The Super-Altro Demonstrator opens possibilities of further design optimization, aiming at lower power and higher number of channels; the results obtained are already the basis for some studies on a future Gas Detector Signal Processing chip (GdSP), currently ongoing at CERN [GdSP]. Figure 5.15 shows that the next developments should attack the power consumption of ADC and PASA.

Recently, due to their relevance for television applications, new ADC architectures have been developed, targeting resolutions of 10 bits and sampling frequencies in the order of 40MHz. Pipeline and synchronous SAR ADCs are being replaced by asynchronous SAR ADCs.
In conventional SAR converters (paragraph 3.2.1), a clock triggers the comparisons at each cycle. With the new asynchronous architecture [CB], the clock just starts the conversion, while the decision on one threshold triggers the next comparison, and the ADC generates automatically its own timing; in principle, the periodic clock could be even replaced by a trigger signal. The great advantage of asynchronous SAR ADCs is a lower power consumption: sub-milliWatt power consumptions have been reported for 10 bit, 40MHz

ADCs [KL].

Concerning the PASA, the fast shaping time of 30ns is useful for detector tests, but not practical for experiment applications, which would rather use the 120ns shaping. Therefore, a next version of the S-Altro should have a slower PASA, which would also require much less power. Moreover, a shaping time in the order of 100-120ns would require an ADC with a slower sampling rate, e.g. 10-20MHz, which in turn decreases the power consumption of the ADC.

As mentioned in the final notes of paragraph 5.3.3, some detectors may need to keep a biasing voltage on the pads. Therefore, the next PASA could have two shutdown lines: one only for the preamplifier, and one dedicated to the shaper. The shaper could be turned off during power pulsing cycles, while the preamplifier stays on and provides the required DC bias.

Figure 5.18 and the associated discussion also give some ideas to improve the power pulsing scheme, using the present Super-Altro Demonstrator with modifications to the test infrastructure. If PASA and ADC are shut down right after the acquisition window, while DSP performs readout, a reduction of a factor 5 is expected in the energy consumption per power pulsing cycle.

Appendix A

Amplifier small-signal models

This appendix contains the small-signal models of the main amplifier described in section 3.4. The models are calculated using the procedure of reference [HL]; in a comparison with this reference, the models reported here include one more node, because the input transistors as well as the load transistors are cascoded[1]. As explained in paragraph 3.4.2, three candidate compensation techniques are considered for this amplifier:

1. Traditional Miller compensation, with the compensation capacitor C_c between the output of the first stage and the output of the second stage of the amplifier. This is considered in section A.1.

2. Indirect compensation between the cascoded current load and the output of the amplifier, considered in section A.2.

3. Indirect compensation between the cascoded input transistor and the output of the amplifier, considered in section A.3.

The amplifier is fully-differential; therefore its common-mode signals are not relevant, and single-ended calculations describe the behaviour of the amplifier completely. For these reasons, the small-signal equivalent models drawn in this appendix are differential and single-ended models.

In all calculations, $s = j\omega$ is the complex angular frequency (radians per unit time); j is the imaginary unit and ω is the angular frequency.

[1] After completing this work, the author became aware of reference [AD], which proposes design methodologies for this type of amplifiers

A.1 Miller compensation

The amplifier with Miller compensation is in figure A.1. Figure A.2 is the equivalent small-signal model.

Kirchhoff's laws applied to this small-signal model result in equations A.1.

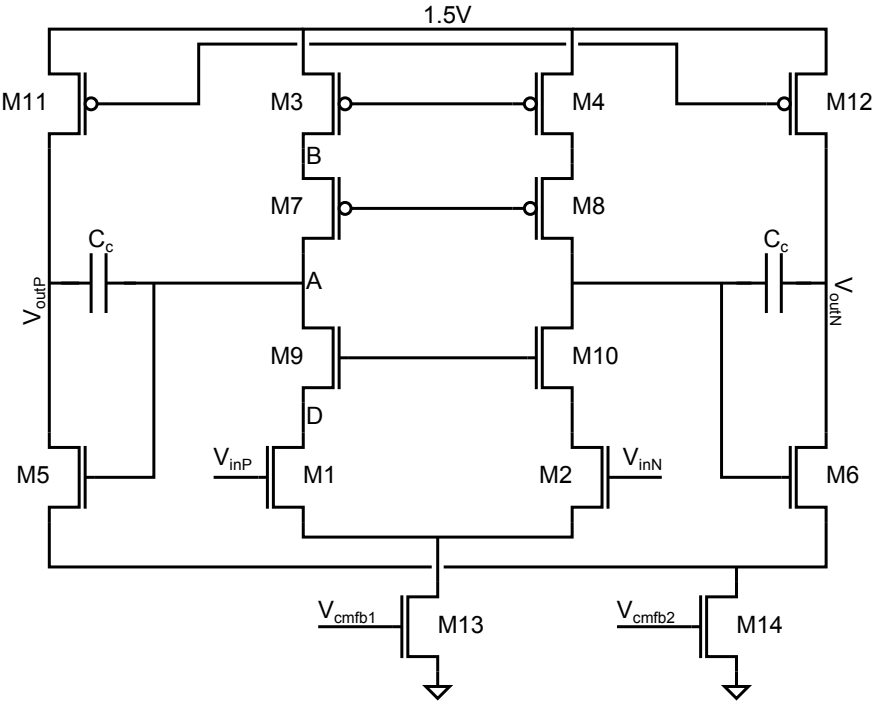

Figure A.1: Schematic of the amplifier with Miller compensation.

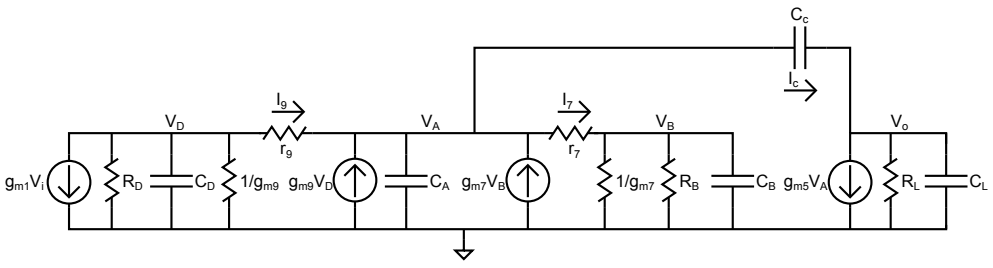

Figure A.2: Small-signal equivalent model of the amplifier with Miller compensation.

$$\begin{cases} g_{m1} \cdot V_i + \frac{V_D}{R_D} + s \cdot C_D \cdot V_D + V_D \cdot g_{m9} + I_9 = 0 \\ I_9 = \frac{V_D - V_A}{r_9} \\ I_c = \frac{V_A - V_o}{s \cdot C_c} \\ I_9 + g_{m9} \cdot V_D + g_{m7} \cdot V_B = \frac{V_A}{R_A} + s \cdot C_A \cdot V_A + I_7 + I_c \\ I_7 = \frac{V_A - V_B}{r_7} \\ I_7 = V_B \cdot g_{m7} + \frac{V_B}{R_B} + V_B \cdot s \cdot C_B \\ I_c = g_{m5} \cdot V_A + s \cdot C_L \cdot V_o + \frac{V_o}{R_L} \end{cases} \tag{A.1}$$

Some expressions are used to make the following equations more readable; these expressions are defined in system A.2, and will be used also in the next sections of this appendix.

$$\begin{cases} x_1 = \frac{1}{R_D} + s \cdot C_D + g_{m9} + \frac{1}{r_9} \\ x_2 = \frac{1}{r_9} + g_{m9} \\ x_3 = \frac{1}{r_9} + s \cdot C_A + \frac{1}{r_7} + s \cdot C_c \\ x_4 = g_{m7} + \frac{1}{r_7} \\ x_5 = \frac{1}{r_7} + g_{m7} + \frac{1}{R_B} + s \cdot C_B \\ x_6 = g_{m5} - s \cdot C_c \\ x_7 = s \cdot C_L + \frac{1}{R_L} + s \cdot C_c = \frac{1}{R_L} + s \cdot (C_c + C_L) \\ x_8 = y_5 + s \cdot (C_c + C_B) \\ x_9 = \frac{1}{R_L} + s \cdot (C_c + C_L) \\ x_{10} = y_1 + s \cdot (C_c + C_D) \end{cases} \tag{A.2}$$

Solving system A.1 gives the following amplifier transfer function:

$$\frac{V_o}{V_i} = \frac{g_{m1} \cdot r_7 r_9 \cdot x_2 x_5 x_6}{r_7 r_9 x_1 x_3 x_5 x_7 + s \cdot C_c r_7 r_9 x_1 x_5 x_6 - r_7 x_2 x_5 x_7 - r_9 x_1 x_4 x_7} \tag{A.3}$$

At this point, expressions y_1, y_3, y_5 are defined as in system A.4. In contrast with x_1, x_3, x_5, they are not a function of the frequency. These expressions will also be used throughout the appendix.

$$\begin{cases} x_1 = y_1 + s \cdot C_D \\ y_1 = \frac{1}{R_D} + \frac{1}{r_9} + g_{m9} \\ x_3 = y_3 + s \cdot (C_A + C_c) \\ y_3 = \frac{1}{r_9} + \frac{1}{r_7} \\ x_5 = y_5 + s \cdot C_B \\ y_5 = \frac{1}{r_7} + g_{m7} + \frac{1}{R_B} \end{cases} \tag{A.4}$$

Equation A.3 is rewritten as:

$$\frac{V_o}{V_i} = \frac{A}{B + C - D - E} = \frac{b_0 \cdot N(s)}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4} \tag{A.5}$$

Components b_0, $N(s)$, a_0, $a_1 s$, a_2, a_3, and a_4 will be calculated later; expressions A, B, C, D, E are defined in system A.6.

$$\begin{cases} A = g_{m1} \cdot r_7 \cdot r_9 \cdot x_2 \cdot x_5 \cdot x_6 \\ B = r_7 \cdot r_9 \cdot x_1 \cdot x_3 \cdot x_5 \cdot x_7 \\ C = sC_c \cdot r_7 \cdot r_9 \cdot x_1 \cdot x_5 \cdot x_6 \\ D = r_7 \cdot x_2 \cdot x_5 \cdot x_7 \\ E = r_9 \cdot x_1 \cdot x_4 \cdot x_7 \end{cases} \tag{A.6}$$

Expanding the expression for A:

$$A = g_{m1} \cdot r_7 \cdot r_9 \cdot x_2 \cdot (y_5 + sC_B)(g_{m5} - sC_c) = \tag{A.7}$$

$$= g_{m1} \cdot r_7 \cdot r_9 \cdot x_2 \cdot y_5 \cdot g_{m5} \cdot \left[1 + s\left(\frac{C_B}{y_5} - \frac{C_c}{g_{m5}}\right) - s^2 \frac{C_c C_B}{y_5 g_{m5}}\right] \tag{A.8}$$

Therefore, frequency-independent b_0 and frequency-dependent $N(s)$ are:

$$b_0 = g_{m1} \cdot r_7 \cdot r_9 \cdot x_2 \cdot y_5 \cdot g_{m5} \tag{A.9}$$

$$N(s) = 1 + s\left(\frac{C_B}{y_5} - \frac{C_c}{g_{m5}}\right) - s^2 \frac{C_c C_B}{y_5 g_{m5}} = \tag{A.10}$$

$$= \left(1 - s\frac{C_c}{g_{m5}}\right) \cdot \left(1 + s\frac{C_B}{y_5}\right) \tag{A.11}$$

Second-order equation A.11 shows that the transfer function of this amplifier has two zeros, calculated forcing $N(s) = 0$:

$$z_1 = \frac{g_{m5}}{C_c} \tag{A.12}$$

$$z_2 = -\frac{y_5}{C_B} = -\frac{\frac{1}{r_7} + g_{m7} + \frac{1}{R_B}}{C_B} \approx -\frac{g_{m7}}{C_B} \tag{A.13}$$

Equation A.12 defines the Right Half-Plane (RHP) zero z_1, while equation A.13 defines the Left Half-Plane (LHP) zero z_2, approximated using approximations A.14.

$$\begin{cases} g_{m7} \approx g_{m9} \\ r_7 \approx r_9 \approx R_B \approx R_D \approx R_L \\ g_{m7}, g_{m9} \gg \frac{1}{r_7}, \frac{1}{r_9}, \frac{1}{R_B}, \frac{1}{R_D}, \frac{1}{R_L} \end{cases} \tag{A.14}$$

Expressions for B, C, D, E are calculated next.

$$\begin{aligned} B &= r_7 \cdot r_9 \cdot x_1 \cdot x_3 \cdot x_5 \cdot x_7 = \\ &= r_7 r_9 (y_1 + sC_D)\left[y_3 + s(C_A + C_c)\right](y_5 + sC_B)\left[\frac{1}{R_L} + s(C_c + C_L)\right] = \\ &= \frac{r_7 r_9 y_1 y_3 y_5}{R_L} + \\ &+ s \cdot r_7 r_9 \left\{ \frac{y_5}{R_L}\left[C_D y_3 + y_1(C_A + C_c)\right] + y_1 y_3 \left[\frac{C_B}{R_L} + y_5(C_c + C_L)\right]\right\} + \\ &+ s^2 \cdot r_7 r_9 \left\{ y_1 y_3 C_B (C_c + C_L) + \frac{y_5}{R_L} C_D (C_A + C_c) + [C_D y_3 + \right. \\ &\left. + y_1(C_A + C_c)]\left[\frac{C_B}{R_L} + y_5(C_c + C_L)\right]\right\} + \\ &+ s^3 \cdot r_7 r_9 \left\{ C_D(C_A + C_c)\left[\frac{C_B}{R_L} + y_5(C_c + C_L)\right] + C_B(C_c + C_L)\cdot \right. \\ &\left. \cdot [C_D y_3 + y_1(C_A + C_c)]\right\} + \\ &+ s^4 \cdot r_7 r_9 C_D C_B (C_A + C_c)(C_c + C_L) \end{aligned} \tag{A.15}$$

$$\begin{aligned} C &= s \cdot C_c r_7 r_9 x_1 x_5 x_6 = s \cdot C_c r_7 r_9 (y_1 + s \cdot C_D)(y_5 + s \cdot C_B)(g_{m5} - s \cdot C_c) = \\ &= s \cdot C_c r_7 r_9 \left[y_1 y_5 g_{m5} + s \cdot (g_{m5} y_5 C_D + g_{m5} y_1 C_B - y_1 y_5 C_c) + \right. \\ &\left. + s^2 \cdot (g_{m5} C_D C_B - y_5 C_c C_D - y_1 C_B C_c) - s^3 \cdot C_c C_D C_B\right] \end{aligned} \tag{A.16}$$

$$\begin{aligned} D &= r_7 x_2 x_5 x_7 = r_7 x_2 (y_5 + s \cdot C_B)\left[\frac{1}{R_L} + s \cdot (C_c + C_L)\right] = \\ &= r_7 x_2 \left\{ \frac{y_5}{R_L} + s \cdot \left[\frac{C_B}{R_L} + y_5(C_c + C_L)\right] + s^2 \cdot C_B (C_c + C_L)\right\} \end{aligned} \tag{A.17}$$

$$\begin{aligned} E &= r_9 x_1 x_4 x_7 = r_9 x_4 (y_1 + s \cdot C_D)\left[\frac{1}{R_L} + s \cdot (C_c + C_L)\right] = \\ &= r_9 x_4 \left\{ \frac{y_1}{R_L} + s \cdot \left[\frac{C_D}{R_L} + y_1(C_c + C_L)\right] + s^2 \cdot C_D (C_c + C_L)\right\} \end{aligned} \tag{A.18}$$

Coefficient a_0 is found through the frequency-independent terms in B, C, D, E:

$$\begin{aligned} a_0 &= r_7 r_9 \frac{y_1 y_3 y_5}{R_L} - \frac{r_7 x_2 y_5}{R_L} - \frac{r_9 x_4 y_1}{R_L} = \\ &= \frac{r_7 r_9}{R_L}\left(\frac{1}{R_D}+\frac{1}{r_9}+g_{m9}\right)\left(\frac{1}{r_7}+\frac{1}{r_9}\right)\left(\frac{1}{R_B}+\frac{1}{r_7}+g_{m7}\right)+ \\ &- \frac{r_7}{R_L}\left(\frac{1}{r_9}+g_{m9}\right)\left(\frac{1}{R_B}+\frac{1}{r_7}+g_{m7}\right)+ \\ &- \frac{r_9}{R_L}\left(\frac{1}{r_7}+g_{m7}\right)\left(\frac{1}{R_D}+\frac{1}{r_9}+g_{m9}\right) \end{aligned} \tag{A.19}$$

Expanding all the terms in the last line of equation A.19, and simplifying with the help of system A.14 gives:

$$a_0 \approx \frac{g_{m9} r_9 R_D + g_{m7} r_7 R_B}{R_B R_D R_L} \tag{A.20}$$

Now the low-frequency gain A_0 of the amplifier can be calculated:

$$A_0 = \frac{b_0}{a_0} \approx g_{m1} g_{m5} (g_{m7} r_7 R_B || g_{m9} r_9 R_D) R_L \tag{A.21}$$

The terms in B, C, D, E which depend linearly on the frequency give coefficient a_1:

$$\begin{aligned} a_1 = r_7 r_9 &\left\{ \frac{y_5}{R_L}\left[C_D y_3 + y_1(C_A + C_c)\right] + y_1 y_3 \left[\frac{C_B}{R_L} + y_5(C_c + C_L)\right]\right\} + \\ &+ r_7 r_9 C_c y_1 y_5 g_{m5} - r_7 x_2 \left[\frac{C_B}{R_L} + y_5(C_c + C_L)\right] - r_9 x_4 \left[\frac{C_D}{R_L} + y_1(C_c + C_L)\right] \end{aligned} \tag{A.22}$$

All terms are expanded, simplifyed with system A.14, and then approximated with system A.24:

$$\begin{aligned} a_1 &\cong \frac{g_{m7} r_7}{R_L} C_D + \frac{g_{m7} r_9}{R_L} + \frac{g_{m7} g_{m9} r_7 r_9}{R_L}(C_A + C_c) + g_{m9} r_9 \frac{C_B}{R_L} + \\ &+ g_{m5} g_{m7} g_{m9} r_7 r_9 C_c - g_{m7} r_9 \frac{C_D}{R_L} \\ &\approx g_{m5} g_{m7} g_{m9} r_7 r_9 C_c \end{aligned} \tag{A.23}$$

$$\begin{cases} C_A \approx C_B \approx C_D \\ C_c \approx C_L \\ C_A, C_B, C_D < C_c, C_L \\ g_{m7} r_7 \approx g_{m9} r_9 \approx g_{m5} r_7 : \ big \\ g_{m9} r_9 C_A, g_{m9} r_9 C_B > C_c \end{cases} \tag{A.24}$$

Since the non-dominant poles p_2, p_3, p_4 are at frequencies much higher than p_1, the dominant pole p_1 is calculated:

$$p_1 = -\frac{a_0}{a_1} \cong -\frac{g_{m7} r_7 R_B + g_{m9} r_9 R_D}{g_{m7} r_7 R_B \cdot g_{m9} r_9 R_D} \cdot \frac{1}{g_{m5} C_c R_L} \tag{A.25}$$

Therefore the gain-bandwidth product GBW is:

$$\begin{aligned} GBW = A_0 \cdot |p_1| = g_{m1} g_{m5} (g_{m7} r_7 R_B || g_{m9} r_9 R_D) R_L \cdot \\ \cdot \frac{g_{m7} r_7 R_B + g_{m9} r_9 R_D}{g_{m7} r_7 R_B g_{m9} r_9 R_D} \cdot \frac{1}{g_{m5} C_c R_L} = \frac{g_{m1}}{C_c} \end{aligned} \tag{A.26}$$

Coefficients a_2, a_3, a_4 are also calculated from the corresponding terms in B, C, D, E:

$$\begin{aligned} a_2 = r_7 r_9 \Bigg\{ y_1 y_3 C_B (C_c + C_L) + \frac{y_5}{R_L} C_D (C_A + C_c) + [C_D y_3 + y_1 (C_A + C_c)] \cdot \\ \cdot \left[\frac{C_B}{R_L} + y_5 (C_c + C_L) \right] \Bigg\} + r_7 r_9 C_c (g_{m5} y_5 C_D + g_{m5} y_1 C_B - y_1 y_5 C_c) + \\ - r_7 x_2 C_B (C_c + C_L) - r_9 x_4 C_D (C_c + C_L) \cong \\ \cong r_9 g_{m9} C_B (C_c + C_L) + r_7 r_9 \frac{g_{m7}}{R_L} C_D (C_A + C_c) + r_7 \frac{C_D C_B}{R_L} + r_9 \frac{C_D C_B}{R_L} + \\ + r_7 r_9 g_{m9} \frac{C_B}{R_L} (C_A + C_c) + g_{m7} r_7 C_D (C_c + C_L) + g_{m7} g_{m9} r_7 r_9 C_A C_c + \\ + g_{m7} g_{m9} r_7 r_9 C_L C_c + g_{m7} g_{m9} r_7 r_9 C_A C_L + g_{m7} g_{m9} r_7 r_9 C_D C_c + \\ + g_{m7} g_{m9} r_7 r_9 C_B C_c \approx + g_{m7} g_{m9} r_7 r_9 (C_A C_c + C_L C_c + C_A C_L + C_D C_c + \\ + C_B C_c) \approx + g_{m7} g_{m9} r_7 r_9 C_c C_L \end{aligned} \tag{A.27}$$

where the first approximation is due to A.14, while the others are due to

A.24.

$$
\begin{aligned}
a_3 = {} & r_7 r_9 \left\{ C_D(C_A + C_c) \left[\frac{C_B}{R_L} + y_5(C_c + C_L) \right] + C_B(C_c + C_L) \left[C_D y_3 + \right. \right. \\
& \left. \left. y_1(C_A + C_c) \right] \right\} + r_7 r_9 C_c (g_{m5} C_D C_B - y_5 C_c C_D - y_1 C_B C_c) \cong \\
\cong {} & r_7 r_9 \left[\frac{C_B C_D}{R_L}(C_A + C_c) + gm7 C_D C_A C_c + g_{m7} C_D C_L C_c + g_{m7} C_D C_A C_L + \right. \\
& + \left(\frac{1}{r_7} + \frac{1}{r_9} \right) C_B C_D (C_c + C_L) + g_{m9} C_B C_A C_c + g_{m9} C_A C_B C_L + \\
& g_{m9} C_B C_L C_c + g_{m5} C_B C_D C_c \left. \right] \approx \\
\approx {} & r_7 r_9 \left[C_c C_L (g_{m7} C_D + g_{m9} C_B) + C_c (G_{m7} C_D C_A + g_{m9} C_A C_B + \right. \\
& \left. + g_{m5} C_B C_D) + C_L (g_{m7} C_A C_D + g_{m9} C_A C_B) \right] \approx r_7 r_9 C_c C_L (g_{m7} C_D + g_{m9} C_B)
\end{aligned}
\tag{A.28}
$$

Again, the first approximation is due to A.14, while the others are due to A.24.

$$
\begin{aligned}
a_4 = {} & r_7 r_9 C_D C_B (C_A + C_c)(C_c + C_L) + r_7 r_9 C_B C_D C_c^2 \approx \\
\approx {} & r_7 r_9 C_B C_D C_c (2C_c + C_L)
\end{aligned}
\tag{A.29}
$$

Non-dominant poles p_2, p_3, p_4 are the solutions to:

$$a_1 + a_2 s + a_3 s^2 + a_4 s^3 = 0 \tag{A.30}$$

If p_3 and p_4 are sent at much higher frequencies than p_2, then p_2 can be calculated as:

$$p_2 \cong -\frac{a_1}{a_2} \cong -\frac{g_{m7} g_{m9} g_{m5} C_c}{g_{m7} g_{m9} C_L} = -\frac{g_{m5}}{C_L} \tag{A.31}$$

The remaining second-order equation is:

$$a_2 + a_3 s + a_4 s^2 = 0 \tag{A.32}$$

The discriminant of this equation will be probably negative, and quite small. Therefore, the amplitudes of the complex conjugate poles p_3 and p_4 are approximated as:

$$|p_{3,4}| \cong \sqrt{\frac{a_2}{a_4}} = \sqrt{\frac{g_{m7} g_{m9} C_L}{2 C_B C_D (C_c + C_L)}} \tag{A.33}$$

A.2 Compensation on the cascoded load

The amplifier with compensation on the cascoded current load is in figure A.3. Figure A.4 is the equivalent small-signal model.

Kirchhoff's laws applied to this small-signal model produce system A.34.

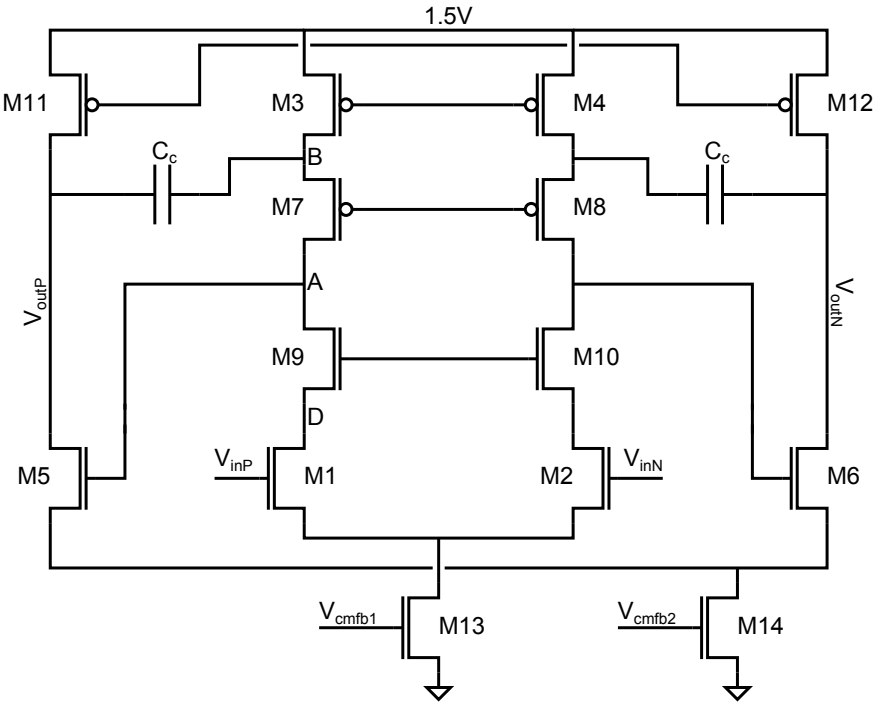

Figure A.3: Schematic of the amplifier compensated on the current load.

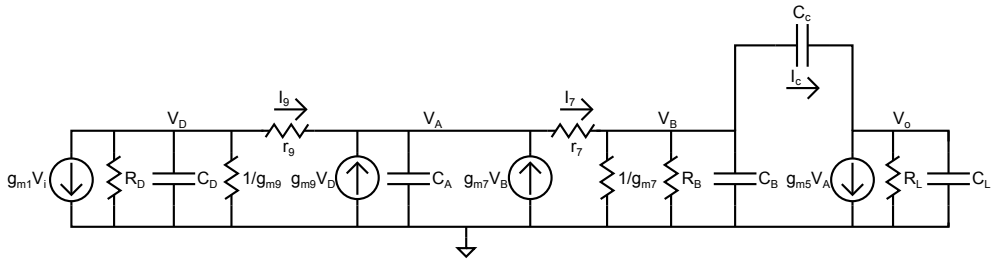

Figure A.4: Small-signal model of the amplifier compensated on the current load.

$$\begin{cases} g_{m1} \cdot V_i + \frac{V_D}{R_D} + s \cdot C_D \cdot V_D + V_D \cdot g_{m9} + I_9 = 0 \\ I_9 = \frac{V_D - V_A}{r_9} \\ I_c = \frac{V_B - V_o}{s \cdot C_c} \\ I_9 + g_{m9} \cdot V_D + g_{m7} \cdot V_B = \frac{V_A}{R_A} + s \cdot C_A \cdot V_A + I_7 \\ I_7 = \frac{V_A - V_B}{r_7} \\ I_7 = V_B \cdot g_{m7} + \frac{V_B}{R_B} + V_B \cdot s \cdot C_B + I_c \\ I_c = g_{m5} \cdot V_A + s \cdot C_L \cdot V_o + \frac{V_o}{R_L} \end{cases} \tag{A.34}$$

The transfer function of this amplifier is:

$$\frac{V_o}{V_i} = \frac{A}{B + C - D} = \frac{b_0 \cdot N(s)}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4} \tag{A.35}$$

where expressions A, B, C, D are given in system A.36.

$$\begin{cases} A = r_9 g_{m1} x_2 (r_7 x_8 g_{m5} - s \cdot C_c) \\ B = r_9 x_4 (y_1 + s \cdot C_D)(s \cdot C_c r_7 g_{m5} - x_9) \\ C = r_7 x_8 (s \cdot C_c r_7 g_{m5} - x_9) \left[x_2 - r_9 (y_1 + s \cdot C_D)(y_3 + s \cdot C_A) \right] \\ D = s \cdot C_c r_7 (r_7 x_8 g_{m5} - s \cdot C_c) \left[x_2 - r_9 (y_1 + s \cdot C_D)(y_3 + s \cdot C_A) \right] \end{cases} \tag{A.36}$$

Expressions $x_1 \ldots x_{10}$, y_1, y_3, y_5 have the same form as in systems A.2 and A.4.

Expanding the expression for A:

$$A = r_9 g_{m1} \left(\frac{1}{r_9} + g_{m9} \right) \left\{ r_7 g_{m5} \left[\frac{1}{r_7} + g_{m7} + \frac{1}{R_B} + s(C_c + C_B) \right] - s C_c \right\} \cong$$
$$\cong r_9 g_{m9} g_{m1} \left\{ r_7 g_{m7} g_{m5} + s \left[r_7 g_{m5} (C_c + C_B) - C_c \right] \right\} \tag{A.37}$$

Therefore:

$$b_0 \cong g_{m1} \cdot g_{m5} \cdot r_7 g_{m7} \cdot r_9 g_{m9} \tag{A.38}$$

Since expression A is linear with the frequency, only one zero z_1 exists; it is calculated from A.37, setting $A = 0$:

$$z_1 = -\frac{r_7 g_{m7} g_{m5}}{r_7 g_{m5} (C_c + C_B) - C_c} \approx -\frac{g_{m7}}{C_c + C_B} \tag{A.39}$$

where the approximation is based on conditions A.24.

Expressions for B, C, D:

$$\begin{aligned} B &= r_9 x_4 (y_1 + s C_D)(s C_c r_7 g_{m5} - x_9) = \\ &= -r_9 x_4 \frac{y_1}{R_L} + s r_9 x_4 \left\{ y_1 \left[C_c (r_7 g m 5 - 1) - C_L \right] - \frac{C_D}{R_L} \right\} + \\ &+ s^2 r_9 x_4 C_D \left[C_c (r_7 g_{m5} - 1) - C_L \right] \end{aligned} \tag{A.40}$$

$$
\begin{aligned}
C &= r_7\left[y_5+s(C_c+C_B)\right]\left[sC_cr_7g_{m5}-\frac{1}{R_L}-s(C_c+C_L)\right]\cdot\\
&\cdot\left[x_2-r_9(y_1+sC_D)(y_3+sC_A)\right]=\\
&= r_7\left(-\frac{y_5}{R_L}\right)(x_2-r_9y_1y_3)+sr_7\frac{y_5r_9}{R_L}(y_3C_D+y_1C_A)+\\
&+sr_7(x_2-r_9y_1y_3)\left\{y_5\left[C_c(r_7g_{m5}-1)-C_L\right]-\frac{1}{R_L}(C_c+C_B)\right\}+\\
&+s^2r_7(x_2-r_9y_1y_3)(C_c+C_B)\left[C_c(r_7g_{m5}-1)-C_L\right]+s^2r_7\frac{r_9y_5C_AC_D}{R_L}+\\
&-s^2r_7r_9(y_3C_D+y_1C_A)\left\{y_5\left[C_c(r_7g_{m5}-1)-C_L\right]-\frac{1}{R_L}(C_c+C_B)\right\}+\\
&-s^3r_7r_9C_AC_D\left\{y_5\left[C_c(r_7g_{m5}-1)-C_L\right]-\frac{1}{R_L}(C_c+C_B)\right\}+\\
&-s^3r_7r_9(y_3C_D+y_1C_A)(C_c+C_B)\left[C_c(r_7g_{m5}-1)-C_L\right]+\\
&-s^4r_7r_9C_AC_D(C_c+C_B)\left[C_c(r_7g_{m5}-1)-C_L\right]
\end{aligned}
\tag{A.41}
$$

$$
\begin{aligned}
D &= sC_cr_7\left\{r_7g_{m5}\left[y_5+s(C_c+C_B)\right]-sC_c\right\}\left[x_2-r_9(y_1+sC_D)(y_3+sC_A)\right]=\\
&= sC_cr_7^2g_{m5}y_5(x_2-r_9y_1y_3)+s^2C_cr_7\left\{(x_2-r_9y_1y_3)\left[(r_7g_{m5}-1)C_c+\right.\right.\\
&\left.\left.+r_7g_{m5}C_B\right]-r_9(y_3C_D+y_1C_A)r_7g_{m5}y_5\right\}+\\
&-s^3C_cr_7\left\{r_9C_DC_Ar_7g_{m5}y_5+r_9(y_3C_D+y_1C_A)\left[(r_7g_{m5}-1)+r_7g_{m5}C_B\right]\right\}+\\
&-s^4C_cr_7r_9C_DC_A\left[(r_7g_{m5}-1)+r_7g_{m5}C_B\right]
\end{aligned}
\tag{A.42}
$$

The coefficient a_0 can be found through the frequency-independent terms in B, C, D:

$$
\begin{aligned}
a_0 &= -r_9x_4\frac{y_1}{R_L}-r_7\frac{y_5}{R_L}(x_2-r_9y_1y_3)=\\
&= -\frac{r_9}{R_L}\left(g_{m7}+\frac{1}{r_7}\right)\left(\frac{1}{R_D}+\frac{1}{r_9}+g_{m9}\right)-\frac{r_7}{R_L}\left(g_{m7}+\frac{1}{r_7}+\frac{1}{R_B}\right)\\
&\cdot\left[\left(\frac{1}{r_9}+g_{m9}\right)-r_9\left(\frac{1}{R_D}+\frac{1}{r_9}+g_{m9}\right)\left(\frac{1}{r_7}+\frac{1}{r_9}\right)\right]\cong\\
&\cong\frac{1}{R_L}\frac{r_7g_{m7}R_B+r_7+r_9+r_9g_{m9}R_D}{R_BR_D}\cong\frac{r_7g_{m7}R_B+r_9g_{m9}R_D}{R_LR_BR_D}
\end{aligned}
\tag{A.43}
$$

The low-frequency gain A_0 of the amplifier is given by:

$$
A_0=\frac{b_0}{a_0}\cong g_{m1}g_{m5}(g_{m7}r_7R_B||g_{m9}r_9R_D)R_L \tag{A.44}
$$

The terms in B, C, D which depend linearly on the frequency give coefficient a_1:

$$\begin{aligned} a_1 = {} & r_9 x_4 \left\{ y_1 \left[C_c(r_7 g_{m5} - 1) - C_L \right] - \frac{C_D}{R_L} \right\} + \\ & + r_7 y_5 \frac{r_9}{R_L}(y_3 C_D + y_1 C_A) + r_7(x_2 - r_9 y_1 y_3) \left\{ y_5 \left[C_c(r_7 g_{m5} - 1) - C_L \right] + \right. \\ & \left. - \frac{1}{R_L}(C_c + C_B) \right\} - C_c r_7^2 g_{m5} y_5 (x_2 - r_9 y_1 y_3) \cong \\ & \cong r_7 g_{m7} \frac{C_D}{R_L} + r_7 g_{m7} r_9 g_{m9} \frac{C_A}{R_L} + r_9 g_{m9} \frac{C_c}{R_L} + r_9 g_{m9} \frac{C_B}{R_L} + \\ & + r_7 g_{m7} r_9 g_{m9} g_{m5} C_c \approx r_7 g_{m7} r_9 g_{m9} g_{m5} C_c \end{aligned} \tag{A.45}$$

The first approximation is based on system A.14, while the second approximation is based on system A.24.

The dominant pole p_1 is:

$$p_1 = -\frac{a_0}{a_1} \cong -\frac{g_{m7} r_7 R_B + g_{m9} r_9 R_D}{g_{m7} r_7 R_B \cdot g_{m9} r_9 R_D \cdot g_{m5} C_c R_L} \tag{A.46}$$

Therefore the gain-bandwidth product GBW is:

$$\begin{aligned} GBW = A_0 \cdot |p_1| = g_{m1} g_{m5} (g_{m7} r_7 R_B || g_{m9} r_9 R_D) R_L \cdot \\ \cdot \frac{g_{m7} r_7 R_B + g_{m9} r_9 R_D}{g_{m7} r_7 R_B g_{m9} r_9 R_D} \cdot \frac{1}{g_{m5} C_c R_L} = \frac{g_{m1}}{C_c} \end{aligned} \tag{A.47}$$

Coefficients a_2, a_3, a_4 are also calculated from the corresponding terms

in B, C, D:

$$\begin{aligned}
a_2 &= r_9 x_4 C_D \left[C_c(r_7 g_{m5} - 1) - C_L\right] + r_7(x_2 - r_9 y_1 y_3)(C_c + C_B)\cdot \\
&\cdot \left[C_c(r_7 g_{m5} - 1) - C_L\right] + \frac{r_7 r_9 y_5 C_A C_D}{R_L} + \\
&- r_7 r_9 (y_3 C_D + y_1 C_A)\left\{y_5\left[C_c(r_7 g_{m5} - 1) - C_L\right] - \frac{1}{R_L}(C_c + C_B)\right\} + \\
&- C_c r_7 \left\{(x_2 - r_9 y_1 y_3)\left[(r_7 g_{m5} - 1)C_c + r_7 g_{m5} C_B\right] + \right. \\
&\left. - r_9 (y_3 C_D + y_1 C_A) r_7 g_{m5} y_5\right\} \cong \\
&\cong r_9 g_{m9}(C_c C_B + C_c C_L + C_B C_L) + \frac{r_7 r_9 g_{m7} C_A C_D}{R_L} + \\
&+ r_7 g_{m7}(C_c C_D + C_D C_L) + r_7 r_9 g_{m7} g_{m9}(C_c C_A + C_L C_A) + \\
&+ \frac{r_7 C_c C_D + r_9 C_c C_D + r_7 r_9 g_{m9}(C_A C_c + C_A C_B) + r_7 C_B C_D + r_9 C_B C_D}{R_L} + \\
&r_7 r_9 g_{m5} g_{m7} C_D C_c \approx r_9 g_{m9} C_c C_L + r_7 g_{m7} C_D (C_c + C_L) + \\
&+ r_7 r_9 g_{m7} g_{m9} C_A (C_c + C_L) + r_7 r_9 g_{m5} g_{m7} C_D C_c + \\
&+ \frac{(r_7 + r_9)(C_c + C_B) C_D + r_7 r_9 g_{m9} C_A (C_c + C_B)}{R_L} \approx \\
&\approx r_7 r_9 g_{m7} g_{m9} C_A (C_c + C_L)
\end{aligned} \tag{A.48}$$

where the first approximation is due to A.14, while the others are due to A.24.

$$\begin{aligned}
a_3 &= -r_7 r_9 C_A C_D \left\{y_5\left[C_c(r_7 g_{m5} - 1) - C_L\right] - \frac{1}{R_L}(C_c + C_B)\right\} + \\
&- r_7 r_9 (y_3 C_D + y_1 C_A)(C_c + C_B)\left[C_c(r_7 g_{m5} - 1) - C_L\right] + \\
&+ r_7 C_c \left\{r_9 C_D C_A r_7 g_{m5} y_5 + r_9 (y_3 C_D + y_1 C_A)\left[(r_7 g_{m5} - 1)C_c + r_7 g_{m5} C_B\right]\right\} \\
&\cong r_7 r_9 g_{m7} C_A C_D (C_c + C_L) + \frac{r_7 r_9}{R_L} C_A C_D (C_c + C_B) + (r_7 + r_9) C_D C_L C_c + \\
&+ (r_7 + r_9) C_B C_D (C_c + C_L) + r_7 r_9 g_{m9} C_A (C_L C_c + C_B C_c + C_B C_L) \approx \\
&\approx r_7 r_9 g_{m9} C_A (C_L C_c + C_B C_c + C_B C_L)
\end{aligned} \tag{A.49}$$

again, the first approximation is due to A.14, while the others are due to A.24.

$$\begin{aligned}
a_4 &= -r_7 r_9 C_A C_D (C_c + C_B)\left[C_c(r_7 g_{m5} - 1) - C_L\right] + r_7 r_9 C_A C_D C_c \cdot \\
&\cdot \left[C_c(r_7 g_{m5} - 1) + r_7 g_{m5} C_B\right] = r_7 r_9 C_A C_D (C_L C_c + C_B C_c C_B C_L)
\end{aligned} \tag{A.50}$$

Non-dominant poles p_2, p_3, p_4 are the solutions to equation A.30, with the values of $a_1 \ldots a_4$ just calculated for this type of compensation. If p_3 and p_4 are sent at much migher frequencies than p_2, then p_2 can be calculated as:

$$p_2 \cong -\frac{a_1}{a_2} \cong -\frac{r_7 r_9 g_{m7} g_{m9} g_{m5} C_c}{r_7 r_9 g_{m7} g_{m9} C_A (C_c + C_L)} = -\frac{g_{m5} C_c}{C_A (C_c + C_L)} \tag{A.51}$$

The remaining second-order equation is A.32. The discriminant of this equation will be quite small. Therefore, the amplitude of the complex conjugate poles p_3, p_4 is approximated as:

$$|p_{3,4}| \cong \sqrt{\frac{a_2}{a_4}} = \sqrt{\frac{g_{m7} g_{m9} \frac{C_c + C_L}{C_c C_L}}{C_D \left(1 + \frac{C_B}{C_c || C_L}\right)}} = \sqrt{\frac{g_{m7} g_{m9}}{C_D \left[(C_c || C_L) + C_B\right]}} \tag{A.52}$$

A.3 Compensation on the cascoded input

The amplifier with compensation on the cascode of the input transistor is in figure A.5. Figure A.6 is the equivalent small-signal model.

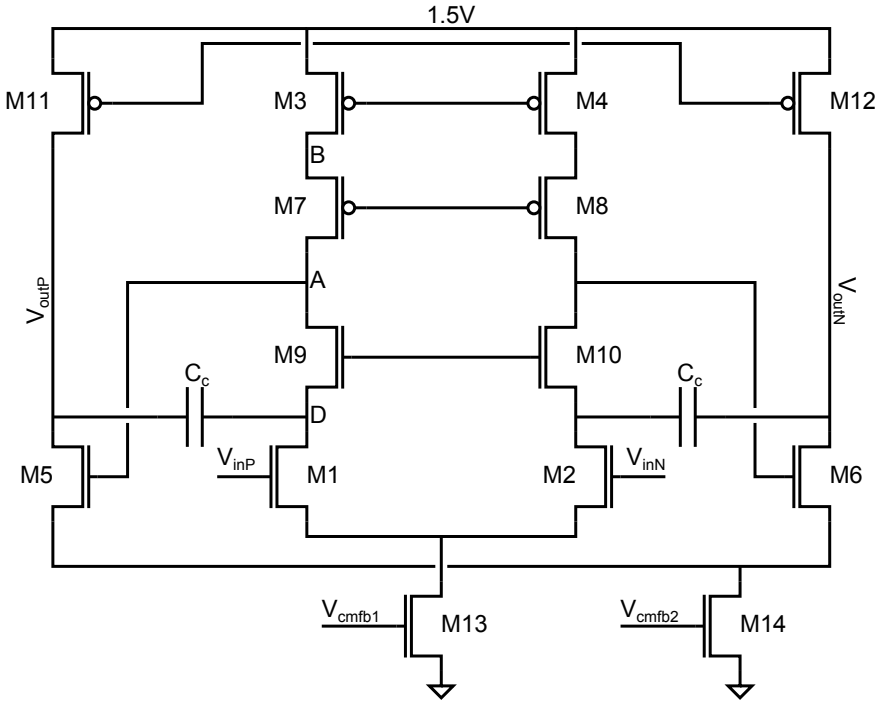

Figure A.5: Schematic of the chosen amplifier, compensated on the cascoded input transistor; copy of figure 3.9.

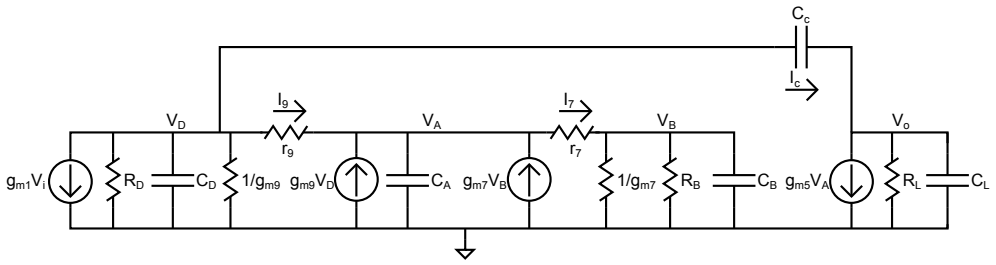

Figure A.6: Small-signal half-signal model of the chosen amplifier, copy of figure 3.10.

Kirchhoff's laws applied to this small-signal model result in system A.53.

$$\begin{cases} g_{m1} \cdot V_i + \frac{V_D}{R_D} + s \cdot C_D \cdot V_D + V_D \cdot g_{m9} + I_9 + I_c = 0 \\ I_9 = \frac{V_D - V_A}{r_9} \\ I_c = \frac{V_D - V_o}{s \cdot C_c} \\ I_9 + g_{m9} \cdot V_D + g_{m7} \cdot V_B = \frac{V_A}{R_A} + s \cdot C_A \cdot V_A + I_7 \\ I_7 = \frac{V_A - V_B}{r_7} \\ I_7 = V_B \cdot g_{m7} + \frac{V_B}{R_B} + V_B \cdot s \cdot C_B \\ I_c = g_{m5} \cdot V_A + s \cdot C_L \cdot V_o + \frac{V_o}{R_L} \end{cases} \tag{A.53}$$

The transfer function of the amplifier is:

$$\frac{V_o}{V_i} = \frac{A}{-B + C + D - E - F} = \frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4} \tag{A.54}$$

where expressions A, B, C, D, E, F are:

$$\begin{cases} A = g_{m1} \cdot r_9 \left[x_2 g_{m5} r_7 (y_5 + sC_B) + x_4 s C_c - r_7 s C_C (y_3 + sC_A)(y_5 + sC_B) \right] \\ B = r_7 \cdot x_9 \cdot x_{10} \cdot x_4 \\ C = r_9 \cdot x_9 \cdot x_{10} \cdot r_7 \cdot (y_3 + sC_A)(y_5 + sC_B) \\ D = r_9 \cdot s \cdot C_c \cdot \left[x_2 g_{m5} r_7 (y_5 + sC_B) + x_4 s C_c - r_7 s C_C (y_3 + sC_A)(y_5 + sC_B) \right] \\ E = x_2 \cdot x_9 \cdot r_7 \cdot y_5 \\ F = s \cdot C_B \cdot x_2 \cdot x_9 \cdot r_7 \end{cases} \tag{A.55}$$

Expressions $x_1 \ldots x_{10}$, y_1, y_3, y_5 are the same as in systems A.2 and A.4. Expanding the expression for A:

$$\begin{aligned} A = {} & g_{m1} g_{m5} r_7 r_9 x_2 y_5 + s \cdot g_{m1} r_9 (C_B x_2 g_{m5} r_7 + x_4 C_c - r_7 y_3 y_5 C_c) + \\ & - s^2 \cdot g_{m1} r_7 r_9 C_c (y_5 C_A + y_3 C_B) - s^3 \cdot g_{m1} r_7 r_9 C_A C_B C_C \end{aligned} \tag{A.56}$$

Therefore:

$$b_0 = g_{m1}g_{m5}r_7r_9\left(g_{m9}+\frac{1}{r_9}\right)\left(g_{m7}+\frac{1}{r_7}+\frac{1}{R_B}\right)\cong$$
$$\cong g_{m1}g_{m5}g_{m7}r_7g_{m9}r_9 \tag{A.57}$$

$$b_1 = g_{m1}r_9\left[C_B\left(g_{m9}+\frac{1}{r_9}\right)g_{m5}r_7+\left(g_{m7}+\frac{1}{r_7}\right)C_c+\right.$$
$$\left.-r_7\left(\frac{1}{r_7}+\frac{1}{r_9}\right)\left(\frac{1}{r_7}+g_{m7}+\frac{1}{R_B}\right)C_c\right]\cong$$
$$\cong g_{m1}r_7r_9\left(g_{m5}g_{m9}C_B-\frac{g_{m7}}{r_9}C_c\right) \tag{A.58}$$

$$b_2 = -g_{m1}r_7r_9C_c\left[\left(\frac{1}{r_7}+g_{m7}+\frac{1}{R_B}\right)C_A+\left(\frac{1}{r_7}+\frac{1}{r_9}\right)C_B\right]\cong$$
$$\cong -g_{m1}g_{m7}r_7r_9C_AC_c \tag{A.59}$$

$$b_3 = -g_{m1}r_7r_9C_AC_BC_c \tag{A.60}$$

Finding the zeros of A in an analytical way is not trivial. In order to simplify the problem, the effect of C_B is neglected for a while.

If $C_B = 0$ (as is the case in [HL]), the equation $A = 0$ becomes:

$$g_{m5}g_{m9} - s\cdot\frac{C_c}{r_9} - s^2\cdot C_AC_c = 0 \tag{A.61}$$

The discriminant of this second-order equation will be small, and the zeros z_1, z_2 can be approximated by:

$$z_{1,2} \cong \pm\sqrt{\frac{g_{m5}g_{m9}}{C_AC_c}} \tag{A.62}$$

At this point, C_B is considered. Since it is present in b_3, it will have effect at high frequencies; therefore, the third zero z_3 can be approximated as:

$$z_3 \cong -\frac{b_2}{b_3} = -\frac{g_{m7}}{C_B} \tag{A.63}$$

Expressions for B, C, D, E, F:

$$B = r_9\left[\frac{1}{R_L}+s\cdot(C_c+C_L)\right][y_1+s\cdot(C_c+C_D)]\,x_4 =$$
$$= \frac{r_9x_4y_1}{R_L}+s\cdot\left[r_9x_4y_1(C_c+C_L)+\frac{r_9x_4}{R_L}(C_c+C_D)\right]+$$
$$+s^2\cdot r_9x_4(C_c+C_L)(C_c+C_D) \tag{A.64}$$

$$
\begin{aligned}
C &= r_9 r_7 \left[\frac{1}{R_L} + s(C_c + C_L)\right] [y_1 + s(C_c + C_D)]\,(y_3 + sC_A)(y_5 + sC_B) = \\
&= \frac{r_7 r_9 y_1 y_3 y_5}{R_L} + \\
&+ s \cdot \left[\frac{r_7 r_9 y_3 y_5}{R_L}(C_c + C_D) + r_7 r_9 y_1 y_3 y_5 (C_c + C_L) + \right. \\
&\left. + \frac{r_7 r_9 y_1 y_5}{R_L} C_A + \frac{r_7 r_9 y_1 y_3}{R_L} C_B \right] + \\
&+ s^2 \cdot \left\{ r_7 r_9 y_3 y_5 (C_c + C_L)(C_c + C_D) + \frac{r_7 r_9 y_1}{R_L} C_A C_B + \right. \\
&\left. (y_5 C_A + y_3 C_B) \left[\frac{r_7 r_9}{R_L}(C_c + C_D) + r_7 r_9 y_1 (C_c + C_L)\right] \right\} + \\
&+ s^4 \cdot r_7 r_9 C_A C_B (C_c + C_L)(C_c + C_D)
\end{aligned} \tag{A.65}
$$

$$
\begin{aligned}
D &= s \cdot x_2 g_{m5} r_7 r_9 y_5 C_c + \\
&+ s^2 \cdot (r_7 r_9 x_2 g_{m5} C_B C_c + x_4 r_9 C_c^2 - r_7 r_9 y_3 y_5 C_c^2) + \\
&- s^3 \cdot r_7 r_9 C_c^2 (y_5 C_A + y_3 C_B) + \\
&- s^4 \cdot r_7 r_9 C_A C_B C_c^2
\end{aligned} \tag{A.66}
$$

$$
E = \frac{r_7 x_2 y_5}{R_L} + s \cdot r_7 x_2 y_5 (C_c + C_L) \tag{A.67}
$$

$$
F = s \cdot \frac{C_B x_2 r_7}{R_L} + s^2 \cdot C_B x_2 r_7 (C_c + C_L) \tag{A.68}
$$

The coefficient a_0 is calculated through the frequency-independent terms in B, C, D, E, F:

$$
\begin{aligned}
a_0 &= -\frac{r_9 x_4 y_1}{R_L} + \frac{r_7 r_9 y_1 y_3 y_5}{R_L} - \frac{r_7 x_2 y_5}{R_L} = \\
&= \frac{1}{R_L}\left(\frac{r_9}{R_B R_D} + \frac{r_9 g_{m9}}{R_B} + \frac{1}{R_B} + \frac{1}{R_D} + \frac{r_7 g_{m7}}{R_D} + \frac{r_7}{R_D R_B}\right) \cong \\
&\cong \frac{1}{R_L}\left(\frac{r_9 g_{m9}}{R_B} + \frac{r_7 g_{m7}}{R_D}\right)
\end{aligned} \tag{A.69}
$$

where the approximation is due to equations A.14.

The low-frequency gain A_0 of the amplifier is given by:

$$
A_0 = \frac{b_0}{a_0} \approx g_{m1} g_{m5} (g_{m7} r_7 R_B || g_{m9} r_9 R_D) R_L \tag{A.70}
$$

The terms in B, C, D, E, F which depend linearly on the frequency give coefficient a_1:

$$\begin{aligned} a_1 = &-r_9 x_4 y_1 (C_c + C_L) - \frac{r_9 x_4}{R_L}(C_c + C_D) + \\ &+ \left[\frac{r_7 r_9 y_3 y_5}{R_L}(C_c + C_D) + r_7 r_9 y_1 y_3 y_5 (C_c + C_L) + \frac{r_7 r_9 y_1 y_5}{R_L} C_A + \right. \\ &\left. + \frac{r_7 r_9 y_3 y_1}{R_L} C_B \right] + x_2 g_{m5} r_7 r_9 y_5 C_c - r_7 x_2 y_5 (C_c + C_L) - \frac{C_B x_2 r_7}{R_L} \end{aligned} \tag{A.71}$$

Expanding all the terms and simplifying with equations A.14:

$$\begin{aligned} a_1 = &\frac{C_c + C_D}{R_L}\left[(1 + g_{m7} r_7) + \frac{r_7 + r_9}{R_B} \right] + \\ &+ (C_c + C_L)\left[\frac{r_9}{R_B}\left(\frac{1}{R_D} + g_{m9} + \frac{1}{r_9} \right) + \frac{r_7}{R_D}\left(\frac{1}{R_B} + g_{m7} + \frac{1}{r_7} \right) \right] + \\ &+ \left(\frac{1}{R_D} + g_{m9} + \frac{1}{r_9} \right)\left(\frac{1}{R_B} + g_{m7} + \frac{1}{r_7} \right) C_A + \\ &+ \frac{C_B}{R_L}\left[\frac{r_7}{R_D} + r_9 \left(\frac{1}{R_D} + g_{m9} + \frac{1}{r_9} \right) \right] + \\ &+ \left(g_{m9} + \frac{1}{r_9} \right) g_{m5} r_7 r_9 \left(\frac{1}{R_B} + g_{m7} + \frac{1}{r_7} \right) C_c \cong \\ &\cong \frac{g_{m7} r_7}{R_L}(C_c + C_D) + \left(\frac{g_{m9} r_9}{R_B} + \frac{g_{m7} r_7}{R_D} \right)(C_c + C_L) + g_{m7} g_{m9} C_A + \\ &\frac{g_{m9} r_9}{R_L} C_B + g_{m5} g_{m7} r_7 g_{m9} r_9 C_c \cong g_{m5} g_{m7} r_7 g_{m9} r_9 C_c \end{aligned} \tag{A.72}$$

Since the non-dominant poles p_2, p_3, p_4 are at frequencies much higher than p_1, the dominant pole p_1 is calculated:

$$\begin{aligned} p_1 = -\frac{a_0}{a_1} &\cong -\frac{1}{R_L}\left(\frac{g_{m9} r_9}{R_B} + \frac{g_{m7} r_7}{R_D} \right) \frac{1}{g_{m5} g_{m7} r_7 g_{m9} r_9 C_c} = \\ &= -\frac{1}{g_{m5} C_c R_L \cdot (g_{m7} r_7 R_B || g_{m9} r_9 R_D)} \end{aligned} \tag{A.73}$$

Therefore the gain-bandwidth product GBW is:

$$\begin{aligned} GBW = A_0 \cdot |p_1| &= \frac{b_0}{a_0} \cdot \frac{a_0}{a_1} = \frac{b_0}{a_1} = \\ &= \frac{g_{m1} g_{m5} g_{m7} r_7 g_{m9} r_9}{g_{m5} g_{m7} r_7 g_{m9} r_9 \cdot C_c} = \frac{g_{m1}}{C_c} \end{aligned} \tag{A.74}$$

Coefficient a_2 is also calculated from the corresponding terms in B, C, D, E, F:

$$\begin{aligned}
a_2 &= -r_9x_4(C_c+C_L)(C_c+C_D)+r_7r_9y_3y_5(C_c+C_L)(C_c+C_D)+\\
&+\frac{r_7r_9y_1}{R_L}C_AC_B+(y_5C_A+y_3C_B)\left[\frac{r_7r_9}{R_L}(C_c+C_D)+r_7r_9y_1(C_c+C_L)\right]+\\
&+r_7r_9x_2g_{m5}C_BC_c+x_4r_9C_c^2+r_7r_9y_3y_5C_c^2-C_Bx_2r_7(C_c+C_L)=\\
&=\left(1+g_{m7}r_7+\frac{r_7+r_9}{R_B}\right)(C_cC_L+C_cC_D+C_LC_D)+\\
&+\left(x_4C_A+\frac{C_A}{R_B}\right)\left[\frac{r_7r_9}{R_L}(C_c+C_D)+r_7r_9\left(x_2+\frac{1}{R_D}\right)(C_c+C_L)\right]+\\
&+\left(\frac{C_B}{r_7}+\frac{C_B}{r_9}\right)\frac{r_7r_9}{R_L}(C_c+C_D)+\frac{C_Br_7}{R_D}(C_c+C_L)+\\
&+C_Br_9\left(\frac{1}{r_9}+g_{m9}+\frac{1}{R_D}\right)(C_c+C_L)+r_7g_{m5}C_BC_c+r_7g_{m5}r_9g_{m9}C_BC_c\cong\\
&\cong g_{m7}r_7(C_cC_L+C_cC_D+C_LC_D)+C_B\frac{r_7+r_9}{R_L}(C_c+C_D)+\\
&+g_{m7}C_A\left[\frac{r_7r_9}{R_L}(C_c+C_D)+r_7r_9g_{m9}(C_c+C_L)\right]+\frac{C_Br_7}{R_D}(C_c+C_L)+\\
&+C_Br_9g_{m9}(C_c+C_L)+r_7g_{m5}C_BC_c+r_7g_{m5}r_9g_{m9}C_BC_c\approx\\
&\approx g_{m7}r_7C_cC_L+g_{m7}r_7g_{m9}r_9C_A(C_c+C_L)+g_{m5}r_7g_{m9}r_9C_BC_c
\end{aligned}\tag{A.75}$$

where the first approximation is due to A.14. The other approximation is due to A.24, which suggest also that the first term ($g_{m7}r_7C_cC_L$) is non-dominant. Therefore:

$$a_2\approx g_{m9}r_9r_7(g_{m7}C_AC_c+g_{m7}C_AC_L+g_{m5}C_BC_c)\tag{A.76}$$

If the first non-dominant pole p_2 is at lower frequencies than the other poles p_3 and p_4, it is approximated as:

$$p_2\cong-\frac{a_1}{a_2}=-\frac{g_{m5}g_{m7}C_c}{g_{m7}C_A(C_c+C_L)+g_{m5}C_BC_c}\tag{A.77}$$

It is interesting to write simplified equations for p_2 in the two cases when $C_B=0$ (as if the current load was not cascoded) and when C_B dominates in equation A.77:

$$C_B=0\Rightarrow\qquad p_2=-\frac{g_{m5}}{C_c+C_L}\cdot\frac{C_c}{C_A}\tag{A.78}$$

$$C_B\ dominant\Rightarrow\qquad p_2=-\frac{g_{m7}}{C_B}\tag{A.79}$$

Term a_3 is calculated in a similar way with B, C, D, E, F:

$$\begin{aligned}
a_3 &= r_7 r_9 (C_c + C_L)(C_c + C_D)(y_5 C_A + y_3 C_B) + \\
&+ C_A C_B \left[\frac{r_7 r_9}{R_L} (C_c + C_D) + r_7 r_9 y_1 (C_c + C_L) \right] - r_7 r_9 C_c^2 (y_5 C_A + y_3 C_B) \cong \\
&\cong r_7 r_9 (C_c C_L + C_L C_D + C_c C_D) \left(g_{m7} C_A + \frac{1}{r_7} C_B + \frac{1}{r_9} C_B \right) + \\
&+ C_A C_B r_7 r_9 \left[\frac{C_c}{R_L} + \frac{C_D}{R_L} + g_{m9} (C_c + C_L) \right] \approx \\
&\approx r_7 r_9 \left[g_{m7} C_A (C_c C_L + C_L C_D + C_c C_D) + \right. \\
&\left. + C_A C_B \left(\frac{C_c}{R_L} + \frac{C_D}{R_L} + g_{m9} C_c + g_{m9} C_L \right) \right] \approx \\
&\approx r_7 r_9 C_A \left\{ g_{m7} \left[C_c C_L + C_D (C_c + C_L) \right] + g_{m9} C_B (C_c + C_L) \right\} = \\
&= r_7 r_9 C_A (C_c + C_L) \left\{ g_{m7} \left[(C_c || C_L) + C_D \right] + g_{m9} C_B \right\}
\end{aligned} \tag{A.80}$$

again, the first approximation is due to A.14, while the others are due to A.24.

If p_3 is clearly distinguished from p_4:

$$p_3 \cong -\frac{a_2}{a_3} = -\frac{g_{m9} \left[g_{m7} C_A (C_c + C_L) + g_{m5} C_B C_c \right]}{C_A \left\{ g_{m7} \left[(C_c || C_L) + C_D \right] + g_{m9} C_B \right\}} \tag{A.81}$$

Also here, p_3 is calculated in the two cases when $C_B = 0$, and when C_B dominates:

$$C_B = 0 \Rightarrow \qquad p_3 = -\frac{g_{m9}}{(C_c || C_L) + C_D} \tag{A.82}$$

$$C_B \; dominant \Rightarrow \qquad p_3 = -\frac{g_{m5}}{C_c + C_L} \cdot \frac{C_c}{C_A} \tag{A.83}$$

Eventually, a_4 is calculated:

$$\begin{aligned}
a_4 &= r_7 r_9 C_A C_B (C_c + C_L)(C_c + C_D) - r_7 r_9 C_A C_B C_c^2 = \\
&= r_7 r_9 C_A C_B (C_c + C_L) \left[(C_c || C_L) + C_D \right]
\end{aligned} \tag{A.84}$$

The last pole p_4 is:

$$p_4 \cong -\frac{a_3}{a_4} = -\frac{g_{m7} \left[(C_c || C_L) + C_D \right] + g_{m9} C_B}{C_B \left[(C_c || C_L) + C_D \right]} \tag{A.85}$$

Again, p_4 is evaluated in the two cases:

$$C_B = 0 \Rightarrow \qquad p_4 = -\frac{g_{m7}}{C_B} \tag{A.86}$$

$$C_B \; dominant \Rightarrow \qquad p_4 = -\frac{g_{m9}}{(C_c || C_L) + C_D} \tag{A.87}$$

Appendix B

Verilog-AMS models

B.1 PASA

```
‘include "constants.vams"
‘include "disciplines.vams"

module Pasa1ch ( Gnd, SupplyP, VOutP, VOutN, BiasDecay, gain1, gain2,
in, polarity, PreampEn, sh1, sh2, sh3, shutdown, substrate );

  inout substrate;
  inout sh3;
  inout gain2;
  inout Gnd;
  inout in;
  inout BiasDecay;
  inout shutdown;
  inout sh2;
  inout SupplyP;
  inout VOutN;
  inout VOutP;
  inout sh1;
  inout PreampEn;
  inout polarity;
  inout gain1;

electrical in, VOutP, VOutN;
electrical Gnd, SupplyP, BiasDecay, gain1, gain2, polarity, PreampEn,
sh1, sh2, sh3, shutdown, substrate;
```

```
electrical PreampOut, PZOut, OutInt1, OutInt2, OutSe;

branch (in, PreampOut) cap, res;
parameter Cf=0.8E-12; // integrating capacitor
parameter Rs=1E6;     // feedback resistance
parameter real DcI=0.2;    // DC input level of the preamplifier
parameter Rpz=Rs/14;
parameter Cpz=Cf*14;
parameter R1=1200;    // series resistance of the pole-zero
                      // cancellation network
parameter G=15;       // DC gain of the T-bridged amplifiers
parameter pi=3.14;
parameter pa=2*pi*10E6; // one pole of the shapers (radians)
parameter pb=2*pi*30E6; // one pole of the shapers (radians)
parameter BaselineP=1.170; // DC level of the positive output
parameter BaselineN=0.330; // DC level of the negative output
analog begin
 I(cap) <+ Cf*ddt(V(cap));
 V(res) <+ Rs*I(res);
 V(PreampOut) <+ -10E3*(V(in)-DcI);
 V(PZOut) <+ R1*( ((V(PreampOut)-V(PZOut))/Rpz) +
                Cpz*ddt(V(PreampOut)-V(PZOut)) );
 V(OutInt1) <+ V(PZOut)-(1/pa)*ddt(V(OutInt1));
 V(OutInt2) <+ V(OutInt1)-(1/pb)*ddt(V(OutInt2));
 V(OutSe) <+ G*V(OutInt2);
 if (V(polarity)>0.75) begin
  V(VOutP) <+ BaselineN+V(OutSe);
  V(VOutN) <+ BaselineP-V(OutSe);
 end else begin
  V(VOutP) <+ BaselineP+V(OutSe);
  V(VOutN) <+ BaselineN-V(OutSe);
 end
end

endmodule
```

B.2 ADC

B.2.1 ADC 1.5bit Stage

```
‘include "constants.vams"
‘include "disciplines.vams"

module RegularStage1b5  ( LSB, MSB, OutP, OutN, VCM, VddA, VddD,
GndA, GndD, BiasCM, BiasGE1N, BiasGE1P, BiasGE2N, BiasGE2P,
BiasStage1, BiasStage2, CmOut, SwiftReg, clk1, clk1d, clk1di,
clk1dd, clk1ddi, clk2, clk2d, clk2di, clk2dd, clk2ddi, InP, InN,
Latch, RefP, RefN, Substrate, SubBFBuffer, SubBFAdc );

  input BiasStage1;
  inout VddD;
  inout GndD;
  input CmOut;
  inout GndA;
  input BiasCM;
  inout VddA;
  input RefP;
  input clk2;
  input clk1d;
  input BiasGE1P;
  input BiasStage2;
  inout VCM;
  input clk1di;
  input clk2di;
  input BiasGE1N;
  input clk1dd;
  input RefN;
  input clk2ddi;
  input clk1ddi;
  input BiasGE2P;
  input SwiftReg;
  input clk2dd;
  input BiasGE2N;
  input clk2d;
  input clk1;
  inout Substrate;
  inout SubBFAdc;
```

```
  inout SubBFBuffer;

electrical VCM, VddA, VddD, GndA, GndD,
BiasCM, BiasGE1N, BiasGE1P, BiasGE2N, BiasGE2P, BiasStage1,
BiasStage2, CmOut, SwiftReg, clk1, clk1d, clk1di, clk1dd, clk1ddi,
clk2, clk2d, clk2di, clk2dd, clk2ddi, RefP, RefN, Substrate,
SubBFBuffer, SubBFAdc;

input Latch;
wire LatchF;
output LSB, MSB;
reg LSB, MSB;
input InP, InN;
electrical InP, InN, Latch;
output OutP, OutN;
electrical OutP, OutN;
parameter real ThrP=0.250;
parameter real ThrN=-0.250;
parameter real Vcm=0.750;
parameter real FullScale=1;
real OutPR, OutNR;

Clk2AMS LatchA2D (
.Clk (Latch),
.ClkI (LatchF)
);

always @ (posedge (LatchF)) begin
       if (V(InP, InN)>ThrP) begin
                LSB<=1'b0;
                MSB<=1'b1;
                OutPR<=Vcm+2*(V(InP)-Vcm)-FullScale/2;
                OutNR<=Vcm+2*(V(InN)-Vcm)+FullScale/2;
        end else if (V(InP, InN)<ThrN) begin
                LSB<=1'b0;
                MSB<=1'b0;
                OutPR<=Vcm+2*(V(InP)-Vcm)+FullScale/2;
                OutNR<=Vcm+2*(V(InN)-Vcm)-FullScale/2;
        end else begin
                LSB<=1'b1;
                MSB<=1'b0;
```

```
                OutPR<=Vcm+2*(V(InP)-Vcm);
                OutNR<=Vcm+2*(V(InN)-Vcm);
        end
end

analog begin
        V(OutP) <+ transition(OutPR);
        V(OutN) <+ transition(OutNR);
end

endmodule
```

B.2.2 Flash ADC 2bit

```
‘include "constants.vams"
‘include "disciplines.vams"

module FlashAdc2bit (Clk, InP, InN, Lsb, Msb);

input Clk;
wire Clk;
output Lsb, Msb;
reg Lsb, Msb;
input InP, InN;
electrical InP, InN;
parameter real ThrP=0.5;
parameter real ThrN=-0.5;

always @ (posedge (Clk)) begin
       if (V(InP, InN)>ThrP) begin
                Lsb<=1’b1;
                Msb<=1’b1;
        end else if (V(InP, InN)<ThrN) begin
                Lsb<=1’b0;
                Msb<=1’b0;
end else if (V(InP, InN)>0) begin
Lsb<=1’b0;
                Msb<=1’b1;
        end else begin
                Lsb<=1’b1;
                Msb<=1’b0;
```

```
        end
end

endmodule
```

B.3 Clock Tree

```
‘timescale 1ns/10ps
‘include "constants.vams"
‘include "disciplines.vams"

module ClockTree ( ClkOut0, ClkOut1, ClkOut2, ClkOut3, ClkOut4,
ClkOut5, ClkOut6, ClkOut7, ClkOut8, ClkOut9, ClkOut10, ClkOut11,
ClkOut12, ClkOut13, ClkOut14, ClkOut15, ClkOutD, GndD, VddD, ClkIn,
ClkSelect, ClkAux, Substrate );

  output ClkOut7;
  output ClkOut14;
  output ClkOut11;
  output ClkOut8;
  output ClkOut5;
  output ClkOut3;
  output ClkOut2;
  output ClkOut0;
  input ClkIn;
  inout VddD;
  output ClkOutD;
  inout GndD;
  output ClkOut6;
  output ClkOut4;
  output ClkOut13;
  output ClkOut12;
  output ClkOut1;
  output ClkOut10;
  output ClkOut15;
  output ClkOut9;
  inout ClkSelect, ClkAux, Substrate;

electrical ClkOut0, ClkOut1, ClkOut2, ClkOut3, ClkOut4, ClkOut5,
ClkOut6, ClkOut7, ClkOut8, ClkOut9, ClkOut10, ClkOut11, ClkOut12,
```

```
ClkOut13, ClkOut14, ClkOut15, GndD, VddD, ClkIn, ClkSelect, ClkAux,
Substrate;

wire ClkOutD;
electrical ClkF;

parameter integer CornerPar=1;
real DelayAdc;
real DelayDig;

initial begin
  if (CornerPar==0) begin
    DelayAdc=540p;
    DelayDig=1130p;
  end else if (CornerPar==1) begin
    DelayAdc=540p;
    DelayDig=1130p;
  end else if (CornerPar==6) begin
    DelayAdc=350p;
    DelayDig=670p;
  end else if (CornerPar==7) begin
    DelayAdc=840p;
    DelayDig=1830p;
  end
end

analog begin
V(ClkOut0) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut1) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut2) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut3) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut4) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut5) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut6) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut7) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut8) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut9) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut10) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut11) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut12) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut13) <+ absdelay(V(ClkIn), DelayAdc);
```

```
V(ClkOut14) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkOut15) <+ absdelay(V(ClkIn), DelayAdc);
V(ClkF) <+ absdelay(V(ClkIn), DelayDig);

end

Clk2AMS DigitalClockA2D (
.Clk (ClkF),
.ClkI (ClkOutD)
);

endmodule
```

Appendix C

Clock Tree

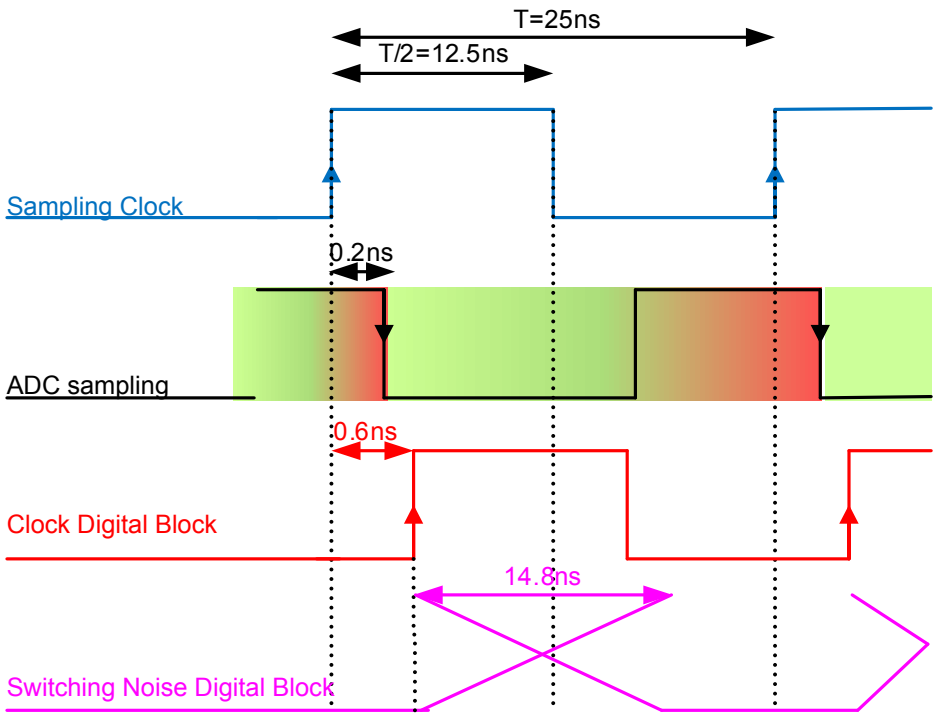

Figure C.1: Simplified clocking scheme of the ADCs and of the DSP block of the S-Altro. The most noise-sensitive period is when the ADCs sample, and shortly before (red shading); after the sampling, and for some time, noise can be tolerated, because the ADC amplifiers will have enough time to absorb the noise before the next sampling (green area). With the clock of the DSP delayed by 400ps, the digital switching logic will introduce noise only during the noise-tolerant period, as in [Bl].

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